A Technique for Reference Spur Eradication in Fractional-N Frequency Synthesis

by

Rachel Katumba, B.Sc.

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Faculty of Graduate and Postdoctoral Affairs
acceptance of the thesis

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Master of Applied Science in Electrical and Computer Engineering

Professor John W. M. Rogers, Thesis Supervisor

Professor Neil Tait, Chair,
Department of Electronics

Ottawa-Carleton Institute for Electrical and Computer Engineering
Department of Electronics
Carleton University
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Abstract

This thesis details a technique of eradicating reference spurs (in theory). It involves a Fixed Width Variable Amplitude Charge Pump (FWVACP) which is inherently insensitive to current mismatch. Charge pump current pulses are modified such that they have a fixed width and occur on the falling edge of the reference signal. Phase error information is embedded in the amplitude of the current pulses. The periodic nature of these pulses creates nulls at integer multiples of the reference frequency. At the VCO output, this translates into nulls at offsets equal to integer multiples of the reference from the carrier effectively eradicating the reference spurs. The spectrum of the current pulses has a sync null whose position depends on their duty cycle. This means that in addition to getting rid of the reference spurs, any spur at an offset greater than the reference frequency can be targeted by choosing the appropriate duty cycle. Charge pump noise contribution can be reduced by using narrow current pulses which limit its on-time when the loop is locked.

The FWVACP and a standard charge pump were fabricated using IBM 0.13 micron CMOS technology. The prototype occupies less than $1mm^2$. The measured reference spur with the FWVACP is more than 10 dB lower than with the standard CP.

This is dedicated to my parents ...

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Nomenclature

$\Sigma\Delta$	Sigma Delta Modulator
AWG	Arbitrary Waveform Generator
BBPD	Bang Bang Phase Detector
BW	Bandwidth
CP	Charge Pump
DAC	Digital to Analog Converter
DIP	Dual In-line Package
DUT	Device Under Test
DZ	Dead Zone
FB	Feedback Signal
FET	Field Effect Transistor
FFT	Fast Fourier Transform
FLL	Frequency Locked Loop
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
FWVA	Fixed Width Variable Amplitude
FWVACP	Fixed Width Variable Amplitude Charge Pump
IC	Integrated Circuit
IF	Intermediate Frequency

LBW	Loop Bandwidth
LO	Local Oscillator
LPF	Low Pass Filter
LSB	Least Significant Bit
MASH	Multi-Stage Noise Shaping
MMD	Multi-Modulus Divider
MUX	Multiplexer
PCB	Printed Circuit Board
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
PN	Phase Noise
PPM	Pulse Position Modulation
PR	Pulse Repetition
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
REF	Reference Signal
RF	Radio Frequency
S/H	Sample-and-Hold
SAR	Successive Approximation Register
SNR	Signal-to Noise-Ratio
SR	Slew Rate
SSPD	Sub-Sampling Phase Detector
VCO	Voltage Controlled Oscillator

Chapter 1

Introduction

Electronics plays an important role in our lives today. There has been a steady increase in the demand for consumer electronics such as cell phones, personal computers and gaming consoles. With this demand comes the need to reduce cost and size, as well as increase speed and functionality of these devices, which has led to an increase in the use of Integrated Circuits (ICs).

This thesis focuses on frequency synthesis, which is a major part of electronic circuit design. Frequency synthesis is the generation of a range of clock frequencies from a stable single frequency reference oscillator such as a crystal oscillator. Frequency synthesizers enable the operation of high frequency oscillators used in modern communication systems like radio transceivers and signal generators. A common example of a frequency synthesizer found in communication ICs is the Phase Locked Loop (PLL). High frequency applications that utilize PLLs include, but are not limited to, clock and data recovery, timing chips, radar, microprocessors and FM Radio.

Figure 1.1 shows a superheterodyne transceiver that employs two synthesizers; one for the RF and one for the IF section of the transceiver. In the receiver chain, the RF synthesizer mixes the RF signal from the antenna down to IF and the IF synthesizer mixes the IF signal down to baseband. On the transmit side, the IF synthesizer mixes the baseband signal up to IF and the RF synthesizer mixes the IF signal up to RF and is then transmitted by the antenna.

Figure 1.1: Superheterodyne transceiver.

1.1 Frequency Synthesiser Architectures

There are three distinct classic architectures for frequency synthesizers [1]. These are the direct (analog) synthesizer, the direct digital synthesizer and the indirect synthesizer.

1.1.1 Direct Analog Synthesizer

The direct analog synthesizer in Figure 1.2 employs multiplication, mixing and division to generate a desired frequency. It is useful for generating a small number of frequencies. Since using switches, it can switch between frequencies very fast. Its drawbacks include large area for the oscillators and mixers, high power consumption and limited programmability [1].

Figure 1.2: Simplified direct analog synthesizer [1].

Figure 1.1: Superheterodyne transceiver.

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Figure 1.2: Simplified direct analog synthesizer [1].

1.1.2 Direct Digital Synthesizer

The Direct digital synthesizer shown in Figure 1.3 employs a look-up table, a Digital-to-Analog Converter (DAC) and a Low Pass Filter (LPF). It generates its waveform by stepping its output using values stored in memory. This synthesizer is very fast when switching from one frequency to another, however synthesizing radio frequencies requires the digital technology to switch at a speed that is at least a multiple of the required frequency. This results in very high power consumption and noise generation [1].

Figure 1.3: Digital synthesizer [1].

1.1.3 Phase Locked Loop

The PLL in Figure 1.4 is a feedback control structure that generates an output signal whose phase is related to that of the input signal. It involves generating a control voltage on the loop filter, which in turn controls the VCO frequency. The PLL is good for tolerating interference and noise because it is always monitoring the output and adjusting the control voltage. Its main drawback is that it is slow in locking to a reference frequency (i.e., slow settling time). The PLL is the most widely used architecture for frequency synthesis and is used extensively for wireless applications [1]. This is the architecture used in this thesis. Chapter 2 explains in detail how the PLL works.

Figure 1.4: Block diagram of a simplified PLL.

1.2 Thesis Outline

Chapter 1 offered a brief introduction to frequency synthesis and the various architectures of frequency synthesizers. Chapter 2 discusses the theory of PLLs and explains integer and fractional PLLs in detail. Motivation for this work, as well as work similar to this one is also presented in this chapter. Chapter 3 explains in detail the origin of reference spurs, examines the nature of the CP current pulses and explains the proposed technique for eradicating reference spurs. The functionality and circuit design of the proposed Fixed Width Variable Amplitude Charge Pump (FWVACP) is detailed in chapter 4. The simulation and measurement results are presented in chapter 5. Lastly, a summary of the work presented in this thesis, future work and conclusions are presented in chapter 6.

Chapter 2

PLL Background

This chapter offers a brief review of closed loop analysis of a PLL and presents closed loop equations, which are used as a starting point for loop design. Type II PLLs and their response to various inputs are then discussed briefly. A detailed review of Type I and Type II closed loop systems and their response to various inputs is included in Appendix A. Integer-N and fractional-N PLLs are presented followed by challenges in the design of PLLs. Finally, motivation for this work and similar work that has been done by others is also presented in this chapter.

2.1 Closed loop analysis of a PLL

PLLs are nonlinear circuits, which can be challenging to analyze. However, the operation of many PLLs can be approximated to an acceptable accuracy with linear models. These are applicable for small phase error, a condition attainable in locked condition [2].

A PLL is a closed loop system that generates a range of frequencies from a single reference. The reference is a clean signal from a crystal oscillator [3]. A basic PLL shown in Figure 2.1 consists of a phase detector, a loop filter, a VCO and a divider. The phase detector compares the phase of the reference signal to the phase of the feedback signal and produces an error signal proportional to this phase difference. The error signal from the phase detector is then filtered by the loop filter to produce a control voltage for the VCO. In addition, the loop filter defines the loop transfer

function and therefore, controls its transient response. The output signal frequency of the VCO is proportional to the control voltage at its input. The VCO output is then divided by N and fed back into the phase detector to complete the loop. It follows that the output frequency is N times the reference frequency. This means that integer multiples of the reference frequency can be generated from a single reference by changing the divider ratio.

Figure 2.1: Phase Locked Loop.

The open loop transfer function is given by:

$$\frac{\theta_o(s)}{\theta_e(s)} = \frac{K_{phase}F(s)K_{vco}}{s} \quad (2.1)$$

The closed loop transfer function is:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_{phase}F(s)K_{vco}}{s + K_{phase}F(s)K_{vco}} \quad (2.2)$$

Refer to Appendix A for a detailed derivation of these transfer functions.

2.2 Types of PLLs

The type of loop refers to the number of integrators in the loop transfer function. From the PLL transfer functions in Equation 2.1 and Equation 2.2 we can see that it is at least a Type I system. Refer to Appendix A for details on Type I PLLs. The work in this thesis is based on a Type II PLL, which has 0 phase error in steady state as detailed below.

In a Type II PLL shown in Figure 2.2, the phase detector is edge triggered and produces an up (UP) or a down (DN) pulse depending on whether the reference leads or lags the VCO output as shown in its timing diagram in Figure 2.3(a). This phase

detector is referred to as a phase frequency detector (PFD). In this example, the PFD operates on the rising edge. If the reference is leading the VCO, the UP signal goes high and it is reset when the rising edge of the VCO comes along. The duration of the pulse is proportional to the phase difference between the two signals. The UP signal causes current I to flow to the capacitor producing a finite voltage V_c , which controls the VCO. In the case of the VCO leading the reference, a DN pulse causes current I to flow from the capacitor to ground.

Figure 2.2: Type II PLL.

Figure 2.3: Type II PLL Timing Diagram and Transfer Function.

The voltage accumulated across the capacitor is proportional to the phase error and is given by:

$$v_c(s) = i\theta_e \frac{1}{sC} \quad (2.3)$$

This means that PFD/CP capacitor combination behaves as an integrator. This integrator in addition to the integrator in the VCO (i.e., K_{vco}/s) makes this PLL a Type II.

The gain of the PFD/CP is given by:

$$K_{phase} = \frac{I}{2\pi} \quad (2.4)$$

The loop filter transfer function is given by:

$$F(s) = \frac{1}{sC} \quad (2.5)$$

The closed loop transfer is given by:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{\frac{K_{phase}K_{vco}}{C}}{s^2 + \frac{K_{phase}K_{vco}}{C}} \quad (2.6)$$

2.2.1 Response of Type II PLLs to various inputs

$$\theta_e(s) = \frac{s^2\theta_i(s)}{s^2 + K_{phase}F(s)K_{vco}} \quad (2.7)$$

Phase step:

$$\theta_i(s) = \frac{1}{s} \quad (2.8)$$

$$\theta_e(s) = \frac{s^2\left(\frac{1}{s}\right)}{s^2 + K_{phase}F(s)K_{vco}} \quad (2.9)$$

$$\theta_e(t = \infty) = \lim_{s \rightarrow 0} \left[s \left(\frac{s^2\left(\frac{1}{s}\right)}{s^2 + K_{phase}F(s)K_{vco}} \right) \right] = 0 \quad (2.10)$$

Equation 2.10 shows that the steady state phase error for a Type II PLL with a phase step at the input is 0. The frequency settles to the same value since there is no change in control voltage.

Frequency step:

$$\theta_i(s) = \frac{1}{s^2} \quad (2.11)$$

$$\theta_e(s) = \frac{s^2\left(\frac{1}{s^2}\right)}{s^2 + K_{phase}F(s)K_{vco}} \quad (2.12)$$

$$\theta_e(t = \infty) = \lim_{s \rightarrow 0} \left[s \left(\frac{s^2 \left(\frac{1}{s^2} \right)}{s^2 + K_{phase} F(s) K_{vco}} \right) \right] = 0 \quad (2.13)$$

Equation 2.13 shows that a Type II PLL with a frequency step at the input will have a 0 phase error in steady state.

2.2.2 Stability of Type II PLLs

The Type II PLL with only one capacitor is unstable because its phase margin is always 0 (refer to Equation 2.6). To stabilize the PLL, a zero is added i.e a resistor in series with the capacitor.

The control voltage then becomes:

$$v_c(s) = i \left(R + \frac{1}{sC} \right) = \frac{i(sRC + 1)}{sC} \quad (2.14)$$

where

$$i = K_{phase} \theta_e = \frac{I}{2\pi} \theta_e \quad (2.15)$$

The closed loop equation then becomes:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{\frac{K_{phase} K_{vco}}{C} (RCs + 1)}{s^2 + K_{phase} K_{vco} R s + \frac{K_{phase} K_{vco}}{C}} \quad (2.16)$$

Equation 2.16 shows that adding a resistor in series with the capacitor in a Type II PLL introduces a zero in the transfer function hence making it stable.

2.3 Integer-N PLLs.

The integer-N PLL in Figure 2.4 is the simplest type of PLL. It draws its name from the fact that the output frequency is an integer multiple of the reference. In the example of a digital radio, it follows that the channel spacing is equal to the reference frequency (Fref). Therefore, in order to have a smaller channel spacing, Fref has to be made smaller [4]. This is usually undesirable because when Fref decreases, N

increases and phase noise goes up as $20\log N$.

Figure 2.4: Integer-N PLL.

An ideal integer-N PLL, once settled i.e. the phase error is zero, will output zero current from the charge pump as the loop filter holds the necessary voltage for the VCO to produce the desired frequency.

2.4 Fractional-N PLLs.

A fractional-N PLL shown in Figure 2.5 generates an output signal with a frequency resolution that is a fraction of the reference frequency. This means that a higher reference frequency, which in turn leads to lower phase noise, can be used while maintaining small channel spacing. The fractional divider ratios are generated by a sigma delta ($\Sigma\Delta$) modulator. It works by dithering between integer values for each reference period whose average is the desired divider ratio. Its resolution can be increased by increasing the number of bits in the accumulators (refer to [5] for a detailed discussion on $\Sigma\Delta$ modulators). A first order $\Sigma\Delta$ modulator is the simplest case in which it dithers between two values. Higher order $\Sigma\Delta$ modulators dither between two or more values. The dithering action pushes the fractional spurs and noise to higher frequencies where they are filtered out by the low pass filtering of the PLL transfer function [6].

Figure 2.5: Fractional-N PLL.

A fractional-N PLL is never truly settled because of the dithering provided by the $\Sigma\Delta$ modulator. This means the current from the charge pump will never settle to zero, although it will average to zero. The charge pump generates current pulses at the reference frequency in response to the $\Sigma\Delta$ modulator.

2.5 Challenges in PLL design

Just like all circuits, PLLs have design challenges associated with them; the greatest being phase noise and frequency spurs in the output signal. Both of these corrupt the signal integrity in the communication system and therefore must be minimized. Phase noise contains noise components at many frequencies whose phase and amplitude are random with respect to the carrier. Phase noise degrades the Signal-to-Noise Ratio (SNR) in a communication system. Spurs differ from phase noise in that they appear as distinct spikes in frequency that rise above the noise floor at deterministic offsets from the carrier. They inter-modulate with other signals in the communication system producing higher-order products which can fall in the desired channel.

There are two types of spurs; reference spurs and fractional spurs. Reference spurs are offset from the carrier frequency by integer multiples of the reference frequency. On the other hand, the position of fractional spurs depends on the dithering action of the $\Sigma\Delta$ modulator.

Reference spurs are a result of a ripple on the VCO control line, which results in frequency components at offsets of the reference frequency and its harmonics. This can be thought of as the VCO output being modulated by the reference. The source

of the ripple is explained below;

- Mismatch in current sources due to differences in the transistor threshold voltages and finite output impedances results in different turn-on times causing a finite charge to be dumped on the loop filter every reference cycle.
- Loop filter leakage current on the high impedance node discharges the integration capacitor. This leakage current is compensated by injecting a finite charge pump current every reference cycle.
- CP charge injection; when the UP and DN switches turn off, their channel charge is injected into the loop filter. The solution is to add dummy switches in series with the current sources.
- Finite C_{gd} capacitances of FET switches cause clock feedthrough from the PFD control line to the loop filter voltage. The solution is to reduce the size of switches or use a smaller control voltage swing.

Another design challenge is the dead zone in the PFD/CP transfer function. Large CP switching times means the CP cannot react to small pulse widths. The absence of a response from the CP means that the VCO clock edges can move unrestrictedly until they reach the point when the CP starts reacting. This results in a clock jitter window equal to the dead-zone. The solution is to introduce a reset delay, which is longer than the switching times of the CP current sources such that there is a period of time when both up and down current sources of the CP turn on before they start measuring the phase difference between the reference and feedback signals.

Lastly, there is a tradeoff between spur amplitude and loop settling time. That is, using a narrow loop bandwidth to attenuate spurs increases channel selection time.

2.6 Motivation

As discussed in the previous section, the biggest challenge in designing PLL based frequency synthesizers is spurs. Spurs are problematic because they can mix with other signals and dump their product on top of the desired signal. For example, in an integer-N PLL the channel spacing is chosen to be equal to the reference frequency,

which means that the reference spur will translate all the adjacent channels to the center of the desired channel as shown in Figure 2.6. These undesired channels appear as an elevated noise floor to the desired channel and limit the SNR.

Figure 2.6: Adjacent Channel Interference due to Reference Spurs.

A number of techniques have been developed to tackle the problem of spurs, two of them are sample and hold and pulse position modulation. These techniques are discussed in detail in the next section. Although these techniques lower the spur amplitude, neither of them actually eliminates these spurs. The motivation for this work is to develop a technique that would completely eradicate the reference spurs. This is achieved by creating nulls at frequency offsets equal to multiples of the reference frequency from the carrier, essentially getting rid of the reference spurs. Chapter 3 explains this technique in detail.

2.7 Literature review

This section covers techniques that have been developed to minimize reference spurs. These include sample and hold, Pulse Position Modulation (PPM), sub-sampling, analog and digital calibration techniques and improved charge pump designs. A summary of each of these techniques is presented below:

2.7.1 Sample and Hold

The sampling of the PFD/CP is non-uniform because the PFD produces variable width pulses aligned to either the reference or VCO output depending on which edge comes first as shown in Figure 2.7. A sample and hold (S/H) block is introduced between the CP and the loop filter as shown in Figure 2.8. After every UP or DOWN pulse, the S/H block samples the voltage across the integrating capacitor and holds it for the reference cycle. By sampling the CP output at regular time intervals, the non-uniform sampling of the PFD/CP is removed. The S/H block also prevents the modulation of the loop filter voltage by the reference signal which eliminates reference spurs in the VCO output. [7].

Figure 2.7: Non-uniform Sampling.

Figure 2.8: S/H $\Sigma\Delta$ Fractional-N Synthesizer [7].

2.7.2 Pulse Position Modulation and Pulse Repetition

Pulse Position Modulation (PPM) randomizes the position of CP current pulses to break their periodicity and redistribute the reference spurs into broadband noise.

Pulse Repetition (PR) involves repeating the pulse N times within one reference period making it appear as a high frequency signal Nf_{ref} . The charge pump current is scaled by a factor of N to keep the charge delivered to the loop filter the same. The reference spurs are pushed to a higher frequency where they are filtered by the loop filter. [8–10] use one or a combination of these methods.

[9] uses a combination of PPM and PR. The UP and DN signals, which control the CP current are delayed by random amounts. This is accomplished by using a digital delay line and a MUX controlled by a random sequence as in [8]. The drawback of the technique used in [9] is increased complexity.

[10] uses distributed PFDs and CPs and two delay lines to convert one UP/DN pulse to N pulses with lower amplitude in one reference cycle. If the N pulses are evenly distributed within the reference period, the PLL output does not exhibit sidebands at f_{ref} , rather the closest sidebands are located at Nf_{ref} where they are filtered. In order to maintain loop characteristics, the gain of the distributed CPs is scaled down. The spurs are further reduced by using PPM to break pulse periodicity. The pulses are delayed using a random binary sequence. This causes the time interval between each pulse to vary every reference cycle eliminating the periodic behaviour on the control line reducing the magnitude of the reference spur harmonics and their products at the VCO output. The drawback of the technique used in [10] is increased implementation complexity in addition to increased layout area and feedthrough due to the total size of CP switches. Also for CPs with low currents, dividing the current further by N may not be practical because of leakage and CP mismatch. Lastly, mismatch and leakage currents may not scale with N leading to net current being injected into the loop filter due to these non-idealities.

2.7.3 Sub-sampling Phase Detector

[11] and [12] use a Sub-Sampling Phase Detector (SSPD) as shown in Figure 2.9, which achieves low level reference spurs (i.e., $< -80\text{dBc/Hz}$) while using high bandwidth of $F_{\text{ref}}/20$. The SSPD samples the VCO output (without using a divider) with the reference clock and converts the VCO phase error into sampled voltage variations. When the VCO and the reference phases are aligned and their frequency ratio is an integer, the sampled voltage v_{sam} has a constant value equal to VDC. When there is a phase error between the VCO and reference, v_{sam} deviates from VDC by an amount equal to the phase error. The CP converts the sampled voltage into current and injects it to the loop filter. The CP is amplitude controlled by the difference between VDC and v_{sam} , which is proportional to $\Delta t / \text{SR}_{\text{vco}}$ where SR_{vco} is the slew rate of the VCO: $\text{SR}_{\text{vco}} = A_{\text{vco}} 2\pi F_{\text{vco}}$. Consequently the shape of the SSPD/CP has the same shape as the VCO waveform, which limits the frequency acquisition range. To make things worse, the SSPD does not distinguish between $N F_{\text{ref}}$ and other harmonics of F_{ref} and thus the SSPD can lock to an unwanted division ratio. An auxiliary frequency locked loop (FLL) is used to solve this problem. The FLL consists of a divide by N and has a Dead Zone (DZ) inserted between the PFD and CP such that for phase errors that fall outside the FLL DZ, the FLL which has a larger gain than the core loop dominates the loop control and brings down the F_{vco} to $N F_{\text{ref}}$. When the loop is close to locking the phase error is small and falls inside the FLL DZ, so the FLL CP produces zero current and the loop settles with a time characteristic determined by the core loop.

The drawback of this technique is that it uses two loops, which occupies a lot of layout area. Also the high SSPD/CP gain due to the high SR_{vco} means that a large integration capacitor has to be used in the loop filter, which requires a lot of layout area.

Figure 2.9: Generic Sub-Sampling PLL (SSPLL) Architecture [11].

2.7.4 Charge Pump design

[13] uses a frequency doubler in the reference path to push the reference spurs to a higher frequency where they can be attenuated by the loop filter. Additionally, a replica of the CP and bias controller are used as a current compensation controller to reduce the current mismatch between the up and down currents.

2.7.5 Analog and digital calibration to minimize reference spurs

[14–16], employ analog and digital CP calibration techniques to minimize reference spurs at the output.

[14] takes advantage of the fact that the magnitude of the disturbance on the VCO control line which results in reference spurs is proportional to the width of the current pulses on the VCO control input when the PLL is locked. It uses a variable delay element in the reset path of the PFD and adjusts the delay using feedback to make the locked pulsewidth approach zero. The feedback circuitry ensures that the overall PFD delay is positive to avoid a DZ. The size of the pulse width can be arbitrarily small by increasing the size of the resistor in the feedback loop as shown in Figure 2.10.

The drawbacks of this technique is that it assumes that all other PLL components

behave in an ideal manner, which is unrealistic. The replicated PFD/CP that creates the delay control voltage, to avoid interfering with loop dynamics, increases complexity and layout area. Lastly, the time constant associated with the feedback capacitor may be too long to make this technique feasible in PLLs that require fast settling times.

Figure 2.10: Block Diagram of the Technique used in [14].

The CP in [15] is designed with current programmability in the discharge path and uses a Static Phase Offset (SPO) detector to indicate whether the reference is leading or lagging the output. An off-chip calibration scheme is used to determine the optimum charge pump current ratio to minimize current mismatch and the resulting reference spurs. The drawback of this technique is that the CP has a finite number of steps (16 in this case) which may not be enough to provide an optimum solution for minimizing reference spurs. Also the increased number of devices in the discharge path increases the noise in the system.

[16] uses a switched delay PFD to switch between an enlarged reset delay when the loop is not locked and a normal reset delay when the loop is locked and the calibration completed. Like [15], the discharge path has digitally controlled current sources. The lock detect indicates when the calibration should begin while the Bang Bang Phase Detector (BBPD) provides phase comparison between UP and DN controlling signals to provide information for the Successive Approximation Register (SAR) controller.

For an N-bit controlled CP, the calibration process repeats N times until the Least Significant Bit (LSB) is determined and the CP code is set. Then the SAR controller puts out a signal indicating that the calibration process is completed, the reset delay is switched back to normal and the digital circuits are turned off.

The drawback of this technique is that the digital calibration adds to the settling time. Also the calibration time is proportional to the reference period and may not be ideal for low frequency reference clocks.

Chapter 3

Charge Pump Current Pulse Analysis in Relation to Reference Spurs

This chapter analyzes charge pump current pulses to show how they cause spurs to appear at the PLL output. A mathematical analysis of a fixed width variable amplitude pulse train which is used as a starting point for the design of a Fixed Width Variable Amplitude Charge Pump (FWVACP) is also presented in this chapter.

For the analysis of the charge pump current pulses to hold, it must be understood how frequency components in the charge pump current appear at the output of the PLL. Frequency components are first attenuated by the loop filter; no mixing occurs at this point so the frequency components in the charge pump current still exist in the voltage signal at the VCO input. Assuming the modulation index for each frequency component at the VCO input is small enough, only narrowband FM modulation occurs. This means that no new frequency components are generated at the VCO output since narrowband FM modulation is linear. Spurs are then visible at the VCO output at the reference offset and its harmonics. Using this reasoning, a technique is presented for creating nulls in the charge pump current at multiples of the reference frequency therefore eliminating reference spurs in the PLL output.

3.1 PPM and PWM and how they relate to Charge Pump Current Pulses

Figure 3.1 shows an example of charge pump current pulses in a typical fractional-N PLL. The charge pump current pulses are affected in two ways by the reference and the feedback signals. Firstly, the width of the charge pump pulses is dependent on the spacing between the rising edges of the two signals i.e. the phase difference between the two signals. This leads to Pulse Width Modulation (PWM). Secondly, the charge pump current pulse may occur before or after the reference rising edge depending on whether the reference leads or lags the feedback. This leads to Pulse Position Modulation (PPM). It is these two factors that cause the charge pump current pulses to generate reference spurs. Other non-idealities such as charge pump mismatch can worsen reference spurs, but their origin is the nature of the pulses.

Figure 3.1: Example of CP Current Pulses in a Typical Fractional-N PLL.

Matlab was used to analyze the effect of the nature of charge pump pulses and the results are shown in Figure 3.2 and Figure 3.3.

Figure 3.2 and Figure 3.3 demonstrate PWM and PPM respectively using 10 MHz pulse trains. In Figure 3.2(a), the pulses appear at constant time intervals but have varying widths while the pulses have a constant width but appear at varying time intervals in Figure 3.3(a). Both spectrums show spurs at 10 MHz and its harmonics in 3.2(b) and Figure 3.3(b).

Figure 3.2: A Pulse Train with PWM and its Spectrum.

Figure 3.3: A Pulse Train with PPM and its Spectrum.

3.2 Mathematical Analysis of Fixed Width Variable Amplitude Pulse Train

This section shows a mathematical analysis of how reference spurs are eliminated from the charge pump output by eliminating PWM and PPM. This is done so by generating a fixed width variable amplitude (FWVA) pulse. In a typical PLL, PPM and PWM modulation are responsible for representing phase error information. With a FWVA pulse, phase error information is stored in the amplitude of the pulse. A generic FWVA pulse train is shown in Figure 3.4.

Figure 3.4: A Generic Pulse Train. a) shows a Continuous Signal. b) shows the Signal after Sampling.

A few restrictions must be placed on the signal; the width of each pulse must be equal and the spacing between each pulse must also be equal. The amplitude of each pulse is set to be arbitrary to solve the general case, and is defined as $a_1 \dots a_p$. Finally, the signal must be periodic.

Discrete Fourier analysis will be used to examine the frequency spectrum of this signal. What the analysis will show is a total cancellation of the frequency components at frequencies related to the beginning edges of each pulse. These frequencies are analogous to integer multiples of the reference frequency in a PLL.

The signal in Figure 3.4(a) is continuous in the time domain. This signal is sampled in order to use discrete-time Fourier analysis. Figure 3.4(b) shows the signal after it has been sampled.

Now we define the discrete signal $x(n)$ based on Figure 3.4.

$$x(n) = \{a_1 a_1 \dots a_1 00 \dots 00 a_2 a_2 \dots a_2 00 \dots 00 a_p a_p \dots a_p 00 \dots 00\} \quad (3.1)$$

Using the discrete Fourier equation we can come up with the spur amplitudes of the reference frequencies. To begin we turn to the analysis equation for discrete-time

periodic signals 3.2. where k is the index of the frequency component. All other variables are defined in Table 3.1.

$$c_k = \frac{1}{N} \sum_{n=0}^{N-1} x(n) e^{-j2\pi kn/N} \quad (3.2)$$

Table 3.1: Variable Definition.

Variable	Variable Definition
$x(n)$	The time domain signal
p	Total number of pulses per period N
n	Index of the signal $x(n)$
w	Number of samples per pulse
z	Number of zeros between pulses
R	Reference period: $w + z$
N	Period of signal: $p(w + z)$

This can be expressed as follows if we substitute in $x(n)$.

$$\begin{aligned}
 c_k = \frac{1}{N} & \left[a_1 \left(1 + e^{\frac{-j2\pi k}{N}} + e^{\frac{-j2\pi k 2}{N}} + \dots + e^{\frac{-j2\pi k(w-1)}{N}} \right) + \right. \\
 & a_2 \left(1 + e^{\frac{-j2\pi k(r)}{N}} + e^{\frac{-j2\pi k(r+1)}{N}} + \dots + e^{\frac{-j2\pi k(r+w-1)}{N}} \right) + \\
 & a_3 \left(1 + e^{\frac{-j2\pi k(2r)}{N}} + e^{\frac{-j2\pi k(2r+1)}{N}} + \dots + e^{\frac{-j2\pi k(2r+w-1)}{N}} \right) + \\
 & \dots + \\
 & \left. a_p \left(1 + e^{\frac{-j2\pi k((p-1)r)}{N}} + e^{\frac{-j2\pi k((p-1)r+1)}{N}} + \dots + e^{\frac{-j2\pi k((p-1)r+w-1)}{N}} \right) \right] \quad (3.3)
 \end{aligned}$$

The number of spurs between each reference frequency is equal to the sequence length i.e. the number of pulses in the sequence, or p in this analysis. This means the first reference spur will occur at c_p . We now solve for c_p . This equation uses $N = pr$ from Table 3.1 where appropriate.

$$\begin{aligned}
 c_p = \frac{1}{N} & \left[a_1 \left(1 + e^{\frac{-j2\pi}{N}} + e^{\frac{-j2\pi 2}{N}} + \dots + e^{\frac{-j2\pi(w-1)}{N}} \right) + \right. \\
 & a_2 \left(1 + e^{\frac{-j2\pi(r)}{N}} + e^{\frac{-j2\pi(r+1)}{N}} + \dots + e^{\frac{-j2\pi(r+w-1)}{N}} \right) + \\
 & a_3 \left(1 + e^{\frac{-j2\pi(2r)}{N}} + e^{\frac{-j2\pi(2r+1)}{N}} + \dots + e^{\frac{-j2\pi(2r+w-1)}{N}} \right) + \\
 & \dots + \\
 & \left. a_p \left(1 + e^{\frac{-j2\pi((p-1)r)}{N}} + e^{\frac{-j2\pi((p-1)r+1)}{N}} + \dots + e^{\frac{-j2\pi((p-1)r+w-1)}{N}} \right) \right] \quad (3.4)
 \end{aligned}$$

We can express everything inside the brackets as X .

$$c_p = \frac{1}{N} \left[a_1 X + a_2 X + a_3 X + \dots + a_p X \right] = \frac{X}{N} \left[a_1 + a_2 + a_3 + \dots + a_p \right] \quad (3.5)$$

This simplification can be performed as follows: In Equation 3.3 we look at the first terms in each of the brackets.

$$1 = e^{-\frac{j2\pi(r)}{r}} = e^{-\frac{j2\pi(2r)}{r}} = e^{-\frac{j2\pi((p-1)r)}{r}} \quad (3.6)$$

Now we look at the second term ...

$$e^{-\frac{j2\pi}{r}} = e^{-\frac{j2\pi(r+1)}{r}} = e^{-\frac{j2\pi(2r+1)}{r}} = e^{-\frac{j2\pi((p-1)r+1)}{r}} \quad (3.7)$$

This process can be done for all of the terms in the brackets. From Equation 3.4 we can see that as long as the pulse train amplitudes a_1 through a_p all sum to zero there is no reference spur. The same strategy can be used to determine the spur amplitude for integer multiples of the p^{th} spur; that is, for any multiple of the reference frequency.

In order to show the derived equation is valid MATLAB is used to generate an arbitrary signal that fits the description in Figure 3.4(b). The signal is shown in Figure 3.5. The pulse frequency is at 10 MHz and the pulse widths are 10%.

Figure 3.5: Sample FWVA Signal in the Time Domain.

Figure 3.6 shows the frequency domain of the signal. Note the nulls that occur every 10 MHz as predicted by Equation 3.4. We also notice the sync function shape has a null at 100 MHz. Having a 10% pulse width gives the first sync null at 10 times the reference. Having a pulse width of 100% would put the sync pulse null on top of the first reference pulse null. This implies that the first reference frequency is the furthest the sync pulse null can be pulled in.

Figure 3.6: Sample FWVA Signal in Frequency Domain.

This result can be exploited to target spurs at any frequency outside the first reference frequency by choosing the appropriate pulse width. Equation 3.8 can be used to find the appropriate pulse width to create a sync null at the spur frequency F_{spur} .

$$\text{pulse width} = \frac{F_{ref}}{F_{spur}} \cdot 100\% \quad (3.8)$$

For example, a PLL with a 10 MHz reference frequency has spurs at 70 MHz offset from the VCO center frequency. The spurs can be eliminated by creating sync nulls at 70 MHz. The appropriate pulse width is calculated to be 14.3% using Equation

3.8. Figure 3.7 (a) shows the pulse train used to create a sync null at 70 MHz and its spectrum in (b).

Figure 3.7: Removing a spur at 70 MHz by setting the pulse width to 14.3%.

Chapter 4

Design of Fixed Width Variable Amplitude Charge Pump

This chapter describes the functionality of the proposed Fixed Width Variable Amplitude Charge Pump (FWVACP). Equations for the gain and maximum phase error of the FWVACP are derived followed by transistor level design of its building blocks.

4.1 Circuit Description

A possible implementation of the FWVACP and its corresponding timing diagram are shown in Figure 4.1 and Figure 4.2 and respectively.

Figure 4.1: Implementation of the FWVACP.

Figure 4.2: Timing Diagram for the FWVACP.

The key idea for the design of the FWVACP is that the output current pulses are of a fixed width set by the width of the PULSE signal. The PULSE signal is generated from the reference signal Fref. PULSE goes high on the falling edge of Fref (refer to Figure 4.2) to close either ‘up pulse switch’ or ‘dn pulse switch’ for a pre-determined fixed time set by the delay element t_{pulse} . It is important to note that PULSE has the same frequency as Fref.

The phase error information from the standard tri-state PFD (labeled PFD in Figure 4.1) is carried in the CHARGE signal. CHARGE closes the ‘charge switch’ so that current I_1 can charge capacitor C for the duration of the CHARGE signal. The charge accumulated on C is proportional to the magnitude of the phase difference between the reference F_{ref} and the feedback F_{fb} and the voltage on C is converted into current I_2 . I_2 flows onto the loop filter if ‘up pulse switch’ is closed and from the loop filter if ‘dn pulse switch’ is closed. These switches always close for a constant time equal to the width of the PULSE signal. Which switch closes, depends on whether F_{ref} is leading or lagging F_{fb} .

In order to create constant width signals from UP and DN, UP_TOGGLE and DN_TOGGLE signals are generated respectively. UP_TOGGLE goes high on the rising edge of UP and goes low on the falling edge of PULSE. DN_TOGGLE behaves the same way (refer to Figure 4.2).

The UP_TOGGLE and DN_TOGGLE signals are then ANDed with PULSE to generate UP_PULSE_ON and DN_PULSE_ON signals respectively (refer to Figure 4.1 and Figure 4.2). These signals are responsible for closing the ‘up pulse switch’ or ‘dn pulse switch’. It is important to note that UP_PULSE_ON and DN_PULSE_ON have a fixed width equal to the width of PULSE.

Timing is very important for the FWVACP to operate as intended. When current is flowing onto or from the loop filter, C must not be charging or draining i.e. when UP_PULSE_ON or DN_PULSE_ON is high, CHARGE and DRAIN must be low (refer to Figure 4.2). This ensures constant current amplitude when ‘up pulse switch’ or ‘dn pulse switch’ is closed.

UP is ANDed with the inverse of UP_PULSE_ON while DN is ANDed with the inverse of DN_PULSE_ON. The resulting signals are ORed together to generate the CHARGE signal (refer to Figure 4.1). The result is that when UP_PULSE_ON or DN_PULSE_ON is high, CHARGE is low (refer to Figure 4.2).

The DRAIN signal is generated using a flip-flop. DRAIN goes high on the falling edge of PULSE and is reset on the rising edge of either UP or DN (refer to Figure 4.1).

The result is that when either CHARGE, or PULSE is high, DRAIN is low. Also, C must be fully drained before the charge switch is closed. Resetting DRAIN on the

rising edge of UP or DN, ensures that C is drained for at least half a cycle ($\theta_e = \pi$). In other words, DRAIN goes high on the falling edge of PULSE and remains high until the rising edge of CHARGE (refer to Figure 4.2). This also ensures that the values of C and I_1 do not affect the loop dynamics when current is flowing on to or from the loop filter.

4.2 Gain and Maximum Phase Error

The gain K_{phase} for a PFD with a FWVACP will now be derived. Current I_1 charges capacitor C for time Δt which is related to the phase error θ_e between Fref and Ffb and the reference period T_{ref} as follows:

$$\Delta t = \left(\frac{\theta_e}{2\pi} \right) (T_{\text{ref}}) \quad (4.1)$$

Charge q is accumulated on C during time Δt and the voltage after time Δt :

$$V = \frac{q}{C} = \frac{I_1 \Delta t}{C} = \left(\frac{I_1}{C} \right) \left(\frac{\theta_e}{2\pi} \right) (T_{\text{ref}}) \quad (4.2)$$

Current from the FWVACP, I_2 is directly proportional to voltage V which in turn is proportional to the phase error θ_e . I_2 is given by:

$$I_2 = KV = \frac{KI_1}{C} \frac{\theta_e}{2\pi} (T_{\text{ref}}) \quad (4.3)$$

where K is the constant of proportionality between voltage V and current I_2 .

The average CP current is determined by the fraction, t_{pulse} of the reference period for which current is flowing onto the loop filter. t_{pulse} is a constant which is determined by the desired pulse width (refer to Figure 4.1 and Figure 4.2).

$$I_{\text{ave}} = I_2 \left(\frac{t_{\text{pulse}}}{T_{\text{ref}}} \right) = \frac{KI_1}{C} \frac{\theta_e}{2\pi} (T_{\text{ref}}) \left(\frac{t_{\text{pulse}}}{T_{\text{ref}}} \right) \quad (4.4)$$

The PFD gain K_{phase} is then determined using the average CP current and phase error θ_e :

$$K_{phase} = \frac{I_{ave}}{\theta_e} = \frac{KI_1 t_{pulse}}{2\pi C} \quad (4.5)$$

The average current is plotted as a function of the phase difference as shown in Figure 4.3. The result can be interpreted as a transfer function of the FWVACP. The capacitor C charges for a maximum time equal to half the reference period (equivalent to a phase error of π). Even if the phase error is larger than π , the ‘charge switch’ must open to allow a constant amplitude current to be delivered to the loop filter. This is the reason for the flat region of the transfer function shown in Figure 4.3. The maximum phase error is 2π , after which the pattern repeats.

Figure 4.3: Average output current vs. phase for PFD and FWVACP.

4.3 Design Flow

The tristate PFD and the building blocks of the FWVACP were implemented at transistor level in cadence using IBM 130nm CMOS technology. Below is a detailed description of the transistor level design of the tristate PFD and the FWVACP blocks shown in Figure 4.1.

4.3.1 Tristate PFD

The tristate PFD in Figure 4.4 is positive edge triggered and is constructed from two D-flip-flops with an active low reset and an AND gate. A delay of about 2 ns is added

in the reset path to avoid a deadzone.

Figure 4.4: Positive Edge Triggered Tristate PFD.

4.3.2 Charge and Drain Switches

Current I_1 is supplied externally to this circuit as shown in Figure 4.5. When the charge signal is high, I_1 charges the external capacitor C to a voltage $V = I_1 \Delta t / C$ where Δt is the duration for which the charge signal is high. When drain signal is high, the external capacitor is discharged to ground. The charging and discharging of the external capacitor is shown in Figure 4.6.

Figure 4.5: Charge and Drain Switches for the Charging Capacitor.

Figure 4.6: Charging and Discharging a 20 pF Capacitor with 500 uA.

4.3.3 Voltage to Current Converter

The voltage to current converter is constructed from an op-amp with negative feedback as shown in Figure 4.7. Current I_2 is the ratio of the voltage on the charging capacitor, V_{cap} and the external resistor R . This current is used as the bias current for the CP current sources.

Figure 4.7: Voltage to Current Converter.

In order to get a wider linear range for input voltage V_{cap} , a 3 V supply is used in

this block instead of a 1.2 V supply. Consequently, 3.3 V transistors that can handle the 3 V supply are used in this block. Figure 4.8 shows that this circuit has an input range of 0 to 1.4 V which is sufficient to produce the appropriate current for the CP current sources since the maximum V_{cap} voltage is 1.2 V.

Figure 4.8: Voltage to Current Converter with $R = 400 \Omega$ and $C = 20 \text{ pF}$.

Figure 4.9 shows a basic CMOS op-amp with two gain stages that was used in the voltage to current converter circuit. It has a gain of 80 dB and 75 degrees of phase margin.

Figure 4.9: Basic CMOS 2-Stage Op-amp.

4.3.4 Charge Pump

Current I_2 is the input bias current for the charge pump current sources. It is generated by the voltage to current converter and is directly proportional to the voltage on the charging capacitor which in turn is proportional to the phase difference between the feedback signal and the reference signal. It is important to note that I_2 is always changing depending on the phase difference. The current sources are controlled by the UP_PULSE_ON and DN_PULSE_ON signals which have a constant width equal to the width of the PULSE signal.

The current sources are designed with a length of 1.5 μm as shown in Figure 4.10 so as to increase the output impedance and improve matching between the NMOS and PMOS transistors. To improve matching further, an op-amp which offers both positive and negative feedback is used. It senses the voltage on the output node and compares to the voltage on the mirrors. If the voltage on the mirrors is higher than the output, it increases the voltage on the PMOS gate causing the current through the NMOS and PMOS to be very similar [5]. Figure 4.11 shows the DC- characteristics of the charge pump i.e how the current varies with output voltage. It shows that the currents are fairly well matched between 0.3 V and 0.9 V.

Figure 4.10: Schematic of CP with Feedback to Equalize UP and DN Currents.

Figure 4.11: Charge pump DC-Characteristics.

4.3.5 Phase Noise of the PFD/FWVACP

The Phase Noise (PN) of the PFD/FWVACP was simulated and the results are shown in Figure 4.12. The simulation is set-up such that the PFD is operating with 2 ns of offset and the CP is pumping up. At 100 kHz the PN is -135 dBc/Hz. The largest noise contributors are the bias transistors in the current mirror.

Figure 4.12: PFD/FWVACP Phase Noise.

4.3.6 Layout of FWVACP

The layout of the PFD/FWVACP in Figure 4.13 is approximately 800 μm x 800 μm . The switching circuitry of the PFD and FWVACP logic is placed at the top while the CP is placed at the bottom to minimize the coupling of these signals to the CP. Coupling of these signals to the CP directly affects the reference spur performance of the PFD/CP. The analog and digital circuitry have dedicated supplies (VDD_DIG and VDD_ANLG) to further reduce interaction between them.

Figure 4.13: Layout of PFD/FWVACP.

Chapter 5

Simulation and Measurement Results

This chapter presents simulation results of an ideal fractional-N PLL with a standard CP and with a FWVACP to show the validity of the proposed technique. Measurement results showing the functionality of the fabricated FWVACP are also presented followed by closed loop measurements of a fractional-N PLL with a standard CP and with a FWVACP.

5.1 Matlab simulation results

The fractional-N PLL shown in Figure 2.5 was implemented in Matlab using lines of code. The standard CP was then replaced with the FWVACP to compare the performance of the two CPs. Table 5.1 shows a summary of loop parameters for the PLL with a standard CP and also with a FWVACP. The $\Sigma\Delta$ modulator is a third-order MASH 1-1-1 with 5 bits. The loop filter is a second-order filter with parameters C_1 , C_2 and R set to yield a loop bandwidth of 75 kHz. The CP has a current I_{CP} of $2\pi 100 \mu A$ and PFD/CP gain K_{phase} of $100 \mu rad$. The VCO has a center frequency f_{center} of 95 MHz and a gain K_{VCO} of 5 MHz/V. C is chosen to be 1 pF while I_1 is chosen to be 1 mA. Depending on the pulse width of the FWVACP chosen, K (constant of proportionality between the V_{cap} and I_2) is adjusted to keep K_{phase} the same for all simulations. Refer to equation 4.5.

Table 5.1: Simulation Loop Parameters.

Parameter	Standard CP	FWVACP
Fref (MHz)	10	10
K_{phase} ($\mu\text{A}/\text{rad}$)	100	100
K_{VCO} (MHz/V)	5	5
f_{center} (MHz)	95	95
C_1 (nF)	6	6
C_2 (nF)	0.6	0.6
R ($\text{k}\Omega$)	1.03	1.03
I_{CP} (μA)	$2\pi 100$	variable
MASH 1-1-1 $\Sigma\Delta$ (bits)	5	5
Loop BW (kHz)	75	75
Damping constant ζ	0.707	0.707
I_1 (mA)	N/A	1
C (pF)	N/A	1
VCO PN at 1MHz offset (dBc/Hz)	-120	-120

The PLL with the parameters in Table 5.1 was simulated in Matlab. The simulation was run for 1.06 ms with a time step of 0.4 ns. The time step could have been reduced to improve the resolution however, this would require extremely long simulation times.

5.1.1 Settling Behavior with Standard CP and FW-VACP

Figure 5.1 shows the settling behavior of the loop filter voltage and the CP current during a cycle slip when a 5.3 MHz frequency step from 95 MHz to 100.3 MHz (divisor

ratio of $10\frac{1}{32}$) is applied to the PLLs. In both cases, the loop filter voltage settles to the same value when the loop is locked. However, the PLL with the FWVACP has approximately twice the cycle slips as the standard CP and therefore takes longer to settle. This is due to higher average current in the standard CP than the FWVACP (refer to Figure 4.3).

Note that with a standard CP the amplitude of the current pulses is constant while the pulse width is variable. In the case of the FWVACP, the current pulses have constant pulse width and variable amplitude. In addition, the FWVACP current pulses agree with the plot of average charge pump current versus phase error shown in Figure 4.3 in that they maintain constant amplitude for phase error θ_e greater than π before cycle slipping at θ_e equal to 2π .

Figure 5.1: Loop filter voltage showing settling for a 5.3 MHz frequency step and charge pump current during a cycle slip.

5.1.2 FFT of Charge Pump Current Pulses and VCO Spectrum

Figure 5.2: Standard CP and FWVACP current pulses when the loop is settled.

Figure 5.2 shows the standard CP and FWVACP pulses when the loop is settled. Notice the constant amplitude but varying width pulses of the standard CP versus the varying amplitude but constant width pulses of the FWVACP.

Figure 5.3(a) and (b) show the FFT of the standard CP current pulses and the spectrum of the VCO output respectively. The reference spurs in the CP directly appear in the VCO output at offsets equal to multiples of the 10MHz. These spurs are entirely due to the nature of the current pulses as discussed in Chapter 3 since an ideal CP is used i.e. the UP and DN currents are perfectly matched.

(a) FFT of standard CP current pulses.

(b) Spectrum of the VCO output.

Figure 5.3: FFT of standard CP current pulses and VCO output spectrum with PLL locked to 100.3 MHz.

The FFT of the FWVACP current pulses is shown in Figure 5.4(a). The reference spurs in 5.3(a) have now been replaced with reference nulls visible at multiples of 10 MHz. The sync null appears at 100 MHz as expected with a 10% pulse width. The reference nulls in Figure 5.4(a) cause nulls to appear in the VCO output at multiples of 10 MHz offset from the VCO frequency as shown in Figure 5.4(b). This shows that the FWVACP has effectively eradicated the reference spurs from the VCO output.

(a) FFT of FWVACP current pulses.

(b) Spectrum of the VCO output.

Figure 5.4: FFT of FWVACP (10% pulse width) current pulses and VCO output spectrum with PLL locked to 100.3 MHz.

5.1.3 PLL Phase Noise with standard CP versus FWVACP

The VCO is modelled to have phase noise of -120 dBc/Hz at 1 MHz offset. The standard CP is modelled with noise current i_n of $1 \frac{nA}{\sqrt{Hz}}$. The i_n of the FWVACP is a bit more complicated to model since it varies with current amplitude. It is modelled as follows:

In a real CP made with CMOS transistors, the main source of noise is the drain noise i_{nd} which is related to the square root of the current I_{DS} through the transistor [5]. For a fair comparison, the FWVACP is modelled to have the same i_n as the standard CP when the current amplitudes are equal i.e when the FWVACP has a current of $2\pi 100 \mu A$, the noise current is $1 \frac{nA}{\sqrt{Hz}}$. Therefore for this simulation, i_n of the FWVACP is modeled as:

$$i_n = 1 \frac{nA}{\sqrt{Hz}} \left(\sqrt[4]{\frac{I_{CP}}{2\pi 100 \mu A}} \right) \quad (5.1)$$

Figure 5.5 shows the phase noise for the standard CP and FWVACP with different pulse widths. The standard CP is shown to have higher phase noise than the FWVACP. Also the phase noise decreases with decreasing pulse width for the FWVACP. This is because the noise performance for the CP is related to both the transistor noise sources and also to the time that the CP is on when the loop is locked [5] as shown in Equation 5.2. t_{CP} is the duration of time for which the CP is on when the loop is locked and T_{ref} is the reference period. Having the CP on for a short period of time causes less phase noise than long periods of time. The phase noise can be significantly reduced with the FWVACP by using narrower pulses. The limit on how small the pulse width can be depends on the turn-on time for the PMOS and NMOS transistors i.e the pulse has to be large enough to prevent a dead zone.

$$\text{phase noise} \propto \left(\sqrt[4]{I_{CP}} \right) \left(\sqrt{\left(\frac{t_{CP}}{T_{ref}} \right)} \right) \quad (5.2)$$

Figure 5.5: PLL Phase noise for standard CP and FWVACP with different pulse widths.

5.2 Measurement Results

The FWVACP and standard CP were fabricated using IBM 0.13 μm CMOS technology. The building blocks of the FWVACP were tested for functionality followed by closed loop measurements with both CPs. The measurement setup is described in section 5.2.2.

5.2.1 Die Micrograph

Both the FWVACP and the standard CP were incorporated on the same chip. Different versions of the designs were included on the chip in order to use up the available 2mm x 2mm area as shown in Figure 5.6. Because of the placement of the pads, multiple bonding options were used to test the different versions. A DIP40 package was chosen since it has enough pins to support all the bonding options without shorting pins between versions.

Figure 5.6: Die Micrograph.

The idea for the multiple versions was to compare performance with different CP topologies. The versions are listed below:

- Version 1: PFD/FWVACP - basic CP with switches in signal path.
- Version 2: PFD/FWVACP - basic CP with switches out of signal path.
- Version 3: PFD/FWVACP - CP with feedback and with switches in the signal path as shown in Figure 4.10.
- Version 4: PFD/Standard CP - basic CP with switches in signal path.
- Version 5: PFD/Standard CP - CP with feedback and with switches in the signal path as shown in Figure 4.10.
- Version 6: Opamp - 3V opamp used in the voltage to current converter as shown in Figure 4.9.

5.2.2 Measurement Setup

The measurement setup was arranged as shown in Figure 5.7. The components used on the testboard are described in Table 5.2.

Table 5.2: Discription of Testboard components.

Component	Device	Description
LDO	HMC1060/MIC2215	4/3 output Low Dropout Regulators
VCXO	AOCJY-10MHz-SW	10 MHz crystal oscillator
RDIV	HMC394LP4	5 bit divider
1:2 RBUFF	PL133-27	1 input, 2 output buffer
DELAY LINE	DS1100L-25	5-tap delay line
BUFF	NC7SV34	Single buffer
INV	NC7SP04	Single inverter
OPAMP	MAX44291	Low noise amplifier
VCO	CVCO55CL-006-0110	60-110 MHz VCO
VCO BUFF	MAX2470	Opamp buffer with diff outputs
FPGA BUFF	PL130-07	Translator buffer to LVCMOS

Most of the board components and the DUT are powered from the low noise on board LDOs. The Agilent E3631A DC power supply is used to supply 5.5V needed to power the LDOs.

The reference signal is provided by the on-board 10 MHz AOCJY crystal oscillator. The crystal has a sinewave output and works off a 3.3V bench supply since it requires more current than the on-board LDOs can provide. The testboard also has the option of bypassing the on-board crystal with an external reference signal if a different frequency is desired.

The RDIV is used to divide the reference signal down to the desired frequency. In case

Figure 5.7: Testboard used for the measurements.

the crystal or the external reference signals are at the desired frequency, the divider is bypassed. It works off a 5V power rail supplied by the HMC1060 LDO.

The reference signal is then fed into the 1:2 RBUFF. This buffer creates two LVCMOS signals from the input signal and is powered at 3.3V using the HMC1060 LDO.

One of the outputs from the RBUFF is fed into a single buffer REF BUFF, which acts as a level translator. It is powered at 1.2V using the MIC2215 LDO. The output of this buffer acts as the reference signal for the DUT.

The second output of the 1:2 RBUFF is fed into a delay line powered at 3.3V using the HMC1060 LDO. The delay line has 5 taps from 5ns to 25ns. This delay is what determines the pulse width of FWVACP current pulses as described in Section 4.1.

The output of the delay line is then fed into a single inverter PLS INV, powered at 1.2V using the MIC2215 LDO. The output of this inverter acts as the pulse_rst signal for the DUT. Refer to section 4.1 for the relationship between pulse_rst and the reference signal.

The feedback signal FB, comes from an FPGA at 3.3V and is translated to 1.2V using a single buffer FB BUFF powered at 1.2V using the MIC2215 LDO. This acts as the feedback signal for the DUT.

The test board has a 40 DIP socket to make it easier to test the different versions of the design without having to do any soldering work.

The DUT circuit blocks powered at 1.2V are supplied using MIC2215 LDO. The 3V circuit block is powered using the HMC1060 LDO.

The charge pump output ICP, is fed into a third order loop filter with a MAX44291 low noise opamp. The charge pump has a 1.2V rail which means that the maximum loop filter voltage is 1.2V but the VCO tuning range is 0.6V to 10V. In order to utilize the full VCO range, a non-inverting amplifier with a gain of 11 is added to the loop filter. To avoid amplifying the op-amp noise by the gain, the passive loop filter and the gain stage are integrated into a single active filter as shown in Figure 5.8. The unity gain bandwidth of the opamp is 10 MHz and it works off $\pm 15V$ dual supplies. The MAX44291 amplifier has CMOS inputs with 25nA input bias current so it does not draw current from the charge pump limiting the creation of spurs at the VCO

output.

Figure 5.8: Third order active loop filter with a non-inverting Opamp.

The output of the loop filter VTUNE, is used to control the VCO which is powered at 5V using the HMC1060 LDO. Its output is ac-coupled to the VCOBUFF which has differential outputs and is powered at 3.3V using the HMC1060 LDO.

The negative output is connected to the Keysight E5052B Signal Source Analyzer (SSA) to monitor its phase noise. It can also be connected to the Keysight E4448A spectrum Analyzer to monitor its spectrum.

The positive output is fed into the FPGA buffer powered at 3.3V using the HMC1060 LDO. This buffer converts the signal to LVCMOS and feeds it into the divider and the $\Sigma\Delta$ modulator.

The divider and the $\Sigma\Delta$ modulator are implemented on the ML525 Virtex5 FPGA. The programmable divider is a Multi-Modulus-Divider (MMD) based on the 2/3 cell structure described in [5]. The 2/3 cell described in [5] consists of latches but since it is not advisable to implement latches on an FPGA, the 2/3 cell is constructed from edge triggered D-type flip flops as described in [17]. Range extension was added to the MMD in order to get a wider range of division values. MMD range extension is explained in [18]. In order to get correct timing and avoid glitches, the output of the MMD is retimed on the falling edge of the input VCO signal. Figure 5.9 shows the complete structure of the MMD with range extension and retimer. It divides from 2

to 15. The $\Sigma\Delta$ modulator is a 16-bit third-order MASH 1-1-1 modulator based on the structure presented in [5].

Figure 5.9: 4-bit Programmable MMD with range extension and a retimer.

5.2.3 VCXO Characterization

The reference dominates the PLL PN at low frequency offsets therefore it is very important to have a clean reference. The AOCJY VCXO has excellent noise performance as shown in its PN profile in Figure 5.10. The PN at 1 KHz offset is -120 dBc/Hz.

Figure 5.10: Phase Noise for the 10 MHz AOCJY VCXO.

5.2.4 VCO Characterization

The VCO is a Crystek CVCO55CL-0060-0100 with the tuning curve and PN profile at 110 MHz shown in Figure 5.11 (a) and (b) respectively. The K_{VCO} is calculated to be 6.3 MHz/V and this is what is used to determine the loop filter component values. The VCO PN at 1 MHz offset is -140 dBc/Hz.

(a) Tuning Curve for the VCO.

(b) VCO PN Profile at 110 MHz.

Figure 5.11: Tuning Curve and PN Profile for the Crystek CVCO55CL-0060-0100.

5.2.5 CP DC Characterization

The loop filter was disconnected from the CP and a Keithley 2400 source meter was used to sweep the CP output voltage while measuring its current. To measure the UP current, the reference was tied high while the feedback was tied low. The reverse was done to measure the DN current. The measured results shown in Figure 5.12 (a) are similar to the simulated results in Figure 4.11. The matching between UP and DN currents is fairly decent between 0.2 V and 0.6 V. Figure 5.12 (b) shows the DC characteristics for the CP without feedback. The current sources are perfectly matched at mid-rail as expected.

(a) DC Current for CP with Feedback.

(b) DC Current for CP without Feedback.

Figure 5.12: DC Current for version 5 and version 4 of the CP.

5.2.6 Functionality of the building blocks of the FW-VACP

The building blocks of the FWVACP were tested for functionality and the results are presented below.

Voltage to Current Converter

The DC voltage on the external capacitor pin (V_{cap}) was swept while measuring the voltage at the external $400\ \Omega$ resistor (V_R). The current was calculated from the voltage drop across the resistor. The measured results in Figure 5.13 agree with the simulated results in Figure 4.8.

Figure 5.13: Voltage to Current Converter with $R = 400 \, \Omega$.

PFD Functionality

Version 1 was used to test the functionality of the PFD since it has the pulse, DN, up_pulse_on, charge and drain signals bonded out. 3 Agilent 33250A AWGs were used to provide the reference, feedback and pulse_rst signals; all at a frequency of 1 kHz.

Figure 5.14 shows a 10% pulse signal generated from the reference and pulse_rst signals. Different pulse widths can be generated by changing the position of the pulse_rst rising edge in relation to the falling edge of the reference.

Figure 5.14: Pulse signal created from reference and pulse_rst.

Figure 5.15 (a) shows the reference lagging the feedback. In this case, the DN signal is high for the duration equal to the phase difference between the signals while the up_pulse_on signal remains low as expected.

In Figure 5.15 (b), the reference leads the feedback so the up_pulse_on signal is high while the DN signal is low. Notice that the up_pulse_on signal has a 10% duty cycle as expected. Refer to Section 4.1 for details on the up_pulse_on signal.

(a) Reference lagging feedback.

(b) Reference leading feedback.

Figure 5.15: PFD signals with the reference lagging and leading the feedback.

Figure 5.16 (a) shows the pulse, DN, drain and charge signals. The drain signal goes

high on the falling edge of the pulse signal and goes low on the rising edge of the DN signal while the charge signal follows the dn signal in this case. Refer to Section 4.1 for a detailed explanation of these signals.

Figure 5.16 (b) shows the charging and discharging of a $1\ \mu\text{F}$ external capacitor with $1.2\ \text{mA}$. The capacitor in this case is charged for $162\ \mu\text{s}$ to a voltage V_{cap} of $200\ \text{mV}$. Notice that the capacitor charges for the duration equal to the charge signal and hold that voltage until the drain signal comes along and discharges it to ground.

(a) Charge and drain signals.

(b) Charging and discharging $1\ \mu\text{F}$ external capacitor with $1.2\ \text{mA}$.

Figure 5.16: Charge and drain signals that control the charging and discharging of the external capacitor.

The FWVACP UP and DN current pulses are shown in Figure 5.17 (a) and (b) respectively. The current pulses in both cases have a 10% duty cycle and their amplitude is proportional to V_{cap} as expected. It should be noted that the current increases until a phase error (θ_e greater than π) after which it remains constant until a cycle slip happens. This agrees with the transfer function in Figure 4.3.

(a) FWVACP pumping down when reference lagging feedback.

(b) FWVACP pumping up when reference leading feedback.

Figure 5.17: FWVACP pumping up and down.

5.2.7 Open Loop Measurements

To prove the validity of the proposed technique, an open loop measurement was done to monitor the spectrum of the CP current pulses. The reference was provided by the 10 MHz VCXO while the feedback signal was varied between different frequencies with an average of 10 MHz. This was accomplished by using a divider with a 3-bit accumulator to get divider values from 8 to 15 in steps of 1. In order to get an average frequency of 10 MHz, the input signal to the divider was set to 115 MHz. The VCO was bypassed and external 115 MHz signal provided by the E8257D PSG Analog Signal Generator was fed into the FPGA buffer. The output of the CP was set to midrail, 600 mV using a voltage divider to the CP rails.

The purpose for this experiment was to mimic the closed loop lock condition in fractional mode where the phase between the reference and the VCO is 0 on average. The results are shown in Figure 5.18 below.

(a) Standard CP current pulses and their FFT.

(b) FWVACP current pulses and their FFT.

Figure 5.18: CP current pulses and their FFT.

Figure 5.18 (a) shows that the standard CP current pulses have constant amplitude but variable width as expected and consequently, their FFT shows spurs at multiples of the reference frequency. Figure 5.18 (b) shows that the FWVACP current pulses have constant pulse width and variable amplitude. The FFT shows nulls at multiples of the reference frequency and a sync null at 70 MHz due to the 15% pulse width. These results agree with the Matlab simulation in Figure 5.3 and Figure 5.4.

5.2.8 Closed Loop measurements

The fractional-N PLL was designed with parameters shown in Table 5.3. The closed loop measurements were done using version 3 and 5 of the chip.

Table 5.3: Measurement Loop Parameters.

Parameter	Standard CP	FWVACP
Fref (MHz)	10	10
K_{phase} (mA/rad)	$\frac{1}{2\pi}$	$\frac{1}{2\pi}$
K_{VCO} (MHz/V)	6.3	6.3
C_1 (nF)	1330	1330
C_2 (nF)	47	47
C_3 (nF)	20	20
C_4 (nF)	2.7	2.7
R_1 (Ω)	18	18
R_2 (Ω)	10	10
R_3 (Ω)	1000	1000
I_{CP} (mA)	1	variable
MASH 1-1-1 $\Sigma\Delta$ (bits)	16	16
Loop BW (kHz)	20	20
Damping constant ζ	0.707	0.707
I_1 (mA)	N/A	1
C (pF)	N/A	22
R (k Ω)	680	680
VCO PN at 1MHz offset (dBc/Hz)	-140	-140

Loop Filter Voltage Settling Characteristics

Figure 5.19 shows the settling behavior of the loop filter voltage when the loop is locked to 56.5 MHz (divisor ratio of 11.3 and 5 MHz reference) For this measurement

the opamp is bypassed. In both cases, the loop filter voltage settles to the same value when the loop is locked. The loop has more cycle slips with the FWVACP than with the standard CP hence takes longer to settle. These results agree with the simulated results in Figure 5.1.

(a) Settling with the Standard CP.

(b) Settling with the FWVACP.

Figure 5.19: Loop Filter voltage showing PLL settling to 56.5 MHz.

PLL Output Spectrum

The spectrum of PLL output with standard CP and with FWVACP with 10% pulse width is shown in Figure 5.20. In both cases the loop is locked to 111 MHz in fractional mode with $N = 11.1$ and 10 MHz reference.

(a) Standard CP.

(b) FWVACP.

Figure 5.20: Spectrum of PLL output with standard CP and with FWVACP with 10% pulse width.

The first reference spur for standard CP is -73 dBc while that of the FWVACP is -85 dBc which is more than 10 dB lower than the standard CP. Notice that the FWVACP spurs are not completely eradicated due to non-idealities in the loop. For example the opamp input bias current, although only 25 nA it draws current from the loop filter every PFD cycle. To keep the VCO tuning voltage constant and the PLL in lock, the CP must replace this bias current every PFD cycle which modulates the tuning voltage causing reference spurs to appear at the PLL output. Also on-board coupling of the reference to the VCO. On-chip coupling of the reference directly to the CP output due to parasitics and absence of on-chip decoupling.

PLL Output Phase Noise

The PN profiles of the standard CP and FWVACP with 10% pulse width with the loop locked to 111 MHz is shown in Figure 5.21. The in-band PN is exaggerated especially at the corner frequency due to the opamp which contributes to both in-band and out of band phase noise. The in-band PN of the standard CP is about 10 dB lower than the FWVACP. The PN of the FWVACP with a 10% pulse width was expected to be lower than the standard CP because the on-time of the CP is constant and shorter than the standard CP. This is not the case in this measurement because the Voltage to Current converter is externally biased with a resistor. This bias noise due to the resistor gets amplified by the gain of the opamp in the Voltage to Current converter. The standard CP is also externally biased using a resistor but it does not have a Voltage to Current converter so its noise does not get amplified. The simulations did not show this result because the bias current used in the Voltage to Current converter was ideal i.e noiseless.

In both cases, the fractional spurs can be seen at multiples of 1 MHz as a result of having the divider set to 11.1.

(a) Standard CP.

(b) FWVACP.

Figure 5.21: PN of PLL output with standard CP and with FWVACP with 10% pulse width.

PN profiles with the standard CP and the FWVACP are shown in Figure 5.22 below. The PN of the loop with the FWVACP is shown for different pulse widths which are set using the 5-tap delay line. The value of the external resistor R is re-calculated in all cases to keep the CP current hence the loop bandwidth constant. For this measurement, the opamp is bypassed and the loop is locked in fractional mode to 58.3 MHz.

Figure 5.22: PN profile with standard CP and with FWVACP for a PLL locked to 58.3 MHz

The standard CP has lower phase noise than the FWVACP for the same reason mentioned earlier. There is no notable difference in the PN with different pulse widths of the FWVACP because the noise is dominated by the bias current going into the Voltage to Current converter and not the noise of the current sources in the CP.

Chapter 6

Conclusion

This chapter summarizes the work done in this thesis. It also talks about the shortcomings of the work and future work that will be done to improve the design.

6.1 Summary of thesis

This thesis proposed that reference spurs are a result of PWM and PPM of the charge pump current pulses. A technique that uses FWVACP current pulses was introduced to eliminate the reference spurs. To prove the validity of the proposed technique, ideal simulations were done using Matlab. The simulations showed that reference spurs were completely eradicated with the FWVACP. The standard CP and FWVACP were fabricated using the IBM 130 nm CMOS process. The spectrum of the FWVACP current pulses showed nulls at multiples of the reference frequency in open loop measurements. Closed loop measurements showed the reference spurs with FWVACP were more than 10 dB lower than with the standard CP.

6.2 Future work

The VCO, the programmable divider and $\Sigma\Delta$ modulator could be integrated on chip with the PFD and FWVACP. Integrating the VCO on chip will remove the need for an opamp in the loop filter. A test mux could be added on chip to make it easy to pipe out different signals for debug purposes. This will reduce the number of pads needed.

A bandgap reference could be included on chip to replace the noisy external resistive bias. The CP design could be improved by adding leakage current to linearize the CP. Programmability could be added to the CP current to make it possible to vary the loop bandwidth without changing the loop filter. Isolation between the analog and digital circuitry could be improved to reduce coupling of the reference to the CP. The variable delay element responsible for creating the pulse width could be incorporated on chip. Finally, decoupling could be added on chip for all supplies to improve their PSRR.

List of References

- [1] J. G. Atallah and M. Ismail, *Integrated Frequency Synthesis for Convergent Wireless Solutions*. New York: Springer, 2012.
- [2] F. M. Gardner, *Phaselock Techniques*. Hoboken, New Jersey: John Wiley & Sons Inc., 2005.
- [3] D. Derickson and M. Müller, *Digital Communications Test and Measurement: High-Speed Physical Layer Characterization*. Boston, MA: Pearson Education, Inc., 2008.
- [4] K. Iniewski, *Wireless Technologies: Circuits, Systems, and Devices*. Boca Raton, FL: CRC Press, 2008.
- [5] J. Rogers, C. Plett, and F. Dai, *Integrated Circuit Design for High-Speed Frequency Synthesis*. Norwood: Artech House, 2006.
- [6] D. K. Banerjee, *Pll Performance, Simulation and Design*. Indianapolis, IN: Dog Ear Publishing, 2006.
- [7] M. Cassia, P. Shah, and E. Bruun, “A spur-free fractional-n pll for gsm applications: linear model and simulations,” *Proceedings of the 2003 International Symposium on Circuits and Systems*, vol. 1, pp. I-1065 – I-1068 vol.1, 2003.
- [8] C. Thambidurai and N. Krishnapura, “Spur reduction in wideband plls by random positioning of charge pump current pulses,” in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 3397 – 3400, 2010.
- [9] C. Thambidurai and N. Krishnapura, “On pulse position modulation and its application to plls for spur reduction,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, pp. 1483 – 1496, 2011.
- [10] T.-C. Lee and W.-L. Lee, “A spur suppression technique for phase-locked frequency synthesizers,” in *IEEE International Solid-State Circuits Conference*, pp. 2432 – 2441, 2006.
- [11] X. Gao, E. A. M. Klumperink, G. Socci, M. Bohsali, and B. Nauta, “Spur reduction techniques for phase-locked loops exploiting a sub-sampling phase detector,” *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 1809 – 1821, 2010.
- [12] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, “A low noise sub-sampling pll in which divider noise is eliminated and pd/cp noise is not multiplied by N^2 ,” *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 3253 – 3263, 2009.

- [13] H. Huh, Y. Koo, K.-Y. Lee, Y. Ok, S. Lee, D. Kwon, J. Lee, J. Park, K. Lee, D.-K. Jeong, and W. Kim, "A cmos dual-band fractional-n synthesizer with reference doubler and compensated charge pump," in *IEEE International Solid-State Circuits Conference*, pp. 100 – 516, 2004.
- [14] C. T. Charles and D. J. Allstot, "A calibrated phase/frequency detector for reference spur reduction in charge-pump pll's," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, pp. 822 – 826, 2006.
- [15] S.-W. Hsiao, C.-C. Chen, R. Caplan, J. Galloway, B. Gray, and A. Chatterjee, "Phase-locked loop design with spo detection and charge pump trimming for reference spur suppression," in *IEEE 32nd VLSI Test Symposium (VTS)*, pp. 1 – 6, 2014.
- [16] C.-F. Liang, S.-H. Chen, and S.-I. Liu, "A digital calibration technique for charge pumps in phase-locked systems," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 390 – 398, 2008.
- [17] T.-H. Chien, C.-S. Lin, C.-L. Wey, Y.-Z. Juang, and C.-M. Huang, "High-speed and low-power programmable frequency divider," in *IEEE International Symposium on Circuits and Systems*, 2010.
- [18] C. S. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35- μ m cmos technology," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1039 – 1045, 2000.
- [19] B. C. Kuo, *Automatic Control Systems*. Upper Saddle River, NJ: Prentice Hall, 1995.
- [20] J. G. Truxal, *Automatic Feedback Control System Synthesis*. New York, NY: McGraw-Hill, 1955.

Appendix A

Background on closed loop systems and PLLs

A.1 Brief review of closed loop systems

PLLs are nonlinear circuits which can be challenging to analyze without linear models. However, the operation of many PLLs can be approximated fairly accurately with linear models. These are applicable for small phase error, a condition attainable in locked condition [2].

Figure A.1 shows an example of closed loop system. $G(s)$ represents the transfer function of the feed forward path while $H(s)$ represents that of the feedback path. $\theta_i(s)$ is the phase of the input signal, $\theta_e(s)$ is the phase error between the input and feedback signal while $\theta_o(s)$ is the phase of the output signal [19].

Figure A.1: Example of a closed loop system.

The open loop transfer function is given by:

$$\frac{\theta_o(s)}{\theta_i(s)} = G(s) \quad (\text{A.1})$$

The closed loop transfer function is given by:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{G(s)}{1 + G(s)H(s)} \quad (\text{A.2})$$

$1+G(s)H(s)=0$ is referred to as the characteristic equation (C.E). The roots of the characteristic equation become the closed loop poles of the overall transfer function. The order of the loop is the highest degree of the characteristic equation while the type of the loop is the number of poles of the loop transfer function $G(s)H(s)$ located at the origin [20]. The type of the loop can be thought of as the number of integrators in the loop gain transfer function. For example [20]:

$$\text{Let } G(s)H(s) = \frac{10}{s(s+10)} \quad (\text{A.3})$$

$$\text{Then } 1 + G(s)H(s) = 1 + \frac{10}{s(s+10)} = 0 \quad (\text{A.4})$$

Therefore the characteristic equation is:

$$C.E = s(s+10) + 10 = s^2 + 10s + 10 \quad (\text{A.5})$$

Therefore the above system is a type 1 second order system [20].

The phase error of the loop in Figure A.1 is given by:

$$\theta_e(s) = \frac{\theta_i(s)}{1 + G(s)H(s)} \quad (\text{A.6})$$

It follows that the steady state phase error is [19]:

$$\theta_e(t = \infty) = \lim_{s \rightarrow \infty} [s\theta_e(s)] \quad (\text{A.7})$$

A.1.1 Types of inputs to the loop

The input signal to the loop $\theta_i(s)$ is characterized as follows:

Phase step:

$$\theta_i(t) = \Delta\theta \quad t \geq 0 \quad (\text{A.8})$$

Or in the frequency domain:

$$\theta_i(s) = \frac{\Delta\theta}{s} \quad (\text{A.9})$$

Where $\Delta\theta$ is the magnitude of the phase step in radians. This corresponds to shifting of the phase of the input signal by $\Delta\theta$ radians.

Frequency step:

$$\theta_i(t) = \Delta\omega t \quad t \geq 0 \quad (\text{A.10})$$

Or in the frequency domain:

$$\theta_i(s) = \frac{\Delta\omega}{s^2} \quad (\text{A.11})$$

Where $\Delta\omega$ is the magnitude of the rate of change of phase in radians per second. This corresponds to an input frequency that is different from the feedback frequency. Therefore $\Delta\omega$ is the frequency difference in radians per second seen at the phase detector.

A.2 Closed loop analysis of a PLL

In the loop shown in Figure 2.1, the phase detector has a gain of K_{phase} (V/rad or A/rad) and the VCO has a gain of K_{VCO} (rads/sec.V). For this analysis, we will assume that the divider ratio N is 1.

Assuming that the loop is locked and phase detector is linear, the phase detector voltage is given by:

$$v_d(s) = K_{\text{phase}}\theta_e(s) \quad \text{where } \theta_e(s) = \theta_i(s) - \theta_o(s) \quad (\text{A.12})$$

The error voltage is processed by the loop filter which suppresses noise and high

frequency components and creates a control voltage for the VCO. Its transfer function is denoted by $F(s)$. The control voltage is given by:

$$v_c(s) = F(s)v_d(s) \quad (\text{A.13})$$

The deviation of the VCO frequency from its center frequency is given by:

$$\Delta\omega = K_{VCO}v_c(t) \quad (\text{A.14})$$

Since frequency is a derivative of phase, the VCO operation can be described as

$$\Delta\omega = \frac{d\theta_o}{dt} = K_{VCO}v_c(t) \quad (\text{A.15})$$

Taking the Laplace transform, we obtain:

$$\theta_o(s) = K_{VCO} \frac{v_c(s)}{s} \quad (\text{A.16})$$

The open loop transfer function is given by:

$$\frac{\theta_o(s)}{\theta_e(s)} = \frac{K_{phase}F(s)K_{VCO}}{s} \quad (\text{A.17})$$

The closed loop transfer function is:

$$\frac{\theta_o(s)}{\theta_e(s)} = \frac{K_{phase}F(s)K_{VCO}}{s + K_{phase}F(s)K_{VCO}} \quad (\text{A.18})$$

From Equation A.18, we can see that the PLL is always at least Type I system because of the integrator in the VCO.

A.3 Type I PLLs

The phase detector for a Type I PLL is a simple XOR gate. Figure A.3(a) shows the timing diagram while Figure A.3(b) shows the relationship between the phase

detector voltage and phase error. The maximum phase error for this phase detector is dependent on the duty cycle of the signals. For 50% duty cycle signals, the maximum phase error is 180 degrees.

Figure A.2: Type I PLL.

Figure A.3: Type I PLL Timing Diagram and Transfer Function.

The steady state VCO frequency requires a control voltage given by:

$$V_{LF} = \frac{\Delta\omega}{K_{VCO}} \quad (\text{A.19})$$

The loop filter transfer function is given by:

$$F(s) = \frac{1}{1 + sRC} = \frac{1}{1 + \frac{s}{\omega_{lpf}}} \quad (\text{A.20})$$

Where ω_{lpf} is the cut off frequency for the loop filter.

The closed loop transfer function for Type I second order PLL is given by:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_{phase}F(s)K_{VCO}}{s + K_{phase}F(s)K_{VCO}} = \frac{K_{phase}K_{VCO}\omega_{lpf}}{s^2 + s\omega_{lpf} + K_{phase}K_{vco}\omega_{lpf}} \quad (\text{A.21})$$

A.3.1 Response to various inputs

$$\theta_e(s) = \frac{s\theta_i(s)}{s + K_{phase}F(s)K_{VCO}} \quad (\text{A.22})$$

Phase step:

$$\theta_i(s) = \frac{1}{s} \quad (\text{A.23})$$

$$\theta_e(s) = \frac{s(\frac{1}{s})}{s + K_{phase}F(s)K_{VCO}} \quad (\text{A.24})$$

$$\theta_e(t = \infty) = \lim_{s \rightarrow 0} \left[s \left(\frac{s(\frac{1}{s})}{s + K_{phase}F(s)K_{VCO}} \right) \right] = 0 \quad (\text{A.25})$$

Therefore the steady state phase error for type I PLL with a phase step at the input is 0. The frequency settles to the same value since there is no change in control voltage.

Frequency step:

$$\theta_i(s) = \frac{1}{s^2} \quad (\text{A.26})$$

$$\theta_e(s) = \frac{s(\frac{1}{s^2})}{s + K_{phase}F(s)K_{VCO}} \quad (\text{A.27})$$

$$\theta_e(t = \infty) = \lim_{s \rightarrow 0} \left[s \left(\frac{s(\frac{1}{s^2})}{s + K_{phase}F(s)K_{VCO}} \right) \right] = \frac{1}{K_{phase}F(s)K_{VCO}} \quad (\text{A.28})$$

Therefore Type I PLL with a frequency step at the input will have a finite phase error in steady state. From Equation A.28 we can see that a steady state phase error in a Type I PLL cannot be avoided but can be reduced by increasing the loop gain but this makes the loop less stable. This loop is locked if the phase difference is constant. In order to achieve zero steady state phase error, a Type II loop is used.

Figure 1.4: Block diagram of a simplified PLL.

1.2 Thesis Outline

Chapter 1 offered a brief introduction to frequency synthesis and the various architectures of frequency synthesizers. Chapter 2 discusses the theory of PLLs and explains integer and fractional PLLs in detail. Motivation for this work, as well as work similar to this one is also presented in this chapter. Chapter 3 explains in detail the origin of reference spurs, examines the nature of the CP current pulses and explains the proposed technique for eradicating reference spurs. The functionality and circuit design of the proposed Fixed Width Variable Amplitude Charge Pump (FWVACP) is detailed in chapter 4. The simulation and measurement results are presented in chapter 5. Lastly, a summary of the work presented in this thesis, future work and conclusions are presented in chapter 6.

function and therefore, controls its transient response. The output signal frequency of the VCO is proportional to the control voltage at its input. The VCO output is then divided by N and fed back into the phase detector to complete the loop. It follows that the output frequency is N times the reference frequency. This means that integer multiples of the reference frequency can be generated from a single reference by changing the divider ratio.

Figure 2.1: Phase Locked Loop.

The open loop transfer function is given by:

$$\frac{\theta_o(s)}{\theta_e(s)} = \frac{K_{phase}F(s)K_{vco}}{s} \quad (2.1)$$

The closed loop transfer function is:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_{phase}F(s)K_{vco}}{s + K_{phase}F(s)K_{vco}} \quad (2.2)$$

Refer to Appendix A for a detailed derivation of these transfer functions.

2.2 Types of PLLs

The type of loop refers to the number of integrators in the loop transfer function. From the PLL transfer functions in Equation 2.1 and Equation 2.2 we can see that it is at least a Type I system. Refer to Appendix A for details on Type I PLLs. The work in this thesis is based on a Type II PLL, which has 0 phase error in steady state as detailed below.

In a Type II PLL shown in Figure 2.2, the phase detector is edge triggered and produces an up (UP) or a down (DN) pulse depending on whether the reference leads or lags the VCO output as shown in its timing diagram in Figure 2.3(a). This phase

detector is referred to as a phase frequency detector (PFD). In this example, the PFD operates on the rising edge. If the reference is leading the VCO, the UP signal goes high and it is reset when the rising edge of the VCO comes along. The duration of the pulse is proportional to the phase difference between the two signals. The UP signal causes current I to flow to the capacitor producing a finite voltage V_c , which controls the VCO. In the case of the VCO leading the reference, a DN pulse causes current I to flow from the capacitor to ground.

Figure 2.2: Type II PLL.

Figure 2.3: Type II PLL Timing Diagram and Transfer Function.

The voltage accumulated across the capacitor is proportional to the phase error and is given by:

$$v_c(s) = i\theta_e \frac{1}{sC} \quad (2.3)$$

This means that PFD/CP capacitor combination behaves as an integrator. This integrator in addition to the integrator in the VCO (i.e., K_{vco}/s) makes this PLL a Type II.

The gain of the PFD/CP is given by:

increases and phase noise goes up as $20\log N$.

Figure 2.4: Integer-N PLL.

An ideal integer-N PLL, once settled i.e. the phase error is zero, will output zero current from the charge pump as the loop filter holds the necessary voltage for the VCO to produce the desired frequency.

2.4 Fractional-N PLLs.

A fractional-N PLL shown in Figure 2.5 generates an output signal with a frequency resolution that is a fraction of the reference frequency. This means that a higher reference frequency, which in turn leads to lower phase noise, can be used while maintaining small channel spacing. The fractional divider ratios are generated by a sigma delta ($\Sigma\Delta$) modulator. It works by dithering between integer values for each reference period whose average is the desired divider ratio. Its resolution can be increased by increasing the number of bits in the accumulators (refer to [5] for a detailed discussion on $\Sigma\Delta$ modulators). A first order $\Sigma\Delta$ modulator is the simplest case in which it dithers between two values. Higher order $\Sigma\Delta$ modulators dither between two or more values. The dithering action pushes the fractional spurs and noise to higher frequencies where they are filtered out by the low pass filtering of the PLL transfer function [6].

Figure 2.5: Fractional-N PLL.

A fractional-N PLL is never truly settled because of the dithering provided by the $\Sigma\Delta$ modulator. This means the current from the charge pump will never settle to zero, although it will average to zero. The charge pump generates current pulses at the reference frequency in response to the $\Sigma\Delta$ modulator.

2.5 Challenges in PLL design

Just like all circuits, PLLs have design challenges associated with them; the greatest being phase noise and frequency spurs in the output signal. Both of these corrupt the signal integrity in the communication system and therefore must be minimized. Phase noise contains noise components at many frequencies whose phase and amplitude are random with respect to the carrier. Phase noise degrades the Signal-to-Noise Ratio (SNR) in a communication system. Spurs differ from phase noise in that they appear as distinct spikes in frequency that rise above the noise floor at deterministic offsets from the carrier. They inter-modulate with other signals in the communication system producing higher-order products which can fall in the desired channel.

There are two types of spurs; reference spurs and fractional spurs. Reference spurs are offset from the carrier frequency by integer multiples of the reference frequency. On the other hand, the position of fractional spurs depends on the dithering action of the $\Sigma\Delta$ modulator.

Reference spurs are a result of a ripple on the VCO control line, which results in frequency components at offsets of the reference frequency and its harmonics. This can be thought of as the VCO output being modulated by the reference. The source

which means that the reference spur will translate all the adjacent channels to the center of the desired channel as shown in Figure 2.6. These undesired channels appear as an elevated noise floor to the desired channel and limit the SNR.

Figure 2.6: Adjacent Channel Interference due to Reference Spurs.

A number of techniques have been developed to tackle the problem of spurs, two of them are sample and hold and pulse position modulation. These techniques are discussed in detail in the next section. Although these techniques lower the spur amplitude, neither of them actually eliminates these spurs. The motivation for this work is to develop a technique that would completely eradicate the reference spurs. This is achieved by creating nulls at frequency offsets equal to multiples of the reference frequency from the carrier, essentially getting rid of the reference spurs. Chapter 3 explains this technique in detail.

2.7 Literature review

This section covers techniques that have been developed to minimize reference spurs. These include sample and hold, Pulse Position Modulation (PPM), sub-sampling, analog and digital calibration techniques and improved charge pump designs. A summary of each of these techniques is presented below:

2.7.1 Sample and Hold

The sampling of the PFD/CP is non-uniform because the PFD produces variable width pulses aligned to either the reference or VCO output depending on which edge comes first as shown in Figure 2.7. A sample and hold (S/H) block is introduced between the CP and the loop filter as shown in Figure 2.8. After every UP or DOWN pulse, the S/H block samples the voltage across the integrating capacitor and holds it for the reference cycle. By sampling the CP output at regular time intervals, the non-uniform sampling of the PFD/CP is removed. The S/H block also prevents the modulation of the loop filter voltage by the reference signal which eliminates reference spurs in the VCO output. [7].

Figure 2.7: Non-uniform Sampling.

Figure 2.8: S/H $\Sigma\Delta$ Fractional-N Synthesizer [7].

Figure 2.9: Generic Sub-Sampling PLL (SSPLL) Architecture [11].

2.7.4 Charge Pump design

[13] uses a frequency doubler in the reference path to push the reference spurs to a higher frequency where they can be attenuated by the loop filter. Additionally, a replica of the CP and bias controller are used as a current compensation controller to reduce the current mismatch between the up and down currents.

2.7.5 Analog and digital calibration to minimize reference spurs

[14–16], employ analog and digital CP calibration techniques to minimize reference spurs at the output.

[14] takes advantage of the fact that the magnitude of the disturbance on the VCO control line which results in reference spurs is proportional to the width of the current pulses on the VCO control input when the PLL is locked. It uses a variable delay element in the reset path of the PFD and adjusts the delay using feedback to make the locked pulsewidth approach zero. The feedback circuitry ensures that the overall PFD delay is positive to avoid a DZ. The size of the pulse width can be arbitrarily small by increasing the size of the resistor in the feedback loop as shown in Figure 2.10.

The drawbacks of this technique is that it assumes that all other PLL components

behave in an ideal manner, which is unrealistic. The replicated PFD/CP that creates the delay control voltage, to avoid interfering with loop dynamics, increases complexity and layout area. Lastly, the time constant associated with the feedback capacitor may be too long to make this technique feasible in PLLs that require fast settling times.

Figure 2.10: Block Diagram of the Technique used in [14].

The CP in [15] is designed with current programmability in the discharge path and uses a Static Phase Offset (SPO) detector to indicate whether the reference is leading or lagging the output. An off-chip calibration scheme is used to determine the optimum charge pump current ratio to minimize current mismatch and the resulting reference spurs. The drawback of this technique is that the CP has a finite number of steps (16 in this case) which may not be enough to provide an optimum solution for minimizing reference spurs. Also the increased number of devices in the discharge path increases the noise in the system.

[16] uses a switched delay PFD to switch between an enlarged reset delay when the loop is not locked and a normal reset delay when the loop is locked and the calibration completed. Like [15], the discharge path has digitally controlled current sources. The lock detect indicates when the calibration should begin while the Bang Bang Phase Detector (BBPD) provides phase comparison between UP and DN controlling signals to provide information for the Successive Approximation Register (SAR) controller.

3.1 PPM and PWM and how they relate to Charge Pump Current Pulses

Figure 3.1 shows an example of charge pump current pulses in a typical fractional-N PLL. The charge pump current pulses are affected in two ways by the reference and the feedback signals. Firstly, the width of the charge pump pulses is dependent on the spacing between the rising edges of the two signals i.e. the phase difference between the two signals. This leads to Pulse Width Modulation (PWM). Secondly, the charge pump current pulse may occur before or after the reference rising edge depending on whether the reference leads or lags the feedback. This leads to Pulse Position Modulation (PPM). It is these two factors that cause the charge pump current pulses to generate reference spurs. Other non-idealities such as charge pump mismatch can worsen reference spurs, but their origin is the nature of the pulses.

Figure 3.1: Example of CP Current Pulses in a Typical Fractional-N PLL.

Matlab was used to analyze the effect of the nature of charge pump pulses and the results are shown in Figure 3.2 and Figure 3.3.

Figure 3.2 and Figure 3.3 demonstrate PWM and PPM respectively using 10 MHz pulse trains. In Figure 3.2(a), the pulses appear at constant time intervals but have varying widths while the pulses have a constant width but appear at varying time intervals in Figure 3.3(a). Both spectrums show spurs at 10 MHz and its harmonics in 3.2(b) and Figure 3.3(b).

Figure 3.2: A Pulse Train with PWM and its Spectrum.

Figure 3.3: A Pulse Train with PPM and its Spectrum.

3.2 Mathematical Analysis of Fixed Width Variable Amplitude Pulse Train

This section shows a mathematical analysis of how reference spurs are eliminated from the charge pump output by eliminating PWM and PPM. This is done so by generating a fixed width variable amplitude (FWVA) pulse. In a typical PLL, PPM and PWM modulation are responsible for representing phase error information. With a FWVA pulse, phase error information is stored in the amplitude of the pulse. A generic FWVA pulse train is shown in Figure 3.4.

Figure 3.4: A Generic Pulse Train. a) shows a Continuous Signal. b) shows the Signal after Sampling.

A few restrictions must be placed on the signal; the width of each pulse must be equal and the spacing between each pulse must also be equal. The amplitude of each pulse is set to be arbitrary to solve the general case, and is defined as $a_1 \dots a_p$. Finally, the signal must be periodic.

Discrete Fourier analysis will be used to examine the frequency spectrum of this signal. What the analysis will show is a total cancellation of the frequency components at frequencies related to the beginning edges of each pulse. These frequencies are analogous to integer multiples of the reference frequency in a PLL.

The signal in Figure 3.4(a) is continuous in the time domain. This signal is sampled in order to use discrete-time Fourier analysis. Figure 3.4(b) shows the signal after it has been sampled.

Now we define the discrete signal $x(n)$ based on Figure 3.4.

$$x(n) = \{a_1 a_1 \dots a_1 \ 00 \dots 00 \ a_2 a_2 \dots a_2 \ 00 \dots 00 \ a_p a_p \dots a_p \ 00 \dots 00\} \quad (3.1)$$

Using the discrete Fourier equation we can come up with the spur amplitudes of the reference frequencies. To begin we turn to the analysis equation for discrete-time

Figure 3.5: Sample FWVA Signal in the Time Domain.

Figure 3.6 shows the frequency domain of the signal. Note the nulls that occur every 10 MHz as predicted by Equation 3.4. We also notice the sync function shape has a null at 100 MHz. Having a 10% pulse width gives the first sync null at 10 times the reference. Having a pulse width of 100% would put the sync pulse null on top of the first reference pulse null. This implies that the first reference frequency is the furthest the sync pulse null can be pulled in.

Figure 3.6: Sample FWVA Signal in Frequency Domain.

This result can be exploited to target spurs at any frequency outside the first reference frequency by choosing the appropriate pulse width. Equation 3.8 can be used to find the appropriate pulse width to create a sync null at the spur frequency F_{spur} .

$$\text{pulse width} = \frac{F_{ref}}{F_{spur}} \cdot 100\% \quad (3.8)$$

For example, a PLL with a 10 MHz reference frequency has spurs at 70 MHz offset from the VCO center frequency. The spurs can be eliminated by creating sync nulls at 70 MHz. The appropriate pulse width is calculated to be 14.3% using Equation

3.8. Figure 3.7 (a) shows the pulse train used to create a sync null at 70 MHz and its spectrum in (b).

Figure 3.7: Removing a spur at 70 MHz by setting the pulse width to 14.3%.

Figure 4.1: Implementation of the FWVACP.

Figure 4.2: Timing Diagram for the FWVACP.

The key idea for the design of the FWVACP is that the output current pulses are of a fixed width set by the width of the PULSE signal. The PULSE signal is generated from the reference signal F_{ref} . PULSE goes high on the falling edge of F_{ref} (refer to Figure 4.2) to close either 'up pulse switch' or 'dn pulse switch' for a pre-determined fixed time set by the delay element t_{pulse} . It is important to note that PULSE has the same frequency as F_{ref} .

$$K_{phase} = \frac{I_{ave}}{\theta_e} = \frac{K I_1 t_{pulse}}{2\pi C} \quad (4.5)$$

The average current is plotted as a function of the phase difference as shown in Figure 4.3. The result can be interpreted as a transfer function of the FWVACP. The capacitor C charges for a maximum time equal to half the reference period (equivalent to a phase error of π). Even if the phase error is larger than π , the ‘charge switch’ must open to allow a constant amplitude current to be delivered to the loop filter. This is the reason for the flat region of the transfer function shown in Figure 4.3. The maximum phase error is 2π , after which the pattern repeats.

Figure 4.3: Average output current vs. phase for PFD and FWVACP.

4.3 Design Flow

The tristate PFD and the building blocks of the FWVACP were implemented at transistor level in cadence using IBM 130nm CMOS technology. Below is a detailed description of the transistor level design of the tristate PFD and the FWVACP blocks shown in Figure 4.1.

4.3.1 Tristate PFD

The tristate PFD in Figure 4.4 is positive edge triggered and is constructed from two D-flip-flops with an active low reset and an AND gate. A delay of about 2 ns is added

Figure 4.6: Charging and Discharging a 20 pF Capacitor with 500 uA.

4.3.3 Voltage to Current Converter

The voltage to current converter is constructed from an op-amp with negative feedback as shown in Figure 4.7. Current I_2 is the ratio of the voltage on the charging capacitor, V_{cap} and the external resistor R . This current is used as the bias current for the CP current sources.

Figure 4.7: Voltage to Current Converter.

In order to get a wider linear range for input voltage V_{cap} , a 3 V supply is used in

this block instead of a 1.2 V supply. Consequently, 3.3 V transistors that can handle the 3 V supply are used in this block. Figure 4.8 shows that this circuit has an input range of 0 to 1.4 V which is sufficient to produce the appropriate current for the CP current sources since the maximum V_{cap} voltage is 1.2 V.

Figure 4.8: Voltage to Current Converter with $R = 400 \Omega$ and $C = 20 \text{ pF}$.

Figure 4.9 shows a basic CMOS op-amp with two gain stages that was used in the voltage to current converter circuit. It has a gain of 80 dB and 75 degrees of phase margin.

Figure 4.9: Basic CMOS 2-Stage Op-amp.

Figure 4.11: Charge pump DC-Characteristics.

4.3.5 Phase Noise of the PFD/FWVACP

The Phase Noise (PN) of the PFD/FWVACP was simulated and the results are shown in Figure 4.12. The simulation is set-up such that the PFD is operating with 2 ns of offset and the CP is pumping up. At 100 kHz the PN is -135 dBc/Hz. The largest noise contributors are the bias transistors in the current mirror.

Figure 4.12: PFD/FWVACP Phase Noise.

4.3.6 Layout of FWVACP

The layout of the PFD/FWVACP in Figure 4.13 is approximately 800 μm x 800 μm . The switching circuitry of the PFD and FWVACP logic is placed at the top while the CP is placed at the bottom to minimize the coupling of these signals to the CP. Coupling of these signals to the CP directly affects the reference spur performance of the PFD/CP. The analog and digital circuitry have dedicated supplies (VDD_DIG and VDD_ANLG) to further reduce interaction between them.

Figure 4.13: Layout of PFD/FWVACP.

Figure 5.1: Loop filter voltage showing settling for a 5.3 MHz frequency step and charge pump current during a cycle slip.

5.1.2 FFT of Charge Pump Current Pulses and VCO Spectrum

Figure 5.2: Standard CP and FWVACP current pulses when the loop is settled.

Figure 5.2 shows the standard CP and FWVACP pulses when the loop is settled. Notice the constant amplitude but varying width pulses of the standard CP versus the varying amplitude but constant width pulses of the FWVACP.

Figure 5.3(a) and (b) show the FFT of the standard CP current pulses and the spectrum of the VCO output respectively. The reference spurs in the CP directly appear in the VCO output at offsets equal to multiples of the 10MHz. These spurs are entirely due to the nature of the current pulses as discussed in Chapter 3 since an ideal CP is used i.e. the UP and DN currents are perfectly matched.

(a) FFT of standard CP current pulses.

(b) Spectrum of the VCO output.

Figure 5.3: FFT of standard CP current pulses and VCO output spectrum with PLL locked to 100.3 MHz.

The FFT of the FWVACP current pulses is shown in Figure 5.4(a). The reference spurs in 5.3(a) have now been replaced with reference nulls visible at multiples of 10 MHz. The sync null appears at 100 MHz as expected with a 10% pulse width. The reference nulls in Figure 5.4(a) cause nulls to appear in the VCO output at multiples of 10 MHz offset from the VCO frequency as shown in Figure 5.4(b). This shows that the FWVACP has effectively eradicated the reference spurs from the VCO output.

(a) FFT of FWVACP current pulses.

(b) Spectrum of the VCO output.

Figure 5.4: FFT of FWVACP (10% pulse width) current pulses and VCO output spectrum with PLL locked to 100.3 MHz.

Figure 5.5: PLL Phase noise for standard CP and FWVACP with different pulse widths.

5.2 Measurement Results

The FWVACP and standard CP were fabricated using IBM 0.13 μm CMOS technology. The building blocks of the FWVACP were tested for functionality followed by closed loop measurements with both CPs. The measurement setup is described in section 5.2.2.

5.2.1 Die Micrograph

Both the FWVACP and the standard CP were incorporated on the same chip. Different versions of the designs were included on the chip in order to use up the available 2mm x 2mm area as shown in Figure 5.6. Because of the placement of the pads, multiple bonding options were used to test the different versions. A DIP40 package was chosen since it has enough pins to support all the bonding options without shorting pins between versions.

Figure 5.6: Die Micrograph.

The idea for the multiple versions was to compare performance with different CP topologies. The versions are listed below:

- Version 1: PFD/FWVACP - basic CP with switches in signal path.
- Version 2: PFD/FWVACP - basic CP with switches out of signal path.
- Version 3: PFD/FWVACP - CP with feedback and with switches in the signal path as shown in Figure 4.10.
- Version 4: PFD/Standard CP - basic CP with switches in signal path.
- Version 5: PFD/Standard CP - CP with feedback and with switches in the signal path as shown in Figure 4.10.
- Version 6: Opamp - 3V opamp used in the voltage to current converter as shown in Figure 4.9.

Figure 5.7: Testboard used for the measurements.

output.

Figure 5.8: Third order active loop filter with a non-inverting Opamp.

The output of the loop filter VTUNE, is used to control the VCO which is powered at 5V using the HMC1060 LDO. Its output is ac-coupled to the VCOBUFF which has differential outputs and is powered at 3.3V using the HMC1060 LDO.

The negative output is connected to the Keysight E5052B Signal Source Analyzer (SSA) to monitor its phase noise. It can also be connected to the Keysight E4448A spectrum Analyzer to monitor its spectrum.

The positive output is fed into the FPGA buffer powered at 3.3V using the HMC1060 LDO. This buffer converts the signal to LVCMOS and feeds it into the divider and the $\Sigma\Delta$ modulator.

The divider and the $\Sigma\Delta$ modulator are implemented on the ML525 Virtex5 FPGA. The programmable divider is a Multi-Modulus-Divider (MMD) based on the 2/3 cell structure described in [5]. The 2/3 cell described in [5] consists of latches but since it is not advisable to implement latches on an FPGA, the 2/3 cell is constructed from edge triggered D-type flip flops as described in [17]. Range extension was added to the MMD in order to get a wider range of division values. MMD range extension is explained in [18]. In order to get correct timing and avoid glitches, the output of the MMD is retimed on the falling edge of the input VCO signal. Figure 5.9 shows the complete structure of the MMD with range extension and retimer. It divides from 2

to 15. The $\Sigma\Delta$ modulator is a 16-bit third-order MASH 1-1-1 modulator based on the structure presented in [5].

Figure 5.9: 4-bit Programmable MMD with range extension and a retimer.

5.2.3 VCXO Characterization

The reference dominates the PLL PN at low frequency offsets therefore it is very important to have a clean reference. The AOCJY VCXO has excellent noise performance as shown in its PN profile in Figure 5.10. The PN at 1 KHz offset is -120 dBc/Hz.

Figure 5.10: Phase Noise for the 10 MHz AOCJY VCXO.

5.2.4 VCO Characterization

The VCO is a Crystek CVCO55CL-0060-0100 with the tuning curve and PN profile at 110 MHz shown in Figure 5.11 (a) and (b) respectively. The K_{VCO} is calculated to be 6.3 MHz/V and this is what is used to determine the loop filter component values. The VCO PN at 1 MHz offset is -140 dBc/Hz.

(a) Tuning Curve for the VCO.

(b) VCO PN Profile at 110 MHz.

Figure 5.11: Tuning Curve and PN Profile for the Crystek CVCO55CL-0060-0100.

5.2.5 CP DC Characterization

The loop filter was disconnected from the CP and a Keithley 2400 source meter was used to sweep the CP output voltage while measuring its current. To measure the UP current, the reference was tied high while the feedback was tied low. The reverse was done to measure the DN current. The measured results shown in Figure 5.12 (a) are similar to the simulated results in Figure 4.11. The matching between UP and DN currents is fairly decent between 0.2 V and 0.6 V. Figure 5.12 (b) shows the DC characteristics for the CP without feedback. The current sources are perfectly matched at mid-rail as expected.

(a) DC Current for CP with Feedback.

(b) DC Current for CP without Feedback.

Figure 5.12: DC Current for version 5 and version 4 of the CP.

5.2.6 Functionality of the building blocks of the FW-VACP

The building blocks of the FWVACP were tested for functionality and the results are presented below.

Voltage to Current Converter

The DC voltage on the external capacitor pin (V_{cap}) was swept while measuring the voltage at the external $400\ \Omega$ resistor (V_R). The current was calculated from the voltage drop across the resistor. The measured results in Figure 5.13 agree with the simulated results in Figure 4.8.

Figure 5.13: Voltage to Current Converter with $R = 400 \, \Omega$.

PFD Functionality

Version 1 was used to test the functionality of the PFD since it has the pulse, DN, up_pulse_on, charge and drain signals bonded out. 3 Agilent 33250A AWGs were used to provide the reference, feedback and pulse_rst signals; all at a frequency of 1 kHz.

Figure 5.14 shows a 10% pulse signal generated from the reference and pulse_rst signals. Different pulse widths can be generated by changing the position of the pulse_rst rising edge in relation to the falling edge of the reference.

Figure 5.14: Pulse signal created from reference and pulse_rst.

Figure 5.15 (a) shows the reference lagging the feedback. In this case, the DN signal is high for the duration equal to the phase difference between the signals while the up_pulse_on signal remains low as expected.

In Figure 5.15 (b), the reference leads the feedback so the up_pulse_on signal is high while the DN signal is low. Notice that the up_pulse_on signal has a 10% duty cycle as expected. Refer to Section 4.1 for details on the up_pulse_on signal.

(a) Reference lagging feedback.

(b) Reference leading feedback.

Figure 5.15: PFD signals with the reference lagging and leading the feedback.

Figure 5.16 (a) shows the pulse, DN, drain and charge signals. The drain signal goes

high on the falling edge of the pulse signal and goes low on the rising edge of the DN signal while the charge signal follows the dn signal in this case. Refer to Section 4.1 for a detailed explanation of these signals.

Figure 5.16 (b) shows the charging and discharging of a $1\ \mu\text{F}$ external capacitor with $1.2\ \text{mA}$. The capacitor in this case is charged for $162\ \mu\text{s}$ to a voltage V_{cap} of $200\ \text{mV}$. Notice that the capacitor charges for the duration equal to the charge signal and hold that voltage until the drain signal comes along and discharges it to ground.

(a) Charge and drain signals.

(b) Charging and discharging $1\ \mu\text{F}$ external capacitor with $1.2\ \text{mA}$.

Figure 5.16: Charge and drain signals that control the charging and discharging of the external capacitor.

The FWVACP UP and DN current pulses are shown in Figure 5.17 (a) and (b) respectively. The current pulses in both cases have a 10% duty cycle and their amplitude is proportional to V_{cap} as expected. It should be noted that the current increases until a phase error (θ_e greater than π) after which it remains constant until a cycle slip happens. This agrees with the transfer function in Figure 4.3.

(a) FWVACP pumping down when reference lagging feedback.

(b) FWVACP pumping up when reference leading feedback.

Figure 5.17: FWVACP pumping up and down.

5.2.7 Open Loop Measurements

To prove the validity of the proposed technique, an open loop measurement was done to monitor the spectrum of the CP current pulses. The reference was provided by the 10 MHz VCXO while the feedback signal was varied between different frequencies with an average of 10 MHz. This was accomplished by using a divider with a 3-bit accumulator to get divider values from 8 to 15 in steps of 1. In order to get an average frequency of 10 MHz, the input signal to the divider was set to 115 MHz. The VCO was bypassed and external 115 MHz signal provided by the E8257D PSG Analog Signal Generator was fed into the FPGA buffer. The output of the CP was set to midrail, 600 mV using a voltage divider to the CP rails.

The purpose for this experiment was to mimic the closed loop lock condition in fractional mode where the phase between the reference and the VCO is 0 on average. The results are shown in Figure 5.18 below.

(a) Standard CP current pulses and their FFT.

(b) FWVACP current pulses and their FFT.

Figure 5.18: CP current pulses and their FFT.

Figure 5.18 (a) shows that the standard CP current pulses have constant amplitude but variable width as expected and consequently, their FFT shows spurs at multiples of the reference frequency. Figure 5.18 (b) shows that the FWVACP current pulses have constant pulse width and variable amplitude. The FFT shows nulls at multiples of the reference frequency and a sync null at 70 MHz due to the 15% pulse width. These results agree with the Matlab simulation in Figure 5.3 and Figure 5.4.

5.2.8 Closed Loop measurements

The fractional-N PLL was designed with parameters shown in Table 5.3. The closed loop measurements were done using version 3 and 5 of the chip.

(a) Settling with the Standard CP.

(b) Settling with the FWVACP.

Figure 5.19: Loop Filter voltage showing PLL settling to 56.5 MHz.

PLL Output Spectrum

The spectrum of PLL output with standard CP and with FWVACP with 10% pulse width is shown in Figure 5.20. In both cases the loop is locked to 111 MHz in fractional mode with $N = 11.1$ and 10 MHz reference.

(a) Standard CP.

(b) FWVACP.

Figure 5.20: Spectrum of PLL output with standard CP and with FWVACP with 10% pulse width.

(a) Standard CP.

(b) FWVACP.

Figure 5.21: PN of PLL output with standard CP and with FWVACP with 10% pulse width.

PN profiles with the standard CP and the FWVACP are shown in Figure 5.22 below. The PN of the loop with the FWVACP is shown for different pulse widths which are set using the 5-tap delay line. The value of the external resistor R is re-calculated in all cases to keep the CP current hence the loop bandwidth constant. For this measurement, the opamp is bypassed and the loop is locked in fractional mode to 58.3 MHz.

Figure 5.22: PN profile with standard CP and with FWVACP for a PLL locked to 58.3 MHz

The standard CP has lower phase noise than the FWVACP for the same reason mentioned earlier. There is no notable difference in the PN with different pulse widths of the FWVACP because the noise is dominated by the bias current going into the Voltage to Current converter and not the noise of the current sources in the CP.

Appendix A

Background on closed loop systems and PLLs

A.1 Brief review of closed loop systems

PLLs are nonlinear circuits which can be challenging to analyze without linear models. However, the operation of many PLLs can be approximated fairly accurately with linear models. These are applicable for small phase error, a condition attainable in locked condition [2].

Figure A.1 shows an example of closed loop system. $G(s)$ represents the transfer function of the feed forward path while $H(s)$ represents that of the feedback path. $\theta_i(s)$ is the phase of the input signal, $\theta_e(s)$ is the phase error between the input and feedback signal while $\theta_o(s)$ is the phase of the output signal [19].

Figure A.1: Example of a closed loop system.

detector voltage and phase error. The maximum phase error for this phase detector is dependent on the duty cycle of the signals. For 50% duty cycle signals, the maximum phase error is 180 degrees.

Figure A.2: Type I PLL.

Figure A.3: Type I PLL Timing Diagram and Transfer Function.

The steady state VCO frequency requires a control voltage given by:

$$V_{LF} = \frac{\Delta\omega}{K_{VCO}} \quad (\text{A.19})$$

The loop filter transfer function is given by:

$$F(s) = \frac{1}{1 + sRC} = \frac{1}{1 + \frac{s}{\omega_{lpf}}} \quad (\text{A.20})$$

Where ω_{lpf} is the cut off frequency for the loop filter.

The closed loop transfer function for Type I second order PLL is given by:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_{phase}F(s)K_{VCO}}{s + K_{phase}F(s)K_{VCO}} = \frac{K_{phase}K_{VCO}\omega_{lpf}}{s^2 + s\omega_{lpf} + K_{phase}K_{vco}\omega_{lpf}} \quad (\text{A.21})$$