A 0.18 μm CMOS Half-Rate Clock and Data Recovery Circuit with Reference-less Dual Loop

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Abstract

The Clock and Data Recovery (CDR) circuit is one of the most important and commonly used components in data communications applications such as in optical fiber backbones, chip-to-chip interconnections and wireless communications. The increasing growth of data transportation requires communication systems to operate at a higher speed, and the design of CDRs becomes more challenging due to the higher input data rate. Some novel structures and specific techniques are necessary in order to achieve better jitter performance, lower power dissipation, and easier integration of CDRs.

This thesis introduces some different CDRs such as half-rate and full-rate CDRs, and linear and bang-bang CDRs. Their characteristics are compared. As well, a PLL-based CDR is discussed in more detail. CDR building blocks such as VCOs, charge pumps, phase and frequency detectors, and loop filters are also discussed.

A half-rate CDR circuit based on bang-bang phase and frequency detector (PFD) is presented. This CDR with reference-less dual loops is implemented in 0.18 μm CMOS technology, and a switching circuitry is used to achieve a smooth transition between the frequency locked loop (FLL) and the phase locked loop (PLL). Measurement results such as eye diagrams, power spectrum, and phase noise are shown. The phase noise of the recovered clock at a 1 MHz offset is -93.47 dBc/Hz with 2.0 Gb/s input data rate.

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List of Abbreviations

BER	Bit Error Rate
CDR	Clock and Data Recovery
CFP	Ceramic Flat Pack
CMC	Canadian Microelectronics Corporation
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
DETFF	Double Edge Triggered Flip Flop
DFF	D Flip Flop
DRC	Design Rule Check
FD	Frequency Detector
FF	Flip Flop
FLL	Frequency Locked Loop
LVS	Layout Versus Schematic
MOS	Metal Oxide Semiconductor
MOSFET	MOS Field Effect Transistor
Mux	Multiplexer
NMOS	N-channel MOSFET
NRZ	Non Return Zero
PCB	Printed Circuit Board

PD	Phase Detector
PFD	Phase and Frequency Detector
PLL	Phase-Locked Loop
PMOS	P-channel MOSFET
PRBS	Pseudo Random Binary Sequence
RMS	Root Mean Square
SCR	Silicon Controlled Rectifier
SERDES	Serializer/Deserializer
SNR	Signal to Noise Ratio
TSMC	Taiwan Semiconductor Manufacturing Company
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration
XOR	Exclusive OR Gate

1.1 Thesis motivation

The communication technique of combining the clock and data at transmitters ensures that the clock and data signals always arrive simultaneously at the receivers. The combination of clock and data at transmitters can reduce the complexity of the interface design, the interconnects, output lines and system size. The most significant benefit of the combination technique is that the clocks of the transmitter and the receiver are independent. Therefore, the distortion and jitter of the incoming data can be removed for further signal processing. However, the separation of the clock and data from the serial input data at the receivers requires a Clock and Data Recovery (CDR) circuit whose function is to extract clock information and to recover data signals from an input serial data stream.

CDR circuits are widely used in high-speed data communications such as optical transceivers, wireless communications, and chip-to-chip interconnections. The CDR technology is extremely important as the demand for much greater bandwidth has grown rapidly for data transmission. The CDR circuit design becomes one of most challenging blocks of building high-speed data links due to the continuous growth of the input data rate and the block complexity.

The Phase-Locked Loop (PLL)-based CDR is a popular architecture that has been used for transceiver design in recent years. The idea of PLL-based CDRs is that, during

each data transition, the phase detector compares the data transition to the clock edge and produces a signal. The signal, which represents phase error, drives a charge pump to adjust the frequency of the internal clock. If the incoming data leads the clock, the clock is sped up. If the incoming data lags the clock, the clock is slowed down. The clock frequency is kept constant and the CDR loop is locked if the data transition and the clock edge are exactly aligned.

1.2 Thesis contributions

The contributions of this research are outlined as follows:

1. A novel acquisition mode switching circuitry from FLL to PLL is employed to avoid potential loss of loop lock. A variable time constant loop filter is introduced to support the CDR acquisition.
2. A complete CDR circuit that achieves both frequency and phase acquisition was implemented. The design follows the concepts reported in [1], [2], [3], but a four-stage ring oscillator with a coarse and fine control is used in the dual-loop structure, along with the FLL to PLL mode switching circuitry.
3. The CDR building blocks are fabricated with 0.18 μm CMOS technology, and experimental results verify that the CDR loop is locked at input data rates from 1.5 Gb/s to 2.5 Gb/s.

1.3 Thesis organization

This thesis is organized into the following chapters:

Chapter 1 is the introduction of the thesis including the motivation, contributions and organization of the thesis.

Chapter 2 overviews the background theory of data communication and structures of different CDRs.

Chapter 3 overviews a PLL-based CDR in modern high-speed serial data transmission. It covers the principle of PLL and the characteristics of CDR with a binary phase detector.

Chapter 4 presents the implementation of the CDR circuit based upon $0.18\mu\text{m}$ CMOS technology provided by the Canadian Microelectronics Cooperation (CMC). It covers the building blocks including the four-stage ring oscillator, the half-rate phase and frequency detector, the comparator and switching circuitry, the charge pump, the loop filter. All the circuits are verified by Spectre based upon schematic and post-layout simulation.

Chapter 5 describes the setup of the chip test environment and discusses the measurement results.

Chapter 6 draws the conclusions of the overall research work and gives some directions for future research.

Overview of CDR and background theory

2.1 Introduction

The architecture of high-speed links with a separate data and clock signal line is shown in Figure 2.1. A receiver must know when to sample the incoming data signals that

Figure 2.1: High-speed link with separate data and clock signal line

it receives from a transmitter in order to accomplish the data transmission successfully. In a data transmission application with the separate data and clock line, the clock signal, which is used to sample the received data stream, is sent from a transmitter to a receiver. The receiver can directly use the clock signal to extract the data information from an incoming data signal when the data rate is low. As the data rate increases, a PLL or a delay-locked loop (DLL) is required to guarantee the precise alignment between the input clock and internal clock signal. For the application of the high-speed links with a separate

clock and data signal, the data and clock lines must be placed carefully to reduce the skew and crosstalk between them. However, it is difficult to match the data and clock signal lines to eliminate the skew between them for a higher data rate system. Moreover, an extra clock signal line is quite expensive and consumes more power.

The combination of the clock and data signals together at the transmitter can eliminate the skew and ensures that the clock and data arrive simultaneously. The architecture of high-speed links with only a data line and a CDR circuit is shown in Figure 2.2. Compared to Figure 2.1, the clock signal line is removed, therefore a CDR circuit is required to extract the clock information from the incoming data stream.

Figure 2.2: High-speed link with data signal line and CDR circuit

This chapter reviews different types of CDRs including linear CDRs, bang-bang CDRs, full-rate CDRs and half-rate CDRs. Some background theory and characteristics of CDRs are also introduced for a better understanding of PLL based CDRs. The characteristics contain phase noise, jitter components, and jitter specifications.

2.2 CDR circuits overview

CDR circuits are widely used in data transmission systems such as optical transceivers, wireless products, and chip-to-chip communications. The CDR technology is very important as a much greater bandwidth is required for high speed data transmission. The

function of CDR circuits is to extract clock information and recover the data from the input serial data signal (NRZ data sequence). The recovered clock can remove the jitter, reduce the distortion, and retime the data signal for future data processing.

Present-day CDR technology mostly uses a PLL structure to synchronize the voltage-controlled oscillator (VCO) clock with the input data. A PLL-based CDR architecture [2], shown in Figure 2.3, is composed of phase detector, charge pump, loop filter, and VCO. The basic idea of the PLL-based CDRs is that, during data transition, the edge of input data and the local VCO clock edge are compared. If the data leads the clock, the clock is sped up. If the data lags the clock, the clock is slowed down. If the edge of the input data and the local clock are precisely aligned, the loop of the CDR is locked and keeps the frequency constant to maintain the locking.

The phase detector (PD) compares the phase between the clock signal generated by the VCO and the input data. The output of the phase detector, which reflects the error information of the clock and the input data, controls a charge pump and the charge pump output is smoothed by a loop filter to force the VCO to follow the frequency of the input data.

Figure 2.3: Basic clock and data recovery architecture

2.3 Linear CDRs and bang-bang CDRs

A phase detector (PD) is one of the most important components in CDR circuits. According to different types of phase detectors, CDR circuits can be categorized into two types of CDRs: linear CDRs which are based upon a linear PD and binary CDRs which are based on a binary PD.

The linear digital PD produces the pulse width which reflects the phase error information between the clock and input data. The output pulse width of linear PDs is linearly proportional to the phase difference between the clock and input data. In contrast, a binary PD produces error information which indicates the relationship between the clock and the input data, and represents whether the clock phase is early or late compared to the input data phase. The characteristics of a linear and binary PD are shown in Figure 2.4 [4]. From PD characteristics, V_{out} is proportional to the phase difference for linear PD when $\Delta\phi$ is between $-\pi$ and π . The binary PD V_{out} , depending on whether clock is early or late compared to the data signal, is either V_1 or $-V_1$ (high or low).

Figure 2.4: Characteristics of (a) linear PD and (b) binary PD

Compared to bang-bang CDRs, linear CDRs have better jitter performance. This is because linear PDs achieve less charge pump activity, produce a smaller ripple on the VCO control line, and hence have better jitter performance [2]. However, linear CDRs

have a smaller frequency locking range and longer acquisition time. In contrast, CDR circuits with binary phase detectors have a wider frequency locking range and shorter acquisition time. PLL-based CDRs with binary (bang-bang) or ternary-quantized phase detectors have become popular since the late 1980's [5]. The jitter of a CDR with binary PDs is high because the output of binary PDs is metastable when the CDR loop is locked.

2.4 Dual loop architecture

In order to get better jitter performance of CDRs, a dual-path loop architecture is commonly employed [3]. As shown in Figure 2.5, the CDR loop is split into two loops: a FLL which is a low frequency path, and a PLL which is a high frequency path. The major benefit of the dual-path loop is that the PLL can suppress the VCO noise and input noise, and FLL can extend the frequency acquisition range of the CDRs.

Figure 2.5: CDR conceptual diagram with dual loops

Upon startup or loss of phase lock, the frequency detector produces a control voltage to drive the frequency of the VCO toward the input data rate. When the frequency error falls within the capture range of the phase locked loop, the phase detector takes over to lock the clock to the input data. In practise, two control lines of the VCO are used. One

is a coarse control for the FLL to enhance the acquisition time and locking range. The other one is a fine control for the PLL to reduce the activity on the VCO control line and lower the output jitter [6]. However, the switching circuitry between the FLL and the PLL should be carefully designed in order to prevent the glitches of the VCO control line during the transition. Large amplitude glitches may change the VCO frequency greatly and the CDR loop may lose lock.

2.5 CDR techniques

CDR architectures can be categorized into three groups according to the VCO frequency: full-rate CDRs, half-rate CDRs and oversampling CDRs. The relationship between the clock and input data for full-rate CDRs and half-rate CDRs is given in Figure 2.6 [7].

Figure 2.6: CDR techniques (a) full-rate clock (b) half-rate clock

2.5.1 Full-rate CDRs

In a full-rate CDR, the edge of the data transition is compared to the rising (or falling) edge of the clock. The relationship between the input data and recovered clock is shown in Figure 2.6 (a). The frequency of the recovered clock is equal to the input data rate for full-rate CDRs. The input data can be retimed by using single-edge triggered flip-flops that operate either on rising or falling edge of the clock.

2.5.2 *Half-rate CDRs*

CDRs can operate at a higher frequency by employing the half-rate technique, which means the clock frequency is half of the data rate. The relationship of the input data stream and recovered clock is shown in Figure 2.6 (b). In half-rate CDRs, the location of the input data transitions is compared to that of both the rising and the falling edges of the recovered clock. The half-rate CDRs require double-edge triggered flip-flops which operate on both the rising and falling edges of the clock.

The advantage of a half-rate architecture is that the clock frequency is only half of the data rate. The reduction of the clock frequency can relieve the VCO design and reduce the power consumption of overall circuits [8].

The half-rate technique is an attractive option as the demand for a higher data rate has grown rapidly in recent years. CDRs with a half-rate technique allow to work at a higher speed while maintaining reliable operation.

2.6 *Characteristics of CDRs*

The performance of CDR circuits affects the proper function of the overall transceivers. The specification of CDRs depends on different applications and may vary greatly in different cases. Some important parameters to consider when designing CDR circuits are acquisition range of recovered clock, acquisition time, phase noise, jitter, power dissipation, and cost. Here only phase noise and jitter are discussed in detail.

2.7 *Phase noise*

In practise, the output of a VCO has undesired phase fluctuations due to intrinsic noise such as thermal noise, shot noise, and flicker noise. Phase noise is widely used to describe the short term random frequency fluctuations of a signal. The VCO phase noise is best described in the frequency domain where the spectral density is characterized by

measuring the noise sidebands on either side of the output signal center frequency. Phase noise power is specified in decibels relative to the carrier (dBc/Hz) at a given frequency offset from the carrier.

The single sideband phase noise (dBc/Hz) is given logarithmically in Equation (2.1) and is depicted in Figure 2.7 (a).

$$S_c(f) = 10 \log \frac{P_{SSB}}{P_C} \quad (2.1)$$

where P_C is the carrier power at the frequency of f_0 and P_{SSB} is the single sideband noise power in unit bandwidth at the frequency ($f_0 + \Delta f$).

Figure 2.7: Single sideband phase noise to carrier ratio

2.8 Jitter

Jitter is one of the most important parameters for CDR circuit design. Jitter, shown in Figure 2.8 [10], can be depicted as the variations of a signal from its ideal position in

Figure 2.8: Jitter in clock signals

time [9], [10]. Period jitter can be measured as the time difference of a signal transition from its ideal position over consecutive clock edges. While cycle-to-cycle jitter can be measured as the time difference between successive periods of a signal [9]. Excess jitter can increase the bit error rate (BER) of a data transmission and degrade the quality of the data communications.

2.8.1 Jitter components

There are two major jitter components: random jitter and deterministic jitter [10].

Random jitter is due to the intrinsic noise of electrical devices and is typically characterized by a Gaussian distribution. Random jitter amplitude is unbounded and the long term reliability of the devices is affected by this jitter. The random jitter comes from random noise sources: thermal vibrations of semiconductor crystal structures, and power supply noise [11].

Deterministic jitter depends on the data pattern and has a non-Gaussian probability density function. It can be predictable and usually bounded in amplitude. Deterministic jit-

ter is related to imperfections in transmission links or may also be caused by power supply noise, cross talk, signal modulation, EMI and simultaneous switching outputs.

2.8.2 Jitter specifications

There are three jitter specifications that define the performance of a transceiver: jitter tolerance, jitter transfer and jitter generation.

Jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied to the input of a CDR circuit without increasing the BER. This is to test the CDR ability to recover data properly when jitter is applied to its input.

Jitter transfer is characterized by the ratio of the output jitter to the input jitter amplitude as a function of frequency. This parameter measures how much the input jitter can be transferred to the output signal through a CDR circuit. It shows the suppression ability of the input jitter amplitude through the CDR circuit. There is a trade-off between external jitter suppression, internal jitter suppression, capture range, and acquisition time. Input jitter can be greatly suppressed if its frequency is higher than the loop bandwidth. Although lower loop bandwidth can strongly suppress the input jitter, the loop can not filter the internal jitter generated by the VCO. The loop bandwidth also affects the circuit capture range and acquisition [8].

Jitter generation is defined as the amount of output jitter that is generated by CDR circuits without jitter applied to the input data. There are a number of sources in a CDR circuit to generate jitter such as VCO, ripple on the control voltage, and power supply noise. Jitter generation is to define the maximum allowable jitter generated by the CDR circuit.

Overview of PLL-based CDR

3.1 Introduction

Using a PLL structure is an attractive choice to accomplish the CDR function. The PLL structure is commonly employed in CDRs to achieve the necessary performance characteristics in terms of jitter suppression, acquisition time, and low phase noise. This chapter introduces the PLL principle and the PLL-based CDR along with some design considerations such as VCO, charge pump, loop filter, and PD.

A basic PLL-based CDR architecture [2] is shown in Figure 3.1. It consists of a VCO, a phase detector, a charge pump, a loop filter and a decision circuit.

Figure 3.1: Basic CDR architecture

3.2 Overview of PLLs

PLL is a frequency feedback system. It is based upon the detection of the phase difference between the input signal and the clock to adjust the phase of the clock and match the phase of the input signal. A basic PLL structure, shown in Figure 3.2, is composed of a phase detector, a charge pump, a loop filter, and a voltage controlled oscillator.

Figure 3.2: Basic structure of PLL

PLLs operate by producing a VCO frequency to match the frequency and phase of an input signal. In the locked condition, any slight change of the input signal first appears as a phase error between the input signal and the VCO clock. The phase detector output, which reflects the phase error, and activates the charge pump, is smoothed by the loop filter, and then forces the phase of the clock toward that of the input signal.

3.2.1 Noise analysis of PLLs

Figure 3.3: PLL linear model with noise sources

A PLL linear model with noise sources is shown in Figure 3.3 [12].

The transfer function of the above PLL can be expressed as follows if all the noise sources are ignored [12]:

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{K_d \frac{K_{VCO}}{s} F(s)}{1 + K_d \frac{K_{VCO}}{s} F(s)} = \frac{K_d K_{VCO} F(s)}{s + K_d K_{VCO} F(s)} \quad (3.1)$$

In order to keep the loop stable, a second order filter (RC network) is usually used to add a pole and a zero to the loop. The expression of the loop filter can be expressed as:

$$F(s) = \frac{1}{C} \cdot \frac{R \cdot C \cdot s + 1}{s} = K_F \cdot \frac{\tau \cdot s + 1}{s} \quad (3.2)$$

The transfer function of PLL with a second order loop can be modified as follows:

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{K_d K_{VCO} K_F (\tau \cdot s + 1)}{s^2 + K_d K_{VCO} K_F \tau \cdot s + K_d K_{VCO} K_F} \quad (3.3)$$

From the transfer function in Equation (3.3), the loop with the second order filter acts as a low pass filter for the input noise.

The transfer functions of other noise sources can be expressed as below:

$$\frac{\phi_o(s)}{V_{n1}(s)} = \frac{\frac{K_{VCO}}{s} F(s)}{1 + K_d \frac{K_{VCO}}{s} F(s)} = \frac{K_{VCO} K_F (\tau \cdot s + 1)}{s^2 + K_d K_{VCO} K_F \tau \cdot s + K_d K_{VCO} K_F} \quad (3.4)$$

$$\frac{\phi_o(s)}{V_{n2}(s)} = \frac{\frac{K_{VCO}}{s}}{1 + K_d \frac{K_{VCO}}{s} F(s)} = \frac{K_{VCO}}{s + K_d K_{VCO} K_F \tau \cdot s + K_d K_{VCO} K_F} \quad (3.5)$$

$$\frac{\phi_o(s)}{\phi_{n3}(s)} = \frac{1}{1 + K_d \frac{K_{VCO}}{s} F(s)} = \frac{s^2}{s^2 + K_d K_{VCO} K_F \tau \cdot s + K_d K_{VCO} K_F} \quad (3.6)$$

The transfer functions of the PD noise, loop filter noise and VCO noise respectively are shown in Equation (3.4), Equation (3.5) and Equation (3.6) [12].

From the above noise analysis equations, the control loop acts as a high pass filter for VCO noise and acts as a low pass filter for input noise. Within the loop bandwidth, the loop suppresses the VCO noise and passes through the input noise. Therefore, the loop bandwidth should be carefully chosen to get optimum noise performance if the input noise is larger than the VCO noise in the high-speed data links. In this case, a narrow bandwidth can be selected to suppress the main noise from the input and get a better jitter performance. However, the narrow bandwidth can reduce the locking range and affect the jitter tolerance performance of the overall loop. To overcome this problem, a dual-loop architecture can be used to suppress the input noise and extend the locking range as well.

3.2.2 Stability analysis of PLLs

As discussed in Section 3.2.1, if all the noise sources are ignored, the closed-loop transfer function of the basic PLL can be expressed as below [13]:

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{K_d \frac{K_{VCO}}{s} F(s)}{1 + K_d \frac{K_{VCO}}{s} F(s)} = \frac{K_d K_{VCO} F(s)}{s + K_d K_{VCO} F(s)} \quad (3.7)$$

Figure 3.4: Simple loop filter

The transfer function of a simple low-pass filter, shown in Figure 3.4, is:

$$F(s) = \frac{1}{1 + \frac{s}{\omega_{LPF}}} \quad (3.8)$$

where $\omega_{LPF} = \frac{1}{R \cdot C}$.

The Equation (3.7) can be rewritten as follows:

$$H(s) = \frac{\phi_o(s)}{\phi_i(s)} = \frac{K_d K_{VCO} F(s)}{s + K_d K_{VCO} F(s)} = \frac{\omega_{LPF} K_d K_{VCO}}{s^2 + \omega_{LPF} s + \omega_{LPF} K_d K_{VCO}} \quad (3.9)$$

According to control theory [14],

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (3.10)$$

where ζ is the damping factor and ω_n is the natural frequency of the system.

Comparing Equation (3.9) and Equation (3.10), the result can be derived

$$\omega_n = \sqrt{\omega_{LPF} K_d K_{VCO}} \quad (3.11)$$

$$\zeta = \frac{1}{2} \sqrt{\frac{\omega_{LPF}}{K_d K_{VCO}}} \quad (3.12)$$

In a second-order system, ζ is usually larger than 0.5 and typically is equal to 0.71 to provide an optimally flat frequency response.

For a frequency step input $\Delta\omega \cdot u(t)$,

$$\Delta\phi_i(t) = \Delta\omega \cdot t \cdot u(t) \quad (3.13)$$

where $u(t)$ is a step function.

For this PLL system, suppose that a frequency step ($\Delta\omega \cdot u(t)$) is applied to the input, then the phase error can be expressed as:

$$\Phi_e(s) = (1 - H(s))\Delta\Phi_i(s) = \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \cdot \frac{\Delta\omega}{s^2} \quad (3.14)$$

The final value of phase error with the frequency step $\Delta\omega \cdot u(t)$ is [13] [14]:

$$\phi_e(t \rightarrow \infty) = \lim_{s \rightarrow 0} s \cdot \Phi_e(s) = \lim_{s \rightarrow 0} s \cdot \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \cdot \frac{\Delta\omega}{s^2} = \frac{2\zeta}{\omega_n} \cdot \Delta\omega = \frac{\Delta\omega}{K_d K_{VCO}} \quad (3.15)$$

From the Equation (3.15), a higher gain ($K_d K_{VCO}$) can reduce the static phase error. But the higher gain means a lower damping factor and degrades the overall loop stability. To overcome the drawback of the PLL with simple loop filter, a loop filter with zero, depicted in Figure 3.5, can be used.

Figure 3.5: Low pass filter with zero

The transfer function of a low pass filter with zero is given by [13] as:

$$F(s) = \frac{R_2 + \frac{1}{C_2 \cdot s}}{R_1 + R_2 + \frac{1}{C_2 \cdot s}} = \frac{R_2 \cdot C_2 \cdot s + 1}{(R_1 + R_2) \cdot C_2 \cdot s + 1} = \frac{\frac{s}{\omega_z} + 1}{\frac{s}{\omega_p} + 1} \quad (3.16)$$

where $\omega_z = \frac{1}{R_2 \cdot C_2}$ and $\omega_p = \frac{1}{(R_1 + R_2) \cdot C_2}$. Therefore, the closed-loop PLL transfer function can be modified as:

$$H(s) = \frac{K_d K_{VCO} F(s)}{s + K_d K_{VCO} F(s)} = \frac{K_d K_{VCO} \frac{\frac{s}{\omega_z} + 1}{\omega_p}}{s + K_d K_{VCO} \frac{\frac{s}{\omega_z} + 1}{\omega_p}} = \frac{\frac{\omega_p K_d K_{VCO}}{\omega_z} s + \omega_p K_d K_{VCO}}{s^2 + \omega_p \left(1 + \frac{K_d K_{VCO}}{\omega_z}\right) s + \omega_p K_d K_{VCO}} \quad (3.17)$$

From the above Equation (3.17), ω_n and ζ can be expressed as follows:

$$\omega_n = \sqrt{\omega_p K_d K_{VCO}} \quad (3.18)$$

$$\zeta = \frac{\omega_p \left(1 + \frac{K_d K_{VCO}}{\omega_z}\right)}{2 \sqrt{\omega_p K_d K_{VCO}}} = \frac{1}{2} \sqrt{\frac{\omega_p}{K_d K_{VCO}}} \left(1 + \frac{K_d K_{VCO}}{\omega_z}\right) \quad (3.19)$$

Increasing the gain ($K_d K_{VCO}$) can decrease the phase error. However, increasing the gain ($K_d K_{VCO}$) also increases the system bandwidth, which may not be desirable for some applications. In addition, this loop filter can not suppress the high frequency noise efficiently. A simple solution to suppress the high frequency noise is to add a small capacitor between Vout and ground. A larger capacitor value may cause loop instability.

3.3 CDR Architecture

CDR circuits include a VCO, phase and frequency detector (PFD), loop filter, and charge pump.

The VCO generates clock signal which is necessary for the PFD and the decision circuits. The phase detector compares the phase of the input data to that of the VCO clock signal, and then generates error information which represents the phase error between the input data and the recovered clock.

The following sections will discuss some building blocks of CDRs including VCO, PFD, and charge pump.

3.3.1 VCO (Ring oscillator)

The VCO plays an important role in CDRs and provides clock information. Basically there are two VCO choices: a voltage-controlled ring oscillator and a voltage-controlled LC oscillator. Although ring oscillators have a higher phase noise than LC oscillators, they are often used in high speed data links for the less stringent requirement of the noise performance. Compared to the LC oscillator, the ring oscillator is a better choice because of its smaller chip area, wider tuning range, lower power consumption, and lower cost. Furthermore, the ring oscillator is easier to integrate.

In this thesis project, a four-stage ring oscillator has been selected. A ring oscillator with an even number of stages is very useful in half-rate CDRs because an even stage oscillator can provide the quadrature clocks which are important in the phase/frequency detector and decision circuits. Moreover, ring oscillators can be implemented by using differential topology which is immune to the common mode noise. The tuning can be split into coarse control and fine control. This dual-loop structure can reduce the output jitter and still has a wide capture range.

Figure 3.6: N-stage differential ring oscillator

A N-stage differential ring oscillator is shown in Figure 3.6. In order to analyze the complex ring oscillator, a general feedback system shown in Figure 3.7 is introduced.

Figure 3.7: General feedback control system

Figure 3.7 shows the input (x), output (y) and error signal (e). Since

$$Y(s) = E(s) \cdot G(s) \quad (3.20)$$

$$X(s) = E(s) - E(s) \cdot G(s) \cdot F(s) \quad (3.21)$$

Then the closed loop transfer function in Figure 3.7 is expressed as below:

$$\frac{Y(s)}{X(s)} = \frac{G(s)}{1 - G(s) \cdot F(s)} = \frac{G(j\omega)}{1 - G(j\omega) \cdot F(j\omega)} \quad (3.22)$$

According to Barkhausen's Criteria for oscillation, the above equation depicts that the loop will maintain oscillation providing $G(j\omega_0) \cdot F(j\omega_0) = 1$. At the frequency ω_0 , the phase shift around the whole loop must be 360 degrees, and the magnitude of the open loop gain must be equal to 1.

Therefore, for N-stage ring oscillators, they also must satisfy Barkhausen's Criteria for oscillation. The open loop gain must be equal to 1 during the normal operation, and the total phase shift must be equal to 360 degrees at the oscillation frequency ω_0 . Assuming that the phase shift of each stage is $\Delta\phi$, then each stage phase shift is $\Delta\phi = \frac{360^\circ}{2N} = \frac{180^\circ}{N}$. According to the above analysis, each stage contributes 45 degrees of frequency-dependent phase shift for 4-stage ring oscillators.

In addition, the oscillator must satisfy the self-start oscillation requirement.

Figure 3.8: Linearized model for a 4-stage ring oscillator

The linearized model for a four-stage ring oscillator is shown in Figure 3.8 [16] and its open loop transfer function is given as

$$H_o(j\omega) = G(j\omega) \cdot F(j\omega) = -\left(\frac{-G_m \cdot R}{1 + j\omega RC}\right)^4 \quad (3.23)$$

In the oscillation system, $H_o(j\omega) = -\left(\frac{-G_m \cdot R}{1 + j\omega_0 RC}\right)^4 = 1$ yielding

$$G_m \cdot R = \sqrt{2} \quad (3.24)$$

$$\omega_0 = \frac{1}{RC} \quad (3.25)$$

Equation (3.24) is the oscillation condition and Equation (3.25) is the oscillation frequency for the four-stage ring oscillator [15].

In order to start the VCO, the open loop gain must be greater than 1 during the start-up period to increase the amplitude. This means that $G_m \cdot R$ should be greater than $\sqrt{2}$ during the startup period. And open loop gain must reduce and equal to 1 during normal operation. This requires a nonlinear device to adjust the VCO gain.

3.3.2 VCO noise analysis

The open loop transfer function can be given by [16]

$$H_o(j\omega) = -\left(\frac{-G_m \cdot R}{1 + j\omega RC}\right)^4 \quad (3.26)$$

Substituting Equation (3.24) and Equation (3.25) to Equation (3.26), the open loop transfer function becomes:

$$H_o(j\omega) = -\left(\frac{-G_m \cdot R}{1 + j\omega RC}\right)^4 = -\frac{2}{\left(1 + j\frac{\omega}{\omega_0}\right)^4} \quad (3.27)$$

$$\frac{dH}{d\omega} = \frac{d\left(\frac{-2}{\left(1 + j\frac{\omega}{\omega_0}\right)^4}\right)}{d\omega} = \frac{-2 \cdot (-4) \left(j\frac{1}{\omega_0}\right)}{\left(1 + j\frac{\omega}{\omega_0}\right)^5} \quad (3.28)$$

$$\left|\frac{dH}{d\omega}\right|^2 \Big|_{\omega=\omega_0} = \frac{64}{\omega_0^2 (\sqrt{2})^5} = \frac{8 \cdot \sqrt{2}}{\omega_0^2} \quad (3.29)$$

Therefore,

$$\left|\frac{N_{out}}{N_{in}}\right|^2 \Big|_{\omega=\omega_0} = \frac{1}{(\Delta\omega)^2 \left|\frac{dH}{d\omega}\right|^2} = \frac{\omega_0^2}{8 \cdot \sqrt{2} \cdot (\Delta\omega)^2} \quad (3.30)$$

The noise in terms of voltage can be expressed as:

$$N_{in} = i_n \left(\frac{R}{1 + j\omega RC}\right) \quad (3.31)$$

$$|N_{in}|^2 = i_n^2 \left(\frac{R^2}{2}\right) \quad (3.32)$$

The noise shaping function [16] for 4-stage ring oscillation is:

$$\left| \frac{N_{out}}{i_n} \right|^2 = \frac{\omega_0^2}{8 \cdot \sqrt{2} \cdot (\Delta\omega)^2} \cdot \frac{R^2}{2} = \frac{R^2 (\omega_0)^2}{16 (\Delta\omega)^2} \quad (3.33)$$

The total additive noise [16] for 4-stage ring oscillator is:

$$8kT \frac{R(1 + \sqrt{2})}{12} \left(\frac{\omega_0}{\Delta\omega} \right)^2 \quad (3.34)$$

It can be seen that R and ω_0 should be reduced for better phase noise.

3.3.3 Binary PD

A PD is used to detect the phase difference between the input data and the recovered clock. The VCO control voltage is determined by the phase error which is detected by the PD. There might not be a data transition at every clock edge since the input data is NRZ data. The CDR loop must keep its previous state when consecutive zeroes or ones appear in the input data. Therefore, the PD does not produce any output signal if there is no data transition, and the control voltage of the VCO should be proportional to the phase error.

There are two common types of PDs: linear PDs and binary PDs. Here only binary (bang-bang) PDs are discussed in detail. As depicted in Chapter 2, bang-bang PDs produce voltage either high or low depending on whether the phase of the clock is early or late compared to the data signal.

Figure 3.9: Alexander phase detector

The Alexander PD [17], shown in Figure 3.9 [8], is a common binary PD. This PD produces three binary samples (A, B and C) of the input data signal.

Figure 3.10 shows the operation of the binary PD for early clock and late clock [8]. If $A = B \neq C$, the clock is early and if $A \neq B = C$, the clock is late. If $A = B = C$, there is no data transition. Therefore, these three samples can be used to detect phase error between the clock and the data. The early signal can be generated by using the XOR gate as $B \oplus C$ and the late signal can be generated by using the XOR gate as $A \oplus B$. The output of the phase error which is the subtraction between the early signal ($B \oplus C$) and the late signal ($A \oplus B$), reflects the information whether the clock is early or late compared to the input data.

Figure 3.10: Operation of binary PD (a) early clock (b) late clock

The above discussed Alexander PD operates in full rate. In a half-rate CDR, the clock frequency is equal to one half of the input data rate and DETFFs are necessary to sample the input data by using both rising and falling edge of the clock signals. The schematic of a half-rate phase detection [1], [8] is shown in Figure 3.11. In-phase clock (Clk_I) and quadrature clock (Clk_Q) are the two clocks to sample the input data. And their outputs are V_I and V_Q respectively. The timing diagram of the half-rate phase detection for early or late clock is shown in Figure 3.12.

Figure 3.11: Schematic of half-rate phase detection

For early clock condition in Figure 3.12 (a), the early clock can be identified that V_I is low during the rising edge of V_Q (0 $\rightarrow$ 1) or V_I is high during the falling edge of V_Q (1 $\rightarrow$ 0). In contrast, for late clock condition in Figure 3.12 (b), the late clock can be identified that V_I is high during the rising edge of V_Q (0 $\rightarrow$ 1) or V_I is low during the fall-

ing edge of V_Q (1 $\rightarrow$ 0). The summary of half-rate detection with early or late clock is depicted in Table 3.1.

Figure 3.12: Half-rate phase detection (a) early clock (b) late clock

TABLE 3.1: Summary of phase detection with early or late clock

V_I	V_Q	Clock and data relationship
high	falling edge	early clock
low	rising edge	early clock
high	rising edge	late clock
low	falling edge	late clock

Therefore, during the falling edge of V_Q , V_I provides the phase information (early clock with V_I =high, and late clock with V_I =low) and during the rising edge of V_Q , the inverse of V_I provides the phase information. According the above analysis, the half-rate PD schematic can be drawn in Figure 3.13 [1].

Figure 3.13: Half-rate PD schematic

Figure 3.14: Half-rate PFD schematic

A three-state half-rate PFD is shown in Figure 3.14 [1]. The input clocks of PD1 are Clk45 and Clk135, and those of PD2 are Clk0 and Clk90. The timing diagram in PFD for slow and fast clocks is shown in Figure 3.15 [1]. If the clock is slower than the input data, VPD1 leads VPD2 and the FD output generates positive pulse. If the clock is faster than the input data, VPD1 lags VPD2 and the FD output generates negative pulse. There is

no positive or negative pulses in the FD output if the clock frequency is equal to the input data rate.

Figure 3.15: Half-rate FD (a) slow clock (b) fast clock

This half-rate FD can produce three-state outputs (positive, negative and zero). The tri-state characteristic of the FD is useful in dual-loop CDR structure and ensures that FLL will not affect CDR after the frequency loop is locked.

Figure 3.16: Half-rate frequency detector state diagram

Figure 3.16 shows the state diagram of the half-rate FD whose implementation is depicted in Figure 3.14. The state2 is assumed initial condition with FD output equal to 0 and the clock frequency is equal to half of the input data rate. V_{FD} is half-rate FD output

which provides three-state outputs (positive, negative, and 0). The half-rate FD state diagram is explained in detail in Table 3.2.

TABLE 3.2: FD state diagram analysis

initial state	condition	V_{FD}	final state
state1	f_{CLK} (increase)	0	state2
state1	f_{Data} (increase)	positive	state1
state2	f_{CLK} (increase)	negative	state3
state2	f_{Data} (increase)	positive	state1
state3	f_{CLK} (increase)	negative	state3
state3	f_{Data} (increase)	0	state2

3.3.4 Charge pump

A three-state PFD and a charge pump are shown in Figure 3.17. The PFD output determines whether the two controlled current sources are connected to the output. They can charge, discharge, or not change the charge of the capacitor which is connected to the VCO control line. When the reference signal leads the clock signal, the capacitor is charged and the VCO is sped up, and when the reference signal lags the clock signal, the capacitor is discharged and the VCO is slowed down. If the reference signal edge and clock signal edge are in alignment, neither of the current sources is connected to the output, and the VCO frequency is kept constant. If the period of the clock is T , the output current is given as:

$$i_d = \frac{I}{2\pi}(\theta_r - \theta_o) = K_{PD}(\theta_r - \theta_o) \quad (3.35)$$

where I is the amount of the current flowing through current sources when the switch is closed.

Figure 3.17: Phase detector and charge pump

Design of CDR building blocks and simulation results

In this chapter, the proposed CDR building blocks and simulation results will be presented. The CDR circuit structure, shown in Figure 4.1, is based on previously published papers about half-rate CDRs [1], [2], [3], [6], [8], [18]. The building blocks include a 4-stage ring oscillator, a half-rate PFD, charge pumps, loop filters, comparators, switching circuitry, and output buffers. This design also comprises a pseudo-random binary sequence (PRBS) generator to generate a pseudo-random binary sequence which is fed to the CDR data input. In order to improve immunity of the common-mode noise, a differential topology is employed for the whole CDR circuit. All the circuit blocks discussed are implemented by using $0.18\mu\text{m}$ CMOS technology. Each of them is individually verified by schematic and post-layout simulation.

The CDR has two control paths: a coarse path (FLL) and a fine path (PLL). The VCO control voltage is also divided into two controls: coarse control and fine control. When the frequency error between the input data and recovered clock is large, FLL adjusts the frequency with a big step by changing the VCO coarse control voltage. If the frequency error is small, FLL does not affect the loop and PLL takes over. PLL adjusts the frequency by a small step. The dynamic performance of the CDR is related to PLL. The two path topology can improve jitter performance and still maintain a wide locking range.

Figure 4.1: CDR circuit structure

4.1 Four-stage ring oscillator

The VCO in this design is a four-stage differential ring oscillator. Compared to LC oscillators, ring oscillators are more easily implemented, have a wider tuning range, require smaller die area and consume lower power [2]. The four-stage ring oscillator, shown in Figure 4.2, provides a multi-phase clock which is necessary in half-rate PFD and recovery circuits.

Figure 4.2: Four-stage differential ring oscillator

The single stage, shown in Figure 4.3, consists of a fast path and a slow path whose outputs are combined [2]. As the power supply voltage is scaled down, the control

voltage swing becomes smaller and maintaining a constant VCO tuning range requires a higher VCO gain. However, the higher VCO gain leads to greater jitter for a given ripple on the VCO control line. In order to reduce the jitter and noise at the VCO output, the VCO control is split into two paths: a coarse control and a fine control. The coarse control is established by a FD and the fine control is established by a PD. When the loop is not locked and the frequency error between the clock and input data is large, the FLL is active and adjusts the VCO frequency close to the input data rate. When the frequency error between the clock and input data is small, the FLL is disabled and the phase locked loop (PLL) takes over.

To extend the tuning range, a Mux is used to select low band or high band. If the high frequency is chosen, input signal (V_{in}) goes through Delay1 cell in the slow path. In contrast, if the low frequency is chosen, the input signal goes through Delay2 cell in the slow path.

Figure 4.3: Implementation of single stage of the ring oscillator

The schematic structure of single stage is shown in Figure 4.4 [2]. The V_{coarse} and the V_{fine} adjust the delay time of each stage by changing the currents which flow in the fast path and the slow path. The control signal (V_{delay}) is used to select a delay time

and get a wider frequency range. Due to limited number of package pins in this design and limited bandwidth of test fixture, the control signal (V_{delay}) is connected to VDD and lower operating frequency of VCO is selected for this design.

Figure 4.4: Transistor level schematic of each stage

According to the noise analysis in Chapter 3, the loop filter time constants, the gain of PD, and that of VCO determine the bandwidth. The noise performance and transient response depends on the bandwidth. The VCO gain is carefully designed to get a good jitter performance of the CDR and still have a wide tuning range. The higher VCO gain can provide a wider tuning range, and reduce the output noise from VCO, but can not suppress the input noise efficiently. The lower VCO gain leads to narrow bandwidth which can not filter the VCO noise at the output and cause a longer settling time or stability problem. Separate coarse control and fine control help mitigate the K_{vco} trade-off. In this design, the current in the coarse path is about ten times that in the fine path. The oscillator gain of the coarse control is approximately 905.3 MHz/V and that of the fine control is about 91.7 MHz/V.

4.2 Half-rate PFD

This section describes the circuit implementation of half-rate PFD [1]. First, the PFD structure based on transistor level will be discussed. The structures of the PD and the FD based on differential topology are shown in Figure 4.5.

Figure 4.5: (a) Phase detector (b) frequency detector

The PD, shown in Figure 4.5 (a), consists of two DETFFs, two DFFs and a MUX. The FD, shown in Figure 4.5 (b), consists of two PDs, two DFFs and a MUX_FD. The basic cells, shown in Figure 4.5, are DFFs, DETFFs, MUXs, and MUX_FDs. The FD can provide a tri-state output (charge, discharge, or remain unchanged). The ternary characteristic of the FD is very important for CDRs with a dual-loop structure because when the frequency loop is locked, FLL should be disabled and not affect the loop any more. The transistor level implementation of the above mentioned cells will be discussed as follows.

4.2.1 D latch structure

The transistor level of D latch based on current mode logic (CML) structure is shown in Figure 4.6. There are two transistor pairs: one is to sample the input data and the other one is to hold the input data. The operation of sample and hold depends on whether the clock signal is high or low. When the clock signal is high, the output signals follow the input signals. This is called sample mode. When the clock signal is low, the hold pairs form a positive feedback to maintain the previous state of the output signal and isolate it from the input data. This is called hold mode. The size of transistors should be carefully optimized for the proper operation. The consideration of designing CML circuits includes voltage swing, current, power dissipation, and speed.

Figure 4.6: D latch (a) schematic (b) symbol

4.2.2 D flip-flop (DFF) structure

The DFF structure, shown in Figure 4.7, is made of two D latches. When the clock signal (CLK) is high, the input data is captured and stored in DLATCH1. When the clock signal (CLK) is low, the stored data in DLATCH1 is transferred to the outputs of DLATCH2, and the outputs will not be affected by the input data until the next clock comes. The CML structure is employed to achieve high speed operation.

Figure 4.7: D flip-flop (a) schematic (b) symbol

4.2.3 Multiplexer (MUX) structure

Figure 4.8 shows the implementation of the MUX and MUX_FD. In Figure 4.8 (a), signals (A and B) are selected by the clock signal (CLKP and CLKN). The output depends on signal A if the clock is high, while the output depends on signal B if the clock is low. MUX_FD, shown in Figure 4.8 (b), is a modified Mux [1] to produce ternary signals of the frequency detector outputs.

Figure 4.8: Schematic of (a) MUX (b) MUX_FD

Figure 4.9 shows differential PFD timing diagram [1] for slow and fast clock. The diagram for slow clock in Figure 4.9 (a) depicts that V_{FDP} is equal to V_{DD} and V_{FDN} produces pulses. In contrast, the diagram for fast clock in Figure 4.9 (b) depicts that V_{FDP} produces pulses and V_{FDN} is equal to V_{DD} . Both V_{FDP} and V_{FDN} are equal to V_{DD} if the clock frequency is half of the input data rate.

Figure 4.9: Half-rate FD with differential outputs (a) slow clock (b) fast clock

Table 4.1 summarizes the relationship between FD outputs (VFDP and VF DN) and the frequency lock condition.

TABLE 4.1: Summary of FD outputs

state	V _{FDP}	V _{FDN}	Condition
state1	VDD	pulse	slow clock
state2	pulse	VDD	fast clock
state3	VDD	VDD	frequency clocked

4.2.4 Double edge triggered flip-flop (DETFF)

Figure 4.10: DETFF structure (a) schematic (b) symbol

The implementation of a half-rate PFD requires DETFFs which are composed of two D-latches and a MUX. The DETFF structure, shown in Figure 4.10, depicts that the clock signals of two DFFs are reversed.

4.3 Comparators and switching circuitry

The PFD outputs are compared with a reference voltage by two comparators whose structure is shown in Figure 4.11. The truth table of comparators is given in Table 4.2.

Figure 4.11: Comparator (a) schematic (b) symbol

Logic equations of the comparators are $OP=INP$ and $ON=\overline{INN}$.

TABLE 4.2: Truth table of comparator signals

INP	INN	OP	ON
0	0	0	1
1	0	1	1
0	1	0	0
1	1	1	0

Figure 4.12: (a) Output of FD (b) $\overline{AB} + \overline{CD}$ logic circuit

The logic equations of FD outputs, shown in Figure 4.12 (a), can be expressed $DN = \overline{FDP}$, $UP = FDN$, $DNB = \overline{FDN}$, and $UPB = FDP$. The outputs in Figure 4.12 (a) are used to control the switching circuitry and the charge pumps in FLL.

The logic equation of the logic circuit, shown in Figure 4.12 (b), is $OUT = \overline{AB} + \overline{CD}$.

Figure 4.13: Schematic of (a) Switching circuitry (b) Transmission gate

Switching circuitry, shown in Figure 4.13 (a), consists of two $\overline{AB+CD}$ logic circuits, labeled (I) and (II), and transmission gates (TG). The TG structure is shown in Figure 4.13 (b). The four inputs of the logic circuits (UP, UPB, DNB, DN) are from the comparator outputs in FLL. And the outputs of TG (VfineP and VfineN) are connected to VCO fine controls. The truth table of two logic circuits in switching circuitry is shown in Table 4.3.

TABLE 4.3: Truth table of logic outputs in switching circuitry

state	A	B	C	D	OUT
state1	UP=0	UPB=1	DNB=1	DN=0	1 (I)
	UP=0	DN=0	DNB=1	UPB=1	0 (II)
state2	UP=1	UPB=0	DNB=0	DN=1	1 (I)
	UP=1	DN=1	DNB=0	UPB=0	0 (II)
state3	UP=1	UPB=1	DNB=0	DN=0	0 (I)
	UP=1	DN=0	DNB=0	UPB=1	1 (II)

The outputs of logic circuit (I) and logic circuit (II) are differential and determine whether TG is on or off. The inputs of TG are connected to reference voltage (Vref). The detailed schematic of switching circuitry is shown in Figure 4.14. When the frequency is not locked (state1 and state2), the signal from FD turns on TG and connects the fine control signals to the common-mode voltage (Vref) to ensure that the VCO fine control voltage (Vfine) falls within the linear frequency region. A large deviation of fine control lines may introduce slewing in the PLL after FLL is locked, potentially causing the frequency

loop unlocked. If the frequency is locked, which is state3 in Table 4.3, TG is open and Vref is disconnected to the VfineP and VfineN, and the PLL takes over.

Figure 4.14: Detailed schematic of switching circuitry

4.4 Charge pump

The charge pump structure is shown in Figure 4.15 and it has differential outputs (OUTP and OUTN). The truth table of the charge pump is given in Table 4.4

Figure 4.15: Charge pump schematic

TABLE 4.4: Truth table of the charge pump

UP	DN	UPB	DNB	OUTP	OUTN
0	0	1	1	charge	discharge
1	1	0	0	discharge	charge
1	0	1	0	high impedance	high impedance

There are two charge pumps in the CDR circuit: One for FLL and the other one for PLL. The charge pump inputs have three states (charge, discharge and high impedance) in FLL and its outputs drive the VCO coarse control lines, but the charge pump inputs only have two states (charge and discharge) in PLL and its outputs drive the VCO fine control lines.

4.5 Loop filter

Second order loop filters are used in the circuit. The differential structure of loop filters is shown in Figure 4.16. Extra capacitors (C_{2c} or C_{2f}) are added to remove high frequency noise. There are two loop filters in the circuit: one, shown in Figure 4.16 (a), is for FLL and the other, shown in Figure 4.16 (b), is for PLL. In order to achieve a lower bandwidth of the FLL, R and C values of the FLL are larger than those of the PLL.

According to CDR applications, the time constant of loop filter usually is several MHz. The parameters of loop filters are carefully selected to get better jitter performance, maintain circuits stability, and achieve fast acquisition time. The time constant is 5 MHz at the beginning and the repeated simulations with different loop filter parameters are required to get the optimized parameters. The final parameters of the loop filter resistors and capacitors are shown in Table 4.5

(a)

(b)

Figure 4.16: (a) Coarse loop filter (b) Fine loop filter**TABLE 4.5: Values of loop filter resistors and capacitors**

R_{1f}	C_{1f}	C_{2f}	R_{1c}	C_{1c}	C_{2c}
10 k Ω	25 pf	1.25 pf	10 k Ω	50 pf	2.5 pf

4.6 Output buffers

In order to drive large external loads (50 Ω cables) at the chip I/O terminals, the output buffers must have strong driving ability. Therefore, large transistors are required. But large transistors without multiple stages are not sufficient to get a minimum delay time. The buffer with a cascade structure [1], shown in Figure 4.17, is necessary to reduce the total delay time. Each stage is larger than the proceeding stage by a factor of 2 [1]. Last

stage resistors with $50\ \Omega$ are used to match the output load. The values of current sources and resistors for each stage are shown in Table 4.6.

Figure 4.17: Output buffers

TABLE 4.6: Resistor and current values of output buffer

stage	stage1	stage2	stage3	stage4
R (Ω)	R1=1.6k	R2=800	R3=400	R4=50
I (mA)	I1=0.5	I2=1	I3=2	I4=4

4.7 PRBS7 generator

A PRBS7 generator [19], shown in Figure 4.18, comprises 7 DFFs and an XOR gate to provide a random sequence of 2^7-1 . The DFF schematic is shown in Figure 4.7 and the XOR gate is shown in Figure 4.19. All cells are based on CML structure.

Figure 4.18: PRBS7 generator

Figure 4.19: CML XOR schematic

4.8 Layout consideration

4.8.1 Transistor layout

In order to reduce the gradient effects across the chip, the common-centroid layout technique [20] is required for some precisely matched circuits such as current sources,

charge pumps, and comparators. The performance of these circuits greatly depends on the matching of the differential paths in the circuits. Therefore, the layout of these circuits should be placed symmetrically by using the common-centroid approach. A large transistor can be split into a number of parallel small transistors to improve the matching of the transistors. This can also improve the performance by reducing the gate resistance with a smaller width for each parallel transistor and by reducing the parasitic capacitances with shared source or drain.

4.8.2 Latch-up protection

Latch-up commonly exists in the CMOS IC design and may lead to malfunction or damage of the circuits. The latch-up circuit acts as a Silicon Controlled-Rectifier (SCR) [20] to short the power supply and ground. And a large short current between the supply and ground causes the circuit malfunction or may damage the circuits in the long run. To avoid the latch-up, adding guard rings between the PMOS and NMOS is an effective approach to reduce the parasitic resistance and prevent forming a positive feedback loop between the power supply and ground. Guard rings can also prevent different cells from interfering with each other.

4.8.3 On-chip decoupling capacitors

The power line might suffer undesirable switching noise and voltage drop which are caused by oscillator, phase detector, and output buffer circuits. This is because of the large switching currents in some blocks such as the buffer circuits and oscillators. The power line noise may induce errors for the comparators and some other logic circuits. In order to reduce the power line noise and improve the reliability of the circuit, decoupling capacitors can be added to filter the noise. However, off-chip decoupling capacitors are not sufficient due to the inductance of the bondwires and that of the connecting trace on the PCB. Therefore on-chip capacitors are necessary to eliminate the high frequency noise. Fortunately, these capacitors can be made by using metal layers in the unused area

without extra cost. They can act as decoupling capacitors which are very useful in the power distribution system.

The capacitors structure [21] are shown in Figure 4.20. Capacitors are created between each metal layer. This structure can make the most use of the metal layers to get a large amount of capacitance.

Figure 4.20: Decoupling capacitor (a) structure (b) symbol

The placement of decoupling capacitors and the blocks in the power distribution system are depicted in Figure 4.21. Each block has a parallel decoupling capacitor which is to reduce the interference between blocks.

Figure 4.21: Decoupling capacitors in power distribution system

4.9 *Simulation results*

This section presents some schematic simulation results with 4Gb/s PRBS input data by using the spectre simulator to simulate the 0.18 μm CMOS technology design. The simulation results include transfer functions of the phase detector and frequency detector, coarse and fine control curves, the eye diagrams of the recovered clock and the retimed data.

4.9.1 *Oscillator gain*

There are two control lines of the ring oscillator: coarse control and fine control. The oscillator gain of the coarse control is approximately 905.3 MHz/V and that of the fine control is about 91.7 MHz/V. The phase noise of the clock is about -88.1 dBc/Hz at 1 MHz offset from a 2.0 GHz. The tuning range of the coarse control is from 1.5 GHz to 2.07 GHz.

4.9.2 *Transfer function of the phase detector and frequency detector*

The transfer functions of the phase detector and the frequency detector are shown in Figure 4.22 (a) and (b) respectively. Their outputs is an average voltage over 100 Baud periods. The waveform in Figure 4.22 (a) shows that the phase detector has dead zone (about 10 ps for 3.125 GHz clock). Beyond the dead zone, the output voltage changes greatly with a slight phase difference between the incoming data and the recovered clock. The waveform in Figure 4.22 (b) shows the characteristics of the frequency detector. The switching point of the frequency detector is 3.125 GHz. The slight frequency error between the input data and recovered clock changes the output voltage polarity. The frequency detector with 40 MHz/V slope depicts its bang-bang characteristic.

(a)

(b)

Figure 4.22: Transfer function (a) phase detector (b) frequency detector

4.9.3 Coarse and fine control curves

Figure 4.23 depicts the control curves for the differential coarse control and fine control lines with 4 Gb/s input data rate. The coarse control lines remain constant after 0.85 μ s. This means the CDR FLL is locked and the FD provides zero signal after that time. And the PLL takes over to adjust the CDR circuit after the frequency is locked.

(a)

(b)

Figure 4.23: Control curves (a) coarse control (b) fine control

4.9.4 Recovered clock and retimed data

The eye diagram of the recovered clock, shown in Figure 4.24 (a), indicates that the ISI peak-to-peak jitter is equal to 16.80 ps.

Figure 4.24: Eye diagram of recovered clock

Figure 4.25: Eye diagram of retimed data

Figure 4.25 depicts the eye diagram of the full-rate retimed data at 4.0 Gb/s. Its peak-to-peak jitter of retimed data is approximately 19.82 ps.

Test setup and measurement results

5.1 Introduction

The half-rate CDR circuit design was fabricated in CMOS 0.18 μ m technology and its package is 24-pin CFP (ceramic flat pack). The test fixture for 24-pin CFP is provided by Canadian Microelectronics Corporation (CMC). This chapter describes the test bench setup and presents measurement results including free-running characteristics of the VCO, two differential coarse and fine control curves for the CDR locking behavior, the spectrum and eye diagram of output signals.

5.2 Test bench setup

The test bench setup of the CDR circuit is shown in Figure 5.1 and the chip structure is shown in Figure 5.2.

A 1.8V DC power supplier is used to provide the DC voltage to the chip. Power lines (VDD and Ground) are not drawn in the test bench setup.

Figure 5.1: Test bench setup

Figure 5.2: Internal structure of the CDR

The RF generator (ROHDE&SCHWARZ) provides a single-ended data signal with a 50 ohms output resistance. BALUN (ZAPDJ-2) is used to produce differential data signals which are necessary for the CDR circuit with differential technology.

Two control signals (Ctrl0 and Ctrl1) control the input data and the output signal due to shortage of the pins for the 24-pin CFP. Ctrl0 selects whether the input of PFD comes from the output of the on-chip PRBS generator (Ctrl0=0), or directly from the off-chip data source (Ctrl0=1). The input of the BALUN is connected to the RF signal genera-

tor. Ctrl1 determines whether the signal output of the chip is the recovered clock (Ctrl1=0) or the recovered data (ctrl1=1). The selection of the input and output signals is summarized in Table 5.1 and Table 5.2.

TABLE 5.1: Selection of input signals

Control signal	Input signal
Ctrl0=0	PRBS generator
Ctrl0=1	Off-chip data

TABLE 5.2: Selection of output signals

Control signal	Output signal
Ctrl1=0	Recovered clock
Ctrl1=1	Recovered data

The current source provides a bias current to the chip. A step signal is used to start up or reset the chip.

Each output signal has two differential terminals: one is positive and the other one is negative. In order to get the spectrum and eye diagram of the output signal, the positive one is connected to the spectrum analyzer (HP8593E Spectrum Analyzer) and the negative one is connected to oscilloscope (Tektronix TDS684B).

5.3 Test fixture and die photograph

Test fixture for 24-pin CFP is shown in Figure 5.3. A clamp is used to fasten the chip to the board with 4 screws. The chip and the clamp must be carefully placed to ensure even pressure on all the terminals of the chip and successful connection between the chip and the printed circuit board. Figure 5.4 shows the die photograph, which occupies an area of $1.28 \times 0.77 \text{ mm}^2$. The bond diagram is shown in Figure 5.5.

Figure 5.3: Test fixture

Figure 5.4: Die photograph

Figure 5.5: Chip bonding

5.4 Measurements results

5.4.1 Free-running VCO characteristics

There are two control lines for the VCO: a coarse control voltage and a fine control voltage. The VCO characteristics for the coarse control voltage and the fine control voltage are shown in Figure 5.6 and Figure 5.7 respectively. The common mode voltage is set to 0.9V during the free-running VCO characteristics test. Compared to the post-layout simulation, the measured VCO frequency is lower due to the resistance of the VCO power lines, or the weakness of VCO core driving ability. The simulations of these effects were conducted but failed to confirm the reason of lower oscillation frequency.

Figure 5.6: VCO frequency versus coarse control voltage

Figure 5.7: VCO frequency versus fine control voltage

5.4.2 Recovered clock and data

When Ctrl0 is equal to 1, the PFD inputs are connected to the off-chip input data source. The recovered clock and data are also sin wave and their frequencies are measured. The measured frequency versus input clock frequency is shown in Figure 5.8.

Figure 5.8: Recovered frequencies vs. input clock frequency

5.4.3 Locking behavior of the CDR circuit

Figure 5.9: Lock acquisition with input data rate at 2.0 Gb/s

Figure 5.9 shows the lock acquisition behavior of the CDR circuit with the input data rate at 2.0 Gb/s. The top two curves represent the fine control signals (V_{fineP} and V_{fineN}) and the bottom two curves represent the coarse control signals ($V_{coarseP}$ and $V_{coarseN}$).

The common mode of the coarse control voltage is not equal to 0.9V. This is because the startup circuit does not charge the coarse control voltage when the initial signal is 0V. During the CDR startup period, the voltage of $V_{coarseN}$ is mostly in discharge mode since the VCO frequency is lower than that of the input data. Therefore, $V_{coarseN}$ is almost equal to 0. Fortunately, differential topology of the VCO is employed in this design. Thus, VCO frequency is related to the differential control voltage.

5.4.4 Eye diagram of the recovered clock and data

Figure 5.10 (a) and (b) show eye diagrams of the recovered data and clock respectively when the input data frequency is 1.6 Gb/s. The single-ended recovered clock frequency is 800.64MHz and its amplitude is approximately 90 mV (peak to peak).

Figure 5.10: Eye diagram at 1.6 Gb/s (a) recovered data (b) recovered clock

Figure 5.11 shows the recovered clock spectrum of the CDR with the input data rate at 1.6 Gb/s. The recovered clock phase noise is about -99.71 dB at 1 MHz offset from the center frequency.

Figure 5.11: Recovered clock spectrum with 1.6 Gb/s input data

Figure 5.12 (a) and (b) show eye diagrams of the recovered data and clock respectively when the input data frequency is 2.0 Gb/s. The single-ended recovered clock frequency is 999.44 MHz and its amplitude is approximately 85.6 mV (peak to peak). The peak-to-peak clock jitter at 2.0 Gb/s is 60 ps (0.06 UI).

Figure 5.12: Eye diagram at 2.0 Gb/s (a) recovered data (b) recovered clock

Figure 5.13 shows the recovered clock spectrum of the CDR with the input data rate at 2.0 Gb/s. The recovered clock phase noise is about -93.47 dB at 1 MHz offset from the center frequency.

Figure 5.13: Recovered clock spectrum with 2.0 Gb/s input data

The measured CDR performance is summarized in Table 5.3.

TABLE 5.3: CDR characteristics summary

parameter	experimental
Supply Voltage	1.8 V
PRBS	2^7-1
Input data rate range	1.5-2.5 Gb/s
VCO frequency range	0.75-1.25 GHz
Phase noise (recovered clock) @ 1 MHz offset	-93.47 dBc/Hz @ 2.0 Gb/s
Output jitter (peak to peak) @ 2.0 Gb/s	0.06 UI
Power dissipation (CDR core)	40 mW

Conclusions and future work

6.1 Conclusions

CDR circuits are widely used in optical receivers, chip to chip interconnects, and wireless communications. With the demand for speed and bandwidth in high-speed data transmission growing rapidly, the challenge of the CDR circuits design increases. More efficient technologies need to be employed to improve the existing circuit performance.

In Chapter 2 and Chapter 3, the background of CDR circuits and the theory of the PLL principle were discussed. Three characteristics of CDR circuits were explained: phase noise, tuning range, and jitter performance. The performance and structure of two CDR circuits (Linear CDR and Bang-bang CDR) were compared. The basic components of CDR circuits including VCO, PFD, the charge pump and loop filter were also discussed in detail.

The main contributions of this design were presented in Chapter 4 and Chapter 5. In Chapter 4, a novel switching circuitry was used to realize the smooth transition between FLL and PLL to avoid potential loss of loop lock, and a variable time constant loop filter was introduced to support the CDR acquisition. The complete CDR circuit that achieves both frequency and phase acquisition was designed. The CDR chip was fabricated with 0.18 μm CMOS technology. In Chapter 5, the setup of the chip test environment was

described and experiment results were shown. The CDR circuit implementation was verified through the measurement results.

6.2 Future Work

The lack of pins made the test and analysis of the CDR circuit inconvenient. In a future design, a package with adequate pins could be chosen, or some probe pins could be used to test and analyze the circuits. Also, a common mode feedback circuit would be necessary in order to ensure the common mode voltage of the VCO control lines. Furthermore, loop filters can be fabricated on the chip if there is enough space and this can improve the loop performance and save several pins which are connected to the off-chip loop filters. In addition, an LC oscillator would be an attractive option to improve the jitter performance of the system. CDR jitter tolerance was unable to be tested due to lack of equipment. Further loop optimization could be performed using behavioral simulation.

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Appendix A: Schematics of the CDR

Appendix A.1: Schematic of the CDR

Appendix A.2: Schematic of the VCO

Appendix A.3: VCO schematic of each stage

Appendix A.5: Schematic of the PD

Appendix A.6: Schematic of the charge pump

Appendix A.7: Schematic of the transmission gate

Appendix B: Layout of the CDR

Appendix B.1: Die diagram of the CDR

$$0.32 \times 0.364 \text{ mm}^2$$

Appendix B.2: Layout of the VCO

$$0.43 \times 0.47 \text{ mm}^2$$

Appendix B.3: Layout of the PFD

$$0.15 \times 0.148 \text{mm}^2$$

Appendix B.4: Layout of the logic circuits and charge pumps

$$0.238 \times 0.062 \text{ mm}^2$$

Appendix B.5: Layout of the PRBS generator