An Ultra-Compact and Reconfigurable X-band GaN-based Control MMIC for 5G Phased Array Transceivers

By

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Abstract

Most of published phased arrays are designed for aerospace and military applications. Since phased arrays has become one of the new technologies for 5G, new designs of phased array need to be carried out for 5G applications. A phased array Transmit/Receive Module (TRM) for 5G was proposed by our research group. This TRM comprises of a control MMIC and a front-end module. This thesis proposes an ultra-compact and reconfigurable X-band control MMIC, consisting of a SPDT switch, a 5-bit digital phase shifter and a 5-bit digital attenuator, for 5G phased array transceivers based on the 0.15-μm GaN HEMT process. To ensure this work is fabrication-driven design, characterization of the fabricated GaN HEMTs, in which it shows the agreements between the design kit model and measurement results, is illustrated first. Layout dimensions indicate the proposed control MMIC occupies an area size of 2 mm × 4 mm including RF and DC pads.

Acknowledgements

I would like to take the chance to express my sincere gratitude and appreciation for several individuals. Without them, I will not have the opportunity to devote to my research interest and persist to achieve my goals.

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I would like to express my deep gratitude and admire to my parents, Liang Jing and Runmin Zhuge, for their continuous encouragement and endless support. Without them, I would never have become the person who fights for his dream and persists to pursue what he believes in no matters what he would have been through.

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List of Abbreviations

1G	The First Generation
2DEG	Two-Dimensional Electron Gas
2G	The Second Generation
4G	The Fourth Generation
5G	The Fifth Generation
AESA	Active Electronically Scanned Array
BDGA	Bi-Directional Gain Amplifier
CMOS	Complementary Metal-Oxide-Semiconductor
DUT	Device-Under-Test
EM	Electromagnetic
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GSG	Ground-Signal-Ground
HBT	Heterojunction Bipolar Transistor
HEMT	High-Electron-Mobility Transistor
IF	Intermediate Frequency
IIP3	The Input-Referred IP3
IoT	Internet of Things
IP	Internet Protocol
IP3	Third-Order Intercept Point

LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
MESFET	Metal–Semiconductor Field-Effect Transistor
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
NRC	National Research Council
OIP3	Output-Referred IP3
P_{1dB}	1-dB Compression Point
PESA	Passive Electronically Scanned Array
pHEMT	Pseudomorphic High-Electron-Mobility Transistor
RF	Radio Frequency
RMS	Root-Mean-Square
Rx	Receiver
SiC	Silicon Carbide
SiGe	Silicon-Germanium
SiP	System-In-Package
S-parameters	Scattering Parameters
SPDT	Single-Pole-Double-Throw
SPST	Single-Pole Single-Throw
TOI	Third-Order Intermodulation
TRM	Transmit/Receive Module
Tx	Transmitter

VGA	Variable Gain Amplifier
VNA	Vector Network Analyzer
VSWR	Voltage Standing Wave Ratio

Chapter 1 Introduction

The Monolithic Microwave Integrated Circuit (MMIC) is a technology which implements both passive and active devices on one single chip[1]. The MMICs operates at a frequency range of 1 GHz to 300 GHz. Highly-integrated and ultra-compact ICs can be realized by using MMIC technology. For Gallium Nitride (GaN)-based MMICs, high power handling capability and high maximum oscillation frequency of this wide-bandgap III-V semiconductor make it a perfect candidate for military and aerospace applications [2]. The adaptive phased array radars, so called active phased array radar or Active Electronically Scanned Array (AESA) radars, have been a key component in modern airborne or space-based communication systems for years. As 5G approaches, phased arrays have become one of the new technologies for the 5G network. There is a Transmit/Receive Module (TRM) in each unit cell of a phased array. Each of these individual TRMs is capable of frequency conversion, phase-shifting and power amplification. The control MMICs (phase shifter, attenuator and switch) in TRMs are significantly important due to the nature of adaptive phased arrays. In this work, an ultra-compact and highly-linear X-band control MMIC is presented.

1.1 Motivation

Thanks to technology advances in mobile communication and the emergence of Internet of Things (IoT), the number of smart devices is unprecedentedly increasing worldwide. Research shows that commercial market is anticipating a new explosion. Juniper Research is forecasting that the number of IoT devices, sensors and actuators will reach over 46 billion in 2021 [3]. With reference to Figure 1-1, Cisco predicts 10 billion new

connected devices will appear in global IP network by 2020, leading to a total amount of 26.3 billion devices [4]. Ericsson has reported in Figure 1-2 that the total number of IoT connected devices will increase up to 28 billion by 2021 [5]. All these forecasts and trends indicate the data traffic for commercial wireless communications is becoming incredibly crowded. This data traffic will certainly reach the bandwidth limit some day in despite of channel capacity improvement techniques. In addition, most of existing cellular communications including 1G, 2G, WCDMA and 4G are occupying the frequency range below 6 GHz. Thus, 5G has no choice but to unlock higher frequency ranges which allows higher speed and channel capacity. Frequency spectrum above 6 GHz traditionally used by military and government users for years due to its natural properties is becoming an actual solution to the issue. Although this frequency range is currently used in airborne, maritime and satellite applications, more and more researchers are starting to focus on devices for IoT applications and mobile communication systems at frequencies above 6 GHz [6] [7]. Although specific spectrum for 5G wireless has yet to be determined, the relevant spectrum can range from 1 GHz to beyond 100 GHz [5]. In most of current IoT systems and proposed 5G mobile communication systems, compact phased array applications like adaptive arrays and smart antennas are key components for data transmission [8]. Phased array has been mostly used as radar for military and government applications in the past decades due to size, cost, performance, etc. Nonetheless, technology advances in wide-bandgap semiconductor is leading them closer to consumer markets where cost and size concerns the most. So far, there are two main types of phased arrays: Passive Electronically Scanned Array (PESA) and Active Electronically Scanned Array (AESA) [9].

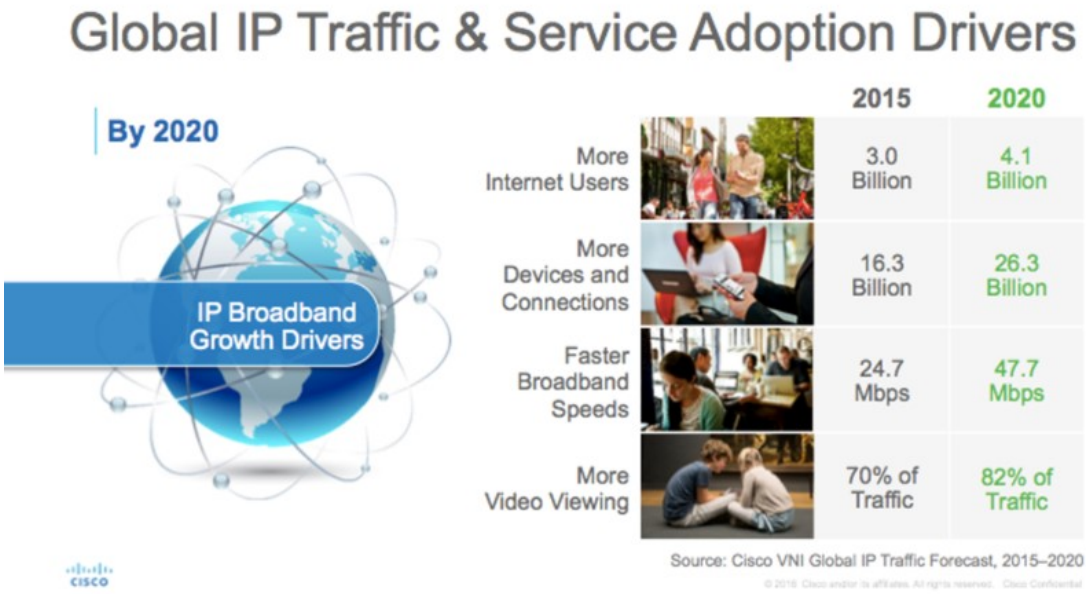

Figure 1-1: IP broadband growth prediction [4]

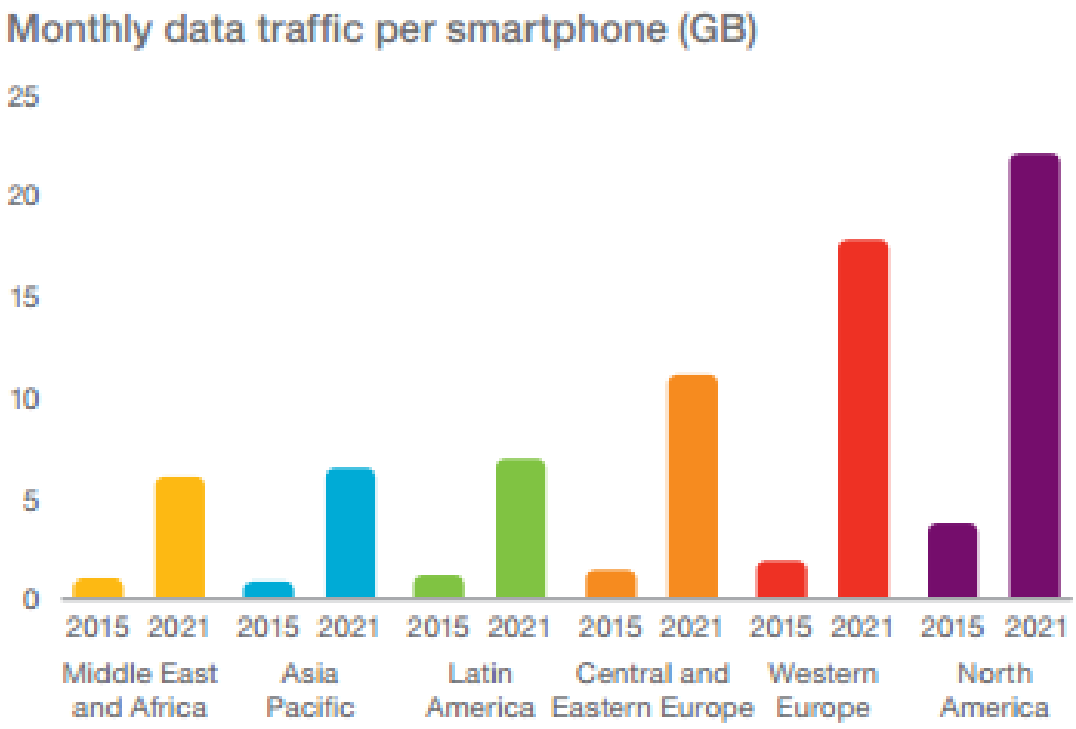

Figure 1-2: Monthly data traffic prediction [5]

The major difference between PESA and AESA is the method of obtaining high-power RF signal for transmission. There is only one single bulky high-power amplifier in PESA

while each of AESA elements is capable of power amplification. Therefore, AESA has several incomparable advantages such as reliability, size, cost, etc. For instance, AESA can still be functioning even if some elements malfunction. On the other hand, PESA will be totally unusable if the power amplifier stops working. Therefore, AESA is more attractive for future applications.

In many current wireless communication systems, linearity of devices significantly limits performance and the range of their applications. Since explosively higher data streams are expected in the future, it is necessary and important to have devices with high linearity in the system to ensure signal integrity during transmission. Furthermore, small sizes and lower weight will facilitate lower cost and ease of deployment. First generation AESAs usually included a chipset for unit-TRMs consisting of five individual chips due to state-of-the-art semiconductor technology. The bulky size of AESAs could only be tolerated in the past for military and government applications where performance outweighs cost and size. We cannot expect consumer market to benefit from the first generation AESAs due to the need for low cost, low weight and mobile solutions. Breakthroughs in semiconductor technology reopen the possibility of AESA applications [10]. Phased array MMICs are drawing industrial and research attention and becoming a hot topic in the field.

1.2 Thesis Contribution

This work contributes to the design and implementation of an active X-band Control MMIC module based on a 0.15-μm GaN process that includes: a SPDT switch, a 5-bit digital phase shifter and a 5-bit digital attenuator to interface directly with a previously

fabricated GaN Front-End Module (FEM) [11]. As reported, the following contributions have been achieved.

- A validation of the 0.15-µm GaN process under dc, small- and large-signal conditions has been made through measurement and modeling.
- The measured extracted models were carefully verified against existing models in the 0.15-µm GaN process and used as the basis for the microwave circuit or the control MMIC designs in this thesis.
- A compact high-linearity SPDT switch has been designed and Electromagnetic (EM) co-simulated based on the measured extracted models.
- To the best of our knowledge, the first GaN-based 5-bit digital phase shifter and 5-bit digital attenuator have been designed and EM co-simulated with the assistance of the extracted models.

1.3 Organization

This thesis is organized as follows.

Chapter 2 describes necessary background for the research presented here. General RF background including performance parameter properties and reviews of MMIC technology and GaN process are presented. Various topologies of state-of-the-art phase shifter, attenuator and SPDT switches are described and discussed.

Chapter 3 presents the measurements on common-gate structure, and common-source GaN FETs. Discrepancies and distortions will be discussed and compared to available models in the Process Design Kit (PDK).

Chapter 4, 5 and 6 discuss the design of the SPDT switch, phase shifter and attenuator design, respectively. The key design parameters and concerning issues are discussed and

a comparison to state-of-the art implementations is presented. Both schematic- and layout-level designs will be reported. Schematic and EM simulation results will be presented and discussed.

Chapter 7 concludes this work and describes improvements needed in the future work.

Chapter 2 Background

This chapter gives a brief overview on radio frequency (RF) transceiver architecture, phased array architecture, control MMICs, GaN technology. Literature reviews on phased array systems, control MMICs are reported for last few years. Definitions of related performance parameters are also introduced afterwards.

2.1 Radio Fundamentals

All the radio theories and techniques we have used for decades to design modern electronic wireless communication systems start from the famous experiment conducted by Heinrich Hertz in 1885. The German physicist was the first one to prove that the transmission of electric waves can be wireless [12]. Ever since then, radio technology began to evolve explosively. Eight years later, Nikola Tesla successfully achieved the wireless transmission of electromagnetic energy in 1893. In 1901, the first transatlantic signal was sent by Guglielmo Marconi, an Italian businessman and electrical engineer, from Ireland to Canada. Lee Deforest, a direct competitor to Marconi at the time, made a triode vacuum tube allowed for amplification of radio signals in 1906. Almost a decade later, Edwin Armstrong patented the Super Heterodyne Receiver which is widely used in modern transceivers. After decades of technology development, the first cellular system using digital CDMA technology was commercially launched by QUALCOMM [12]. It is a milestone for modern radio technology. To satisfy technical specifications for various applications, several RF system architectures have been developed. Superheterodyne and direct conversion transceivers are two main types of modern transceiver architecture. A

typical half-duplex superheterodyne radio transceiver is shown in Figure 2-1. A half-duplex transceiver works alternatively between transmitting and receiving signal while signal can be transmitted and received at the same time in a full-duplex tranceiver [13].

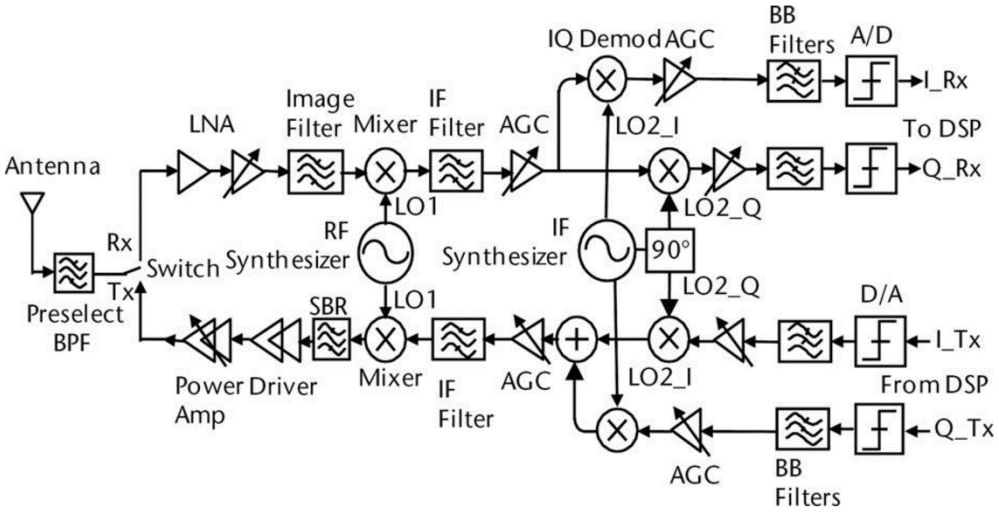

Figure 2-1: A typical half-duplex superheterodyne transceiver [13]

In superheterodyne transceivers, there are two stages of frequency conversions in both transmitter path and receiver path. Signals are first converted to Intermediate Frequency (IF) and will be further converted to baseband. For direct conversion transceivers, there is no IF stage and signals will be directly converted to baseband. Direct conversion transceivers require lower supplied power and less area size than superheterodyne transceivers since only one frequency synthesizer is needed and some filters such as image filter can be eliminated. However, missing IF stage causes issues like local oscillator (LO) spurs coupling to the RF path. Other than superheterodyne and direct conversion transceivers, there are also other types of RF system architecture: low-IF transceiver, sliding-IF transceiver, etc.

2.2 Phased Arrays & TRM

Concepts of electronic beam steering can be found in a British patent [14] as early as 1899. Later, large electronically scanned arrays for missile and space applications were carried out by MIT Lincoln Labs [9]. During the 1980s, the advent of AESAs led phased array technology to a new stage because of technology advances in GaAs MMICs. The principal of designing phased arrays is to steer the transmitted or received signals. There are two main types of phased arrays: PESA and AESA [9]. The major difference between PESA and AESA is the method of obtaining high-power RF signal for transmission.

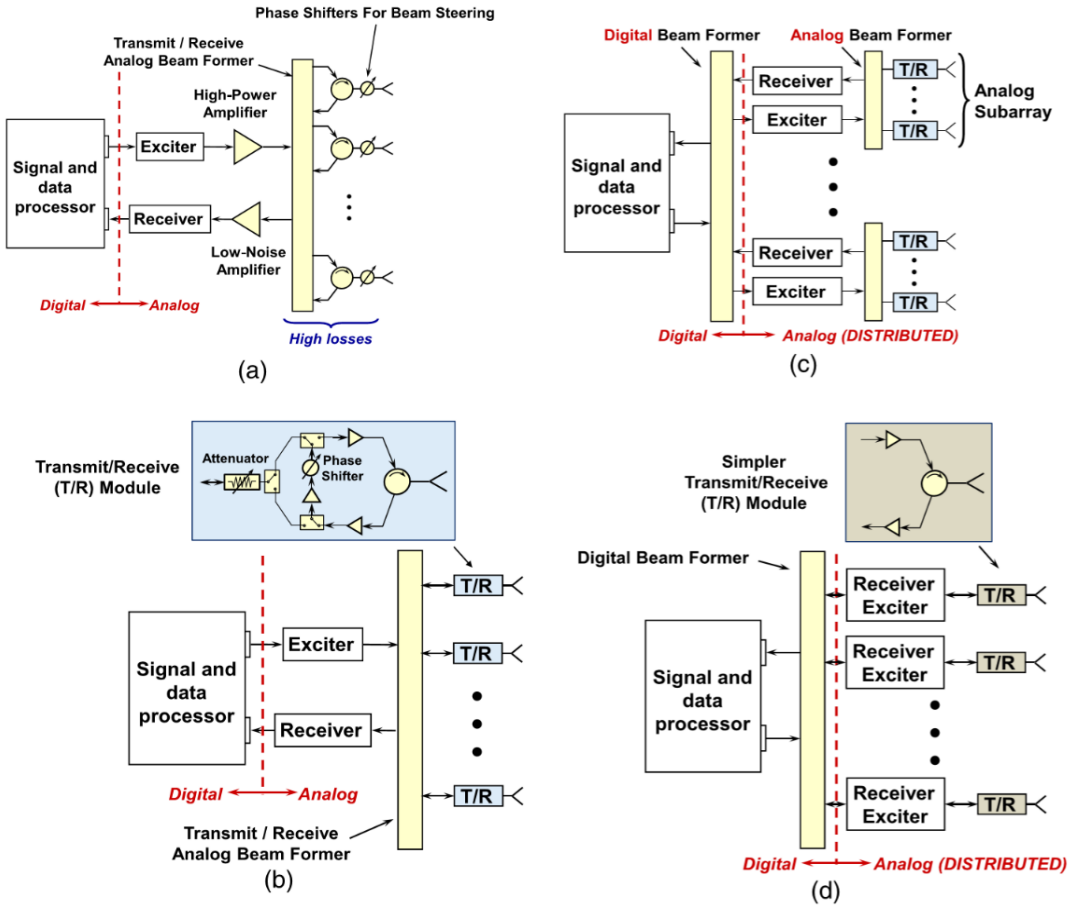

Figure 2-2: Phase array systems: (a) analog passive phased arrays (b) analog active phased arrays (c) subarray-level digital arrays (d) element-level digital arrays [15]

In PESAs, all the elements share RF power for signal transmissions from one high power amplifier. In contrast, each element in AESAs can be fully functioning as usual RF

TRMs. Thus, one chief advantage that AESAs have over PESAs is reliability. AESAs can maintain minimal performance until the limit number of failed elements is reached while the functioning of PESAs relies on every element since failure of one single element destroys the performance [9].

As research advances on phased array technology, element-level digital arrays appear. Element-level digital arrays significantly simplify the design of massive RF TRMs, however, also increases the complexity of circuits and brings challenges on signal processing and data management [16]. Figure 2-2 shows four main phased array radar architectures in the past few years [15]. Here, only analog active phased arrays and subarray-level digital arrays will be discussed. Both analog active and subarray-level digital phased arrays have the same TRM including control MMICs while the other two do not have so. In [17], a 60-GHz four-element phased-array TRM System-in-Package (SiP) was designed using 65-nm flip-chip CMOS process. The system includes 4-bit RF switched LC phase shifters, phase compensated variable gain amplifier (VGA), 4:1 Wilkinson power combining/dividing network, variable-gain low-noise amplifier, power amplifier, 6-bit unary digital-to-analog converter, bias circuit, electrostatic discharge protection, and digital control interface. The system including Tx/Rx phased arrays were packaged with four antennas in low-temperature co-fired ceramic modules. The four-element Tx array has an output P_{1dB} of 5 dBm per channel while the four-element Rx array gives an average gain of 25 dB per channel. The Tx part occupies an area of 3.74 mm^2 while the Rx part has an area of 4.18 mm^2. Phase error introduced by gain imbalance of the switched LC phase shifter has been minimized by using the proposed phase-compensated VGA. The authors have claimed the proposed phased array is the

first V-band phased-array Tx/Rx SiP antenna modules with phase compensated VGA techniques. Rather than going further into phased arrays design, research on transceiver design for X-band phased array is more of interest here. A fully integrated transceiver for X-band phased-array systems was designed based on 0.18-μm CMOS technology. Each of Tx/Rx paths has a 6-bit phase shifter, a 6-bit attenuator and two input and output amplifiers [18]. A new transceiver core chip, shown in Figure 2-3 (a), and a new circuit of 5.625° phase shift block were proposed. It is claimed that the Root-Mean-Square (RMS) phase and amplitude errors of the overall chip are better than 2° and 0.25 dB, respectively. The output P_{1dB} is higher than 10 dBm over X-band. The transceiver core chip occupies an area size of 4.4 × 2.9 mm^2. More recently, a design of an X-band phased-array transceiver core chip using 0.13 μm SiGe BiCMOS technology was reported in 2016 [19]. The transceiver chip is designed based on all-RF phased-array architecture. Figure 2-3 (b) shows its block diagram, in which LCAs stands for low compensation amplifiers. The system consists of low-noise amplifier, power amplifier and the common leg 5-bit phase shifter with loss compensation amplifiers. The receiver shows an output P_{1dB} of 6 dBm, an RMS phase error less than 3.8° and an RMS amplitude error less than 1.2 dB at 9-11 GHz in the RX mode while the transmitter demonstrates a P_{1dB} of 28 dBm, an RMS phase error less than 3° and an RMS amplitude error less than 0.6 dB at 9-11 GHz. The whole transceiver has an area size of 5.2 × 3 mm^2. Besides, other designs of X-band T/R chipset for phased array based on various technologies can be found in [20] [21].

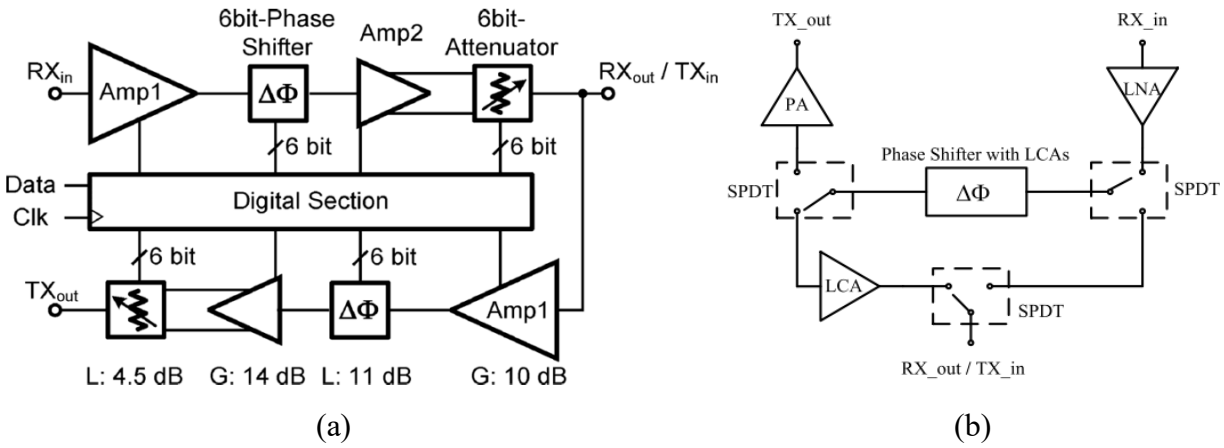

Figure 2-3: Transceiver architectures in literature: (a) proposed transceiver architecture [18] (b) proposed X-band transceiver architecture [19]

2.3 Control MMICs

Control components play a vital role in modern RF and microwave systems, especially in phased array radar system. Control component ICs have been developed using various semiconductor technologies including but not limiting to PIN diodes, GaAs MESFET, GaN HEMT, SiGe HBT and Si CMOS technology. Control components will be discussed here includes switches, phase shifters and attenuators. Switches are used to control the signal flow in the system while phase shifters and attenuators manipulates the phase and amplitude of the transmitted signal, respectively. For example, hundreds of control circuits are implemented in an AESA system for accurate control of the radiated beams. In the very early years, solid-state PIN diodes and ferrites were used to design control components [2]. During 1980s, researchers started to develop low-cost GaAs MESFET control MMICs for X-band and higher frequency bands. Figure 2-4 shows a brief timeline developments of control component circuits from 1980 to the present [2]. As we can see from the timeline, X-band has always been the frequency band of interest

although more and more control components are being explored in high frequency up to 60 GHz.

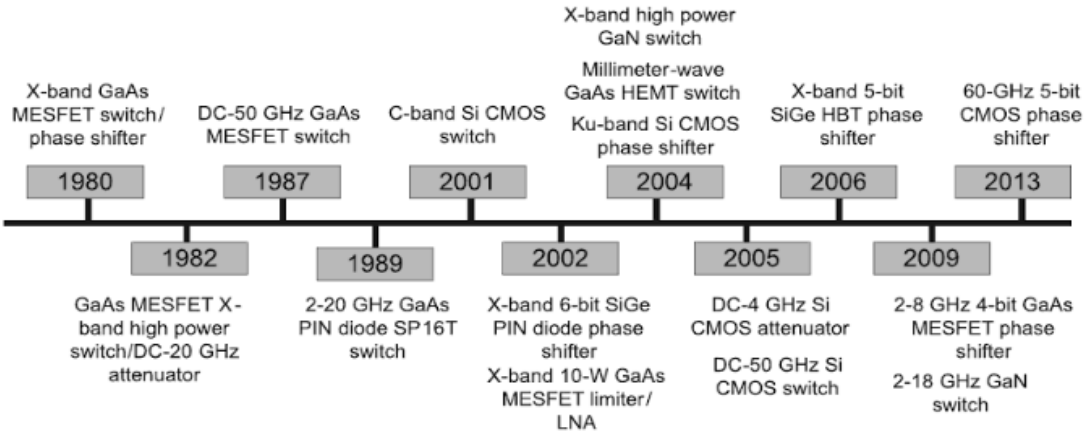

Figure 2-4: Timeline developments of monolithic control components from 1980 to the present [2]

To design the control circuits, there are two options in terms of architecture: the "Separate" and "Common Leg" architectures as shown in Figure 2-5. In the "Separate" architecture, all the required gain is realized in the separate Tx or Rx path. This implementation requires the phase shifter and attenuator to be bi-directional or reciprocal. The "Common Leg" implementation integrates phase shifter and attenuator with buffer amplifiers which reduce the design complexity of phase shifter and attenuator. Both architectures have been widely used for different applications since there is a trade-off between performance parameters. Three main performance parameters to be considered are amplitude/phase errors, noise figure and third-order intercept point (IP3). Advantages and disadvantages of both architecture candidates and reasons for those were listed in [22]. In short, the "Common Leg" architecture has slightly better amplitude/phase errors, IP3 and Voltage Standing Wave Ratio (VSWR) than the "Separate" architecture while the latter has much better noise figure performance than the former one.

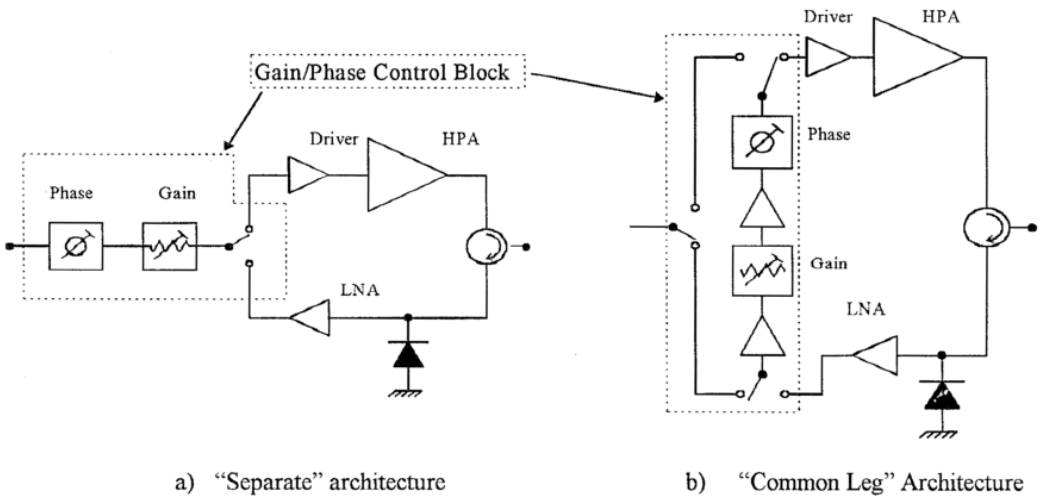

Figure 2-5: Alternative TRM control circuit architecture [22]

In the first decade of 21st century, X-band control component MMICs were carried out [23] [24] [25]. More recently, several designs of control MMICs have also been published. Andrea Bentini et al. designed a X-band core-chip including a 6-bit attenuator, a 6-bit phase shifter, a Tx/Rx switch, a digital serial-to-parallel converter and two gain amplifiers on both Tx and Rx paths in 2012 [26]. The "Separate" architecture was selected due to low complexity and smaller required area. The MMIC were fabricated in 0.18 μm OMMIC GaAs pHEMT process and the operating frequency is 9-10.2 GHz. The average insertion gain for Tx and Rx mode are 6 dB and 8 dB respectively. The core chip occupies an area size of 4.0 × 3.7 mm^2. Another X-band T/R control chipset using CMOS technology was published one year later in 2013 [27]. This T/R chipset, which is based on the "Separate" architecture, constitutes of a bi-directional gain amplifier (BDGA), a 5-bit digital step attenuator with two BDGAs and a 6-bit phase shifter. The chipset results in a 360^o coverage with the Least Significant Bit (LSB) of 5.625^o for phase variation and a 31-dB coverage with the LSB of 1dB for attenuation. The reference state gain is higher than 3.5 dB and the return losses are better than 11dB at 8.5-10.5 GHz. The chipset

results in a 4.3° RMS phase error and a 0.8 dB RMS amplitude error for phase shift accuracy at 8.5-10.5 GHz. Meanwhile, the attenuation accuracy with a 0.33 dB RMS amplitude error and a 7.4° RMS phase error is claimed. The output 1-dB Compression Point (P_{1dB}) of the chipset is higher than 6.5 dBm. The overall chip size is 2.06 × 0.58 mm^2 including pads. The authors reported the design as a smallest X-band CMOS Tx/Rx chipset consuming lowest power to-date. In 2014, Andrea Bentini et al. designed a 6-18 GHz multifunctional chip for Tx/Rx modules based on OMMIC 0.18 μm Enhanced/Depletion GaAs MMIC technology [28]. This chip integrates multiple functioning blocks including low noise/medium power amplifiers, gain amplifiers, SPDT switches, digital/analog attenuators and stepped phase shifter. The "Common Leg" architecture was selected over the "Separate" architecture due to its superior performance. Two gain amplifiers, a stepped phase shifter and the analog attenuator were placed in the common leg shared by both paths. For the overall chip, a Tx output P_{1dB} of 17 dBm and a Rx input P_{1dB} of -13 dBm are achieved. The chip results in a maximum RMS phase error of 13° and a RMS amplitude error of 1.3 dB for phase settings. The chip also gives a RMS amplitude error of 0.8 dB and a RMS phase error of 6° for attenuation settings. The final area size of the chip is 6 × 4.3 mm^2.

2.4 The proposed architecture

The control MMIC is a subsystem of a previously proposed T/R module for X-band phased array. Figure 2-6 (a) shows the architecture of the proposed T/R module for X-band phased array. Although only five elements are shown in the figure, phased array designers can implement as many as needed for a specific application. Each of these T/R modules consists of an attenuator, a phase shifter, two SPDT switches for control of

signal path, a low noise amplifier for Rx mode and a power amplifier for Tx mode. These T/R modules will then be connected to beam-forming networks and antennas for radiation.

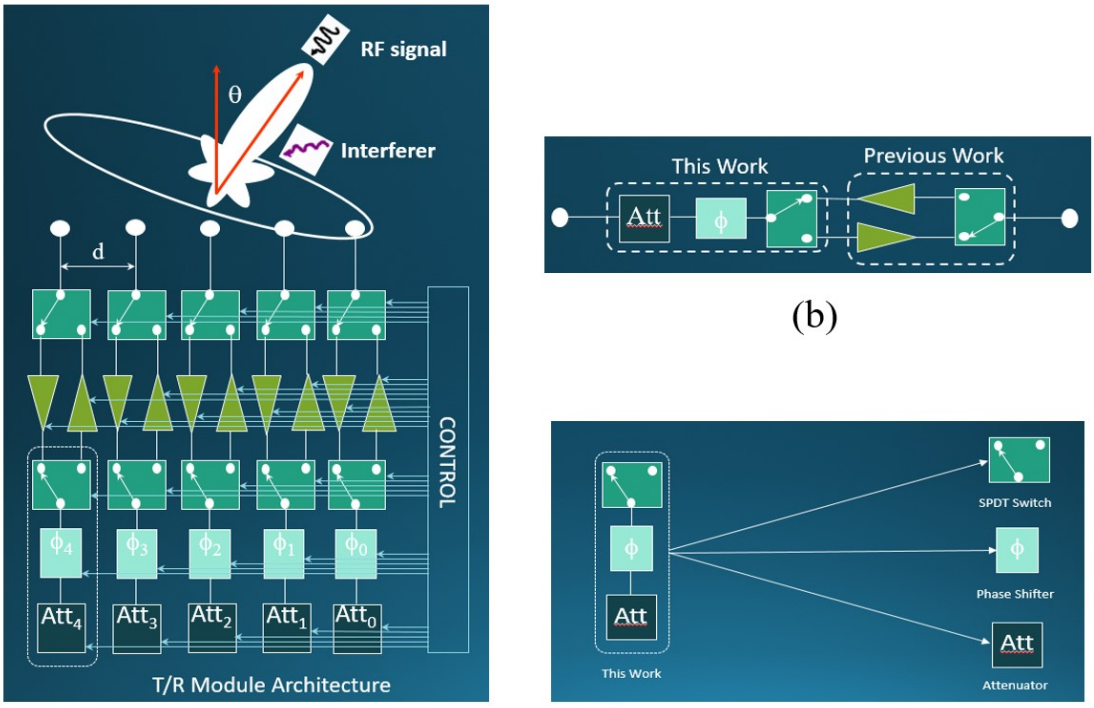

Figure 2-6: Proposed phased array system: (a) Proposed TRM architecture

(b) Two subsystems in T/R module (c) This work architecture

In Tx mode, the attenuator and phase shifter adjust amplitude and phase of the signal to be transmitted in a particular direction. In Rx mode, the adjustments of amplitude and phase of signals allows the phased array to receive the desired signal from specific direction and block signal interferences. Usually, some gain amplifiers are placed along the signal path for phase and gain compensations. In our case, these gain amplifiers are excluded for compact size. As presented in Figure 2-6 (b), the proposed T/R module constitutes of a control MMIC and a front-end module. The control MMIC includes a 5-bit attenuator, a 5-bit phase shifter and a SPDT switch. The front-end module contains a

low-noise amplifier, a power amplifier and a SPDT switch. The front-end module was designed and fabricated using National Research Council (NRC) 0.15-µm GaN HEMT technology [11]. Figure 2-6 (c) shows the control MMIC proposed in this work. The "Separate" control circuit architecture rather than the "Common Leg" one was selected because of smaller required area and less design complexity. The details of design considerations will be presented in following chapters.

2.5 Process

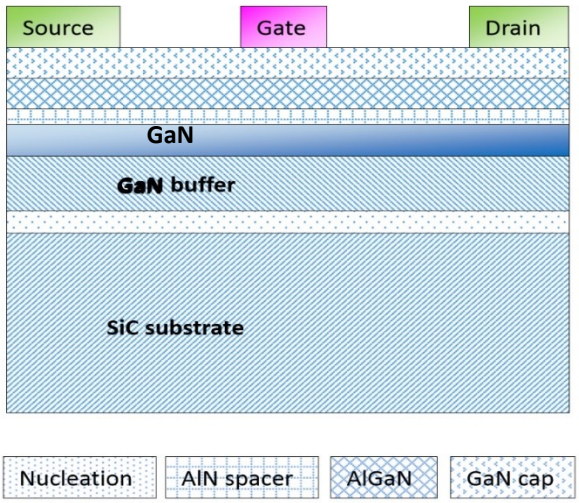

Figure 2-7: Cross-Sectional view of a GaN HEMT [29]

The MMIC in this work was designed by using the NRC GaN150 v1.4 process provided by the National Research Council of Canada. The GaN-based HEMT technology in the process was fabricated on 3-inch silicon carbide wafers of 75 µm thickness [29]. The cross-section view of the GaN HEMT devices is shown in Figure 2-7. In this process, GaN HEMT layers are grown on a SiC substrate which has a high thermal conductivity. The high thermal conductivity helps GaN HEMT devices dissipate the self-heating quickly and allows them to be operated at high power levels [30]. A nucleation layer and a GaN buffer layer are inserted between the undoped GaN layer and SiC substrate. An

AIN spacer is placed above the undoped GaN layer to further separate the Two-Dimensional Electron Gas (2DEG) from the AlGaN layer. The AlGaN layer is followed by GaN cap and ohmic contacts are finally used for HEMT device terminals. The HEMTs, featuring a 150-nm gate length and 2 fingers per device, have a T-shaped design instead of field plate design in order to obtain better frequency performance. Compared to NRC 500nm GaN process, this 150-nm GaN process results in a nominal f_T of 35 GHz and a nominal f_{max} of 75 GHz. Thus, it is safe enough to design circuits operating at X-band using GaN HEMT devices from the process.

Table 2-1: GaN HEMT Critical DC parameters

Parameters	Units	Min	Nominal	Max
Saturation Current, J_{DSS}	A/mm	0.6	0.8	1
Threshold Voltage, V_{th}	V	-3.6	-4.2	-4.6
Gate-to-Source Voltage, V_{GS}	V	-8	-	2
Reverse gate leakage at V_{GS}=-6 V	A/mm	-	1E-5	1E-4
Cutoff Frequency, f_T	GHz	30	35	-
Max Oscillation Frequency, f_{max}	GHz	50	60	-

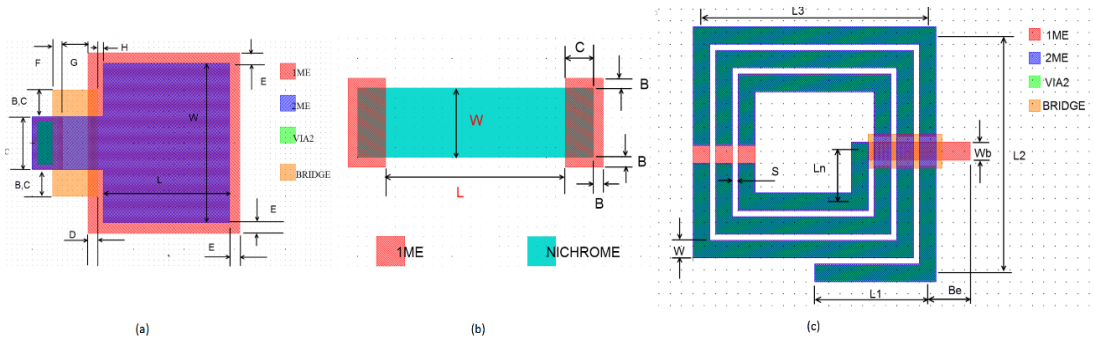

Figure 2-8: The GaN process discrete components: (a) MIM capacitor (b) Nichrome Resistor (c) Spiral Inductor

According to the foundry manual [29], the process works up to 30 V maximum drain voltage bias and yields power levels of 7 W/mm at 8 GHz. The drain to source breakdown voltage is greater than 100 V while the DC power handling capability is 10 W per mm gate-width. Critical DC process parameters for the HEMTs are shown in Table 2-1. There are two metal layers (1ME and 2ME) for interconnects in the process. The resistivity for 1ME and 2ME are respectively 27 mΩ/sq and 9 mΩ/sq. The thickness of 1ME and 2ME are 1 μm and 3 μm respectively. Structures of other discrete components are shown in Figure 2-8. The nichrome resistor has a resistivity of 50 Ω/sq. Metal-Insulator-Metal (MIM) capacitors with a capacitance density of 0.19 fF/μm^{2}are built by 2ME on top of 1ME without a via connection between them. In contrast to NRC's previous GaN500 process, the through-wafer vias are available in GaN150 process to improve the thermal performance and design flexibility.

2.6 Performance parameters

2.6.1 S-parameters

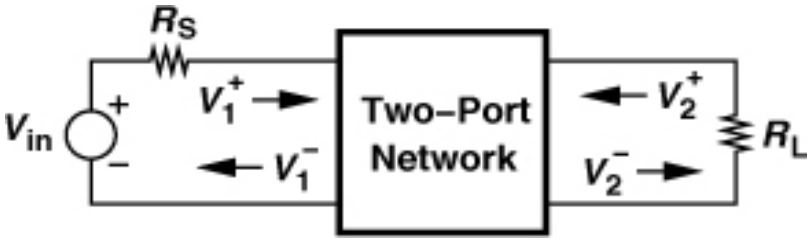

Figure 2-9: S-parameters Illustration [31]

For microwave circuits, power quantities are mostly used instead of voltage or current due to microwave theory. In addition, power can be easily measured by instruments in the laboratory while measurement of high-frequency voltage or current always turns out frustrating. To describe any circuit that can be seen as a two-port network, the so-called

"Scattering Parameters" (S-parameters) are introduced here. Figure 2-9 shows a general two-port network. The V_1^+ and V_1^- denote the incident and reflected waves at input, respectively. The V_2^+ and V_2^- denote the incident and reflected waves at output, respectively. The S-parameters can be defined as [31]

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \quad \text{Eq. 2-1}$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \quad \text{Eq. 2-2}$$

Thus, S-parameters can be derived as

$$S_{11} = \frac{V_1^-}{V_1^+}|_{V_2^+=0} \quad \text{Eq. 2-3}$$

$$S_{12} = \frac{V_1^-}{V_2^+}|_{V_1^+=0} \quad \text{Eq. 2-4}$$

$$S_{21} = \frac{V_2^-}{V_1^+}|_{V_2^+=0} \quad \text{Eq. 2-5}$$

$$S_{22} = \frac{V_2^-}{V_2^+}|_{V_1^+=0} \quad \text{Eq. 2-6}$$

As we can see from equations above, the S-parameters can be calculated only when there is no reflection wave from input or output port. Since power quantity is mostly used in microwave circuit analysis, S-parameters can be expressed in dB as

$$S_{xy}\ (dB) = 20\log|S_{xy}| \quad \text{Eq. 2-7}$$

The subscripts x and y denote the input or output port. S_{11} and S_{22} are known as input and output reflection coefficients. S_{12} is the reverse voltage gain and S_{21} is the forward voltage gain. In microwave passive circuit design, three of the four S-parameters are mostly of interest. S_{11} and S_{22} are defined as input and output Return Loss (dB), respectively. The return loss indicates accuracy of the input and output matching. S_{21} is

defined as gain (dB). For RF switches, S_{21} is defined as insertion loss or isolation when the switch is in the on or off state, respectively. The insertion loss represents extra loss introduced by the two-port network or Device-Under-Test (DUT) between two reference planes. The isolation represents how far in quantity the two reference planes are separated.

2.6.2 Linearity

The P_{1dB} and IP3 point are the two parameters used mostly to describe linearity of the circuit. Both parameters are introduced in this section, however, only the IP3 point will be will be used as a performance parameter for this work since measurement of the P_{1dB} is extremely difficult at high frequency and high-power level. Using the Volterra series, transfer function or input/output characteristic of a memoryless system can be approximately expressed as [31]

$$y(t) \approx a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \qquad \text{Eq. 2-8}$$

The dc and higher order components are eliminated in Eq. 2-8 for simplicity since they are not of interest.

2.6.2.1 1-dB Compression Point

If we have a 1-tone input signal and assume the input signal $x(t) = Acos\omega t$ in Eq. 2-8,

$$y(t) = a_1 Acos\omega t + a_2 A^2 \cos^2 \omega t + a_3 A^3 \cos^3 \omega t \qquad \text{Eq. 2-9}$$

$$= \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3 A^3}{4}\right) cos\omega t + \frac{a_2 A^2}{2} cos2\omega t + \frac{a_3 A^3}{4} cos3\omega t \qquad \text{Eq. 2-10}$$

The fundamental component has an amplitude of $a_1 A + \frac{3a_3 A^3}{4}$ which depends on the value of A. If $a_1 a_3 > 0$, the fundamental component will behave as an exponential function as A increases. If $a_1 a_3 < 0$, the fundamental component will have a compressive behavior as A increases. In most cases, RF circuits are compressive. As a result, the fundamental component behaves as a linear function of input amplitude A until A increases up to certain level. The P_{1dB} is the point at which the fundamental component becomes 1 dB less than the ideal value. Figure 2-10 illustrates the definition. The dashed line extrapolated from fundamental component indicates the ideal fundamental component without compression.

According to the definition, the input P_{1dB} can be calculated as [31]

$$20log\left|a_1 + \frac{3}{4}a_3 A_{in,1dB}^2\right| = 20\log|a_1| - 1\ dB \qquad \text{Eq. 2-11}$$

$$A_{in,1dB} = \sqrt{0.145\left|\frac{a_1}{a_3}\right|} \qquad \text{Eq. 2-12}$$

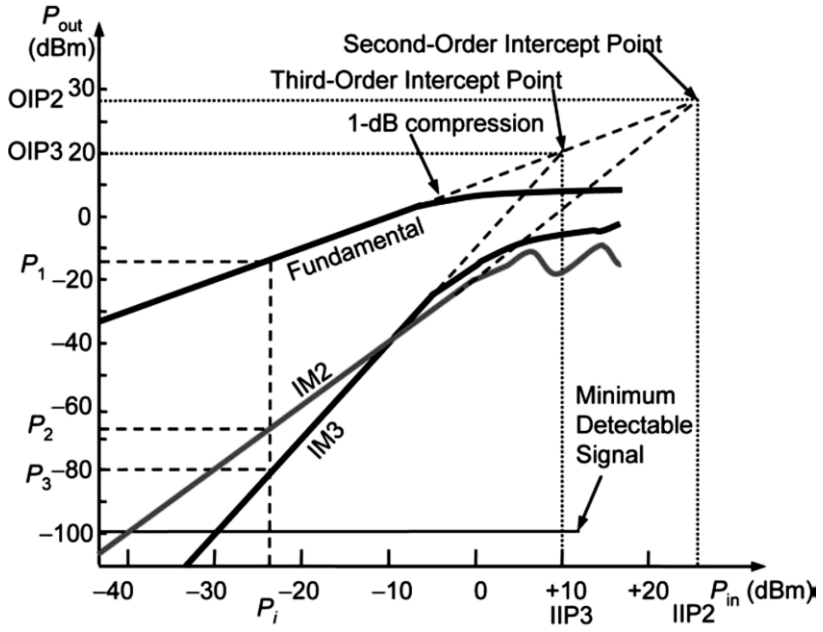

Figure 2-10: Definition of 1-dB compression point and third-order intercept point [32]

Eq. 2-12 gives the peak value of a voltage swing. The input P_{1dB} can be expressed in power quantity as

$$P_{in,1dB}\ (dBm) = 20\log\left(A_{in,1dB}\right) \qquad \text{Eq. 2-13}$$

2.6.2.2 Third-Oder Intercept

Assuming a two-tone signal is applied to input and $x(t) = A_1 cos\omega_1 t + A_2 cos\omega_2 t$, the output signal can be expressed as using Eq. 2-8

$$\begin{aligned} y(t) = {} & a_1(A_1\cos\omega_1 t + A_2\cos\omega_2 t) \\ & + a_2(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^2 \\ & + a_3(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^3 \end{aligned} \qquad \text{Eq. 2-14}$$

The intermodulation products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ in the right-hand side of Eq. 2-14 are the only concerned products here since $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ usually falls in the operating frequency channels and cannot be filtered out. After expanded the right-hand side of Eq. 2-14, amplitudes of intermodulation products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ can be expressed as [31]

$$\omega = 2\omega_1 - \omega_2 : \frac{3a_3A_1^2A_2}{4}\cos(2\omega_1 - \omega_2)t \qquad \text{Eq. 2-15}$$

$$\omega = 2\omega_2 - \omega_1 : \frac{3a_3A_1A_2^2}{4}\cos(2\omega_2 - \omega_1)t \qquad \text{Eq. 2-16}$$

As presented in Figure 2-10, the IP3 point is the point at which amplitudes of ideal fundamental and intermodulation components become equal. The Input-referred IP3 (IIP3) point or Output-referred IP3 (OIP3) point are mostly used to denote the third-order intercept point referred to either input or output. The IIP3 point then can be determined as [31]

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} \quad \text{Eq. 2-17}$$

Dividing A_{IIP3} by $A_{in,1db}$,

$$\frac{A_{IIP3}}{A_{in,1dB}} = 3.03 \approx 9.6\ dB \quad \text{Eq. 2-18}$$

Theoretically, the IIP3 point is 9.6 dB higher than the P_{1dB} point.

As mentioned above, measurement of the P_{1dB} point is challenging for microwave circuits. It will only be much more difficult to directly measure the IP3 point since the IP3 point is even higher than the P_{1dB} point. Nonetheless, the IP3 point can be calculated by using measurement of the intermodulation products. Assuming we have measured the fundamental power P_1 and intermodulation products power P_3 referred to Figure 2-10, the IIP3 point can be calculated as [32]

$$IIP_3 = P_i + \frac{1}{2}(P_1 - P_3) \quad \text{Eq. 2-19}$$

Here, the P_i denotes the corresponding input power. In Figure 2-10, the second-order intercept point is also presented. Since the second-order intercept point is considered when needed, it will not be illustrated in this work.

2.6.3 RMS Phase/Amplitude Error

The RMS error is one of the important parameters to evaluate the performance of multi-bit phase shifter and attenuator. The general RMS phase/amplitude error can be defined as [2]

$$RMS\ error = \sqrt{\frac{\sum_{i=1}^{N} \delta_i^2}{N}} \quad \text{Eq. 2-20}$$

where

$$\delta_i = x_i - r_i \quad \text{Eq. 2-21}$$

where δ_i is the phase or amplitude error of state i. x_i is the relative phase shift or amplitude of state i and r_i is the ideal phase shift or amplitude of state i To evaluate the performance of phase shifter and attenuator, definitions of RMS phase and amplitude errors are slightly different.

Phase shifter

For RMS phase error, δ_i is the phase shift error of state i. x_i is the relative phase shift of state i and r_i is the ideal phase shift of state i. For RMS amplitude error, δ_i is the amplitude error of state i. x_i is the insertion loss of state i and r_i is the insertion loss of the reference state. N is total number of phase shift states.

Attenuator

For RMS amplitude error, δ_i is the amplitude error of state i. x_i is the relative insertion loss of state i and r_i is the ideal insertion loss of state i. For RMS phase error, δ_i is the phase shift error of state i. x_i is the phase shift of state i and r_i is the phase shift introduced in the reference state. N is total number of attenuation states.

2.6.4 Switching Speed

The switching speed is the time a transistor or PIN diode needs to be switched between

the on and off states. The switching speed can be an important design consideration in many switching circuits including those used in TRMs and high-speed digital circuits.

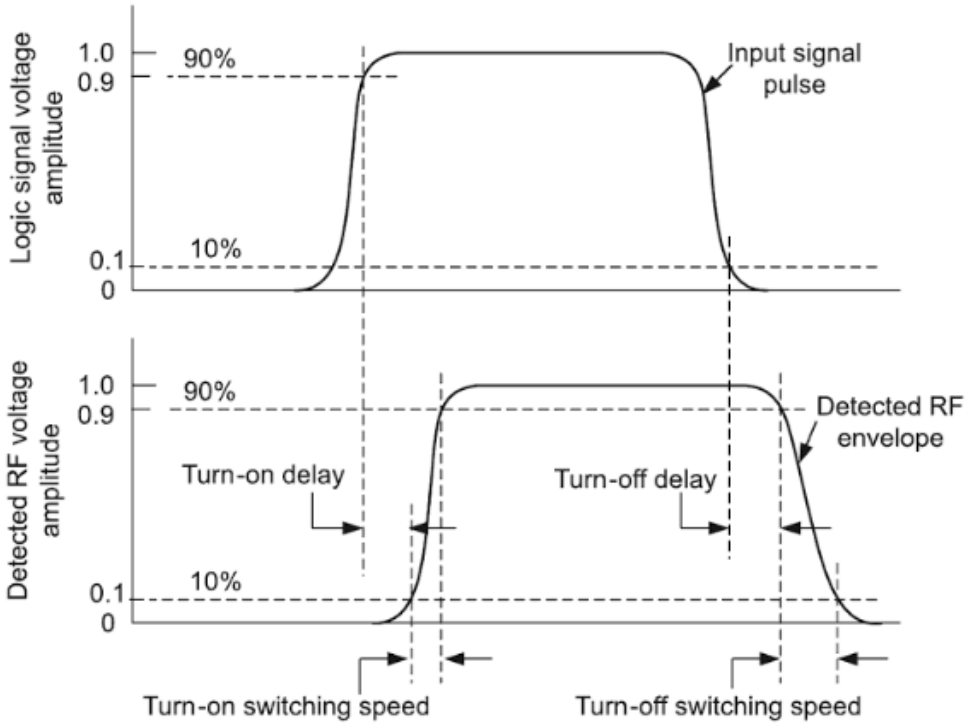

Figure 2-11: Definitions of switching speed terms [2]

Several delay terms for the switching speed are defined in Figure 2-11. “Turn-on delay” is defined as the time interval between the time when input voltage level reaches 90% of the peak value and the time when output (detected) voltage level achieves 10% of the peak value. “Turn-on delay” is the time interval output (detected) voltage level needed to increase from 10% of the peak value to 90% of the peak value. The other two terms “Turn-off delay” and “Turn-off switching speed” are defined similarly as presented in Figure 2-11.

For some applications, obtaining estimated value of the switching speed is attractive for design considerations. The switching speed can be estimated mathematically as [2]

$$\tau = R_b C_{ge} \qquad \text{Eq. 2-22}$$

where C_{ge} is the effective gate capacitance. In most cases, C_{ge} is approximately equal to two times the off-capacitance of transistor, $2C_{off}$.

2.6.5 Technology Comparison

A qualitative comparison of different switch technologies is shown inTable 2-2. As shown here, GaN switches have high power handling and switching speed as well as small required size and god integration capability with respect to other switch technologies. In terms of all the performance parameters listed, GaN switches have comparable performances and are especially suitable for compact designs.

Table 2-2: Qualitative comparison of switch technologies

Device	*PIN Diode*		*MESFET/HEMT*	*HEMT*	*CMOS*
Technology	Si	GaAs	GaAs	GaN/SiC	Si
Insertion loss	Low	Moderate	Moderate	Moderate	High
Isolation	Good	Good	Excellent	Good	Good
Bandwidth	Narrow	Narrow	Ultrabroad	Broadband	Broadband
Power handling	Very high	Moderate	Moderate	High	Low
Switching speed	Low	High	Very high	High	High
Power consumption	High	High	Low	Moderate (high power); low (low power)	Low
Integration capability	Limited	Good	Good	Good	Excellent
Size	Large	Small	Small	Very small	Very small

2.7 Conclusion

In this chapter, background of this work was given. Radio fundamentals were introduced first, followed by an introduction of phased arrays and phased array TRMs. The proposed TRM was briefly described as well as the GaN process. Definitions of performance parameters were also illustrated.

Chapter 3 Process Validation and Measurements

The dc, small-signal and large-signal measurement of the fabricated 0.15-µm GaN HEMTs in common-source structure were performed. In this section, measurement setup and results are detailed. Comparison between simulated and measured results is presented. In addition, discrepancy analysis is also provided.

3.1 Device-Under-Test (DUT) Overview

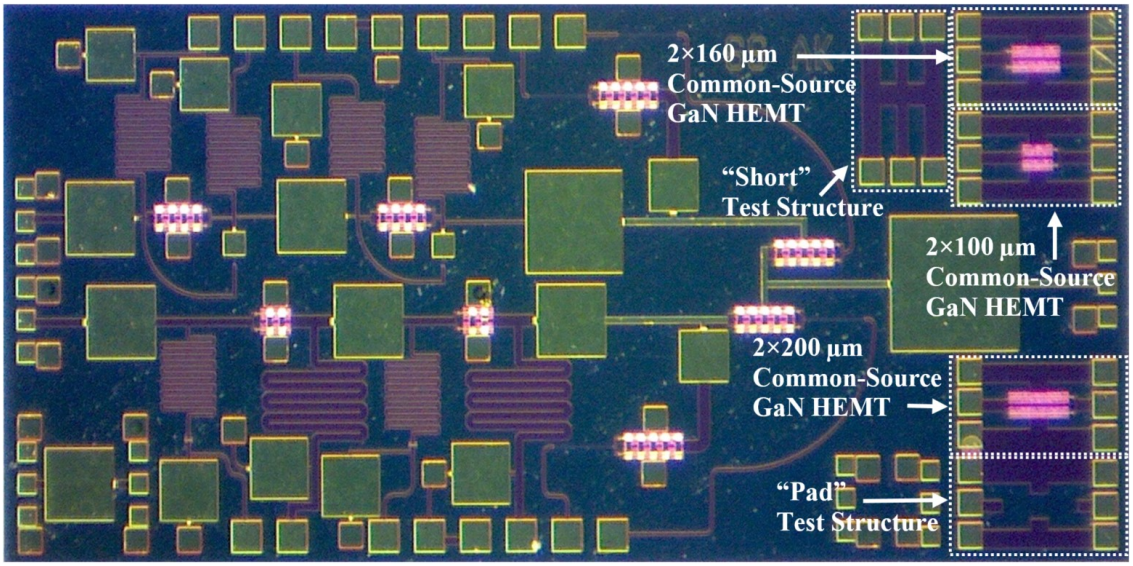

Figure 3-1: Photograph of the GaN chip design by Sumit Saha et al.

The common-source GaN HEMT was designed by Sumit Saha [11] and fabricated in the NRC GaN150 v1.01 process. The fabricated common-source GaN HEMTs have three different gate widths: 2×100 µm, 2×160 µm and 2×200 µm. As illustrated in Figure 3-1, three common-source GaN HEMTs of varied sizes have distinctive gate orientations. The 2×100 µm and 2×160 µm common-source GaN HEMTs have the same gate orientation and the gate terminal of both HEMTs faces the right-hand side of the chip. The gate terminal of the 2×160 µm common-source GaN HEMT faces the left-hand side of the

chip. All the three GaN HEMTs are connected to the RF pads in the same manner. All the RF pads are designed as Ground-Signal-Ground (GSG) pads to land probes with a 100-μm pitch. The source terminal is connected to the ground pads while the gate and drain terminal are connected to the signal pads on both sides, respectively.

3.2 DC Measurement Setup

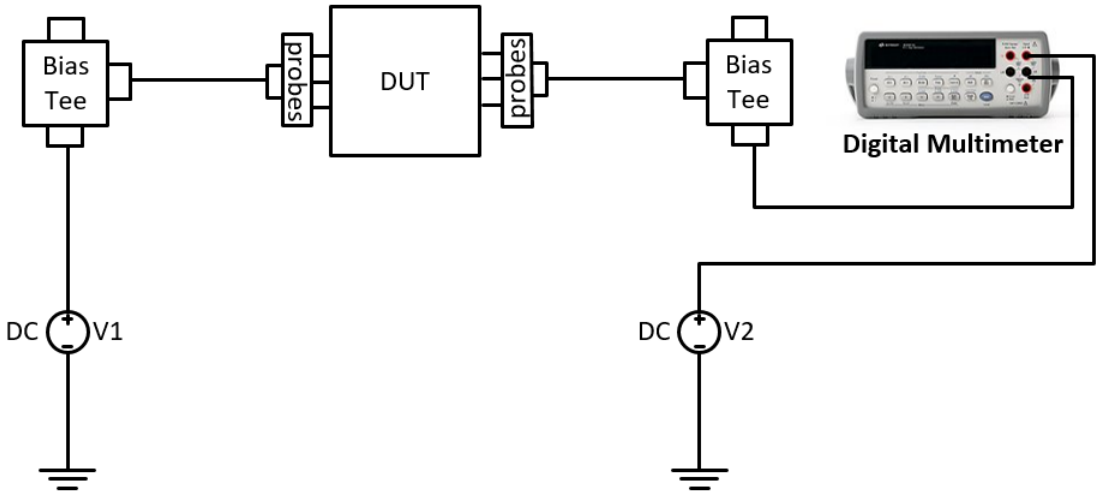

Figure 3-2: DC measurement setup

The DC measurement measures the I-V characteristic of common-source GaN HEMTs.

Figure 3-2 presents the DC measurement setup. In this setup, DC bias voltages are applied to the DUTs through bias tees. The digital multi-meter is inserted between the "V2" bias voltage and the bias tee. In DC measurement of the common-source GaN HEMTs, "V1" denotes the gate bias voltage and "V2" denotes the drain bias voltage.

3.3 Small-Signal Measurement Setup

The small-signal S-parameter measurement of the common-source GaN HEMTs is performed in order to validate the small-signal model for GaN HEMTs in design kit and further ensure that this work is a fabrication-driven design.

3.3.1 Measurement Setup

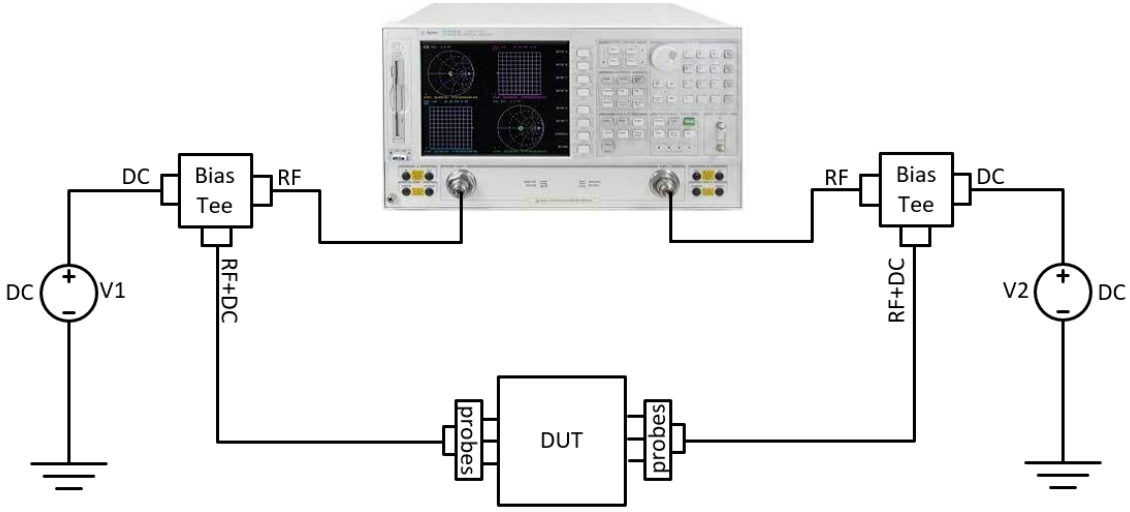

Figure 3-3: Small-signal S-parameter measurement setup

The small-signal S-parameter measurement setup is presented in Figure 3-3. The Agilent 8722ES Vector Network Analyzer (VNA) is utilized to generate RF signal and measure the S-parameters. Bias tees are placed to feed DC bias voltage to DUTs. In the setup, both VNA and DC power supplies are connected to the corresponding ports in bias tees. The RF+DC port of bias tees is then connected to the probes through a female to male connector. For the common-source GaN HEMTs, "V1" denotes gate bias voltage V_G while "V2" denotes drain bias voltage V_D.

3.3.2 De-Embedding Technique

"SOLT" Calibration Method

In simulation, all RF signal sources and DC power supply are assumed ideal without any loss. Also, RF and DC cables used to connect instrument and DUT are also ideal. However, all these losses have not been accounted for will destroy the measurement results. Thus, de-embedding is mandatory for small-signal S-parameter measurement. Here, calibration kit and substrate for Picoprobes from GGB Industries Inc. is used and

the “SOLT” calibration technique [33] is selected for de-embedding. The “SOLT” calibration procedure is given below.

1. The “T5150” calibration sequence for the probes was loaded into VNA.
2. A full two-port “SOLT” calibration was performed as
    1) The “Short” structure was inserted between probe tips and calibrated.
    2) The “Open” structure was inserted between probe tips and calibrated.
    3) The “Load” structure was inserted between probe tips and calibrated.
    4) The “Thru” structure was inserted between probe tips and calibrated.

A 50-Ω load is placed between the signal and ground pads in the “Load” structure. After the “SOLT” calibration is performed, all the losses introduced by non-ideal components should be de-embedded and the VNA is ready for small-signal S-parameter measurement.

Two-Step De-Embedding Method

Despite “SOLT” calibration method is implemented to calibrate ports to the tips of probes, the effects of RF pads and interconnects are not accounted for. An additional two-step de-embedding method is used to eliminate these parasitic effects. There are several de-embedding methods for removing these parasitic effects, however, this two-step de-embedding method is selected due to a compromise between complexity of test structures and accuracy of the de-bedding method. The mathematical deduction of this two-step de-embedding method has been detailed in [34]. The procedure of this two-step de-embedding method is illustrated here.

1. The s-parameter measurement of three structures was performed.
    1) S-parameters of the “Open” structure [S_{open}] was measured.

2) S-parameters of the "Short" structure [S_{short}] was measured.

3) S-parameters of the "DUT" [S_{DUT}] structure was measured.

2. [S_{open}], [S_{short}] and [S_{DUT}] were then converted to [Y_{open}], [Y_{short}] and [Y_{DUT}].

3. The actual Y-parameters of transistor were calculated as

$$Y_{trans} = \left(\left(Y_{DUT} - Y_{open}\right)^{-1} - \left(Y_{short} - Y_{open}\right)^{-1}\right)^{-1} \qquad \text{Eq. 3-1}$$

3.4 Large-Signal Third-Order Intermodulation (TOI) Measurement Setup

Small-signal S-parameter measurement can only measure performance of the DUT under small-signal condition. However, small-signal performance of the DUT is not sufficient to describe the overall performance of designs for high power application. The large-signal TOI measurement is used to measure linearity performance (e.g. IP3 and P_{1dB}) of the DUT. As mentioned in Section 2.6.2.2, P_{1dB} will not be measured here due to the power limitation of instrument and high operating frequency.

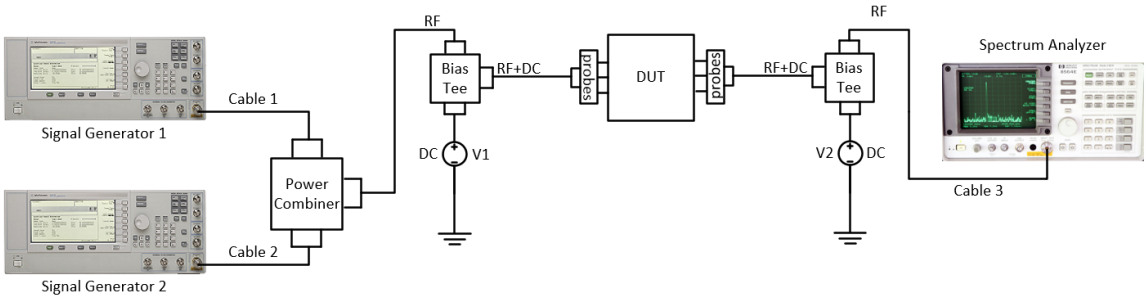

Figure 3-4: Large-Signal TOI Measurement Setup

3.4.1 Measurement Setup

The large-signal TOI measurement setup is illustrated in Figure 3-4. Two signal generators working up to 20 GHz are utilized to provide high power RF signal and are

connected to a power combiner/splitter through Cable 1 and 2. The combined high-power RF signal goes into the RF port of bias tee through a connector. Meantime, a DC power supply is connected to bias tee. The bias tee is then connected to the probes. On the other side, output RF signal goes into a spectrum analyzer through Cable 3. Note that there are only three high-quality RF cables used in this measurement setup. Similar to bias voltage setting in small-signal S-parameter measurement, "V1" denotes the gate bias voltage V_G and "V2" denotes the drain bias voltage V_D for common-source GaN HEMTs.

3.4.2 De-embedding Technique

In the small-signal measurement, losses introduced by non-ideal components (e.g. RF cables, power combiner, probes etc.) are not negligible compared to the applied and output RF signals. The de-embedding procedure consists of two parts: large-signal and small-signal de-embedding. Large-signal de-embedding uses Signal Generators and Spectrum Analyzer to characterize the losses introduced by RF cables and power combiner while small-signal de-embedding utilizes VNA to measure the losses of bias tees and probes.

Large-Signal De-Embedding

1. Cable 1 was inserted between Signal Generator 1 to Spectrum Analyzer and the power degradation was measured.
2. Cable 2 was inserted between Signal Generator 1 to Spectrum Analyzer and the power degradation was measured.
3. Cable 3 was inserted between Signal Generator 1 to Spectrum Analyzer and the power degradation was measured.

4. The power combiner was connected to Signal Generator 1, 2 and Spectrum Analyzer through Cable 1, 2 and 3 as shown in Figure 3-4. No bias tee and DUT was needed here. The power degradation was measured.

Small-Signal De-Embedding

1. A 3.5 mm female-to-female adapter was inserted between Port 1 and Port 2 of the VNA. The insertion loss was measured.
2. Two probes connected with two bias tees was inserted between Port 1 and Port 2 of the VNA. The "Thru" Structure of the "SOLT" calibration was inserted between two probes. The insertion loss was measured.

Note that the losses of bias tees and probes under small-signal and large-signal conditions are assumed to be equal.

3.5 Measurement results & Discrepancy Analysis

As introduced in Section 2.7.1, the common-source GaN HEMTs of three varied sizes were fabricated in the 0.15-μm GaN process which is used in this work. The dc, small-signal and large-signal measurements of the common-source GaN HEMTs were performed. The simulated and measured results are provided and the comparison is also illustrated. Meanwhile, discrepancy analysis of these results is given by side.

3.5.1 DC Measurement Results

The measured dc characteristic results are presented and compared to simulation. Figure 3-5 and Figure 3-7 shows the I-V characteristic of two varied-size GaN HEMT. Higher discrepancy appears between simulated and measured results as gate-source bias voltage rises. Specifically, measured results coincide with simulated for low gate- source voltages

(-4 V and -8 V). Measured results start to deviate as forward bias on the GaN HEMTs increases as shown in Figure 3-10. The corresponding I_D-V_{GS} characteristic is demonstrated in Figure 3-6 and Figure 3-8. For the 2×100 µm GaN HEMT, measured threshold voltage is approximately equal to simulation. For the 2×160 µm GaN HEMT, drain current appears when gate-source voltage approaches -5.8 V. Figure 3-9 illustrates the drain current difference under different bias conditions.

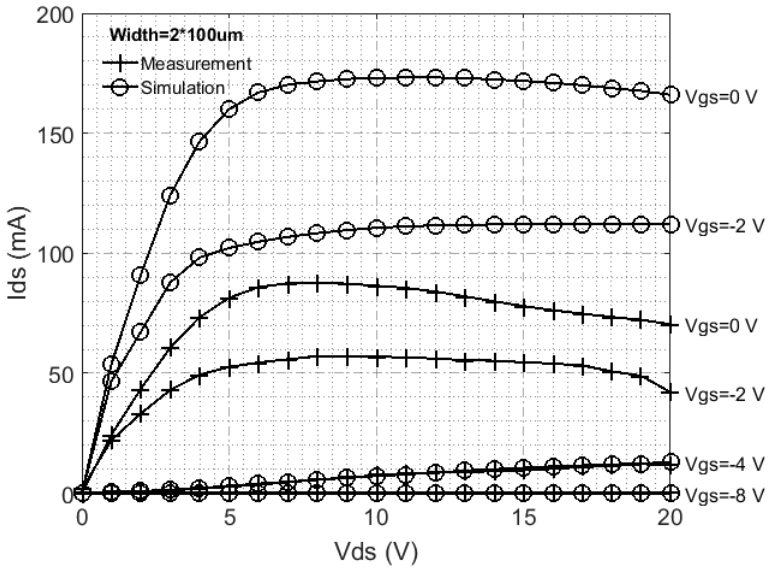

Figure 3-5: I-V characteristic of 2×100 µm GaN HEMT

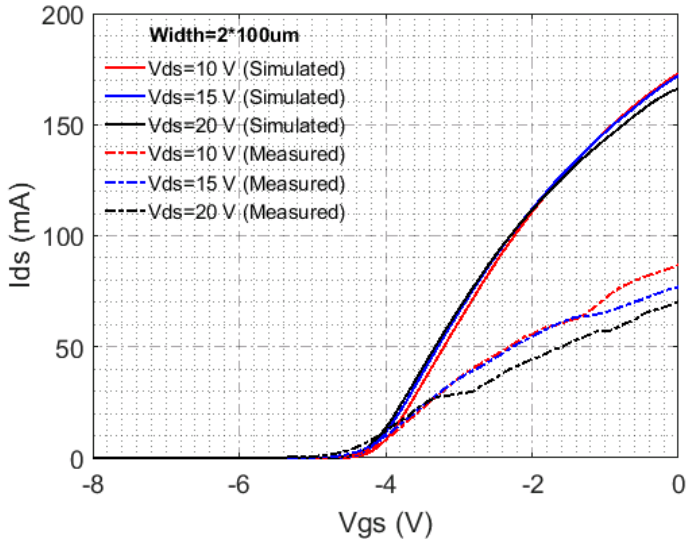

Figure 3-6: Drain current vs gate-source voltage of 2×100 µm GaN HEMT

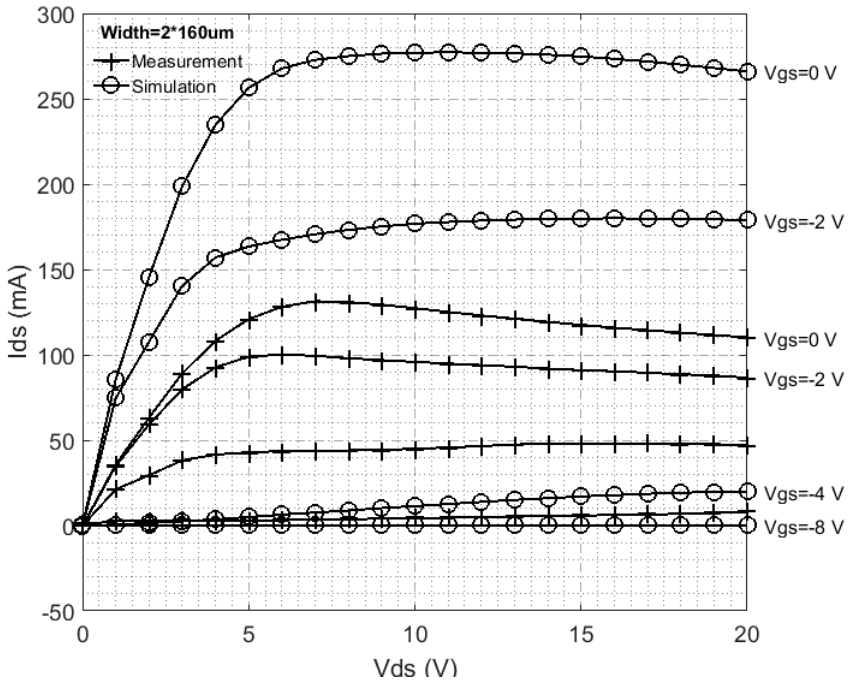

Figure 3-7: I-V characteristic of 2×160 µm GaN HEMT

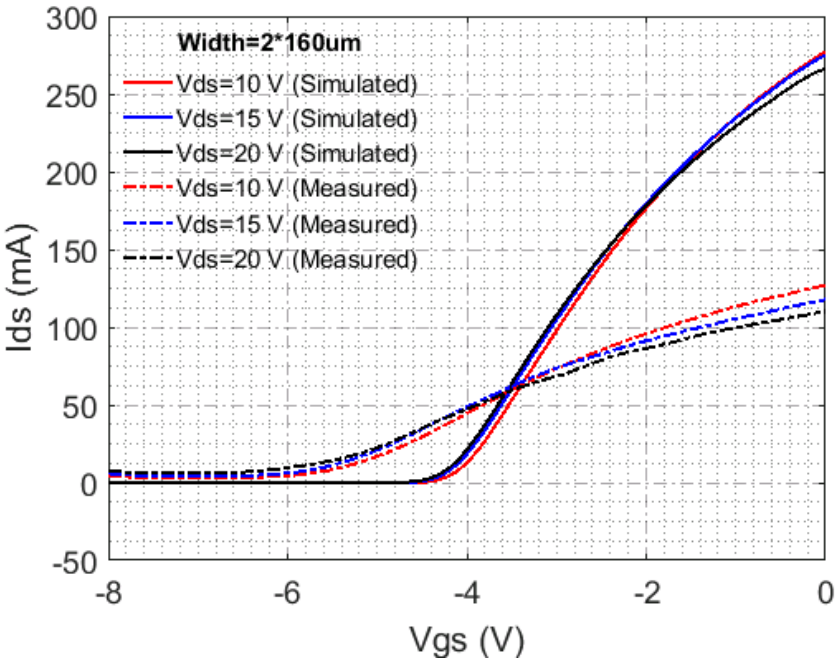

Figure 3-8: Drain current vs gate-source voltage of 2×160 µm GaN HEMT

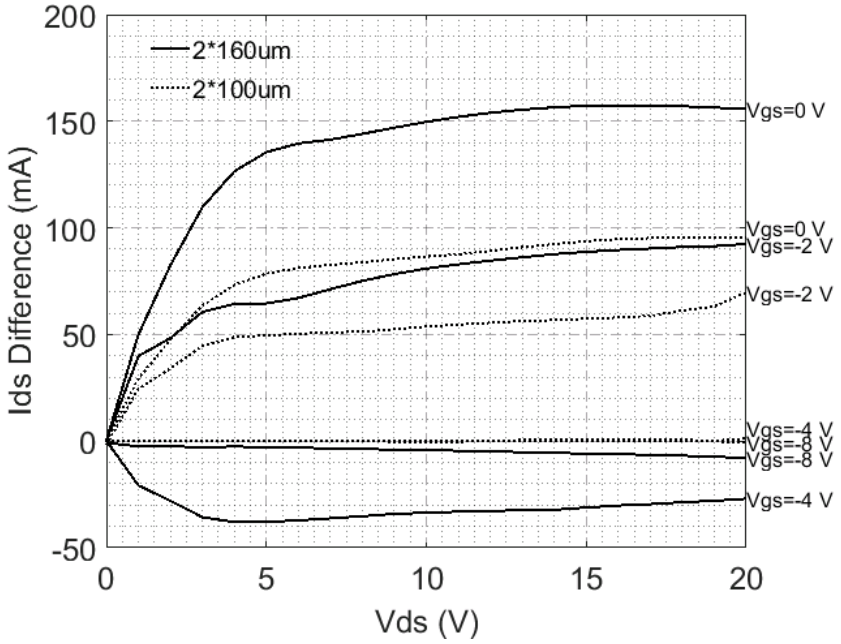

Figure 3-9: Drain current difference vs drain-source voltage

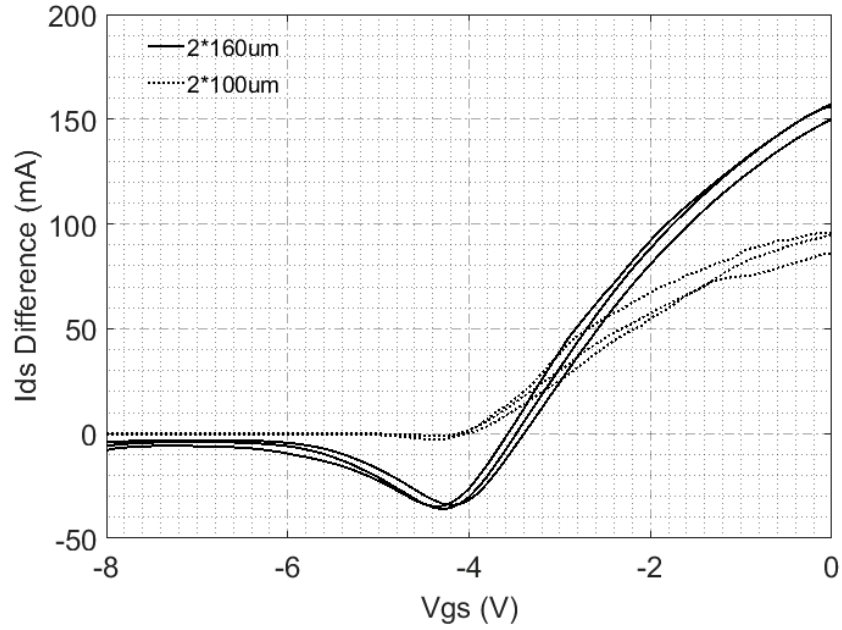

Figure 3-10: Drain current difference vs gate-source voltage

Discrepancy Analysis

The main factor which introduces discrepancy of the measured I-V characteristic is thermal effects. According to [35], thermal effects have a significant impact on the properties of semiconductor material e.g. thermal conductivity and carrier mobility. Temperature variations also have profound influence on thermal conductivity of semiconductor materials. In Figure 3-11, it is illustrated that conductivity of SC and GaN decrease to a quarter of initial values when temperature varies from 200 K to 600 K. Since the GaN HEMTs used in this work are constructed above SiC substrate, large reductions of thermal conductivity lead to a dramatic increase of temperature in a brief time as demonstrated in Figure 3-12. In this work, continuous dc (I-V) measurement was performed instead of pulsed dc (I-V) measurement because of no access to the instrument for pulsed dc measurement. This elevated temperature effect significantly reduces drain current of the DUT. Temperature effects also influence the electron velocity of semiconductors. Figure 3-13 demonstrates that the electron velocity in GaN reduces about 30% as temperature rises from 300 K to 1000 K.

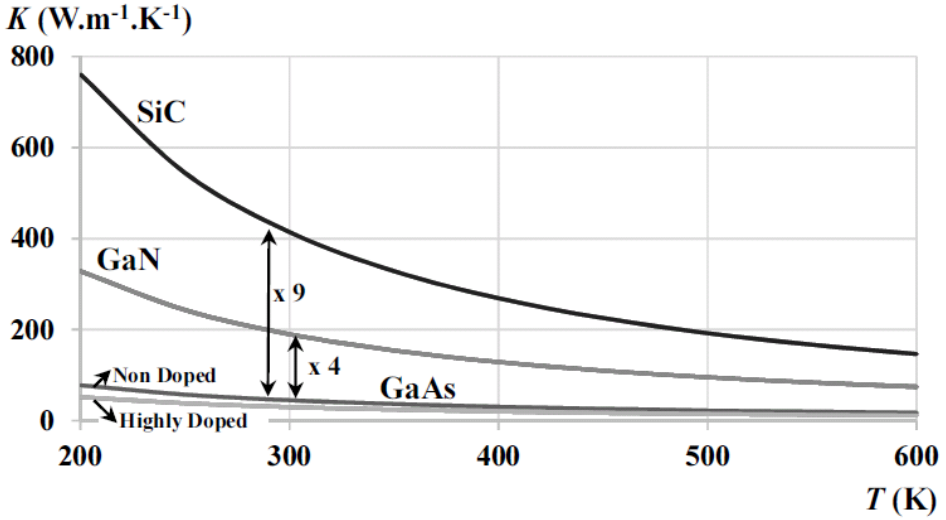

Figure 3-11: Thermal conductivity variation vs T for GaN, GaAs and SiC [35]

Since the electron velocity directly relates to the channel current, fluctuations in DC power dissipation changes the channel current. Figure 3-14 shows the pulsed and continuous bias measurement examples and indicates the discrepancy.

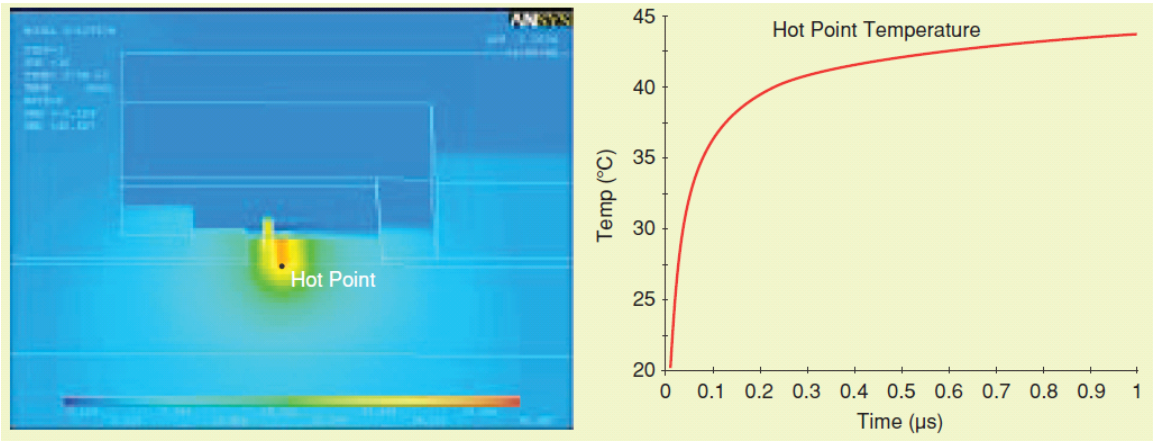

Figure 3-12: Temperature increase of AlGaN/GaN HEMTs (SiC substrate) [36]

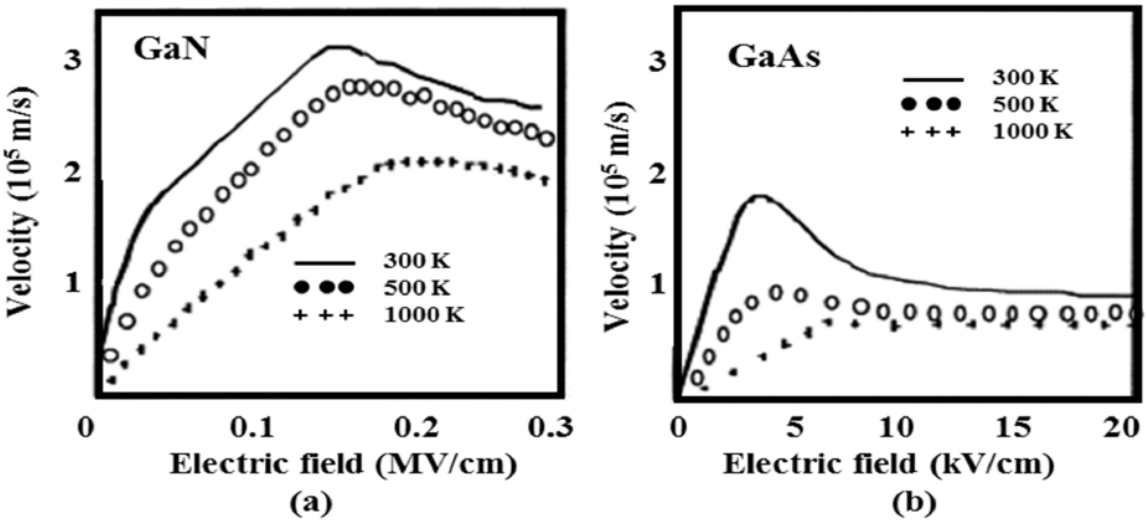

Figure 3-13: Velocity characteristics vs Electric field at different temperatures for (a) GaN and (b) GaAs semiconductors [35]

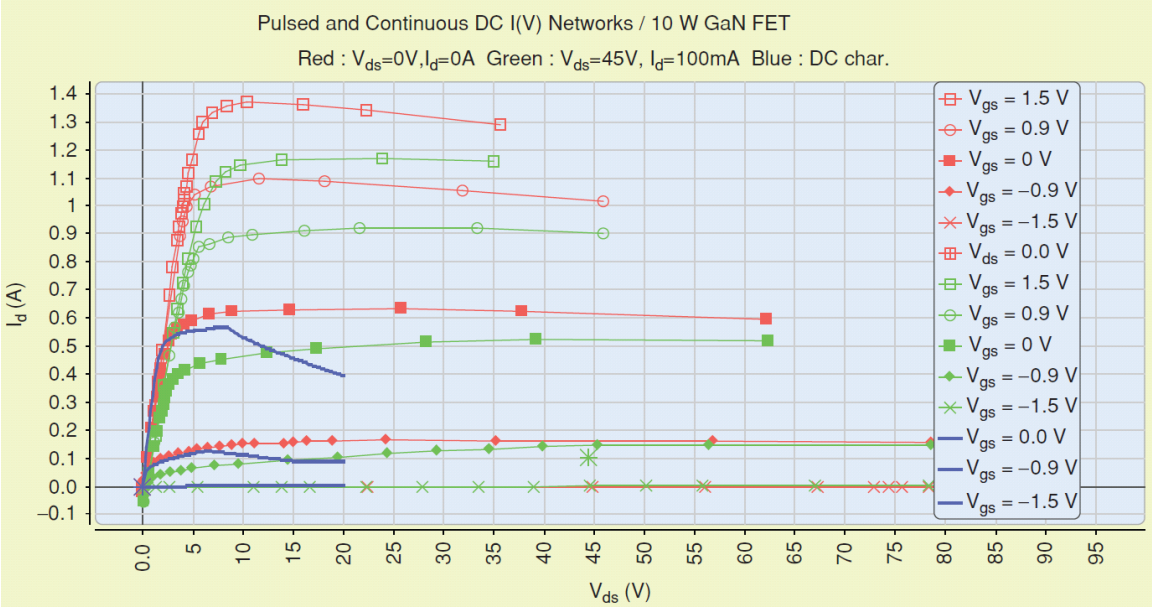

Figure 3-14: Pulsed and continuous bias measurement [36]

Several factors contribute to the discrepancy of measured I-V characteristic. The detailed analysis of contributions of each factor can be found in [35] [36]. In addition, a fact related to the discrepancy is that the transistor root model does not include thermal effects [29].

3.5.2 Small-Signal S-Parameter Measurement Results

Small-signal S-parameter measurement of the GaN HEMTs was performed to verify accuracy of the process ADS model under small-signal condition. Also, small-signal equivalent circuit parameters were extracted from the s-parameter measurement as detailed below. The s-parameter measurement results are presented in Figure 3-15**Error! Reference source not found.** to Figure 3-26**Error! Reference source not found.**. The gate-source voltage was varied from -8 V to 0V and the drain-source voltage was varied from 10 V to 20 V in a 5-V increment. Results under few bias conditions (V_{GS}=-8, -4.2, 0

V; V_{DS}=10, 20 V) are provided here. In the figures of gain, the dashed line indicates the measured S_{21} while the solid line indicates the simulated S_{21}.

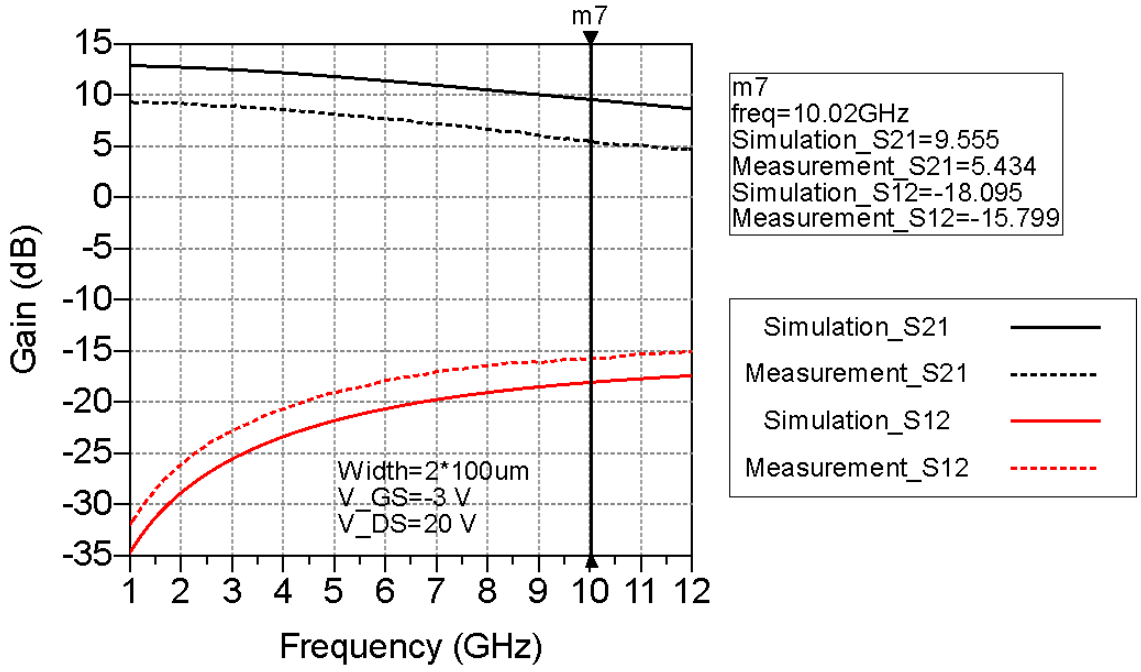

Figure 3-15: Gain (S_{21}) of the 2×100 µm GaN HEMT (V_{GS}=-3 V, V_{DS}=20 V)

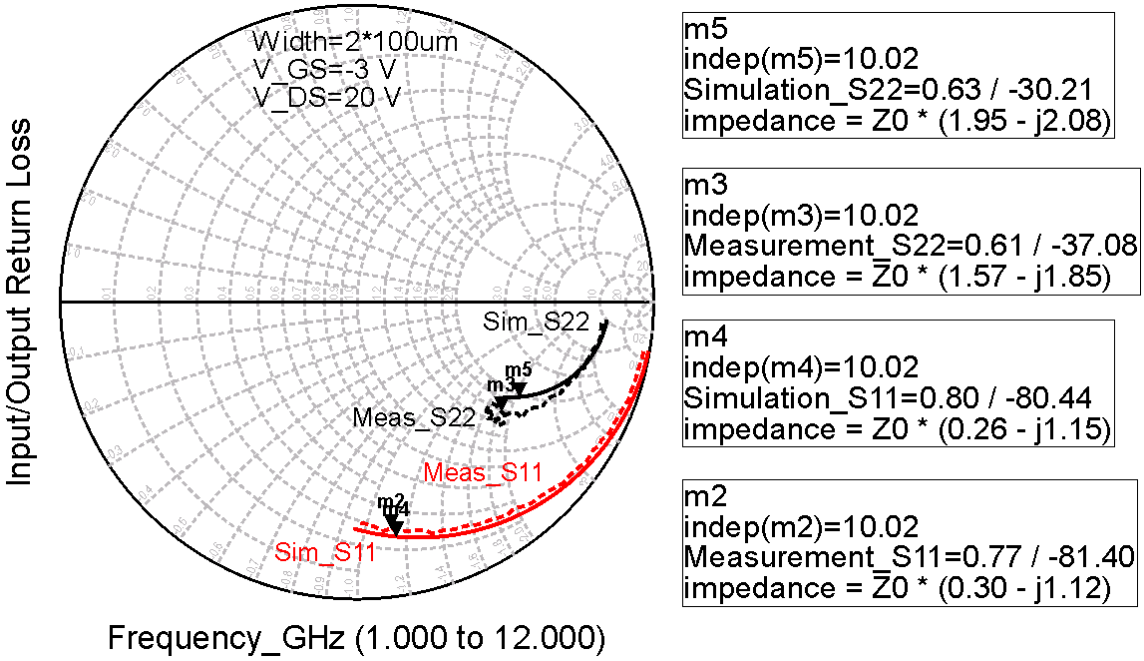

Figure 3-16: Input/output return loss (S_{11} and S_{22}) of the 2×100 µm GaN HEMT (V_{GS}=-3 V, V_{DS}=20 V)

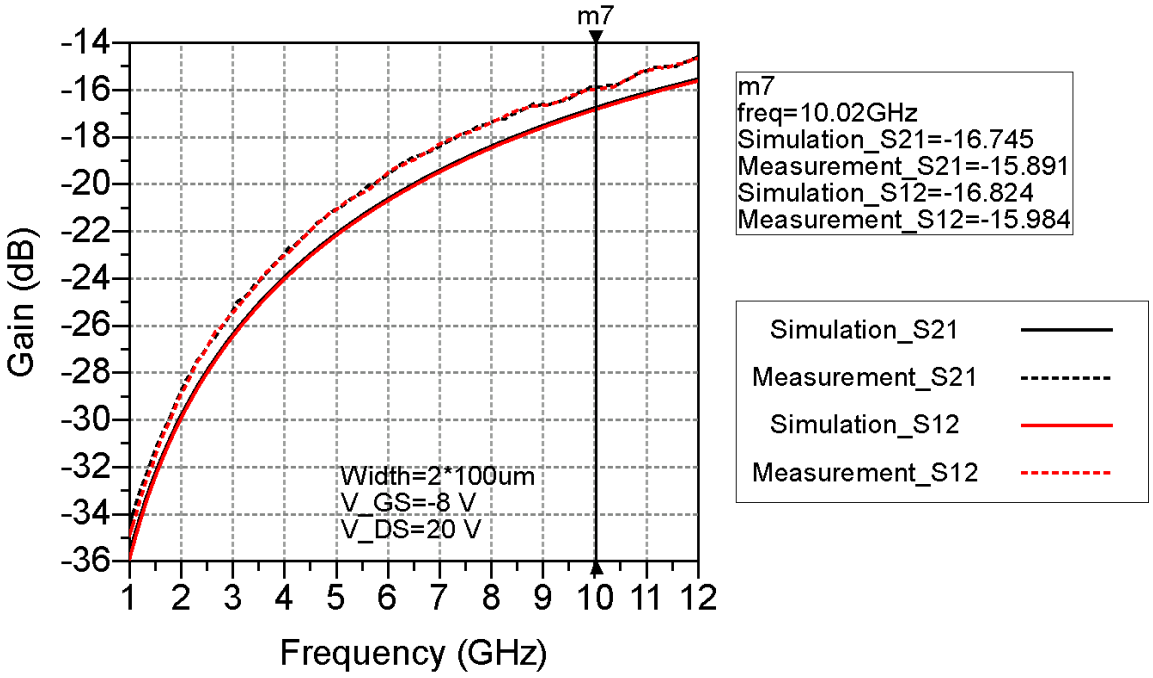

Figure 3-17: Gain (S_{21}) of the 2×100 µm GaN HEMT (V_{GS}=-8 V, V_{DS}=20 V)

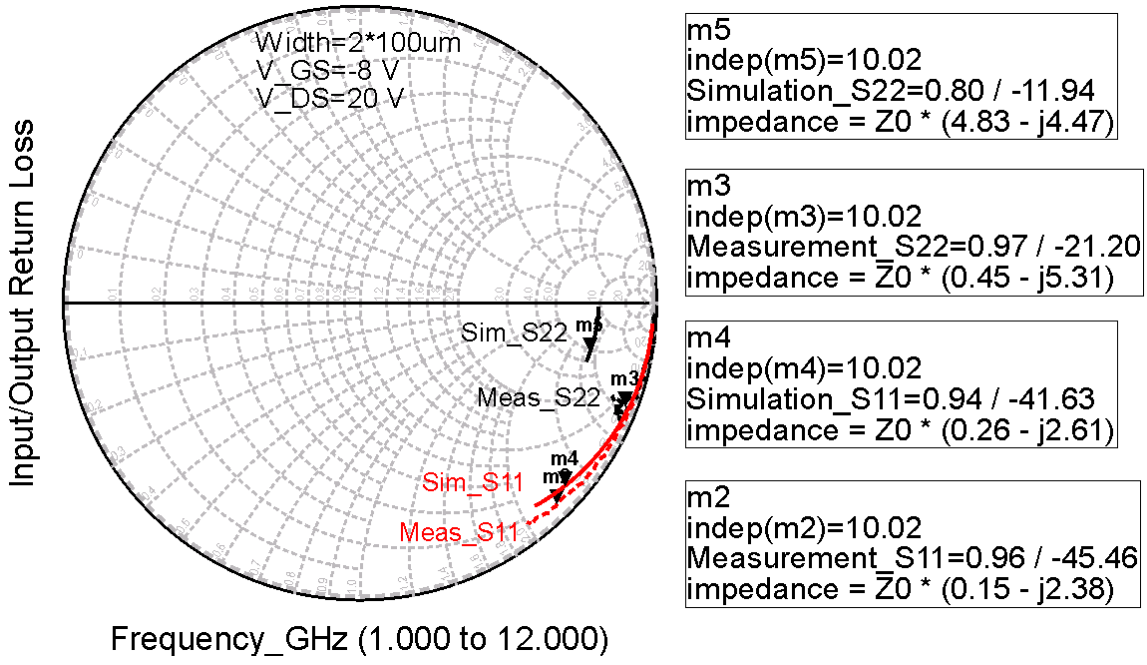

Figure 3-18: Input/output return loss (S_{11} and S_{22}) of the 2×100 µm GaN HEMT (V_{GS}=-8 V, V_{DS}=20 V)

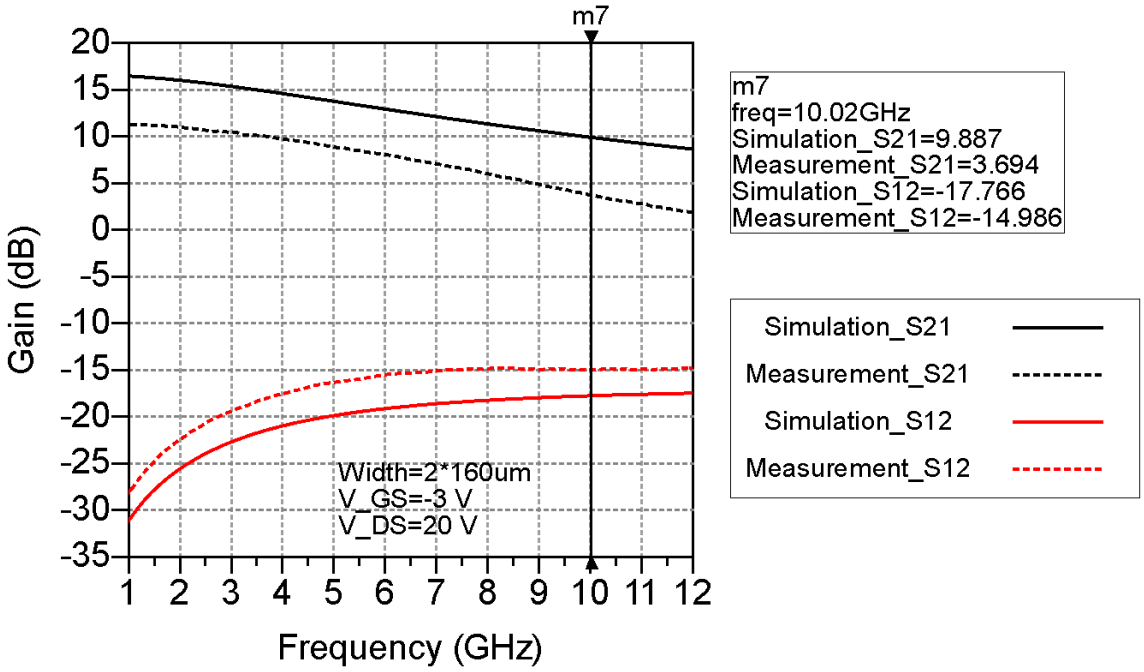

Figure 3-19: Gain (S_{21}) of the 2×160 µm GaN HEMT (V_{GS}=-3 V, V_{DS}=20 V)

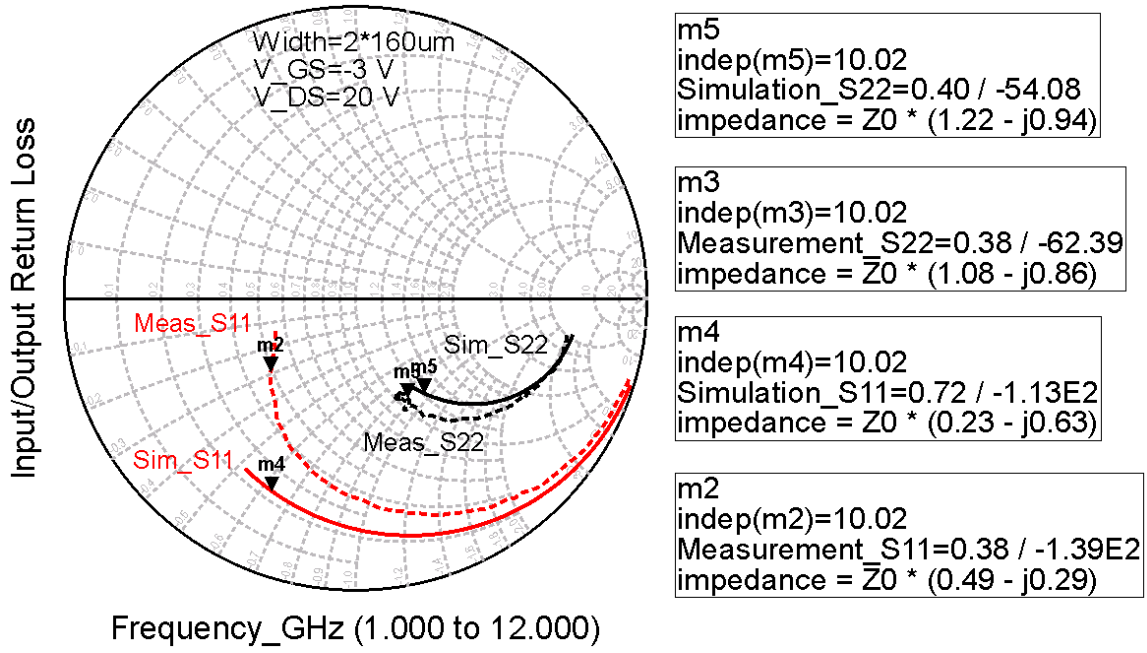

Figure 3-20: Input/output return loss (S_{11} and S_{22}) of the 2×160 µm GaN HEMT (V_{GS}=-3 V, V_{DS}=20 V)

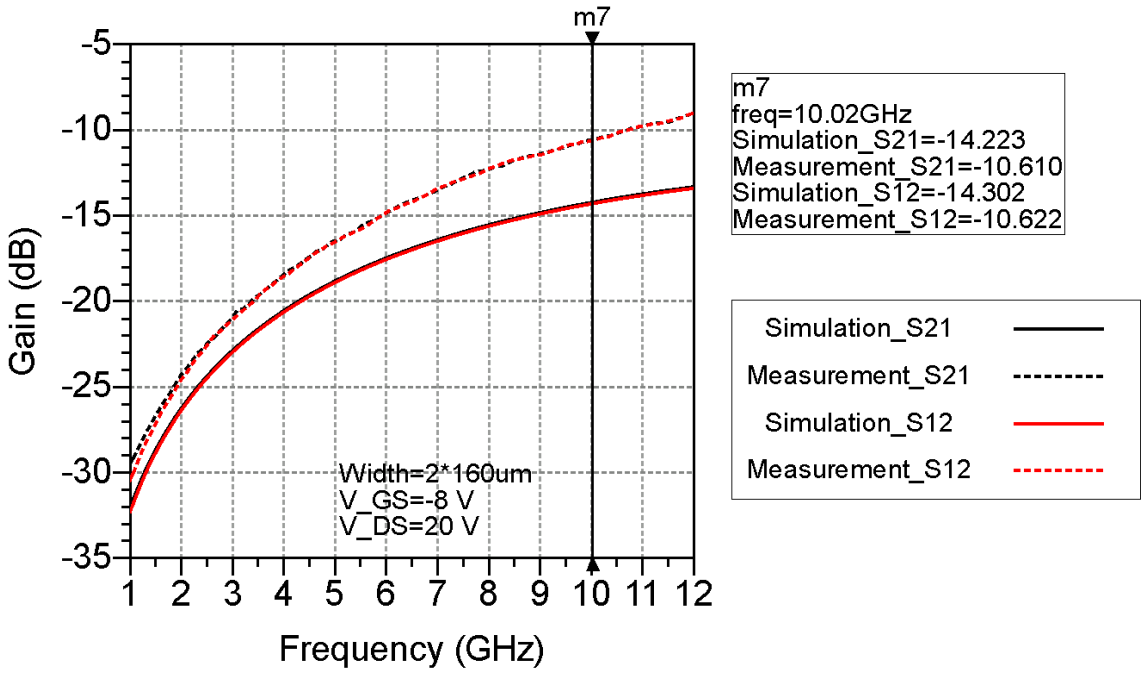

Figure 3-21: Gain (S_{21}) of the 2×160 µm GaN HEMT (V_{GS}=-8 V, V_{DS}=20 V)

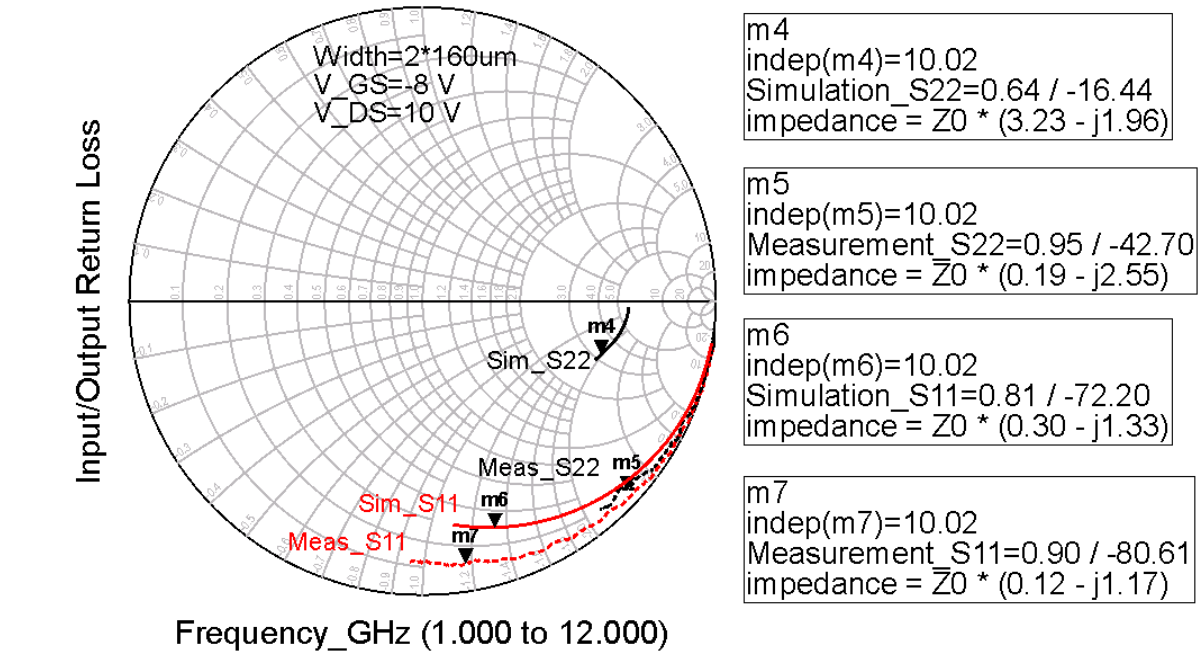

Figure 3-22: Input/output return loss (S_{11} and S_{22}) of the 2×160 µm GaN HEMT (V_{GS}=-8 V, V_{DS}=20 V)

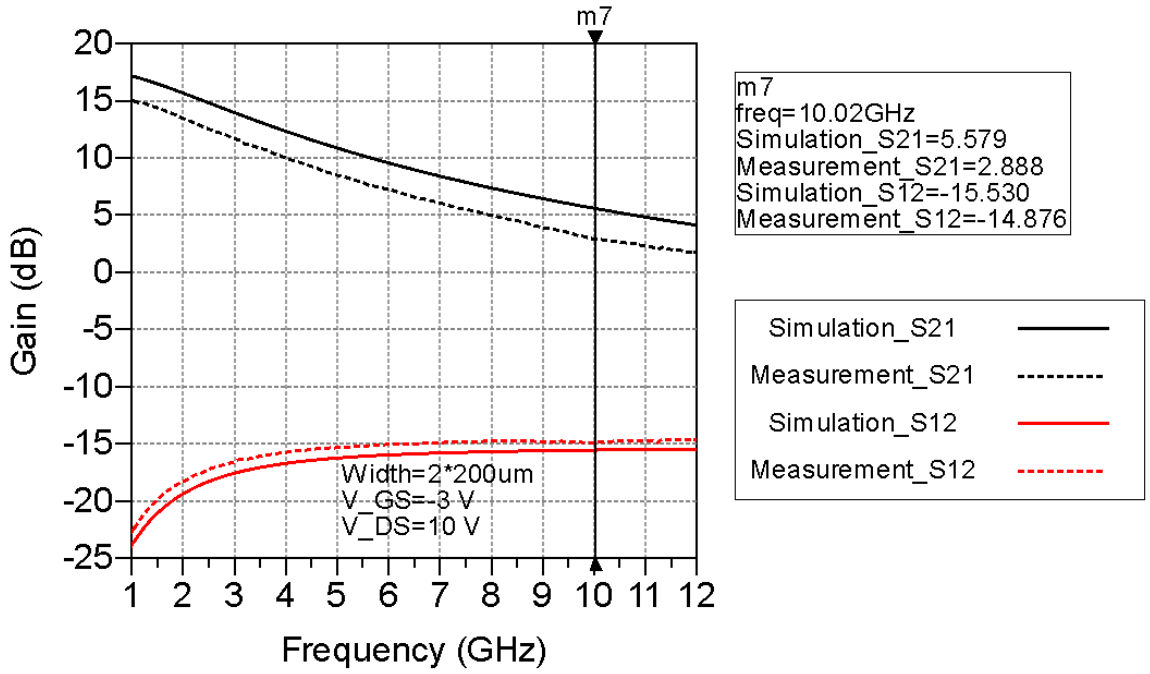

Figure 3-23: Gain (S_{21}) of the 2×200 µm GaN HEMT (V_{GS}=-3 V, V_{DS}=10 V)

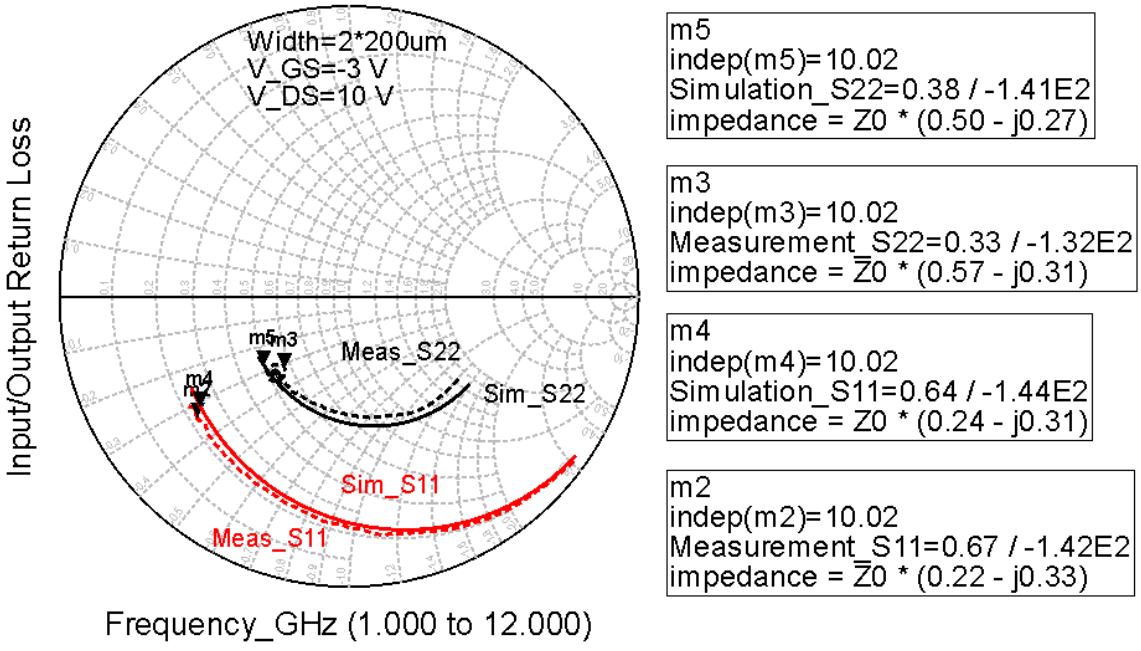

Figure 3-24: Input/output return loss (S_{11} and S_{22}) of the 2×200 µm GaN HEMT (V_{GS}=-3 V, V_{DS}=10 V)

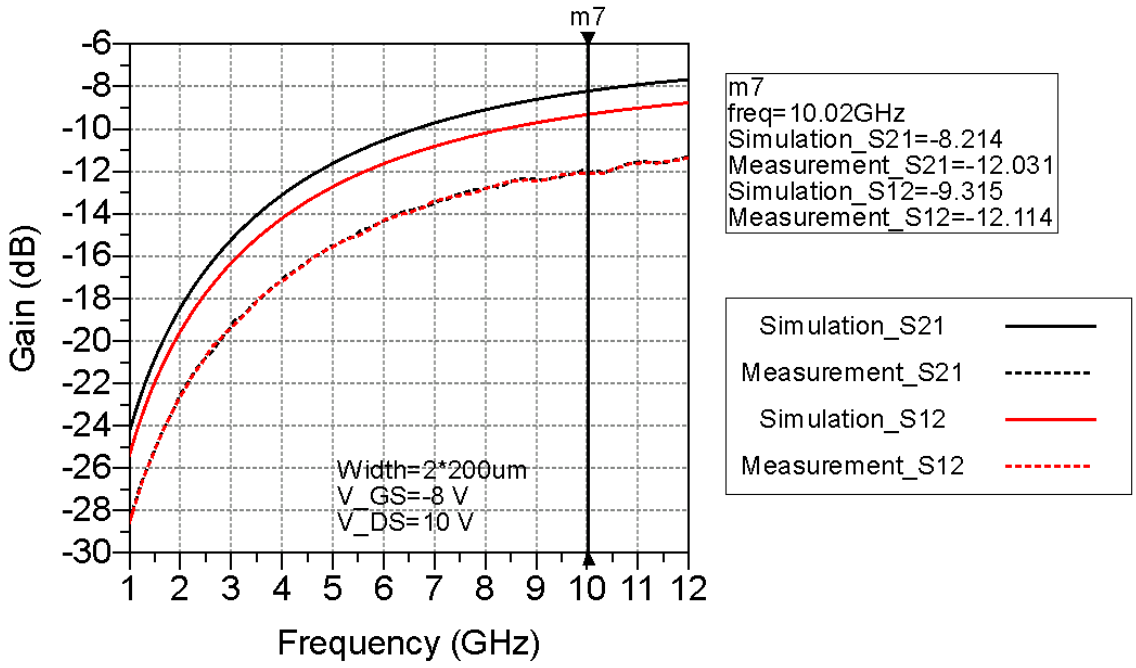

Figure 3-25: Gain (S_{21}) of the 2×200 µm GaN HEMT (V_{GS}=-8 V, V_{DS}=10 V)

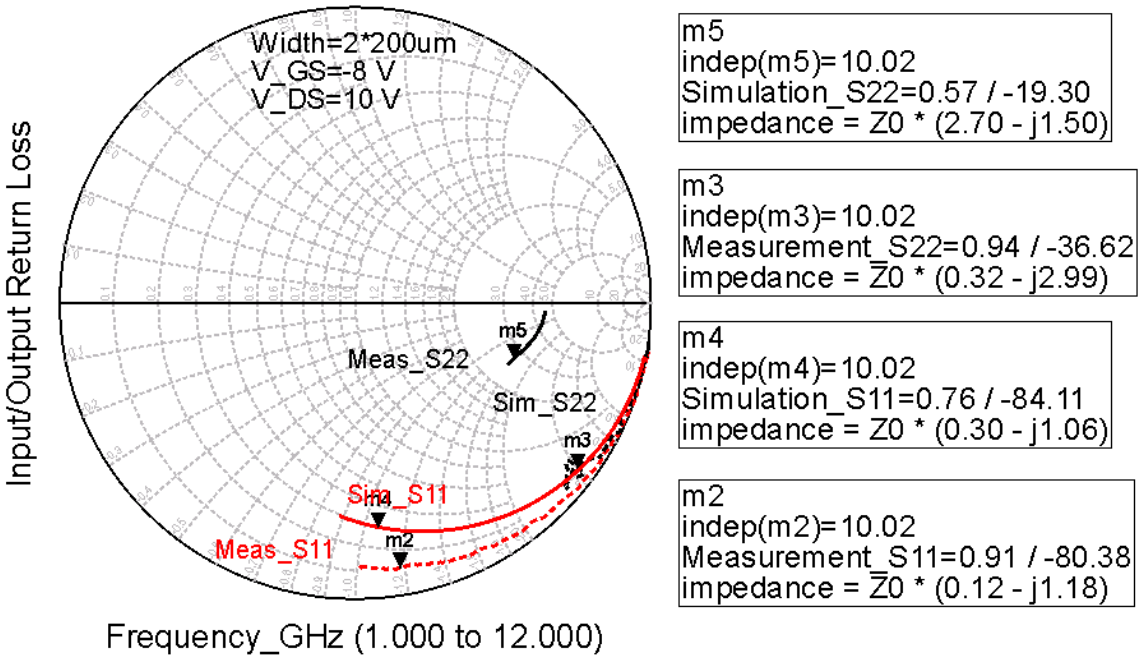

Figure 3-26: Input/output return loss (S_{11} and S_{22}) of the 2×200 µm GaN HEMT (V_{GS}=-8 V, V_{DS}=10 V)

In the figures of return loss, the red lines denote S_{11} and the black lines denote S_{22}. Meantime, the dashed lines denote the measured S_{11} and S_{22} while the solid lines denote the simulated S_{11} and S_{22}. Four markers numbered from 4 to 7 are placed to read out the specific values.

Discrepancy Analysis

As shown in the figures, there are a few discrepancies exists between measured and simulated results. First, the largest discrepancy is observed in S_{22} for all three varied sizes biased at -8 V which is well below threshold voltage. The explanation of discrepancy in S_{22} can be easily found in the foundry manual [29]. According to [29], s-parameters of the transistor model becomes less accurate as gate-source bias voltage goes below threshold, especially for S_{22}. This statement explains the largest discrepancy for the small-signal s-parameter measurement while other s-parameters have a fairly good agreement with simulation. Second, the measured S_{11} has a nearly perfect agreement with simulation under different bias conditions at low frequencies. Discrepancy appears as frequency increases. As illustrated by markers in the figures, a statement can be made that the measured results have a smaller imaginary part of input impedance. If we look into the common-source transistor from the gate, the input impedance of common-source

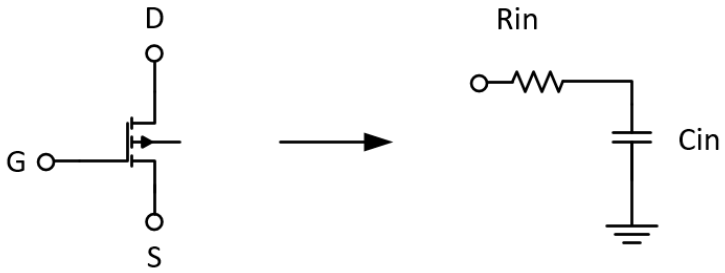

Figure 3-27: Input impedance model for common-source transistor

transistor can be modeled as a series combination of a resistor and a capacitor. Thus, the measured results have a larger input capacitance than the simulated results. The discrepancy of input capacitance is mostly contributed by the extrinsic capacitances among gate, drain and source contacts. Also, parasitic capacitances introduced by interconnects also contributes to the increase of input capacitance since it is stated that the model in the GaN design kit accounts only for the intrinsic two gate device in the foundry manual [29]. Finally, difference in S_{21} can also be seen in the figures. As we have already de-embedded the potential impacts from RF cables, probes, pads and interconnects using the SOLT calibration method and the additional two-step de-embedding method, other discrepancies can be introduced by temperature and process variations. To further validate the process, the small-signal equivalent circuit was extracted and used in the design of a simple SPDT switch. The proposed small-signal model for a GaN switch is illustrated in Figure 3-28. The switch in the on state is modeled as a simple series resistance while the switch off-state equivalent circuit consists of a large off-resistance in parallel with an off-state capacitance.

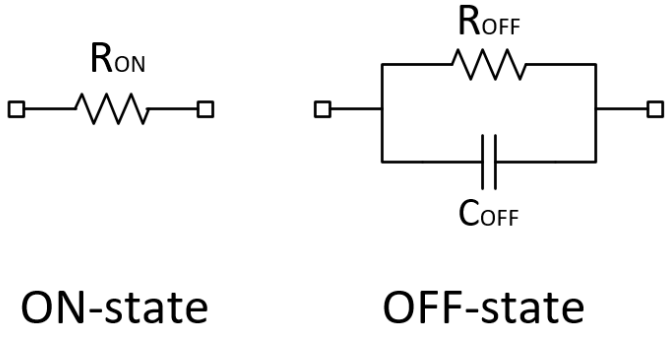

Figure 3-28: Small-signal equivalent circuit for GaN switch

Small-Signal Equivalent Circuit Extraction

The GaN switch is a common-gate device, however, we only have GaN HEMTs fabricated in common-source structure. Therefore, the problem is to determine the switch equivalent circuit components from measurement of common-source GaN HEMTs. According to [37], the on-state resistance of a GaN switch is mainly determined by the source-drain resistance for gate bias voltages higher than threshold. On the other hand, the off-state resistance is governed by the large source-drain resistance due to the suppressed 2DEG. The proposed GaN HEMT switch small-signal equivalent circuit is illustrated in Figure 3-29 [37]. In addition, source-drain capacitance dominates the off-state capacitance, the output capacitance of a common-gate device [37] [38]. A switch-based GaN HEMT model was introduced in [38] and presented in Figure 3-30. To simplify the model, all lumped-element components are linear except for the output resistance of the device which is modeled as a voltage-controlled switch

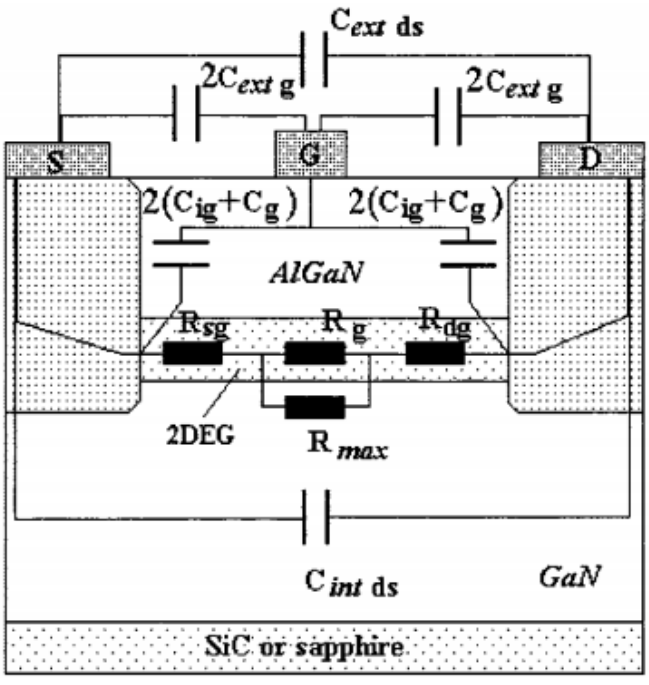

Figure 3-29: The small-signal equivalent-circuit in GaN HEMT structure [37]

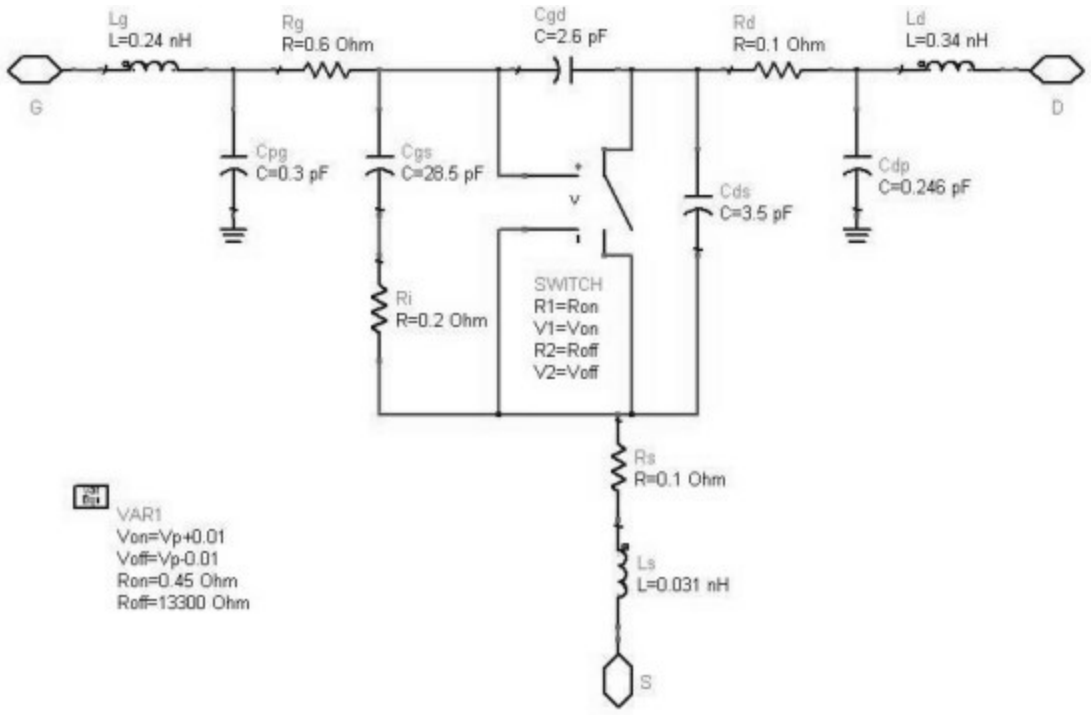

Figure 3-30: Circuit topology for the developed switch-based transistor model [38]

despite the lumped-element components indeed varies as bias changes. In this work, we assume that source-drain resistance and capacitance dominate the resistances and capacitance in the proposed GaN switch small-signal model for off state.

To determine the source-drain resistance and capacitance of GaN HEMTs, a method introduced in [39] is implemented. The small-signal equivalent circuit is shown in Figure 3-31 and equations for the small-signal equivalent circuit is presented below.

$$Y_{11} = \frac{R_i C_{gs}^2 \omega^2}{1 + \omega^2 C_{gs}^2 R_i^2} + j\omega \left(\frac{C_{gs}}{1 + \omega^2 C_{gs}^2 R_i^2} + C_{gd} \right) \quad \text{Eq. 3-2}$$

$$Y_{12} = -j\omega C_{gd} \quad \text{Eq. 3-3}$$

$$Y_{21} = \frac{g_m \exp(-j\omega\tau)}{1 + jR_i C_{gs}\omega} - j\omega C_{gd} \quad \text{Eq. 3-4}$$

$$Y_{22} = g_d + j\omega(C_{ds} + C_{gd}) \quad \text{Eq. 3-5}$$

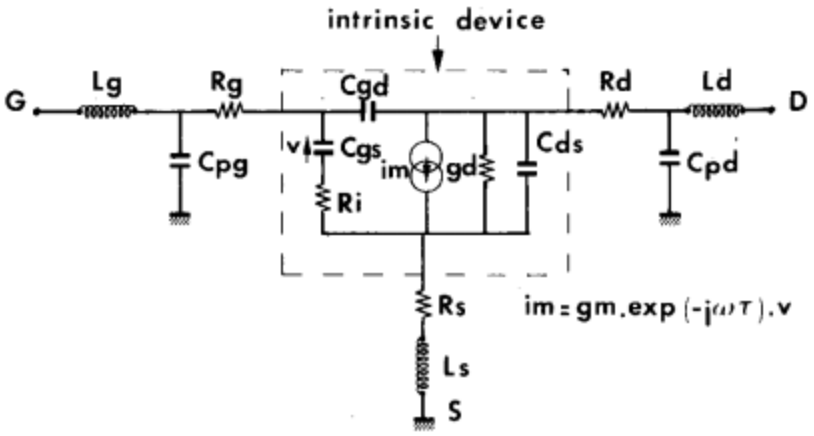

Figure 3-31: Small-signal equivalent circuit of a field effect transistor [39]

As shown in Figure 3-31, the small-signal equivalent circuit constitutes of intrinsic and extrinsic components. All the extrinsic components were assumed to be negligible here. The measured s-parameters was first converted to y-parameters. The drain transconductance g_d and the drain-source capacitance C_{ds} was then deduced from Eq. 3-3 and Eq. 3-5. The drain-source resistance R_{ds} was deduced as

$$R_{ds} = \frac{1}{g_d} \qquad \text{Eq. 3-6}$$

To avoid repetitions, the extraction of GaN switch small-signal model was only performed for the 2×100 um GaN HEMT at a drain-source bias voltage of 10V. The C_{ds} and R_{ds} extracted from the measured s-parameters are plotted as a function of gate-source voltage V_{gs} in Figure 3-32. As shown in Figure 3-32, the off-capacitance C_{OFF} and the off-resistance R_{OFF} are 33.456 fF and 3761 Ω, respectively. Similar behaviors of the C_{ds} and R_{ds} can be found in [37] (Figure 3-33).

For on-state resistance, this deduction of drain-source resistance might be accurate since small-value extrinsic components omitted in the deduction become non-negligible for on-state resistance. A more general dc approach is used and validated later.

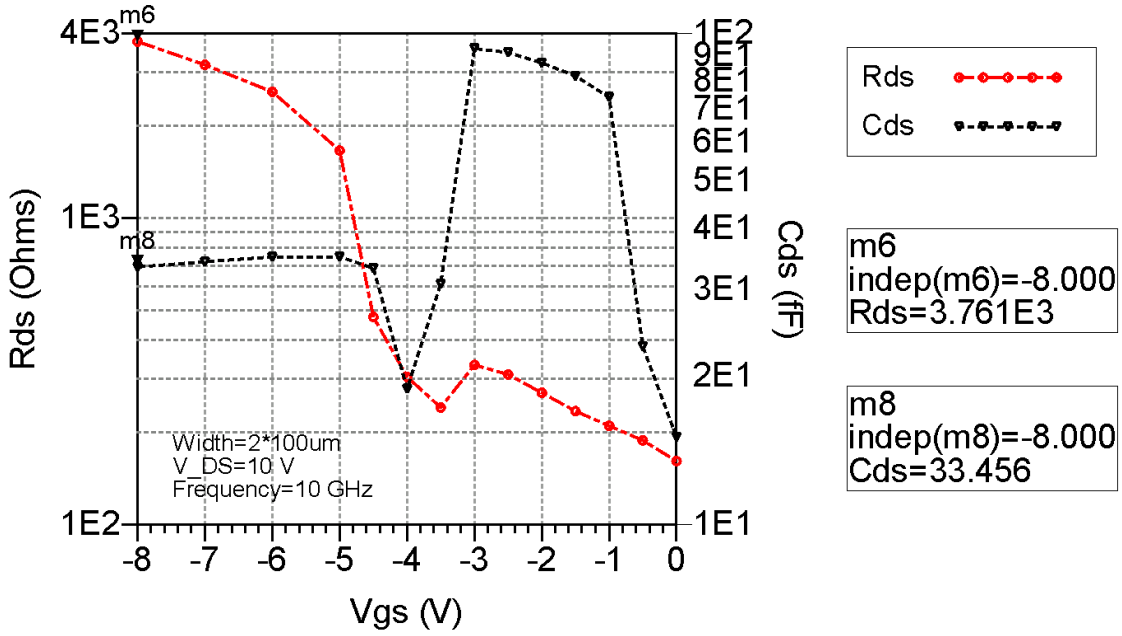

Figure 3-32: Extracted C_{ds} and R_{ds} for the 2×100 um GaN HEMT (V_{DS}=10 V, frequency=10 GHz)

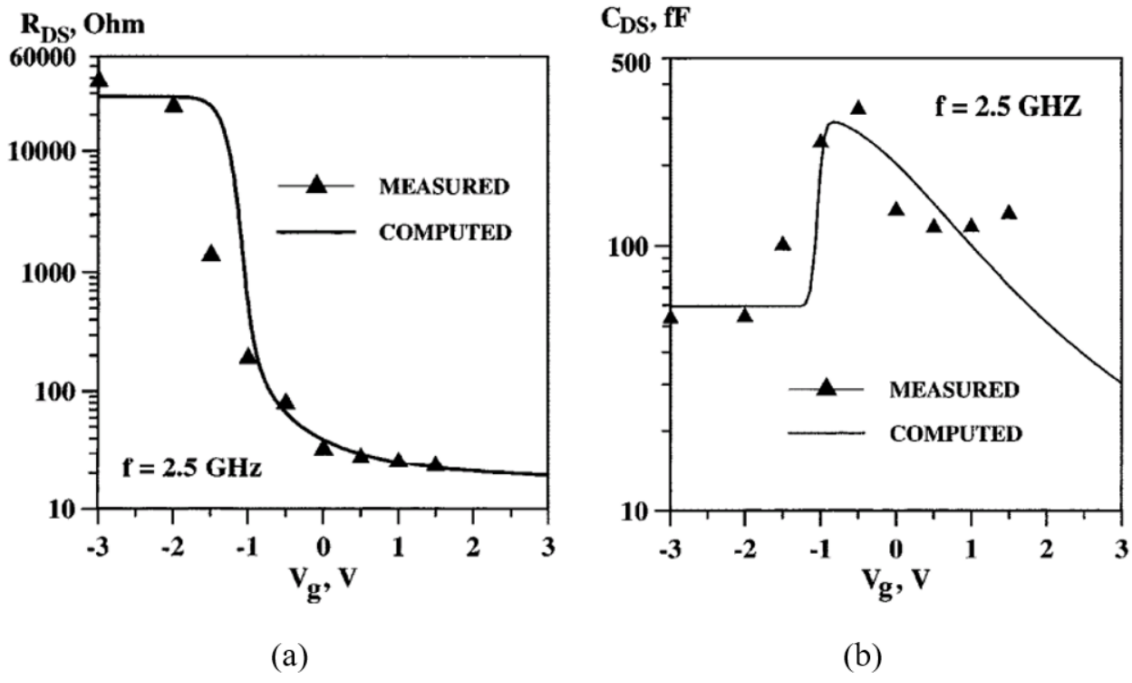

Figure 3-33: R_{ds} and C_{ds} versus dc gate voltage [37]

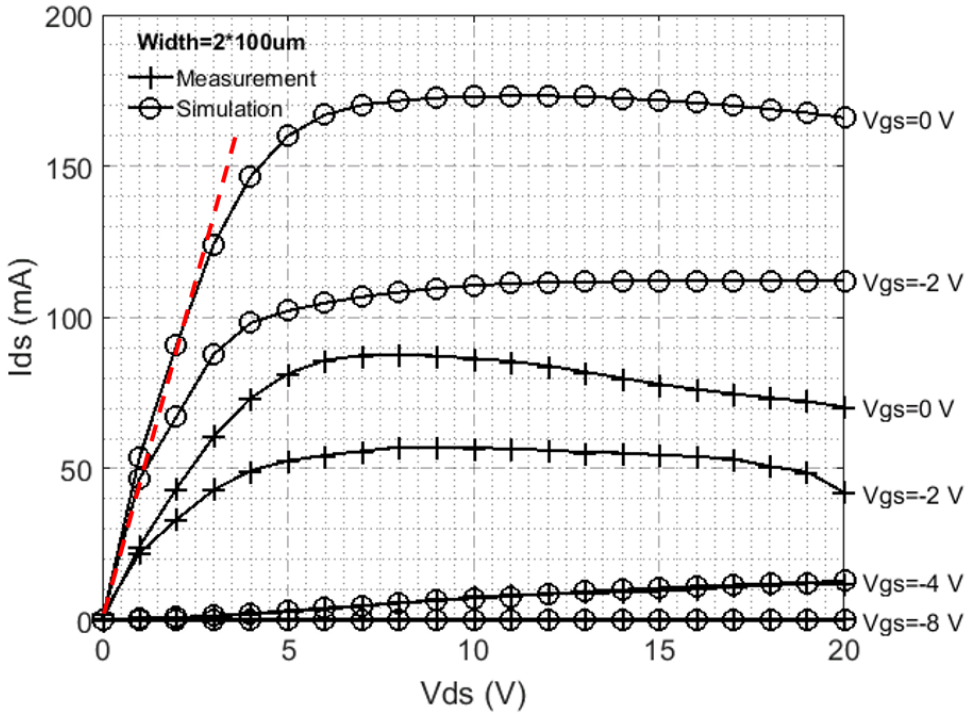

Figure 3-34: I-V characteristic of the 2×100 um GaN HEMT with extrapolated line

As demonstrated in Section 3.5.1, the measured I-V characteristic was defective due to temperature effects. Here, we assume that the simulated I-V characteristic is accurate and reliable. To obtain the drain-source resistance R_{ds}, the I-V curve is extrapolated in linear region as illustrated in Figure 3-34. The R_{ds} can be calculated the reciprocal of slope of the extrapolated line and is equal to 25 Ω. Thus, the on-resistance of a 2×100 µm GaN switch is 25 Ω.

Small-Signal Equivalent Circuit Validation

A simple series GaN switch was first simulated to validate the proposed small-signal equivalent circuit (Figure 3-35). As illustrated in Figure 3-36, simulated results agree with those from small-signal equivalent circuit for both insertion loss and isolation at 10 GHz. Furthermore, a series-shunt GaN switch was simulated and compared to the small-signal equivalent circuit. The simulation setup and results are presented in

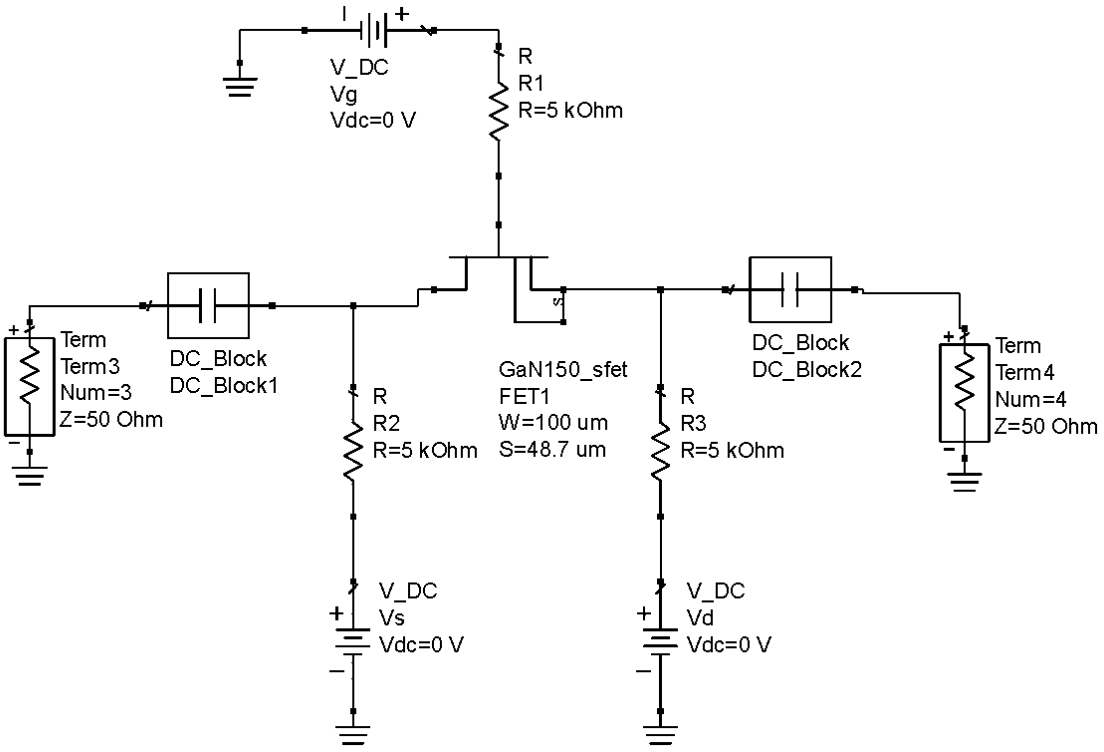

Figure 3-35: Single series GaN Switch simulation setup

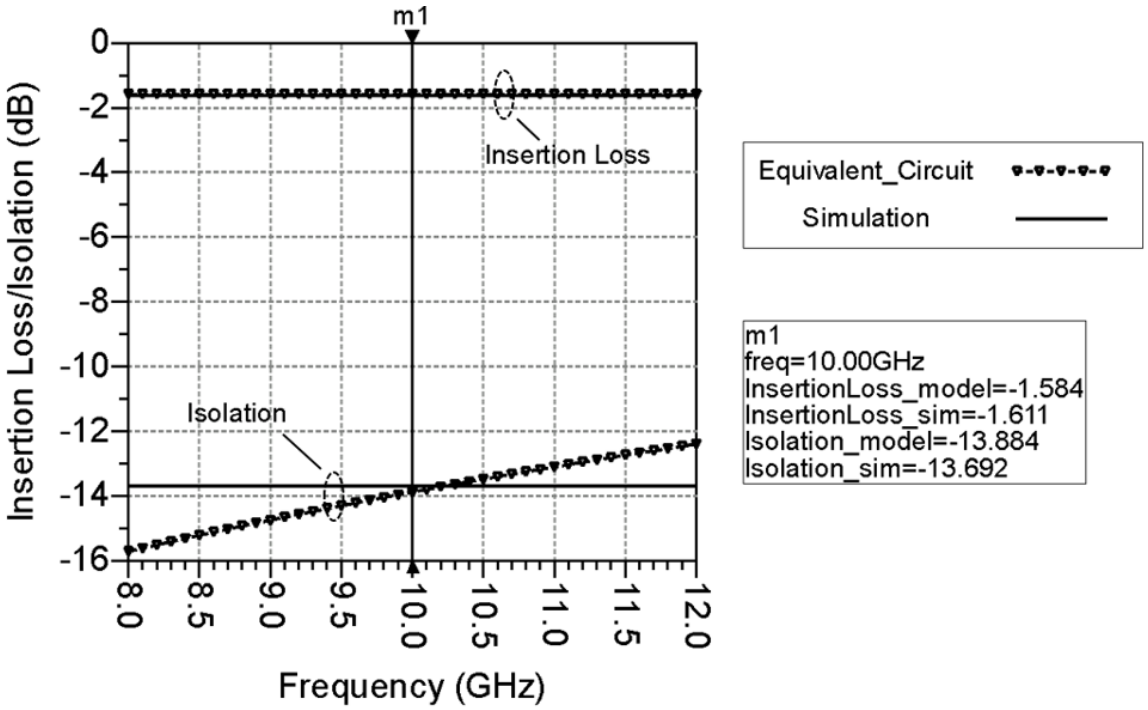

Figure 3-36: Insertion loss and isolation comparison for single series GaN switch

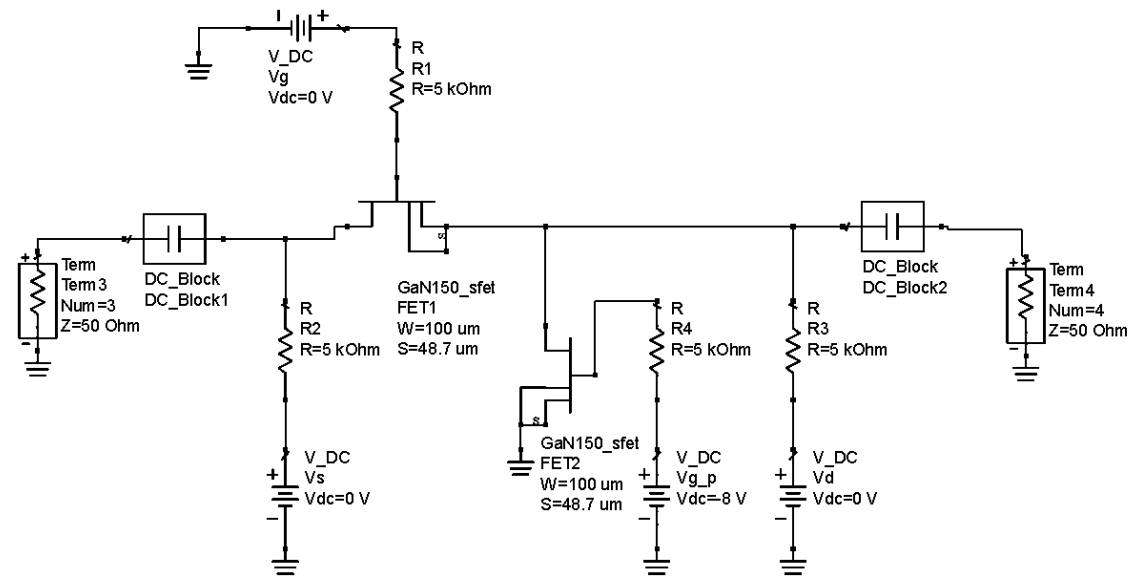

Figure 3-37: Series-shunt GaN switch simulation setup

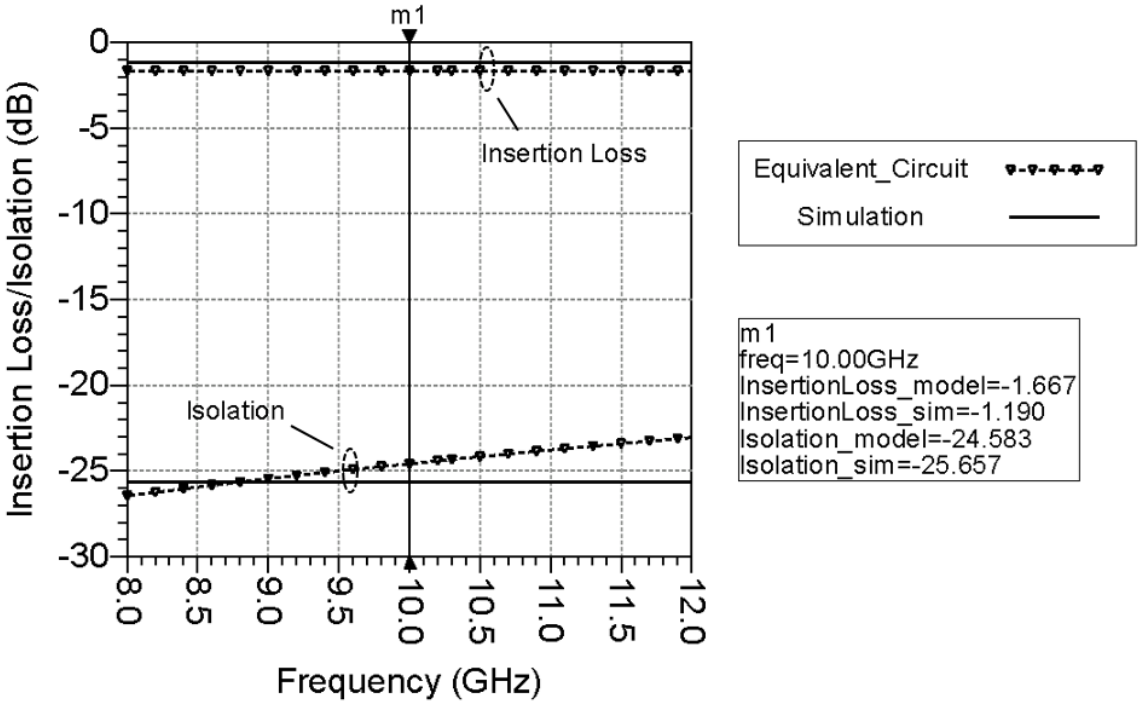

Figure 3-38: Insertion loss and isolation comparison for series-shunt GaN switch

Figure 3-37 and Figure 3-38, respectively. At 10 GHz, the modeled isolation is 1.1 dB worse than the simulated isolation and the modeled insertion loss is 0.5 dB worse than the simulated insertion loss. It is demonstrated that the GaN ADS model strongly agrees with the small-signal model extracted from measurement.

3.5.3 Large-Signal Third-Order Intermodulation Measurement Results

The large-signal TOI measurement was performed to validate the GaN process ADS model. Instrument setup and de-embedding results for the large-signal TOI measurement are shown in Table 3-1 and Table 3-2, respectively.

Table 3-1: instrument setup for the large-signal TOI measurement

Signal Generator 1 & 2		Spectrum Analyzer		Power Supply	
Center Frequency	10 GHz (SG1); 9.99 GHz (SG2)	Center Frequency	10 GHz	Output 1 (Vg)	-8 V to 0 V (0.5-V step)
Output Power	-20 dBm to 10 dBm (5-dB step)	Span	60 MHz	Output 2 (Vd)	10 V to 20 V (5-V step)
		Resolution Bandwidth	30 Hz		

Table 3-2: De-embedding results for the large-signal TOI measurement

Insertion Loss @ 10 GHz(Large-Signal)		Insertion Loss @ 10 GHz(Small-Signal)	
Cable 1	0.33 dB	"Thru" Bullet	1.5 dB
Cable 2	0.33 dB	Cable for VNA	1 dB
Cable 3	0.33 dB	Bias Tee + 1 Probe	4.45 dB
Power Splitter	5 dB		

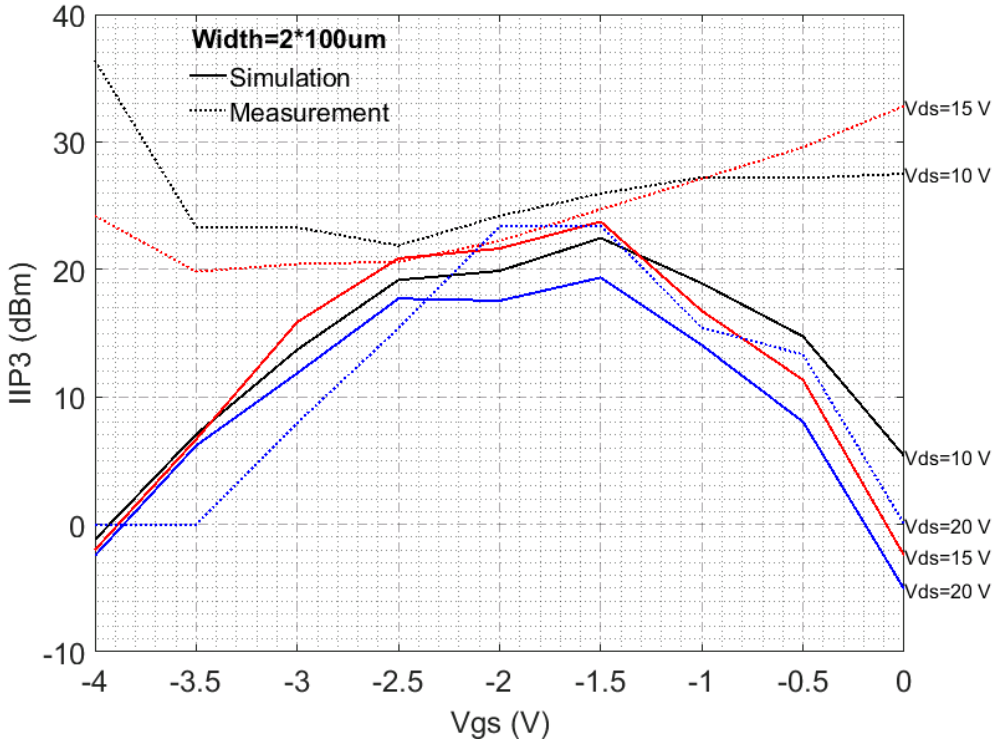

Figure 3-39: The large-signal TOI measurement results for the 2 × 100 µm GaN HEMT

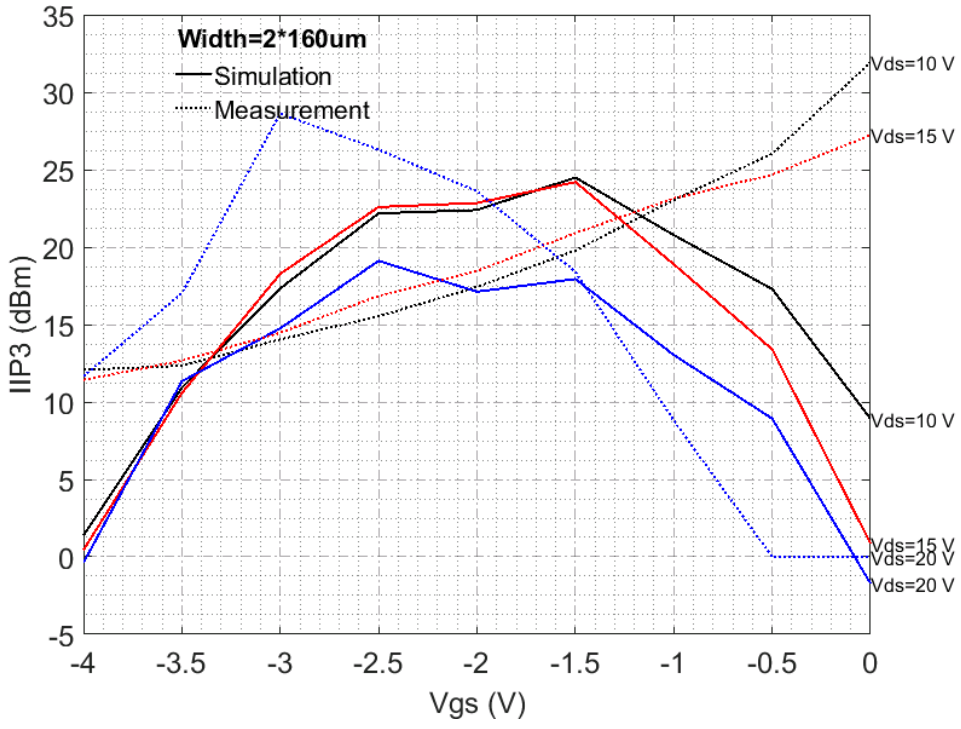

Figure 3-40: The large-signal TOI measurement results for the 2 × 160 µm GaN HEMT

Figure 3-41: The large-signal TOI measurement results for the 2 × 200 µm GaN HEMT

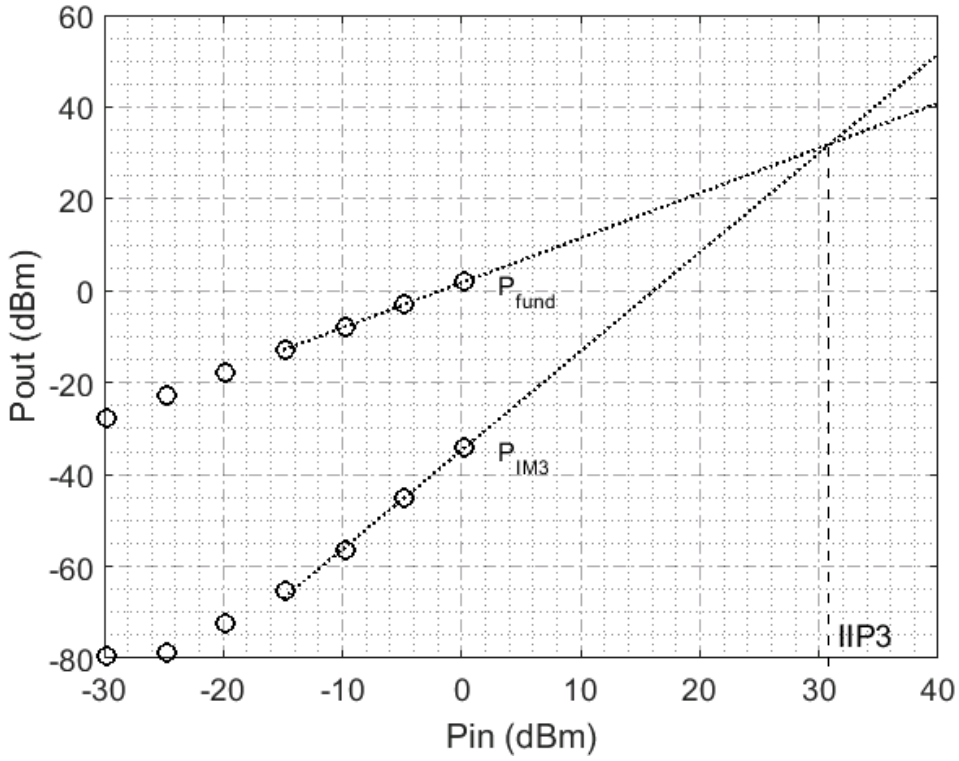

Figure 3-42: Example for IIP3 extrapolation

The IIP3 points for varied-size GaN HEMTs are plotted as a function of gate-source voltage in Figure 3-39, Figure 3-40 and Figure 3-41. As shown, simulation agrees with measurement in a gate-source voltage range of -3 V to -1.5 V. In another word, the GaN ADS model for high power works well in this range. In [29], it is stated that accurate predictions of the ac characteristic can be given around the recommended bias point (V_{GS} = -3 V and V_{DS} = 20 V). The GaN ADS model becomes less accurate when the gate-source bias voltage is lower than threshold voltage. Figure 3-42 gives an example of how the IIP3 point was extracted. It is shown that the third-order intermodulation power was only extrapolated at high input power since the third-order intermodulation power is dominated by noise floor of the spectrum analyzer at low input power.

3.6 Conclusion

This chapter presented dc, small-signal s-parameter measurement and large-signal third-order intermodulation measurement of the common-source GaN HEMTs fabricated in varied sizes. An overview of the DUT was first given. The setup of three measurements was then illustrated. Measurement results were also presented and analyzed. Large discrepancy found in dc measurement was analyzed. Overall, the GaN ADS model can provide accurate predictions for both dc and ac characteristics despite some limitations exist.

Chapter 4 RF switch design

4.1 Literature Review

The RF SPDT switch has always been an indispensable component in the modern wireless communication system due to its nature properties. Although SPDT switches implemented using various semiconductor technologies have been developed, GaN SPDT switch at X-band will be mainly discussed here due to the research field of this work. In [40], Charles F. Campbell et al. from TriQuint Semiconductor designed a reflective SPDT switch MMIC using GaN on SiC technology for a frequency range of DC-12 GHz. The power handling and power dissipation for the SPDT switch were explored in terms of frequency, gate bias voltage and transistor size for optimization. The SPDT switch employed the series-shunt topology. In [41], Bob Y. Ma et al. developed a GaN SPDT switch MMIC based on the shunt topology for Ku-band applications. Topology, transistor size, drain-source spacing and $\lambda/4$ transmission line were determined in terms of insertion loss and isolation. In [42], a GaN single-chip transceiver frontend MMIC for X-band applications was designed by Satoshi Masuda et al. The SPDT switch in the GaN frontend MMIC employed a series-shunt topology with a quarter-wavelength transmission line and aimed to minimize the noise figure for the receiver and power loss for the transmitter. In [43], Bernd Bunz et al. from Germany designed two broadband GaN switch MMICs using UMS GH25-10 GaN technology. Two types of topologies were applied: the series-shunt-shunt topology and the shunt-shunt topology. Both switches have an additional voltage pad to shift switch voltage level to avoid an additional negative voltage in the TRM. Besides small-signal characterization, large-

signal characterization was further performed to illustrate performance limitations of the switches. In [44], M. Hangai et al. designed a GaN HEMT MMIC SPDT switch for X-band based on a band-pass/low-pass configuration. The SPDT switch serves as a band-pass filter at Tx-mode and a low-pass filter at Rx-mode. This band-pass/low-pass configuration gave a solution to the trade-off between power and loss performances. There are two main methods to improve the power handling of switches: Stacked transistor technique and resonant circuit technique [45]. In [46], K. Hettak et al. designed a GaN SPDT switch MMIC based on series-shunt topology. The SPDT switch employed the stacked transistor method to improve the power handling. A resonance inductor was placed in parallel with the series HEMTs to further improve the isolation. In [47], I. Ju et al. proposed an asymmetric SPDT Tx/Rx switch for X-band based on SiGe BiCMOS technology. The asymmetric switch, co-designed with a Low Noise Amplifier (LNA), behaves as both a lumped-element matching network and a noise matching network in the receive mode. In [48], G. Tsai et al. designed a three-stub filter embedded SPDT switch using packaged PIN diode. A novel resonator structure was used to absorb the high parasitic inductance. In addition to existing literature X-band SPDT switch designs, the SPDT switch proposed in this work will also be compared to currently available commercial X-band SPDT switches.

4.2 Single-Pole Single-Throw (SPST) Switch Design

The SPST switch is the fundamental circuit in switch design. Various multi-pole multi-throw switches can be constructed based on SPST switch. There are numerous topologies that can be used to implement SPST switch. Compared to shunt-only topology, series-only topology has worse insertion loss but better isolation. To demonstrate the statement,

a single-series switch was designed and the simulation setup is shown in Figure 4-1. The control voltage (-5 V for off state; 0V for on state) is applied to gate of the transistor through an isolation resistor of 5 kΩ. Two ideal dc blocks are used to demonstrate the performance and will be replaced by MIM capacitors in further implementation. A shunt resistor of 10 kΩ is placed at source of the transistor to provide a return path for the dc current. The insertion loss and isolation of the series switch are presented in Figure 4-2. An insertion loss of -1.53 dB and an isolation of -17.6 dB were achieved. In addition, Figure 4-3 shows the simulation setup of a single-shunt switch.

As shown in Figure 4-4, the single-shunt switch exhibits an insertion loss of 0 dB and an isolation of -7.47 dB. The simulation results demonstrate that either single-series switch or single-shunt switch cannot achieve good insertion loss and isolation at the same time. To achieve both good insertion loss and isolation, the series-shunt topology was selected. Figure 4-5 shows the simulation setup. The bias network was similar to the one in previous two simulations. Figure 4-6 presents insertion loss and isolation of the series-shunt switch. An insertion loss of -1.28 dB and an isolation of -29.37 dB were achieved. Compared to the series-only and shunt-only topologies, the series-shunt topology has a fairly good insertion loss but a much better isolation. Thus, the series-shunt topology was selected to further construct the SPDT switch.

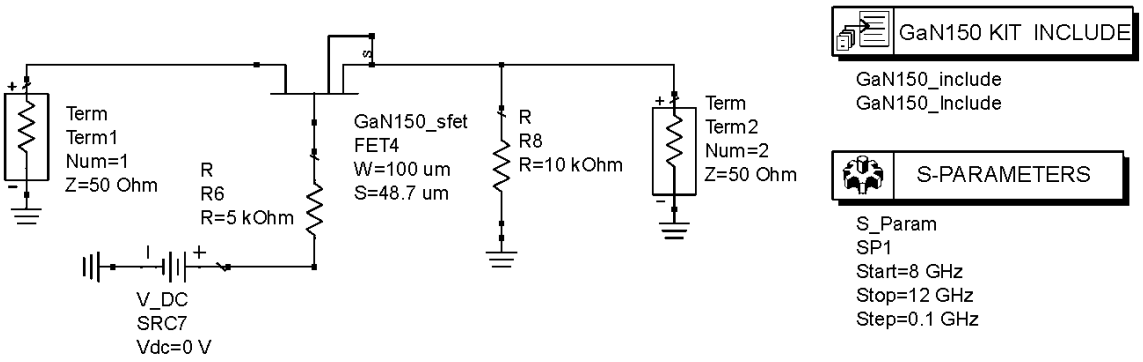

Figure 4-1: Single-series switch s-parameter simulation setup

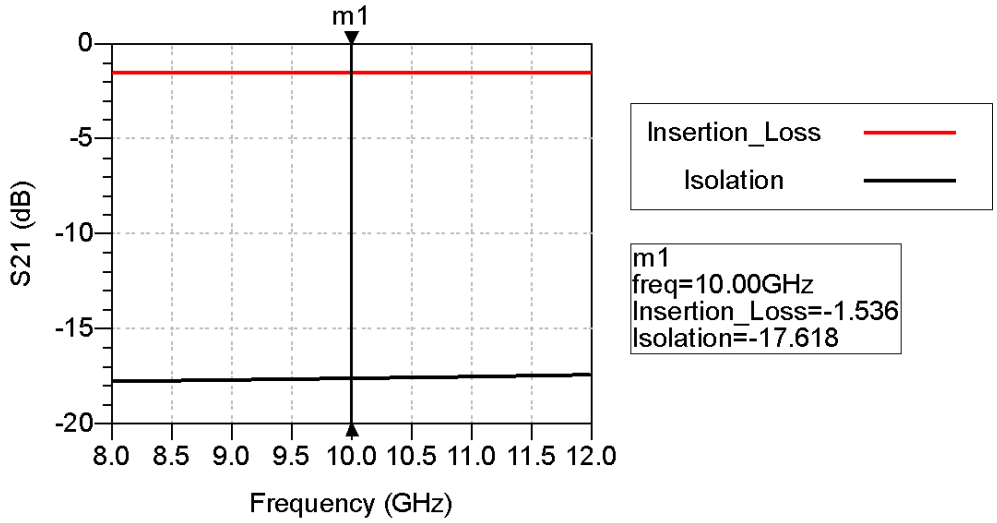

Figure 4-2: S_{21} of the single-series switch

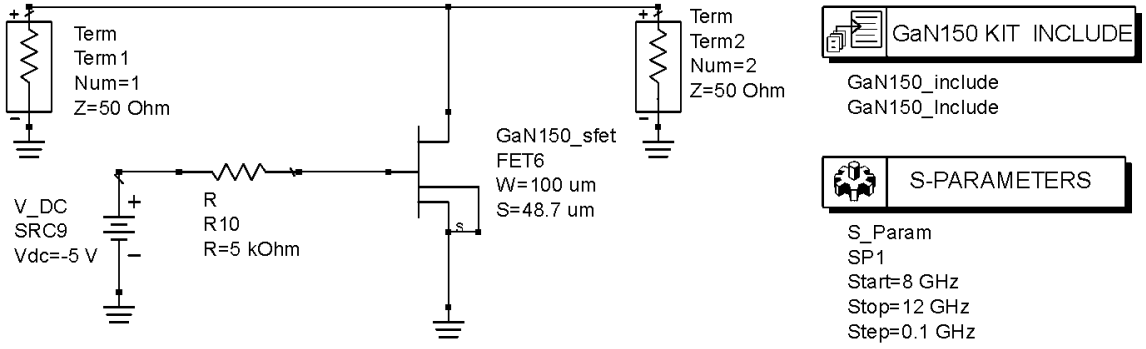

Figure 4-3: Single-shunt switch s-parameter simulation setup

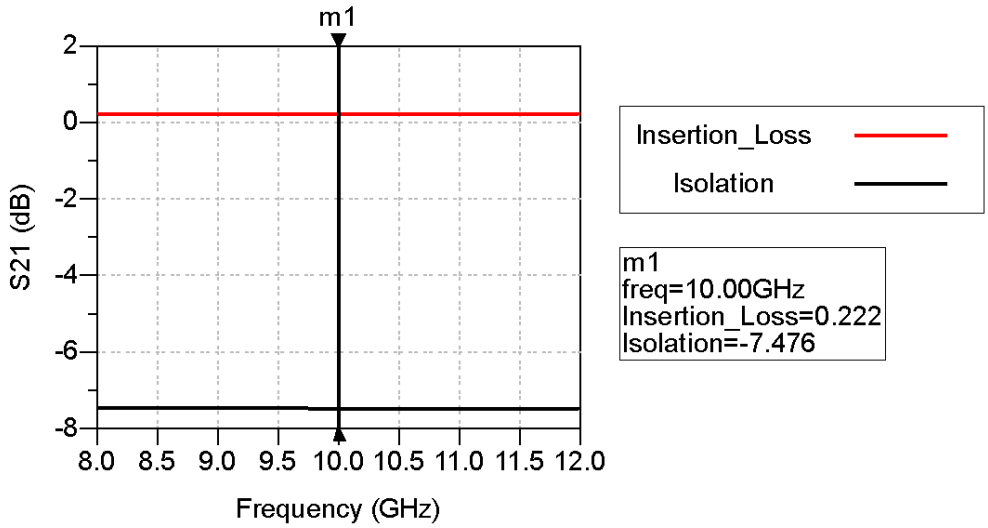

Figure 4-4: S_{21} of the single-shunt switch

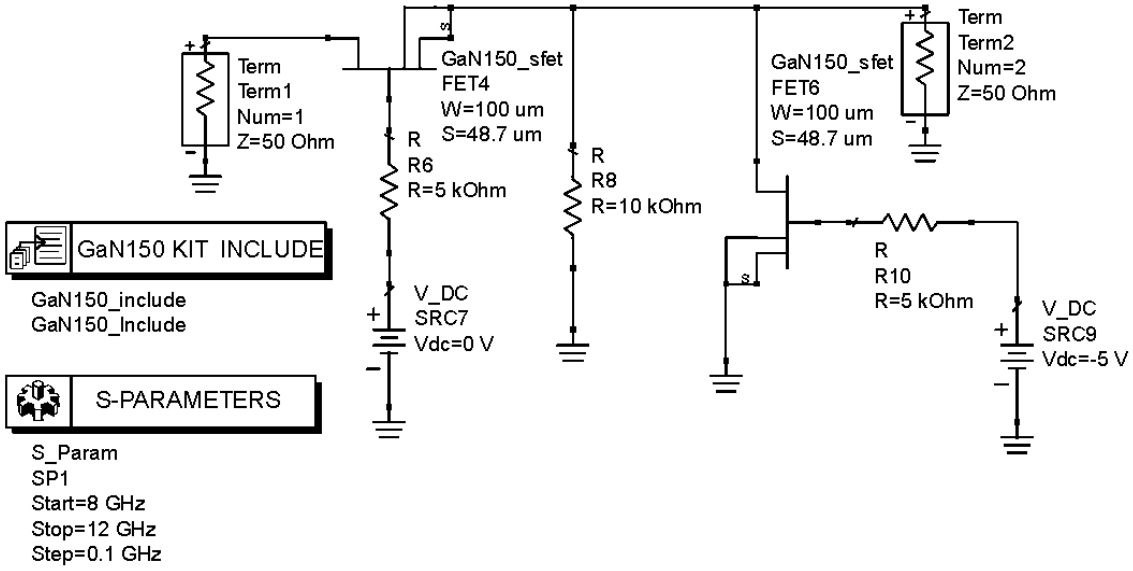

Figure 4-5: Series-shunt switch s-parameter simulation setup

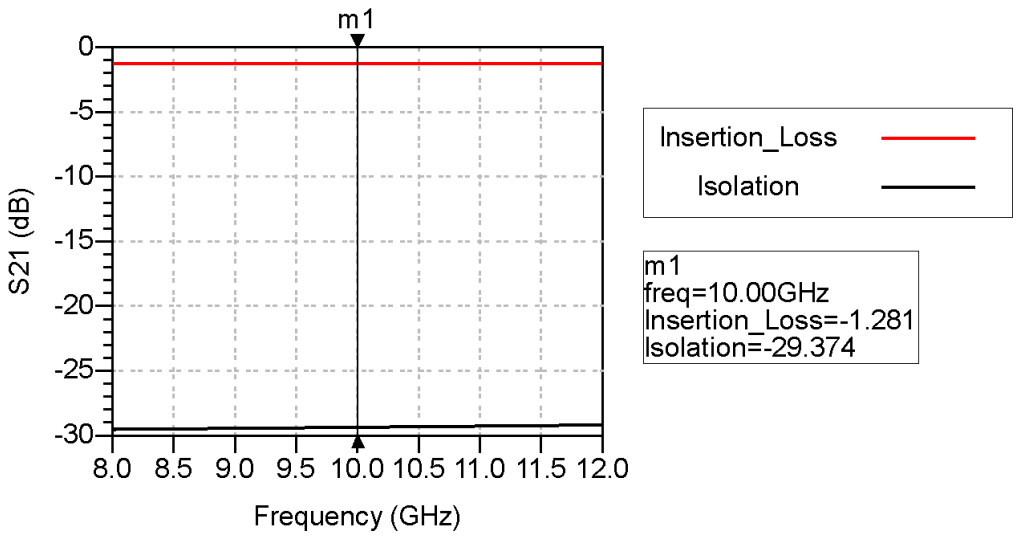

Figure 4-6: S_{21} of the series-shunt switch

4.3 SPDT Switch Design

4.3.1 Types of SPDT Switches

As shown in Figure 4-7, there are two types of switches: reflective and absorptive switches. In reflective SPDT switches, the isolated port is open and not connected to any termination. Reflective SPDT switches have low insertion loss with respect to absorptive switches, however, they introduce significant reflections between components [2]. In absorptive SPDT switches, the isolated port is terminated in 50 Ω. In many applications, absorptive SPDT switches are preferred. In this work, the absorptive SPDT switch was selected.

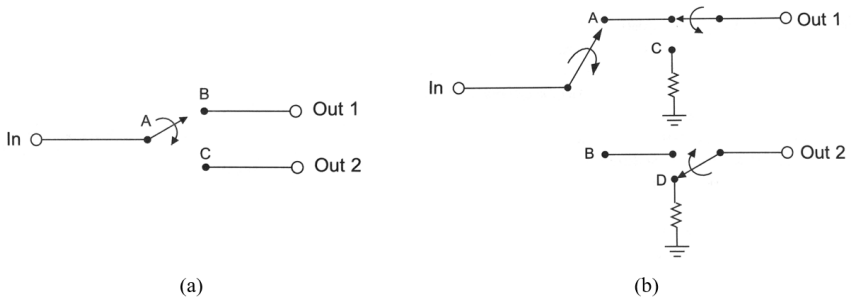

Figure 4-7: Types of SPDT switches: (a) reflective switch (b) absorptive switch

4.3.2 Basic Theory of Switches

Insertion Loss and Isolation

For a series-shunt configuration switch, the insertion loss and isolation can be expressed as [2]

$$IL = \left| \frac{1}{2} + \frac{(Z_0 + Z_h)(Z_0 + Z_l)}{2Z_0 Z_h} \right|^2 \quad \text{Eq. 4-1}$$

$$Isolation = \left| \frac{1}{2} + \frac{(Z_0 + Z_l)(Z_0 + Z_h)}{2Z_0 Z_l} \right|^2 \quad \text{Eq. 4-2}$$

where Z_h is the device off-state impedance and Z_l is the device on-state impedance.

Maximum Power Handling

The maximum power handling of a switch is dominated by the maximum voltage limit in the off state and the maximum current limit in the on state [2]. When the switch is in the off state, the maximum allowable drain voltage and the corresponding gate bias voltage can be calculated as [2]

$$V_{max} = V_b - V_p \quad \text{Eq. 4-3}$$

$$V_g = \frac{V_b + V_p}{2} \quad \text{Eq. 4-4}$$

where V_b is the gate-drain breakdown voltage and V_p is the pinch-off voltage. The maximum power handling can be calculated as [2]

$$P_{max} = \frac{V_{max}^2}{2Z_0} \quad \text{Eq. 4-5}$$

where Z_0 is the system characteristic impedance. When the switch is in the on state, the maximum power handling can be calculated as

$$P_{max} = \frac{1}{2} I_{dss}^2 Z_0 \quad \text{Eq. 4-6}$$

where I_{dss} is the maximum drain-source current.

Third-Order Intercept Point

The IP3 point of a series switch can be generally expressed as [49]

$$IP3 = \frac{Z_0}{2R_S^3 \alpha_3}\left(1 + \frac{2Z_0}{R_S}\right) \quad \text{Eq. 4-7}$$

where Z_0, R_S are system characteristic impedance and the device on-state resistance. The α_3 is the third-order term determined from the I-V characteristics. The nonlinear I-V characteristic can be written as [49]

$$I_{DS} = \sum_{n=1}^{\infty} \alpha_n V_{DS}^n \quad \text{Eq. 4-8}$$

where α_n are the nonlinear coefficients as a function of the gate bias circuitry and the on-state resistance R_S.

4.3.3 Large-Signal Design Considerations

In many applications, SPDT switches are preferred to offer high power handling. To obtain a highly-linear SPDT switch design, effects of all circuit components on the IP3 points were explored. The proposed SPDT switch and the simulation setup are shown in Figure 4-8. The path on the left hand (Input port to Output port) is the transmitted path while the path on the right hand (Term port to Output port) is the isolated path. A series resistor is inserted between the shunt switch and ground to make the SPDT switch absorptive. Note that all simulations were performed at an input power of -45 dBm.

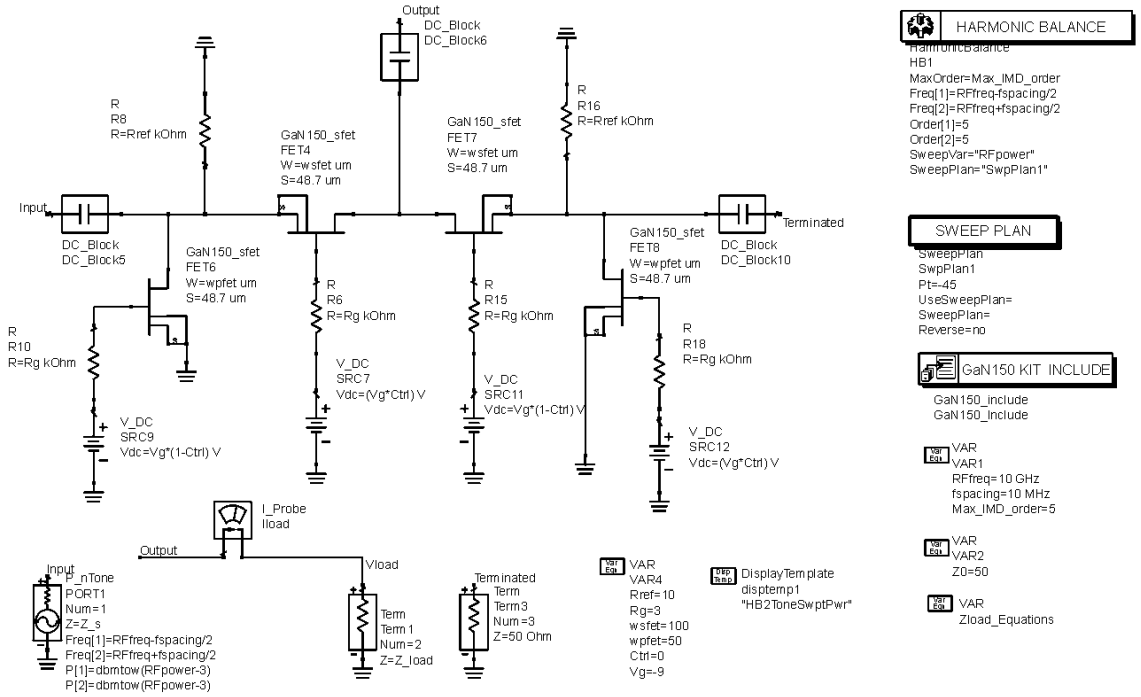

Figure 4-8: The large-signal simulation setup of the proposed SPDT switch

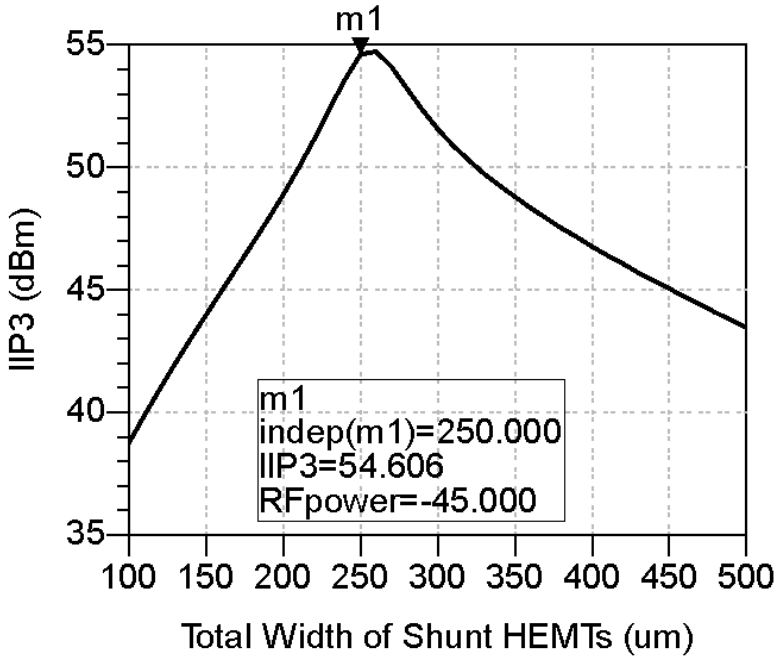

Figure 4-9: The IIP3 point vs width of series HEMTs

Transistor Size

As mentioned in the previous chapter, the on-state resistance and off-state capacitance of switches are determined by transistor sizes. Since the SPDT switch has two paths, the power handling of SPDT switch depends not only on series transistor in the transmitted path (series-on transistor) but also on series transistors in the isolated path (series-off transistor). The width of two series transistors was both swept at the same time. As shown in Figure 4-9, a maximum IIP3 point of 54.6 dBm is achieved at a transistor width of 250 µm. Furthermore, width of the series transistors in two paths was swept individually. As shown in Figure 4-10, the red line denotes the series-off transistor while the black line denotes the series-on transistor. The IIP3 point increases as width of the series-on transistor increases and the IIP3 point remains nearly constant after a width of 300 µm is achieved. It is explained that power handling of a series transistor in the on state is dominated by the maximum drain-source current which is proportional to transistor size.

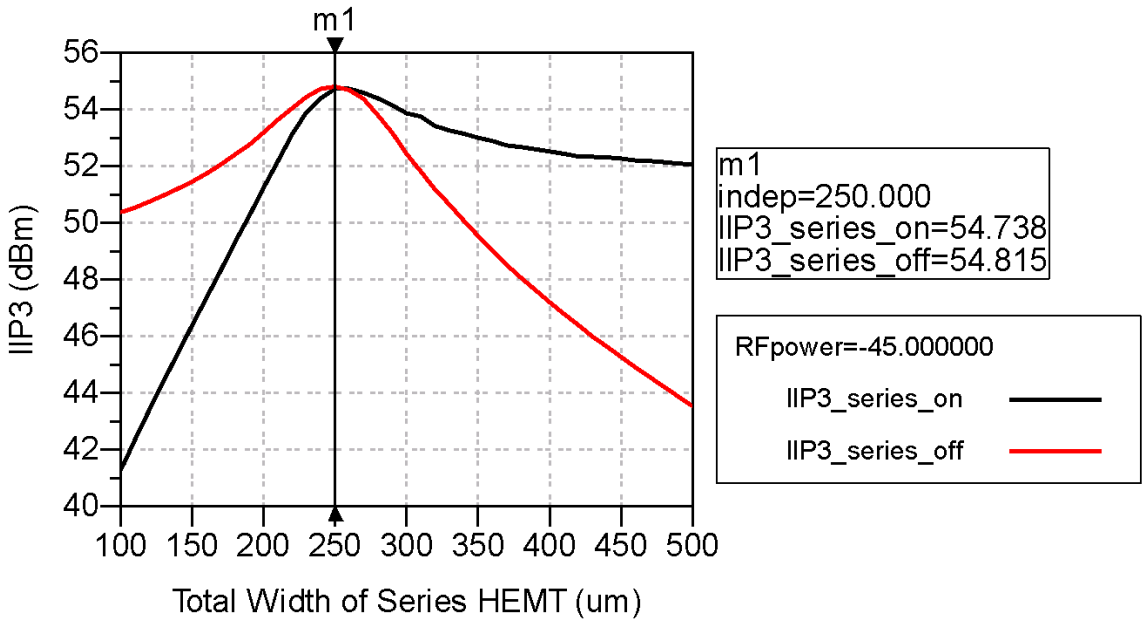

Figure 4-10: IIP3 point vs width of series HEMT (separated)

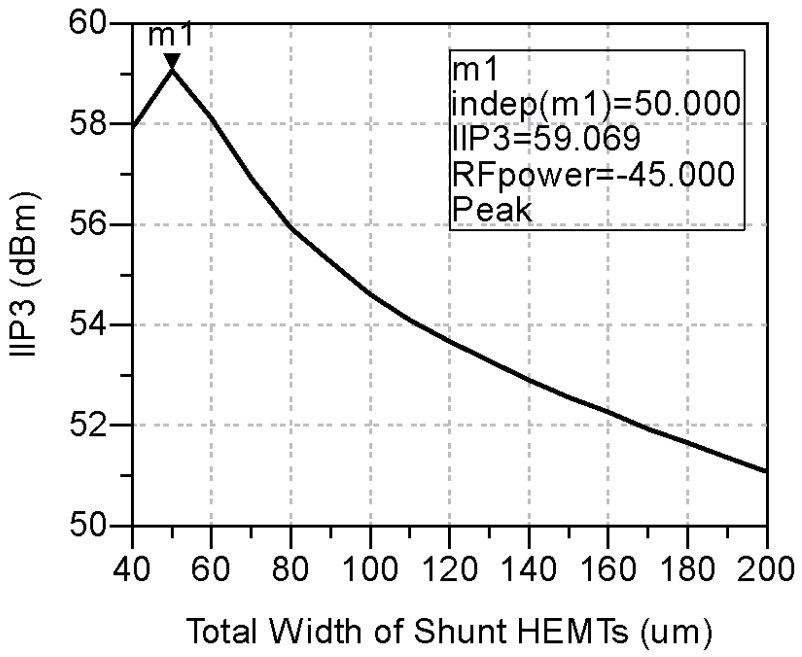

Figure 4-11: IIP3 point vs width of shunt-off HEMT

As for the series-off transistor, the IIP3 point slightly increases before the series-off transistor reached a total width of 50 µm and then decreases dramatically after the maximum point. The transistor width determines the off-capacitance which affects the ratio of RF swing appears at the gate of transistor. The series-off transistor can possibly be turned on if the RF swing at gate is large enough. Thus, a total width of 250 µm for both series-on and -off transistors was selected. In addition, width of the shunt HEMTs in the transmitted path was swept. Similar behavior of the IIP3 point is shown in Figure 4-11. A total width of 50 µm for the shunt HEMTs was then selected.

Gate Isolation Resistance

The gate bias voltage is applied to gate of transistors through the gate isolation resistor. The selection of gate isolation resistor is crucial due to its impact on frequency of operation and power handling capability [2]. The gate isolation resistance was swept and

Figure 4-12 shows that the gate isolation resistance has a significant impact on IIP3 point. An optimal IIP3 of 62 dBm can be achieved at a gate isolation resistance of 3 kΩ.

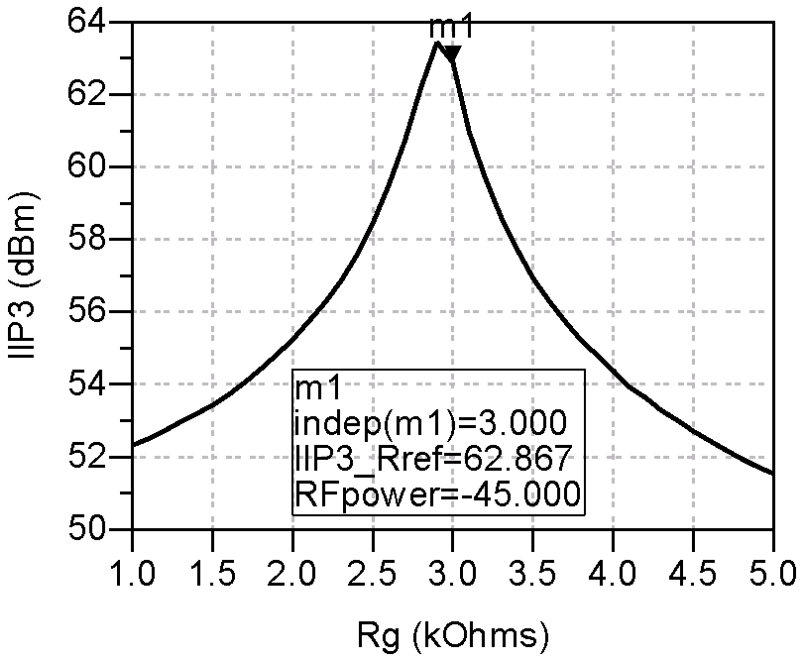

Figure 4-12: The IIP3 point vs gate isolation resistance

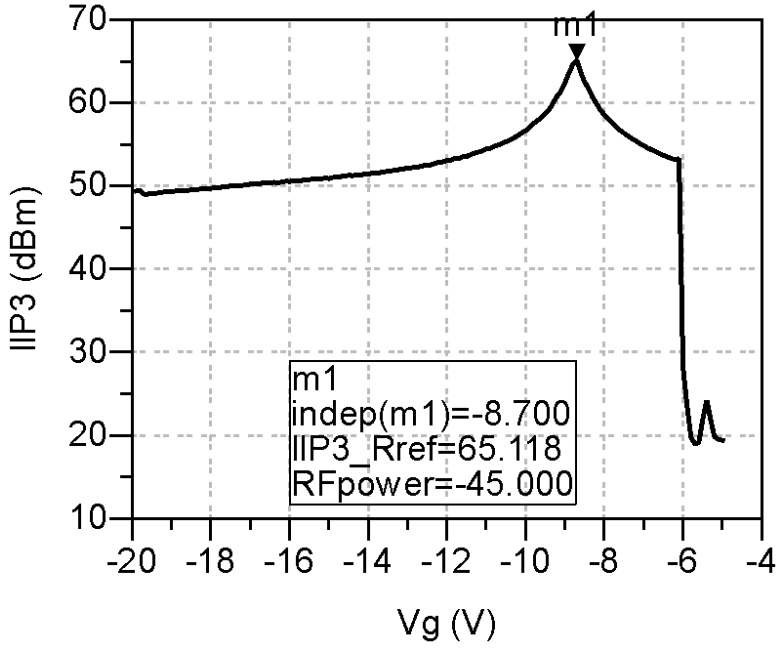

Figure 4-13: The IIP3 point vs gate control voltage

Gate Bias Voltage

As mentioned above, gate bias voltage determines the power handling of switches. Both intrinsic resistances and capacitances vary as a function of gate bias voltage. These intrinsic resistances and capacitances determines the RF voltage swing at the gate. The gate bias voltage was swept. As shown in Figure 4-13, an optimal IIP3 point of 65 dBm is achieved at a gate bias voltage at -8.7 V. A gate bias voltage of -9 V was eventually selected.

4.3.4 Simulation Results

Figure 4-14 shows a full schematic of the proposed SPDT switch which is symmetric and has two identical paths. Each path consists of a series HEMT, a reference isolation resistor, a transmission line, three shunt HEMTs, a shunt source resistor and a block capacitor. All the component values for the proposed SPDT switch are listed in Table 4-1. The small-signal and large-signal simulation results at schematic level are presented in Figure 4-15 and Figure 4-16. The return loss at all three ports are around -12 dB. The insertion loss is -0.3 dB and the isolation is -25.3 dB. The IIP3 point is approximately 40.5 dBm. Figure 4-17 shows layout details for the proposed SPDT switch. The “Port 1” denotes the common-port while the “Port 2” and “Port 3” denote the two input/output ports. The “Vc” and “VcB” denote the complimentary gate bias voltages: -9 V and 0 V. The proposed SPDT switch occupies an area size of 794 μm × 1108 μm. The EM Co-Simulation was finally performed to account for parasitic effects including coupling and metal loss. The EM Co-Simulation results are presented in Figure 4-18 and Figure 4-19. The EM insertion loss and isolation are -0.65 dB and -24.8 dB, respectively. The return

loss S_{11}, S_{22} and S_{33} are low than -10 dB through a frequency range of 8-12 GHz. An IIP3 point of 41 dBm was achieved in the EM Co-Simulation.

Table 4-1: Design values for components in the proposed SPDT switch

Series HEMT Size	125 µm
Shunt HEMT Size	25 µm
Transmission Line Length	630 µm
Transmission Line Width	15 µm
Shunt Source Resistor	200 Ω
Reference Isolation Resistor	5 kΩ
Gate Isolation Resistor	3 kΩ
Block Capacitor	1.69 pF
Gate Bias Voltage	-9 V (OFF); 0 V (ON)

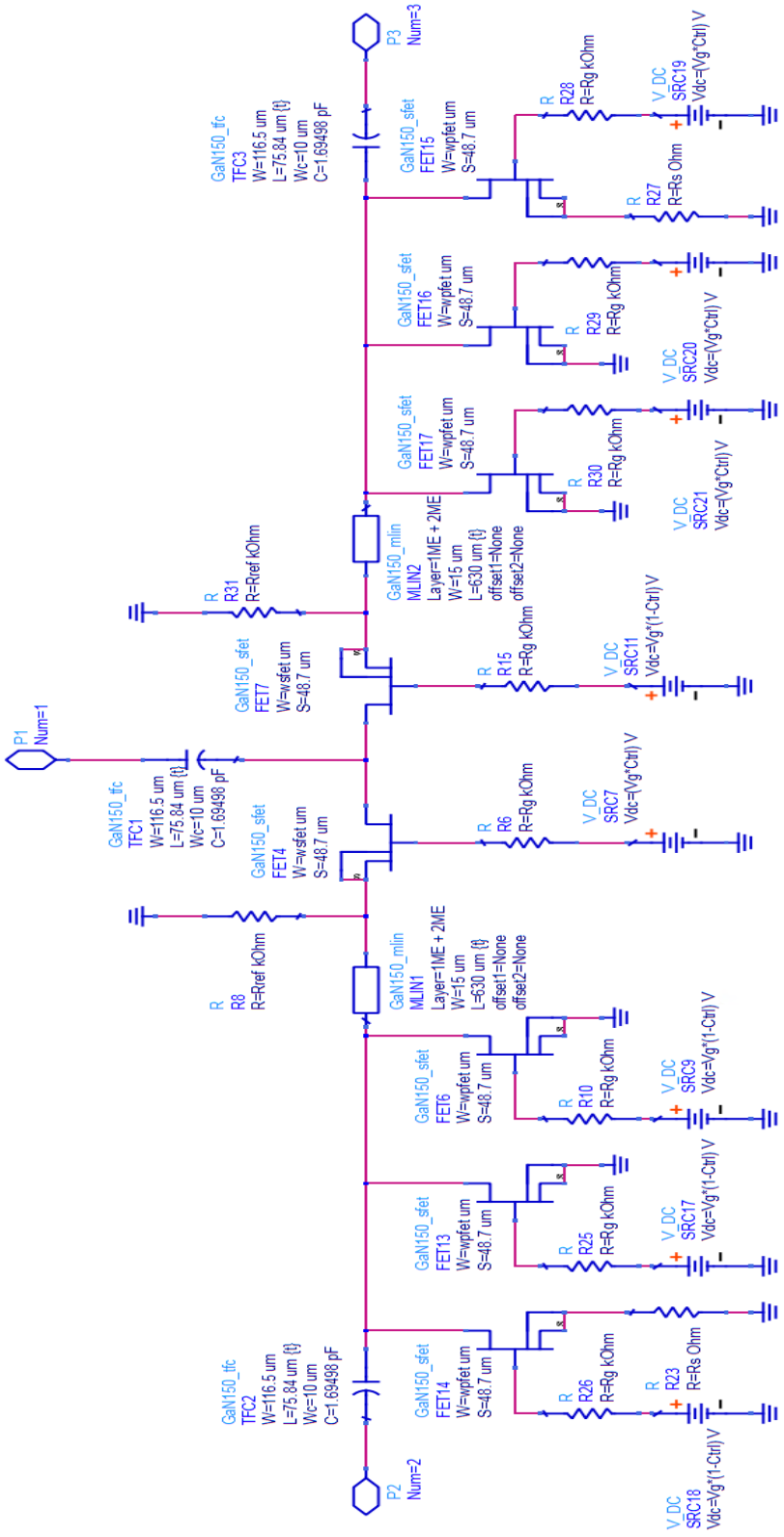

Figure 4-14: The proposed SPDT switch schematic

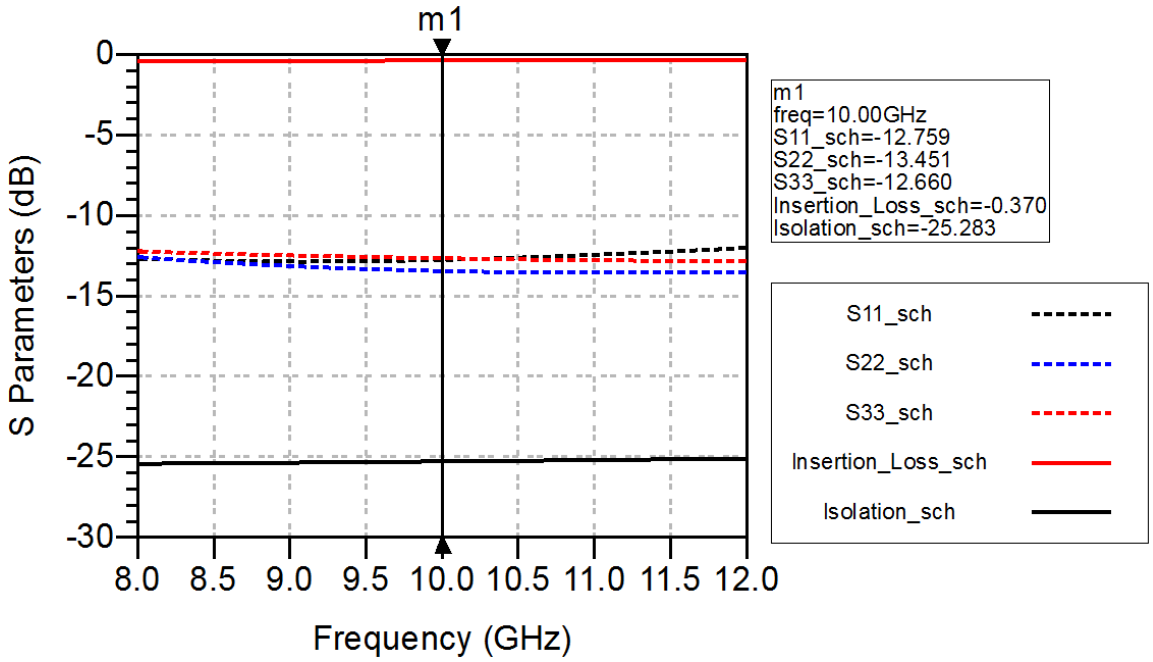

Figure 4-15: S-parameters for the proposed SPDT switch (schematic)

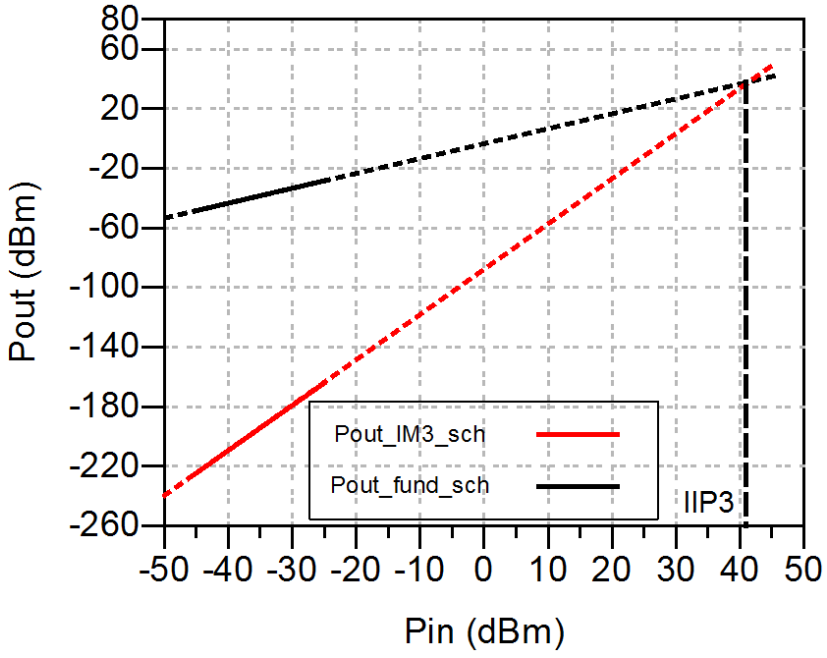

Figure 4-16: The IIP3 point for the proposed SPDT switch (schematic)

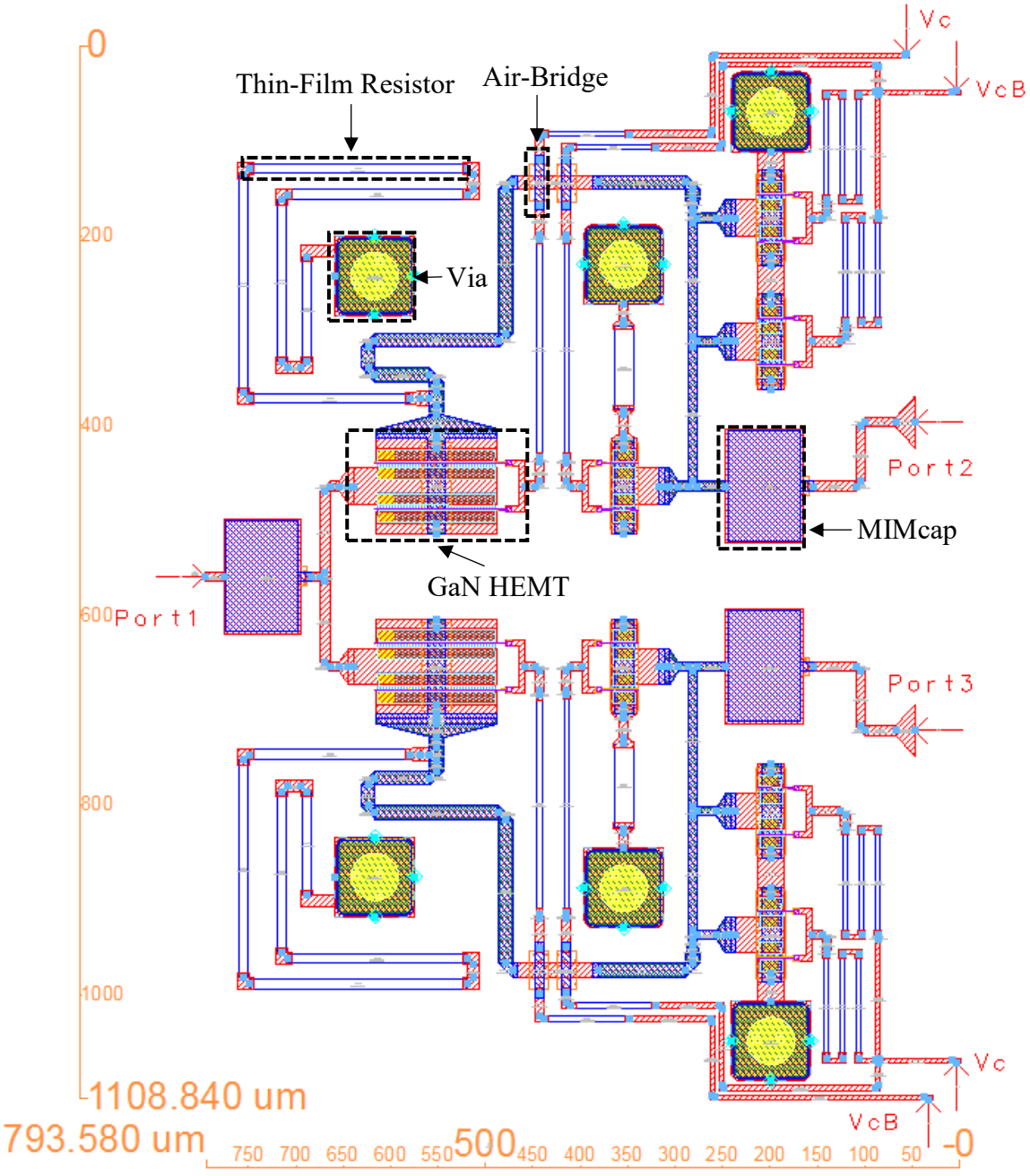

Figure 4-17: The proposed SPDT switch layout

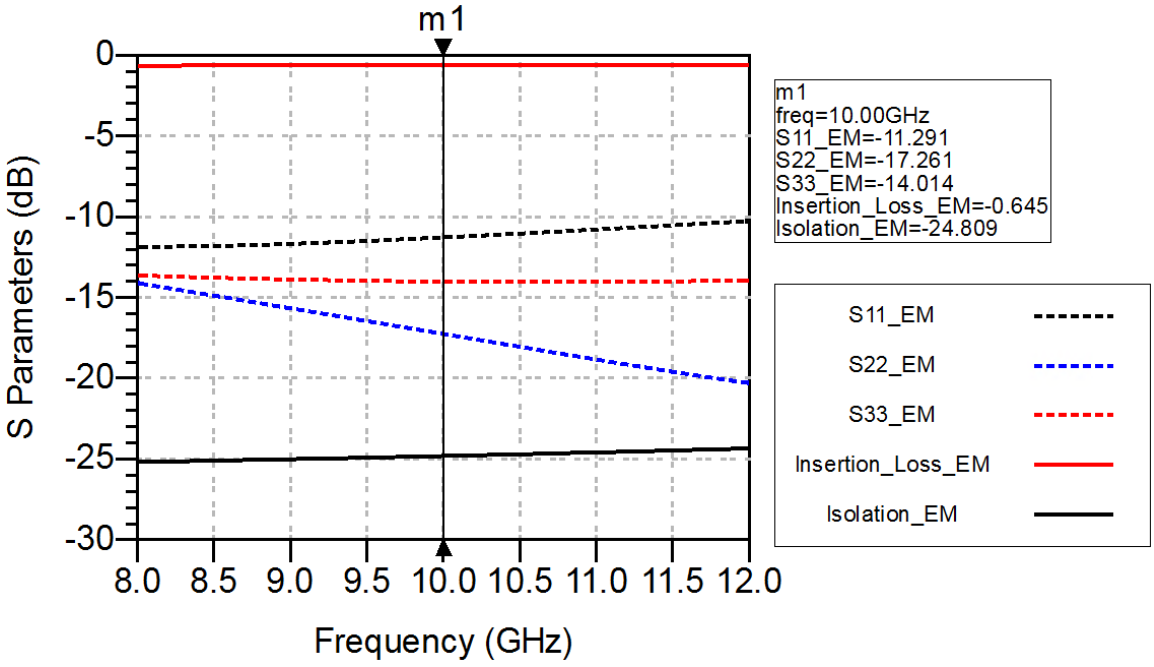

Figure 4-18: S-parameters for the proposed SPDT switch (EM co-simulation)

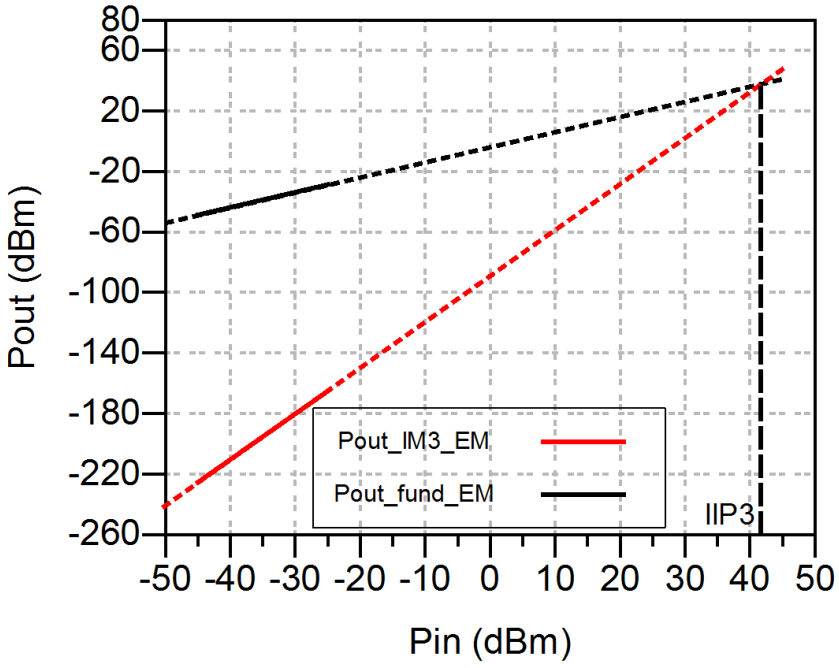

Figure 4-19: The IIP3 point for the proposed SPDT switch (EM co-simulation)

Table 4-2: SPDT Switch Performance Comparison

Ref.	Technology	Frequency (GHz)	Topology	IL (dB)	Isolation (dB)	P_{1dB}/IIP3 (dBm)	Size area (mm^2)
[40]	TriQuint GaN	DC-12	Series-Shunt	1	30	41.76/-	1.15 × 1.66
[41]	GaN	15-20	Shunt	1.4	35	36/54	-
[42]	0.25-µm GaN	DC-12	Series-Shunt	1.2	30	39.2/-	1.8 × 2.4
[43]-1	UMS GH25-10 GaN	5-18	Series-Shunt	1.3	21	43/-	3.25 × 2.4
[43]-2	UMS GH25-10 GaN	5-18	Series-Shunt	1.4	27	41.7/-	3.25 × 2.4
[44]	GaN	7-13	Band-pass/low-pass	1.2	39	43/-	2.8 × 1.7
[46]	Coplanar GaN	8-12	Stacked-shunt	1.6	20	38/-	-
[47]	0.13-µm SiGe BiCMOS	8-12	SPDT-LNA	1.1	26	26.9/-	0.5
1*	GaAs	DC-12	-	1.9	40	-/42	3 × 3 (Package)
2*	Qorvo VPIN	4-20	-	0.9	35	24/-	2.24 × 1.63
This work**	GaN	8-12	Series-Shunt	0.65	24.8	-/41	0.79 × 1.1

1*: Analog Device HMC347ALP3E

2*: Qorvo TGS2302

** Note that performance results for this work are simulation results.

4.4 Conclusion

In this chapter, design of a compact SPDT switch with high linearity was proposed. Literature review on SPDT switch was presented first and performance of other SPDT switch designs was listed. The SPST switches were then explored in terms of small-signal performance. Basic theory of switch design was introduced. In Section 4.3.2, effects of switch circuit components on the IIP3 point were given. Taking care of these effects leads to a high-linearity SPDT switch design. The schematic simulation and EM Co-simulation results proved the design considerations given previously. A SPDT switch performance comparison with existing SPDT switch designs is listed in Table 4-2. Compared to existing SPDT switch designs, the proposed SPDT switch has achieved a lowest insertion loss and smallest area size along with high IIP3 point and comparable isolation performance.

Chapter 5 Phase Shifter Design

5.1 Literature Review

Phase shifters can be implemented by using different structures such as switched-line, loaded-line, reflection-type, high-pass/low-pass etc. Ever since the high-pass/low-pass structure has first been introduced by P. Onno and A. Pitkins 40 years ago in [50], it has always been an interesting topic for research due to its wide-band and size-saving properties. Later in 1972, R. V. Garver summarized design techniques for four types of phase shifter: switched line, reflection, loaded line, and high-pass/low-pass [51]. Theoretical design equations for each of them were elaborated. In [52], Tyler N. Ross et al. proposed a linear model for the switching GaN HEMT transistors and designed two 22.5^{o} high-power GaN phase shifters based on two different phase shifter design techniques by using the proposed linear model. The switched-filter phase shifter was designed to switch between a by-pass circuit and a low-pass filter circuit. The novel resonator-based phase shifter was designed to switch between a shunt LC resonator and a high-pass filter by using two SPDT switches. The power handling of two phase shifters was evaluated by using linear ac analysis to calculate voltages across transistors. In [53], Qi Wang et al. designed an X-band 6-bit MMIC phase shifter using 0.25μm GaAs pHEMT technology. The proposed loaded-line topology for small phase shift states (5.625^{o} and 11.25^{o}) cascaded loaded-capacitors in series of the shunt transistor instead of loaded-line. The middle (22.5^{o} and 45^{o}) and large (90^{o} and 180^{o}) phase shift states were implemented based on all-pass and high-pass/low-pass networks. Each phase shift state was optimized for a balanced trade-off in terms of insertion loss, phase error and return

loss. In [54], Hamed Alsuraisry et al. designed a 5-bit switch type phase shifter in 0.18 μm CMOS technology for X-band applications. The 180º state was implemented based on the high-pass/low-pass network while other phase shift states were based on the T-bridged topology. The 5-bit switch type phase shifter occupies a small chip size of 0.81 mm^2 with 0 mW dc power consumption. In [55], Ilker Kalyoncu et al. designed a 4-bit passive phase shifter for X-band phased arrays using 0.25-μm SiGe BiCMOS technology. The switched low-pass network was adopted for the 22.5º and 45º bits while the high-pass/low-pass network was used for the 90º and 180º bits. The high-pass/low-pass filters were implemented by using MIM capacitors and on-chip spiral inductors. Isolated NMOS transistors were used for switching functionality. In [56], Moon-Kyu Cho et al. designed an X-band 5-bit phase shifter using a commercial 0.18-μm SOI process. All bits were based on low-pass/band-pass or low-pass/high-pass filters. Both SPDT switches and DPDT switches were used to switch between low-pass/band-pass or low-pass/high-pass filters. The dc power consumption of this 5-bit phase shifter is 0-mW. In [57], Matthew A. Morton et al. designed a 5-bit digital X-band phase shifter based on hybrid topology using 0.13-μm SiGe BiCMOS technology. The hybrid pi/t bit passive topology can reduce the chip size area significantly compared to conventional all-pi or all-t structure. In contrast to another all-pi phase shifter using same SiGe BiCMOS technology, the hybrid phase shifter shows a total die-area reduction of 50% and the absolute phase error was decreased by 13º. In [58], Matthew A. Morton et al. also analyzed the error sources in silicon-based monolithic high-pass/low-pass microwave phase shifters due to device size limitations, parasitic inductor, loading effects and non-ideal switches. It was found that series resistance and self-resonance of inductors causes a shift in the location of the

local minimum in phase. Also, the match of switches plays a significant role in multiple-bit phase shifters. Besides, there are some errors arising from fabrication constraints that are difficult to deal with. In some cases, intelligent bit ordering might help this. In [59], Xinyi Tang and Koen Mouthaan proposed the theory and a design method for distributed digital phase shifters, considering both the phase-error and the return-loss bandwidth simultaneously. A transmission-line branch and a bandpass filter branch forms the proposed distributed digital phase shifter. Grounded shunt quarter-wavelength stubs are used in bandpass filter branch to align insertion phase with the transmission-line branch. A 4-bit phase shifter with SPDT switches was designed to validate the design technique.

5.2 Component Characterization

5.2.1 Unloaded and loaded Q

Quality factor Q is a key performance parameter of passive components which quantifies the loss due to parasitic effects of passive components. The quality factor Q is defined as [60]

$$Q = \omega \frac{average\ energy\ stored}{energy\ loss\ per\ second} \qquad \text{Eq. 5-1}$$

If the quality factor Q only measures the loss of passive components, it is called unloaded Q, Q_0. When an external network e.g. a load resistor is connected, external network introduces extra loss which lowers the overall quality factor. The overall quality factor is called loaded Q, Q_L. If we define an external Q as Q_e, then the loaded Q can be expressed as [60]

$$\frac{1}{Q_L} = \frac{1}{Q_e} + \frac{1}{Q_0} \qquad \text{Eq. 5-2}$$

To quantify the loss of passive component itself, unloaded Q is used. In this work, quality factor Q denotes the unloaded Q unless it is further clarified.

5.2.2 Inductors

Inductors can be realized either as on-chip spiral inductors or as series transmission lines depending on the required inductance. Figure 5-1 presents layout of a spiral inductor and the equivalent circuit of an on-chip spiral inductor. In addition to inductance, spiral inductors also have unwanted resistive loss, feedback capacitance and parasitic capacitance.

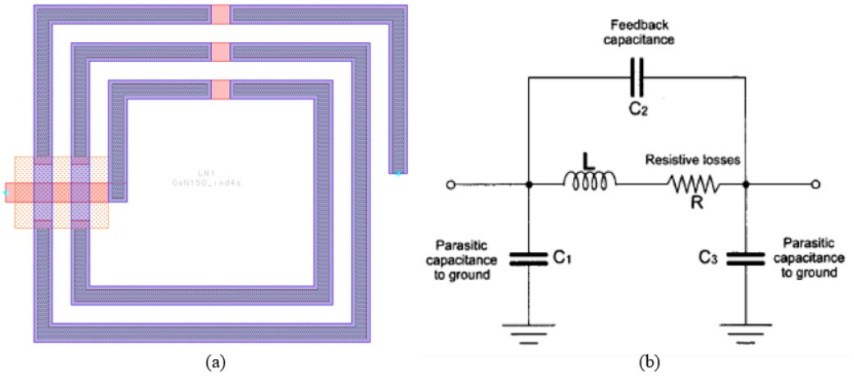

Figure 5-1: Spiral inductor illustration: (a) Layout of spiral inductor in GaN150 Process (b) Equivalent circuit of on-chip spiral inductor [1]

These parasitic capacitances lead the spiral inductor to self-resonance at a specific frequency called self-resonance frequency f_r. To ensure spiral inductors offering the required inductance, the operating frequency should be much lower than the self-resonance frequency f_r. Number of turns was swept to obtain the relationship between inductance and self-resonance frequency. As shown in Figure 5-2, the self-resonance frequency of a spiral inductor rises as number of turns decreases. The quality factor of a spiral inductor reaches the optimum at about half of the self-resonance frequency. In addition, the optimum of quality factor also increases as number of turns decreases.

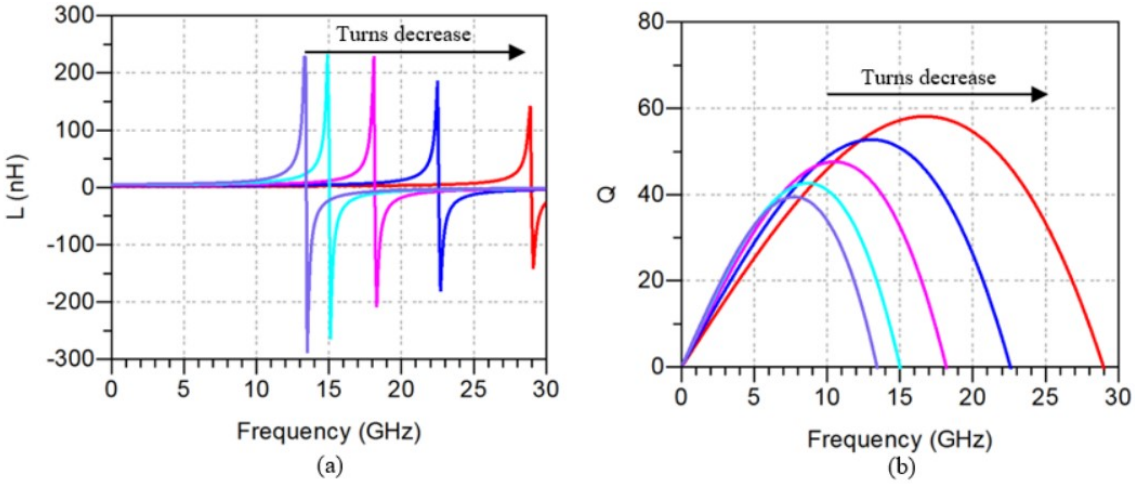

Figure 5-2: The spiral inductor performance: (a) Inductance vs frequency (b) Quality factor vs frequency

5.2.3 Capacitors

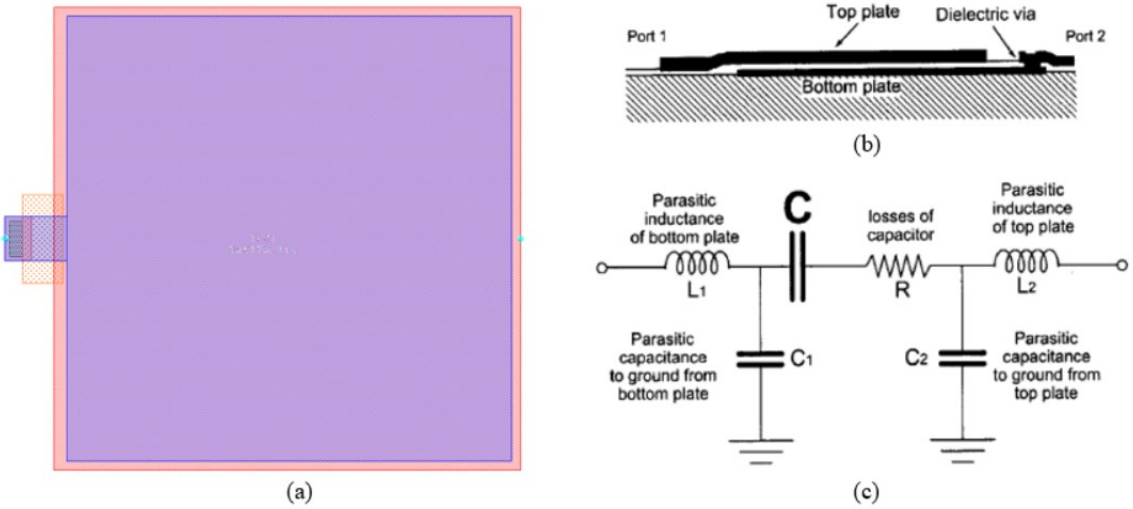

Figure 5-3: MIM capacitor illustration: (a) Layout of MIM capacitor in GaN150 process

(b) Cross-view of general MIM capacitor [1] (c) Equivalent circuit of general MIM capacitor [1]

Two types of capacitors are mostly used in MMIC design: interdigitated capacitors and overlay capacitors. Interdigitated capacitors usually give a capacitance less than 1 pF with good accuracy. Overlay capacitors are mostly realized as MIM capacitors. Figure 5-3 (a) shows layout of a MIM capacitor in GaN150 process and Figure 5-3 (b) shows the cross-view of a general MIM capacitor. Figure 5-3 (c) shows the equivalent circuit of a

general MIM capacitor. In the GaN150 process, MIM capacitors are formed by two metal layers with a thin silicon nitride layer in middle. Air-bridge is used to let the top metal cross the bottom metal. The MIM capacitor has a maximum capacitance of 122 pF which is sufficient for most of MMIC designs.

5.3 Types of Phase Shifter

The phase shifter is a two-port network that provides the desired phase shift. In a general sense, phase shifters can be classified into two types: digital phase shifters and analog phase shifters. Digital phase shifters have discrete phase shift states and can be controlled by either digital or analog control. Analog phase shifters offer a continuous value of phase shift in a range of 0°-360°.

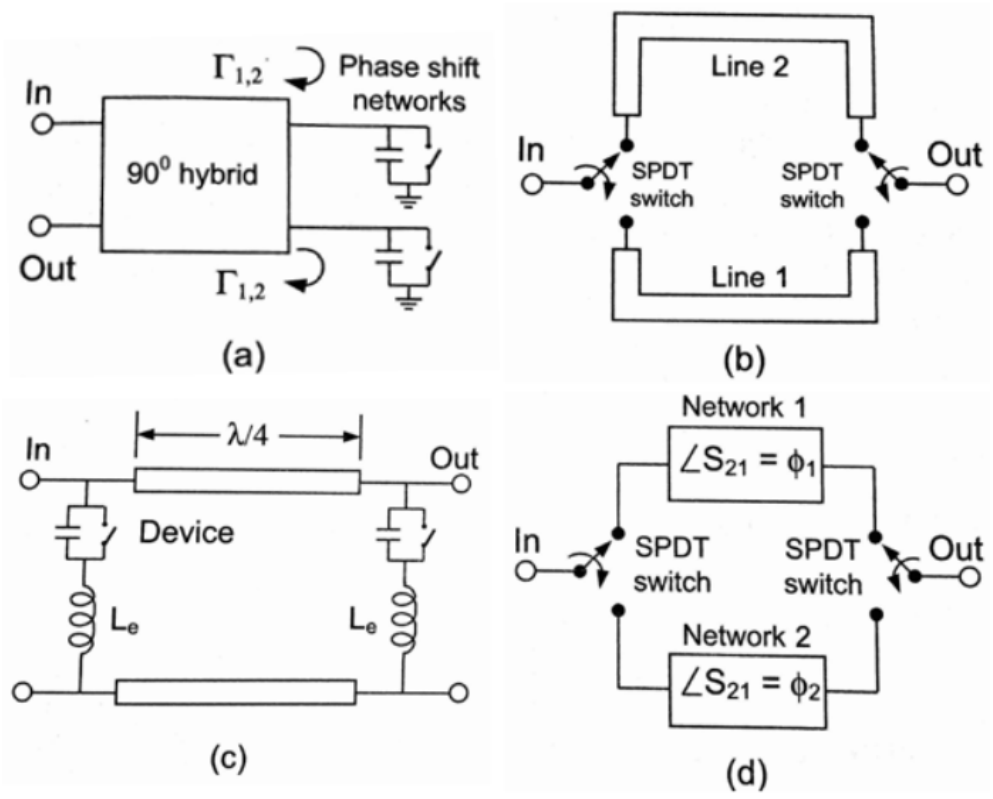

Figure 5-4: Phase shifter configurations [2]: (a) reflection-type (b) switched-line (c) loaded-line (d) switched-network

5.3.1 Analog Phase Shifter

In contrast to discrete values of digital phase shifters, analog phase shifters, also called tunable phase shifters, offer continuous phase shift in a specific range. Analog phase shifters are mainly implemented as two types of phase shifters: reflection-type and transmission-type phase shifters. Varactor is a key component for both reflection-type and transmission-type phase shifters to obtain continuous value of phase response. The transmission-type phase shifters can be modeled as a distributed network, resulting a linear phase response as a function of frequency. Since analog phase shifter is beyond the scope of this work, further details and analysis will not be given here.

5.3.2 Digital Phase Shifter

Digital phase shifters can be implemented based on many topologies. Figure 5-4 shows the four main topologies: reflection-type, switched-line, loaded-line and switched-network. Typical configurations for each of four main topologies are introduced.

Reflection-Type Phase Shifter

The reflection-type phase shifter is basically a one-port network where the control voltage controls the phase shift of the reflected signal. A 3-dB coupler is usually used to convert the one-port network into a two-port network. The phase shift of reflection-type phase shifter can be obtained by a switched-length or switched-reactance circuit. One

$$\Delta\phi = \tan^{-1}\left[-\frac{2Z_0\omega C_H}{1-(Z_0\omega C_H)^2}\right] - \tan^{-1}\left[-\frac{2Z_0\omega C_L}{1-(Z_0\omega C_L)^2}\right] \qquad \text{Eq. 5-3}$$

design example of reflection-type phase shifters shown in Figure 5-4 (a) has a capacitive reactance. Figure 5-5 presents a reflection-type phase shifter using Lange coupler and series capacitor. The phase shift of this phase shifter can be expressed as [2]

where subscripts L and H denote low and high impedance state of the switch, Z_0 is the system characteristic impedance, $C_L = C_1$, and $C_H = C_1//C_{off}$.

Switched-Line Phase Shifter

The switched-line phase shifter consists of two SPDT switches and two transmission lines with different length l_1 and l_2. The longer path has a phase delay with respect to the shorter path. Figure 5-5 (b) shows a conventional switched-line phase shifter. The phase delay can be calculated as [2]

$$\Delta\phi = \frac{2\pi\sqrt{\epsilon_{re}}}{\lambda_0}(l_2 - l_1) \qquad \text{Eq. 5-4}$$

where ϵ_{re}, λ_0, l_1 and l_2 are effective dielectric constant for the microstrip line, free space wavelength, length of the bottom transmission line and length of the upper transmission line, respectively. Besides the conventional configuration, Schiffman section has also been employed to broaden the bandwidth of a switched-line phase shifter.

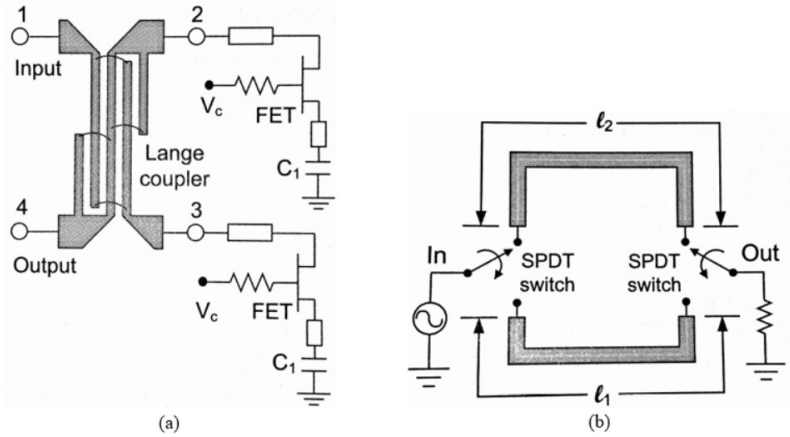

Figure 5-5: (a) Reflection-type phase shifter using Lange coupler and series capacitor

(b) Conventional switched-line phase shifter [2]

Loaded-Line Phase Shifter

As shown in Figure 5-6, the loaded-line phase shifter has a typical configuration including a quarter-wavelength transmission line at center frequency and two identical

admittances on each side. The two admittances contain a shunt or series switch to switch the phase shifter between the reference state and phase shift state. When the two admittances are connected to transmission path, equivalent circuit of the phase shifter can be modeled as an effective transmission line having an effective phase shift. Assuming two admittances are identical, the differential phase shift of the loaded-line phase shifter can be expressed as

$$\Delta\phi = \cos^{-1}(cos\theta - B_{on}Y_t sin\theta) - \cos^{-1}(\cos\theta - B_{off}Y_t sin\theta) \quad \text{Eq. 5-5}$$

where θ, B_{on}, B_{off} and Y_t are electrical length of the transmission line, susceptance in the on state, susceptance in the off state and admittance of the transmission line, respectively.

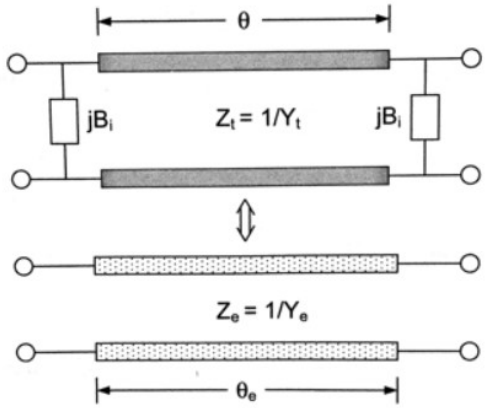

Figure 5-6: Typical loaded-line phase shifter and its equivalent circuit [2]

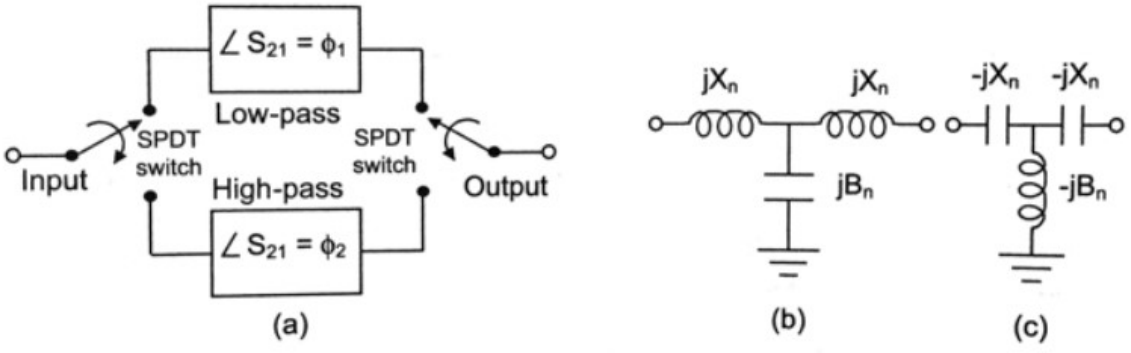

Figure 5-7: (a) Typical switched-network phase shifter (b) Low-pass network (c) High-pass network [2]

Switched-Network Phase Shifter

The switched-network phase shifters have two networks with different insertion phase. Two SPDT switches are usually used to switch between two paths to obtain a differential phase shift. A typical switched-network phase shifter consisting of a low-pass network and a high-pass network is shown in Figure 5-7 (a). If T-network is employed to implement both low-pass and high-pass networks, the differential phase shift between two networks can be expressed as [2]

$$\Delta\phi = 2\tan^{-1}[-\frac{B_n + 2X_n - B_n X_n^2}{2(1 - B_n X_n)}] \quad \text{Eq. 5-6}$$

Where B_n and X_n are the susceptance and reactance of the T-network as shown in Figure 5-7 (b) and (c). Besides the T-network, π-network can also be used to implement low-pass and high-pass networks as long as the component values are reasonable.

Embedded-Device Phase Shifter

Embedded-device phase shifters are also known as device-integrated phase shifters or T-bridged phase shifters. A typical embedded-device phase shifter was presented in Figure 5-8 (a). When FET1 is in the on state and FET2 is in the off state, the equivalent circuit of this phase shifter is only the on-resistance of FET1, hence, the phase shift is considered as zero. Meantime, the off-capacitance of FET2 will be resonated out by a parallel inductor L_p, resulting open circuit. When FET1 is in the off state and FET2 is in the on state, the equivalent circuit, presented in Figure 5-8 (b), is a simplified π-network and the parallel inductor L_p is shorted by the small on-resistance of FET2. C_T is equal to a combination of C_s and off-capacitance of FET1. The differential phase shift of the embedded-device phase shifter is expressed as [2]

$$\Delta\phi = \tan^{-1}\left(\frac{\omega L}{Z_0}\frac{1}{\omega^2 LC_T - 1}\right) \qquad \text{Eq. 5-7}$$

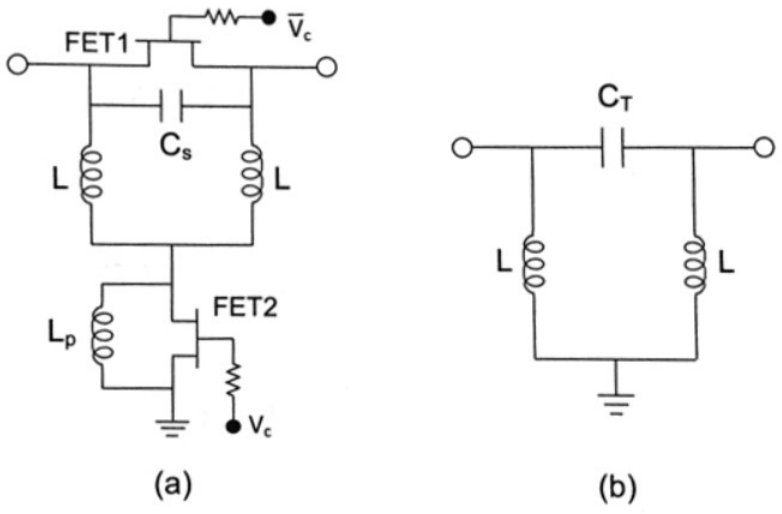

Figure 5-8: (a) An example for embedded-device phase shifter (b) The equivalent circuit

where Z_0, ω and L are the system characteristic impedance, operating radian frequency and inductance in the π-network. T-network can also be integrated into an embedded-device phase shifter as shown in Figure 5-9.

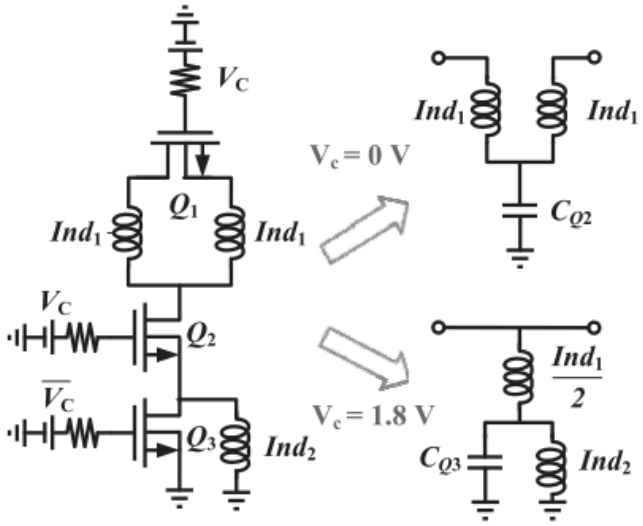

Figure 5-9: Embedded-device phase shifter using T-network [54]

5.4 Multi-bit Phase Shifter

Different types of phase shifters introduced above can be employed for different bit states depending on the desired performance parameters e.g. insertion loss, frequency response, RMS error, area size etc. In this section, details of each bit state will be given.

5.4.1 The 180° Bit

The 180° bit employed the low-/high-pass network due to the large desired phase shift. The 180° bit was built as the one shown in Figure 5-7 (b) and (c). By solving Eq. 5-5 and considering matching condition, $|S_{11}| = 0$, the normalized reactance and susceptance can be expressed as [51]

$$X_n = \tan(\frac{\Delta\phi}{4}) \quad \text{Eq. 5-8}$$

$$B_n = \sin(\frac{\Delta\phi}{2}) \quad \text{Eq. 5-9}$$

where $\Delta\phi$ is the desired phase shift. The component values are shown below.

Table 5-1: Calculated values for the 180° bit low-/high-pass phase shifter

$\Delta\phi$	Z_0	ω_o	X_n	B_n	C	L
180°	50 Ω	10 GHz	1	1	318 fF	795 pH

5.4.2 90°/45°/22.5°/11.25° Bit

Except for the 180° bit, all other four bits were implemented based on the embedded-device topology due to required compact size. In the embedded-device topology, transistors are absorbed into the phase shifter instead of being only switches in low-/high-

pass topology. In this work, the bridged-T network shown in Figure 5-9 was used. The desired component values can be calculated as [2]

$$L_1 = \frac{Z_0}{2\pi f_0}\tan(\frac{\Delta\phi}{2}) \quad \text{Eq. 5-10}$$

$$L_2 = \frac{Z_0}{4\pi f_0 \tan(\frac{\Delta\phi}{2})} \quad \text{Eq. 5-11}$$

$$C_2 = \frac{\sin(\Delta\phi)}{2\pi f_0 Z_0} \quad \text{Eq. 5-12}$$

$$C_3 = \frac{\tan(\frac{\Delta\phi}{2})}{\pi f_0 Z_0} \quad \text{Eq. 5-13}$$

where $\Delta\phi$, Z_0 and $\omega_0 = 2\pi f_0$ are the desired phase shift, system characteristic impedance and operating frequency. The calculated component values are shown Table 5-2.

Table 5-2: Calculated component values for the bridged-T type phase shifter

$\Delta\phi$ (^{o})	Z_0 (Ω)	f_o (GHz)	L_1 (nH)	L_2 (nH)	C_2 (fF)	C_3 (fF)
90	50	10	0.795	0.4	318	636
45	50	10	0.33	0.96	225	264
22.5	50	10	0.16	2	122	127
11.25	50	10	0.078	4	62	62

5.4.3 The 5-bit Digital Phase Shifter

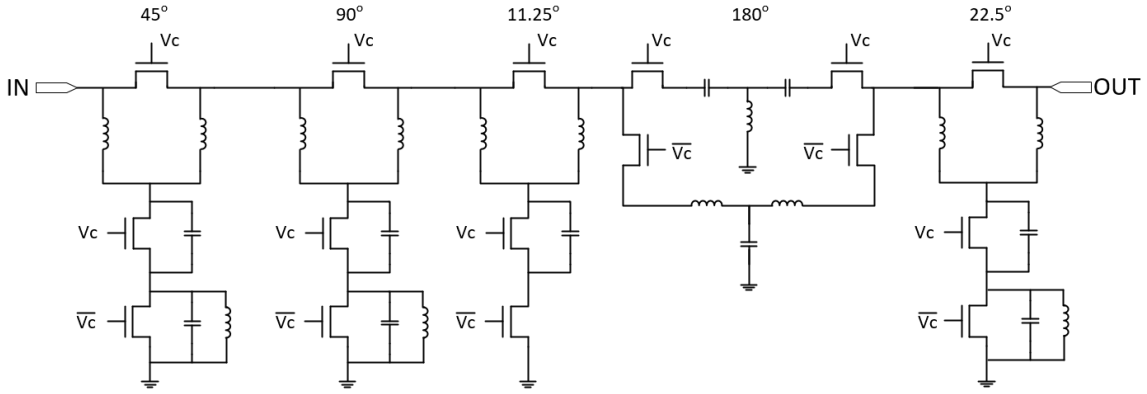

Figure 5-10: The proposed 5-bit phase shifter schematic

The 5-bit phase shifter has a lease significant bit of 11.25° and a most significant bit of 180°. In other words, the 5-bit phase shifter covers a phase shift range of 360° in an increment of 11.25°. The principle of bit ordering optimization is to arrange the bit stages with worse return loss between the bit stages with better return loss. In this case, the 11.25°, 22.5° and 45° bit stages have better return loss than the 90° and 180° bit stages do. The 5-bit phase shifter schematic is shown in Figure 5-10. As illustrated in the previous section, the 180° bit employed the high-pass/low-pass configuration while other four bits employed the embedded-device configuration. The inductor in parallel with the bottom transistor for resonance has been eliminated in the 11.25° bit since the inductance becomes high enough so that its impedance is significantly larger than the impedance of the bottom transistor. In the circuit implementation, transmission lines were employed for the relatively small inductors. Spiral inductors were utilized for relatively large inductors due to its superior quality factor. MIM capacitors were used for all capacitors in the circuit.

Simulation Results

The simulation setup for the 5-bit phase shifter is presented in Figure 5-11. Equations for the RMS phase and amplitude error have been given in Section 2.6.3. The EM co-simulation results have been presented in Figure 5-12 to Figure 5-17. Figure 5-12 presents the RMS phase and amplitude error of the 5-bit phase shifter. The 5-bit phase shifter has achieved a worst RMS phase error of 9.9^{o} over a frequency range of 8-12 GHz. In the best case, the RMS phase error is as low as 4.8^{o}. At center frequency (10 GHz), a RMS phase error of 6.5^{o} has been achieved. The RMS amplitude error decreases as frequency increases. A range of 3-6.5 dB for the RMS amplitude error has been reached. At center frequency, the RMS amplitude error is 5 dB. Figure 5-13 presents the insertion loss of all 32 states, including the reference state, for the 5-bit phase shifter. As illustrated, the blue solid line denotes the insertion loss of the reference state. The reference insertion loss is -9.8 dB at center frequency. The reference insertion loss varies from -13 dB to -8 dB over 8-12 GHz. The high reference insertion loss is mainly due to the high on-resistance of the GaN HEMTs while the variation can be contributed by the parasitic effects to ground and finite off-capacitance of the GaN HEMTs in the 180^{o} bit stage. Figure 5-14 presents relative phase shifts of all 32 states and Figure 5-15 presents the return loss for all 32 states. As shown in Figure 5-15, return loss for most states has tuned to be low than -10 dB at center frequency although it has been compromised for the RMS phase error. The IIP3 of the reference state is 14 dBm as shown in Figure 5-16. Figure 5-17 shows that the IIP3 of the 5-bit phase shifter varies as the phase shift state switches. Since the 5-bit phase shifter is in fact a cascade of five low pass and high pass filters, this cascade in different states change the impedance seen by transistors. In

addition, the capacitors paralleled with the middle transistor in the embedded-device topology alter the ratio of gate-drain capacitance and gate-source capacitance which further alters the voltage swing appeared at gate terminal. However, the quantitative analysis of this effect, which will not be illustrated here, is complex and beyond the scope of this work. Entire layout for the 5-bit phase shifter is presented in Figure 5-18. All five bit stages have been illustrated. This 5-bit phase shifter occupies an area size of 1.26 mm × 1.37 mm excluding pads.

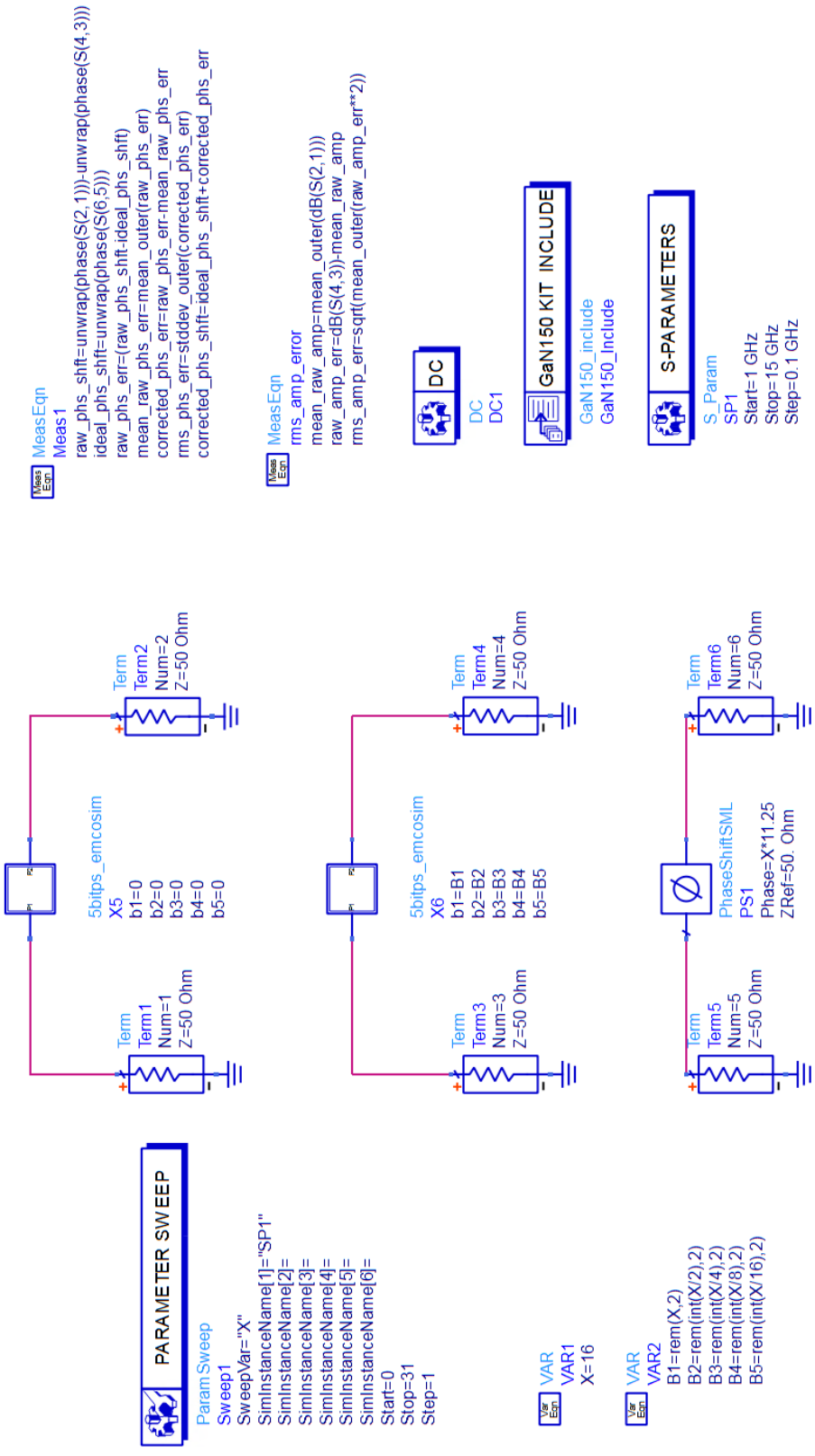

Figure 5-11: Small-signal simulation setup for the 5-bit digital phase shifter

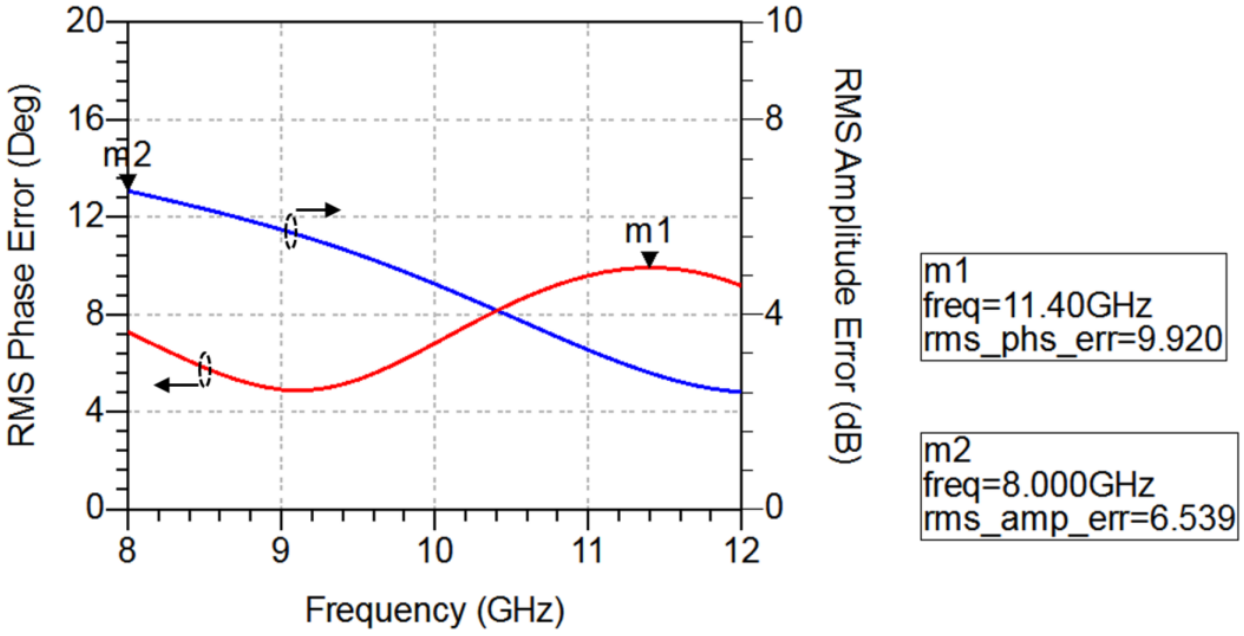

Figure 5-12: RMS phase error and amplitude error for the 5-bit digital phase shifter

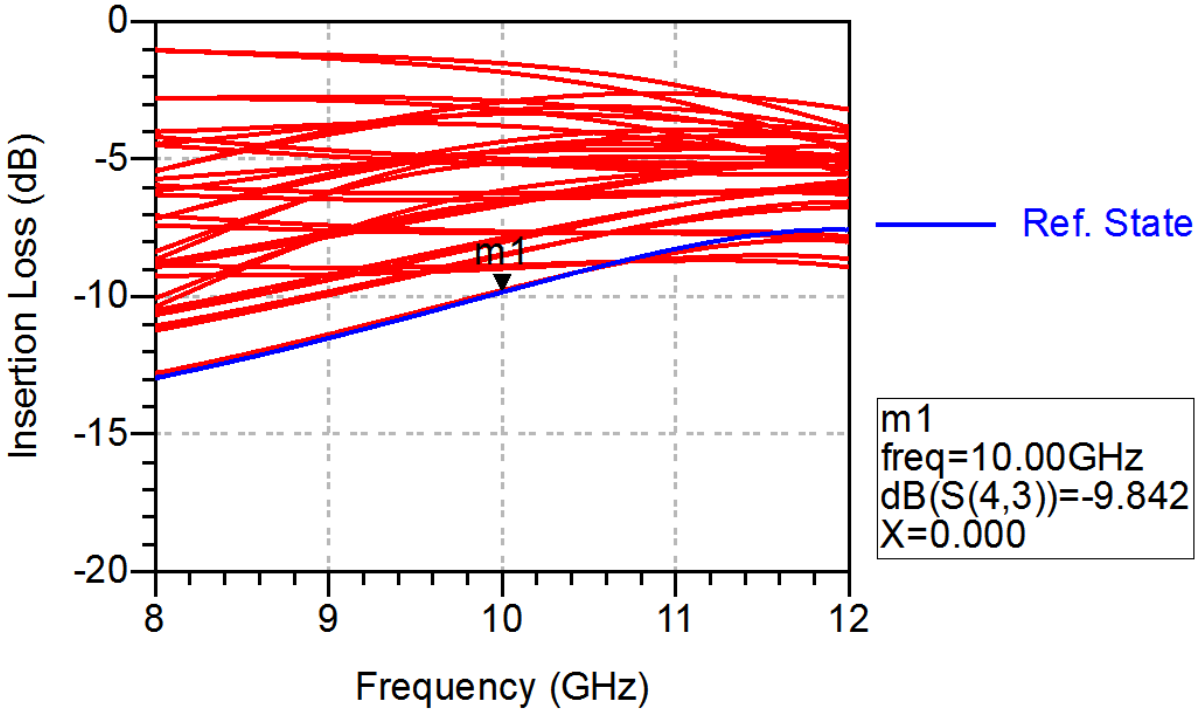

Figure 5-13: Insertion loss of all 32 states for the 5-bit digital phase shifter

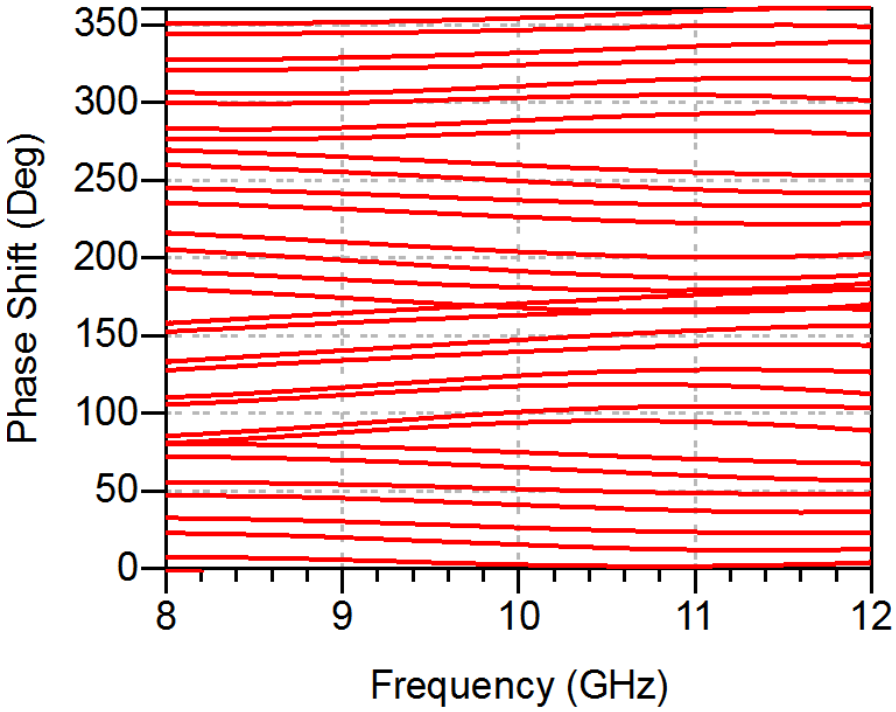

Figure 5-14: All 32 phase shift states for the 5-bit phase shifter

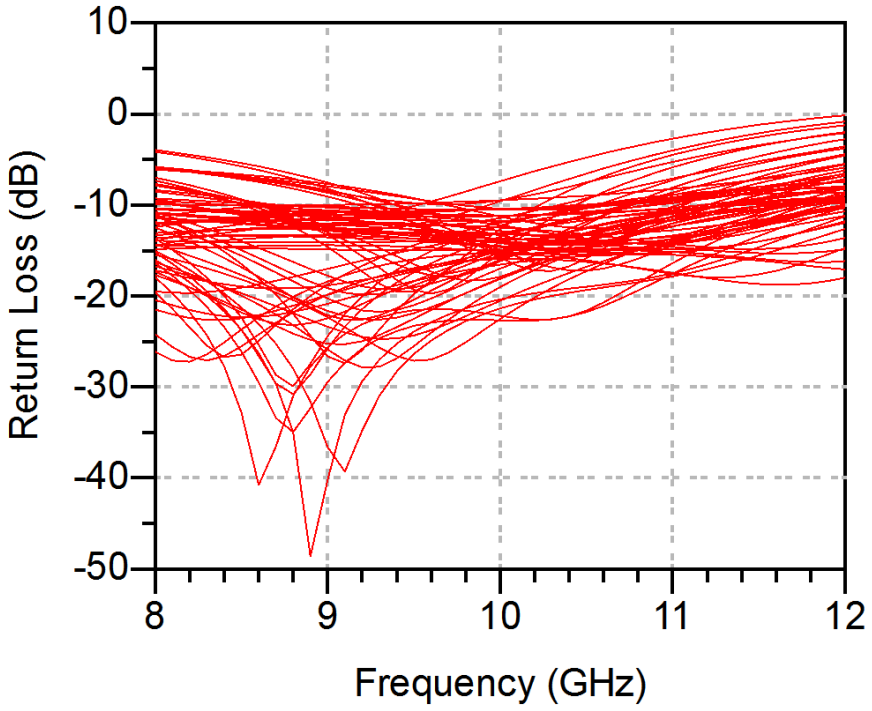

Figure 5-15: Return loss for the 5-bit phase shifter

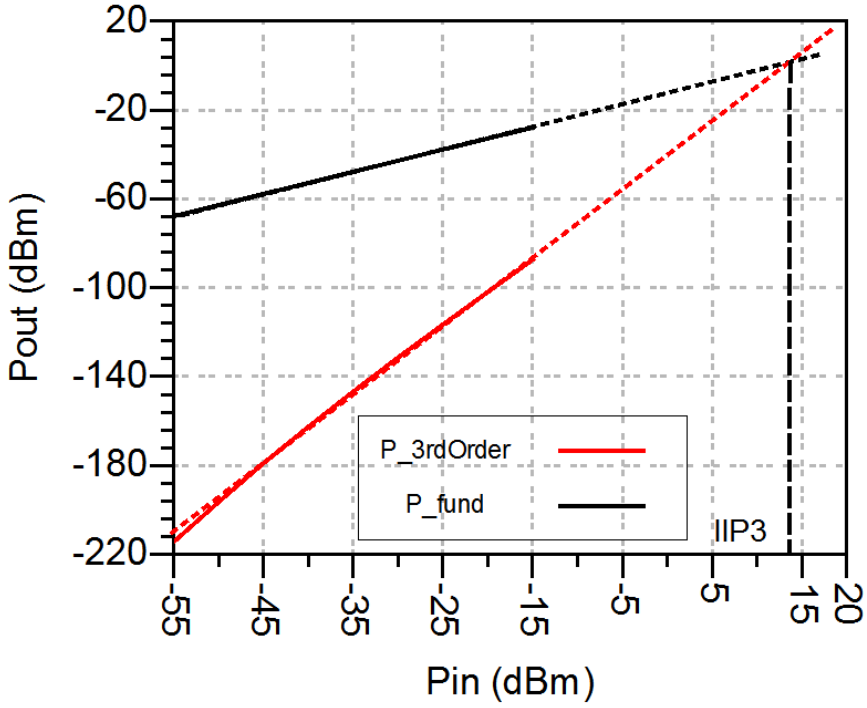

Figure 5-16: Reference-state IIP3 for the 5-bit phase shifter

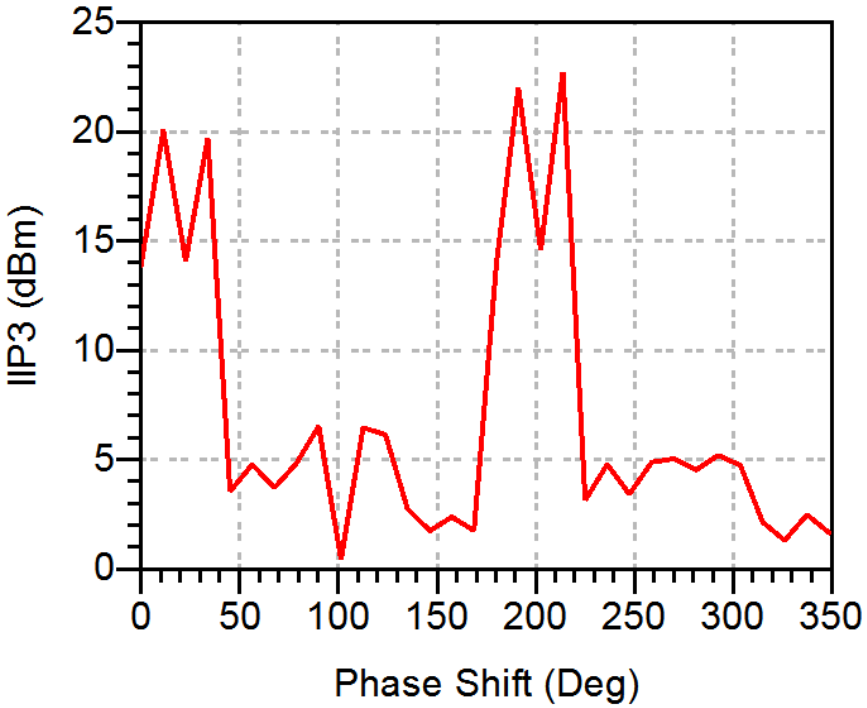

Figure 5-17: The IIP3 of all 32 states for the 5-bit phase shifter

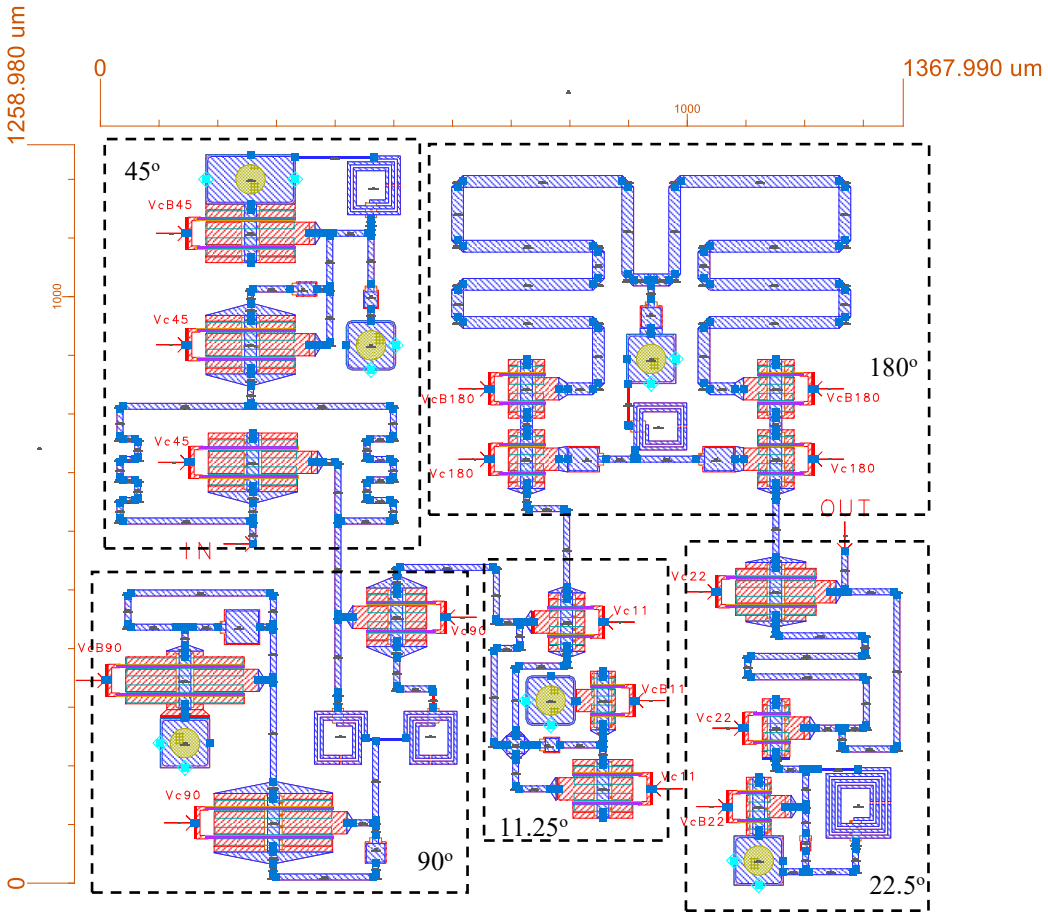

Figure 5-18: The proposed 5-bit phase shifter layout

5.5 Conclusion

In this chapter, a compact 5-bit phase shifter using 0.15-µm GaN technology was proposed. Literature review on X-band digital phase shifter was given first. The lumped components, spiral inductor and MIM capacitor, were then characterized for further utilization. Different types of phase shifters were introduced and several circuit topologies were also illustrated. EM co-simulation of the 5-bit phase shifter was performed to ensure that electromagnetic effects, including coupling and parasitic, are also accounted for. The performance of the 5-bit phase shifter has been compared to other digital phase shifters using different semiconductor technologies in Table 5-3. To the

author's knowledge, the proposed 5-bit phase shifter is the first 5-bit digital phase shifter designed in GaN technology.

Table 5-3 Comparison of previous works on digital phase shifter

Ref.	Tech.	Freq. (GHz)	# of bits	Topology	IL (dB)	RL (dB)	RMS Phase/Amp. Error (dB)/(º)	P_{1dB}/IIP3 (dBm)	Size area (mm^2)
[52]-1	0.5-µm GaN	8-16	1	22.5º switched-filter	2	11.15	0.5*/5.2*	40/46.2	0.304
[52]-2	0.5-µm GaN	7.5-13	1	22.5º LC resonator	5	11	3*/5.63*	30.1/46.3	1.05
[53]	0.25-µm GaAs pHEMT	8-12	6	Switched-network; loaded-line	7.6	10	3.3/0.7	-/-	4.2 × 2.2
[54]	0.18-µm CMOS	8-12	5	Switched-network; embedded device	17	8	8.8/1.3	-/-	1.15 × 0.7
[55]	0.25-µm SiGe BiCMOS	8-12	4	Switched-network; embedded device	14	10	2/1	-/-	-
[56]	0.18-µm SOI	8-12	5	Switched-network	10.8	12	6.5/0.5	10/-	1.14 × 0.78**
[57]	0.13-µm SiGe BiCMOS	8-12	5	Switched-network	25	13	13*/-	-/-	0.446
This work ****	0.15-µm GaN	8-12	5	Switched-network; embedded device	9.8	7	9.9/6.5	-/0-14	1.26 × 1.37**

*The value is relative not RMS.

**The Chip size excludes pads.

***Note that insertion loss, return loss, RMS phase error and amplitude error are shown in the worst case.

**** Note that performance results for this work are simulation results.

Chapter 6 Attenuator Design

6.1 Literature Review

Attenuators are widely used not only in phased array radars but also in other modern radio frequency wireless communication systems. Designs based on distinctive design techniques have been demonstrated in the literature. In [61], Egor Alekseev et al. demonstrated the first single-bit attenuator MMIC based on AlGaN/GaN HEMT technology. The attenuator utilized a PI-network topology has a high dynamic range of 30 dB at 8 GHz. In [62], Bon-Hyun Ku et al. designed two 6-bit digital step attenuators with inductive and capacitive phase correction circuits were fabricated in 1P6M 0.18-µm CMOS technology. Phase variations of conventional switched Pi/T attenuators have been quantitatively analyzed in the literature. The inductive and capacitive phase correction circuits based on low-pass filter are used to compensate phase variations. The performance of two fabricated digital attenuators were state-of-art and given in the literature. In [63], Zhang Hao et al. designed a 6-bit X-band high linearity digital attenuator with low phase variations based on 0.13-µm BiCMOS technology. Inductive and capacitive phase correction networks were employed to compensate phase variations. High linearity was obtained by employed the floating substrate technique. In [64], Murat Davulcu et al. designed a 7-bit CMOS digital step attenuator for X-band phased array radar applications based on IHP 0.25-µm SiGe BiCMOS technology. Isolated NMOS devices were used to reduce the insertion loss caused by parasitic capacitances. Low-pass filters were utilized as phase correction networks. In [65], Kazuo Miyatsuji et al. proposed a technique to improve the distortion of digital attenuators. It was found that the

steep cutoff Id-Vgs characteristic of conventional FETs results in the distortion. They developed the squeezed-gate structure where the FETs with different threshold voltages are connected in parallel to make use of the short channel effect and claimed the third order intermodulation distortion has been reduced by 10 dB from the measurement. For other types of variable attenuators, Junfeng Sun et al. designed a broadband 3-bit Micro-electro-mechanical system digital attenuator for 0-20 GHz [66]. Yong-Sheng Dai et al. presented an ultra-wideband digital/analog compatible MMIC variable attenuator based on GaAs technology [67]. The digital/analog compatible MMIC attenuator works at the frequency range of 0.045-50 GHz and has a control circuit using the equivalent load method of control signals.

6.2 Types of Attenuators

Similar to the definition of phase shifter, attenuators are two-port networks that change the amplitude of the signal. There are three main types of attenuators: fixed-value attenuators, analog attenuators and digital attenuators.

6.2.1 Fixed-value Attenuators

Fixed-value attenuators which offer a single value of attenuation usually have attenuation values of 3 dB, 6 dB, 10 dB, 20 dB. Thin-film and thick-film hybrid technologies are employed to fabricate MMIC resistors. Another kind of fixed-value attenuators is called temperature variable attenuator which eliminates the temperature variations. The temperature coefficient of resistor films is another performance parameter of temperature variable attenuators [2].

6.2.2 Analog Attenuators

Analog attenuators are the attenuators offer a continuous range of attenuation value controlled by bias voltages. Unlike fixed-value attenuators and digital attenuators, analog attenuators can tolerate variations in the process of fabrication. There are several kinds of analog attenuators: T- or π- network analog attenuators, reflection-type analog attenuators, balanced analog attenuators etc. Many voltage variable attenuators employ the T- and π-configurations. To obtain a range of attenuation value, the devices in voltage variable attenuators are biased in non-linear resistance region instead of linear resistance region, so called as the triode region. Both PIN diodes and transistors are used in voltage variable attenuators. The resistance of a PIN diode mostly depends on the DC bias current while the resistance of a zero-biased FET varies as a function of gate bias voltage. To achieve a linear attenuation response, many design techniques have been utilized such as look-up table approach, multi-FETs method, multi-FET with voltage shift diodes [2] etc. More information on analog attenuators can be found in the literature [1].

6.2.3 Digital Attenuators

In contrast with analog attenuators, digital attenuators provide a range of attenuation values in steps. To realize the individual attenuation states, digital attenuators consist of cascaded bits which are binary-weighted. The lease significant bit (LSB) level defines the resolution of a digital step attenuator while the most significant bit (MSB) level determines the maximum attenuation range. There are four topologies mainly employed to design digital step attenuators: switched-path, switched scaled-FET, switched T-/π-network, and embedded-device topologies.

Switched-path attenuators

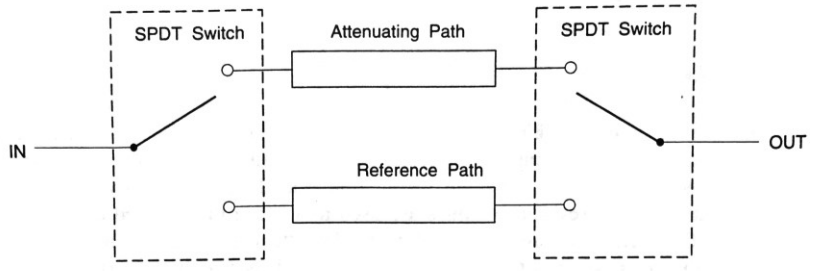

Figure 6-1: Schematic diagram of a switched-path attenuator [1]

As shown in Figure 6-1, the switched-path attenuator consists of two SPDT switches and two transmission paths: attenuation path and reference path. When the switched-path attenuator is in the off state, two SPDT switches pass the signal through the reference path. When the switched-path attenuator is in the on state, the transmission path is switched to the attenuation path. The difference between insertion losses in two states is the relative attenuation. The attenuation path is usually based on T- or π- networks. Phase alignment between two paths can be achieved by equalizing lengths of two paths. The SPDT switches dominates the input and output matching for the switched-path attenuators. The switched-path attenuators are usually utilized for larger attenuation bits.

Switched scaled-FET Attenuators

In the switched scaled-FET attenuators, different sizes transistors are employed as low on-resistance resistors to replace the thin-film resistors. The difference between on-resistances of transistors with different gate periphery gives the desired relative attenuation value. Figure 6-2 shows the two examples of the switched scaled-FET attenuators employing the T-network configuration. In Figure 6-2 (a), two series transistors and a shunt resistor used in each path are of different sizes and values.

Compared to Figure 6-2 (a), the switched scaled-FET attenuator shown in Figure 6-2 (b) has an additional shunt FET in series with the shunt resistor. The series transistors should have a large size to obtain a minimum insertion loss. Also, transmission lines might be needed in some designs for phase equalization. The switched-scaled FET attenuators are suitable for small attenuation bit (<4 dB) due to finite on-resistance of transistors. Besides T-network, the switched scaled-FET attenuators can also be based on π-Network configuration.

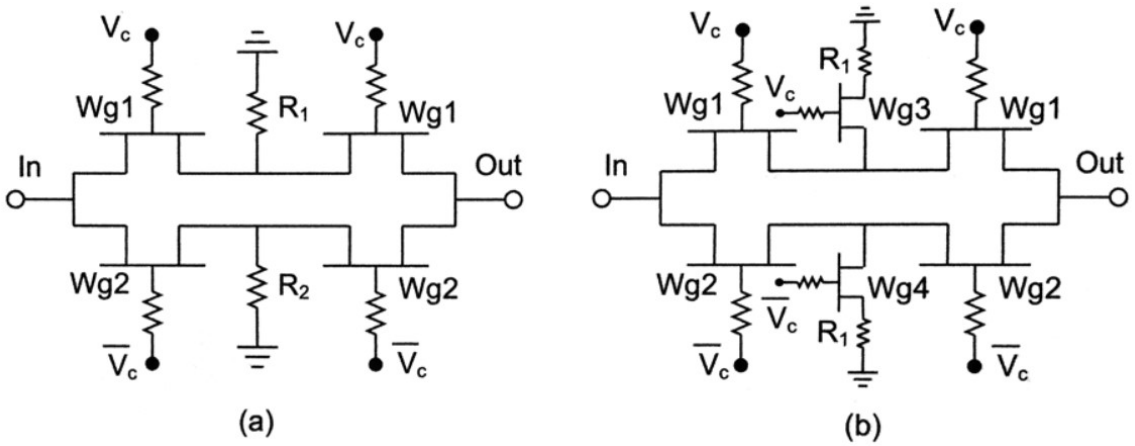

Figure 6-2: Switched scaled-FET attenuators [2]

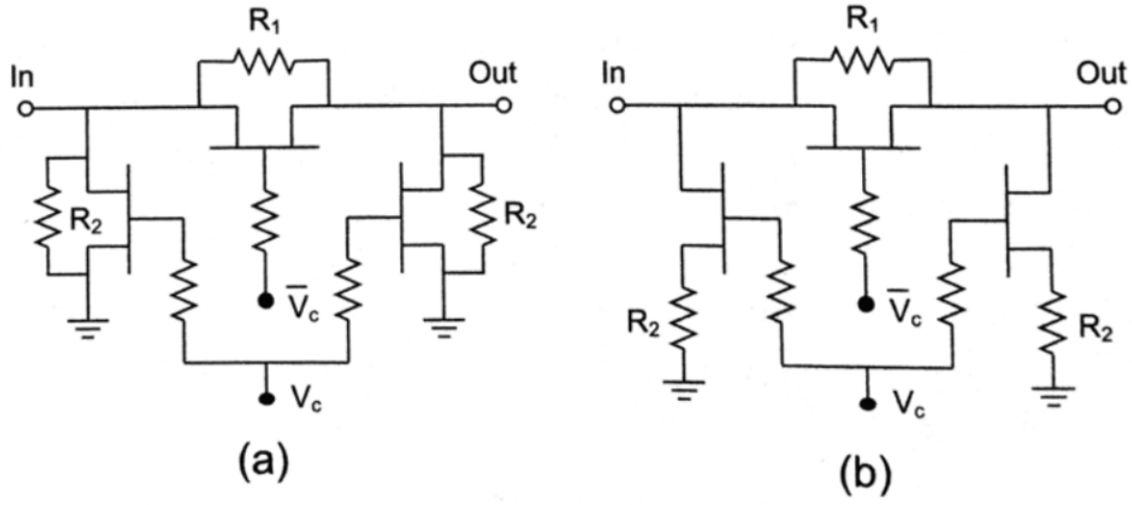

Figure 6-3: Switched T-/π-network attenuators [2]

Switched T-/π-Network Attenuators

The switched T-/π-Network attenuators utilize transistors as simple switches to switch in or out the resistors. Since smaller transistors can be used in this topology, less parasitic capacitances result in a better high frequency characteristic compared to switched scaled-FET attenuators. As demonstrated in the literature [1], switched T-/π-network attenuators can provide low RMS amplitude error but may have a serious phase shift problem. In addition to low RMS amplitude error, symmetric configuration gives switched T-/π-network attenuators ability to tolerate fabrication and temperature variations.

Embedded-Device Attenuators

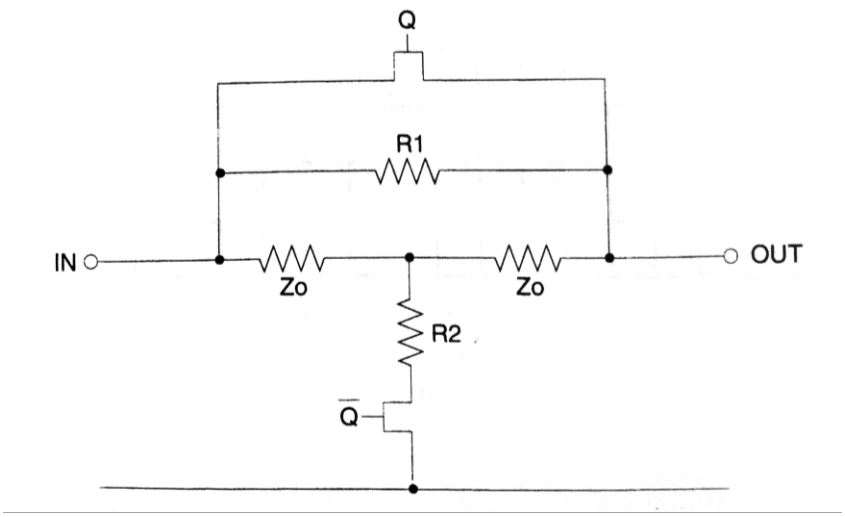

Figure 6-4: Embedded-device attenuator [1]

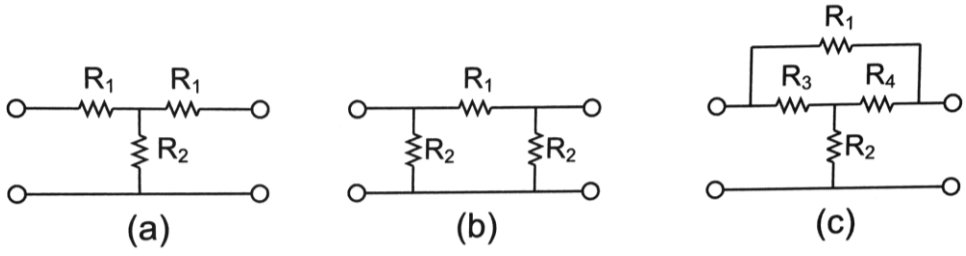

Figure 6-5: Networks used for attenuators: (a) T-network (b) π-network (c) bridged-T network

The embedded-device attenuators can be based on T-network, π-network, and bridged-T network. An embedded-device attenuator employing bridged-T network, also termed as switched bridged-T attenuator [1], is shown in Figure 6-4. The series and shunt transistor are used to switch the attenuator between reference state and attenuation state. When the attenuator is in reference state, the series transistor is on and shunt transistor is off. The insertion loss is only determined by the on-resistance of the series transistor. When the attenuator is in attenuation state, the series transistor is off and the shunt transistor is on, leaving a classic bridged-T network. Compared to other topologies, one main advantage of the switched bridged-T attenuator in Figure 6-4 is that it is intrinsically matched to the system characteristic impedance. Also, the embedded-device attenuators are attractive to compact designs since the transistors are integrated into the classic T-network, π-network, or bridged-T network.

6.3 Theory of Attenuators

As mentioned in the previous section, digital attenuators employing different topologies are based on the classic T-network, π-network, or bridged-T network shown in Figure 6-5. To obtain the desired attenuation value and match to the system characteristic impedance Z_0, the resistance values for these three networks can be expressed as follow [2]. For the T-network,

$$R_1 = \frac{Z_0(A-1)}{A+1} \qquad \text{Eq. 6-1}$$

$$R_2 = \frac{2Z_0A}{(A+1)(A-1)} \qquad \text{Eq. 6-2}$$

For the π-network,

$$R_1 = \frac{Z_0(A - 1/A)}{2} \quad \text{Eq. 6-3}$$

$$R_2 = \frac{Z_0(A + 1)}{A - 1} \quad \text{Eq. 6-4}$$

For the bridged-T network,

$$R_2 = \frac{Z_0}{A - 1} \quad \text{Eq. 6-5}$$

$$R_1 = Z_0(A - 1) \quad \text{Eq. 6-6}$$

where A is the voltage attenuation ratio in linear. Note that the attenuation ratio A is a positive term and is defined as the ratio of source available voltage to load available voltage.

6.4 Multi-bit Attenuator

6.4.1 The 4-dB/8-dB/16-dB Bits

The 4-dB/8-dB/16-dB bits employs a new kind of embedded-device topology based on T-network configuration. The 16-dB bit consists of two identical 8-dB bits due to its large desired attenuation value. Compared to classic T-network configuration, the new configuration has smaller insertion loss when it is in the reference state since the series transistor is the only one factor contributes to insertion loss. Besides, the shunt transistor which is off improves return loss for reference state. When it is in the attenuated state, the new configuration switches back to a classic T-network configuration. An additional transistor is placed in parallel with the shunt resistor for the 4-dB bit to improve return loss of its attenuated state. All the resistors in these three bits are implemented by the thin-film resistors which are available in the GaN process.

6.4.2 The 1-dB/2-dB Bits

The 1-dB/2-dB bits employs also a kind of embedded-device topology based on classic T-network configuration. Unlike the configuration previously mentioned, this simple configuration has only one shunt transistor. The switching between reference and attenuated states is achieved by a shunt transistor. When it is in the reference state, the transistor is off. When it is in the attenuated state, the shunt transistor is on and the total shunt resistance is the sum of on-resistance of the shunt resistor and shunt resistance. In the 1-dB and 2-dB bits, series resistors are replaced by transmission lines due to the relatively small desire values with respect to losses along transmission lines.

6.4.3 The 5-Bit Digital Attenuator

The 5-bit digital attenuator has a LSB of 1 dB and a MSB of 16 dB. It covers an attenuation range of 31 dB in an increment of 1dB. Figure 6-6 presents the 5-bit digital attenuator diagram. The bit-ordering optimization is similar to that for the 5-bit digital phase shifter. The principle is still to arrange the bit stage that has worse return loss in between the bit stages with better return loss.

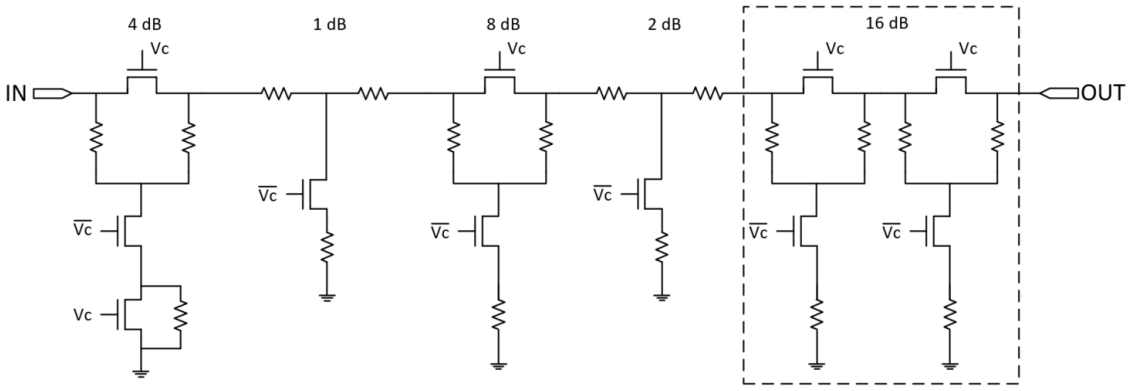

Figure 6-6: The 5-bit digital attenuator diagram

Simulation Results

Simulation results from EM co-simulation are presented in following figures. Figure 6-8 presents the RMS amplitude and phase errors for the attenuator. The RMS amplitude error varies from 0.3 dB to 0.7 dB over 8-12 GHz while the RMS phase error decreases from 6º to 3º as frequency goes from 8 GHz to 12 GHz. As shown in Figure 6-9, the reference-state insertion loss is as low as -1.8 dB over 8-12 GHz. The reference-state insertion loss at center frequency is -2.3 dB and slightly decreases as frequency rises. Figure 6-10 presents the relative attenuation of all 32 states and Figure 6-11 presents return loss of all 32 states. As illustrated in Figure 6-11, return loss of all 32 states are better than -8 dB over 8-12 GHz. Figure 6-12 presents the IIP3 for the attenuator as a function of attenuated states. Similar to the IIP3 for the 5-bit digital phase shifter, the IIP3 for the attenuator behaves periodically. The maximum IIP3 is 33 dBm while the minimum IIP3 is 10 dBm.

Figure 6-7: Small-signal simulation setup for the 5-bit digital attenuator

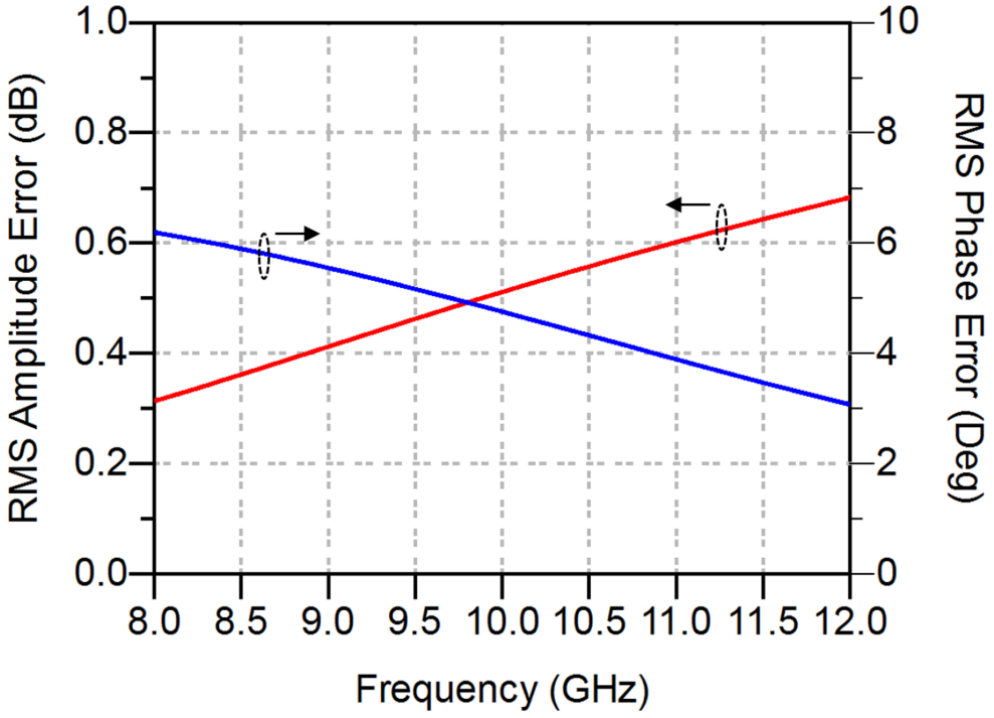

Figure 6-8: The RMS amplitude and phase error for the 5-bit digital attenuator

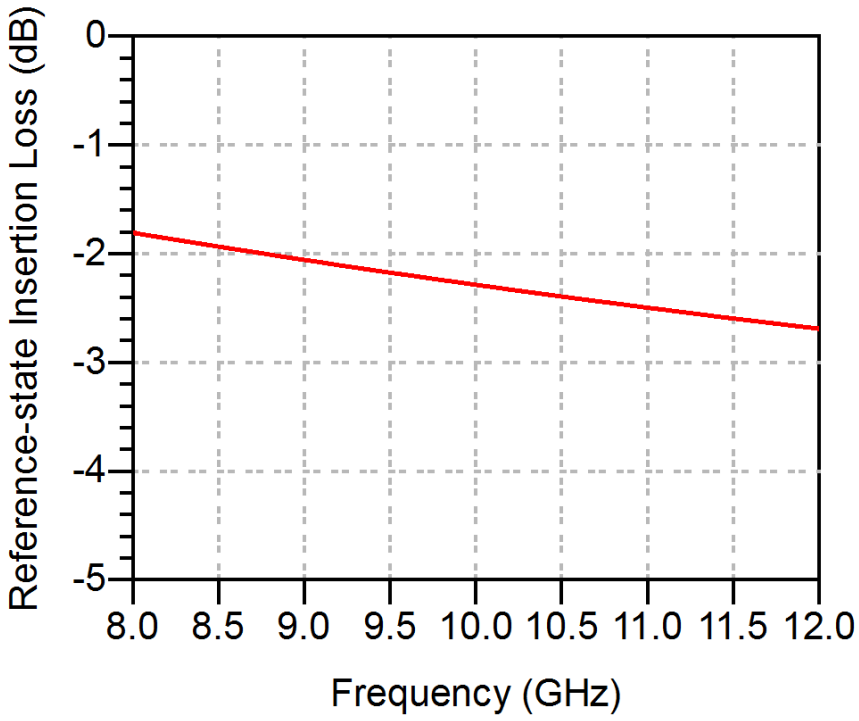

Figure 6-9: The reference-state insertion loss for the 5-bit digital attenuator

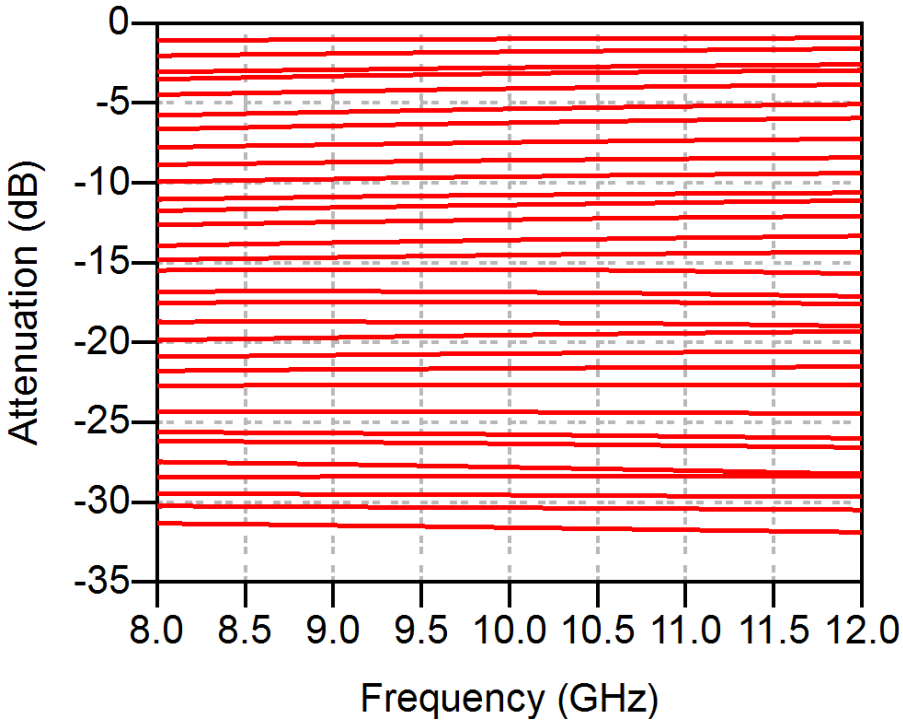

Figure 6-10: The relative attenuation of all 32 states for the 5-bit digital attenuator

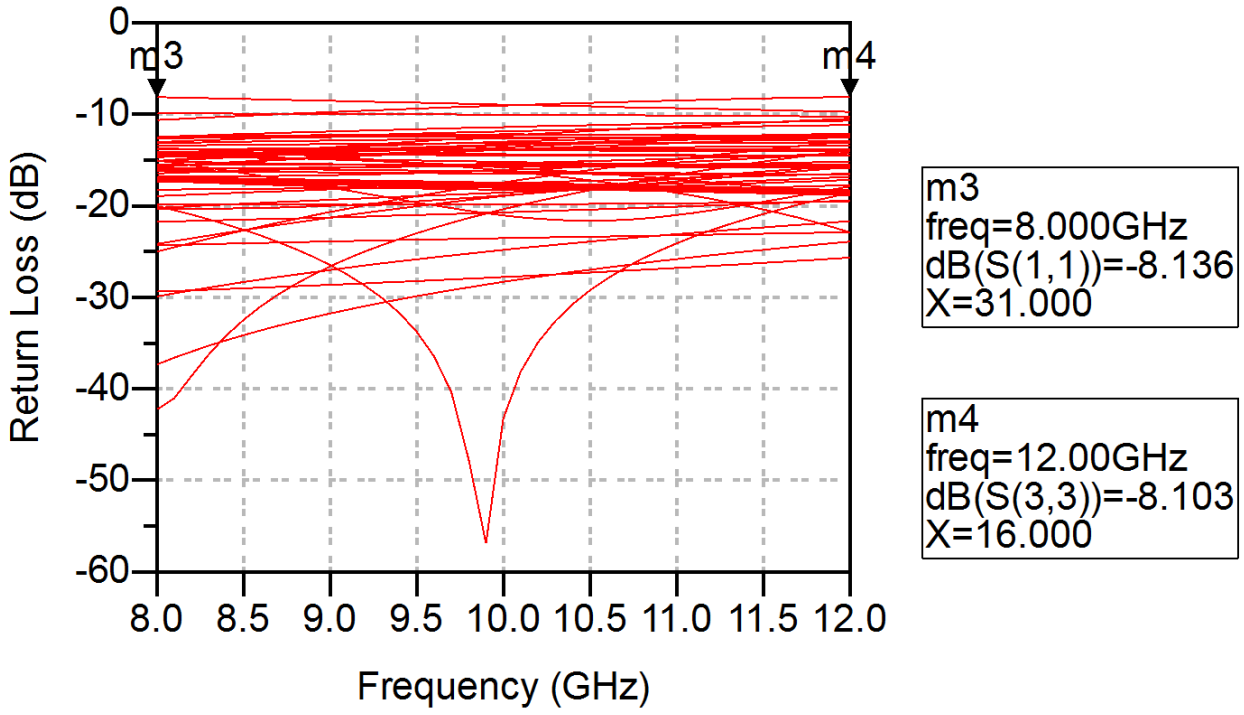

Figure 6-11: The return loss of all 32 states for the 5-bit digital attenuator

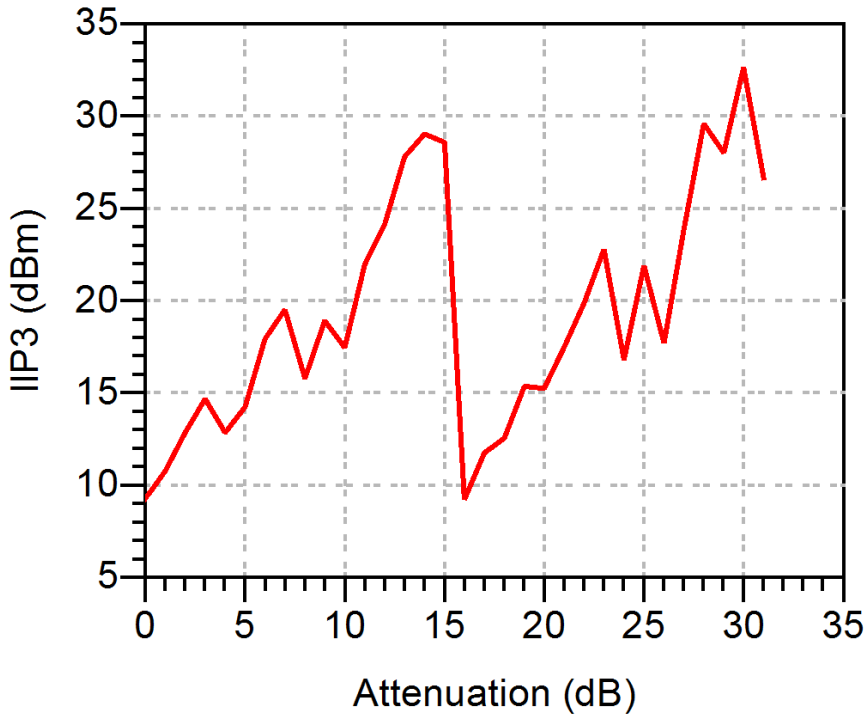

Figure 6-12: The IIP3 for the 5-bit digital attenuator as a function of attenuated states

6.5 Conclusion

This chapter proposed a 5-bit digital attenuator using GaN technology. Literature review on digital attenuators was performed and performance of different digital attenuator designs were listed in Table 6-1. Thin-film resistor available in the GaN process was characterized before started the design. Types of attenuators were then introduced and different topologies to implement digital attenuator were compared. Design equations for T-, π- and bridged-T network configuration were listed after. The circuit topology and design considerations for the 5-bit digital attenuator were illustrated in the previous section. Finally, results from EM co-simulation were presented and entire layout for the 5-bit digital attenuator was shown. The proposed 5-bit digital attenuator occupies an area size of 1.29 mm × 1.05 mm.

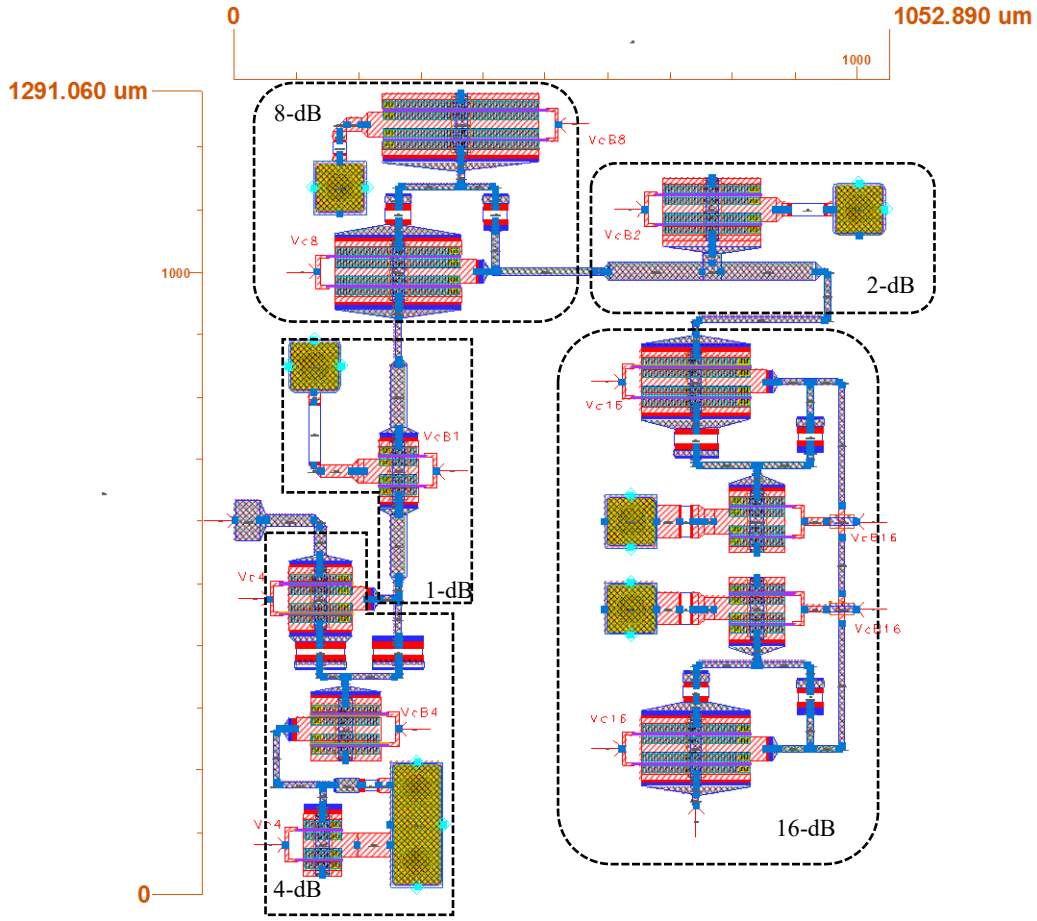

Figure 6-13: The proposed 5-bit digital attenuator layout

Table 6-1: Comparison of previous works on digital attenuators

Ref.	Tech.	Freq. (GHz)	Topology	IL (dB)	RL (dB)	RMS Amplitude/ Phase Error (dB)/(°)	P_{1dB}/IIP3 (dBm)	Size area (mm^2)
[62]-1	0.18-µm CMOS	8-12	Switched Pi/T w/ inductive phase correction	8-9.3	10	0.3 / 3.5	15/29	1.25 × 0.4*
[62]-2	0.18-µm CMOS	8-12	Switched Pi/T w/ capacitive phase correction	9.8-11.3	11	0.4 / 2.2	13/28	0.67 × 0.5*
[63]	0.13-µm BiCMOS	7-13	Switched Pi w/ phase correction	6.67	20	0.7 / 0.6	15.5/-	1.8 × 2.4
[64]	0.25-µm SiGe BiCMOS	6-12.5	Switched Pi w/ phase correction	12.7	13	0.26 / 3.5	12.5/-	0.29*
This work***	0.15-µm GaN	8-12	Embedded-T	2.8	8	0.7/6	-/10-33	1.29 × 1.05*

*Chip size excluding pads

**Note that insertion loss, return loss, RMS phase error and amplitude error are shown in the worst case.

*** Note that performance results for this work are simulation results.

Chapter 7 Conclusion & Future Work

7.1 Conclusion

In this thesis, an ultra-compact and reconfigurable X-band GaN-based control MMIC was presented along with the characterization of fabricated GaN HEMTs.

The validation of the 0.15-µm GaN process was done through the characterization of previously fabricated HEMTs. In the characterization, the GaN HEMTs were measured under dc, small- and large-signal conditions. Validation shows that the design kit model strongly agrees with measured results. In addition, a linear small-signal model extracted from measured s-parameters for switch-based GaN HEMT was proposed. Series and series-shunt SPST switches using the measured extracted linear small-signal model were simulated and compared to the design kit model. The proposed SPDT switch has achieved high linearity performance and compact area size simultaneously. Besides, the proposed SPDT switch also maintain reasonable performance in terms of insertion loss, isolation and return loss. To the author's knowledge, the proposed 5-bit digital phase shifter was the first ever implementation using GaN technology. The proposed phase shifter has a comparable performance in reference to digital phase shifters in other competing microwave technologies with the exception of linearity. The proposed attenuator also has achieved competitive performance while maintaining a compact size.

In summary, this work validates the 0.15-µm GaN process and explores the possibilities of designing control MMICs using the 0.15-µm GaN process. To the best of our

knowledge, this work has designed the first 5-bit digital phase shifter and the first 5-bit digital attenuator using the 0.15-µm GaN process.

7.2 Future work

In this work, the design of an ultra-compact and reconfigurable X-band GaN-based MMIC has been presented. As presented in Figure 7-1, the proposed SPDT switch, 5-bit digital phase shifter and 5-bit digital attenuator were fitted into one single chip which has a frame size of 2 mm × 4 mm. Two RF pads were placed on the right side of the control MMIC chip for Tx and Rx paths, respectively. In addition, a digital inverter in GaN was designed to provide complementary dc control signals in order to reduce the number of required dc pads. Although the final MMIC has not been fabricated due to delays in the fabrication schedule as well as increased cost of fabrication, it can be seen that all 3 blocks can easily be fitted into a 2 mm × 4 mm chip. The full design of the control MMIC has passed DRC and LVS requirements and is ready for fabrication.

In addition, Monte-Carlo analysis and sensitivity analysis will be necessary to further complement fabrication of the control MMIC. If possible, the linearity of the phase shifter and attenuator could be improved by further examining simpler topologies such as low-/high-pass switched networks, switched line, loaded line, etc.

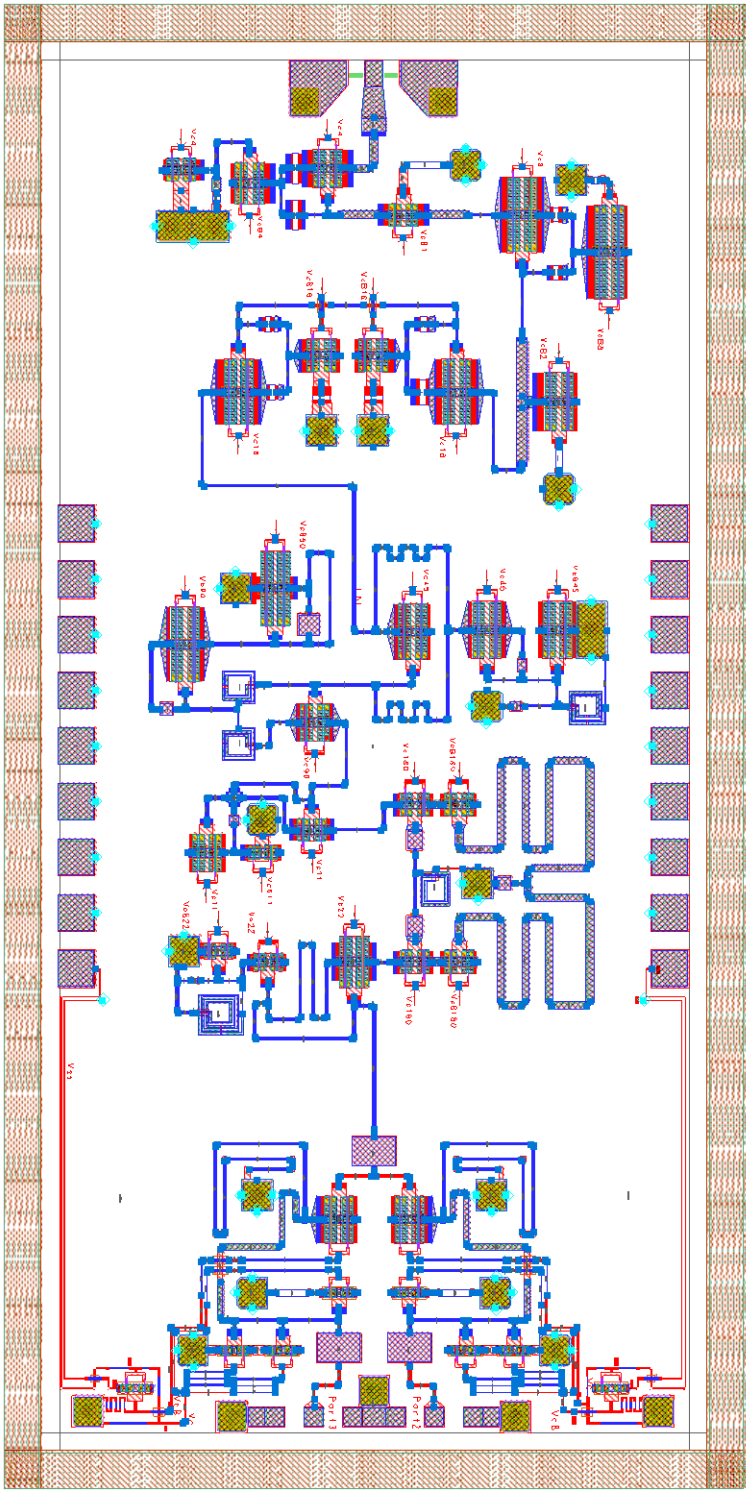

Figure 7-1: Simplified layout for the proposed control MMIC (Frame size: 2 mm × 4 mm)

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