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**New Approaches For Designing
High Voltage, High Current
Silicon Step Recovery Diodes
for Pulse Sharpening Applications**

by

Michael John Chudobiak, B.Sc. (Hons.)

**A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements
for the degree of
Doctor of Philosophy**

**Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Carleton University
Ottawa, Ontario, Canada**

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**“New Approaches For Designing High Voltage,
High Current Silicon Step Recovery Diodes
for Pulse Sharpening Applications”**

submitted by

Michael John Chudobiak. B.Sc. (Hons.)

in partial fulfillment of the requirements
for the degree of Doctor of Philosophy

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Thesis Supervisor

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Sept. 13, 1996

Abstract

Two promising new approaches for designing step recovery diodes (SRDs) for operation at voltages of several hundred volts are considered in this thesis. An entirely new type of step recovery diode is presented, which can operate with reverse voltages of several hundred volts and which exhibits exceptionally long lifetimes of several microseconds. These diodes have been named "wide field step recovery diodes (WFSRDs)". Experimental results for two batches of fabricated devices are presented for 300 V operation into a 50 Ω load. Pulse sharpening operation with rise times as low as 0.9 ns and storage times as large as 9 ns has been observed for fabricated diodes with effective carrier lifetimes of 4500 ns. Pulse sharpening operation has also been observed with rise times as low as 0.6 ns and storage times as large as 30 ns for fabricated diodes with effective carrier lifetimes of 950 ns. These diodes have a diffused p- π -n structure. A comprehensive design theory is developed by considering the nature of the reverse transient in the diode. A method of calculating the breakdown voltage of diffused structures without resorting to simulations is also presented. It is shown that fabrication difficulties will limit the usefulness of the WFSRD to operating voltages below 1 kV.

High-voltage drift step recovery diodes (DSRDs), previously proposed in other work, are also considered. As DSRDs are biased with a pulse, the nature of the forward transient in the diode is considered in detail here. From this, the existing design theory is greatly extended. In particular, the optimum values of the width of the lightly doped layer and the bias current can now be predicted based on the new theory. The maximum storage time consistent with good step recovery action can also now be calculated. These theoretical results are compared to experimental results presented elsewhere, and are in good agreement. It is shown that storage time limitations restrict the use of the DSRD to operating voltages above 1 kV.

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J_F/J_0 the corresponding values of N_D are 2.6×10^{12} , 1.2×10^{13} , 5.6×10^{13} , 2.6×10^{14} , and $1.2 \times 10^{15} \text{ cm}^{-3}$122

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List of Symbols

Symbol	First appears on page:	Meaning (common units)
α_{eff}	159	effective ionization coefficient. (m^{-1})
α_n	158	electron ionization coefficient. (m^{-1})
α_p	158	hole ionization coefficient. (m^{-1})
Δx	82	the distance between x_{nj} and x_{p0} , see equation (5.15). (μm)
Δx	120	a small distance. (μm)
ΔT	168	a temperature differential. (K)
ϵ	24	dielectric constant of silicon, approximately $11.8 \epsilon_0$. (F/m)
ϕ	168	heat flux. (W/cm^2)
κ	167	thermal conductivity. (W/cmK)
λ	42	a dopant diffusion length. (μm)
λ_1	42	a dopant diffusion length. (μm)
λ_2	42	a dopant diffusion length. (μm)
π	ii	lightly doped p-type region.
ρ	167	density. (g/cm^3)
τ	15	high-level ambipolar lifetime, defined by equation (2.3). (ns)
τ_{EFF}	2	effective carrier lifetime. Defined by equation (3.4). (ns)
τ_{n0}	15	low-level electron lifetime. (ns)
τ_{p0}	15	low-level hole lifetime. (ns)
τ_{RC}	86	RC time constant of the reverse-biased diode near breakdown. (ns)
τ_{th}	167	thermal time constant. (s)
μ_n	15	electron mobility. (cm^2/Vs)
μ_p	15	hole mobility. (cm^2/Vs)
ω	143	angular frequency. (rad/s)

A	6	diode cross-sectional area. (mm^2)
A	143	a DC bias voltage applied to a diode in C-V measurements. (V)
a	159	effective ionization parameter, see equation (C.4). (m^{-1})
A_0	82	a constant defining the parabola in equation (5.14).
A_1	82	a constant defining the parabola in equation (5.14).
a_l	18	location of left sweeping-out boundary. (μm)
a_n	158	electron ionization parameter, see equation (C.1). (m^{-1})
a_p	158	hole ionization parameter, see equation (C.1). (m^{-1})
a_r	18	location of right sweeping-out boundary. (μm)
B	15	a mobility ratio: $(\mu_n - \mu_p)/(\mu_n + \mu_p)$.
B	143	amplitude of a sine-wave voltage applied in C-V measurements. (V)
b	159	effective ionization parameter, see equation (C.1). (V/cm)
b_n	158	electron ionization parameter, see equation (C.1). (V/cm)
b_p	158	hole ionization parameter, see equation (C.1). (V/cm)
BV_{non}	26	breakdown voltage of a non-punch-through structure. (V)
BV_{pt}	25	breakdown voltage of a punch-through structure. (V)
C	29	a capacitance. (F)
C_p	167	specific heat capacity. (J/gK)
C_{th}	167	thermal capacity. (J/K)
d	15	one-half of the width of the s (or i) middle layer. $d = W/2$. (μm)
D	16	ambipolar diffusion coefficient, defined by equation (2.5). (cm^2/s)
D_d	61	dopant diffusion constant. (cm^2/s)
DFn	63	designator for a diffused structure.
D_n	16	electron diffusion coefficient (cm^2/s)
D_p	6	hole diffusion coefficient. (cm^2/s)
E	20	electric field. (V/cm)
E_{bulk}	119	the electric field in the bulk of the middle s-layer. (V/cm)

E_c	25	critical electric field. Electric field at junction at breakdown. (V/cm)
E_{c0}	51	empirically determined constant in equation (4.10). (V/cm)
EPn	63	designator for an epitaxial structure.
f	118	defined by equation (8.22).
g	70	a unitless parameter defined by equation (5.4).
i	11	intrinsic region.
I	64	a current. (A)
I_0	125	the critical current, at which $f = 1$. (A)
I_{BIAS}	1	forward bias current in a SRD or WFSRD. (A)
I_f	125	forward bias current. (A)
I_L	143	leakage current. (μA)
I_R	162	reverse current during storage time. (A)
J_0	120	the critical current density, at which $f = 1$. (A/mm^2)
J_{diff}	118	diffusion current density. (A/mm^2)
J_F	15	forward bias current density, I_f/A . (A/mm^2)
J_n	116	electron current density. (A/mm^2)
J_p	116	hole current density. (A/mm^2)
J_R	5	reverse current density. (A/mm^2)
K	25	a constant, $4010 \text{ V cm}^{-5/8}$.
L	29	an inductance. (H)
L	42	thickness of a wafer. (μm)
L_d	6	characteristic diffusion length of injected charge carriers. (μm)
M	51	empirically determined constant in equation (4.10). (unitless)
M	159	ionization multiplication factor.
N	25	doping of the s (or i) middle layer. (cm^{-3})
$n(x)$	15	electron density. (cm^{-3})
n^+	11	heavily-doped n-type region.
N_1	161	doping profile to the left of the junction. (cm^{-3})

N_2	161	doping profile to the right of the junction. (cm^{-3})
N_A	161	acceptor density. (cm^{-3})
N_{A-}	68	ionized acceptor density. (cm^{-3})
n_{avg}	18	average carrier density in intrinsic layer. (cm^{-3})
N_B	42	background doping. (cm^{-3})
N_D	5	donor density. (cm^{-3})
N_{D-}	68	ionized donor density. (cm^{-3})
N_{eff}	38	an effective doping, as defined by equation (3.2). (cm^{-3})
N_S	42	surface doping. (cm^{-3})
N_{S1}	42	left surface doping. (cm^{-3})
N_{S2}	42	right surface doping. (cm^{-3})
$p(x)$	16	hole density. (cm^{-3})
p^+	11	heavily-doped p-type region.
p_0	69	mobile hole density in the space-charge region. (cm^{-3})
P_{avg}	169	average dissipated power. (W)
q	5	electron charge. (C)
Q	85	integrated charge density. (C/m^2)
Q	142	quality factor.
Q_-	126	charge removed by reverse bias. (C)
Q_+	125	charge stored by forward bias. (C)
Q_{impl}	96	dose of ion-implanted impurities. (cm^{-2})
Q_N	83	net charge density at $x = x_0$. (C/m^3)
Qn	151	a transistor.
R	29	a resistance. (Ω)
R_L	3	load resistance, usually 50 Ω .
R_T	167	thermal resistance. (K/W)
s	11	lightly-doped region, either p or n type.
s	114	the Laplace s-coordinate variable
t	11	time. (ns)

T	113	time normalized to τ .
T	168	temperature. (K)
t_d	123	the time at which double injection begins. (ns)
t_{EST}	89	predicted switching speed for a WFSRD. (ns)
t_F	3	pulse width of the forward bias pulse, for a DSRD. (ns)
t_R	1	switching time and/or rise time. (ns)
t_{RR}	11	reverse recovery time. $t_s + t_R$. (ns)
t_s	11	storage time. (ns)
t_T	126	diode transit time. (ns)
V_1	51	empirically determined constant in equation (4.10). (V)
V_{bias}	29	a circuit voltage, see Figure 3.1. (V)
V_{BR}	2	breakdown voltage. (V)
V_{BR0}	51	first iteration result when calculating V_{BR} . (V)
V_{CEsat}	151	collector-emitter saturation voltage. (V)
V_d	143	diode voltage.
V_F	11	forward bias applied across a diode and load. (V)
V_{IN}	1	maximum positive input voltage to a pulse-sharpening circuit. (V)
V_{max}	29	a circuit voltage, see Figure 3.1. (V)
V_{OP}	1	operating voltage. Maximum reverse bias applied by a circuit to a SRD. (V)
V_R	11	reverse bias applied across a diode and load. (V)
v_R	70	charge removal velocity. (cm/s)
V_{RAMP}	1	diode voltage immediately before the fast transient starts. (V)
v_s	5	saturation velocity of electrons and holes, approximately 10^7 cm/s for silicon.
V_T	117	thermal voltage, kT/q . (V)
W	24	width of the s (or i) middle layer. $W = 2d$. (μm)
W_{DR}	39	width of the depletion region. (μm)

WF	127	width factor, W normalized to the width of the depletion region at V_{BR} in a non-punchthrough structure.
W_L	113	width of the s (or i) middle layer normalized to L .
W_Q	125	distance between the p ⁺ n junction and the meeting point of the sweeping-out boundaries. (μm)
X	113	distance normalized to L .
x^*	159	dummy integration variable. (μm)
x_0	82	the location of the apex of the parabola defined in equation (5.14). (μm)
x_1	39	location of the left edge of the depletion region. (μm)
x_2	39	location of the right edge of the depletion region. (μm)
x_s	43	location of high-low junction, defined by equation (4.14). (μm)
x_{mj}	43	location of the metallurgical junction. (μm)
x_{p0}	69	the location of the high-low junction. (μm)
z	162	dummy variable.
Z_{OUT}	105	output impedance of a voltage source. (Ω)

Chapter 1 - Introduction

1.1 - Motivation

Step recovery diodes (SRDs) have remained extremely useful in wave-shaping applications in the three and a half decades since they were first presented [Boff60]. [Moll62]. No other device rivals their combination of fast switching speed and ease of use. Figure 1.1 shows the typical circuit configurations for SRD pulse sharpening. In both circuits, the SRD is initially biased with a constant forward bias current I_{BIAS} , which stores charge in the SRD. When the voltage source V_{IN} rises, reverse biasing the SRD, the SRD conducts for a short period of time, removing the stored charge. This keeps the voltage across the diode very low. Then the stored charge is abruptly exhausted, and the SRD switches to a high-impedance, high-voltage state, resulting in a sharpening of the output voltage waveform.

Fall time sharpening (or pulse width control)

Rise time sharpening (or delay control)

Figure 1.1 - Standard step recovery diode pulse sharpening circuits.

Unfortunately, conventional step recovery diodes are somewhat limited in their maximum breakdown voltages. Most commercially available SRDs have breakdown voltages of less than 100V, since the switching times tend to increase rapidly with rated voltage. Table 1.1 surveys commercial offerings, and illustrates this problem. Table 1.1 lists the three main figures of merit that are used in this thesis to evaluate SRDs: the operating voltage, V_{OP} (which, except for the A8.6 and MA44952, is taken to be V_{RR}), the time-rate-of-change during the step recovery, given approximately by V_{OP}/t_R , and the maximum effective carrier lifetime τ_{EFF} . Table 1.1 contrasts the commercial offerings with the experimental SRDs discussed in this thesis, and clearly shows the desirable fast switching speeds and long lifetimes of the experimental diodes.

It is of great interest to extend the voltage range of SRDs, to allow their use in high-voltage pulse generators.

This thesis considers methods of designing high-voltage SRDs, for operation from several hundreds of volts to several kilovolts. One entirely new method is presented, and results from fabricated devices are reported. A second (previously proposed) method is also considered in detail. The existing design theory is shown to be incomplete, and is greatly extended by the work presented here. This new theory is compared to experimental results obtained elsewhere, and to simulations presented here

Table 1.1 - Commercially Available SRDs. Note the rapid increase in switching time with breakdown voltage. (The data for the last four diodes are measured values, the other data was obtained from the manufacturers' data books.)

Manufacturer [Ref]	Part No.	Diode Type	V_{OF} (V)	t_R (ns)	V_{OF}/t_R (V/ns)	τ_{EFF} (ns)
Hewlett Packard [HP90]	5082-0020	SRD	25	0.06	417	20
Hewlett Packard [HP90]	5082-0021	SRD	40	0.1	400	100
Hewlett Packard [HP90]	5082-0017	SRD	75	0.3	250	300
Alpha [Alpha92]	DVB6104-06	SRD	75	0.4	187	100
M/A-COM [MACO88]	MA44753	SRD	100	1.0	100	150
M/A-COM [MACO88]	MA44750	SRD	180	3.0	60	500
M/A-COM [MACO88]	MA44952	multiple series SRD	300	1.0	300	195
experimental [Chapter 7]	A8.6	WFSRD	300	0.9	333	4500
experimental [Chapter 7]	A8.PT.850.1	WFSRD	300	0.6	500	950
experimental [Foci96]	"Type II"	DSRD	1700	5.0	340	250

1.2 - New Approaches for Step Recovery Diodes

Traditional SRDs are constructed with an epitaxial p-i-n structure [Moll69]. The middle i-layer is kept quite narrow, so that all of the charge injected by a forward bias is stored close to the two junctions. This ensures that most of the stored charge is removed while the voltage that has accumulated across the expanding space charge regions is low. In other words, the narrow width ensures that the dynamic punch-through voltage is low relative to the operating voltage. After punch-through occurs, a significant electric field exists throughout the entire i-layer and any remaining mobile carriers are rapidly swept out, causing the voltage across the diode to "snap" to its final value.

The abrupt-epitaxial structure with an intrinsic layer has some drawbacks. During the removal of the stored charge, the space-charge regions in the i-layer consist solely of mobile carriers. No fixed charge is present to compensate the mobile carriers. As a result, the electric field gradients will be relatively steep, thus requiring a narrow i-layer to achieve a low punchthrough voltage. Also, the abrupt junction will have a relatively low breakdown voltage, compared to graded junctions.

For these reasons, this thesis considers two different approaches for designing SRDs. Each approach focuses on a different aspect of the SRD, and the two approaches are in a sense "orthogonal". These two approaches are believed to be the only practical methods currently available for designing high-voltage, single-device SRDs.

The first approach attempts to reduce the steep electric field gradients by using a diffused doping profile. One advantage of this is obvious: higher breakdown voltages can be obtained with a diffused profile. Also, by using a diffused profile, a lower punch-through voltage can be obtained (under certain conditions). The reason for this is that rather than developing steep, narrow electric field profiles at the junctions, lower, wider, electric field profiles develop due to the charge-compensating effect of the doping.

It is well known that in theory [Benda67] and experiment [Chud95b], [Appendix B], diffused high-voltage power diodes will have a “snappier” reverse recovery transient than epitaxial diodes. However, snappiness in power diodes has generally been treated as an undesirable phenomena, rather than as a useful wave-shaping effect [Roul90]. Indeed, virtually all modern power diodes are constructed with epitaxial structures to guarantee a smooth reverse transient. This thesis considers the snappiness of diffused power diodes as a useful effect, and for the first time presents a design theory and experimental results for the use of these diodes as high voltage SRDs. These new diodes are termed “wide-field step recovery diodes”, or WFSRDs for short.

The second approach focuses on keeping the stored charge near the (abrupt) diode junctions. In traditional SRDs the forward bias is nearly steady-state, and the diodes rely on a narrow i-layer to keep the charge in close proximity to the junctions. Grekhov has proposed a new SRD, called the “drift step recovery diode” (DSRD), that uses pulsed forward biasing [Grek85], [Grek89], [Belk94]. If the duration of the pulse is much less than the carrier lifetimes, the carriers will be concentrated very close to the junctions. This has produced some very fast switching. 1700 V transitions into 50 Ω have been reported with less than 2 ns transition times [Grek85]. (The concept of pulsed biasing to achieve concentrated charge injection has also been demonstrated in very-high-power thyristor-like devices [Grek83], [Gorb88].)

However, only two design equations are presented in [Grek85], one being:

$$J_R = q v_s N_D \quad (1.1)$$

which relates the reverse current density J_R to the lightly-doped layer doping N_D . The other is:

$$t_F \ll \frac{L_d^2}{D_p} \quad (1.2)$$

which limits the forward bias pulse width to a fraction of the base transit time.

By assuming that the diode is operated at voltages near the breakdown voltage V_{BR} , one can write:

$$J_R A = \frac{V_{BR}}{R_L} \quad (1.3)$$

where A is the cross-sectional area and R_L is the load resistance (generally 50Ω). Also, the breakdown voltage is a function of the doping. In mathematical terms,

$$V_{BR} = f(N_D) \quad (1.4)$$

By combining the design equation (1.1) with (1.3) and (1.4), one can determine the optimum values of A and N_D for a given V_{BR} . However, this information is not sufficient to design the diode structure or to choose the ideal biasing conditions. In particular, the optimum lightly-doped layer width can not be predicted (and hence, through (1.2), neither can the maximum storage time), nor can the ideal forward biasing current level.

By considering in detail the nature of the forward transient in the DSRD, new results are developed in this thesis that allow these important parameters to be derived.

1.3 - Remarks on the Philosophy Adopted in This Study

Before beginning to discuss the theoretical aspects of this thesis, it is important to first note the approach taken by this author. The SRDs discussed in this thesis have been

studied and developed for the intended application of waveshaping in pulse generators. As such, the primary goal of this thesis is to develop relatively simple (or at least easily computable) expressions for engineering purposes, rather than exact descriptions of the underlying physics.

Given the practical orientation of this thesis, some effort is also devoted to considering the fact that the step-recovery effects described here already occur (unintentionally) in some commercial devices. The properties of these non-optimized diodes are considered, since they may prove to be more economical than custom-built devices, and since they provide insight into the step recovery mechanism.

Most of the common simplifying assumptions in diode physics, such as the low-injection, high-injection, or abrupt-junction assumptions will not apply here, and as such, computer simulations were used as a primary tool in this study. In particular, many diode simulations were run using MEDICI, a powerful large-signal semiconductor simulator. Insofar as the physical diode structures were described accurately to the simulator, the simulations are believed to take into account all significant effects (e.g., the variation of lifetimes with injection level, concentration-dependent mobilities, etc.). All simulated structures used conservative gridding, at the expense of longer computation time, to ensure accuracy.

Since the WFSRD is an entirely new device, working devices have been fabricated and tested for this thesis in order to validate the design theory. In the case of the DSRD, experimental results have been presented elsewhere so devices have not been fabricated. Instead, the new theoretical results are compared to the reported results, and to computer simulations.

1.4 - Main Contributions

This thesis examines two methods of obtaining high-voltage SRDs. The following contributions are related to the first method:

1. A new step-recovery mechanism is proposed, which relies upon a diffused doping structure. Methods of optimizing this structure are provided.
2. A new method of estimating the breakdown voltage of diffused rectifiers is presented. This empirical method has a wide range of applicability.
3. This new step-recovery phenomenon is shown to be present in certain obsolete commercially-produced diffused ultrafast rectifiers. The limitations imposed by the fact that these diodes are not optimized for use as SRDs are discussed.
4. Optimized diodes based on this new effect are fabricated and demonstrated for the first time. These diodes are shown to exhibit very long lifetimes and extremely fast switching speeds, making them highly desirable for pulse sharpening applications.

The contributions described in points 1 and 4 have been summarized and accepted for publication [Chud96a].

The following contributions are related to the second method:

5. The existing design theory for DSRDs is shown to be inadequate for designing an optimal device. A new, more complete design theory is proposed, which uniquely specifies an optimum device for a given operating voltage.

6. A new expression is derived for the evolution of the charge carrier densities in a pin diode during the forward transient. The new expression is considerably more compact than the conventional one.

Portions of the contributions described in points 5 and 6 have been summarized and accepted for publication (subject to minor revision) [Chud96b].

The following contributions are related to instrumentation and measurement issues:

7. A new, simple, low cost method of measuring C-V curves at kilovolt voltages, for the purposes of determining doping profiles, is presented. This contribution has been summarized in [Chud95a].
8. A new high-speed pulse amplifier configuration was developed for use in reverse-recovery t_{RR} measurements. This contribution has been summarized in [Chud95b].

1.5 - Organization

Chapter 1 is the introduction. Chapter 2 is a review of diode reverse transient physics, including both SRDs and power rectifiers.

Chapters 3 to 6 deal with the new diffused step recovery diode. Chapter 3 discusses experimental results from commercially available diodes. It is shown that some (but relatively few) obsolete ultrafast rectifiers can be used as high voltage SRDs, but with definite limitations. From high-voltage C-V measurements, it is shown that all of the diodes that act as SRDs have a diffused structure. As a prelude to developing a full design theory for the diffused high voltage SRDs, Chapter 4 presents a new method of estimating the breakdown voltage of diffused rectifiers. Chapter 5 develops the switching theory for the WFSRDs, and uses these results and those of Chapter 4 to propose a design

for a 300 V WFSRD. The fabrication method for this diode is documented in Chapter 6. Experimental results are presented in Chapter 7.

Chapter 8 discusses the existing design theory for DSRDs. It is shown that by examining the nature of the forward bias transient, a new design theory can be developed that permits a more optimal design. These results are compared to previously reported experimental results, and to simulations.

Chapter 9 contains the concluding remarks.

Appendix A discusses the instrumentation developed to allow C-V measurements to be made at kilovolt voltages.

A very fast, medium-voltage dc-coupled non-linear pulse amplifier circuit is presented in Appendix B. This pulse amplifier configuration is shown to be very useful for making fast reverse-recovery lifetime measurements.

Appendix C examines the relationship between the maximum electric field at breakdown, E_C , with the breakdown voltage V_{BR} from a theoretical standpoint. This compliments the empirical discussion presented in Chapter 4.

Appendix D discusses the relationship between the WFSRD switching time and the carrier lifetimes.

Chapter 2 - Review of Diode Reverse Transient Physics

2.1 - Introduction

It is well known that when the current through a diode is reversed from forward bias to reverse bias the voltage across the diode does not change instantaneously from a positive voltage to a negative voltage, due to the stored charge in the diode junction. Typical current transients for the circuit of Figure 2.1 are shown in Figures 2.2a and 2.2b. The diode structure can be designed to tailor the reverse recovery transient. For instance, step recovery diodes are designed to achieve a long storage time, t_s , and an extremely short fall time, t_r . In contrast, power rectifiers are generally designed to minimize the total length of the reverse recovery transient, $t_{RR} = t_s + t_r$ and to minimize t_s/t_r .

Figure 2.1 - Reverse recovery test circuit

The ubiquitous high voltage power rectifier and the step-recovery diode (SRD) share a common structure, that of the $p^+ i n^+$ (or just "pin") diode. The ideal pin diode consists of an intrinsic layer sandwiched between a heavily doped p-type (" p^+ ") region and a heavily doped n-type (" n^+ ") region. In practice this is difficult to achieve, so a psn diode is used, where "s" represents the lightly-doped middle layer, which can be p or n-type, sandwiched between the p^+ and n^+ regions. Both epitaxial structures (Figure 2.3) and diffused structures (Figure 2.4) are common.

Figure 2.2a - Ideal reverse recovery transients for a step recovery diode.

Figure 2.2b - Ideal reverse recovery transients for a power rectifier.

Figure 2.3 - Typical epitaxial diode structure

Figure 2.4 - Typical diffused diode structure

Despite the similar underlying structures in the SRD and the power rectifier, these two devices have developed as separate areas of study. This is due to two factors. First, as will be explained later, the conditions necessary to achieve the fast-transition characteristic of conventional SRDs require a relatively narrow s-layer, typically several microns. In contrast, power rectifiers are required to support large reverse voltages (i.e. hundreds of volts), which demands an s-layer width of several tens of microns. Secondly,

the fast transition (short t_q) that the SRD is designed to achieve is generally unwanted in power rectifier applications. Sudden current transitions can lead to large inductive voltages in power circuits. Also, the entire reverse recovery transient is undesirable in power applications, as it is a source of power loss. As a consequence, considerable effort has been expended by device designers to suppress the possibility of SRD-like fast switching in power rectifiers by minimizing t_{RR} and, within that constraint, maximizing t_R . (For examples, see [Amem82], [Coop83], [Shim84], [Howe88], [Mori92], and [Mehr93]).

Virtually no effort has been spent considering the possibility of optimizing power rectifier structures to achieve the opposite behavior; that is SRD-like switching behavior for other applications, such as in high-voltage pulse generators. Commercially available SRDs with sub-nanosecond transition times are generally not available with breakdown voltages of more than 100V. Experimental evidence presented in Chapter 3 suggests that it is possible to design power rectifiers that can switch several hundreds of volts into a 50 Ω load in approximately 1 ns. Chapters 5 to 7 of this thesis investigate this possibility.

2.2 - Review of Power Diode Switching Principles

2.2.1 - Principles of Power Rectifier Operation - pin Diodes

Pin and psn diodes with abrupt junctions have been extensively studied in the literature. This section summarizes the essential characteristics of pin diodes, and largely follows the pioneering work of Benda and Spenke [Bend67] (as do Sections 2.2.2 and 2.2.3).

Figure 2.5 shows an ideal pin diode structure, which will be considered here. For the purpose of illustrative calculations, the following conditions will be assumed:

$$\tau = 500 \text{ ns}$$

$$d = 30 \mu\text{m}$$

$$\mu_n = 1350 \text{ cm}^2/\text{Vs}$$

$$\mu_p = 480 \text{ cm}^2/\text{Vs}$$

$$J_F = 200 \text{ mA/mm}^2$$

In forward bias, it can be shown [Bend67] that the carrier distribution in the quasi-neutral middle layer can be written as

$$n(x) = \frac{\tau \cdot J_F}{2 \cdot q \cdot L_d} \cdot \left(\frac{\cosh \frac{x}{L_d}}{\sinh \frac{d}{L_d}} - B \frac{\sinh \frac{x}{L_d}}{\cosh \frac{d}{L_d}} \right) \quad (2.1)$$

Figure 2.5 - pin doping structure and carrier densities

This expression is exact for pin diodes and approximate for psn diodes. Since, by definition, the middle region of the pin diode is under high injection, the carrier concentrations are approximately equal, that is

$$p(x) \approx n(x) \quad (2.2)$$

The lifetime τ in (2.1) is the high-level ambipolar lifetime [Ghan77].

$$\tau = \tau_{n0} + \tau_{p0} \quad (2.3)$$

and the diffusion length L_d is

$$L_d = \sqrt{D \cdot \tau} \quad (2.4)$$

where D is the high-level ambipolar diffusion constant, given by

$$D = \frac{2 \cdot D_n \cdot D_p}{D_n + D_p} \quad (2.5)$$

Benda and Spenke have also analytically solved the time evolution of the carrier distribution for a reverse transient, for the time when the middle region is still entirely quasi-neutral. The exact solution is lengthy and of little interest itself, but its solution is plotted for several different instants in Figure 2.6. The solution at $t = 0$ reduces to equation (2.1). The key observation relating to this thesis is that the carrier concentration falls to zero at the $p^+ i$ junction first, and much later at the $i n^+$ junction. This can be seen analytically by noting that the current at a $p^+ i$ junction is carried almost entirely by holes, and that while quasi-neutrality holds, no significant electric field can develop, so that

$$J(-d) \approx qD_p \frac{dp}{dx} \Big|_{x=-d} \quad (2.6)$$

and similarly

$$J(+d) \approx -qD_n \left. \frac{dn}{dx} \right|_{x=+d} \quad (2.7)$$

It is also evident that

$$J(-d) = J(+d) \quad (2.8)$$

Consideration of equations (2.2), (2.6), (2.7), (2.8) then gives

$$D_p \left. \frac{dn}{dx} \right|_{x=-d} = -D_n \left. \frac{dn}{dx} \right|_{x=+d} \quad (2.9)$$

Since $D_n \approx 3D_p$, the slope of the carrier concentration at $x = -d$ must be three times larger than that at $x = +d$ to satisfy (2.9); hence the concentration will fall to zero sooner at $x = -d$. This is clearly seen in Figure 2.6.

Once the charge distribution predicted by the analytical expression becomes negative, a space-charge region will develop. This space charge is maintained by mobile carriers in the intrinsic region, rather than by fixed ionized donors or acceptors. The assumption of quasi-neutrality can no longer be maintained after this time, and an exact analytical treatment is not available.

Figure 2.6 - Charge Removal in the i-Layer.

Benda and Spenke have analyzed the development of the space-charge regions by assuming that the boundary between the space charge regions and the quasi-neutral region in the intrinsic layer is very sharp, that is, there is a sudden discontinuous jump between the very small carrier concentration in the space-charge region and the very high quasi-neutral concentration. This concept is illustrated in Figure 2.7. The movement of these two boundaries can then be analyzed by assuming a constant reverse current, I_R . If one neglects recombination, and approximates the initial carrier concentration with a constant average concentration n_{avg} , it is straightforward to show that the right and left boundaries, $x = -a_l(t)$ and $x = +a_r(t)$, move with the velocities

$$\left| \frac{da_l}{dt} \right| = \frac{\mu_n}{\mu_n + \mu_p} \frac{I_R}{q \cdot n_{\text{avg}}} \quad (2.10)$$

and

$$\left| \frac{da_r}{dt} \right| = \frac{\mu_p}{\mu_n + \mu_p} \frac{I_R}{q \cdot n_{avg}} \quad (2.11)$$

respectively. Hence the space-charge region at the p+ junction expands approximately three times as fast as the one at the n+ junction, since $\mu_n/\mu_p \approx 3$.

Figure 2.7 - Schematic illustration of carrier removal [Benda67]

2.2.2 - Principles of Power Rectifier Operation - psn Diodes

The presence of light doping in the middle layer of the psn diode affects the spatial growth rate of the space-charge regions only minimally, but it has a strong influence on the voltage development in these space-charge regions. For instance, if the doping is n-type, the space charge at the p+ n junction can be composed of the fixed ionized donors, rather than mobile charge. When this occurs, the voltage at this junction develops as $V \propto (-d + a_j(t))^2$. In contrast, if the doping is p-type, a high-low junction exists at $x = -d$. The space-charge must then be composed of mobile holes. Furthermore, this mobile hole concentration must be larger than the acceptor concentration, if a positive space charge is to be maintained. However, since

$$-I_R = q\mu_p p(x)E(x) \quad (2.12)$$

and since i_R falls and $E(x)$ rises as the reverse transient progresses, $p(x)$ must fall rapidly. (Neglecting diffusion current in (2.12) is generally justified, see Appendix 1 of [Benda67] for details.) However, $p(x)$ must remain larger than n_A in order for a positive space charge to exist. Thus if n_A is large, $p(x)$ will asymptotically approach n_A , and this region will act as an ohmic resistance. Then $V \propto (-d + a_1(t))$, so the voltage develops much more slowly than in the previous case. Whether or not this occurs depends on the relative sizes of $p(x)$ and n_A . If n_A is very small, an ohmic region will develop very late into the transient, where the current is very low, so this effect may not be visible.

The results of this section and the previous one in terms of the reverse recovery transient can be summarized as follows:

1. Space charge develops at the p^+ junction before it does at the n^+ junction.
2. The space charge region widens more rapidly at the p^+ junction than it does at the n^+ junction.
3. Voltage develops much more slowly at p^+p and n^+n junctions than at p^+n and $p n^+$ junctions.

These facts allow one to predict the relative differences between ps_pn and ps_nn diodes. In the ps_pn rectifier, the space-charge region (or "SCRs") develops first at the p^+p junction, so initially the voltage across the diode develops very slowly. Later, a space-charge region will develop at the $p n^+$ junction. Then, the voltage across the diode will increase moderately quickly. This is depicted in Figure 2.8.

Figure 2.8 - Reverse voltage development in a $p_s p_n$ rectifier.

In the $p_s n_n$ rectifier, the space-charge region develops first at the $p+n$ junction, so initially the voltage across the diode develops very rapidly. However, since the same amount of charge must be removed as in the case of the $p_s p_n$ rectifier, the voltage development will taper off and develop a long "tail". This is depicted in Figure 2.9.

Figure 2.9 - Reverse voltage development in a $p_s n_n$ rectifier.

This means that the ps_pn rectifier will have a short t_{RR} and a short t_r . Conversely, the ps_nn rectifier will have a long t_{RR} and a "softer" transient waveform, which as explained earlier, is desirable in most power rectifier circuits. For this reason, almost all modern commercially available power rectifiers are of the ps_nn type. Furthermore, it is easier to achieve high breakdown voltage in ps_nn rectifiers, since surface inversion can occur in the middle p-layer of ps_pn rectifiers [Grov65]. ps_nn rectifiers also have sharper breakdown "knees" than ps_pn rectifiers [Ghan77].

Before the widespread use of epitaxy, the only feasible method of rectifier production was diffusion. Thus older, obsolete diodes specified as ultra-fast rectifiers may use the ps_pn structure since, as noted above, it results in shorter t_{RR} times for an identical amount of stored charge relative to a ps_nn structure. However, the modern approach is to use a ps_nn structure with abrupt epitaxial boundaries, which reduces the total stored charge for a given forward current [Coop83]. Thus using epitaxy reduces both t_r and t_s , whereas using diffused ps_pn structures reduces t_r but increases t_s .

2.2.3 - Principles of Power Rectifier Operation - Diffused Diodes

The diffused rectifier will show a combination of the characteristics described in the previous two sections. Since the doping gradually varies from a very high level to a very low level near the junction, the edge of the swept-out region will initially be in the heavily doped region, and an ohmic region will develop as described in Section 2.2.2. A small voltage will be built up across this ohmic region. As the edge of the swept out region approaches the junction, the doping level will fall, and the situation will be more akin to the intrinsic doping case discussed in Section 2.2.1. At this time, a space charge region will develop, and the voltage will rapidly increase. A much more detailed discussion can be found in [Bend68].

Thus, a period of charge removal with little voltage buildup will be followed by a period of very rapid voltage buildup. This is in fact the sequence desired for a step recovery diode, although this mode of operation has not been exploited previously in SRDs.

2.3 - Review of Conventional Step Recovery Diode Switching Principles

As noted earlier, although SRDs share the same basic structure as power rectifiers, there is a difference of scale: the i-layer is generally more than an order of magnitude smaller for an SRD. In practice, this means that the boundary between the space-charge regions and the quasi-neutral regions can not be considered as abrupt. Instead, they are sloped, and the two sloped boundaries quickly overlap to form an approximately triangular carrier distribution, as shown in Figure 2.10. The following analysis follows the analysis presented by Roulston [Roul90].

Figure 2.10 - Carrier density and net charge evolution in an SRD [Roul90]

Figure 2.10 also shows the approximate net charge distribution in an SRD as the transient progresses. On the left side, the positive charge density can be estimated using

$$p = \frac{J_R}{q \cdot v_s} \quad (2.13)$$

The assumption has been made that the electric fields are high enough that the hole velocities are saturated. Similarly, on the right side the electron density is

$$n = \frac{J_R}{q \cdot v_s} \quad (2.14)$$

If the further assumptions are made that the space-charge regions begin to expand simultaneously, and that when the two space-charge regions overlap the current is still approximately J_R (which is characteristic of a good SRD), then the total voltage when the space-charge regions overlap can be estimated by using Poisson's equation. This gives:

$$\begin{aligned} V_{\text{RAMP}} &= \frac{(0.5W)^2 J_R}{v_s \epsilon} + \frac{(0.5W)^2 J_R}{v_s \epsilon} \\ V_{\text{RAMP}} &= \frac{W^2 J_R}{2v_s \epsilon} \end{aligned} \quad (2.15)$$

The left space-charge region is assumed to have expanded at the same rate as the right space-charge region, meaning that they meet at $x = 0.5 W$.

The fast transition characteristic of the SRD begins when the two space-charge regions overlap. At this moment, almost no free charge remains in the middle region to be evacuated, and the electric field "snaps" to support the final voltage. Since the voltage

development during the charge evacuation stage is comparatively slow, it is important that $V_{\text{RAMP}} \ll V_R$ for the transient to approach to ideal rectangular SRD waveform.

2.4 - Difficulties with High Voltage Step Recovery Operation

As noted earlier, the voltage development in the ps_{pn} rectifier is initially gradual, which is followed by a sudden rapid increase, similar in concept to the operation of an SRD. The voltage at which this occurs can be estimated from (2.15). However, since W must be large in power rectifiers to sustain a high breakdown voltage, and $V_{\text{RAMP}} \propto W^2$, it is difficult to design high voltage SRDs, at least according to the theory presented thus far.

Baliga [Bali87] reports that the breakdown voltage of an abrupt punch-through psn structure, BV_{pt} , can be estimated using

$$BV_{\text{pt}} = E_c W - \frac{qNW^2}{2\epsilon} \quad (2.16)$$

and

$$E_c = K \cdot N^{\frac{1}{8}} \quad (2.17)$$

where W is the width of the middle layer, E_c is the critical field at which avalanche breakdown occurs, N is the doping of the middle layer, and K is a empirical constant given by:

$$K = 4010 \text{ volt} \cdot \text{cm}^{-\frac{5}{8}} \quad (2.18)$$

If one substitutes (2.17) into (2.16), and takes the derivative of (2.16) with respect to N , one can calculate the optimum value of N for a given W that will maximize BV_{pt} .

This yields:

$$N = \left(\frac{K\epsilon}{4qW} \right)^{\frac{8}{7}} \quad (2.19)$$

Substituting (2.17) and (2.19) into (2.16) yields an expression for BV_{pt} in terms of the middle layer width:

$$BV_{pt} = \frac{7}{16} \left(\frac{32\epsilon K^8 W^6}{q} \right)^{\frac{1}{7}} \quad (2.20)$$

Punch-through diodes involve a trade-off between doping and width. For a given breakdown voltage, a punchthrough diode has a narrow middle layer, which improves forward conduction, but it also has lighter doping, which can be more difficult to fabricate than a non-punchthrough diode. Thus in practice, the optimum value may not be used.

Ghandi [Ghan77] reports that for a non-punchthrough abrupt pin structure, the breakdown voltage BV_{non} , in volts, can be related empirically to the depletion width by

$$W = \left(2.57 \times 10^{-2} \mu\text{m} \cdot \text{volt}^{-\frac{7}{6}} \right) \cdot (BV_{non})^{\frac{7}{6}} \quad (2.21)$$

Equations (2.15), (2.20) and (2.21) are compared in Figure 2.11. For the purposes of equation (2.15) a current density of 6 A/mm^2 has been assumed. (This current density corresponds to a 300V transient into a 50Ω load, with a 1 mm^2 diode.) For reasons noted above, the actual breakdown voltage will fall between BV_{pt} and BV_{non} . Figure 2.11 clearly shows that V_{RAMP} rapidly becomes a significant portion of the breakdown voltage. SRD are typically either specified in terms of the 20% to 80% or the 10% to 90% transition time, so it is important to keep $V_{RAMP} < 0.2 \text{ BV}$. For the optimum punchthrough diode, $V_{RAMP} = 0.2 \text{ BV}$ at $BV = 200 \text{ V}$. Beyond this point on the graph, the breakdown

voltages rise almost linearly, but V_{RAMP} rises quadratically, so higher voltage SRDs based on the abrupt-psn structure rapidly become impractical. For instance, for a diode designed to operate at 300 V, and having a breakdown voltage of 500V, no fast transient is predicted at all.

Figure 2.11 - A comparison of ramp voltage V_{RAMP} and corresponding breakdown voltages for punchthrough and non-punchthrough pin structures.

The curve for V_{RAMP} in Figure 2.11 has been plotted assuming a constant cross-sectional area, however equation (2.15) apparently offers the possibility of reducing V_{RAMP} for high voltage structures by increasing A and hence reducing J_r . Unfortunately, this leads to an increased parasitic capacitance, which is highly undesirable. This issue will be discussed in later chapters.

Perhaps the best illustration of the difficulty of building step recovery diodes with high breakdown voltages is to simply survey the commercial offerings, as was done in Table 1.1. This table clearly shows the increase in transition rates at higher voltages.

Chapter 3 - Experimental Evidence from Commercial Devices

3.1 - Introduction

Most of the theory outlined in the previous chapter assumes that the pin or psn structures have abrupt doping boundaries. Virtually all reverse transients studies have been restricted to abrupt boundary devices, due to the simple mathematical boundary conditions that these devices offer. This structure is in fact the optimum structure for low voltage SRDs [Moll69] since it concentrates the stored charge in a narrow layer where it is easily removed. Power rectifiers on the other hand, often take advantage of the higher breakdown voltages possible with diffused junctions, which are poorly approximated by abrupt boundaries. (However, as noted before, there has been a move to power rectifiers with abrupt junctions, to reduce the stored charge.) Experimental evidence from several obsolete rectifiers presented below indicates that certain diffused structures can exhibit good step recovery characteristics. Computer simulations, presented later, have confirmed this. While previous theories predict qualitatively that voltage development across a diffused rectifier may occur with a period of slow voltage development followed by a rapid step-recovery-diode-like transient, no studies have predicted that the entire voltage swing (i.e. 10% - 90%) can occur via the step recovery transient.

3.2 - Experimental Observations With Commercial Diodes

As mentioned above, certain commercially produced power rectifiers have been observed to exhibit step-recovery action. It is important to note that this phenomenon was not intentional, that is, the diodes were not specified to exhibit step recovery. Most rectifiers specify only t_{RR} , rather than t_S and t_R , so it is generally impossible to judge a rectifier's step recovery action without experimentation. This step-recovery action was observed by this author in the course of proprietary pulse generator research and

development before this thesis began, but has not been satisfactorily explained previously.

Figure 3.1 shows a typical SRD circuit, with ideal waveforms. This circuit is typically used in a pulse generator to sharpen the pulse fall time using low-voltage SRDs. The diode is normally forward biased by a DC current through the two inductors. Initially, the intrinsic region of the pin SRD is swamped with electrons and holes, providing a high conductivity path through the diode. When the input pulse reaches the diode the diode initially stays in conduction, so the output voltage follows the input voltage. However, in a good SRD, the stored charge in the intrinsic layer will quickly fall and the electric fields will suddenly increase, as discussed earlier. The diode will then develop the full reverse voltage across it, and act as an open circuit, so the output voltage will fall to zero.

This section reports the results of tests where the SRD of Figure 3.1 is replaced with a commercially available power rectifier. In this test voltages much higher than those used in normal SRD applications were used. Specifically,

- $V_{\max} = 300\text{V}$ (thus $I_R = 6\text{ A}$)
- V_{bias} = varied to obtain best waveform, see Table 3.1
- $R = 50\ \Omega$
- $L = 200\ \mu\text{H}$
- $C = 0.1\ \mu\text{F}$

For these tests, a specially modified Avtech avalanche-transistor-based pulse generator was used as the signal source. The unit was modified so that the output stage of the pulse generator was replaced with the sharpening stage of Figure 3.1, and the distance between the Avtech output and the sharpening circuit was kept as small as possible, to minimize the possibility of undesirable transmission line reflections. The purpose of this sharpening stage is to reduce the fall time (and pulse width) of the input pulse (see Figure

1.1). Figure 3.2 shows the output waveform with no sharpening stage added (thus it is essentially the input waveform when the sharpening stage is added, if reflections are ignored).

Figure 3.1 - Step Recovery Test Circuit

A wide range of commercially produced diodes were tested. All of those that exhibited step recovery action, and a small fraction of the comparable diodes that did not are listed in Table 3.1. Interestingly, the breakdown voltages of most of the diodes were extremely conservatively rated.

Table 3.1 - Results of Experiments on Commercially Produced Diodes

Diode Specifications	Diode No.	I_{BIAS} (mA)	V_{BR} (Volts)	Shows step Recovery?	Obsolete
$V_{BR} = 200 \text{ V}$, $t_{RR} = 150 \text{ ns}$	13	200	> 1400	No	No
$V_{BR} = 200 \text{ V}$, $t_{RR} = 200 \text{ ns}$	103	200	1000	No	No
$V_{BR} = 200 \text{ V}$, $t_{RR} = 200 \text{ ns}$	100	200	970	No	No
$V_{BR} = 200 \text{ V}$, $t_{RR} = 200 \text{ ns}$	47	200	800	Yes	Yes
$V_{BR} = 600 \text{ V}$, $t_{RR} = 200 \text{ ns}$	89	80	750	Yes	No
$V_{BR} = 400 \text{ V}$, $t_{RR} = 20 \text{ ns}$	88	500	510	Yes	Yes

Figure 3.2 - Output of pulse generator (158 V/div, 5 ns/div)

Figure 3.3 - Output pulse when sharpened with diode 13. (158 V/div, 5 ns/div)

Figure 3.4 - Doping profile of diode 13. Note the very wide epitaxial layer, bounded by a highly doped substrate.

Figure 3.5 - Output pulse when sharpened with diode 103. (158 V/div, 5ns/div)

Figure 3.6 - Doping profile of diode 103. Note the moderately wide epitaxial layer, bounded by a highly doped substrate.

Figure 3.7 - Output pulse when sharpened with diode 100. (158 V/div, 5ns/div)

Figure 3.8 - Doping profile of diode 100. Note the moderately wide epitaxial layer, bounded by a highly doped substrate.

Figure 3.9 - Output pulse when sharpened with diode 47. (158 V/div, 5ns/div). Note the SRD-like pulse sharpening.

Figure 3.10 - Doping profile of diode 47. Note the diffused profile.

Figure 3.11 - Output pulse when sharpened with diode 89. (158 V/div, 5ns/div). Note the SRD-like pulse sharpening.

Figure 3.12 - Doping profile of diode 89. Note the diffused profile.

Figure 3.13 - Output pulse when sharpened with diode 88. (158 V/div, 5ns/div). Note the SRD-like pulse sharpening.

Figure 3.14 - Doping profile of diode 88. Note the diffused profile.

Figures 3.3, 3.5, etc., show two distinct types of diode transient behavior. The diodes numbered 13, 103, and 100 show no step recovery response. The voltage outputs, and hence the diode impedances, change quite gradually. In contrast diodes 47, 88, and 89 show step responses, where the diode initially conducts, and the output looks quite similar to the input. Then the diodes switch off rapidly, and the output voltages have fall times on the order of 2 ns. These diodes, which are not optimized for step recovery operation, already show better performance than the M/A-COM diode MA44750 listed in Table 1.1!

(All oscilloscope measurements in this thesis were performed using a Tektronix S4 sampling head in a 7S11 sampling unit, with a 7T11 time base, in a 7704 mainframe. The S4 sampling head has a bandwidth of 14 GHz. Where applicable, all rise and fall times measurements are 10%-90% values.)

Tellingly, two of the three diodes that were tested and exhibited step recovery were obsolete, all were fast rectifiers, and one (diode 88) was rated as an extremely fast rectifier. This, for reasons explained in section 2.2.2, strongly suggests that these diodes are ps_n diffused rectifiers. One part of this hypothesis is easily confirmed using C-V measurements.

For each of the diodes listed in Table 3.1, C-V plots were obtained using the circuit described in Appendix A. This novel C-V profiling instrument allowed measurement over the entire reverse bias range, which ranged down to -1400V for some diodes. From these C-V profiles, the effective doping profile $N_{eff}(W)$ was plotted for each diode, using [Moll64]

$$\frac{dC}{dV} = \frac{C^3}{q\epsilon A^2 N_{eff}} \quad (3.1)$$

where

$$\frac{1}{N_{\text{eff}}(W_{\text{DR}})} = \frac{1}{|N(x_1)|} + \frac{1}{|N(x_2)|} \quad (3.2)$$

and

$$W_{\text{DR}} = x_2 - x_1 \quad (3.3)$$

In these equations, W_{DR} represents the width of the depletion region, x_1 and x_2 represent the location of the edges of the depletion region, C is the measured capacitance and V is the applied bias. Hence, knowing the variation of C with V allows $N_{\text{eff}}(W_{\text{DR}})$ to be plotted against W_{DR} . For each diode, the cross-sectional area was estimated by visual inspection using a microscope.

These doping profiles clearly show that the diodes that exhibit high-voltage step recovery also have diffused doping profiles, and those that do not show step recovery were epitaxially grown. These findings show that step recovery diodes can be made to operate at voltages significantly higher than those that have been developed previously, through the use of diffused-type profiles rather than the textbook abrupt profile.

3.3 - Usefulness of Commercial Diodes as High-Voltage SRDs

While several of the commercial diodes presented above do exhibit step recovery, their actual usefulness is somewhat limited. This is for two reasons. First, most of the diodes that exhibit this effect are now obsolete, probably reflecting the declining use of diffused profiles. Second, all of the diodes found to exhibit this effect were found to be fast or ultrafast rectifiers, meaning that the carrier lifetimes in the diodes have deliberately been made small. This is highly undesirable for pulse sharpening applications, as it increases the forward bias required to obtain a storage time of reasonable duration. For instance, Table 3.1 indicates that diode 88 was biased with 500 mA of current. This is a relatively large current to handle. The diodes presented in Chapter 7 are shown to require bias currents that are at least an order of magnitude

smaller for comparable storage times. However, these problems are somewhat mitigated by the fact that these commercial diodes are quite cheap, when available.

Table 3.2 lists the main figures of merit for the diodes of Table 3.1 that displayed step-recovery action, compared to the experimental diodes presented later. The effective lifetime, τ_{EFF} , is calculated from the formula:

$$\frac{t_s}{\tau_{\text{EFF}}} = \ln \left(1 + \frac{I_F}{I_R} \right) \quad (3.4)$$

where t_s is the diode storage time (i.e. the reverse conduction time, which is equal to the output pulse width in the waveforms presented above). This formula is based on a simple charge-control model [Neud89], [Moll62]. It should be noted that in this model the lifetime is not directly linked to any physical parameter like carrier lifetimes or transit times, so it is an “effective” lifetime. More rigorous formulas or numerical approaches for calculating diode storage time are available [King54], [Lax54], [Ko61], [Kuno64], [Bend67], [Rauh90], [Darl95], but equation (3.4) has the advantage of simplicity, and it allows direct comparison with the lifetime values presented in manufacturers’ data books [HP90].

Table 3.2 clearly shows the superiority of the optimally-designed diodes over those that show parasitic step recovery, on the basis of both speed and particularly effective lifetime.

Table 3 2 - Figures of merit for the diodes displaying step recovery action.

Diode No.	Diode Type	V_{OP} (V)	best switching time t_R (ns)	V_{OP}/t_R (V/ns)	τ_{EFF} , effective lifetime (ns)
47	"fast rectifier"	300	1.6	188	152
89	"fast rectifier"	300	1.2	250	340
88	"ultrafast rectifier"	300	1.8	167	69
A8.6	WFSRD	300	0.9	333	4500
A8.PT.850.1	WFSRD	300	0.6	500	950
"Type II"	DSRD [Foci96]	1700	5	340	250

Chapter 4 - Calculation of V_{BR} for Diffused Diodes

4.1 - Introduction

The purpose of this thesis is to develop step recovery diodes that can operate at voltages much higher than those currently available. Hence, they must also have higher breakdown voltages, and a rapid method for estimating V_{BR} is required. Despite the widespread use of diffused psn rectifiers (where the "s" represents a lightly doped region) few results have been published on calculating their breakdown voltage. Numerous authors [Koko66], [Warn72], [Wils73], [Bali87] have considered the breakdown voltage of single diffused junctions of the form:

$$N(x) = N_S \operatorname{erfc}\left(\frac{x}{\lambda}\right) - N_B \quad (4.1)$$

Bulucea [Bulu91] has extended this by calculating the breakdown voltages for low-voltage ps_nn rectifiers with both a single diffused p region and an epitaxial n region. However high voltage psn diodes often have two diffused regions, both of which influence the breakdown voltage.

This chapter considers the breakdown voltage of rectifiers with the structure shown in Figure 4.1, corresponding to:

$$N(x) = N_{S1} \exp\left(-\frac{x^2}{\lambda_1^2}\right) + N_B - N_{S2} \exp\left(-\frac{(x-L)^2}{\lambda_2^2}\right) \quad (4.2)$$

with $N(x) > 0$ taken to mean net acceptor doping, and $N(x) < 0$ net donor doping. N_{S1} and N_{S2} are the surface concentrations, and N_B is the wafer background doping. This structure

can be made in practice by implanting and diffusing p and n type dopants into opposite sides of a wafer of thickness L .

Figure 4.1 Doping profile of the devices considered in this chapter.

Although breakdown voltages can be calculated by numerically solving the ionization integrals using simulators such as Medici [Medi93], it is still of interest to have a simple, fast method of estimating the breakdown voltage for use in device optimization, particularly when several parameters must be optimized. A new method of estimating V_{BR} is presented in this chapter.

4.2 - Basic Method

Determining the breakdown voltage due to impact ionization to a high degree of precision is a task best suited to numerical simulation, given the nonlinear nature of the problem. However, it is fairly straightforward to obtain an estimate by assuming that breakdown occurs at a given critical electric field E_c , rather than by considering the field dependent ionization coefficients.

The breakdown voltage will be determined using the following assumptions:

1. Breakdown occurs when a given critical electric field E_c is exceeded at the metallurgical junction. The method of determining E_c is discussed below.
2. Avalanche breakdown is the only breakdown mechanism considered. Tunneling and thermal effects are not included. (The doping levels and gradient are much too low in the devices considered in this thesis for tunneling to be of any significance. The justification for ignoring thermal effects in this thesis is provided in Appendix E.)
3. The mobile charge in the space charge regions is negligible. Hence the space charge is determined entirely by the doping profile. This is a reasonable assumption for slowly-varying conditions or near the end of a reverse recovery transient. This assumption also implies that there is only one space charge region, with the electrostatic junction at the metallurgical junction x_{mj} .
4. The space charge region is assumed to have sharp boundaries at x_1 and x_2 , with $x_1 = x_{mj} < x_2$. This is the usual depletion region approximation.

If the metallurgical junction location is represented by x_{mj} , which can be determined by numerically solving (4.2) for $N(x_{mj}) = 0$ and given N_{Si} , $N_{Si'}$, N_B , λ_{-1} , λ_{+1} , and L , then the boundary x_1 (the left boundary) can be determined by using Poisson's equation and integrating the space charge between x_1 and x_{mj} , varying x_1 until the maximum electric field (which is at x_{mj}) is equal to the critical field. Analytically,

$$E_c = \left[\frac{q}{\epsilon} \int_{x_1}^{x_{mj}} -N(x) dx \right] \quad (4.3)$$

Substituting (4.2) gives

$$E_c = \frac{q}{\epsilon} \int_{x_1}^{x_m} \left[N_{S1} \exp\left(-\frac{x^2}{\lambda_1^2}\right) + N_B - N_{S2} \exp\left(-\frac{(x-L)^2}{\lambda_2^2}\right) \right] dx \quad (4.4)$$

Equation (4.4) can be rewritten as:

$$E_c = \frac{qN_B(x_{mj} - x_1)}{\epsilon} + \frac{q\sqrt{\pi}}{2\epsilon} \left[N_{S1}\lambda_1 \left(\operatorname{erf}\left(\frac{x_{mj}}{\lambda_1}\right) - \operatorname{erf}\left(\frac{x_1}{\lambda_1}\right) \right) + N_{S2}\lambda_2 \left(\operatorname{erf}\left(\frac{x_1-L}{\lambda_2}\right) - \operatorname{erf}\left(\frac{x_{mj}-L}{\lambda_2}\right) \right) \right] \quad (4.5)$$

The boundary x_1 can then be determined, knowing E_c and the doping profile factors (N_{S1} , N_{S2} , N_B , λ_1 , λ_2 , and L).

The boundary x_2 can be obtained by balancing the positive and negative space charge such that:

$$\int_{x_1}^{x_m} N(x) dx = - \int_{x_m}^{x_2} N(x) dx \quad (4.6)$$

Substituting (4.2) into (4.6) and evaluating the integrals yields:

$$(x_2 - x_1) \cdot N_B + \frac{\sqrt{\pi}}{2} \left[N_{S1}\lambda_1 \left(\operatorname{erf}\left(\frac{x_2}{\lambda_1}\right) - \operatorname{erf}\left(\frac{x_1}{\lambda_1}\right) \right) + N_{S2}\lambda_2 \left(\operatorname{erf}\left(\frac{x_1-L}{\lambda_2}\right) - \operatorname{erf}\left(\frac{x_2-L}{\lambda_2}\right) \right) \right] = 0 \quad (4.7)$$

Thus given x_1 and the doping profile factors, x_2 can be determined.

The breakdown voltage can then be calculated using

$$V_{BR} = - \int_{x_1}^{x_2} \int -\frac{q}{\epsilon} N(x) dx \quad (4.8)$$

If (4.2) is substituted into (4.8), one obtains

$$\begin{aligned} V_{BR} = & \frac{qN_B}{2\epsilon} (x_2 - x_1)^2 + \frac{qN_{s2}\lambda_2^2}{2\epsilon} \left[\exp\left(\frac{-(x_1 - L)^2}{\lambda_2^2}\right) - \exp\left(\frac{-(x_2 - L)^2}{\lambda_2^2}\right) \right] \\ & + \frac{qN_{s1}\lambda_1}{2\epsilon} \left[\sqrt{\pi} x_2 \left(\operatorname{erf}\left(\frac{x_2}{\lambda_1}\right) - \operatorname{erf}\left(\frac{x_1}{\lambda_1}\right) \right) + \lambda_1 \left(\exp\left(\frac{-x_2^2}{\lambda_1^2}\right) - \exp\left(\frac{-x_1^2}{\lambda_1^2}\right) \right) \right] \\ & + \frac{qN_{s2}\lambda_2\sqrt{\pi}}{2\epsilon} (x_2 - L) \left[\operatorname{erf}\left(\frac{x_1 - L}{\lambda_2}\right) - \operatorname{erf}\left(\frac{x_2 - L}{\lambda_2}\right) \right] \end{aligned} \quad (4.9)$$

Thus, given the doping profile of the diode and the critical electric field, the breakdown voltage can be determined.

This method relies heavily on the proper choice of E_C . Unfortunately, E_C is neither a physical parameter (i.e. the underlying solid-state physics is not described by E_C , rather it is governed by ionization coefficients), nor a constant. Empirical expressions relating E_C to doping parameters are available for the textbook cases of n+ p abrupt diodes and linearly graded diodes [Bali87], but no expressions are available for the case of the diffused doping profile considered in equation (4.2). This chapter presents a new empirical method of estimating E_C , and hence breakdown voltages, for diffused profiles. This method provides good accuracy and very fast speed compared to device simulators.

4.3 - Calculating E_C

Figure 4.2 shows the constant V_{BR} contours in λ -L space that result when a constant critical breakdown field of $E_C = 225$ kV/cm is assumed, and V_{BR} is calculated

using the procedure outlined in the previous section. (For Fig. 4.2, $N_{s1} = N_{s2} = 10^{17} \text{ cm}^{-3}$, $N_B = 1.85 \times 10^{14} \text{ cm}^{-3}$, and it has been assumed that $\lambda_1 = \lambda_2 = \lambda$, which is a reasonable assumption if boron and phosphorus are the p and n dopants, respectively.) Figure 4.3 shows a similar plot generated from Medici simulations, and Figure 4.4 shows the difference of the values in Figure 4.2 relative to these Medici simulations. The Medici simulations used the Van Overstraeten and De Man data [Van70] for the ionization rates in silicon. (The breakdown voltages were determined using Medici by noting the diode voltage at which the reverse current exceeded $100 \mu\text{A}/\text{mm}^2$. Between 0 V and 200 V the voltage was incremented in 2V steps, and above 200 V it was incremented in 10V steps.)

The Medici simulations used in this thesis were almost all defined as one-dimensional structures with 300 equally-spaced nodes. This proved to be inadequate for only a very few structures which had very steep doping gradients. In these cases, the gridding was modified to decrease the spacing in the vicinity of the steep gradients. The validity of the simulation results in these special cases was confirmed by running several simulations with different gridding for each structure, to ensure that the gridding was sufficiently fine that a small change in grid spacing would not affect the simulation results.

Figure 4.2 The breakdown voltage contours (labeled in Volts) calculated using $E_c = 225$ kV/cm.

Figure 4.3. The breakdown voltage contours (labeled in Volts) calculated using the Medici device simulator.

Figure 4.4. The relative difference between the breakdown voltages presented in Figure 4.2 and the Medici simulations in Figure 4.3.

The results of the two sets of data agree within $\pm 15\%$ for voltages above 170V, and both show the same general trends. However, the quantitative agreement for lower voltage devices is rather poor. The agreement is poorest when there is a steep doping gradient at the metallurgical junction. This is not surprising since the constant critical electric field approximation works best when comparing devices with similar doping levels [Bulu91],[Sze66]. Thus, if the approximation works well for the high voltage devices, where the depletion region extends mostly through regions where $N(x) \approx N_B$, it is unlikely to hold for the low voltages devices which have steep doping gradients in the depletion region.

The results are fairly sensitive to the value of E_C . Choosing a different value for E_C , $E_C = 210$ kV/cm, provides a lower difference for the higher voltage devices, but the voltage above which the agreement is $\pm 15\%$ or better is raised to 270V. The limitations of

assuming a constant E_c for an extended range of doping profiles are clearly demonstrated by these two examples.

To determine a method of choosing a geometry-dependent critical field $E_c(\lambda, L)$, values for x_1 , x_2 , and E_c were determined by working backwards from the $V_{BR}(\lambda, L)$ results obtained in the Medici simulations. The results for $E_c(\lambda, L)$ are shown in Figure 4.5. The contours of the data shown in Figure 4.5, Figure 4.3 and Figure 4.2 show a striking resemblance, leading to the unexpected result that there is an approximate one-to-one correspondence between breakdown voltage and critical field for a wide range of structures. This suggests that better estimates for E_c can be obtained by first calculating a $V_{BR0}(\lambda, L)$ using a constant critical field E_{c0} , and then choosing a new E_c based on the $V_{BR0}(\lambda, L)$ calculation. In practice, it has been found that the empirical function

$$E_c(\lambda, L) = E_{c0} \cdot \left(1 - M \cdot \log_{10} \frac{V_{BR0}(\lambda, L)}{V_1} \right) \quad (4.10)$$

proposed here for the first time, produces excellent results. The desired $V_{BR}(\lambda, L)$ are then calculated as before, but using $E_c(\lambda, L)$ rather than E_{c0} . (The crookedness of the contours in Figure 4.5 is due to the discretization used in the simulator, and not the physical phenomenon itself.)

Using this method, and the empirically determined parameters $E_{c0} = 208$ kV/cm, $M = 0.33$, and $V_1 = 1000$ V, the difference plot of Figure 4.6 was obtained, with an overall average difference magnitude of 3.3%. This plot is considerably better than that of Figure 4.4. These parameter values produced the best results for the particular combination of N_{s1} , N_{s2} and N_b considered above, but the parameters can vary over a fairly large range and still produce good results. The parameters $E_{c0} = 190$ kV/cm, $M = 0.47$, and $V_1 = 1000$ V produced the best results on average for a wider range of power structures. For instance, using these parameters on the structure discussed above yielded

6.8% average difference magnitude, and a second structure with $N_{s1} = N_{s2} = 10^{19} \text{ cm}^{-3}$ and $N_b = 10^{13} \text{ cm}^{-3}$, yielded an average difference magnitude of 8.2%.

Figure 4.5. The critical electric field, $E_c(\lambda, L)$, contours (labeled in kV/cm) as determined from the Medici simulations.

Figure 4.6. The relative difference between the breakdown voltages calculated using the $E_c(\lambda, L)$ given in equation (4.10) and Medici simulations.

A fifty by fifty array of λ - L points was used to generate the data for Figure 4.6. It required 3.5 minutes of processor time on a 90 MHz Pentium-class personal computer to calculate all 2500 voltages. In contrast, using Medici on a Sun Sparc 10 workstation to calculate breakdown voltage for a single λ - L combination typically takes several minutes of computer time (depending on grid spacing and other simulation parameters), so a very large time saving is realized by use of the approximations presented here.

The equations presented above assume that only λ and L are being varied, however, since equation (4.3) does not depend explicitly on any doping or geometry parameters, any such parameter can be varied during optimization.

4.4 - Conclusions Regarding the Method of Calculating V_{BR}

A new two-step method of rapidly estimating the breakdown voltage of diffused rectifiers has been presented, which should prove useful for device optimization. By using the critical field approximation rather than the more rigorous ionization integral approach, significant time savings are realized. The first step is used to determine a value for $E_c(\lambda, L)$, and the second step uses this value to determine $V_{BR}(\lambda, L)$. This method takes advantage of the fact that there is an approximate one-to-one relationship between the device breakdown voltage and the critical field for a wide range of device structures. These results have been compared to Medici simulations, and have been shown to agree very well for a wide range of power diodes.

The interesting fact that E_c and V_{BR} are linked through an approximate one-to-one relationship is explored from a theoretical standpoint in Appendix C.

4.5 - Qualitative Observations on the Nature of $V_{BR}(\lambda, L)$

The contours of Figure 4.2 (and Figure 4.3) have several interesting features. For instance, consider the breakdown voltage variation for $\lambda = 25 \mu\text{m}$ as L is varied. For the limiting case of $L \rightarrow 0$ the breakdown voltage will be large, since the two gaussian profiles will largely cancel each other, leading to a region of low doping which extends across most of the structure. As L increases, V_{BR} falls as this compensation decreases. The breakdown voltage eventually reaches a minimum value, at $L \approx 35 \mu\text{m}$. The cause of this minimum can be seen by referring to Figure 4.7. The minimum occurs when the doping gradient at the junction is largest. Figure 4.8 shows the doping profile and electric field profile at breakdown for this case. The high gradient produces a very narrow depletion region.

Figure 4.7. The doping gradient at the junction.

Figure 4.8. Doping and field profiles for $\lambda = 25 \mu m$, $L = 35 \mu m$.

For a given λ , the L that produces the lowest breakdown voltages can be obtained by setting

$$\left. \frac{d}{dL} \frac{dN(x)}{dx} \right|_{x=x_m} = 0 \quad (4.11)$$

Using (4.2), this can be written as

$$0 = \frac{N_{s2}}{\lambda_2^2} \exp\left(\frac{-(x_m - L)^2}{\lambda_2^2}\right) - 2N_{s2} \frac{(x_m - L)^2}{\lambda_2^4} \exp\left(\frac{-(x_m - L)^2}{\lambda_2^2}\right) \quad (4.12)$$

The locus of points given by (4.12) is shown in Figure 4.2, labeled "A". This curve clearly follows the V_{BR} minima.

As L increases along the $\lambda = 25 \mu\text{m}$ line the two gaussian profiles move apart and the doping gradient at the junction decreases, so the breakdown voltage steadily increases. Figure 4.9 shows the doping and electric field for $L = 125 \mu\text{m}$. The depletion region is much wider than in the previous case. Eventually, however, the breakdown voltages saturate, as seen by the horizontal contours lines in Figure 4.2. This effect is shown in Figures 4.10 and 4.11 for $L = 200 \mu\text{m}$ and $L = 250 \mu\text{m}$ respectively. At $L = 200 \mu\text{m}$ the electric field to the left of the junction is built up over an area where $N(x) \approx N_B$, and breakdown occurs when

$$\frac{q}{\epsilon} (x_m - x_1) N_B = E_C \quad (4.13)$$

For the values used in this simulation, equation (4.13) yields $x_m - x_1 = 79 \mu\text{m}$. Figure 4.10 is in excellent agreement with this estimate. When L is increased to $250 \mu\text{m}$, the doping level between x_1 and x_m is essentially unaffected, so the electric field shape is essentially unchanged (other than a uniform movement to the right), and the breakdown voltage does not change.

Figure 4.9. Doping and field profiles for $\lambda = 25 \mu\text{m}$, $L = 125 \mu\text{m}$.

Figure 4.10. Doping and field profiles for $\lambda = 25 \mu\text{m}$, $L = 200 \mu\text{m}$.

Figure 4.11. Doping and field profiles for $\lambda = 25 \mu\text{m}$, $L = 250 \mu\text{m}$

The locus of points where V_{BR} saturates can then be calculated by requiring that $N(x) \approx N_B$ between x_1 and x_m . If the gaussian profile is considered separately from the background doping, and the point x_a is defined (referring to Figure 4.1) as the point where

$$N_{S1} \exp\left(\frac{-x_a^2}{\lambda_1^2}\right) = N_B \quad (4.14)$$

or, equivalently,

$$x_a = \lambda_1 \sqrt{\ln \frac{N_{S1}}{N_B}} \quad (4.15)$$

then $N(x) \approx N_B$ for $x_1 < x < x_m$, if $x_1 \geq x_a$. The locus of points given by $x_1 = x_a$ is shown in Figure 4.2 by the curve labeled "B". The points above this curve are punchthrough structures, and the points below are non-punchthrough structures.

Now consider the breakdown variation for a fixed L , as λ is varied. As λ is increased from zero for $L = 200 \mu\text{m}$, the breakdown voltage slowly increases. This is due to the decreased doping gradient to the right of the junction, and the accompanying widening of electric field on the right side of the junction. Since these points lie below curve "B", the electric field shape on the left side of the junction remains essentially

unchanged, for the reasons discussed above. This is shown in Figures 4.12 and 4.13 for $L = 200 \mu\text{m}$, $\lambda = 10 \mu\text{m}$ and $L = 200 \mu\text{m}$, $\lambda = 20 \mu\text{m}$ respectively. In Figure 4.12, $x_2 - x_{mj} \approx 10 \mu\text{m}$ and in Figure 12, $x_2 - x_{mj} \approx 15 \mu\text{m}$. Although $x_{mj} - x_1$ must also change, to satisfy the charge balance, the relative change is only a few percent, compared to the 50% increase in $x_2 - x_{mj}$. Since most of the voltage is developed to the left of the junction, the breakdown voltage varies relatively slowly.

Figure 4.12. Doping and field profiles for $L = 200 \mu\text{m}$, $\lambda = 10 \mu\text{m}$.

Figure 4.13. Doping and field profiles for $L = 200 \mu\text{m}$, $\lambda = 20 \mu\text{m}$.

As λ is increased further the breakdown voltage responds as it would to a decreasing L , as discussed above. A maximum breakdown voltage is reached, close to the curve "B" (this corresponds to the structure in Figure 4.9). For larger values of λ , the diode become a punchthrough structure and the voltage begins to fall, until the curve "A" is reached, where the doping gradient at the junction is largest. Then the breakdown voltage will tend to rise again.

It can be seen from Figure 4.2 that the voltage variation below curve "B" is a slowly-varying function of λ , and that V_{BR} appears to approach a non-zero limiting value as $\lambda \rightarrow 0$. This value can be calculated by noting that this situation corresponds to a one-sided junction with a uniform doping of N_B . The width of the depletion region in this limiting case can be found using (4.13), which gives

$$x_{mj} - x_1 = \frac{\epsilon E_C}{q N_B} \quad (4.16)$$

The voltage developed across a one-sided junction with uniform doping can be found by integrating Poisson's equation, yielding

$$V_{BR} = \frac{q N_B (x_{mj} - x_1)^2}{2\epsilon} \quad (4.17)$$

Combining (4.16) and (4.17) gives the limiting V_{BR} :

$$V_{BR} = \frac{\epsilon E_C^2}{2q N_B} \quad (4.18)$$

For the case of Figure 4.2, with $E_C = 225$ kV/cm and $N_B = 1.85 \times 10^{14}$ cm⁻³, the limiting V_{BR} is 892 Volts.

Figures 4.2 and 4.3 show that when designing high-voltage rectifiers for a given breakdown voltage, wafer thickness, and surface and background doping levels, there are generally two diffusion lengths λ that produce the same breakdown voltage. Generally, it is the λ that lies above curve "B" that is chosen, since a narrower low-concentration region yields a lower forward voltage, for devices with similar carrier lifetimes [Benda67]. The other possible λ will lie beneath the "B" curve, and will have a much wider low-concentration region, leading to a higher forward voltage. However, if forward voltage is not the main concern, the smaller λ does offer the advantage of shorter processing times, since from simple diffusion theory [Jaeg88]

$$\lambda = 2\sqrt{D_d \cdot t} \quad (4.19)$$

where D_d is the diffusion coefficient of the dopant and t is the diffusion time. This can be a considerable advantage for high-voltage devices, which can have junction depths many tens of microns deep, requiring several days of high temperature diffusion.

For each of the higher-voltage contours, however, there is generally a point where only one λ will yield the desired voltage. This occurs at the minimum L that can be used to obtain this voltage. This is useful to know when the structure is to be fabricated in an epitaxial layer, and the dopants to be diffused are introduced on one side from the wafer surface and on the other side of the epi-layer from the base substrate itself. Narrower epitaxial widths are easier and faster to fabricate.

The low-voltage contours centered about the "A" curve show that for a given breakdown voltage, diffusion length, and surface and background doping levels, there are generally two diode thicknesses L that produce the same breakdown voltage. The smaller value of L may allow the diode structure to be formed in a thick epitaxial layer, or choosing the larger value of L may allow the diode to be diffused from the opposite sides of a thin uniform wafer.

Chapter 5 - The Theory of Wide-Field Step Recovery Diodes (WFSRD)

5.1 - Remarks on the Philosophy Adopted in This Study

Before beginning to discuss the theoretical aspects of the WFSRD, it is important to first note the approach taken by this author. It was concluded based on the results of Chapter 3 that the desired devices were likely diffused structures, and it is obvious that the diodes must be under high-level injection conditions for reasonable forward bias given the light doping required to support high breakdown voltages. This situation is thus not likely to immediately offer simple *exact* analytical results: most analytical studies in the literature and in textbooks deal strictly with abrupt junctions and/or low-level injection. Most of the common simplifying approximations are not appropriate in this case. For this reason, computer simulations were used as a primary tool in this study. In particular, simple one-dimensional diffused structures were simulated many times using MEDICI, a powerful large-signal semiconductor simulator. The theoretical results in this section were developed after noting patterns in the simulations. For this reason, the approach taken in this section is to introduce particular diode structures with known (simulated) characteristics, and then develop the analytical theory, rather than starting "from scratch". The fabricated devices reported in later sections are almost ideal parallel-plane structures, so the one-dimensional simulations are directly applicable.

One other aspect should be noted. The diodes studied here have been developed with pulse generator applications in mind, since this is the context in which this phenomenon was discovered. This means the diodes are intended to act as pulse sharpeners. Given their similarity to SRDs, they may also prove to be useful in frequency multiplication applications. These applications have not been considered here.

5.2 - Introductory Reference Structures

5.2.1 - Abrupt Structures versus Diffused Structures

For the purposes of comparison, two reference structures are introduced in this section. The first structure, shown in Figure 5.1, is an ideal abrupt ps_pn diode that shall be referred to herein as EP1. The second, shown in Figure 5.2 is a diffused diode, with two gaussian profiles superimposed on a uniform background, and shall be referred to herein as DF1. More precisely, for Figure 5.2,

$$N(x) = N_S \exp\left(-\frac{x^2}{\lambda^2}\right) + N_B - N_S \exp\left(-\frac{(x-L)^2}{\lambda^2}\right) \quad (5.1)$$

where $N(x)$ is the doping profile, with $N(x) > 0$ taken to mean net acceptor doping, and $N(x) < 0$ net donor doping. N_S is the surface concentration, and N_B is the wafer background doping. For both EP1 and DF1, $A = 1 \text{ mm}^2$, $L = 212 \text{ } \mu\text{m}$, $N_S = 10^{19} \text{ cm}^{-3}$, $N_B = 1.2 \times 10^{14} \text{ cm}^{-3}$, and $\tau_{p0} = \tau_{n0} = 55 \text{ ns}$. For DF1, $\lambda = 29.7 \text{ } \mu\text{m}$. For EP1, $W = 30 \text{ } \mu\text{m}$.

Figure 5.1 - Doping Profile of EP1

Figure 5.2 - Doping Profile of DF1

Figure 2.1 shows the simple reverse-recovery test circuit that has been simulated, with $R_L = 50 \Omega$. The reverse recovery transient should consist of a period of roughly constant reverse current (I_R for time t_S) followed by the decay of the current to zero, in time t_R , as discussed in Chapter 2. Figures 5.3 and 5.4 show the simulated transient response for EP1 and DF1 respectively. As expected, EP1 shows the slow ramp/fast transition characteristic of $p^n p^n$ abrupt rectifiers. When $V_d = V_{RAMP}$, where V_{RAMP} is obtained from (2.15), the diode current is determined by the circuit loop equation, giving:

$$I = \frac{V_R}{R + \frac{W^2}{2v_S \epsilon A}} \quad (5.2)$$

$$I = 32 \text{ A}$$

This agrees reasonably well with Figure 5.3, which shows the fast transient beginning at approximately $I = -3.7 \text{ A}$.

Figure 5.3 - The transient response of EP1. The labeled data points correspond to the individual curves in Figure 5.5.

Figure 5.4 - The transient response of DF1. The labeled data points correspond to the individual curves in Figure 5.6.

The parameters of DF1 have been deliberately chosen to produce a reverse recovery transient that displays step recovery. It clearly yields a "snappier" transient, although the storage time is reduced, which is generally undesirable in pulse generator applications.

To understand why EP1 and DF1 behave so differently, the time evolution of the electric fields in the devices is plotted in Figures 5.5 and 5.6 respectively. It is immediately apparent that the p^+p and $p n^+$ junctions in EP1 produce strong, narrow, one-sided electric field profiles, which of course are characteristic of abrupt one-sided junctions. In contrast, the field profiles generated by DF1 are much lower and much more diffuse. They resemble the fields generated at linear junctions. Since the fields generated at the two junctions in the diode are so much more diffuse, they overlap much sooner in DF1 than EP1. Also, when they overlap, the area under the electric field curve is much smaller in the case of DF1 than EP1, hence this occurs at a much lower voltage in the DF1 case. By comparing Figure 5.3 to Figure 5.5, and 5.4 to 5.6, it is evident that the fast transition begins when the entire middle layer is under high-field conditions. The spread-out nature of the electric field profiles in the DF1 diode then is the key to high voltage step recovery.

Figure 5.5 - Electric field evolution in EP1. The curve labels correspond to the individual time points shown in Figure 5.3.

Figure 5.6 - Electric field evolution in DF1. The curve labels correspond to the individual time points shown in Figure 5.4. (Curves A and B are too small to appear at the scale used.)

5.2.2 - The Influence of Background Doping

Not all diffused diodes will produce the desired electric field overlap discussed above. The background doping N_b can have a very large impact on the nature of the diode recovery. The influence of N_b can be explained by referring to the Medici simulation results in Figures 5.7 to 5.16. These graphs show the time evolution of the net charge (that is, $p - n + N_D - N_A$) and the current transient waveform for five different doping profiles, DF2 to DF6 for the circuit in Figure 2.1. All have $A = 1 \text{ mm}^2$, $N_c = 10^{19} \text{ cm}^{-3}$, $\lambda = 29.7 \text{ } \mu\text{m}$, and $L = 212 \text{ } \mu\text{m}$. Each has a different background doping: $-5 \times 10^{14} \text{ cm}^{-3}$, $-1.2 \times 10^{14} \text{ cm}^{-3}$, 0 cm^{-3} , $+1.2 \times 10^{14} \text{ cm}^{-3}$, $+5 \times 10^{14} \text{ cm}^{-3}$, for DF2 to DF6 respectively. (Positive values refer to p-type doping.)

The net charge development is quite different in each case. For the two n-type doped diodes, DF2 and DF3, the area of positive net charge appears to propagate from left to right, in a simple fashion. This occurs because the positive space charge required to form the right side of the p^+n junction is supplied largely by the ionized donors. The nn^+ junction essentially plays no part in the recovery until the charge wave from the p^+n junction sweeps over to it. In contrast, the space charge required to form the right side of the p^+p junction in DF5 is initially supplied by mobile holes rather than by fixed charge. As the current falls, the mobile hole concentration is not sufficient to compensate the ionized acceptors near the p^+p junction. Then, the positive net-charge peak appears to collapse, rather than propagate, and the necessary positive charge is provided by ionized donors on the right side of the metallurgical junction.

Since DF2 exhibits a simple expanding charge wave, propagating from the p^+n metallurgical junction, only one electric field peak develops, as shown in Figure 5.17. In the contrast, DF5 initially develops a field at the p^+p (non-metallurgical) junction. When the mobile charge is removed from the vicinity of the metallurgical junction, a second electrostatic junction must form. Thus when the space charge has propagated from the

p+p junction to the metallurgical junction, it forces a second electric field peak to develop in response, as is shown in Figure 5.18. This causes a substantial electric field to cover to entire middle region, which triggers the desired fast transition, as all remaining mobile charge carriers are removed from the diode at, or near, their saturation velocity.

It is important to determine where exactly the p+ p space charge region forms. This is obvious in abrupt structures, where there is ideally an infinite doping gradient, at which an electrostatic junction must occur. There is no such singularity in the p+ p diffused junction. As discussed earlier, the positive space charge in the p+ p junction must be provided by mobile holes. The concentration of mobile holes must exceed the net acceptor concentration for a net positive charge to exist. The point where these two concentrations are equal (i.e. zero net charge) defines the p+ p junction (if one neglects mobile electrons). Since a large electric field develops at the junction rather quickly, as witnessed in Figure 5.18, and since hole and electrons velocities start to saturate at relatively low electric fields ($\sim 10^4$ V/cm) compared to the scale in Figure 5.18, the hole density in the space-charge region can be approximated as

$$p_0 \approx \frac{J_R}{qv_s} \quad (5.3)$$

For the circuit of Figure 2.1, $p_0 = 3.7 \times 10^{14} \text{ cm}^{-3}$ (again using $A = 1 \text{ mm}^2$). This concentration is noted on the net charge graphs with a thin solid line. Since the net charge is equal to the negative of the doping at the end of the transient, the intersection of the last time curve and p_0 indicates the starting position of the p+ p junction, x_{p0} . x_{p0} is also shown on the net charge graphs, by a thin vertical line.

It is fairly straightforward to deduce that N_B must fall between 0 and p_0 . If $N_B < 0$, (as is the case in Figures 5.7 to 5.10) the positive space charge will be composed largely of fixed ionized donors, so the junction will not need to extend into the n+ regions to

uncover fixed charge until near the end of the transient, as noted earlier. Thus the desired double-peaked electric field does not develop.

The net charge evolution for DF6 in Figure 5.16 depicts a situation where $N_B > p_0$. In this case, the mobile charge is unable to build a significant positive space charge to the left of the metallurgical junction. This leads to the development of a significant electrostatic junction at the metallurgical junction only, so a single peaked electric field develops. While this does lead to a good waveform, as shown in Figure 5.15, it is no better than the more lightly doped DF5 waveform (where $0 < N_B < p_0$), and the breakdown voltage is significantly worse. Medici simulations show that DF5 has $V_{BR} \approx 660V$, whereas DF6 has $V_{BR} \approx 550V$.

Thus one can conclude that for step recovery to occur, one should have

$$N_B = g \cdot p_0 \quad (5.4)$$

or, equivalently,

$$N_B = g \frac{J_R}{qv_R} \quad (5.5)$$

where

$$0 < g < 1 \quad (5.6)$$

In equation (5.5) the general charge removal velocity v_R has been used rather than v_s as in (5.1). This is because usually the electric fields at the beginning of the fast transient are not quite high enough to fully saturate the electron and hole velocities. In practice, the best results have been obtained using:

$$v_R = \frac{v_s}{2} \quad (5.7)$$

DF4 is an intermediate case with $N_b = 0$. It shows elements of both charge propagation and charge collapse.

Appendix F includes the simulation batch-file used to generate the Medici simulation of DF5, so that future researchers can reproduce these results.

Figure 5 7 - Transient response of DF2. The labeled data points correspond to the individual curves in Figure 5 8 and 5 17.

Figure 5 8 - Net charge evolution in DF2. The curve labels correspond to the individual time points shown in Figure 5 7. (Curves A and B are too small to appear at the scale used.) The arrow shows the "charge wave" nature of the charge evolution with time.

2

PM-1 3 1/2" x 4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

PRECISIONSM RESOLUTION TARGETS

Figure 5.9 - Transient response of DF3. The labeled data points correspond to the individual curves in Figure 5.10.

Figure 5.10 - Net charge evolution in DF3. The curve labels correspond to the individual time points shown in Figure 5.9. (Curves A, B and C are too small to appear at the scale used.)

Figure 5.11 - Transient response of DF4. The labeled data points correspond to the individual curves in Figure 5.12.

Figure 5.12 - Net charge evolution in DF4. The curve labels correspond to the individual time points shown in Figure 5.11. (Curves A and B are too small to appear at the scale used.)

Figure 5.13 - Transient response of DF5. The labeled data points correspond to the individual curves in Figure 5.14 and 5.18.

Figure 5.14 - Net charge evolution in DF5. The curve labels correspond to the individual time points shown in Figure 5.13. (Curves A and B are too small to appear at the scale used.) The left arrow shows the "charge collapse" nature of the charge evolution with time. The right arrow shows the later development of the second space charge region.

Figure 5.15 - Transient response of DF6. The labeled data points correspond to the individual curves in Figure 5.16.

Figure 5.16 - Net charge evolution in DF6. The curve labels correspond to the individual time points shown in Figure 5.15. (Curves A and B are too small to appear at the scale used.)

Figure 5.17 - Electric field evolution in DF2. The curve labels correspond to the individual time points shown in Figure 5.7. (Curves A and B are too small to appear at the scale used.)

Figure 5.18 - Electric field evolution in DF5. The curve labels correspond to the individual time points shown in Figure 5.13. (Curves A and B are too small to appear at the scale used.)

5.3 - General Description of the New SRD Mechanism

Now that some of the salient details have been introduced in the previous section, a general review of the new proposed SRD mechanism will be provided in this section.

The new SRD mechanism operates as follows. The diode is biased with a small constant forward DC current. This swamps the middle region of the psn diode with electrons and holes, and high injection conditions prevail. The diode acts as a low resistance. When a large reverse bias voltage is suddenly applied, the reverse bias slowly withdraws electrons and hole from the middle region. This region is still largely neutral, so the current will be almost entirely a diffusion current. This means that the slope of the carrier concentrations will change. This will lead to the removal of charge from the quasi-neutral middle region, and this region will shrink. A significant space charge region develops at the p^+p^- junction first, as discussed in Chapter 2. However, as mobile charge is removed from the center, too few holes are left on the p^- side of the junction to support a positive space charge. Since a positive space charge must exist to counterbalance the ionized acceptors in the p^+ region, a second space charge region develops around the metallurgical junction, and the positive space charge is now provided by the ionized donors in the n^+ region. This leads to envelopment of the entire middle region with space charge. After this point, the electric fields rapidly remove the free carriers, and hence the electric fields rapidly "snap" to the full reverse voltage.

(It should be mentioned that the first SRDs manufactured also had a diffused profile, and a graded junction [Moll62], [Kocs76]. The graded junction provided a built-in electric field throughout the active region, which aided in charge removal. This is an entirely different mechanism than that presented here. The carrier densities are too high, and the doping too low, for significant built-in electric fields to exist in WFSRDs.)

Figure 5.19 - A typical SRD pulse-sharpening waveform.

Figure 5.19 shows a typical SRD pulse-sharpening waveform. From this diagram, it is obvious what must be optimized. The maximum operating voltage must be maximized. This implies that the diode breakdown voltage V_{BR} must be maximized. It is also desirable to maximize t_S . Conversely, t_R , V_{RAMP} , and the effect of the diode capacitance, which manifests itself as a "tail" on the waveform, must be minimized. At the same time the conditions for step recovery to occur (equations (5.4) to (5.6)) must be satisfied. Since the occurrence of step recovery and V_{BR} both depend very heavily on N_B , it is obvious that some optimization process will be required.

The remaining section in this chapter will be devoted to determining these parameters from the diode doping profile. The discussion of the method of determining V_{BR} has already been presented in a separate chapter, due to its length.

5.4 - Parameter Determination

5.4.1 - N_B

For consistency, the results of section 5.2.2 will be repeated here. It was shown that for step recovery to occur,

$$N_B = g \cdot p_0 \quad (5.8)$$

or, equivalently,

$$N_B = g \frac{J_R}{qV_R} \quad (5.9)$$

where

$$0 < g < 1 \quad (5.10)$$

and

$$p_0 = \frac{J_R}{qV_R} \quad (5.11)$$

It should be noted that the factor g is directly related to the diode cross-sectional area, since for the circuit of Figure 2.1,

$$J_R = \frac{V_{OP}}{A \cdot R} \quad (5.12)$$

5.4.2 - V_{RAMP}

When the two space charge regions overlap significantly, the voltage developed across the device, obtained by integrating the electric field:

$$V = - \int_0^L E dx = \frac{q}{\epsilon} \int_0^L \int (p - N(x) - n) dx \quad (5.13)$$

should be minimized. This voltage is the ramp voltage that one wishes to minimize in a step recovery diode. Determining the voltage across the device exactly is a difficult problem best suited to simulators such as MEDICI, however, some simple approximations can be made to avoid this need in the initial stages of design.

When the space charge regions begin to overlap, the net charge should be zero at two points: at the p+ p junction x_{p0} , and at the metallurgical junction x_m . This is seen in Figure 5.14 for the DF5 structure. (From Figures 5.14 and 5.18, it is evident that the space charge regions overlap at instant "F"). The shape of the positive space charge: $P(x)$ between these two points can be approximated as a parabola, that is:

$$P(x) = A_0(x - x_0)^2 + A_1 \quad (5.14)$$

For the purposes of this approximation, the apex of the parabola will be assumed to be at the midpoint between x_{p0} and x_m , such that

$$x_0 = x_{p0} + \frac{\Delta x}{2} \quad (5.15)$$

Since

$$P(x_{p0}) = P\left(x_0 - \frac{\Delta x}{2}\right) = 0 \quad (5.16)$$

one of the constants in (5.14) can be eliminated, this yields:

$$P(x) = A_1 \cdot \left(1 - \frac{4}{\Delta x^2}(x - x_0)^2\right) \quad (5.17)$$

The voltage developed across the left electric field peak can be estimated by using equation (5.13) and integrating the positive space charge between x_{p0} and x_m , so that

$$V_+ = \frac{q}{\epsilon} \int_{x_0 - \frac{\Delta x}{2}}^{x_0 + \frac{\Delta x}{2}} \int A_1 \cdot \left(1 - \frac{4}{\Delta x^2} (x - x_0)^2 \right) dx \quad (5.18)$$

The voltage developed across the negative space charge that is to the left of x_{q0} , V_- , must also be accounted for. As a first approximation, it shall be assumed that $V_+ = V_-$. Then, evaluating (5.18) yields a simple expression for the voltage at overlap, V_{RAMP} :

$$V_{\text{RAMP}} = 2V_+ = \frac{4q}{3\epsilon} \cdot A_1 \cdot \Delta x^2 \quad (5.19)$$

A value for A_1 must also be determined. From (5.16) it can be seen that $A_1 = P(x_0)$, so the space charge at x_0 must be found. The net charge Q_N is the given by

$$Q_N = q(p - N(x) - n) \quad (5.20)$$

The doping $N(x)$ can be found directly from (5.1), and the mobile hole concentration p from (5.3). If one makes the assumption that the mobile electron concentration n is small compared to the other two components, then

$$A_1 = \frac{J_R}{qv_R} - \left(N_S \exp\left(-\frac{x_0^2}{\lambda^2}\right) + N_B - N_S \exp\left(-\frac{(x_0 - L)^2}{\lambda^2}\right) \right) \quad (5.21)$$

or, using (5.9),

$$A_1 = \frac{N_B}{g} - \left(N_S \exp\left(-\frac{x_0^2}{\lambda^2}\right) + N_B - N_S \exp\left(-\frac{(x_0 - L)^2}{\lambda^2}\right) \right) \quad (5.22)$$

If this is substituted into (5.19), and if it is noted that $x_0 = (x_{p0} + x_{mj})/2$ and $\Delta x = x_{mj} - x_{p0}$, then one obtains

$$V_{\text{RAMP}} = \frac{4q}{3\epsilon} \cdot (x_{mj} - x_{p0})^2 \cdot \left(\frac{N_B}{g} - N_S \exp\left(-\frac{(x_{p0} + x_{mj})^2}{4\lambda^2}\right) - N_B + N_S \exp\left(-\frac{(x_{p0} + x_{mj} - 2L)^2}{4\lambda^2}\right) \right) \quad (5.23)$$

In this analysis, it has also been assumed that the voltage developed across the p-n⁺ junction is small compared to that of the p⁺-p- junction. In practice, this assumption is a reasonable one.

Since x_{p0} and x_{mj} depend on the choice of λ and L , V_{RAMP} will be a complicated function of λ and L . When designing the diode, $V_{\text{RAMP}}(\lambda, L)$ must be minimized to achieve a low initial ramp voltage. However, a second constraint is required to choose an optimum λ and L once N_B has been determined from (5.9). This second constraint is obtained by considering the need to maximize the breakdown voltage of the device.

5.4.3 - The Transition Time t_R

The fast transition begins when a small electric field exists throughout the entire middle region. In other words, this is the point where the condition of quasineutrality is just beginning to fail throughout this region. We can make several assumptions to obtain a good approximation of the transition time. First, we can assume that all electrons have been removed from the left of the metallurgical junction, and all holes have been removed from the right. Secondly, we can assume the entire middle region is still neutral (such that the accumulated voltage is very small). Thus, considering the left half of the middle region, every acceptor is compensated by a mobile hole, and to the right of the junction every donor is compensated by an electron. The total mobile charge can then be

determined by integrating the absolute value of the doping across the depletion region. We can observe from the electric field and net charge plots previously shown that the edges of the now-homogeneous space charge region varies very little between the beginning of the fast transient and the end, so we can use the values of x_1 and x_2 as calculated in Chapter 4 as the edges of the region. The third assumption will be that the fast transient voltage is linear with time, which is the ideal waveform. Then the time can simply be calculated from a charge control approach as

$$t_R = Q / \frac{I_R}{2} \quad (5.24)$$

where

$$Q = qA \int_{x_1}^{x_{mj}} N(x) dx \quad (5.25)$$

or, equivalently,

$$Q = qA \int_{x_{mj}}^{x_2} |N(x)| dx \quad (5.26)$$

If one compares the expression given in (5.25) to that given in equation (4.3), it becomes apparent that (5.24) can be written more simply as

$$t_R = 2 \frac{\epsilon A E_C}{I_R} \quad (5.27)$$

At first glance, the expression in (5.27) may be misleading, in that it suggests that semiconductors with lower critical fields will have shorter transition times. This is not true, since any decrease in E_C will be more than offset by an increase in A , for a given operating voltage. This is due to the fact that a lower E_C will require a wider depletion region to accommodate the same voltage. However, (5.19) shows that V_{KAMP} increases approximately quadratically with width, hence A will have to increase similarly to

counterbalance the change in V_{RAMP} . (Increasing A lowers J_R , which as shown in (5.21) will act to lower V_{RAMP} .)

The expression in (5.27) is a fairly simple estimate of t_R . Calculating t_R more accurately would require an exact knowledge of the carrier distribution evolution during the reverse transient, and during the forward steady-state as well. Realistically, this can only be achieved by complete computer simulations. Several such simulations are presented in Appendix D, in order to gauge the effect of lifetime variation on t_R . This second-order effect is not included in (5.27).

5.4.4 - RC Time Constant

Since, as noted before, the edges of the space charge region are nearly stationary after the start of the fast transient, the junction capacitance is also nearly constant. It is important to minimize this capacitance, since it acts to slow down the fast transient, with a time constant of $R_L C$. (R_L , the load resistance, is assumed to be 50Ω throughout this thesis.) It will add an exponential "tail" onto the end of the transient, as depicted in Fig 5.19. The junction capacitance can be treated as a first approximation as a parallel plate capacitor, with plates at x_1 and x_2 ; hence

$$C = \frac{\epsilon A}{x_2 - x_1} \quad (5.28)$$

and

$$\tau_{RC} = \frac{\epsilon A R_L}{x_2 - x_1} \quad (5.29)$$

where τ_{RC} is the characteristic time constant of the junction capacitance - load resistance network.

5.4.5 - Storage Time t_s

Calculating the storage time is in fact an extremely complicated task if an exact answer is desired. Knowledge of the actual carrier distribution throughout the diode is required, which is impossible to do analytically due to the lack of simple boundary conditions in the diffused rectifier. Even for the case of an abrupt pin geometry with constant recombination lifetimes throughout the i region, the storage time has only been calculated numerically [Slat80]. Since the device is in high injection, the assumption of constant recombination lifetimes is not correct.

The storage time can be estimated using simple (but not very accurate) charge control techniques. This yields equation (3.4), repeated here:

$$\frac{t_s}{\tau_{EFF}} = \ln \left(1 + \frac{I_F}{I_R} \right) \quad (5.30)$$

where τ_{EFF} is the effective lifetime of the charge carriers in the device. However, this equation is not especially useful for design, since the carrier lifetimes are highly dependent on the fabrication process, and are not easily measured. Also, τ_{EFF} is a complex function of parameters, such as the diode structure, low-level carrier lifetimes, and carrier density.

As mentioned earlier, diffused structures have larger effective lifetimes than comparable epitaxial structures, since a diffused rectifier will have more stored charge for a given bias current than an epitaxial rectifier [Coop83]. In an epitaxial rectifier, the stored charge is confined between the two junctions. The diffused rectifier has much poorer charge confinement, and a considerable additional portion of charge will exist in the p^+ and n^+ regions of the diode.

5.5 - Design Methodology

In the previous chapters, expressions for V_{BR} , V_{RAMP} , t_r , and τ_{RC} were obtained in terms of the doping profile and circuit parameters. This chapter presents a method of using the expressions to obtain the best possible device for a given application.

It is not possible to work backwards from the desired switching parameters and breakdown voltage to find the best doping. Instead, many doping profiles must be considered, and the parameters calculated for each. However, for each profile some optimization is required, since the ramp voltage decreases with increasing area, whereas t_r and τ_{RC} increase.

A program has been written that will perform the required device optimization. Its operation is discussed below.

5.5.1 - Optimization

The program considers many different profiles. The user may vary the number of profiles considered, and what ranges of values are used for N_{S1} , N_{S2} , N_B , λ_1 , λ_1/λ_2 , and L . For each profile, the breakdown voltage is calculated using the method discussed in Chapter 4. No optimization is necessary at this point, since V_{BR} is independent of the device cross-sectional area. If the value of V_{BR} is not within the desired range, the calculations for this structure are discarded. Otherwise they continue as described below.

The program also lets the user set what fraction of the breakdown voltage the operating voltage V_{OP} will be. (Ideally, the operating voltage should be slightly less than V_{BR} , but in practice a safety margin must be added.) Also, the user can set what fraction of V_{OP} the ramp voltage V_{RAMP} may be. Since rise times are usually defined as 10%-90%, V_{RAMP} is usually set at 10% of V_{OP} . Any higher would produce an insufficiently "square" waveform, and a smaller value would increase t_r and τ_{RC} more than necessary.

Given this information, and the calculated values of V_{BR} and V_{OF} , the program determines the value of g that will yield the desired V_{RAMP} , using equation (5.23). The diode cross-sectional area can then be determined using (5.12). With all doping and geometrical factors now determined, t_R and τ_{RC} can be determined. As a figure of merit, the program computes

$$t_{EFF} = \sqrt{t_R^2 + (2.2\tau_{RC})^2} \quad (5.31)$$

for each structure and ranks each solution, such that the best structure for a given operating range can be found. (The factor of 2.2 converts the RC time constant to a 10%-90% rise time [Sedr91]).

Figure 5.20 shows a typical screen shot from the program. At the bottom, the best three structures are shown. All structures that satisfied the breakdown voltage required were stored in a file as well.

The figure of merit t_{EFF} is only an approximate figure of merit, so that when choosing between two structures with very similar t_{EFF} (i.e. $\pm 20\%$) it is wise to confirm the choice with a device simulator such as Medici, especially if one is more manufacturable than the other.

Electrical and Diffusion		Solution Array Setup		File	
Desired V_{br} , ±10%	500 V	Minimum N_{s1}	1e17 cm ⁻³	File name:	test.txt
V_{op}/V_{br}	0.6	Number of N_{s1} values	7	Directory:	c:\papers\card
V_{ramp}/V_{op}	0.1	Values per decade	3		
Critical Field at 1000V	200 kV/cm	Minimum N_{s2}	1e17 cm ⁻³		
Critical Field Slope Factor	0.33	Number of N_{s2} values	7		
particle velocity: v_a/v_{amax}	0.5	Values per decade	3		
		Minimum N_b	1e14 cm ⁻³		
		Number of N_{s1} values	11		
		Values per decade	10		
		Minimum λ/λ_2	1		
		Number of values	1		
		Step Size	0		
		minimum Lambda	5 um		
		maximum Lambda	50 um		
Miscellaneous				Current Values	
Distance Tolerance	0.001 um			N_{s1}	1.00E+17
Function Tolerance	0.1 %			N_{s2}	1.00E+17
Dielectric Constant	01.0 cd			N_b	3.30E+14
				λ/λ_2	01.00
				λ	33.00
				L	075.00

-t _{eff} ,ns-	N_{s1}	N_{s2}	N_b	Ratio	λ	L	V_{br}	V_{ramp}	t_r	t_{rc}	t_{on}	t_{off}
00.00	1.00E+17	1.00E+17	1.00E+14	01.00	49.00	215.00	0450.1	0020.4	00.73	00.15	00.00	00.45
00.02	1.00E+17	1.00E+17	1.20E+14	01.00	45.00	200.00	0452.6	0020.1	00.75	00.15	00.02	00.57
00.02	1.00E+17	1.00E+17	2.52E+14	01.00	45.00	200.00	0451.2	0020.3	00.75	00.15	00.02	01.29

Figure 5.20 - Typical screen shot from WFSRD parameter calculation program.

5.6 - The Chosen Device

Figure 5.21 shows the optimization parameters used to find a good structure to implement a device with $V_{BR} = 500$ V and $V_{OP} = 300$ V. (Note the considerable safety margin.) In Figure 5.21, the program has been run to display the characteristics of a single structure, the one that was ultimately fabricated. A rise time (t_{EFF}) of 1.1 ns is predicted for this device. This combination of parameters did not produce the very best theoretical switching performance, but it had the advantage of having a not-too-small value of L and small value of λ . (As indicated in Figure 5.20, the fast predicted switching time was 0.80 ns). The desirability of a large L and a small λ are discussed in the next chapter.

Figure 5.21 - WFSRD parameter calculation program output for the device to be fabricated.

5.7 - Operating Range Limitations

It is of interest to establish the maximum voltage that WFSRDs can be expected to operate at. To determine this, the WFSRD parameter calculation program was run many times to determine the fastest devices as a function of voltage. Several limits were imposed on the search-space, to keep the device practical. In particular, λ was restricted to vary between 5 μ m and 100 μ m (in 1 μ m steps), and L was varied between 50 μ m and 500 μ m (in 5 μ m steps). The results are shown in Figure 5.22.

Figure 5.22 - Dimensional and switching parameters for the fastest WFSRD devices with the indicated breakdown voltage.

The results of Figure 5.22 show that the 100 μm limitation on λ is in fact a severe restriction. The optimal devices would actually occur above this limit. However, obtaining diffusion lengths above 100 μm is not practical. The 30.6 μm diffusion length used in fabricating the device discussed in the next chapter required an extremely long drive-in diffusion of 180 hours, and an extremely hot temperature of 1250°C. Since $t \propto \lambda^2$, where t is time, the drive-in time required for $\lambda = 100 \mu\text{m}$ is excessive (11 weeks at 1250°C).

Figure 5.23 shows the same data as Figure 5.22, except that it is for devices whose switching time is 33% greater than those in Figure 5.22. It shows that some gains in practicality can be made if non-optimum devices are used. If a λ of 50 μm is considered the maximum practical dopant diffusion length (this corresponds to three weeks of drive-in at 1250°C), then practical devices exist for $V_{BR} < 1100 \text{ V}$.

Figure 5.23 - Dimensional and switching parameters for devices that are 33% slower than the fastest WFSRD devices with the indicated breakdown voltage.

These results suggest that the maximum practical operating voltage for DSRDs is on the order of 1 kV. The precise limit is a function of manufacturing constraints. If exceedingly long drive-in times or slower devices can be tolerated, then devices with higher breakdown voltages can be obtained. However, it is probably more practical to use multiple lower-voltage devices connected in series.

Chapter 6 - Fabrication Method for WFSRD Devices

6.1 - Introduction

As noted in Figure 5.21, the device parameters chosen for fabrication are:

- $N_{S1} = 10^{17} \text{ cm}^{-3}$
- $N_{S2} = 10^{17} \text{ cm}^{-3}$
- $N_a = 1.5 \times 10^{14} \text{ cm}^{-3}$, p-type
- $\lambda = 30.6 \text{ } \mu\text{m}$
- $L = 150 \text{ } \mu\text{m}$
- $A = 1.35 \text{ mm}^2$

Unfortunately each one of these values falls outside the normal ranges of values typically encountered in a VLSI fab. The surface dopings are quite low. Usually, one wants them to be as high as possible to ensure a good ohmic contact. As for N_a , lightly-doped p-type substrates are generally harder to obtain than lightly-doped n-type substrates. The value of λ given is very, very long compared to normal VLSI standards for diffusion. (Values on the order of $0.1 \text{ } \mu\text{m}$ are more common). Lastly, the thickness L is quite thin, compared to standard wafer thicknesses.

6.2 - General Approach

Three general methods were considered for fabrication. The first approach consisted of thinning a standard wafer with a background doping of N_a down to the desired device length of $150 \text{ } \mu\text{m}$, and diffusing in the remaining dopants. The primary disadvantages of this approach were that the thin wafer might complicate handling and yield, and that the high value of λ would require a very long time in a very hot diffusion

furnace (approximately 10 days at 1250 °C). The advantages were that the thinning process was relatively inexpensive (US\$110/wafer), and the diffusion could be done in-house with existing equipment at Carleton.

The second possible approach was the use of variable-dopant epitaxy to grow the exact profile desired on a thick conducting substrate. However, this would require a relatively thick (but not unheard of) epitaxial growth. Also, obtaining reasonable control of doping at 10^{14} cm^{-3} levels would require a large amount of experimentation. For these reasons, quotes for performing this growth commercially (at Lawrence Semiconductor Research Laboratory, Inc.) proved to be expensive (US\$2750 setup, plus \$175/wafer). The possibility of performing this epitaxy in-house on Carleton's AET RX rapid thermal CVD system existed, however, at the time this thesis began, this equipment was brand new and not yet operational, and represented relatively untried technology.

Both of these approaches yield essentially one-dimensional structures. More complex schemes, involving selectively thinning a thick substrate were also considered. However, endpoint detection in thinning etches would be problematic. Also, the increased dimensionality is undesirable, as it would likely introduce undesired parasitic effects.

For these reasons, the first approach (thinning and long diffusion) was chosen.

6.3 - Substrate Preparation and Dopant Implantation

By happy coincidence, wafers with almost precisely the desired value of N_B were available from a surplus-wafer broker. Furthermore, these wafers were float-zone refined rather than Czochralski-refined, which is highly desirable for high-voltage devices. Float-zone material tends to produce devices with higher breakdown voltages, due to lower oxygen and other impurity content [Ghan83]. (The Czochralski refining process is performed in a quartz crucible, which leaches some oxygen into the molten silicon. Float-

zone refining isolates the molten portion of the silicon ingot from contact with any crucible.)

The complete wafer specifications were as follows: Prime Grade, <100>, Boron-doped, 75-95 Ω -cm, float zone, 4 inch diameter, two standard flats, polysilicon backside, 510-540 μ m thickness, made by Wacker-Siltronic, US\$14. Twenty-five wafers were purchased.

To thin the wafer to the required 150 μ m thickness, fifteen wafers were sent to Virginia Semiconductor for chemi-mechanical polishing (CMP). Only eight wafers survived the process, due to the thinness. The others shattered. Upon their return, the eight wafers were cleaned in Caro's acid (1 litre of sulfuric acid at 100 °C, mixed with 100 mL of 30% H_2O_2) for ten minutes, and rinsed in de-ionized water.

At this point, six wafers (designated "A" to "F") were sent to Implant Center Inc, to implant the remaining dopants. A dose of $2.7 \times 10^{14} \text{ cm}^{-2}$ of boron was implanted with a moderate energy of 80 keV on one side of each wafer, and a similar dose of phosphorus on the opposite side. The dose, Q , is related to N_s and λ through the relationship:

$$Q_{\text{impl}} = \frac{\sqrt{\pi}}{2} \lambda N_s \quad (6.1)$$

For $N_s = 10^{17} \text{ cm}^{-3}$ and $\lambda = 30.6 \text{ } \mu\text{m}$, $Q_{\text{impl}} = 2.7 \times 10^{14} \text{ cm}^{-2}$. The total cost was very low, approximately US\$130. One wafer ("B") broke during implantation, due to the wafer's thinness.

After the wafers were returned from implantation, one wafer (designated "A") was cleaned in Caro's acid. Apparently due to thermal shock, the wafer broke into two roughly equal-size pieces. However, as it had been the intention to break the wafer into

several pieces at a slightly later stage. this breakage did not present a significant problem and processing continued with this wafer.

6.4 - Dopant Drive-In Diffusion

The dopants introduced by the implants were redistributed to obtain the desired values of N_{S1} , N_{S2} , and λ by using a drive-in diffusion. However, as noted earlier, the large value of λ requires a very long and hot diffusion. Simulations on the Suprem III simulator indicated that to obtain the desired values, a drive-in time of approximately 180 hours was required if a temperature of 1250 °C was used. (This temperature represented the maximum usable temperature of the quartz tubes that were available.) This long diffusion raises two potential problems: that of dopant suck-out, and impurity diffusion. Dopant suck-out occurs when the dopants evaporate out of the silicon wafer, or diffuse into the surface film. Impurity diffusion occurs when temperatures are high enough that impurities (like sodium) can diffuse through the furnace quartz tube and enter the wafer.

The first problem was addressed by adding an oxide layer on the wafer "A" to seal in the dopants. The "LOTOX" (low-temperature oxide) was added by placing the "A" wafer in the furnace in an oxygen atmosphere at 405 °C for 15 minutes. Judging from the gold color of the deposited oxide, the oxide thickness was about 0.2 μm . Suprem III simulations indicated that this would be sufficient to contain most of the dopants. (A standard pre-furnace RCA clean was performed before the LOTOX deposition.)

After the Lotox deposition, the wafer "A" was broken into ten smaller, roughly equal-size pieces designated "A0" to "A9". These pieces were cleaned in a standard HCl- H_2O_2 mixture (chosen so as not to etch the protective oxide), followed by a brief 5% HF dip. Pieces "A1" to "A9" were then placed into the furnace for the drive-in. The furnace operated at 1250 °C, with a 2% oxygen, 98% nitrogen atmosphere. (The nitrogen was chosen since it is relatively inert, and the oxygen prevented any nitride formation on the wafer surface). At twenty-two hours intervals, approximately, the wafer pieces were

removed from the furnace, and the furnace tube was gettered with HCl for one hour, at 1250 °C. After each gettering, one wafer piece was removed, and the remainder were reloaded into the furnace. In this manner, pieces with drive-in times of approximately 23 hr, 44 hr, 65 hr, 86 hr, 107 hr, 128 hr, 149 hr, 170hr, and 199 hr were obtained, corresponding to A1 to A9, respectively. This was done in order to calibrate the drive-in process, relative to the SUPREM simulations. This process took about 10 working days. On weekends, the wafer boat was moved to the end of the furnace tube, and the temperature was dropped to 1000 °C, with a nitrogen purge. This effectively halted the drive-in, on weekends. (This measure was taken as a precaution against power outages, or other equipment problems which might arise over the weekend, when technicians were not present.)

Wafer pieces "A5" to "A9" were sent to Solecon Laboratories Inc. for spreading resistance measurements, so that the doping profiles could be examined. The results of these measurements are shown in Figure 6.1, in doping-concentration form rather than in raw resistance measurements. (The resistance-to-doping calculation was performed by Solecon.)

Figure 6.1 indicates that both A8 and A9 have nearly the ideal doping profile. The only significant deviation is the 30% lower-than-expected surface concentrations. Evidently, some dopant evaporated, or was "sucked-out" into the oxide layers. This should not have a significant impact on device operation, since the active region is the lightly-doped area around the junction. (However, relatively poor forward-bias conduction can be expected, due to poor ohmic contacts.)

Figure 6.1 - Doping profile as a function of drive-in time

As a result of the drive-in, approximately $0.7\ \mu\text{m}$ of oxide coated the wafer pieces. This was removed by etching the wafers in a 10% HF solution for approximately 35 minutes. (The endpoint of an oxide etch can be determined by observing when the silicon surface becomes hydrophobic.)

6.5 - Lifetime Killers

At this point, the fabrication sequence branched into two parts. One portion of wafer A.8 proceeded directly to metallization. A second portion, redesignated "A8.PT.850", had lifetime-killers (platinum) introduced, and then proceeded to metallization.

The platinum impurity centers were introduced into A8.PT.850 by dipping the wafer into undiluted Emulsitone Platinumfilm, a spin-on dopant source. The wafer then

underwent a four hour, 850 °C, oxygen atmosphere diffusion to drive-in the platinum. Surface oxide was removed with a 10% HF solution.

6.6 - Metallization

Both A.8 and A8.PT.850 followed the same metallization steps.

The silicon surfaces were cleaned with a 2 minute, 900 V, 100 W sputter etch in 8 milliTor of argon, to remove any oxide that had grown during the time since the HF etch, or indeed any other surface contamination. All sputtering was performed using a Materials Research Corporation 8620 diffusion-pumped multi-target system.

A chromium target was pre-sputtered by a 3 minute, 1.25 kV, 100 W etch in 8 milliTor of argon. The wafer piece was then sputtered with the chromium for 20 minutes, at the 1.35 kV, 100 W, 8 milliTor argon settings. Identical pre-sputtering and sputtering steps were then performed with a gold target. This produced a 6000 Å thick gold layer, bonded to the silicon surface with a 1000 Å thick chromium adhesive layer. The silicon piece was then flipped, and the process repeated, so that identical metallization existed on both sides of the wafer.

Gold was used as the top metal to ensure that the diode could be easily hand-soldered to.

A photomask was generated on a 2.5" × 2.5" glass substrate (designated CU-170-01). The pattern consisted of 45 mil × 45 mil squares (representing the desired metallization) on a 50 mi' grid (1 mil ≈ 25 μm). A positive photoresist (HPR-504) was applied to one side of the wafer, and was developed. The exposed metallization was removed with a 60 minute, 900 V, 100 W, 8 milliTor argon sputter etch. The excess photoresist was then removed using acetone and Microstrip 2001. It was found that a

black residue (presumably charred photoresist) remained on the metal surface despite the use of the photoresist strippers. This was removed with the gentle use of a cotton swab.

A dry etch, rather than a wet etch, was used to remove the excess metallization in the belief that a dry etch would introduce fewer contaminants, such as potassium, which might have deleterious effects on the breakdown voltage.

To reduce sputtering damage, and to improve the metallization adhesion, the wafer underwent a 15 second, 450 °C rapid thermal anneal (RTA).

A Tempress diamond scribe was used to scribe "A8" and "A8.PT.850" into individual devices (designated "A8.*n*" and "A8.PT.850.*n*", respectively, where *n* is a number). These devices were then separated by running a roller over the wafer surface, cleaving the devices along the scribe lines.

Chapter 7 - Experimental Results for WFSRD Devices

7.1 - Introduction

In this chapter experimental results for the diodes fabricated by the process described in the previous chapter, and described theoretically in Chapters 4 and 5, are presented. DC measurements are presented to confirm the basic diode operation in section 7.2. The switching transients for the series-connected pulse-sharpening circuit configuration (see Figure 1.1) are presented in section 7.3. The switching transients for the shunt-connected pulse-sharpening circuit configuration (see Figure 1.1) are presented in section 7.4. A discussion of the results obtained is presented in section 7.5.

7.2 - DC Measurements

Figure 7.1 shows the reverse breakdown characteristics of a typical diode (designated "A8.6") fabricated in Chapter 6, as measured on a Fairchild 6200-A curve tracer. As described in Section 5.6, the diode was conservatively chosen to have an operating voltage of 300 V and an ideal theoretical breakdown voltage of 529 V, based on the predictions of Chapter 4. Figure 7.1 confirms that the breakdown voltage is indeed around 500 V, if we arbitrarily define breakdown as occurring at $I = -200 \mu\text{A}$.

Figure 7.1 - Reverse I-V characteristic for A8.6. Scale: 100 V/div horizontally, 50 μ A/div vertically. The origin is at the upper-right corner.

Figure 7.2 shows the forward bias I-V curve for the diode A8.6. It is obvious that the forward conduction characteristics are less than ideal. For instance, a large forward bias of $V = 6$ V is required for $I = 100$ mA. This poor forward characteristic is not surprising, due to the low surface doping, and hence poor ohmic contacts in the device. Additional dopant implants at the wafer surface after the drive-in could fix this problem very easily in future devices. However, the next section will show that the forward bias currents required for good pulse-sharpening behavior are small, resulting in low power dissipation despite the high on-voltages.

Figure 7.2 - Forward I-V curve for A8.6. Scale: 1 V/div horizontally, 10 mA/div vertically. The origin is at the lower-left corner.

7.3 - Series-Connected Pulse-Sharpening Operation

Figure 7.3 shows the “series-connected” pulse-sharpening circuit used to obtain the waveforms of Figure 7.4 and 7.5. Figure 7.4 shows seven different waveforms. The widest pulse is the 11 ns wide, 300 V input waveform, measured with the diode shorted out. The remaining six waveforms show the operation of the diode A8.6 for $I_{\text{BIAS}} = 2, 4, 6, 8, 10,$ and 12 mA, in order of increasing pulse width. In each case, the output fall time is about 1.7 ns. During this time, the diode switches 300 V and 6.0 A of current. In Figure 7.5, the input pulse width has been greatly extended, and output waveforms are shown for $I_{\text{BIAS}} = 6, 12, 18, 24,$ and 30 mA. Clearly, the pulse sharpening action diminishes for output pulse widths above 10 ns. Both the ramp voltage and the fall time increase.

Figure 7.3 - Series-connected pulse sharpening test circuit.

Figure 7.4 - Output of the circuit of Figure 7.3 for A8.6 with $I_{BIAS} = 2, 4, 6, 8, 10, \text{ and } 12 \text{ mA}$. The widest pulse is the input waveform. (Actual output scale: $50 \text{ mV/div} \times 70 \text{ dB} = 158 \text{ V/div}$, and 5 ns/div).

Figure 7.5 - Output of the circuit of Figure 7.3 for A8.6 with $I_{\text{BIAS}} = 6, 12, 18, 24$, and 30 mA. The widest pulse is the input waveform. (Actual output scale: $50 \text{ mV/div} \times 70 \text{ dB} = 158 \text{ V/div}$, and 5 ns/div).

Figure 7.6 - Output of the circuit of Figure 7.3 for A8.PT.850.1 with $I_{\text{BIAS}} = 20, 40, 60, 80, 100, 120, 140, 160, 180$, and 200 mA. The widest pulse is the input waveform. (Actual output scale: $50 \text{ mV/div} \times 70 \text{ dB} = 158 \text{ V/div}$, and 5 ns/div).

Figure 7.6 shows the circuit output for the diode with the added lifetime-killer impurities (A8.PT.850.1). The widest pulse is the 38 ns wide, 300 V input waveform, measured with the diode shorted out. The remaining ten waveforms show the operation of the diode A8.6 for $I_{\text{BIAS}} = 20, 40, 60, 80, 100, 120, 140, 160, 180,$ and 200 mA, in order of increasing pulse width. In each case, the output fall time is about 1.5 ns. The pulse sharpening action diminishes for output pulse widths above 30 ns. Both the ramp voltage and the fall time increase.

7.4 - Shunt-Connected Pulse-Sharpening Operation

Figure 7.7 shows the "shunt-connected" pulse-sharpening circuit used to obtain the waveforms of Figure 7.8. Figure 7.8 shows five different waveforms. The earliest (i.e., farthest to the left) pulse is the 300 V input waveform, measured with the diode removed from the circuit. The remaining four waveforms show the operation of the diode A8.6 for $I_{\text{BIAS}} = 2, 4, 6,$ and 8 mA, in order of increasing delay. The first sharpened pulse has an extremely fast rise time of about 0.9 ns. The remaining three have longer rise times, on the order of 2 ns.

Figure 7.7 - Fast input shunt-connected pulse sharpening test circuit.

Figure 7.8 - Output of the circuit of Figure 7.7 with diode A8.6 for $I_{BIAS} = 0, 2, 4, 6$ and 8 mA. The earliest pulse is the input waveform. (Actual output scale: $50 \text{ mV/div} \times 70 \text{ dB} = 158 \text{ V/div}$, and 2 ns/div)

Since SRDs tend to work best with waveforms that already have a fast rise time, the input waveform of Figure 7.8 is a best-case waveform. Figure 7.9 shows the output of another shunt-connected circuit using diode A8.6 which uses a slower input waveform (generated by a commercially-available Avtech AVR-3-PW-C-OP1 pulse generator.) This particular unit had a rise time of about 20 ns for a maximum output amplitude of 200 V . Since the pulse source in this circuit has a very low output impedance (compared to the 50Ω sources used above), the pulse sharpening circuit has been inductively coupled. (Details on coupling techniques are available in [HP918]). Figure 7.10 shows that a 4:1 improvement in rise time is easily obtained with the pulse sharpener. (To improve the rise time further, multiple stages can be used).

Figure 7.9 - Slower input shunt-connected pulse sharpening test circuit

Figure 7.10 - Output of Figure 7.9 with diode A8.6 for $I_{BIAS} = 0, 6, 12$ and 18 mA. The slowest pulse is the input waveform. (Actual output scale: 20 mV/div $\times$ 70 dB = 63 V/div, and 10 ns/div)

Figure 7.11 shows six different waveforms from the circuit of Figure 7.7. The earliest (i.e., farthest to the left) pulse is the 300 V input waveform, measured with the diode removed from the circuit. The remaining five waveforms show the operation of the diode A8.PT.850.1 for $I_{BIAS} = 15, 30, 45$ and 60 mA, in order of increasing delay. The first sharpened pulse has an extremely fast rise time of about 0.6 ns.

Figure 7.11 - Output of the circuit of Figure 7.7 with diode A8.PT.850.1 for $I_{\text{BIAS}} = 0, 15, 30, 45$ and 60 mA . The widest pulse is the input waveform. (Actual output scale: $50 \text{ mV/div} \times 70 \text{ dB} = 158 \text{ V/div}$, and 1 ns/div)

7.5 - Discussion

Overall, excellent experimental results have been obtained. The series-connected SRD configuration is very useful in pulse generators for varying the pulse width of a fast input, while also realizing fast fall times. Fall times as fast as 1.7 ns were obtained for 300 V pulses into 50Ω loads, using A8.6 This agrees reasonably well with the theoretical estimate of 1.1 ns (see section 5.6). It was especially pleasing to note that relatively wide pulses (on the order of 10 ns) could be obtained with very low forward bias currents. For instance, in Figure 7.4, a pulse width of 9 ns was obtained with a bias current of 12 mA . As a comparison, Figure 3.13 shows that a pulse width of 4 ns was obtained (with a similar fall time) with an extremely large bias current of 500 mA for the commercial diode designated "no. 88", making power dissipation prohibitively high for wider pulse widths. Evidently, the fabricated diode A8.6 had a much longer effective lifetime - indeed, Tables 1.1 and 3.2 show that the 4500 ns effective lifetime of A8.6 is at least an *order of magnitude* of greater than nearly all of the commercial-available SRDs (Table 1.1) and parasitic SRDs (Table 3.2).

The effective carrier lifetime of A8.PT.850.1 was deliberately decreased by adding platinum impurities. The reduced lifetime of 850 ns (calculated from equation (3.4)) resulted in slightly faster switching times, and significantly higher bias currents, as one would expect. Interestingly, the shorter τ_{EFF} also allowed longer storage times to be used, without significant rise-time degradation. This is due to the fact that the stored charge in the diode is stored closer to the junctions than in a longer-lifetime diode, so less charge diffuses into the middle regions during a given storage time.

The shunt-connected SRD configuration is useful in pulse generators for improving the rise time of input pulses. Figure 7.8 shows that a fast 300 V pulse, with a 2 ns rise time, was sharpened using A8.6 to obtain a rise time of 0.9 ns, with a bias current of 2 mA. This agrees very well with the predicted 1.1 ns switching time. (The rise time increased as the bias, and hence storage time, increased, to a maximum of about 2 ns). Even more impressively, Figure 7.11 shows a 300 V pulse, with a 2 ns rise time, that was sharpened using A8.PT.850.1 to obtain a rise time of 0.6 ns. Table 1.1 shows that this time-rate-of-change is superior to that of all of the listed commercial SRDs.

Figure 7.10 shows a slower 200 V input, with a 20 ns rise time, that has been sharpened to a 5 ns rise time using A8.6, a 4:1 improvement. Multiple sharpening stages can be used to improve this [HP918].

These experimental results clearly indicate that the new WFSRD exceeds the capabilities of currently available SRDs. They also show that by controlling the carrier lifetimes, either the storage times or the switching times can be optimized.

Chapter 8 - The Theory of Drift Step Recovery Diodes (DSRD)

8.1 - Introduction

In traditional step recovery diodes charge is stored in the diode by means of a nearly steady-state forward current flow. That is, the forward bias exists continuously for times comparable to or longer than the hole and electron lifetimes in the active region. However, the more recent high-power drift step-recovery diode (DSRD) uses a short forward bias pulse to introduce stored charge to the device [Grek85], [Grek89], [Belk94], [Foci96]. Since the pulse width is considerably less than the carrier lifetimes, the charge is concentrated near the junctions, which is desirable for a sharp reverse step recovery. Other more complicated high-power devices have been designed with similar pulsed biasing in mind [Grek83], [Gorb88]. For instance, by using this "reversible injection control" [Grek89] two-terminal functional equivalents of the thyristor have been made, which do not suffer from current localization effects characteristic of three terminal devices. Because of this, these new structures have been shown to be capable of operating at much higher power levels than conventional structures, and as such, it has become more important to examine the nature of the forward transient in the basic p^+n^+ diode structure.

8.2 - The Forward Transient In pin Structures

It is possible to obtain an analytical solution for the forward transient for two cases, those being the p^+in^+ structure, where high injection is implicitly assumed, and the p^+sn^+ structure if it is assumed that the s layer (either p -type or n -type) is under low injection. Since the devices mentioned above are power devices, the low injection case is not of interest here. The forward current is assumed to be constant for the duration of the transient.

The solution for a rectangular pin structure can be obtained by solving the differential equation [Vars69]

$$\frac{\partial p(X,T)}{\partial T} = \frac{\partial^2 p(X,T)}{\partial X^2} - p(X,T) \quad (8.1)$$

where $p(x,t)$ is the excess hole density, X is the distance normalized to the ambipolar diffusion length L_d , and T is the time t normalized to the lifetime τ .

Equation (8.1) is subject to the boundary conditions [Vars69],[Bend67]

$$\left. \frac{\partial p}{\partial X} \right|_{X=0} = -\frac{J_F L_d}{2qD_p} \quad (8.2)$$

$$\left. \frac{\partial p}{\partial X} \right|_{X=W_L} = \frac{J_F L_d}{2qD_n} \quad (8.3)$$

and the initial condition [Vars69]:

$$p(X,0) = 0 \quad (8.4)$$

where W_L is the width of the I region, normalized by L_d , and J_F is the forward current density. In obtaining (8.3), it has been assumed that neutrality exists in the I region, such that $p(X,T) = n(X,T)$.

Solving (8.1) using Laplace transform methods, subject to (8.2) and (8.3) yields the intermediate solution

$$p(X, s) = \frac{J_F L_d}{2qD_p D_n} \frac{D_n \cosh(\sqrt{s+1}(X - W_L)) + D_p \cosh(\sqrt{s+1}X)}{s\sqrt{s+1} \sinh(\sqrt{s+1}W_L)} \quad (8.5)$$

which can be rewritten as

$$s \cdot p(X, s) = \frac{J_F L_d}{2qD_p D_n} \frac{D_n \cosh(\sqrt{s+1}(X - W)) + D_p \cosh(\sqrt{s+1}X)}{\sqrt{s+1} \sinh(\sqrt{s+1}W)} \quad (8.6)$$

Taking the inverse Laplace transform of both sides, under consideration of equation (8.4), yields

$$\frac{\partial p(X, T)}{\partial T} = \frac{J_F L_d}{2qD_p D_n} \text{Laplace}^{-1} \left\{ \frac{D_n \cosh(\sqrt{s+1}(X - W_L)) + D_p \cosh(\sqrt{s+1}X)}{\sqrt{s+1} \sinh(\sqrt{s+1}W_L)} \right\} \quad (8.7)$$

or, equivalently,

$$\frac{\partial p(X, T)}{\partial T} = \frac{J_F L_d}{2qD_p D_n} \exp(-T) \cdot \text{Laplace}^{-1} \left\{ \frac{D_n \cosh(\sqrt{s}(X - W_L)) + D_p \cosh(\sqrt{s}X)}{\sqrt{s} \sinh(\sqrt{s}W_L)} \right\} \quad (8.8)$$

By using the Laplace transform pair [Spie65],

$$\frac{\cosh(x\sqrt{s})}{\sqrt{s} \sinh(a\sqrt{s})} \leftrightarrow \frac{1}{a} + \frac{2}{a} \sum_{n=1}^{\infty} (-1)^n \exp\left(-\frac{n^2 \pi^2 t}{a^2}\right) \cos\left(\frac{n\pi x}{a}\right) \quad (8.9)$$

and integrating both sides of (8.8), the final solution can be obtained:

$$p(X, T) = \frac{J_F L_d}{2q W_L D_p D_n} \left[\left(D_p + D_n \right) \left(1 - e^{-T} \right) + 2 \sum_{n=1}^{\infty} (-1)^n \frac{1 - e^{-T \left(\frac{n^2 \pi^2}{W_L^2} + 1 \right)}}{\frac{n^2 \pi^2}{W_L^2} + 1} \left(D_n \cos \left(\frac{n\pi(X - W_L)}{W_L} \right) + D_p \cos \left(\frac{n\pi X}{W_L} \right) \right) \right] \quad (8.10)$$

This solution is considerably simpler and more compact than an equivalent solution presented in [Vars69]. (It should be noted that both equation (8.10) and the solution given in [Vars69] only satisfy the initial condition given in (8.4) in the limit of $t \rightarrow 0$, not at $t = 0$. This is because the boundary conditions (8.2) and (8.3) are in fact inconsistent with the initial condition, a fact which is not always appreciated.)

The evolution of $p(X, T)$ is shown for $\tau = 10 \mu s$, $W = 250 \mu m$, $J_F = 10 A/cm^2$ in Figure 8.1. (The steady state solution is denoted as $p_{ss}(X)$). It is immediately evident that substantial charge injection occurs at both $x = 0$ (the p^+i junction) and at $x = W$ (the i^+n junction) throughout the entire transient.

8.3 - The Forward Transient In psn Structures

If the forward current in a p^+sn^+ diode is sufficiently large, the injected carriers will overwhelm the background doping, allowing the analytical results for a pin diode to be used to determine the transient response. This section quantifies the critical current density above which these results can be used. It will be shown below that even for very light doping, the expression derived above rapidly becomes inaccurate.

Figure 8.1. Calculated charge injection in a pin diode during the forward transient, for several different values of t/τ . The horizontal axis is linear, and the vertical axis is logarithmic. Note that substantial charge injection occurs at both junctions throughout the entire transient. $p_{ss}(X)$ is the steady-state distribution.

Consider a device with a lightly doped n-type middle layer, and assume that quasi-neutrality exists in this layer. Then,

$$p = n - N_D \quad (8.11)$$

Also assume that the doping in the p^+ and n^+ regions is much higher than in the n^- middle region. Then the current at the p^+n^- junction ($x=0$) will be almost entirely a hole current, and the current at the n^-n^+ junction ($x=w$) will be an electron current. Mathematically,

$$J_p(0, t) = J_F \quad (8.12)$$

$$J_n(0, t) = 0 \quad (8.13)$$

$$J_p(W, t) = 0 \quad (8.14)$$

$$J_n(W, t) = J_F \quad (8.15)$$

The transport equations can be written as

$$J_p(x, t) = q\mu_p \left(-V_T \frac{\partial p(x, t)}{\partial x} + p(x, t)E(x, t) \right) \quad (8.16)$$

and

$$J_n(x, t) = q\mu_n \left(V_T \frac{\partial n(x, t)}{\partial x} + n(x, t)E(x, t) \right) \quad (8.17)$$

where V_T is the thermal voltage kT/q . If (8.14) is substituted into (8.16), the electric field at $x = W$ can be found:

$$E(W, t) = \frac{V_T}{p(d, t)} \frac{\partial p(W, t)}{\partial x} \quad (8.18)$$

and similarly, from (8.13) and (8.17),

$$E(0, t) = \frac{-V_T}{n(0, t)} \frac{\partial n(0, t)}{\partial x} \quad (8.19)$$

This allows the current at either junction to be calculated in terms of the doping and carrier distribution. If (8.19), (8.12) and (8.11) are substituted into (8.16), one obtains

$$J_F = -q\mu_p V_T \left(2 - \frac{N_D}{n(0, t)} \right) \frac{\partial n(0, t)}{\partial x} \quad (8.20)$$

Similarly, using (8.18), (8.15) and (8.11) in (8.17) gives

$$J_F = q\mu_p V_T \left(1 + \frac{n(W, t)}{n(W, t) - N_D} \right) \frac{\partial n(W, t)}{\partial x} \quad (8.21)$$

If the first terms in equations (8.16) and (8.17) are identified as diffusion terms, and written as J_{diff} , and if we define

$$f(x, t) = \frac{N_D}{n(x, t) - N_D} \quad (8.22)$$

then (8.20) and (8.21) can be rewritten in the form:

$$\frac{J_{diff}(0, t)}{J_F} = \frac{1}{2 - \frac{f(0, t)}{f(0, t) + 1}} \quad (8.23)$$

and

$$\frac{J_{diff}(W, t)}{J_F} = \frac{1}{2 + f(W, t)} \quad (8.24)$$

Equations (8.23) and (8.24) show that the balance of the drift and diffusion currents at the junctions is affected by the presence of doping in the middle layer. These two functions are plotted as a function of f in Figure 8.2. As $N_D \rightarrow 0$, and hence $f \rightarrow 0$, both functions approach the value 0.5, which of course leads to equations (8.2) and (8.3). In other words, the drift and diffusion currents at both junctions in a pin diode are equal. This remains largely true for $f < 0.1$. As N_D increases, and f increases correspondingly, the current at the $n\bar{n}$ junction is dominated by a drift current, and the current at the $p\bar{n}$ junction is dominated by the diffusion component. Since the diffusion current at the high-low junction becomes small, dn/dx is also small and very little charge is built up at the high-low junction.

Figure 8.2. Diffusion current as a fraction of the total current, at both junctions. In the limiting case of no middle-layer doping, $f = 0$ and the diffusion and drift components are equal. For very heavy doping, $f \rightarrow \infty$ and the high-low junction current is almost entirely drift current, and the p^+n junction current is almost entirely diffusion current.

It is straightforward to show that f increases rapidly with N_D , if one considers the time immediately after the beginning of the forward transient current pulse. At this early time, no holes will have yet traveled to the n^+n junction, so we can write:

$$\frac{dE}{dx} = \frac{q}{\epsilon} (n(W, 0^+) - N_D) \quad (8.25)$$

The current in the bulk of the middle layer must be ohmic, since little charge has been injected and $n \approx N_D$. Thus, in this region,

$$E_{bulk} = \frac{J_F}{q\mu_n N_D} \quad (8.26)$$

If this bulk electric field is assumed to build up from zero over a short distance Δx near the n^+n junction, then the derivative dE/dx in (8.25) can be approximated as $E_{\text{bulk}}/\Delta x$. Then, combining (8.25), (8.26) and (8.22) so as to eliminate $n(w,0^+)$ yields

$$f(W,0^+) = \frac{N_D}{n(W,0^+) - N_D} \approx \frac{q^2 N_D^2 \mu_n \Delta x}{\epsilon J_F} \quad (8.27)$$

An estimate for Δx can be obtained by writing

$$\begin{aligned} \frac{E_{\text{bulk}}}{\Delta x} &\approx \frac{q}{\epsilon} (n(W,0^+) - N_D) \\ &\approx \frac{q}{\epsilon} \left[\left(N_D + \frac{dn}{dx} \Delta x - N_D \right) \right] \\ &= \frac{q}{\epsilon} \frac{dn}{dx} \Delta x \end{aligned} \quad (8.28)$$

The value of dn/dx in (8.28) can be estimated from the electron diffusion current. Of course, the diffusion current to total current ratio varies with f , as discussed above. The most interesting case is for $f=1$, where the diffusion current is $1/3$ of J_F , since the diode behaviors for $f \gg 1$ and $f \ll 1$ are quite different. The case of $f=1$ is a "critical" boundary case. Thus,

$$\frac{dn}{dx} = \frac{J_F}{3q\mu_n V_T} \quad (8.29)$$

Then combining (8.26) to (8.29) to eliminate Δx yields:

$$f(W,0^+) = \frac{J_0}{J_F} \quad (8.30)$$

where

$$J_0 = \sqrt{\frac{3\mu_n^2 V_T}{\epsilon}} (q N_D)^3 \quad (8.31)$$

Hence, for current densities substantially larger than J_0 (say $J_F > 10 J_0$), the diode acts as though it were intrinsic, leading to balanced drift and diffusion currents, and charge injection from both junctions. For current densities substantially less than J_0 (say $J_F < 0.1 J_0$), the charge injection will be dominated by the p^+n junction, and relatively little charge will be stored at the high-low junction. Since $J_0 \propto N_D^{3/2}$, the critical current density $J_F = J_0$ (corresponding to $f \approx 1$) increases moderately quickly with doping, and the usefulness of the intrinsic approximation becomes restricted for even relatively light doping levels.

Physically, equation (8.22) shows that the condition $f(x,t) = 1$ corresponds to an injected carrier density of $n(x,t) = 2 N_D$. Thus, if the forward current is large enough such that $n(w,0^+) \gg 2 N_D$ at the high-low junction immediately after the beginning of the transient (i.e. $J_F \gg J_0$), the diode will act as a pin diode.

The validity of this estimate of J_0 is shown by comparison with MEDICI simulations in Figure 8.3. The hole distribution at $t = 60$ ns is shown for several values of N_D , and hence J_0 (calculated from (8.31)), with $\tau = 10$ μ s, $W = 250$ μ m, and $J_F = 10$ A/cm². (Since the time is the same in each case, the total charge in each of the diode structures is approximately equal.) Clearly, the hole distributions for J_F/J_0 equal to ∞ (i.e., a pin diode), 100, and 10 are very similar and show significant charge injection from both junctions, as expected. In contrast, the hole distributions for J_F/J_0 equal to 0.1 and 0.01 show injection at the p^+n junction only, as expected. The curve for $J_F/J_0 = 1$ is an intermediate case, showing some charge injection from the high-low junction, but much less than for the cases with larger J_F/J_0 ratios. These simulations confirm the theoretical results derived above. (It should be noted that the doping corresponding to J_0 is quite small - only 5.6×10^{13} cm⁻³.)

Figure 8.3. Simulations calculated using the MEDICI simulator to confirm the validity of the derived expression for J_0 . J_0 is calculated from (8.31). For $J_F/J_0 > 10$, the diode behaves like a pin diode, with substantial charge injection at both junctions. For $J_F/J_0 < 0.1$, charge injection occurs exclusively at the p^+n junction. $J_F = J_0$ is an intermediate case. In each case $J_F = 10 \text{ A/cm}^2$, and N_D is varied to change J_0 . In order of decreasing J_F/J_0 the corresponding values of N_D are 2.6×10^{12} , 1.2×10^{13} , 5.6×10^{13} , 2.6×10^{14} , and $1.2 \times 10^{15} \text{ cm}^{-3}$.

Equation (8.30) predicts how the charge is injected at short times after the beginning of the transient. Obviously, as time progresses, the value of $f(W,t)$ will change, since substantial charge is stored near the high-low junction in the steady state. The key turning point occurs when injected holes from the p^+n junction reach the high-low junction. This of course will increase $n(W,t)$, and increase $f(W,t)$. In other words, double injection occurs [Dean69], and injected charge will rapidly build up at the high-low junction after this time. This time can be estimated by dividing the middle region width W , by the drift velocity, such that

$$t_{di} = \frac{W}{\mu_p E_{bulk}} \quad (8.32)$$

This can be rewritten using (8.26):

$$t_{di} = b W \frac{q N_D}{J_F} \quad (8.33)$$

where

$$b = \frac{\mu_n}{\mu_p} \quad (8.34)$$

Figure 8.4 illustrates the validity of this calculation for $W = 250 \mu\text{m}$ and $J_F = 10 \text{ A/cm}^2$, for a range of N_D from 10^{14} to $5 \times 10^{14} \text{ cm}^{-3}$. The hole concentration is plotted at $t = t_{di}$ for each particular doping. In each case, the peak injected charge at the high-low junction is just beginning to become significant, reaching a density approximately equal to N_D . (Figure 8.1 shows that the steady state distribution is between 10^{16} and 10^{17} cm^{-3} , about two orders of magnitude higher than N_D .)

Of course, even after $t = t_{di}$, diodes with $J_F < J_0$ will still have less charge injected at the high-low junction than diodes with $J_F > J_0$, but the difference will be less noticeable than for $t < t_{di}$.

Figure 8.4. Simulations calculated using the MEDICI simulator. The injected hole density at the high-low junction at $t = t_a$ is shown for several different dopings. In each case, the peak density $\approx N_D$. The charge injected at the high-low junction grows rapidly after $t = t_a$ due to the onset of double injection.

8.4 - Implications For Pulse Sharpening Diodes Design Theory

The use of drift step-recovery diodes in pulse sharpening applications has been described in [Grek85], [Grek89], [Belk94], [Foci96]. An important characteristic describing the reverse transient of any step recovery diode is the ramp voltage, which is the voltage built up across the diode just before the fast sharpening transient begins. The ramp voltage should be as small as possible to obtain an ideal step waveform. In the DSRD, the fast transient begins when the charge sweeping-out boundary [Bend67] emanating from the p-n junction meets the sweeping-out boundary emanating from the high-low junction. If the distance between the p-n junction and the meeting point of the sweeping-out boundaries is termed W_Q , the ramp voltage V_{RAMP} can be found by applying

Poisson's equation to the fixed ionized charge and the mobile charge, assumed to be moving at the saturation velocity v_s . Thus,

$$V_{\text{RAMP}} = \frac{q}{2\epsilon} \left(N_D + \frac{J}{q v_s} \right) W_Q^2 \quad (8.35)$$

The voltage developed across the quasineutral region between $x = W_Q$ and the high-low junction will be much smaller than the voltage developed across the p-n junction space charge region [Bend67], and is ignored.

To minimize V_{RAMP} , it is necessary to minimize W_Q . This implies maximizing $|dn/dx|$ at the p-n junction such that the charge injected by the forward transient is kept very close to the junction. From the preceding section, we can see that this requires that $J_f < J_0$. Significant improvement in ramp voltage will occur as J_f is brought down from $10J_0$ to $J_0/10$, and relatively little improvement will occur below this, as suggested by Figure 8.2. For instance, a DSRD designed to operate at 1700 V, with $N_D = 10^{14} \text{ cm}^{-3}$, will have $J_0 = 24.8 \text{ A/cm}^2$. For a cross sectional area of 0.3 cm^2 , this corresponds to $I_0 = 7.4 \text{ A}$. A diode with these parameters was manufactured and presented in [Grek85], where a value of $I_f = 3 \text{ A}$ was used. Clearly these values of J_f and I_f fall within the predicted desirable range. Decreasing J_f further would have had the undesirable effect of either increasing the cross-sectional area and the junction capacitance, or increasing the forward pulse width t_f , which has its own limits as discussed below.

The expression derived for J_0 can also be used to estimate the maximum charge consistent with good step recovery action that can be stored in a DSRD. The charge stored in a DSRD during the forward bias pulse is given by

$$Q_+ = I_f t_F \quad (8.36)$$

where t_f is the duration of the forward pulse. Grekhov noted in [Grek85] that for the injected charge to remain near the junction, t_f should be much smaller than the diode transit time t_T , where

$$t_T = \frac{W^2}{2D_p} \quad (8.37)$$

If we choose

$$I_F \approx \frac{I_0}{2} \quad (8.38)$$

and

$$t_F \approx \frac{t_T}{100} \quad (8.39)$$

(such that the effective characteristic length, L_{eff} , of the injected carrier distribution is $W/10$) as reasonable maximum values, the maximum Q_- can be determined as a function of N_D and W . A more useful exercise is to calculate the reverse transient storage time t_s as a function of V_{BR} and W , where

$$t_s = Q_- / \frac{V_{BR}}{2R_L} \quad (8.40)$$

where Q_- is the maximum charge that can be removed from the diode during the reverse transient. It is important to note that Q_- and Q_+ are not necessarily the same thing. For a wide-base diode under low injection, the maximum net charge that can be extracted from a diode is $Q_-/2$ [Lind65]. Similarly, for a narrow-base diode, $Q_- = 2/3 Q_+$. However, for the high-injection case examined here,

$$Q_- = Q_+ \quad (8.41)$$

as Belkin and Shulzchenko [Belk94] and Focia et al. [Foci96] have reported experimentally. Grekhov's [Grek85] reported experimental values of $Q_+ = (400 \text{ ns})(3 \text{ A})$ and $Q_- = \frac{1}{2} (50 \text{ ns})(34 \text{ A})$, resulting in $Q_+/Q_- = 0.71$; however computer simulations reported below cast some doubt on the accuracy of this.

The breakdown voltage V_{BR} can be calculated from [Bali87]

$$V_{BR} = 5.34 \times 10^{13} N_D^{-3/4} \quad (8.42)$$

where N_D is in cm^{-3} . In equation (8.40), it is assumed that the diode is operated just below breakdown, and that the pulse to be sharpened is a linear ramp (hence the average voltage of $V_{BR}/2$). To determine the cross-sectional area of the device, the DSRD design equation from [Grek85] is used:

$$\frac{V_{BR}}{A} = q v_s N_D \quad (8.43)$$

Consideration of equations (8.31) and (8.36)–(8.43), and assuming $R = 50 \Omega$, allows N_D and A to be chosen for a particular V_{BR} . However, this leaves one unspecified physical parameter, W . Making W large will increase the maximum stored charge Q_+ , but it will also increase V_{RAMP} . Ultimately, computer simulations are required to confirm the proper choice of W . However, for the convenience of calculations, the width W will be normalized as a parameter, called the "width factor", or WF , where:

$$W = WF \times 2.67 \times 10^{10} N_D^{-7/8} \quad (8.44)$$

For $WF = 1$, W is equal to the width of the depletion region at breakdown [Bali87]. (In (8.44), W is in cm and N_D is in cm^{-3} .) In other words, for $WF=1$, the depletion region consumes the entire middle layer at V_{BR} . For $WF > 1$, portions of the middle layers are

never covered by the depletion region, and for $WF < 1$ the diode is a punchthrough device. (If a punchthrough structure is used, equation (8.42) no longer applies.)

Consideration of equations (8.34)-(8.44) produces the plot shown in Figure 8.5. The device presented in [Grek85] corresponds to $WF = 1.65$, and $V_{BR} = 1700$ V, for which the ideal t_s is predicted to be about 57 ns. This agrees rather well with the 50 ns value that was used in the experiment. It was reported that the step recovery action degraded noticeably above 50 ns, as one would expect.

Figure 8.5. The curves on this design chart show the maximum practical storage time t_s in nanoseconds, for a psn diode with a middle-layer width factor WF of 1, 1.65, 2, or 3, and breakdown voltage V_{BR} (in Volts).

It is apparent from Figure 8.5 that the DSRD structure is of little use below 500 V, as the maximum useful storage times become very short.

Previous design approaches for DSRDs [Grek85] did not specify a simple method of choosing J_F and w . The equations presented above, in the form of (8.31) and Figure 8.5, partially rectify this situation. The equations given above do not guarantee that a

given diode structure can be used as a DSRD. Choosing $J_f \ll J_0$ ensures that the ramp voltage is minimized as much as possible for a particular structure, but it does not ensure that the ramp voltage is insignificant relative to V_{BR} . To calculate V_{RAMP} exactly computer simulations are required. The next section reports the results of such simulations.

8.5 - DSRD Ramp Voltage

To develop a design approach for the DSRD ramp voltage, simulations were performed using the MEDICI device simulator, for fifteen devices. Values of N_D , A , and I_f were determined using the theory presented in the last section for devices with V_{BR} values of 500 V, 1000 V, 1500 V, 2000 V, and 2500 V. For each of these voltages, three values of WF were considered: 1, 2, and 3. Knowledge of WF allowed t_f and t_s to be calculated for each device.

The results of the transient simulations are very simple. For $WF = 1$, $V_{RAMP}/V_{BR} = 0.1$, regardless of V_{BR} . Similarly, for $WF = 2$, $V_{RAMP}/V_{BR} = 0.25$, regardless of V_{BR} , and for $WF = 3$, $V_{RAMP}/V_{BR} = 0.4$, regardless of V_{BR} . It is not surprising that for a given WF the V_{RAMP}/V_{BR} ratio is independent of V_{BR} , because for each diode with the same WF the shape of the injected charge is identical, if it is normalized to the width of the middle layer. Thus, the normalized position where the sweeping-out boundaries from the left and right meet (initiating the step recovery action) will be identical for diodes with the same WF. Similarly, the normalized width of the depletion region at V_{BR} is also identical for devices with a given WF, by definition. Thus the ratio of the two positions, and hence the ratio of the corresponding voltages (V_{RAMP} and V_{BR}) will be identical.

This considerably simplifies the design of DSRDs. Typically, one wishes to have $V_{RAMP}/V_{BR} \leq 0.1$, and as large a storage time as possible, so $WF = 1$ is the ideal choice. With WF fixed, all parameters are now uniquely specified for a given V_{BR} . With this in mind, Figure 8.5 can be simplified and enlarged, as in Figure 8.6. It is now evident that the DSRD is restricted to high voltages, of at least 1 kV, if $V_{RAMP}/V_{BR} \leq 0.1$ is to be

achieved. Below 1 kV, the storage time becomes too short to work with, as does the forward bias pulse width, t_f .

Figure 8.6. Maximum practical storage time t_s and the corresponding forward bias time t_f in nanoseconds, for a psn diode with the ideal middle-layer width factor WF of 1 and breakdown voltage V_{BR} (in Volts).

8.6 - DSRD Transition Times

Grekhov et al [Grek85] calculated that the maximum voltage rate of change for saturation-velocity limited silicon devices is 2000 V/ns. Since the current density and carrier distributions change radically during the diode reverse transient, it is not possible to sustain the extraction velocity of the carriers at the saturation velocity for the entire step recovery transient, so in practice one can only expect to achieve a fraction of this maximum transition speed. The switching time results (t_r) from some of the simulations described in the previous section (with the addition several high-voltage devices) are summarized in Table 8.1, along with the physical and electric parameters used in the simulations. Table 8.1 shows that the maximum realizable voltage-rate-of-change is about

500 V/ns, which is the approximate maximum value for conventional SRDs and WFSRDs as well (see Table 1.1). (It is not clear why there appears to be a rate-of-change minimum around the 2500 V device.) Also, the low values of τ_{EFF} at and below 1 kV again show the operating voltage restrictions of the DSRD.

Figure 8.7 shows a typical simulated waveform for the 4000 V device specified in Table 8.1.

Table 8.1 - Switching times for various DSRDs, with $WF = 1$. τ_{EFF} is calculated from equation (3.4), using the values in the table.

V_{BR} , V	Calculated Physical Parameters			Calc. Electrical Parameters			Simulation Results			
	N_D , cm^{-3}	A, mm^2	L, μm	I_F , A	t_F , ns	t_S , ns	t_R , ns	V_{BR}/t_R , V/ns	V_{RAMP} , V	τ_{EFF} , ns
500	5.1×10^{14}	1.75	36.3	2.47	5.5	2.7	1.0	500	50	12.2
1000	2.0×10^{14}	8.83	81.5	3.11	27.7	8.6	2.1	476	100	59.5
1500	1.2×10^{14}	22.7	131	3.56	71.2	16.9	3.1	484	150	151
1700	9.9×10^{13}	30.5	151	3.71	95.4	20.8	3.6	472	170	208
2000	8.0×10^{13}	44.5	183	3.92	139	27.3	5.5	364	200	292
2500	5.9×10^{13}	74.9	237	4.22	235	39.7	8.9	281	250	590
3000	4.7×10^{13}	114.6	293	4.49	359	53.7	7.4	405	300	744
4000	3.2×10^{13}	224.3	411	4.94	703	86.8	7.8	513	400	1450
5000	2.4×10^{13}	377.5	533	5.32	1183	126	9.9	505	500	2430

Figure 8.7 - Optimum pulse sharpening action of the 4000 V device described in Table 8.1. The sharpened output 10%-90% rise time is 7.8 ns.

These results do not agree entirely with Grekhov's [Grek85]. In [Grek85], a 1700 V diode was reported with a 1.5 ns rise time, giving a V_{BR}/t_R ratio of 1133 V/ns. This seems overly fast, compared to the results listed in Tables 8.1 and 1.1. Figure 8.8 shows the results of a Medici simulation reproducing the conditions described in [Grek85] (i.e., $N_D = 10^{14} \text{ cm}^{-3}$, $A = 30 \text{ mm}^2$, $L = 250 \text{ } \mu\text{m}$, $I_f = 3 \text{ A}$, $t_f = 400 \text{ ns}$, $t_s = 40 \text{ ns}$). From the simulation, the 10%-90% rise time is calculated to be 15.2 ns. If just the fast part of the transient is considered, from 22% - 90%, the corresponding rise time is 3.7 ns, which is in line with the results of the simulations given in Table 8.1. It is not clear what transition time definition was used in [Grek85], particularly since the output waveform appears to be hand-drawn, rather than photographed. Similarly, Grekhov has reported a 2000 V, 2 ns device in [Grek89], yielding 1000 V/ns, but again the actual output waveform photo is not shown. For the same voltage, the optimized device of Table 8.1 indicates a 10%-90% rise time of 5.5 ns.

Figure 8.8 - Simulation results for the diode and circuit conditions in [Grek85].

Also, Figure 8.8 suggests that the value of Q/Q_+ of 0.71, calculated from the values given in [Grek85] is too low, as additional charge is removed from the diode after the input voltage has reached 1700 V. In other words, the voltage ramp time could have been increased to $Q/Q_+ = 1$. This simulation result tends to support the use of equation (8.41), and agrees with [Belk94].

The simulated results are in better agreement with the recent experimental results reported in [Foci96]. A rise time of approximately 5 ns is reported for a voltage swing of 1700 V, for an average switching rate of 340 V/ns. Also, the reported values of storage time and I_F/I_R yield an effective lifetime of 250 ns. Both of these values agree reasonably well with the results for the 1700V device given in Table 8.1.

8.7 - Other DSRD Issues

The maximum operating voltage for a single DSRD is somewhat limited by the fact that the diode area increases very rapidly (and undesirably) with voltage. Combining equations (8.42) and (8.43) shows that

$$A \propto V_{BR}^{7/3} \quad (8.45)$$

whereas the desirable increase in storage time t_s is much slower:

$$t_s \propto V_{BR}^{5/3} \quad (8.46)$$

For this reason, at higher voltages it may be advantageous to use multiple series-connected DSRDs rather than a single device. Belkin and Shulzchenko [Belk94] used this approach to obtain 6 kV pulses, with four lower-voltage DSRDs connected in series. This approach also has the advantage that higher middle layer dopings can be used, which makes device fabrication easier.

8.8 - Conclusion

In this section, the evolution of the carrier distributions in p^+sn^+ diodes during the forward transient has been considered. A critical current density, J_0 , has been derived. For $J \gg J_0$, a p^+sn^+ diode will behave as a pin diode, with significant charge injection at both junctions. For $J \ll J_0$, significant charge injection will occur only at the pn junction for times $t < t_d$. For $t > t_d$, carriers will be injected by both junctions. Interestingly, doping levels in the middle layer (typically 10^{14} cm^{-3}) can be orders of magnitude less than the forward steady state carrier concentrations (typically $> 10^{16} \text{ cm}^{-3}$), and yet can dramatically affect the evolution of the carrier distributions.

The critical current J_0 has been shown to be an important parameter in the design of drift step recovery diodes. To minimize the ramp voltage, J_F should be less than J_0 . Also, knowledge of J_0 allows an estimate of the maximum usable stored charge in a DSRD. This results in a much more comprehensive design theory for DSRDs than that which was previously available. This parameter should prove useful in the design of several other high-power devices that rely upon transient forward biasing, or reversible injection control.

Chapter 9 - Concluding Remarks

9.1 - Summation and Conclusions

Two approaches to realizing high-voltage step recovery diodes have been considered in this thesis. By examining switching transients in commercially available power diodes, and by considering the results of computer simulations, a new step recovery mechanism has been proposed and demonstrated. It has been shown that these high voltage SRDs can be fabricated by using a diffused structure on a lightly-doped p-type substrate.

Diodes based on this principle were successfully fabricated and demonstrated in several different common circuit configurations. Switching times as low as 0.6 ns were shown for a 300 V transient into a 50 Ω load. This is considerably better than what is possible with commercially available devices. It has also been shown that these devices can be fabricated with very long effective carrier lifetimes, which makes them very easy to use in practical pulse generation circuits. Indeed, this author is pleased to report that these devices were commercialized even before the defense of this thesis. These diodes have been incorporated into shipped units of the Avtech Electrosystems Ltd. line of AVRF pulse generators.

These new diodes have been termed "wide field step recovery diodes (WFSRDs)". Theoretical expressions were developed to permit the optimum design of these devices. In particular, expressions for predicting the transition time and estimating the ramp voltage of WFSRDs were obtained. A straightforward, two-step method of empirically estimating the breakdown voltage of WFSRDs, and diffused rectifiers in general, was also presented. This theory resulted from the unexpected observation that there appears to be an approximate one-to-one relationship between the diode breakdown

voltage and the critical electric field of the diode, regardless of the exact details of the diffused structure.

The design theory for the previously-proposed "drift step recovery diode (DSRD)" was also examined, and found to be incomplete. Previous design theories had not considered the nature of the forward transient used to bias the DSRD. By considering the nature of the forward transient, a critical current density related to the substrate doping has been derived. For forward transient currents below this level, the injected charge tends to remain close to the p+ n- junction, which is desirable for DSRD operation. Currents above this level tend to inject charge at both junctions, which is undesirable. This provides an additional design constraint, and allows a definitive choice of the optimum bias current. This also permits an estimate of the maximum stored charge consistent with step recovery action. It is shown that previous designs reported in the literature agree well with the new theories. The new theory justifies the previously unjustified choices of bias current and the lightly-doped layer width, and agrees well with experimental observations of the maximum stored charge consistent with step recovery action.

Also, in considering the general nature of the forward transient, a new expression for the charge carrier density evolution with time during the forward transient in a pin diode has been derived. This expression is considerably more compact than the conventional expression.

It was found experimentally that WFSRDs offer the possibility of very long carriers lifetimes. Indeed, the experimentally measured lifetimes were orders of magnitude better than those of conventional SRDs. WFSRDs are not expected to be useful above 1 kV. In contrast, the DRSDs have been found to be useful primarily above 1 kV, and offer lifetimes only somewhat better than conventional SRDs. As such, these two devices have been found to occupy different application niches.

9.2 - Alternative Approaches to High Speed Semiconductor Switching

It is worth considering the avenues to high-speed diode switching that have not been explored in the main body of this thesis. For instance, other semiconductor materials might be considered for use in these devices. However, a cursory examination of the properties of other readily available semiconductors shows that silicon offers the best compromise between critical breakdown fields and hole mobility. Silicon carbide offers high breakdown voltages, but much lower mobilities. Gallium arsenide offers comparable hole mobility, but lower breakdown fields. No reasonable semiconductor offers both improved breakdown and mobility. Furthermore, direct bandgap semiconductors (like GaAs) suffer the serious disadvantage of inherently lower carrier lifetimes, which is highly undesirable in SRDs.

However, interesting possibilities may arise from the clever use of heterostructures. For instance, one might envisage a step recovery diode band diagram like that shown in Figure 9.1. In this case, a silicon-germanium alloy layer exists in the lightly-doped middle region, adjacent to the p^+ n junction. The injected charge would accumulate in the valence band pedestal next to the junction, due to the favorable energy conditions. This would ensure that the charge remains right at the junction, as is desired in a SRD, while maintaining a wide lightly-doped layer capable of withstanding a large reverse voltage. However, incorporation of SiGe layers into Si lattices still represents state-of-the-art laboratory technology [Meye92], which has certainly never been tried at the reverse biases required here. The question of whether or not reasonable lifetimes could be obtained in view of the likely dislocations and other lattice defects also arises.

Figure 9.1 - Possible heterostructure SRD, using Si-Ge alloys.

This thesis has focused on step-recovery diodes, in the traditional sense. That is, these step-recovery diodes operated primarily due to charge storage effects. Other devices exist, which might be used in SRD-like applications, but which owe their behavior to more exotic effects. For instance, extremely fast transitions have been reported by Grekhov et al. [Grek81], [Grek89] using delayed-avalanche devices. Essentially, a very fast-rising reverse pulse is applied to a diode. The rate of rise is sufficiently fast that the critical electric field of the diode can be greatly exceeded for a few nanoseconds without generating significant ionization current. Suddenly, an ionization wave will develop and engulf the space charge region with carriers, causing a voltage collapse. The propagation speed of the ionization wave is not limited to the carrier saturation velocity, so the voltage transition can be very rapid. Switching speeds of 0.2 ns have been reported for 3000 V, 60 A transitions [Grek81]. Switching times of 50 ps have been reported for switched powers of 100 kW [Grek89]. These devices differ significantly from conventional SRDs in their mode of operation, and also from the fact that once the ionization plasma is extinguished, the diode voltage rises again. Also, this diode *requires* an already extremely-fast input waveform.

This thesis has also focused on single devices. Naturally, fast high voltage switching can also be obtained by series-connecting many lower voltage conventional SRDs. One example has been reported experimentally, where eight carefully matched

conventional SRDs were connected to obtain a 400 to 500 V, 0.8 ns composite SRD [Brow87]. This careful matching will represent a considerable expense in the fabrication of such devices. Also, mechanical reliability can be a concern in stacked devices. More seriously, commercially available stacked SRDs (such as the M/A-COM 44950 series) are aimed primarily at frequency multiplier operations. Achieving long lifetimes and storage times in multiplier diodes is not a priority, since the diode switches once per cycle, and is typically used at GHz frequencies. The short lifetimes make these diodes essentially useless in the series-connected pulse sharpening configuration. The short storage times will also limit the shunt-connected circuits to sharpening input signals that are already quite fast. These short storage times are an inherent feature in stacked SRDs, as can be seen in equation (3.4), repeated here:

$$\frac{t_S}{\tau_{\text{eff}}} = \ln \left(1 + \frac{I_F}{I_R} \right) \quad (9.1)$$

Relative to a single SRD, a stack of N SRDs will have an N -times larger I_R , since the allowable operating voltage and load voltage is N times larger. However, I_F generally can not be increased by N times, due to the increased steady-state power dissipation and thermal considerations. Thus, from (9.1), t_S will be considerably lower for a given τ_{eff} .

The stacked approach does offer a viable alternative in certain cases. Of course, it should be pointed out that the WFSRDs and DSRDs discussed in this thesis could also be stacked to generate very-high voltage composite devices.

Exceedingly rapid voltage transitions have also been predicted for pin diodes used as photoconductive switches [Sun92]. These diodes are biased in the reverse state, and very few free carriers exist until the diode is illuminated with a rapid, high intensity laser pulse, which generates carriers, collapsing the voltage across the diode. This, however, is a rather complex and expensive approach.

9.3 - Future Work Beyond This Thesis

The theory presented within this thesis for the WFSRD does not present a simple method, aside from simulations, of calculating the maximum storage time (and carrier lifetimes) consistent with good step recovery action. As it is desirable to make the storage times as long as possible for pulse sharpening purposes, it would be desirable to have a simple method of calculating it. Again, this is problematic, since it requires exact knowledge of the carrier distribution in the diffused psn diode during the forward steady state. As discussed earlier, the lack of clear boundary conditions makes this an extremely challenging problem to solve analytically.

This thesis has dealt exclusively with high-voltage SRD device design. The study of SRD circuits is also a worthwhile endeavor. The pulsed biasing of the DSRD represents an increase in circuit complexity over conventional SRD circuits, especially since the DSRD operates at much higher voltages. Considerable opportunities exist to propose and experiment with new practical pulsed-bias DSRD circuits.

One other promising area of study is the examination of the benefits and tradeoffs of connecting arrays of WFSRDs and DSRDs in series and in parallel to create a high-voltage, high-current, ultra-fast composite switch. Dr. Alexei Kardo-Sysoev reports that a circuit consisting of 120 stacked DSRDs has been used to sharpen 100 kV pulses, to rise times on the order of 1 ns, resulting in 100 MW of switched power [Kard96]. Very little has been published on this topic, particular theoretically, even including conventional SRDs.

Appendix A - The High-Voltage CV Measurement Instrument

A.1 - Introduction

Capacitance-voltage profiles are widely used as a diagnostic tool in the study of semiconductors. In particular, the C-V profiles provide insight to the doping profiles of semiconductor junctions, and in special cases can be related directly to the doping profile [Hili60]. Although numerous instruments are commercially available to measure the small-signal differential capacitance of semiconductor junctions [Palm90], these instruments generally do not allow DC biases of more than 200V. As an example, the Boonton 71-AR meter allows a DC bias to be directly applied for voltages up to 200V. For measurements at higher voltages, the bias can be applied by connecting the test capacitance to the meter through a large DC-blocking capacitor, and by applying the DC bias to the test capacitance through two parallel resonant filters [Boon]. This leads to several difficulties. The parallel filters must be closely tuned to 1 MHz, and the Q of the inductors used in the filter must be greater than 200. Inductors with such high Q are not widely available. Furthermore, both the DC-blocking capacitor and the bypass capacitor on the DC bias power supply must have a voltage rating greater than the maximum bias.

The circuit presented here eliminates these difficulties. Only one component requires the full DC bias rating, and no high Q inductors are required.

A.2 - Theory

Figure A.1 - Diode model used for measuring C-V profiles in reverse bias. The current source represents the DC leakage current, and the capacitor models the diode junction capacitance.

A pn junction can be modeled as a parallel combination of a voltage-dependent current source and a voltage-dependent capacitance, as shown in Figure A.1. If a DC bias voltage, A , is applied to the cathode of a diode, and a small AC signal $B\sin(\omega t)$ is applied to the anode, as shown in Figure A.1, the voltage across the diode will be

$$V_d = A - B \cdot \sin(\omega t) \quad (\text{A.1})$$

and the resultant current will be

$$I = I_L(V_d) - C(V_d)B\omega \cos(\omega t) \quad (\text{A.2})$$

As a simplifying assumption, one can assume the leakage current and the capacitance depend only on the DC component of the diode voltage, such that

$$I = I_L(A) - C(A)B\omega \cos(\omega t) \quad (\text{A.3})$$

In general, this is a reasonable assumption for large values of ω and for small values of B and I_L . This is not a good assumption in forward bias or in reverse breakdown. However, it is generally the C-V profile in the reverse bias before breakdown that is of interest.

If this current flows through a resistance R , the resultant voltage will be

$$V_R = I_L(A)R - C(A)RB\omega \cos(\omega t) \quad (\text{A.4})$$

Thus by observing the AC component of this voltage on an oscilloscope or on an AC voltmeter, the capacitance $C(A)$ can be measured, since R , B , and ω are known. Also, the diode leakage current can be measured by observing the DC component.

A.3 - Circuit Implementation

The circuit shown in Figure A.2 implements equations (A.1) - (A.4) directly. The DC bias, A , is applied to the cathode of the diode under test (DUT). The LH0032 is a high-speed, low bias current op amp used as a unity gain voltage follower to apply the AC test signal $B\sin(\omega t)$ to the anode of the DUT. Since the inverting input of the LH0032 has such a small bias current (typically < 500 pA), the diode current must flow through the resistor R , yielding a voltage across the resistor given by equation (A.4). The AMP-05 is a high-speed, low bias current instrumentation amplifier, used in this circuit as a unity gain voltage buffer. Since the voltage at the non-inverting and inverting inputs of the LH0032 will be equal (ignoring, for now, a small DC offset), the voltage across the input of the AMP-05 will equal the voltage across the resistor R .

Figure A.2 - Schematic diagram of the high-voltage C-V profiler circuit. The output voltage V_R is directly proportional to the capacitance of the diode under test (DUT)

The inverting input of the AMP-05 is connected to the non-inverting input of the LH0032, rather than the inverting input, to minimize the parasitic capacitance present at the anode of the DUT. The inverting input of the LH0032 will contribute some parasitic capacitance, which can not be removed. However, this capacitance, and any other stray capacitances to ground will appear as a constant offset in the measurements, which can be accounted for by measuring the output with the DUT removed.

By separating the DC bias and the AC test signal, the amplifiers and the sensing resistor R can all be standard low-voltage components. The only component that requires a high voltage rating (aside from the DUT itself) is the bypass capacitor C_b on the DC bias power supply. This capacitor serves two functions; it provides the AC path to ground for the AC test signal, and secondly, in conjunction with the inductor L, it suppresses any

ripple present in the DC power supply. The circuit will actually measure the series combination of the DUT capacitance $C(A)$ and C_b , so one should have $C_b > 100 C(A)$ over the voltage range of interest for C_b to introduce less than 1% error.

For the measurements presented here, the values $R = 31.9 \text{ k}\Omega$, $B = 100 \text{ mV}_{pp}$ (35.3 mV_{RMS}), $\omega = 2\pi \times 1 \text{ MHz}$ were used. This yields a capacitance sensitivity of $\omega BR = 20.0 \text{ mV}_{pp}/\text{pF}$, and a leakage current sensitivity of $1/R$, or $31.3 \text{ mV}_{dc}/\mu\text{A}_{dc}$. The AC output voltage, and hence the capacitance, was measured using a Hewlett-Packard HP400F AC millivoltmeter. With no DUT in the circuit, a parasitic offset capacitance of 4.0 pF was observed.

To generate the 100 mV , 1 MHz sine wave a standard crystal oscillator circuit [Matt83], which generates a stable 1 MHz square wave, followed by a 4 pole 0.5dB -ripple Chebyshev lowpass filter [Horo89] nominally tuned to 1.2 MHz was used. A Kepco ABC1000M power supply was used to generate the DC bias.

A.4 - Discussion

The primary advantage of this circuit is the relative ease with which small-signal capacitances can be measured at kilovolt DC biases. There is no inherent limit on the maximum DC voltage that can be applied to the DUT, other than practical considerations. That is, the bypass capacitor C_b must have a voltage rating greater than the maximum DC bias, and the physical construction of the circuit must be appropriate for high-voltage use.

Since the amplitude of the AC test signal, B , can be measured accurately with less than 1% error using an oscilloscope or by other means, and the frequency is crystal-controlled, the accuracy of the circuit is primarily limited by the tolerance of R and the gain-setting resistors of the instrumentation amplifier. These errors can be reduced by measuring the output with a known capacitance and adjusting the gain accordingly, otherwise one could expect 2% error. The nonlinearity of the AMP-05 amplifier is

typically 0.001%, and can be ignored. As mentioned earlier, C_b must be sufficiently large to eliminate its effect on the measured capacitance.

The LH0032 and AMP-05 were chosen for their low input bias currents. The LH0032 typically has $I_b < 500$ pA, and AMP-05 has $I_b < 30$ pA. Since the AC current induced in the diode will be on the order of several microamps for the circuit values used above, these input bias currents can be neglected. Both amplifiers will introduce a small DC offset voltage, however this will not affect the capacitance measurement, which is based on an AC signal. Although the DC component can be used to measure the leakage current, better instruments are available for this purpose. However, monitoring the DC component does allow the user to avoid the onset of diode breakdown.

If the current-sensing resistor R is made too large, the instrumentation amplifier slew rate may be exceeded. The typical AMP-05 slew rate is 7.5 V/ μ s, which limits the output voltage to 2.4 V_{pp} for a 1 MHz signal. Thus, in consideration of equation (A.4), R can not exceed 190 k Ω for a 20 pF capacitance. In practice, it is wise to make R smaller, such that the resistive component of R is much smaller than the impedance of the parasitic capacitance that will exist in the resistor(s). (For this reason, when implementing R in a circuit, it is desirable to use resistors in series rather than resistors in parallel, to reduce parasitic capacitance across R . Parasitic inductance can be neglected at these frequencies.)

The input sine wave must be relatively pure, since the measured current is a function of the derivative of this input. The sinewave output available from typical function generator instruments and integrated circuits are often formed using diode forming networks, which will produce slight "knees" in the generated sine wave, which are magnified in the derivative [AD76]. A filter is necessary to remove the undesired harmonics.

For special cases, doping profiles can be related directly to the C-V profiles [Hili60]. However, these relationships generally involve C and dC/dV . Since C varies so slowly at higher voltages a digital AC millivoltmeter must be used to obtain the necessary precision, rather than the analog HP400F. There is no inherent limitation in the circuit of Figure A.1, other than the noise floor, preventing a satisfactory degree of precision from being obtainable.

The results presented here have also been reported by this author in [Chud95a].

Appendix B - A High Speed, Medium Voltage Pulse Amplifier For Diode Reverse Transient Measurements

B.1 - Introduction

A dc-coupled non-linear pulse amplifier circuit is presented in this chapter. The circuit presented can produce 40 V peak-to-peak pulses with 3 ns rise and fall times. This speed is obtained by using Class D transistor amplifier stages. This circuit is shown to be useful for measuring the reverse recovery transients of fast switching diodes such as the 1N4148, and fast recovery power rectifiers. The results presented here have also been reported by this author in [Chud95b].

The fastest op amps available today, such as the Comlinear CLC203 are capable of generating pulses with 20 V peak-to-peak amplitudes and 4 ns rise times [Com93]. Sub-nanosecond switching speeds can be obtained for amplitudes of up to 100 V or higher by using step recovery diode pulse sharpening circuits [HP918]. However, in many cases this method is needlessly expensive and too fast, since very careful physical circuit construction is required to avoid inductive ringing and electromagnetic interference. Between these two circuit approaches there are relatively few circuits that will allow the generation of pulses of several tens of volts amplitude in 50 Ω loads, with rise times of a few nanoseconds.

This appendix presents a circuit that uses Class D transistor switches. In a Class D amplifier, the transistors switch between a high-voltage, zero-current cutoff state and the low-voltage, high-current saturation state. This produces very low steady-state losses. Unfortunately, significant power dissipation can occur during switching. For these reasons, Class D circuits have traditionally been used for low frequency, high power applications [Page65], [Chud69]. In addition, Class D circuits have traditionally been

used in pulse width modulation circuits, with low-pass filters on the output to obtain a sine wave output. However, this appendix shows that if the low-pass filter is dispensed with, Class D switching circuits can be built for use as pulse amplifiers with switching times of a few nanoseconds.

The pulse amplifier presented in this paper was developed to provide a high speed voltage pulse source for reverse recovery measurements in diodes. Reverse recovery measurements are widely used as a tool in the study of diodes, since they can provide information about the diode structure and the carrier lifetimes inside the diode.

B.2 - Amplifier Circuit

Figure B.1 shows the amplifier circuit to be considered. It is based on a pulse amplifier chain presented by Krauss et al [Krau80] which was originally intended for a pulse width modulation circuit, with several modifications to allow for high speed operation. The level shifting diodes D2, D3 and D4 have been added to allow bipolar operation. The zener diodes D1 to D4 have been bypassed with large capacitors, which in effect means that the circuit is both dc-coupled through the zener diodes, and ac-coupled through the capacitors. The capacitors will present a low impedance to switching transients which will increase the transient base drive and decrease the transistor switching times, and the zener diodes provide for dc-coupling, which permits pulses of long duration to be amplified. Since the inputs of the Class D stages will have relatively low input impedances [Came66], complementary emitter-follower stages have been added as voltage buffers. This reduces the output current required from the first Class D stage, which improves the switching speed. Also, the first Class D stage operates from lower power supply voltages than the second stage, to reduce the transistor power dissipation and switching time, since the full output voltage swing is not required to drive the second stage. Lastly, since a sine wave output is not desired, no tuned filter is present on the output.

Figure B.1. Schematic diagram of the pulse amplifier. The first Class D stage shapes a fast pulse to trigger the second Class D stage. Both stages are buffered by complementary emitter-followers to ease the drive requirements.

The power supply voltages for the circuit of Figure B.1 are $\pm 20V$. The Zener diodes D5 to D8 drop these voltages to $\pm 8.1V$ to power the first stage of the circuit. The breakdown voltage of the Zener diode D1 is 6.2V, and 10 V for D2. When the input voltage is zero, the voltage at the emitters of Q1 and Q2 (point C in Figure B.1) will be approximately 0.7V, and there will be a negligible voltage drop across the base-emitter junction of Q4, so the diode D2 is reversed biased with approximately 8.8 V across it, which is less than its breakdown voltage. Thus almost no current flows in the diode, and transistor Q4 is in the cutoff state. However, D1 is in breakdown, since the base voltage of Q3 is approximately $+8.1V - 0.7V$, and the voltage at point C is 0.7 V, yielding 6.7 V across D1 and R1, causing D1 to conduct. Thus Q3 is saturated, and the output voltage is $+8.1V + V_{CEsat1} \approx 8 V$.

When the input rises to the high level (+3.5V), D1 no longer has enough potential across it to sustain breakdown, and becomes non-conducting, forcing Q3 off. D2 is driven into breakdown, and conducts, turning Q4 on and driving it into saturation. The collector

voltage falls to $-8.1\text{ V} + V_{CEsat2} \approx -8\text{ V}$. This yields a fast $\pm 8\text{ V}$, inverted pulse at point D, which drives the second buffer and inverting Class D stages in a similar manner.

Figure B.2 shows a typical output pulse for the circuit of Figure B.1. It shows a $\pm 20\text{ V}$ pulse into a $50\ \Omega$ load, with rise and fall times of less than 3 ns . This is considerably better than what can be obtained with the fastest available op amps. By changing the Zener diodes D1 to D4, the output voltages can be easily changed to values other than $+20\text{ V}$ and -20 V . In practice, it is found that the pulse repetition frequency should be kept below 1 MHz to ensure that the switching losses in the transistors do not become excessive and damage the transistors [Clar7!].

Figure B.2. Typical output waveform for the circuit of Figure B.1. Scale: 10 V/div , 10 ns/div .

B.3 - Application to Reverse Transient Measurements

Figure B.3 shows the circuit used for diode reverse recovery measurements presented here. An output waveform for the common 1N4148 fast switching diode is shown in Figure B.4. At $t < 30\text{ ns}$, the diode is forward biased. At $t = 30\text{ ns}$, the voltage across the diode-resistor network is switched. For another 5 ns the diode appears as a low

resistance due to the stored charge in the diode, and a large reverse current flows. After $t = 35$ ns, most of the stored charge has been removed, and the diode begins to accumulate a reverse voltage, and the diode current eventually falls to almost zero. This diode was chosen to illustrate the need for a high speed voltage pulse. Since the reverse transient is only several nanoseconds long, a fast pulse edge is required.

Figure B.3. Test circuit for reverse recovery transient measurements. The diode conducts a reverse current for a short time.

Figure B.4. Reverse recovery transient for a 1N4148 diode. The 1N4148 is a fast switching diode, as demonstrated by its very short reverse recovery transient. Scale: 10 V/div, 10 ns/div.

Figure B.5. Reverse recovery transient for a TRW DSR3400X fast-recovery rectifier. Note the undesirable "snappy" response. Scale: 10 V/div, 10 ns/div.

Figure B.6. Reverse recovery transient for a Central Semiconductor 1N4936 fast-recovery rectifier. Note the classic textbook form of the reverse recovery transient. Scale: 10 V/div, 20 ns/div.

Figures 5 and 6 show reverse recovery transients for two other diodes, both 400 V fast-recovery power rectifiers. The diode used for Figure B.5 is a TRW DSR3400X. The diode current shows a very "snappy" response, that is, the ratio of the constant reverse

current time to the decaying reverse current time is very high. For most applications, a snappy transient is highly undesirable, since it can create large inductive voltage spikes. In contrast, the waveform for the Central Semiconductor 1N4936 shown in Figure B.6 shows the classic textbook reverse recovery transient, with a constant current period followed by a very smooth fall in current.

The nature of the reverse transient can be linked to the diode's doping profile. For instance, the snappy nature of the DSR3400X transient suggests that it is either has a diffused structure, or an epitaxial $p^+p^-n^+$ structure [Bend67]. The smoother recovery of the 1N4936 suggest that it has an epitaxial $p^+n^-n^+$ structure [Bend67] or an epitaxial $p^+n^--n^-n^+$ structure [Woll81], [Bali87]. Figure B.7 shows the approximate doping profile for the TRW DSR3400X, and Figure B.8 shows the approximate doping profile for the 1N4936, with the junctions at $x = 0$. The profiles were obtained from high voltage $C-V$ measurements [Chud95a], assuming that the junctions were one-sided (i.e. $|N(x)| \rightarrow \infty$ for $x < 0$). Figure B.7 clearly shows that the DSR3400X is indeed a diffused structure, as the doping gradually varies from a very low level to a very high level. The 1N4936 clearly shows a $p^+n^--n^-n^+$ structure. That is, two lightly doped regions exist: the one closest to the junction is nearly intrinsic silicon with doping of less than 10^{12} cm^{-3} (n^--) followed by a second layer of higher, but still quite light doping of around 10^{14} cm^{-3} (n^-). This structure is specifically designed to provide a smooth transient [Woll81], [Bali87].

Figure B.7. Doping profile of the TRW DSR3400X fast-recovery rectifier. The doping profile is clearly diffused, as suggested by the snappy reverse recovery transient.

Figure B.8. Doping profile of the Central Semiconductor 1N4936 fast-recovery rectifier. The doping profile shows an active region consisting of an nearly intrinsic layer followed by a lightly doped layer. This modern design produces the smooth transient shown in Figure B.6, rather than an abrupt transient like that shown in Figure B.7.

Figure B.9 shows the reverse transient for the M/A-Com MA44952 step recovery diode listed in Table 1.1. By noting that $I_F = 320$ mA, $I_R = 480$ mA, $t_s = 100$ ns, and using equation (3.4), the effective lifetime can be calculated as $\tau_{EFF} = 195$ ns, as indicated in Table 1.1.

Figure B.9. Reverse transient for the M/A-Com MA44952 step recovery diode. This data allows the effective lifetime to be calculated.

Appendix C - The Relationship Between V_{BR} and E_C

C.1 - Introduction

The results of Chapter 4 rely on the empirical observation that there is an approximate one-to-one relationship between the breakdown voltage, V_{BR} , and the peak electric field at breakdown, E_C . This appendix briefly considers this relationship from a theoretical viewpoint. It is shown that this one-to-one relationship can be predicted mathematically for the case of the two-sided abrupt junction, with uniform doping levels N_A and N_D . It is also shown that the mathematics rapidly become intractable for cases more complex than this, such as the diffused rectifier discussed in Chapter 4.

C.2 - Theory

The avalanche breakdown process is most accurately described by ionization equations of the form [Van70]:

$$\begin{aligned}\alpha_n &= a_n \exp\left(\frac{-b_n}{|E|}\right) \\ \alpha_p &= a_p \exp\left(\frac{-b_p}{|E|}\right)\end{aligned}\tag{C.1}$$

where α_n and α_p are the numbers of electron-hole pairs produced by ionization per unit length (in the direction of the electric field) per electron and hole, respectively. For silicon, the relevant ionization coefficients are [Van70]:

$$\begin{aligned}
 a_n &= 7.03 \times 10^5 \text{ cm}^{-1} \\
 b_n &= 1.231 \times 10^6 \text{ Vcm}^{-1} \\
 a_p &= 1.582 \times 10^6 \text{ cm}^{-1} \\
 b_p &= 2.036 \times 10^6 \text{ Vcm}^{-1}
 \end{aligned}
 \tag{C.2}$$

The total number of electron hole pairs generated in the depletion region (of width W) of a p-n junction by a single pair initially generated at x is then given by [Ghan77]:

$$M(x) = 1 + \int_0^x \alpha_n M(x') dx' + \int_x^W \alpha_p M(x') dx'
 \tag{C.3}$$

Breakdown occurs when $M(x)$ becomes infinite.

Using equations (C.1) in (C.3) for the case of $M(x) \rightarrow \infty$ does not produce simple mathematical results. However, a simpler "effective" ionization rate equation is also available, which combines the effects of hole and electron ionization [Van70]:

$$\alpha_{\text{eff}} = a \exp\left(-\frac{b}{|E|}\right)
 \tag{C.4}$$

where

$$\begin{aligned}
 a &= 7.03 \times 10^5 \text{ cm}^{-1} \\
 b &= 1.468 \times 10^6 \text{ Vcm}^{-1}
 \end{aligned}
 \tag{C.5}$$

These values are valid in the range $1.75 \times 10^5 \text{ V/cm} < |E| < 6.40 \times 10^5 \text{ V/cm}$.

With this simplified ionization equation, a simple condition for $M(x) \rightarrow \infty$ can be obtained [Koko66]:

$$\int_0^W \alpha_{\text{eff}}(E) dx = 1 \quad (\text{C.6})$$

For the purposes of examining the relationship between V_{BR} and E_c , consider a diode junction of arbitrary profile, with the proviso that:

$$\begin{aligned} N(x) &< 0 \text{ for } x < 0 \\ N(x) &> 0 \text{ for } x > 0 \end{aligned} \quad (\text{C.7})$$

In this case, $E > 0$ in the depletion region, so our equations can be simplified slightly by removing the absolute value operators from equation (C.4). Also, the depletion region will be defined as:

$$-x_1 < x < +x_2 \quad (\text{C.8})$$

with the junction at $x = 0$.

Then equation (C.6) can be rewritten, taking into consideration (C.4), (C.7) and (C.8), as:

$$\int_{-x_1}^0 a \exp\left(\frac{-b}{E}\right) dx + \int_0^{x_2} a \exp\left(\frac{-b}{E}\right) dx = 1 \quad (\text{C.9})$$

Consideration of Poisson's equation for this structure:

$$\frac{dE}{dx} = -\frac{q}{\epsilon} N(x) \quad (\text{C.10})$$

linked with the conditions in (C.7) and (C.8) shows that the electric field is monotonic with distance in the range $-x_1 < x < 0$, and is also monotonic (in the opposite direction) in

the separate range $0 < x < x_2$. This allows us to establish a one-to-one relationship between $E(x)$ and x in each of these ranges (separately), and thus rearranging (C.10) to find an expression for dx in terms of dE allows (C.9) to be rewritten in the form:

$$-\int_0^{E_c} \frac{a}{\frac{q}{\epsilon} N(x)} \exp\left(\frac{-b}{E}\right) dE - \int_{E_c}^0 \frac{a}{\frac{q}{\epsilon} N(x)} \exp\left(\frac{-b}{E}\right) dE = 1 \quad (\text{C.11})$$

where the variable of integration has been changed. The fact that $E = E_c$ at $x = 0$, and that $E = 0$ at $x = x_1$ and $x = x_2$ has also been used in deriving (C.11). Since, as noted above, $E(x)$ and x are related uniquely in each region, $N(x)$ can be written as $N(E)$, eliminating the distance coordinate entirely from (C.11). this yields, with some rearranging:

$$-\int_0^{E_c} \frac{1}{N_1(E)} \exp\left(\frac{-b}{E}\right) dE + \int_0^{E_c} \frac{1}{N_2(E)} \exp\left(\frac{-b}{E}\right) dE = \frac{q}{a \epsilon} \quad (\text{C.12})$$

where $N_1(E)$ is the doping as a function of electric field in the range $-x_1 < x < 0$, and where $N_2(E)$ is the doping as a function of electric field in the range $0 < x < x_2$.

In a pn junction with uniform doping on the opposite sides of the junction, $N_1(E)$ and $N_2(E)$ are constants, equal to $-N_D$ and $+N_A$, respectively. This greatly simplifies the mathematics, since (C.12) can be reduced to:

$$\left(\frac{1}{N_D} + \frac{1}{N_A} \right) \int_0^{E_c} \exp\left(\frac{-b}{E}\right) dE = \frac{q}{a \epsilon} \quad (\text{C.13})$$

It is now simple to show that E_c and V_{BK} are related by noting that for an abrupt junction as described above, the voltage applied across the junction can be written from simple diode theory as:

$$V_{BR} \approx \frac{\epsilon E_C^2}{2q} \left(\frac{1}{N_D} + \frac{1}{N_A} \right) \quad (C.14)$$

(The approximation comes from the fact that the diode built-in voltage has been ignored, since it is typically orders of magnitude smaller than the breakdown voltages considered in this thesis.) Thus, combining (C.13) and (C.14) yields:

$$\frac{2 V_{BR}}{E_C^2} \int_0^{E_C} \exp\left(\frac{-b}{E}\right) dE = \frac{1}{a} \quad (C.15)$$

Evaluating the integral and using the tabulated "exponential integral" function $E_1(z)$, which is given by [Abra65]:

$$E_1(z) = \int_z^{\infty} \frac{e^{-t}}{t} dt \quad (C.16)$$

allows (C.15) to be rewritten as:

$$V_{BR} = \frac{E_C}{2a} \frac{1}{\exp\left(-\frac{b}{E_C}\right) - \frac{b}{E_C} E_1\left(\frac{b}{E_C}\right)} \quad (C.17)$$

This expression shows that V_{BR} is directly related to E_C , regardless of the choice of N_A or N_D . Furthermore, it is simple to show that V_{BR} decreases monotonically with increasing E_C , so V_{BR} and E_C have a one-to-one relationship.

(The expression in (C.17) is similar to one in [Koko66] which was derived for the case of a one-sided junction. However, since there is only one geometrical parameter to

vary in a one-sided junction, the light-side doping N , both V_{BR} and E_C can be written as a function of N . Thus N can be eliminated from these two expressions and V_{BR} can be written in terms of E_C . To show convincingly that the relationship between E_C and V_{BR} is independent of doping parameters, more than one doping parameter must be variable, as is the case for the two-sided junction considered above.)

The fact that V_{BR} decreases with increasing E_C is worth some reflection, because at first glance it appears to be counter-intuitive, since (C.14) predicts that $V_{BR} \propto E_C^2$. This can be explained by examining the nature of equation (C.4). The ionization rate $\propto_{FF}$ increases very rapidly with increasing electric field due to the exponential nature of (C.4). Thus, the depletion region width, W_{DR} , required to satisfy (C.6) falls very rapidly with increasing E_C . Since

$$V_{BR} = \frac{1}{2} E_C W_{DR} \quad (C.18)$$

an increase in E_C will be more than offset by the corresponding decrease in W_{DR} . Comparing (C.17) and (C.18) shows that W can be written as a function of E_C :

$$W_{DR} = \frac{1}{a} \frac{1}{\exp\left(-\frac{b}{E_C}\right) - \frac{b}{E_C} E_1\left(\frac{b}{E_C}\right)} \quad (C.19)$$

A plot of W_{DR} versus E_C is for the critical electric field range of interest in this thesis is shown in Figure C.1. It is also compared to a simple $1/E_C$ function, showing that W_{DR} decreases proportionately faster than E_C increases.

Figure C.1 - Depletion region width as a function of E_C . The $4000/E_C$ curve shows that W_{DR} decreases proportionately faster than E_C increases. E_C is in V/cm, W is in cm.

In the asymptotic limit of $E_C \rightarrow \infty$, $W_{DR} \rightarrow 1/a$. However, this is of limited interest, since the electric fields required to approach this limit are much higher than any field that can be practically generated in a simple pn junction.

A quick survey of the mathematics in this chapter shows that obtaining similar analytical results for a diffused structure, or a generalized structure, is not possible. The mathematics rapidly become intractable. Furthermore, we know from the simulations of Chapter 4 that there is only an approximate one-to-one relationship between E_C and V_{BR} for the diffused devices, which is more difficult to prove mathematically than the exact one-to-one relationship that exists for the abrupt structures discussed above. However, it is not too great a leap of logic to say that the one-to-one relationship that has been demonstrated theoretically for the abrupt junctions is likely to hold (approximately) for diffused junctions as well, since one can look at the abrupt junction as a limiting case of a diffused structure.

Appendix D - The Relationship Between t_r and τ

D.1 - Introduction

As mentioned in Chapter 5, the expression for calculating the intrinsic switching time given in equation (5.4.3.4) is a fairly simple estimate of t_r . The results presented in Chapter 7 show that this equation is quite reasonable as an engineering estimate. However, it would be more useful if it established the relationship between t_r and the carrier lifetime τ . Regrettably, this relationship is far too complex to be dealt with analytically. This appendix presents the results of several computer simulations, and shows that the switching time varies weakly with carrier lifetime.

Intuitively, one would expect that the switching time would decrease with lower carrier lifetimes, since this would concentrate charge at the edges of the middle region, which is the goal of most conventional SRD designs.

D.2 - Computer Simulations

Several simulations were run for the structure described in Section 5.6 in the series-connected circuit configuration described in Section 7.3, with different values for τ . Since $\tau \approx \tau_n + \tau_p$ at high injection levels (see equation (2.3)), the actual simulation parameters τ_n and τ_p were each set at $\tau/2$. The forward bias was adjusted in each case such that the storage time t_s was approximately 5 ns in all cases. In other words, each device had a similar amount of stored charge. The results of the simulations are summarized in Figure D.1.

Figure D.1 - Variation of simulated switching time with lifetime, for equal stored charge, with the structure described in Section 5.6 and the circuit described in Section 7.3.

Evidently a 50:1 change in lifetime only induces a 1.8:1 change in switching time. As an experimental check on this relationship, one can compare the results obtained with the two WFSRDs in section 7.3. Diode A8.PT.850.1 had an effective lifetime about five times lower than that of diode A8.6. This 5:1 lifetime difference corresponded to a 1.13:1 difference in switching times, which agrees well with the simulated results. (The other commercial diodes had higher switching times despite their lower carrier lifetimes; evidently these commercial structures were further from the optimum structure than diode 89.)

Based on these results, equation (5.4.3.4) can be applied with the expectation that the result will be accurate within a factor 2.

Appendix E - Thermal Considerations

E.1 - Introduction

Thermal effects have been ignored in the preceding chapters. The next section justifies this approach, by showing that the temperature differential between the ends of the diode and its interior regions is always low, so that if good heat-sinking is used the entire device will remain cool. It is also shown that thermal effects occur on a much longer time scale than the electrical switching effects.

E.2 - Theory

The thermal resistance of a structure of length L and cross-sectional A can be calculated in a manner analogous to electrical resistance, that is:

$$R_{th} = \frac{1}{\kappa} \frac{L}{A} \quad (E.1)$$

where κ is the thermal conductivity. The thermal capacity can be calculated by multiplying the specific heat capacity, C_p , by the mass of the structure:

$$C_{th} = C_p \rho L A \quad (E.2)$$

where ρ is the density. The $R_{th}C_{th}$ product represents the thermal time constant, and from (E.1) and (E.2) is given by:

$$\tau_{th} = \frac{C_p \rho L^2}{\kappa} \quad (E.3)$$

Taking the fabricated WFSRD as an example (with $L = 150 \mu\text{m}$), and the appropriate physical constants for silicon ($C_p = 0.7 \text{ J/gK}$, $\rho = 2.328 \text{ g/cm}^3$, $\kappa = 1.5 \text{ W/cmK}$ [Sze81]) yields $\tau_{th} = 245 \mu\text{s}$. Since this is 5 orders of magnitude higher than the electrical switching time, one can conclude that the temperature of the WFSRD does not vary appreciably during the switching transient. Similar results hold for the DSRD.

The effect of a heat flux ϕ on a one-dimensional slab in thermal equilibrium can be expressed as [Edwa89]:

$$\phi = -\kappa \frac{dT}{dx} \quad (\text{E.3})$$

where T is temperature. Consider again the WFSRD, and assume that the power dissipated by the diode is concentrated in the center of the structure ($x = L/2$) and that the temperature at the two ends of the diode ($x = 0$ and $x = L$) is fixed by good heating-sinking. Then the heat flux at any point (except at $L/2$) is given by

$$\phi = \frac{P_{avg}}{2A} \quad (\text{E.4})$$

since half of the average dissipated power is absorbed by each end. Then, from (E.3), the temperature difference between the center (which is the hottest point) and either end (the coolest points) will be given by:

$$\Delta T = \frac{L P_{avg}}{4 \kappa A} \quad (\text{E.5})$$

If one assumes that the WFSRD is operate at low duty cycles, such that the bulk of the power dissipation occurs during the forward biasing, then $P_{avg} \approx I_f V_f$. If we take $I_f \approx 200 \text{ mA}$ and $V_f \approx 1 \text{ V}$ as typical worst-case values for a WFSRD with ideal ohmic

contacts, and use the fabricated values of $L = 150 \mu\text{m}$ and $A = 1.35 \text{ mm}^2$ in (E.5), one obtains $\Delta T \approx 0.04 \text{ K}$.

Power dissipation will be higher if the device is not operated at low duty cycles, since the current can be very large during the storage time. If we assume as a worst case that the reverse conduction storage time t_s represents 10% of the period, then $P_{\text{avg}} \approx 0.1 I_R V_F$. For $I_R \approx 6 \text{ A}$ and $V_F \approx 1 \text{ V}$, then $\Delta T \approx 0.1 \text{ K}$.

The devices reported in Chapter 7 did not have perfect ohmic contacts, with the results the forward voltage drop was on the order of 6 V, rather than 1 V. However even so, $\Delta T < 1 \text{ K}$. Thus for a device with effective heat-sinking, such that the temperature at the device ends is near room temperature, thermal effects should be negligible.

Similar results hold for the DSRD.

3

OF/DE

3

PM-1 3 1/2" x 4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

PRECISIONSM RESOLUTION TARGETS

Appendix F - Sample Medici File

As mentioned previously, the Medici simulations used in this thesis were almost all defined as one-dimensional structures with 300 equally-spaced nodes. The integrity of this approach was confirmed by running several simulations with different gridding for each structure, to ensure that the 300-node gridding was sufficiently fine that a small change in grid spacing would not affect the simulation results.

The following Medici batch-file was used to generate the simulation results for DF5. Since the circuit conditions ensured that the diode operated at voltages well below breakdown, the "IMPACT.I" impact ionization parameter was not included in the "MODELS" statement. This parameter was of course included for the breakdown simulations reported in Chapter 4. (As mentioned in Chapter 4, the default ionization parameters were used, which are based on the generally-accepted Van Overstraeten and De Man data [Van70] for ionization rates in silicon.)

```

TITLE      June 16, 1996 - data for "DF5" figures in Chapter 5 of thesis

COMMENT    set up mesh
MESH       RECTANGU OUT.FILE=df5mesh
X.MESH     WIDTH=1000000 N.SPACES=1
Y.MESH     DEPTH=212 N.SPACES=300

COMMENT    define region
REGION     NUM=1 SILICON

COMMENT    define electrodes
ELECTRODE  NUM=1 TOP
ELECTRODE  NUM=2 BOT

```

```

COMMENT    define impurity profile
PROFILE    p-TYPE N.PEAK=1.2E14 UNIFORM
PROFILE    p-TYPE N.PEAK=1E19 Y.MIN=0 Y.MAX=0 Y.CHAR=29.7
PROFILE    N-TYPE N.PEAK=1E19 Y.MIN=212 Y.MAX=212 Y.CHAR=29.7

COMMENT    show doping
PLOT.1D    DOPING Y.LOG COLOR=2 LINE=1 BOT=1E10 TOP=1E20
+          X.STA=0 X.END=0 Y.STA=0 Y.END=150
+          TITLE="df5 - DOPING PROFILE"
+          DEVICE=POSTSCRIPT PLOT.OUT=df5dop.ps

COMMENT    Attach a lumped resistance to the p+ contact
CONTACT    NUM=1 RESIST=50

COMMENT    Specify physical models to use
MODELS     CONSRH AUGER CONMOB FLDMOB
MATERIAL    SILICON TAUN0=55E-9 TAUP0=55E-9

COMMENT    Symbolic factorization
SYMB       NEWTON CARRIERS=2
method     stacks=10

COMMENT    Perform a + volt steady state solution, then simulate
COMMENT    the transient turn-off characteristics for the diode.
SOLVE      V1=0 OUT.FILE=df5.s00
SOLVE      V1=12 OUT.FILE=df5.s01
SOLVE      V1=-300 TSTEP=0.1E-9 TSTOP=8E-9 dt.max=0.025 OUT.FILE=df5.s02

COMMENT    Plot the diode current
PLOT.1D    X.AXIS=TIME Y.AXIS=I1 POINTS TOP=1 BOT=-7 RIGHT=8E-9
+          TITLE="df5 Current vs. Time" COLOR=2
+          DEVICE=POSTSCRIPT PLOT.OUT=df5cur.ps out.file=df5cur.dat

```

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