Distributed Amplifiers Employing Constant-k and m-Derived Sections

by

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in

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“Distributed Amplifiers Employing
Constant-k and m-Derived Sections”

submitted by Jorge Aguirre, B. Eng., in partial fulfilment of the requirements for the degree of Master of Engineering in Electrical Engineering

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Abstract

Distributed amplifiers achieve larger bandwidths than lumped element amplifiers by incorporating the input and output capacitances of the individual gain cells into artificial transmission lines. These artificial transmission lines are composed of filter sections. In this thesis, the m-derived T filter section is shown to be a useful alternative to the constant-k T filter section in the design of distributed amplifiers.

Two single-ended, three-stage, SiGe, HBT distributed amplifiers employing m-derived filter sections in the output artificial transmission lines have been designed, fabricated and measured. The small die size ($1.0 \times 1.1 \text{ mm}^2$) and fabrication in SiGe translates into low cost. The distributed amplifiers have a low power consumption of 125 mW and a measured passband of 100 MHz to 50 GHz. The measured results demonstrate that distributed amplifiers in SiGe can be competitive with those in III - V processes.

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Table of Contents

Abstract	iii
Acknowledgments	iv
Table of Contents	v
List of Tables	vii
List of Figures	viii
List of Symbols	xvi
Chapter 1: Introduction	1
1.1 Thesis Goals	1
1.2 Thesis Outline	2
Chapter 2: Filter Sections	3
2.1 The Constant-k T Networks	3
2.2 The m-Derived T Section	6
2.3 The Bisected- π m-Derived Filter Section	10
2.4 Summary	11
Chapter 3: Bandwidth	12
3.1 Gain-Bandwidth Product	12
3.2 Bandwidth	13
3.3 Summary	16
Chapter 4: Distributed Amplifier Circuit Theory	17
4.1 ABCD parameters	17
4.2 Image parameters	18
4.3 Distributed Amplifier Analysis	21
4.3.1 Transistor model	22
4.3.2 Artificial Transmission Lines	23
4.3.3 Gain	24

4.3.4	Number of Stages	28
4.3.5	Maximum Bandwidth	29
4.4	Recent Work in Distributed Amplification	29
4.5	Summary	32
Chapter 5: Distributed Amplifier Design		33
5.1	Design Goals	33
5.2	Topology of The Single Cell	34
5.3	The Artificial Transmission line	39
5.4	The single-ended distributed amplifiers	46
5.5	The differential distributed amplifiers	54
5.6	Summary	56
Chapter 6: Experimental Results		57
6.1	Inductor measurements	57
6.2	Distributed Amplifier Testing	62
6.2.1	Measurement Setup	63
6.2.2	Off-Chip Terminations and Reflections	63
6.2.3	Measured S-parameters	70
6.2.4	1 dB Compression point	78
6.2.5	Stability	80
6.2.6	Process Variations	82
6.2.7	Variations in DC conditions	88
6.3	Summary	93
Chapter 7: Conclusions		95
7.1	Summary of Thesis Contributions	96
7.2	Future and Current Work	97
References		99
Appendix A		103
Appendix B		127

List of Tables

Table 4.1.	Summary of some recently published distributed amplifier designs	30
Table 5.1.	Specifications for a Distributed Amplifier Pre-Driver	33
Table 5.2.	The Specifications for the Large-u and Small-u distributed amplifiers . .	52
Table 5.3.	Summary of the simulated results for the Large-u and Small-u distributed amplifiers.	53
Table 5.4.	Summary of the simulated results for the InP and SiGe differential distributed amplifiers.	55
Table 6.1.	The average variation from the mean S-parameters for the Singlewire and Indline distributed amplifiers.	82
Table 6.2.	Input Bias voltage and the corresponding output current	93
Table 7.1.	The measured performance of the Singlewire and Indline distributed amplifiers.	95

List of Figures

Figure 2.1.	(a) The constant-k T filter section and (b) the m-derived T filter section. .	4
Figure 2.2.	The attenuation and phase constants versus frequency for the constant-k T filter section.	5
Figure 2.3.	The Image impedance of the constant-k T filter section.	6
Figure 2.4.	The (a) attenuation and (b) phase constants of the m-derived T filter section propagation factor for various values of m.	8
Figure 2.5.	(a) $ S_{21} $ and (b) $ S_{11} $ for the m-derived T section with resistive terminations for various values of m.	9
Figure 2.6.	Bisected- π m-derived termination	10
Figure 2.7.	The real portion of the output image impedance of the bisected- π m-derived filter section	11
Figure 3.1.	A simple amplifier utilizing a two terminal coupling network.	12
Figure 3.2.	A constant-k filter section	13
Figure 3.3.	Parallel connected constant-k filter sections	14
Figure 3.4.	Resistively terminated, constant-k T filter ladder network.	14
Figure 3.5.	(a) One and two stage constant-k ladder networks and (b) the corresponding $ S_{11} $ and $ S_{21} $. Where $\omega_C = 2/(\sqrt{LC})$, $C = 127$ fF and $L = 318$ pH.	15
Figure 4.1.	A Y parameterized Generic network	18
Figure 4.2.	A simplified distributed amplifier (biasing is not shown).	21
Figure 4.3.	The model for the heterojunction bipolar transistor.	22
Figure 4.4.	A simplified model for the heterojunction bipolar transistor.	22
Figure 4.5.	A further simplified model for the heterojunction bipolar transistor. ...	23
Figure 4.6.	The input artificial transmission line of a distributed amplifier	23
Figure 4.7.	The output artificial transmission line of the distributed amplifier.	24
Figure 4.8.	A generic L section created by removing from the simple section.	24
Figure 4.9.	Input line L section	25
Figure 5.1.	Cascode gain stage used in the distributed amplifiers.	34

Figure 5.2.	A simple model for two cascode connected transistors in the common emitter configuration.	35
Figure 5.3.	The output artificial transmission line transition from the common emitter device to the cascode common emitter gain stage.	36
Figure 5.4.	The gain stage used in the Singlewire and Indline distributed amplifiers	38
Figure 5.5.	The gain stage used in the Large-u and Small-u distributed amplifiers ..	39
Figure 5.6.	A comparison between the constant-k T section and the m-derived T section ($m = 0.1$).	41
Figure 5.7.	A comparison between the m-derived T section ($m = 0.1$) and a constant-k T section with bisected- π sections before the terminations ($m = 0.6$).	42
Figure 5.8.	A comparison between the m-derived T section ($m = 0.1$) and a m-derived T section ($m = 0.1$) with bisected- π sections ($m = 0.6$) before the terminations.	43
Figure 5.9.	The inductor layout for the: (a) Singlewire amplifier m-derived T section and (b) Singlewire amplifier constant-k T section, (c) Indline amplifier m-derived T section and (d) Indline amplifier constant-k T section.	44
Figure 5.10.	Layout of the Large-u and Small-u distributed amplifier inductors.	45
Figure 5.11.	Inductor model	46
Figure 5.12.	Topology for the Singlewire and Indline distributed amplifiers.	47
Figure 5.13.	The topology for the Large-u and Small-u distributed amplifiers	47
Figure 5.14.	Simulated S-parameters of the Singlewire distributed amplifier using IBM models for the inductors.	48
Figure 5.15.	Simulated S-parameters of the Singlewire distributed amplifier using Momentum models for the inductors.	49
Figure 5.16.	Simulated S-parameters of the Indline distributed amplifier.	49
Figure 5.17.	Calculated Group Delay from the simulated S-parameters of the Singlewire distributed amplifier	50
Figure 5.18.	Calculated Group Delay from the simulated S-parameters of the	

Inline distributed amplifier	50
Figure 5.19. The layout of the Singlewire distributed amplifier	51
Figure 5.20. The layout of the Indline distributed amplifier	52
Figure 5.21. The layout of the (a) Large-u and (b) Small-u distributed amplifiers ...	54
Figure 5.22. Cascode differential pair gain stage	56
Figure 6.1. Cross section of the BiCMOS 7HP technology	57
Figure 6.2. Simulation and test set up for the inductor line measurements.	58
Figure 6.3. Measured and simulated input collector line (a) Singlewire $ S_{11} $ and $ S_{12} $ (b) Indline $ S_{11} $ and $ S_{12} $	59
Figure 6.4. Measured and simulated input collector shunt arm inductor (a) Singlewire $ S_{11} $ and $ S_{12} $ (b) Indline $ S_{11} $ and $ S_{12} $	60
Figure 6.5. Measured and simulated base output line (a) Singlewire $ S_{11} $ and $ S_{12} $ (b) Indline $ S_{11} $ and $ S_{12} $	61
Figure 6.6. Photo of the Singlewire distributed amplifier	62
Figure 6.7. Measured and spline approximation of the (a) Singlewire amplifier $ S_{11} $ and (b) Indline amplifier $ S_{11} $	64
Figure 6.8. Measured and spline approximation of the (a) Singlewire amplifier $ S_{12} $ and (b) Indline amplifier $ S_{12} $	65
Figure 6.9. Measured and spline approximation of the (a) Singlewire amplifier $ S_{21} $ and (b) Indline amplifier $ S_{21} $	66
Figure 6.10. Measured and spline approximation of the (a) Singlewire amplifier $ S_{22} $ and (b) Indline amplifier $ S_{22} $	67
Figure 6.11. Calculated group delay using the measured data and the spline approximation to the data for the (a) Singlewire amplifier and (b) Indline amplifier.	68
Figure 6.12. A comparison of the measured $ S_{11} $ of the output artificial transmission line with a 50 Ohm dummy load termination and with the 50 Ohm termination replaced with port 2 of the network analyzer and the spline approximation of $ S_{11} $ and port 2 of the network analyzer	

as the dummy load.	69
Figure 6.13. A comparison of the measured $ S_{11} $ of the input artificial transmission line with a 50 Ohm dummy load termination and with the 50 Ohm termination replaced with port 2 of the network analyzer and the spline approximation of $ S_{11} $ and port 2 of the network analyzer as the dummy load.	70
Figure 6.14. Measured and simulated $ S_{11} $ for the (a) Singlewire and (b) Indline distributed amplifiers.	72
Figure 6.15. Measured and simulated $ S_{12} $ for the (a) Singlewire and (b) Indline distributed amplifiers.	73
Figure 6.16. Measured and simulated $ S_{21} $ for the (a) Singlewire and (b) Indline distributed amplifiers.	74
Figure 6.17. Measured and simulated $ S_{22} $ for the (a) Singlewire and (b) Indline distributed amplifiers.	75
Figure 6.18. Calculated group delay from Measured and simulated data for the (a) Singlewire amplifier and (b) Indline amplifier.	76
Figure 6.19. The input and output artificial transmission line $ S_{21} $ for the Singlewire distributed amplifier.	77
Figure 6.20. The input and output artificial transmission line $ S_{21} $ for the Indline distributed amplifier.	78
Figure 6.21. The input referred 1 dB compression point for the Singlewire and Indline distributed amplifiers with respect to frequency.	79
Figure 6.22. The output referred 1 dB compression point for the Singlewire and Indline distributed amplifiers with respect to frequency.	80
Figure 6.23. The calculated stability constant K using the IBM models and the Momentum models for the distributed amplifier	81
Figure 6.24. The calculated stability constant B using the IBM models and the Momentum models for the distributed amplifier	81
Figure 6.25. Measured (a) Singlewire amplifier $ S_{11} $ and (b) Indline amplifier $ S_{11} $	

in various locations across the wafer.	83
Figure 6.26. Measured (a) Singlewire amplifier S12 and (b) Indline amplifier S12 in various locations across the wafer.	84
Figure 6.27. Measured (a) Singlewire amplifier S21 and (b) Indline amplifier S21 in various locations across the wafer.	85
Figure 6.28. Measured (a) Singlewire amplifier S22 and (b) Indline amplifier S22 in various locations across the wafer.	86
Figure 6.29. Calculated (a) Singlewire amplifier Group Delay and (b) Indline amplifier Group Delay from measured data in various locations across the wafer	87
Figure 6.30. Measured (a) Singlewire amplifier S21 and (b) Indline amplifier S21 for various values of cascode collector supply voltage.	89
Figure 6.31. (a) Measured Singlewire amplifier S21 and (b) measured Indline amplifier S21 for various values of cascode base supply voltage.	91
Figure 6.32. (a) Measured Singlewire distributed amplifier S21 and (b) measured Indline amplifier S21 for various values of input DC bias voltage.	92
Figure A.1. Measured (a) Singlewire amplifier S11 and (b) Indline amplifier S11 for various values of cascode collector supply voltage.	103
Figure A.2. Measured (a) Singlewire amplifier S12 and (b) Indline amplifier S12 for various values of cascode collector supply voltage.	104
Figure A.3. Measured (a) Singlewire amplifier S22 and (b) Indline amplifier S22 for various values of cascode collector supply voltage.	105
Figure A.4. Calculated group delay from measured data for the (a) Singlewire and (b) Indline amplifiers for various values of cascode collector supply voltage.	106
Figure A.5. Measured (a) Singlewire amplifier S11 and (b) Indline amplifier S11 for various values of cascode base supply voltage.....	107
Figure A.6. Measured (a) Singlewire amplifier S12 and (b) Indline amplifier S12 for various values of cascode base supply voltage.....	108

Figure A.7. Measured (a) Singlewire amplifier $ S_{22} $ and (b) Indline amplifier $ S_{22} $ for various values of cascode base supply voltage.....	109
Figure A.8. Calculated group delay from measured data for the (a) Singlewire and (b) Indline amplifiers for various values of cascode base voltage.....	110
Figure A.9. Measured (a) Singlewire amplifier $ S_{11} $ and (b) Indline amplifier $ S_{11} $ for various values of input bias.	111
Figure A.10. Measured (a) Singlewire amplifier $ S_{12} $ and (b) Indline amplifier $ S_{12} $ for various values of input bias.	112
Figure A.11. Measured (a) Singlewire amplifier $ S_{22} $ and (b) Indline amplifier $ S_{22} $ for various values of input bias.	113
Figure A.12. Calculated group delay from measured data for the (a) Singlewire amplifier and (b) Indline amplifier for various values of input bias....	114
Figure A.13. The measured 1 dB compression point for the Singlewire distributed amplifier at a frequency of 1 GHz.	115
Figure A.14. The 1 dB compression point for the Singlewire distributed amplifier at a frequency of 1 GHz (a) simulated with the IBM Singlewire model (b) simulated with the Momentum Singlewire model.	116
Figure A.15. The measured 1 dB compression point for the Singlewire distributed amplifier at a frequency of 10 GHz.	117
Figure A.16. The 1 dB compression point for the Singlewire distributed amplifier at a frequency of 10 GHz (a) simulated with the IBM Singlewire model (b) simulated with the Momentum Singlewire model.	118
Figure A.17. The measured 1 dB compression point for the Singlewire distributed amplifier at a frequency of 30 GHz.	119
Figure A.18. The 1 dB compression point for the Singlewire distributed amplifier at a frequency of 30 GHz (a) simulated with the IBM Singlewire model (b) simulated with the Momentum Singlewire model.	120
Figure A.19. The measured 1 dB compression point for the Singlewire distributed amplifier at a frequency of 49 GHz.	121

Figure A.20. The 1 dB compression point for the Singlewire distributed amplifier at a frequency of 49 GHz (a) simulated with the IBM Singlewire model (b) simulated with the Momentum Singlewire model.	122
Figure A.21. The 1 dB compression point for the Indline distributed amplifier at a frequency of 1 GHz (a) measured (b) simulated with the IBM Singlewire model.	123
Figure A.22. The 1 dB compression point for the Indline distributed amplifier at a frequency of 10 GHz (a) measured (b) simulated with the IBM Singlewire model.	124
Figure A.23. The 1 dB compression point for the Indline distributed amplifier at a frequency of 30 GHz (a) measured (b) simulated with the IBM Singlewire model.	125
Figure A.24. The 1 dB compression point for the Indline distributed amplifier at a frequency of 49 GHz (a) measured (b) simulated with the IBM Singlewire model.	126
Figure B.1. Simulated $ S_{11} $ for the (a) large and Small-u amplifiers and (b) the differential amplifier.	128
Figure B.2. Simulated $ S_{12} $ for the (a) large and Small-u amplifiers and (b) the differential amplifier.	129
Figure B.3. Simulated $ S_{21} $ for the (a) large and Small-u amplifiers and (b) the differential amplifier.	130
Figure B.4. Simulated $ S_{22} $ for the (a) large and Small-u amplifiers and (b) the differential amplifier.	131
Figure B.5. Simulated group delay for the (a) large and Small-u amplifiers and (b) the differential amplifier.	132
Figure B.6. Simulated stability constant K for the (a) large and Small-u amplifiers and (b) the differential amplifier.	133
Figure B.7. Simulated stability constant B for the (a) large and Small-u amplifiers and (b) the differential amplifier.	134

Figure B.8. The simulated 1 dB compression point at 1 GHz for the (a) Large-u amplifier, (b) Small-u amplifier.....	135
Figure B.9. The simulated 1 dB compression point at 1 GHz for the differential distributed amplifier.....	136
Figure B.10. The simulated 1 dB compression point at 10 GHz for the differential distributed amplifier.....	136
Figure B.11. The simulated 1 dB compression point at 10 GHz for the (a) Large-u amplifier, (b) Small-u amplifier.....	137
Figure B.12. The simulated 1 dB compression point at 25 GHz for the (a) Large-u amplifier, (b) Small-u amplifier.....	138
Figure B.13. The simulated 1 dB compression point at 25 GHz for the differential distributed amplifier.....	139
Figure B.14. The simulated 1 dB compression point at 40 GHz for the differential distributed amplifier.....	139
Figure B.15. The simulated 1 dB compression point at 40 GHz for the (a) Large-u amplifier, (b) Small-u amplifier.....	140
Figure B.16. The (a) input and (b) output referred 1 dB compression point for the large and Small-u distributed amplifiers and the differential distributed amplifier with respect to frequency.	141
Figure B.17. The simulated eye diagrams for an input 32 Gb/s data stream, (a) the ideal input eye, (b) the filtered input eye.....	142
Figure B.18. The simulated output eye diagram for an input 32 Gb/s data stream....	143
Figure B.19. The simulated ideal input eye diagram for a 40 Gb/s data stream.....	143
Figure B.20. The simulated eye diagrams for an input 40 Gb/s data stream, (a) the filtered input eye and (b) the output eye.	144
Figure B.21. The schematic of the gain stage for the InP differential amplifier.....	145
Figure B.22. The layout of the gain stage for the InP differential amplifier.....	146
Figure B.23. The simulated Two-port S-parameters ($ S_{11} $, $ S_{12} $, $ S_{21} $, $ S_{22} $) for the eight stage InP distributed amplifier.	146

List of Symbols

A_B	Input (base) line attenuation per section
A_C	Output (collector) line attenuation per section
A_V	Voltage gain
$A_V B$	Gain-bandwidth product
C	Shunt arm capacitance
C_T	Emitter-base capacitance summed with the Miller capacitance
C_μ	Collector-base capacitance
$C_{\mu j}$	Miller capacitance (where $j = 1, 2$)
C_π	Emitter-base capacitance
f_{max}	Maximum frequency of oscillation
f_T	Unity current gain frequency
G	Power gain
g_m	Transconductance
g_{mx}	Transconductance per node (where $x = 1, 2, 3, \dots$)
I_j	Port currents (where $j = 1, 2, \dots$)
I_x	Current at each node (where $x = 1, 2, 3, \dots, N$)
I_{Z_C}	Total current at the terminations of the output (collector) line
k	Characteristic impedance of the constant-k filter sections
L	Series arm inductance
L_B	Input (base) line series arm inductance
L_C	Output (collector) line series inductance
m	Variable used to control the resonant frequency
N	Number of gain stages

N_{opt}	Optimum number of stages
R_{BB}	Intrinsic base resistance
r_e	Emitter resistor
R_E	Emitter degeneration resistor
R_O	Collector output resistance
R_μ	base-collector shunt resistance
R_π	Base input resistance
V_{in}	Base line input voltage
V_j	Port voltages (where $j = 1, 2, \dots$)
V_{out}	Collector line output voltage
V_π	small-signal base-emitter voltage
$V_{\pi X}$	small-signal base-emitter voltage for the X^{th} transistor
ω	Frequency
ω_C	Cut-off frequency
ω_R	Resonant frequency
Ψ	phase shift
Ψ_B	Input (base) line phase shift per section
Ψ_C	Output (collector) line phase shift per section
Ψ_k	phase shift per section (where $k = 1, 2, \dots, n$)
Z_B	Input (base) artificial transmission line termination
Z_{iBj}	input (base) line image impedance per section (where $j = 1, 2$)
Z_C	Output (Collector) artificial transmission line termination
Z_{ij}	Image impedance (where $j = 1, 2, \dots$)

Z_{i_kj}	Image impedance (where $j = 1, 2, \dots$ and $k = 1, 2, \dots, n$)
Z_I	Image impedance
Z_π	Constant-k π filter section image impedance
Z_O	Characteristic impedance

Chapter 1: Introduction

High-speed front ends are reporting clock and data recovery of 40 Gb/s [1]-[2]. Voltage controlled oscillators are being designed with frequencies of oscillation of 40 GHz or more [3]-[5]. Multimedia communications has fueled a rapid growth in faster transmission systems. Data rates and frequencies are increasing, exceeding 40 Gb/s and 40 GHz respectively. These new high speed systems require amplifiers that have large bandwidth and gain. Distributed amplifiers can be used to meet the gain and broadband needs of the telecommunications industry.

Distributed amplifiers have been in use for over 50 years. These amplifiers have contributed to radar systems, particle detection, oscillography, and various other applications including broadband communications systems. In the telecommunications industry distributed amplification is most often seen in modulator drivers and optoelectronic receivers. The exotic III-V technologies have allowed distributed amplifiers to exhibit extremely large bandwidths exceeding 70 GHz, and gains of 10 dB or more [6]-[10]. Most component manufacturers have obtained wide bandwidth by using expensive technologies with high f_T . High speed circuits are now being designed in SiGe with bit rates at or above 40 Gb/s, obtaining results previously only seen in the exotic III-V technologies [11]-[14]. The IBM BiCMOS SiGe process employed in the fabrication and design of the distributed amplifiers presented in this thesis reports an f_T of 120 GHz and an $f_{\max}$ of 100 GHz [15], [16].

1.1 Thesis Goals

Distributed amplification is the use of filter sections to connect gain stages in parallel. The filter sections create artificial transmission lines that incorporate the input and output capacitance of each gain stage. These transmission lines enable a distributed amplifier to obtain a wider bandwidth and more gain than is possible for a single stage

amplifier. The input artificial transmission line allows each gain stage to take the input signal and amplify it. Each gain stage then uses the signal summing capabilities of the artificial transmission lines to create the desired output signal.

The artificial transmission lines are typically composed of constant- k T filter sections. The performance of the filter section determines the performance of the artificial transmission line and thus greatly affects the performance of the distributed amplifier. Because the performance of the distributed amplifier is dependent on the artificial transmission line, other filter sections are commonly added to the transmission line to improve its performance.

The research presented here has three main thrusts:

- 1) To use m -derived T filter sections in place of constant- k T and bisected- π m -derived filter sections in the artificial transmission lines.
- 2) To explore the capabilities of the SiGe process and to determine if it is a viable alternative to the more exotic III-V technologies.
- 3) To develop good design methodologies for designing high performance distributed amplifiers.

1.2 Thesis Outline

Chapter 2 contains basic information on the properties of some two-port networks. Issues concerning bandwidth and the gain-bandwidth product are presented in Chapter 3. Chapter 4 contains basic distributed amplifier theory. In Chapter 5 the distributed amplifier designs are presented. The experimental results are discussed in Chapter 6. Chapter 7 will summarize the thesis and presents some current and future work.

Chapter 2: Filter Sections

In this chapter a brief introduction of the two-port networks most frequently used in the design of the artificial transmission lines employed by distributed amplifiers is given.

A key component of distributed amplification is the artificial transmission line. If the definition of transmission lines is restricted to those lines that are used to transmit data, then transmission lines are a means of transporting data over large distances with a minimum of loss. The most frequently used transmission lines are twisted pair, coaxial line, parallel plate, microstrip, waveguide and optical fiber [17], [18]. Transmission lines are frequently modeled as distributed circuits with resistive, capacitive and inductive elements. An artificial transmission line uses these same lumped elements to mimic the performance of an actual transmission line. These lines can be simplified by assuming that both the conductor and the dielectric are lossless. Therefore a lossless artificial transmission line consists of capacitive and inductive elements.

2.1 The Constant-k T Networks

The two-port networks of Figure 2.1 are frequently used as simple models for the lossless artificial transmission lines of distributed amplifiers [19]-[21]. These two-port networks pass low-frequency signals while attenuating the high-frequency signals and can therefore be defined as low-pass filter sections. The frequency response of these networks is divided into two regions, the passband where $\omega < \omega_C$ and the stopband where $\omega > \omega_C$.

The cutoff frequency ω_C is defined as:

$$\omega_C = \frac{2}{\sqrt{LC}} \quad (2.1)$$

Figure 2.1. (a) The constant-k T filter section and (b) the m-derived T filter section

The frequency response of the attenuation (real) and phase (imaginary) components of the propagation factor for the constant-k section are shown in Figure 2.2. The propagation factor is defined as:

$$\psi = \psi_r + j\psi_i \quad (2.2)$$

where ψ for the constant-k filter section is:

$$\psi = \ln \left(1 - \frac{2\omega^2}{\omega_c^2} + \frac{2\omega^2}{\omega_c^2} \sqrt{\frac{\omega^2}{\omega_c^2} - 1} \right) \quad (2.3)$$

Figure 2.2. The attenuation and phase constants versus frequency for the constant-k T filter section.

The input and output impedance of the two port networks are the image impedances. Therefore, both ports are matched when terminated with their image impedance. The image impedance for Figure 2.1a is given by [21]:

$$Z_I = \sqrt{\frac{L}{C}} \sqrt{1 - \frac{\omega^2 LC}{4}} = Z_O \sqrt{1 - \frac{\omega^2}{\omega_c^2}} \quad (2.4)$$

where the nominal characteristic impedance Z_O is:

$$Z_O = \sqrt{\frac{L}{C}} = k \quad (2.5)$$

The image impedance shown in (2.4) is not constant and is dependant on frequency. For low frequencies the image impedance is real (the passband), while for high frequencies (the stopband) the image impedance is imaginary. This dependency on frequency is a limitation of the constant-k T section, since the image impedance will not match any given source or load [21].

Figure 2.3. The Image impedance of the constant-k T filter section

2.2 The m-Derived T Section

The m-derived T section of Figure 2.1 (b) is a modification of the constant-k T section. Both sections still maintain the same image impedance as defined by (2.4) but the new m-section has an LC series resonance in the shunt arm of the filter. The resonant frequency of the LC shunt arm is defined as [21]:

$$\omega_R = \frac{\omega_C}{\sqrt{1-m^2}} \quad (2.6)$$

The propagation factor for the m-derived T filter section is:

$$\psi = \ln \left(1 + \frac{1}{2} \frac{-\left(\frac{2\omega m}{\omega_c}\right)^2}{1 - (1 - m^2)\left(\frac{\omega}{\omega_c}\right)^2} + \sqrt{\frac{-\left(\frac{2\omega m}{\omega_c}\right)^2}{1 - (1 - m^2)\left(\frac{\omega}{\omega_c}\right)^2} \left(1 + \frac{1}{4} \frac{-\left(\frac{2\omega m}{\omega_c}\right)^2}{1 - (1 - m^2)\left(\frac{\omega}{\omega_c}\right)^2} \right)} \right) \quad (2.7)$$

Note that $0 < m < 1$, and if m is set to 1, the passband and stopband characteristics are identical to those of the constant-k T section. Figure 2.4 shows the real and imaginary parts of the propagation factor versus frequency for the m-derived T filter section.

Recall that the required termination for the m-derived section is the image impedance of (2.4). This impedance is frequency dependant and not easily realizable and therefore is often replaced with a resistor. It is worth while to show the magnitudes of S21 and S11 for an m-derived filter section with resistive terminations (see Figure 2.5). If we compare Figure 2.4 to Figure 2.5 we can see that the resistively terminated m-derived section has a lower attenuation. Also, the input reflection coefficient approaches unity as the frequency approaches the cutoff. This occurs because the real portion of the image impedance goes to zero at the cutoff frequency while the resistive termination remains constant over the entire frequency band. It can be clearly seen from Figure 2.4 that the best performance is obtained when $m = 0.1$. The input reflection coefficient is significantly better than the constant-k section ($m = 1$) and $|S21|$ exhibits a flatter passband and a much sharper roll-off.

It is commonly accepted that for an m-derived section, $m = 0.6$ provides the best performance. In fact this value for m provides the best output match to a resistive termination for the bisected- π m-derived filter section (this filter section is discussed later in the chapter).

(a)

(b)

Figure 2.4. The (a) attenuation and (b) phase constants of the m -derived T filter section propagation factor for various values of m .

(a)

(b)

Figure 2.5. (a) $|S_{21}|$ and (b) $|S_{11}|$ for the m -derived T section with resistive terminations for various values of m .

2.3 The Bisected- π m-Derived Filter Section

The m-derived and constant-k T filter sections have an image impedance that is a function of frequency. A resistor often replaces the required termination for these sections. As seen in Figure 2.5 a resistive termination reduces the performance of these two-port networks. One way to correct for this reduced performance is to convert the m-derived T section into a π section. This conversion changes the image impedance to [21]:

$$Z_I = Z_O \frac{1 - (1 - m^2)(\omega/\omega_C)^2}{\sqrt{1 - (\omega/\omega_C)^2}} \quad (2.8)$$

This new image impedance allows us to use m to minimize the effects of frequency. The π section can be bisected and used before a resistive termination as part of a network of filter sections. The new bisected- π m-derived filter section of Figure 2.6 has an input image impedance equal to that of (2.4) and an output image impedance as seen in (2.8). Figure 2.7 clearly shows that $m = 0.6$ provides the best match to a resistive termination.

Figure 2.6. Bisected- π m-derived termination

Figure 2.7. The real portion of the output image impedance of the bisected- π m -derived filter section

2.4 Summary

Many of the filter sections discussed in this chapter will be used in the following chapters to design the artificial transmission lines that are integral to the design of distributed amplifiers. These filter sections can be used not only to design distributed amplifiers but to design filters and any other applications that require distributed networks. The choice of which combination or simply which two-port network to use is often determined by not only the required specifications of the design but the space needed to implement that design.

Chapter 3: Bandwidth

The largest possible bandwidth for an amplifier is limited by parasitics, matching and the performance of the active devices. There are several performance metrics that are used to quantify the performance of an amplifier. Typical metrics are linearity and stability, the metric that is presented in this chapter is the gain-bandwidth product. This chapter will also briefly present the frequency performance of constant-k two-port ladder networks.

3.1 Gain-Bandwidth Product

It is obviously desirable to maximize the gain-bandwidth product. There exists a two terminal coupling network with an impedance Z (see Figure 3.1) that maximizes the gain-bandwidth product

Figure 3.1. A simple amplifier utilizing a two terminal coupling network.

This two terminal network consists of inductive and capacitive components and has an impedance described by:

$$Z = \left[\frac{1}{2} (\sqrt{\omega_c^2 - \omega^2} + j\omega) C \right]^{-1} \quad (3.1)$$

The maximum gain bandwidth product obtained by using this two terminal coupling network is [20]:

$$A_V B = \frac{g_m}{\pi C} \quad (3.2)$$

where A_V is the voltage gain and B is the 3 dB bandwidth in units of Hertz. This impedance shown in (3.1) is very similar to the image impedance of the constant-k π filter section of Figure 3.2.

Figure 3.2. A constant-k π filter section

The constant-k filter sections have both a π and T form. The π form image impedance is:

$$Z_{\pi} = \left[\frac{1}{2} (\sqrt{\omega_c^2 - \omega^2}) C \right]^{-1} \quad (3.3)$$

The ideal coupling network has an impedance that maximizes the bandwidth and by extension the gain-bandwidth product. The constant-k filter sections can be used to realize this network.

3.2 Bandwidth

The constant-k π filter section provides a means of connecting two devices without sacrificing the gain bandwidth product. The difficulty is achieving the desired gain with the required bandwidth.

The bandwidth issue can be addressed by connecting multiple filter sections in parallel, as in Figure 3.3. It can be clearly seen that constant-k T sections are being created, by connecting multiple π sections in parallel. This ladder network must be terminated with a realizable impedance. An approximate termination for the ladder network

must be used, since the image impedance of the filter section is a function of frequency. It can be shown that converting from π to T sections and terminating with a resistive element (see Figure 3.4), provides a reasonable approximation to the ideal π ladder network [20].

Figure 3.3. Parallel connected constant-k π filter sections

Figure 3.4. Resistively terminated, constant-k T filter ladder network.

To maintain the desired impedance magnitude, the inductive and capacitive components are adjusted for the number of sections desired. This method of distributing the total capacitance and inductance has the added benefit of increasing the bandwidth, which can clearly be seen from Figure 3.5 and (2.1) which also applies to the constant-k π filter section.

Figure 3.5. (a) One and two stage constant-k ladder networks and (b) the corresponding $|S_{11}|$ and $|S_{21}|$. Where $\omega_c = 2/(\sqrt{LC})$, $C = 127$ fF and $L = 318$ pH.

3.3 Summary

We now have a means of obtaining the desired bandwidth and gain from an amplifier. The distributed technique discussed in this chapter is the fundamental precept behind distributed amplification. The constant- k filter sections can be used to connect together multiple gain stages. The bandwidth of the amplifier increases as the input and output capacitances of the gain stages decrease. Therefore, it is desirable to reduce the size and gain of each gain stage in order to reduce the input and output capacitance. More gain stages can be added to achieve or maintain the desired gain of the amplifier. It is important to note that there is a practical limit to the number of gain stages. This limit is presented in the following chapter entitled Distributed Amplifier Circuit theory.

Chapter 4: Distributed Amplifier Circuit Theory

An analysis of a distributed amplifier using the image parameter method is presented in this chapter. The image parameter method was chosen for its simplicity. The resulting equations can be used in computer aided simulation for a more rigorous analysis.

4.1 ABCD parameters

The analysis begins with the ABCD matrix, which will be used later in the analysis of the distributed amplifier. The ABCD matrix is a representation of the transmission characteristics of a two-port network. The ABCD matrix is defined as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (4.1)$$

The voltage and current of port one and port two are represented by V_1 , I_1 and V_2 , $-I_2$ respectively. The negative sign for I_2 indicates that current flows out of the terminal while positive current is defined to flow into the terminal [22], [23].

One of the benefits of using the ABCD matrix is that a cascade of two-port networks has an ABCD matrix that can be determined by the multiplication of the constituent two-port ABCD transmission matrices.

A cascade of two networks is as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_3 \\ -I_3 \end{bmatrix} \quad (4.2)$$

An example of ABCD parameters expressed in terms of Y parameters for the two-port network of Figure 4.1 are as follows [21]:

$$A = 1 + \frac{Y_2}{Y_3}, \quad (4.3)$$

$$B = \frac{1}{Y_3}, \quad (4.4)$$

$$C = Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3}, \quad (4.5)$$

and

$$D = 1 + \frac{Y_1}{Y_3} \quad (4.6)$$

The ABCD parameters (4.3) - (4.6) will be used in the analysis of the distributed amplifier

Figure 4.1. A Y parameterized Generic π network

4.2 Image parameters

The image parameter method is a simple way of analyzing the performance of a two-port filter network. The analysis uses the passband and stopband characteristics as well as the ABCD transmission matrix to design the network. The image impedances for a two-port network are defined as [21]:

image impedance of port 1:

$$Z_{i1} = \sqrt{\frac{AB}{CD}} \quad (4.7)$$

image impedance of port two:

$$Z_{i2} = \sqrt{\frac{BD}{AC}} \quad (4.8)$$

The image impedances given by (4.7) and (4.8) are valid only when the other port is terminated with its corresponding image impedance.

The two-port voltage and current ratios can be expressed as follows [21]:

$$\frac{V_2}{V_1} = \sqrt{\frac{D}{A}}(\sqrt{AD} - \sqrt{BC}) \quad (4.9)$$

and

$$\frac{-I_2}{I_1} = \sqrt{\frac{A}{D}}(\sqrt{AD} - \sqrt{BC}) \quad (4.10)$$

where the propagation factor for the two-port network is:

$$e^{-\Psi} = \sqrt{AD} - \sqrt{BC} \quad (4.11)$$

In a reciprocal network $AD - BC = 1$, therefore:

$$e^{\Psi} = \frac{1}{\sqrt{AD} - \sqrt{BC}} = (\sqrt{AD} + \sqrt{BC}) \quad (4.12)$$

and

$$\cosh \Psi = \frac{(e^{\Psi} + e^{-\Psi})}{2} \quad (4.13)$$

We can show that

$$\cosh \psi = \sqrt{AD} \quad (4.14)$$

and

$$\sinh \psi = \sqrt{BC} \quad (4.15)$$

Using (4.7) through (4.15), we can define an ABCD matrix in terms of the two-port network image parameters:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{Z_{i1}}{Z_{i2}}} \cosh \psi & \sqrt{Z_{i1}Z_{i2}} \sinh \psi \\ \sqrt{(Z_{i1}Z_{i2})^{-1}} \sinh \psi & \sqrt{\frac{Z_{i2}}{Z_{i1}}} \cosh \psi \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (4.16)$$

The matrix for a network composed of n two-port networks is as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{Z_{i1,1}}{Z_{i1,2}}} \cosh \psi & \sqrt{Z_{i1,1}Z_{i1,2}} \sinh \psi \\ (\sqrt{Z_{i1,1}Z_{i1,2}})^{-1} \sinh \psi & \sqrt{\frac{Z_{i1,2}}{Z_{i1,1}}} \cosh \psi \end{bmatrix} \begin{bmatrix} V_{n+1} \\ -I_{n+1} \end{bmatrix} \quad (4.17)$$

where:

$$\psi = \sum_{k=1}^n \psi_k \quad (4.18)$$

The voltage and current ratios are now expressed as:

$$\frac{V_{n+1}}{V_1} = \sqrt{\frac{Z_{i1,2}}{Z_{i1,1}}} \sum_{k=1}^n e^{-\psi_k} \quad (4.19)$$

and

$$\frac{I_{n+1}}{I_1} = -\sqrt{\frac{Z_{i1}}{Z_{i2}}} \sum_{k=1}^n e^{-\psi_k} \quad (4.20)$$

With the equations thus far outlined in this chapter we can now proceed to the analysis of the simple distributed amplifier of Figure 4.2.

Figure 4.2. A simplified distributed amplifier (biasing is not shown)

4.3 Distributed Amplifier Analysis

The image parameter method is commonly used to analyze the performance of the artificial transmission lines created in the design of distributed amplifiers. This method assumes that the networks are terminated with their characteristic impedances and as such serves only as an estimate to the actual performance of the distributed amplifier. The image impedance is referred to as the characteristic impedance when a network is symmetrical or $Z_{i1} = Z_{i2}$.

4.3.1 Transistor model

The analysis of the distributed amplifier requires that a transistor model be chosen. A Heterojunction Bipolar Transistor (HBT) device (the model for which can be seen in Figure 4.3) is the obvious choice because the design discussed in the following chapter uses the IBM SiGe BiCMOS 7HP process. This seven metal layer process provides high speed HBTs with a reported f_T of 120 GHz and an f_{max} of 100 GHz [15].

Figure 4.3. The π model for the heterojunction bipolar transistor.

A simplified model is desired for the analysis of the distributed amplifier. The model of Figure 4.4 assumes that R_O and R_μ are very large. Therefore both R_O and R_μ have a negligible effect on the circuit and can be removed.

Figure 4.4. A simplified π model for the heterojunction bipolar transistor.

Two further simplifications are employed (see Figure 4.5). The Miller theorem is used to split C_{μ} and R_{BB} is removed to simplify the analysis. It is important to note that the Miller theorem requires a constant gain. This then requires the analysis of the distributed amplifier to assume a constant gain over the bandwidth of operation.

Figure 4.5. A further simplified π model for the heterojunction bipolar transistor.

4.3.2 Artificial Transmission Lines

The distributed amplifier can be split up into two segments, the input line and the output line which contains the gain elements. The network of Figure 4.6 uses constant- k T filter sections to create an artificial transmission line terminated with its characteristic impedance. The artificial transmission line is the input line of a distributed amplifier and as such has a voltage source as part of the left hand termination.

Figure 4.6. The input artificial transmission line of a distributed amplifier

The output artificial transmission line of Figure 4.7 is terminated at both ends by its characteristic impedance. There are N gain stages, and unlike the input line, there are N input points where the signal is transmitted to the output line.

Figure 4.7. The output artificial transmission line of the distributed amplifier.

Both the input and output artificial transmission lines have a interstage propagation factor ψ_B and ψ_C respectively.

4.3.3 Gain

To determine the voltage gain of the distributed amplifier we must first find a two-port network that has $Z_{i,k2} = Z_{i,k+11}$ and is a fundamental repeatable unit of the artificial transmission line. Figure 4.8 depicts such a section which is commonly known as an L section.

Figure 4.8. A generic L section created by removing Y_1 from the simple π section.

The ABCD parameters for the L section can be determined from (4.3) to (4.6):

$$A = 1 + \frac{Y_2}{Y_3}, \quad (4.21)$$

$$B = \frac{1}{Y_3}, \quad (4.22)$$

$$C = Y_2, \quad (4.23)$$

and

$$D = 1 \quad (4.24)$$

The voltage at any arbitrary node in the input line can be obtained by using the section of Figure 4.9 and its corresponding two-port image impedance parameters.

Figure 4.9. Input line L section

From (4.19) we have

$$V_{\pi x} = V_{in} \sqrt{\frac{Z_{iB2}}{Z_{iB1}}} e^{-(x-1/2)\psi_B} \quad (4.25)$$

where x is a number from 1 to N , and N is the number of gain stages. From Figure 4.7 the current at each node can be expressed as:

$$I_x = -g_{mx} V_{\pi x} \quad (4.26)$$

The total current as seen by either termination of Figure 4.7 can be expressed as (assuming uniform excitation):

$$I_{Z_C} = \frac{1}{2} e^{\frac{-\Psi_C}{2}} \sum_{x=1}^N I_x e^{-(N-x)\Psi_C} \quad (4.27)$$

Therefore the output voltage at either of the terminations is:

$$V_{out} = -\frac{Ng_m V_{in} Z_C}{2} \sqrt{\frac{Z_{iB2}}{Z_{iB1}}} e^{\frac{\Psi_B - \Psi_C}{2}} e^{-N\Psi_C} \sum_{x=1}^N e^{x(\Psi_C - \Psi_B)} \quad (4.28)$$

where $\sum_{x=1}^N g_{mx}$ is replaced by Ng_m assuming $g_{m1} = g_{m2} \dots = g_{mN}$

The voltage gain can now be expressed as:

$$\frac{V_{out}}{V_{in}} = -\frac{Ng_m}{2} Z_C \sqrt{\frac{Z_{iB2}}{Z_{iB1}}} e^{\frac{\Psi_B - \Psi_C}{2}} e^{-N\Psi_C} \sum_{x=1}^N e^{x(\Psi_C - \Psi_B)} \quad (4.29)$$

If we assume the input and output lines to be ideal and phase synchronized then

$\Psi = \Psi_B = \Psi_C$ and the voltage gain is now:

$$A_V = \frac{V_{out}}{V_{in}} = -\frac{Ng_m}{2} \sqrt{\frac{L_C}{C_{\mu2}}} \sqrt{\frac{Z_{iB2}}{Z_{iB1}}} e^{-N\Psi} \quad (4.30)$$

where the characteristic impedance of the output line is: $Z_C = \sqrt{\frac{L_C}{C_{\mu2}}}$

Recall that power gain is defined as:

$$G = \frac{P_{out}}{P_{in}} = \frac{|I_{Z_C}|^2 Z_C}{\left| \frac{V_{in}}{Z_B} \right|^2 Z_B} \quad (4.31)$$

Therefore the power gain for the distributed amplifier is:

$$G = \frac{N^2 g_m^2 Z_{iB}^2}{4 Z_{iB}^1} e^{-2N\psi} \sqrt{\frac{L_C L_B}{C_{\mu 2} C_T}} \quad (4.32)$$

From (4.21) to (4.24) and Figure 4.9 we can show that:

$$\frac{Z_{i2}^B}{Z_{i1}^B} = \left[\left(1 - \frac{\omega^2}{\omega_C^2} \right) + j \frac{\omega L_B}{R_\pi} \right]^{-1} \quad (4.33)$$

where $\omega_C = \frac{2}{\sqrt{L_B C_T}}$

Therefore:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{N g_m}{2 \sqrt{\left(1 - \frac{\omega^2}{\omega_C^2} \right) + j \frac{\omega L_B}{R_\pi}}} \sqrt{\frac{L_C}{C_{\mu 2}}} e^{-N\psi} \quad (4.34)$$

and

$$G = \frac{N^2 g_m^2}{4 \left[\left(1 - \frac{\omega^2}{\omega_C^2} \right) + j \frac{\omega L_B}{R_\pi} \right]} \sqrt{\frac{L_C L_B}{C_{\mu 2} C_T}} e^{-2N\psi} \quad (4.35)$$

The derivations for voltage and power gain are valid only after a large set of assumptions:

- The output artificial transmission line is lossless and therefore uses ideal capacitors and inductors in the constant-k T sections. The input artificial transmission line is also assumed to be lossless except for the addition of R_π from the transistor model.
- A simplified transistor model is used, with no parasitic resistances or capacitances.
- the feed through properties of the HBT model due to C_μ are not taken into account.
- A constant gain is assumed to allow the use of the Miller theorem.

- The frequency dependence of the constant-k T sections prevents the practical implementation of the terminations.
- the current sources are assumed to have a uniform excitation and are not phase synchronized to a wave propagating to one of the terminations.

Therefore the equations outlined in this chapter thus far serve only as a starting point for computer simulations.

4.3.4 Number of Stages

The above derivations for gain do not account for a practical limit on the number of stages. This practical limit occurs when the benefits of adding another gain stage to a distributed amplifier are out weighed by the losses introduced by the new stage. The optimum number of stages can be obtained by taking the derivative of the power gain equation for a distributed amplifier, equating the result to zero and solving for N. The accuracy of this value is dependant on including all sources of loss incurred in the design of the distributed amplifier. The optimal number of stages has been shown to be [19] - [21]:

$$N_{opt} = \frac{\ln(A_C/A_B)}{A_C - A_B} \quad (4.36)$$

where A_B and A_C represent the per stage input and output line attenuation.

It can be clearly seen from (4.36) that the optimal number of stages is limited only by the losses in the input and output lines. It is also clear that those losses increase in an exponential manner. The optimum number of stages may exceed ten but it is widely accepted that little improvement is seen beyond 8 stages [24], [25]. The optimum number of stages may be significantly lower for lossy substrates.

4.3.5 Maximum Bandwidth

The maximum possible bandwidth for a distributed amplifier is limited by f_{max} . The frequency where the maximum available power gain becomes unity (f_{max}) for a given device changes from process to process. The gain bandwidth product for a distributed amplifier is $A_v f_C$. A widely accepted limitation for distributed amplifiers is that the maximum obtainable gain bandwidth product is $0.8f_{max}$. This limitation was observed by Beyer and coworkers (1984) for GaAs FET distributed amplifiers [20]. This limitation also assumes that the bandwidth is less than f_C . The assumed bandwidth occurs at the 1 dB rolloff point.

4.4 Recent Work in Distributed Amplification

Distributed amplification has been a popular research topic in the last few years. Most of the work done has focused on larger bandwidth and larger output voltage swings. There has also been some interesting research done in an attempt to better understand the capabilities of distributed amplification. The following is a short summary of some of the available research done over the past few years. This by no means is an attempt to create a complete list of research done in distributed amplification. It is merely an attempt to provide the reader with a overview of the recent advances in distributed amplification.

Reference	DC Power (W)	DC Supply (V)	Gain (dB)	Return Loss (dB)	Output Power (dBm)	Output Voltage swing (V_{p-p})	Bandwidth (GHz)	Technology and Process
[26]	0.75	9	12	-8	20	6.3	DC - 50	0.15 μm GaAs PHEMT
[26]	0.8 - 1.1	5	8	-8	Not reported	7, 9	DC - 45	0.15 μm GaAs PHEMT
[27]	0.1	5.2	11.4	-15	Not reported	Not reported	DC - 49.1	0.18 μm SiGe BiCMOS HBT
[28]	Not reported	12	10	-5	31.5	23.8	2 - 8	GaAs HBT
[29]	0.42	6	8 - 9	-10	16 - 17	3	0.5 - 16	GaAs HBT
[30]	1.9	Not reported	15	-10	Not reported	6	DC - 58	InP D-HBT
[30]	Not reported	Not reported	12.5	-6	Not reported	Not reported	DC - 92	InP D-HBT
[31]	2	6	15	-10	20	6	0.0001 - 54	0.15 μm AlGaAs-InGaAs-AlGaAs PHEMT
[32]	0.105	4.5	13.4	-12	11	2	0.045 - 65	0.15 μm GaAs MHEMT
[33]	0.216	3	5.5	-6	Not reported	Not reported	0.5 - 8.5	0.6 μm CMOS

Table 4.1. Summary of some recently published distributed amplifier designs

Most of the distributed amplifiers presented in Table 4.1 employ a cascode gain stage. The use of the cascode gain stage increases the obtainable bandwidth.

Reference [26]: This research paper reports one single-ended and two differential distributed amplifiers. The variation in gain over the passband is approximately 5 dB for all the amplifiers. The authors report poor performance in their eye diagrams for 10 Gb/s data. No information regarding the performance of the amplifiers with 40 Gb/s input data is presented.

Reference [27]: This is a transimpedance single-ended distributed amplifier, the input or output impedance values are not reported. The transimpedance gain is 220 Ohms. This amplifier has a 3 dB gain variation in the passband. The distributed amplifier would require a 50 Ohm driver to be useful for most broadband communication systems. The output impedance would also limit the available applications.

Reference [28]: This amplifier has a gain variation of 0.4 dB and a power added efficiency of 18% to 31%. The performance over the measured bandwidth makes up for the small bandwidth that limits the usefulness of this amplifier in broadband communication systems. The cascode gain cell employs a capacitor in series with the input of the gain cell to reduce the input capacitance and improve the input line cutoff frequency.

Reference [29]: This amplifier employs capacitors at the input to reduce the input artificial transmission line capacitance. As a result the amplifier has a fairly high lower bandwidth limitation.

Reference [30]: This paper reports on several distributed amplifiers. The two that are summarized in Table 4.1, exhibit extremely large bandwidths. The large bandwidth is due to the large f_{max} and f_T of the InP process, 140 GHz and 170 GHz respectively. The report makes no mention of DC supply voltages.

Reference [31]: This amplifier employs inductive source degeneration and an inductor, capacitor, and resistor in the gate of the cascode transistor. These passive components are in place to improve stability and reduce passband gain ripple.

Reference [32]: This amplifier has an overall good performance but the InP distributed amplifiers are better. The benefit of the technology employed in this design is the lower cost.

Reference [33]: This differential amplifier employs a simple differential pair as the gain stage. The amplifier also uses on chip spiral inductors instead of transmission lines or horseshoe inductors for the artificial transmission lines.

4.5 Summary

This chapter presented a simple analysis of some of the key points in the design of a distributed amplifier. The information presented in this chapter is intended to be used as a starting point for CAD simulation. Many aspects of the derivations have been simplified for this reason.

Chapter 5: Distributed Amplifier Design

This chapter will present six distributed amplifier designs.

- Two single-ended three stage distributed amplifiers (the Indline and Singlewire amplifiers) have been fabricated and tested using IBMs BiCMOS 7HP SiGe process.
- Two single-ended five-stage distributed amplifiers (the large and Small-u amplifiers) were designed using IBM's SiGe process.
- A differential distributed amplifier designed in SiGe as a buffer.
- A differential distributed amplifier designed using TRWs InP process

All the designs use HBTs and a cascode topology. The Singlewire and Indline distributed amplifiers are the main focus of this chapter and are the only amplifiers that have been fabricated and tested.

Information regarding the metal thicknesses, widths, inductance per unit length and all other process information for the IBM and TRW technologies cannot be included in this thesis because of the proprietary nature of the information.

5.1 Design Goals

The distributed amplifiers were designed to meet the loose specifications for a pre-driver for the transmit side of a 43 Gb/s fiber optical network (see Table 5.1).

Input Reflection coefficient S11 (dB)	-10
output reflection coefficient S22 (dB)	-10
Input voltage swing (V_{p-p})	0.5
output voltage swing (V_{p-p})	1.4
3 dB bandwidth (GHz)	50

Table 5.1. Specifications for a Distributed Amplifier Pre-Driver

5.2 Topology of The Single Cell

A cascode design was chosen (as seen in Figure 5.1) for the individual gain cells of the distributed amplifiers. The cascode topology improves the isolation between the input and output artificial transmission lines. This increased isolation is brought about by the addition of the second transistor as a load or current buffer (see Figure 5.2). The second transistor supplies a small load resistance that reduces the Miller effect of $C_{\mu 1}$. Also, the common base configuration of the second transistor has the added benefit of removing the Miller effect of $C_{\mu 2}$. This removal and reduction of the Miller effect also has the potential of increasing the upper frequency limit of the gain cell. The trade off for the improvements is the added pole and the reduction in output voltage swing.

Figure 5.1. Cascode gain stage used in the distributed amplifiers

Figure 5.2. A simple model for two cascode connected transistors in the common emitter configuration

From the simplified cascode model of Figure 5.2 (ignoring capacitance) it can be shown that:

$$V_{\pi 2} = -g_{m1} V_{\pi 1} r_{e2} = -V_{\pi 1} \quad (5.1)$$

where:

$$r_{e2} = R_{\pi 2} \parallel \frac{1}{g_{m2}} \approx \frac{1}{g_{m2}} \quad (5.2)$$

The DC gain of the first stage in the cascode configuration is approximately -1, if we assume that $g_{m1} = g_{m2}$ in (5.1). Therefore the overall DC gain of the cascode configuration is approximately $g_m R$, where R is an arbitrary resistive load of the amplifier. This gain equation is identical to that of the single transistor common emitter configuration.

The previous chapter presented a simple distributed amplifier utilizing a common emitter transistor for the gain cell. The equations developed for the gain (both power and voltage) have on the surface, not changed because of the migration to the cascode gain stage. The input artificial transmission line remains the same. The main difference lies in the output artificial transmission line, and the transition from C_{μ} , split by Millers theorem into $C_{\mu 1}$ and $C_{\mu 2}$ to $C_{\mu 2}$ of the cascode transistor. Therefore the variable $C_{\mu 2}$,

which first represented the Miller capacitance split by the Miller theorem for the common emitter transistor now represents the diffusion and depletion capacitance of the base-collector junction of the second transistor in a cascode gain stage. The current source is now transformed from the simple common emitter to a cascode current source with higher output impedance (see Figure 5.3).

Figure 5.3. The output artificial transmission line transition from the common emitter device to the cascode common emitter gain stage.

The cascode gain stage of Figure 5.1 is used in all the distributed amplifiers, in approximately this form, and has three dc supplies for biasing (input bias, output bias and the cascode base bias). The supply voltage for the voltage divider is kept separate from the supply provided to the output line. This separation is in place to allow an extra degree of freedom for testing the amplifier. The separate dc supply also provides a means of turning

the amplifier off, by switching the cascode base supply voltage off. The input DC bias level is established by the preceding circuit and as such no bias circuitry is necessary for the input line of the distributed amplifier.

The emitter degeneration resistor is in place to reduce the gain of the stage to the desired level. The emitter resistor was used instead of reducing the size of the transistors due to concerns with the reliability of the smaller devices. The emitter degeneration resistor has the added benefit of reducing the input capacitance and output distortion. It is important to note here that the larger devices have larger input and output capacitances. The larger capacitances result in smaller cutoff frequencies in the artificial transmission lines.

The introduction of the emitter degeneration resistance modifies the simple gain equations presented in the preceding chapter. The R_π resistance of the common emitter single device gainstage can be replaced by $R_{\pi 1} + g_m R_{\pi 1} R_E$ for the cascode gain stage (if we ignore the capacitance). So the voltage gain and power gain equations become:

$$A_V = -\frac{NG_m}{2\sqrt{\left[(1 - \omega^2/\omega_C^2) + j\frac{\omega L_B}{R_{\pi 1} + g_m R_{\pi 1} R_E}\right]}} \sqrt{\frac{L_C}{C_{\mu 2}}} e^{-N\psi} \quad (5.3)$$

and

$$G = \frac{N^2 G_m^2}{4\left[(1 - \omega^2/\omega_C^2) + j\frac{\omega L_B}{R_{\pi 1} + R_E + g_m R_{\pi 1} R_E}\right]} \sqrt{\frac{L_C L_B}{C_{\mu 2} C_T}} e^{-N\psi} \quad (5.4)$$

Where the transconductance is now:

$$G_m = \frac{g_m}{1 + g_m R_E} \quad (5.5)$$

There are four designs using the single-ended cascode gain stage. The Singlewire and Indline designs use the same gain stage (see Figure 5.4). The active and passive devices are implemented using the models supplied by IBM. The Large-u and Small-u designs implement a slightly different cascode gain stage due to changes in the design kit. These updates changed the performance of the active and passive devices. The transistor size has been reduced and a capacitor has been added to the emitter degeneration resistor. These two designs use the same gain stage (see Figure 5.5).

Figure 5.4. The gain stage used in the Singlewire and Indline distributed amplifiers

Figure 5.5. The gain stage used in the Large-u and Small-u distributed amplifiers

5.3 The Artificial Transmission line

As discussed in previous chapters, the constant-k T section has an image impedance that is a function of frequency. For optimum performance the filter section must be terminated with its corresponding image impedance. This frequency dependant impedance is not physically realizable as a termination and so, often takes the form of a resistor. To improve the frequency response of the artificial transmission line a bisected- π section is often placed before the fifty ohm termination. This π section reduces the frequency dependence of the output image impedance and as a result improves the performance of the artificial transmission line.

The performance of the artificial transmission line is dependant on the type of filter sections used. Figure 5.6 through Figure 5.8 show a performance comparison of the

different filter sections discussed in Chapter 2. Figure 5.6 shows that the m -derived T section has a flatter passband and a better input reflection coefficient than its corresponding constant- k T section. Figure 5.7 shows that the performance of the constant- k T section is significantly improved by adding the bisected- π matching sections before the resistive terminations. Finally, Figure 5.8 shows that the best performance can be obtained by using m -derived T sections with bisected- π matching sections.

For purposes of reliability the simpler the circuit the better, so long as the specifications for the design are met. Also, the available values of inductance and capacitance as well as the size of the parasitics are limiting factors on ω_C and the performance of the artificial transmission lines. Therefore the available space, complexity of design and technology used are limitations on what filter sections to employ in the artificial transmission lines of distributed amplifiers. With those limitations in mind, it was decided that the use of m -derived π half sections were not necessary for the input or output lines of the distributed amplifiers. An artificial transmission line composed of m -derived sections is ideal for a distributed amplifier. However, there is a draw back. The m -derived sections take up more layout area. The choice then becomes a trade off between desired (or required) performance and the available die space. Therefore, the m -derived filter sections should be employed where better performance from the artificial transmission line is needed.

Figure 5.6. A comparison between the constant-k T section and the m-derived T section ($m = 0.1$).

Figure 5.7. A comparison between the m-derived T section ($m = 0.1$) and a constant-k T section with bisected- π sections before the terminations ($m = 0.6$).

Figure 5.8. A comparison between the m -derived T section ($m = 0.1$) and a m -derived T section ($m = 0.1$) with bisected- π sections ($m = 0.6$) before the terminations.

The Singlewire and Indline distributed amplifiers employ m -derived T sections in the output lines and constant- k T sections in the input lines. The inductances required for the lines were implemented using IBM's Singlewire and Indline models.

The IBM Singlewire model is a scalable cell that models the performance of a metal line over a metal ground plane (see Figure 5.9a and Figure 5.9b). The Indline model is used for metal over a deep trench ground plane (see Figure 5.9c and Figure 5.9d). The purpose of the deep trench ground plane is to minimize the loss in the inductors. The distributed amplifier employing the metal ground plane is referred to as the Singlewire amplifier and the deep trench ground plane amplifier is referred to as the Indline amplifier.

Figure 5.9. The inductor layout for the: (a) Singlewire amplifier m -derived T section and (b) Singlewire amplifier constant- k T section, (c) Indline amplifier m -derived T section and (d) Indline amplifier constant- k T section.

Agilent's Momentum EM planar simulator was used to confirm the performance of the Singlewire model but not the Indline model. The Indline model employs a deep trench mesh that cannot be accurately simulated with a planar EM simulator.

The Large- u and Small- u distributed amplifiers were designed with specifications that were slightly different from the specifications for the Singlewire and Indline ampli-

ers. It was decided that the focus for these designs would be to obtain as much gain as possible without adding more complexity and to reduce the size of the amplifier as much as possible. The specifications in Table 5.1 call for an input and output return loss better than -10 dB and a bandwidth of 50 GHz. It was decided to relax these specifications in order to conform to the request. The m-derived T section was abandoned in favour of the constant-k T section, due to the amount of space required in the layout for the inductive components.

The inductive elements for the Large-u and Small-u distributed amplifiers are composed of metal over substrate (see Figure 5.10). There are no models provided by IBM for metal over substrate inductors. Therefore, models created in Agilent's Advanced Design System (or ADS) were used to design the distributed amplifiers.

Figure 5.10. Layout of the Large-u and Small-u distributed amplifier inductors.

The circuit of Figure 5.11 is a result of a modeling exercise to determine a circuit that accurately represents the Singlewire, Large-u and Small-u inductors employed in the artificial transmission lines of the distributed amplifiers. This model was deemed necessary not only to confirm the IBM models but to also accurately model the parasitic inductance, capacitance and resistance of the inductors. The layout of the various inductors was

first simulated in Momentum to obtain the characteristic two port S-parameter matrix of the passive element. The model of Figure 5.11 was then optimized to fit the S-parameters obtained from Momentum.

The inductor model is composed of three pairs of substrate capacitive and resistive elements ($R_2, C_2, R_3, C_3, R_4, C_4$). The contribution of the oxide layer to these shunt arms is small and can be considered to be part of the substrate components. L_1 and R_1 represent the inductance and series resistance. The parallel L and R components are used as an attempt to correctly model the frequency dependant resistance and inductance that occur as a result of the substrate skin effect [34], [35].

Figure 5.11. Inductor model

5.4 The single-ended distributed amplifiers

There are four single-ended distributed amplifiers. The Singlewire and Indline distributed amplifiers employ the topology of Figure 5.12, while the Large-u and Small-u amplifiers have the topology of Figure 5.13.

Figure 5.12. Topology for the Singlewire and Indline distributed amplifiers

Figure 5.13. The topology for the Large-u and Small-u distributed amplifiers

The simulated S-parameters for the three-stage Singlewire and Indline distributed amplifiers are in Figure 5.14 through Figure 5.18. We can see from the simulations that the Singlewire and Indline distributed amplifiers meet the small signal specifications.

The number of stages for the Singlewire and Indline distributed amplifiers was determined to be $2.42 \approx 3$ by simplifying (5.4) and rearranging for N :

$$N = \frac{2A_v}{G_m} \sqrt{\frac{C_{\mu 2}}{L_C}} \quad (5.6)$$

The number of stages was confirmed through simulation. The distributed amplifiers were designed with off-chip terminations. The off-chip terminations allow for a greater degree of freedom, and the option of sweeping the terminations to optimize the results. Unfortunately the electrical length introduced by the off-chip terminations was not taken into account.

Figure 5.14. Simulated S-parameters of the Singlewire distributed amplifier using IBM models for the inductors.

Figure 5.15. Simulated S-parameters of the Singlewire distributed amplifier using Momentum models for the inductors.

Figure 5.16. Simulated S-parameters of the Indline distributed amplifier.

Figure 5.17. Calculated Group Delay from the simulated S-parameters of the Singlewire distributed amplifier

Figure 5.18. Calculated Group Delay from the simulated S-parameters of the Indline distributed amplifier

The designs were fabricated by IBM and the wafers were tested at Nortel Networks. The simulation and experimental results of the Indline and Singlewire distributed amplifiers are presented in the next chapter. The layouts for the distributed amplifiers are shown in Figure 5.19 for the Singlewire amplifier and Figure 5.20 for the Indline distributed amplifier

Figure 5.19. The layout of the Singlewire distributed amplifier

Figure 5.20. The layout of the Indline distributed amplifier

The Large-u and Small-u distributed amplifiers (see Figure 5.21), were designed with slightly changed specifications (see Table 5.2).

Input Reflection coefficient S11 (dB)	−5
output reflection coefficient S22 (dB)	−5
Forward transmission coefficient S21 (dB)	11
3 dB bandwidth (GHz)	40

Table 5.2. The Specifications for the Large-u and Small-u distributed amplifiers

The Large-u and Small-u amplifiers employ smaller transistors than the Singlewire and Indline distributed amplifiers. The smaller transistors allow the gain stages to have smaller input and output capacitances. The smaller capacitance allows for larger cut-off

frequencies and therefore larger bandwidths for the amplifiers. More than three gain stages have been added to the Large-u and Small-u distributed amplifiers to meet the gain requirements shown in Table 5.2. Note that the required gain in Table 5.2 is larger than the required gain for the Singlewire and Indline distributed amplifiers which employ three gain stages. From (5.6) it was determined that the Large-u and Small-u distributed amplifiers would require $4.28 \approx 5$ gain stages to meet the required specifications.

On chip terminations were used for the dummy loads of the Large-u and Small-u distributed amplifiers. The dummy load is the termination of the artificial transmission line that is not the input or output port of the distributed amplifier. The on chip terminations were incorporated into the design to address the problem encountered with the Singlewire and Indline designs regarding the added electrical length of the off-chip terminations. The consequences of having off-chip terminations for the Singlewire and Indline distributed amplifiers is discussed in Chapter 6. The simulation results for the Large-u and Small-u distributed amplifiers are presented in Appendix B, a summary of the results are in Table 5.3.

	Large-u	Small-u
S11 (dB)	-10	-10
S12 (dB)	-40	-40
S21 (dB)	12 - 9	9 - 11
S22 (dB)	-5	-5
3 dB Bandwidth (GHz)	42	42
Group Delay (ps)	20	20
Input referred 1 dB compression point (dBm)	-9.5	-5.14
Output referred 1 dB compression point (dBm)	-8	1.68

Table 5.3. Summary of the simulated results for the Large-u and Small-u distributed amplifiers.

Figure 5.21. The layout of the (a) Large-u and (b) Small-u distributed amplifiers

5.5 The differential distributed amplifiers

A differential distributed amplifier was designed in TRW's InP process. The process reported an f_T and f_{max} of 150 GHz. The goal for this design was to meet or exceed

the specifications outlined in Table 5.1. Specifically the large f_{max} would allow the distributed amplifier to have a bandwidth of 80 GHz. A cascode gain stage (see Figure 5.22) was employed for the reasons outlined in section 5.2. Also, the differential configuration allows for better power supply and substrate coupling noise performance, as well as a larger voltage swing.

A differential distributed amplifier was designed using the IBM SiGe process. The distributed amplifier was designed as an output buffer stage for a high speed multiplexer. The differential gain stage topology employed was the same as the InP design (see Figure 5.22)

The challenge for these two distributed amplifier designs was the differential input and output artificial transmission lines and their layout placement. The InP artificial transmission lines were even more challenging because of the thick substrate and the need to use coplanar lines. Simulation results and layouts for the InP and SiGe differential distributed amplifiers are presented in Appendix B, a summary of the results are in Table 5.4.

	SiGe differential	InP differential
S11 (dB)	- 10	- 10
S12 (dB)	-40	- 30
S21 (dB)	11 - 8	8
S22 (dB)	- 5	- 11
3 dB bandwidth (GHz)	41	80
Group Delay (ps)	20	
Input referred 1 dB compression point (dBm)	- 5	
Output referred 1 dB compression point (dBm)	3.24	

Table 5.4. Summary of the simulated results for the InP and SiGe differential distributed amplifiers.

Figure 5.22. Cascode differential pair gain stage

5.6 Summary

This chapter presented the Singlewire and Indline single-ended, three-stage, SiGe, HBT distributed amplifiers fabricated in the IBM BiCMOS 7HP process. The Large-u and Small-u distributed amplifiers were also presented. Finally, the two differential distributed amplifiers in InP and SiGe respectively were mentioned. The simulation results for the Large-u and Small-u distributed amplifiers are in Appendix B. Also, in Appendix B is the simulation and layout data for the InP and SiGe differential designs. The measured results for the Singlewire and Indline distributed amplifiers are in the following chapter.

Chapter 6: Experimental Results

In this chapter the measurement data for both the Singlewire and Indline distributed amplifiers will be presented. The data collected for the inductive input and output lines as well as the inductors for the m-derived T sections will also be discussed.

6.1 Inductor measurements

Two types of ground planes were used in the design of the inductive elements for the filter sections. Singlewire uses a metal conductor over a metal ground plane. The Singlewire amplifier has two Singlewire lines. A line using top metal over bottom metal (the output line) and the input line which uses the 4th metal layer (In a five metal layer process, see Figure 6.1) over the bottom metal layer. The IBM process uses copper for all metal layers except for the top two layers where aluminum is used. The Indline distributed amplifier uses top level metal over a deep trench lattice. This lattice forms a grid under the conductor. The purpose of the deep trench lattice is to isolate the inductor from the surrounding components by breaking up the field lines.

Figure 6.1. Cross section of the BiCMOS 7HP technology

The inductor segment lines of the distributed amplifiers were simulated and measured (see Figure 6.2 for the simulation and measurement test bench). These inductor lines are composed of the input and output filter section inductors of the distributed amplifiers artificial transmission lines

Figure 6.2. Simulation and test set up for the inductor line measurements.

Figure 6.3 through Figure 6.5 show the Indline and Singlewire S-parameter simulations and measured data for the input and output lines. These inductor lines include:

- The input inductor line of the constant k T section
- The output inductor line of the m -derived section (excluding the shunt arm)
- One shunt arm of an m -derived section.

We can see from Figure 6.3 through Figure 6.5 that the Momentum models have the worst fit to measured data. Conversely, the simulations clearly show that the IBM models are quite good at approximating the frequency response of the inductors. The Momentum models were created in an attempt to confirm the IBM models. Since, the IBM and Momentum simulation data differed, it was decided to use both in the design process.

The Indline inductors use a deep trench ground plane. This deep trench is actually a lattice of deep trench and substrate that serves to break up the field lines and isolate the inductor from its surroundings. Figure 6.3 through Figure 6.5 show that the Indline models are not as accurate as the Singlewire models but are still a reasonable approximation with regard to the frequency response. It is not possible to model the deep trench lattice in Momentum, as such no simulations were done with Momentum models for the Indline inductors.

(a)

(b)

Figure 6.3. Measured and simulated input collector line (a) Singlewire $|S_{11}|$ and $|S_{12}|$ (b) Indline $|S_{11}|$ and $|S_{12}|$.

Figure 6.4. Measured and simulated input collector shunt arm inductor (a) Singlewire $|S_{11}|$ and $|S_{12}|$ (b) Indline $|S_{11}|$ and $|S_{12}|$.

(a)

(b)

Figure 6.5. Measured and simulated base output line (a) Singlewire $|S_{11}|$ and $|S_{12}|$ (b) Indline $|S_{11}|$ and $|S_{12}|$.

The simulated and measured data for the lines tells us that the inductors are operating as designed, with relatively steady losses over the desired bandwidth (noting that Indline seems to be more lossy). It is apparent from Figure 6.5 that the shape of the Singlewire distributed amplifiers $|S_{21}|$ is heavily affected by the base input line.

6.2 Distributed Amplifier Testing

This section presents the results of testing the 50 GHz SiGe Indline and Singlewire amplifiers that incorporate the m-derived filter sections. The amplifiers consist of three gain stages interconnected with inductors formed with metal or deep trench ground planes. The objective of this section is to verify the design discussed in the previous chapter. The Singlewire $988 \mu\text{m} \times 1075 \mu\text{m}$ distributed amplifier is shown in Figure 6.6. A discussion of the test setup used to collect the data is presented. The measured S-parameters at various bias voltages are discussed as is the 1 dB gain compression. Also, process variations are explored, as well as the consequences of having off-chip terminations.

Figure 6.6. Photo of the Singlewire distributed amplifier

6.2.1 Measurement Setup

The S-parameter measurement setup was divided into two parts, software and hardware. The software part, consisting of ICCAP, was used to record and capture the S-parameter data. As well there was software that allowed remote operation (through the GPIB or general purpose interface bus) of the HP 8510C network analyzer and pico probe station. The HP 8510C network analyzer is capable of measuring the frequency response of a device under test (DUT) from 45 MHz to 50 GHz. the hardware components also included off-chip 50 Ohm terminations, DC blocking capacitors, bias Ts and DC supplies. All the equipment used with the exception of the network analyzer and DC supplies were rated for use beyond 50 GHz.

The power measurements were done with a different station that provided a signal generator and spectrum analyzer. The losses in the interconnect used to attach the amplifiers to the signal generator and spectrum analyzer were also measured for de-embedding purposes.

All testing was done at the wafer level with pico probes. The probes consisted of GSG probes (used in the measurement of the break out lines) and GSGGSG probes (used to measure the amplifiers). where G represents a ground pad and S represents a signal pad.

6.2.2 Off-Chip Terminations and Reflections

Both the Indline and Singlewire amplifiers were designed with off-chip 50 Ohm terminations. The electrical length introduced by the off-chip terminations was not taken into account and introduced multiple reflections throughout the passband. Figure 6.7 through Figure 6.11 show the typical reflections present in the S-parameters and calculated group delay as well as a spline approximation of the reflection free frequency response.

(a)

(b)

Figure 6.7. Measured and spline approximation of the (a) Singlewire amplifier $|S_{11}|$ and (b) Indline amplifier $|S_{11}|$.

(a)

(b)

Figure 6.8. Measured and spline approximation of the (a) Singlewire amplifier $|S_{12}|$ and (b) Indline amplifier $|S_{12}|$.

(a)

(b)

Figure 6.9. Measured and spline approximation of the (a) Singlewire amplifier $|S_{21}|$ and (b) Indline amplifier $|S_{21}|$.

(a)

(b)

Figure 6.10. Measured and spline approximation of the (a) Singlewire amplifier $|S_{22}|$ and (b) Indline amplifier $|S_{22}|$.

(a)

(b)

Figure 6.11. Calculated group delay using the measured data and the spline approximation to the data for the (a) Singlewire amplifier and (b) Indline amplifier.

Figure 6.12 and Figure 6.13 show a comparison between the measured and approximated reflection free input reflection coefficient of the Singlewire distributed amplifier. The output (see Figure 6.12) and input (see Figure 6.13) artificial transmission line $|S_{11}|$ was measured first with port 1 of the network analyzer and an off-chip termination for the dummy load and then with the termination replaced with port 2 of the network analyzer. It can be clearly seen that the removal of the off-chip termination also removes the reflections. A comparison between the measured $|S_{11}|$ and spline approximated reflection-free $|S_{11}|$ of the artificial transmission lines (see Figure 6.12 and Figure 6.13) shows that the spline approximation is an adequate representation of the reflection-free frequency response.

Figure 6.12. A comparison of the measured $|S_{11}|$ of the output artificial transmission line with a 50 Ohm dummy load termination and with the 50 Ohm termination replaced with port 2 of the network analyzer and the spline approximation of $|S_{11}|$ and port 2 of the network analyzer as the dummy load.

Figure 6.13. A comparison of the measured $|S_{11}|$ of the input artificial transmission line with a 50 Ohm dummy load termination and with the 50 Ohm termination replaced with port 2 of the network analyzer and the spline approximation of $|S_{11}|$ and port 2 of the network analyzer as the dummy load.

The reflections due to the off-chip terminations can be easily corrected for in a future design. The reflections can be removed by implementing on-chip terminations.

The difference between the Indline and Singlewire amplifiers is the use of the two different inductors (metal over bottom metal and top metal over deep trench respectively), it is assumed that the reflection free frequency response in the Indline amplifier is also well represented by the spline approximation. The spline approximation to the reflection free frequency response will be used for all the S-parameter and group delay plots.

6.2.3 Measured S-parameters

The S-parameters were measured with a HP 8510C network analyzer and pico probe station. The HP 8510C network analyzer is limited to a maximum bandwidth of 50 GHz. From Figure 6.15 the passband can be seen to exceed 50 GHz for both the Indline

and Singlewire distributed amplifiers. The amplifiers exhibit a passband gain (measured from 100 MHz to 50 GHz) that varies from approximately 8.5 dB to 6 dB for the Indline amplifier and 9 dB to 5 dB for the Singlewire amplifier for a passband ripple of 2.5 dB and 4 dB respectively. The input reflection coefficients are better than -15 dB for both amplifiers and the output reflection coefficients are better than -10 dB. The reverse transmission coefficient is better than -20 dB for the Indline amplifier and better than -40 dB for the Singlewire amplifier. Finally the calculated group delay from measured S-parameters is approximately 20 ps and is relatively constant over the passband. Referring back to the loose specifications (see Table 5.1), we can see that the Singlewire and Indline distributed amplifier meet or exceed many of the specifications. Both the Indline and Singlewire distributed amplifiers have a gain that is less than required by specifications.

The Singlewire distributed amplifier simulations were done with the supplied IBM models and models created from simulations in Momentum. The models created from the Momentum simulations are less accurate but still provide a relatively good estimation of the performance of the Singlewire amplifier. The Momentum models were created in an attempt to confirm the IBM models. Since, the IBM and Momentum simulation data differed, it was decided to use both in the design process. The Indline amplifier has input and output inductors created using the IBM Indline models. These models represent inductors created with the top metal over a deep trench lattice. The design of the deep trench lattice prevents simulation in Momentum. A comparison between the measured and simulated data has shown that although the Indline simulations are less accurate than the Singlewire simulations they still represent a decent estimation of the measured values.

(a)

(b)

Figure 6.14. Measured and simulated $|S_{11}|$ for the (a) Singlewire and (b) Indline distributed amplifiers.

(a)

(b)

Figure 6.15. Measured and simulated $|S_{12}|$ for the (a) Singlewire and (b) Indline distributed amplifiers.

(a)

(b)

Figure 6.16. Measured and simulated $|S_{21}|$ for the (a) Singlewire and (b) Indline distributed amplifiers.

(a)

(b)

Figure 6.17. Measured and simulated $|S_{22}|$ for the (a) Singlewire and (b) Indline distributed amplifiers.

(a)

(b)

Figure 6.18. Calculated group delay from Measured and simulated data for the (a) Singlewire amplifier and (b) Indline amplifier.

The passband of the Singlewire distributed amplifier drops by approximately 4 dB from 100MHz to 20 GHz. This phenomena is observed in the IBM simulations but not the Momentum simulations for $|S_{21}|$ of the distributed amplifier (see Figure 6.16). Recall that both the Momentum models and IBM models were used to design the distributed amplifiers. Since, the phenomena was not observed in both simulations it was decided to proceed with the fabrication of the amplifier as is. The IBM simulations of the distributed amplifiers were found to be a more accurate representation of the measured frequency response.

The drastic drop in gain for the Singlewire distributed amplifier is due to the input artificial transmission line. This can be seen from Figure 6.19. The cutoff frequency of the input line occurs at approximately 20 GHz. Conversely, the Indline distributed amplifier input and output artificial transmission lines have a much better performance (see Figure 6.20).

Figure 6.19. The input and output artificial transmission line $|S_{21}|$ for the Singlewire distributed amplifier.

Figure 6.20. The input and output artificial transmission line $|S_{21}|$ for the Indline distributed amplifier.

6.2.4 1 dB Compression point

The output power was measured with respect to input power for a few values of frequency (1 GHz, 10 GHz, 30 GHz, 49 GHz). The losses incurred in the cables connectors and other equipment were taken into account when de-embedding the collected data.

The distributed amplifier was not designed as a power device but the measurement of power can be used to determine the approximate dynamic range of the device. The dynamic range is typically measured from the noise floor (or the minimum detectable signal) to the 1 dB compression point. The 1 dB compression point is the point where the output power curve deviates from the linear approximation by 1 dB. This definition of dynamic linear range allows for approximately 10% distortion due to the intermodulation components [36].

If operation across the entire bandwidth is desired then an input power limitation as seen from Figure 6.21 is approximately measured to be 0.84 dBm for the Singlewire DA and -0.66 dBm for the Indline. This is the upper limit of input power because it is the lowest measured 1 dB input referred compression point. The corresponding output powers as seen in Figure 6.22 are 8.49 dBm and 6.42 dBm for the Singlewire and Indline DA's

respectively (the 1 dB gain compression curves are in appendix A, Figure A.13 through Figure A.24).

Referring back to the loose specifications (see Table 5.1), we can see that both the Indline and Singlewire distributed amplifiers have a voltage swing that is slightly less than specification requires.

Figure 6.21. The input referred 1 dB compression point for the Singlewire and Indline distributed amplifiers with respect to frequency

Figure 6.22. The output referred 1 dB compression point for the Singlewire and Indline distributed amplifiers with respect to frequency

6.2.5 Stability

Figure 6.23 and Figure 6.24 show the distributed amplifiers calculated stability constants (K) and (B). From the figures, it can be clearly seen that the Singlewire and Indline amplifiers are unconditionally stable ($B > 0$ and $K > 1$). The small signal stability of an amplifier is its ability to be free from oscillations [23].

Figure 6.23. The calculated stability constant K using the IBM models and the Momentum models for the distributed amplifier

Figure 6.24. The calculated stability constant B using the IBM models and the Momentum models for the distributed amplifier

6.2.6 Process Variations

The parameters of passive and active devices change from lot-to-lot, wafer-to-wafer and die-to-die. These parameter changes are due to variations in process parameters (e.g. oxide thickness), which result in changes in device dimensions. The variation in device dimension can result in changes in device performance (e.g. electrical parameters).

To obtain an idea of the process variations across the test wafer S-parameter data was collected from various locations on the wafer (Figure 6.25 through Figure 6.29). At the time, only one wafer was available and therefore only die-to-die variations on the same wafer were explored. Four sets of S-parameter data were obtained by testing dice at four locations on the wafer (centre, top edge, left edge and right edge).

The average variation with respect to the mean for both the Singlewire and Indline distributed amplifiers was obtained by first calculating the mean. That is, the average for the two-port S-parameter matrices obtained from the various locations on the wafer. Then obtaining the deviation from the mean for each of the locations and the average of the deviations with respect to frequency.

It can be seen from Table 6.1 that the distributed amplifiers are relatively insensitive to the die-to-die process variations. The larger variations are seen in $|S_{11}|$, $|S_{22}|$, and $|S_{12}|$ and as such represent very small changes. The variation in $|S_{21}|$ is under 0.5 dB and the change in group delay is less than 1.8 ps.

Distribute Amplifier	$ S_{11} $ (dB)	$ S_{12} $ (dB)	$ S_{21} $ (dB)	$ S_{22} $ (dB)	Group Delay (ps)
Singlewire	1.54	4.25	0.30	1.17	1.25
Indline	1.55	1.14	0.33	1.44	1.77

Table 6.1. The average variation from the mean S-parameters for the Singlewire and Indline distributed amplifiers.

(a)

(b)

Figure 6.25. Measured (a) Singlewire amplifier $|S_{11}|$ and (b) Indline amplifier $|S_{11}|$ in various locations across the wafer.

(a)

(b)

Figure 6.26. Measured (a) Singlewire amplifier $|S_{12}|$ and (b) Indline amplifier $|S_{12}|$ in various locations across the wafer.

(a)

(b)

Figure 6.27. Measured (a) Singlewire amplifier $|S_{21}|$ and (b) Indline amplifier $|S_{21}|$ in various locations across the wafer.

(a)

(b)

Figure 6.28. Measured (a) Singlewire amplifier $|S_{22}|$ and (b) Indline amplifier $|S_{22}|$ in various locations across the wafer.

(a)

(b)

Figure 6.29. Calculated (a) Singlewire amplifier Group Delay and (b) Indline amplifier Group Delay from measured data in various locations across the wafer

6.2.7 Variations in DC conditions

The DC conditions were changed in order to measure the frequency response of the Singlewire and Indline distributed amplifiers. The voltages were swept for the cascode DC collector supply voltage, the cascode DC base supply voltage and the input DC bias voltage. Each voltage was swept independently while the others were kept constant.

The shunt arm of the m-derived section is composed of a capacitance and an inductance. The capacitance is provided by the collector base capacitance which is composed of the depletion and junction capacitance of the cascode collector base junction. According to [37] the junction capacitance is larger than the depletion capacitance for HBTs due to the heavily doped base. This then results in a shunt arm capacitance that is largely affected by changes in the cascode collector base junction capacitance.

It can be seen from Figure 6.30 that the changes in the cascode collector supply voltage have a significant effect on the bandwidth of the distributed amplifiers. A change in the collector base voltage of the cascode transistor affects the value of the corresponding junction capacitance. Therefore the resonance in the shunt arm of the m-derived section changes with the cascode DC collector supply voltage. Changes in the resonance of the shunt arm varies the bandwidth of the distributed amplifiers. The other S-parameters and the group delay (Figure A.1 through Figure A.4 in Appendix A) exhibit some changes with shifts in the cascode DC collector supply voltage but these changes are small.

A dip in the measured S-parameters of the Indline and Singlewire amplifiers appears for some DC supply voltages. This dip may be due to the changes in the output artificial transmission line, or possibly a process variation. Note that this dip appears in some locations on the wafer with a cascode collector supply voltage of 5V for the Indline distributed amplifier (see Figure 6.27). This issue is discussed further in the summary section of this chapter.

(a)

(b)

Figure 6.30. Measured (a) Singlewire amplifier $|S_{21}|$ and (b) Indline amplifier $|S_{21}|$ for various values of cascode collector supply voltage.

Changes in the cascode base supply voltage also have an effect on the bandwidth of the distributed amplifiers. From Figure 6.31 it is clear that the bandwidth increases as the base supply voltage increases. Once again we are seeing the effect of the cascode collector base junction capacitance in the resonant shunt arm of the m -derived sections. As before the changes in S-parameters and group delay (Figure A.5 through Figure A.8) are minimal.

Figure 6.30 and Figure 6.31 show that the bandwidth of the amplifier varies with the collector base voltage on the cascode transistor. This implies that the bandwidth can be maximized by choosing the appropriate base and collector bias voltage for the cascode transistor.

The input bias voltage was swept from 850 mV to 1 V (see Table 6.2 for the corresponding output currents). The base emitter capacitance is composed of a depletion capacitance that is proportional to the collector current and a junction capacitance that changes with variations in the emitter base voltage. The input constant- k T section capacitance is insensitive to bias voltage changes because the base emitter voltage is relatively constant. Recall, that the junction capacitance is larger than the depletion capacitance and as such comprises the major portion of the base emitter capacitance. The depletion capacitance changes with the collector current but has very little effect on the total capacitance of the junction. The result is that the bandwidth of the distributed amplifiers is insensitive to changes in the input bias voltage.

Changes in the base voltage result in changes in the collector current (see Table 6.2) and therefore the g_m of the input transistor and gain of the gain cell which can be clearly seen in Figure 6.32. The other S-parameters and group delay are relatively insensitive to input bias changes (see Figure A.9 through Figure A.12).

(a)

(b)

Figure 6.31. (a) Measured Singlewire amplifier $|S_{21}|$ and (b) measured Indline amplifier $|S_{21}|$ for various values of cascode base supply voltage.

(a)

(b)

Figure 6.32. (a) Measured Singlewire distributed amplifier $|S_{21}|$ and (b) measured Indline amplifier $|S_{21}|$ for various values of input DC bias voltage.

	Singlewire Distributed Amplifier	Indline Distributed Amplifier
Input Bias (V)	Output Current (mA)	Output Current (mA)
1	18.53	17.86
950m	12.26	11.69
900m	6.75	6.42
850m	2.78	2.67

Table 6.2. Input Bias voltage and the corresponding output current

The changes in DC bias have shown that $|S_{11}|$, $|S_{22}|$, $|S_{12}|$ and group delay are only slightly affected by changes in DC voltage (Figure A.1 through Figure A.12). This shows the robustness of the distributed amplifier design. It is also important to note that $|S_{21}|$ (Figure 6.30 through Figure 6.32) is sensitive to the bias conditions but the conditions explored here well exceed normal reasonable operational variations in DC bias. In fact if we assume a 10% variation (which is quite large) from the nominal operating DC values then $|S_{21}|$ would not show significant changes in bandwidth.

6.3 Summary

This chapter presented the test results of the Singlewire and Indline distributed amplifiers, fabricated using IBM's SiGe BiCMOS 7HP technology. The test results confirm the designed operation of the distributed amplifiers with some anomalies.

Referring back to the loose specifications (see Table 5.1), we can see that the Singlewire and Indline distributed amplifiers meet or exceed most specifications. The gain of both amplifiers and the voltage swings are less than required but are still acceptable.

The early cut-off frequency of the input artificial transmission line of the Singlewire distributed amplifier results in a 4dB drop in gain from 100MHz to 20GHz. This drop in gain can be corrected by redesigning the input artificial transmission line.

The reflections introduced by off-chip terminations are very significant, but they can be corrected by simply placing the terminations on-chip.

In the variations in DC condition section of this chapter the measured S-parameter data for the Indline and Singlewire amplifiers exhibits a large dip in the passband (see Figure 6.30 through Figure 6.32). There are several possible explanations for this anomaly. Firstly it must be noted that this dip is also visible for some of the S-parameter data obtained from different locations on the wafer (see Figure 6.25 through Figure 6.29). Therefore, one possible explanation is that the dip is a product of process variations. Another possible explanation has to do with how IBM applies their metal fill to the dice. At the time of submission I was not aware of an exclusion layer that must be placed over sensitive components to prevent fill from being placed on or near them. The pcell components used in layout all have the exclusion layer, it is the custom components that must have this layer added. For example the metal ground plane for the Singlewire amplifier and the deep trench for the Indline amplifier were both custom made and as such did not include the exclusion layer. As a result, some of the amplifiers may have been compromised. In other words, blocks of metal (from top to bottom metal inclusive) were placed on and around the amplifiers. These metal blocks were not accounted for in simulation. The metal fill depending on where it was placed may have changed the frequency response of the amplifiers and may have resulted in the observed dip. The changes in the frequency response may even vary from die-to-die depending on how the fill is placed on a wafer. Another possible explanation is with regard to the reflections and spline approximation to the measured data. The spline averages out the ripples to obtain a best fit curve. This curve might not be a true representation of a reflection free frequency response, since the reflections may alter the overall position of the curve.

Chapter 7: Conclusions

This thesis presented two 0.1 - 50 GHz, single-ended, three-stage, SiGe, HBT, distributed amplifiers that were designed, fabricated and tested using IBM's BiCMOS 7HP SiGe process. Both amplifiers employ m-derived filter sections and constant-k filter sections in the artificial transmission lines. The measured performance of the Singlewire and Indline distributed amplifiers can be seen in Table 7.1 .

	Singlewire Amplifier	Indline amplifier
S11 (dB)	-10	-10
S12 (dB)	-40	-20
S21 (dB)	9 - 5	8.5 - 6
S22 (dB)	-15	-15
Group Delay (ps)	20	20
Input referred 1 dB compression point (dBm)	0.84	-0.66
Output referred 1 dB compression point (dBm)	8.49	6.42
Power dissipation (mW)	125	125
Die size (mm ²)	1 x 1.1	1 x 1.1

Table 7.1. The measured performance of the Singlewire and Indline distributed amplifiers.

A comparison of the performance of the Indline amplifier to the Singlewire amplifier clearly shows that the Indline amplifier has less gain variation and more substrate coupling. The large gain variation in the Singlewire distributed amplifier was identified and can easily be corrected by redesigning the input artificial transmission line.

The performance of the distributed amplifier is dependant on the performance of the artificial transmission lines. The cut-off ω_C frequency of the artificial transmission lines is a limiting factor for the bandwidth of a distributed amplifier. This cut-off fre-

quency is much lower for lossy substrates and can therefore make it difficult to achieve the desired bandwidth with constant-k filter sections. It is clear that the m-derived filter sections can be employed when better performance is needed to obtain the desired (or required) results.

A comparison of the measured results of the Singlewire and Indline distributed amplifiers to the published amplifiers in Table 4.1, shows that the return loss, the bandwidth, the gain and power consumption are comparable. The differences are in the output power, voltage swings and cost (cost is not shown in Table 4.1). It is obvious that for distributed amplification the exotic III - V technologies can outperform SiGe in terms of output power, voltage swing and in some cases bandwidth. The benefits of using SiGe for 40 Gb/s applications are the cost savings and the ability to have system on a chip (SOC) designs. It is important to note that although the III - V technologies can outperform SiGe the measured performance of the Singlewire and Indline distributed amplifiers shows that SiGe is still competitive with the III - V distributed amplifier designs.

7.1 Summary of Thesis Contributions

1. A 0.1 - 50 GHz single-ended, three-stage, SiGe HBT distributed amplifier employing deep trench ground planes under the inductors of the artificial transmission lines has been fabricated and tested on wafer.
2. A 0.1 - 50 GHz single-ended, three-stage, SiGe HBT distributed amplifier employing a copper ground plane under the inductors of the artificial transmission lines has been fabricated and tested on wafer.
3. The performance benefits of employing m-derived filter sections in distributed amplifier artificial transmission lines were explored.

4. The use of the SiGe process as an alternative to the more exotic III - V technologies for distributed amplification was demonstrated.

7.2 Future and Current Work

The lack of available time set a limit on what could be explored and documented in this thesis. A brief list of some of the work that could be done and what is currently being worked on is as follows.

Current work:

1. Two single-ended, five stage, HBT distributed amplifiers are awaiting fabrication. These amplifiers have been designed with more gain and less bandwidth than the Ind-line and Singlewire designs.
2. A distributed amplifier is currently being designed for a 10 Gb/s application. This amplifier will have a large input and output voltage swing.

Future work:

1. It would be interesting to see if it is possible to design a distributed power amplifier with a high power added efficiency.
2. Matrix amplification and different topologies for the gain cells could be studied to see if it is possible to increase the gain of the Singlewire and Indline distributed amplifiers without sacrificing bandwidth.
3. Another gain related investigation would be to improve gain flatness. Techniques such as feedback, feed forward and tapering could be explored to this end.

4. The performance of a differential distributed amplifier compared to two capacitively coupled single-ended distributed amplifiers could be explored. The optimum layout placement of the artificial transmission lines would also be of interest.
5. Since the distributed amplifiers presented in this thesis are for communication systems, it would be interesting to explore the best ways to optimize output eye diagrams for the various amplifiers designed and being designed as a result of this thesis.
6. The frequency dependent terminations of the artificial transmission lines are a performance stumbling block of the distributed amplifiers. It would be interesting to explore the possibilities of creating a simple frequency dependent termination.
7. Another possible avenue of study would be to explore the possibility of increasing the maximum input and output power of a distributed amplifier by controlling the constructive voltage and current effects present in the artificial transmission lines.
8. The cascode topology of the distributed amplifier designs presented in this thesis present an interesting opportunity to explore the possibility of designing variable gain distributed amplifiers.
9. Another possible avenue of exploration would be to apply the distributed techniques discussed in this thesis to other circuits such as, high frequency filters and oscillators.

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Appendix A

(a)

(b)

Figure A.1. Measured (a) Singlewire amplifier $|S_{11}|$ and (b) Indline amplifier $|S_{11}|$ for various values of cascode collector supply voltage.

(a)

(b)

Figure A.2. Measured (a) Singlewire amplifier $|S_{12}|$ and (b) Indline amplifier $|S_{12}|$ for various values of cascode collector supply voltage.

(a)

(b)

Figure A.3. Measured (a) Singlewire amplifier $|S_{22}|$ and (b) Indline amplifier $|S_{22}|$ for various values of cascode collector supply voltage.

(a)

(b)

Figure A.4. Calculated group delay from measured data for the (a) Singlewire and (b) Indline amplifiers for various values of cascode collector supply voltage.

(a)

(b)

Figure A.5. Measured (a) Singlewire amplifier $|S_{11}|$ and (b) Indline amplifier $|S_{11}|$ for various values of cascode base supply voltage.

(a)

(b)

Figure A.6. Measured (a) Singlewire amplifier $|S_{12}|$ and (b) Indline amplifier $|S_{12}|$ for various values of cascode base supply voltage.

(a)

(b)

Figure A.7. Measured (a) Singlewire amplifier $|S_{22}|$ and (b) Indline amplifier $|S_{22}|$ for various values of cascode base supply voltage.

(a)

(b)

Figure A.8. Calculated group delay from measured data for the (a) Singlewire and (b) Indline amplifiers for various values of cascode base voltage.

(a)

(b)

Figure A.9. Measured (a) Singlewire amplifier $|S_{11}|$ and (b) Indline amplifier $|S_{11}|$ for various values of input bias.

(a)

(b)

Figure A.10. Measured (a) Singlewire amplifier $|S_{12}|$ and (b) Indline amplifier $|S_{12}|$ for various values of input bias.

(a)

(b)

Figure A.11. Measured (a) Singlewire amplifier $|S_{22}|$ and (b) Indline amplifier $|S_{22}|$ for various values of input bias.

(a)

(b)

Figure A.12. Calculated group delay from measured data for the (a) Singlewire amplifier and (b) Indline amplifier for various values of input bias

Figure A.13. The measured 1 dB compression point for the Singlewire distributed amplifier at a frequency of 1 GHz.

Figure A.14. The 1 dB compression point for the Singlewire distributed amplifier at a frequency of 1 GHz (a) simulated with the IBM Singlewire model (b) simulated with the Momentum Singlewire model.

Figure A.15. The measured 1 dB compression point for the Singlewire distributed amplifier at a frequency of 10 GHz.

Figure A.16. The 1 dB compression point for the Singlewire distributed amplifier at a frequency of 10 GHz (a) simulated with the IBM Singlewire model (b) simulated with the Momentum Singlewire model.

Figure A.17. The measured 1 dB compression point for the Singlewire distributed amplifier at a frequency of 30 GHz.

Figure A.18. The 1 dB compression point for the Singlewire distributed amplifier at a frequency of 30 GHz (a) simulated with the IBM Singlewire model (b) simulated with the Momentum Singlewire model.

Figure A.19. The measured 1 dB compression point for the Singlewire distributed amplifier at a frequency of 49 GHz.

Figure A.20. The 1 dB compression point for the Singlewire distributed amplifier at a frequency of 49 GHz (a) simulated with the IBM Singlewire model (b) simulated with the Momentum Singlewire model.

Figure A.21. The 1 dB compression point for the Indline distributed amplifier at a frequency of 1 GHz (a) measured (b) simulated with the IBM Singlewire model.

Figure A.22. The 1 dB compression point for the Indline distributed amplifier at a frequency of 10 GHz (a) measured (b) simulated with the IBM Singlewire model.

Figure A.23. The 1 dB compression point for the Indline distributed amplifier at a frequency of 30 GHz (a) measured (b) simulated with the IBM Singlewire model.

Figure A.24. The 1 dB compression point for the Indline distributed amplifier at a frequency of 49 GHz (a) measured (b) simulated with the IBM Singlewire model.

Appendix B

The Large-u and Small-u SiGe distributed amplifiers

The Large-u and Small-u distributed amplifiers are identical designs except for the output line inductors. The Large-u amplifier employs a large horse-shoe inductor while the Small-u design uses a smaller horse-shoe inductor. The inductor models used in the distributed amplifier simulations were obtained from Agilent's Momentum and ADS simulators.

The simulation results for the distributed amplifiers are shown in Figure B.1 through Figure B.16. The simulation data includes S-parameters, calculated group delay, the 1 dB compression point simulated at 1 GHz, 10 GHz, 25GHz, and 40 GHz, and the stability constants K and B plotted versus frequency.

The SiGe differential distributed amplifier

The differential distributed amplifier was designed as a broadband output buffer for a high-speed multiplexer.

The simulation results for the differential distributed amplifier are shown in Figure B.1 through Figure B.20. The simulation data includes Two-port S-parameters, calculated group delay, the 1 dB compression point simulated at 1 GHz, 10 GHz, 25GHz, and 40 GHz, and the stability constants K and B plotted versus frequency. The simulated input and output eye diagrams for an input bit stream at 32 Gb/s and 40 Gb/s are shown in Figure B.20 and Figure B.20 respectively. The input data is filtered to approximate a more realistic input data stream.

(a)

(b)

Figure B.1. Simulated $|S_{11}|$ for the (a) large and Small-u amplifiers and (b) the differential amplifier.

(a)

(b)

Figure B.2. Simulated $|S_{12}|$ for the (a) large and Small-u amplifiers and (b) the differential amplifier.

(a)

(b)

Figure B.3. Simulated $|S_{21}|$ for the (a) large and Small-u amplifiers and (b) the differential amplifier.

(a)

(b)

Figure B.4. Simulated $|S_{22}|$ for the (a) large and Small-u amplifiers and (b) the differential amplifier.

(a)

(b)

Figure B.5. Simulated group delay for the (a) large and Small-u amplifiers and (b) the differential amplifier.

(a)

(b)

Figure B.6. Simulated stability constant K for the (a) large and Small-u amplifiers and (b) the differential amplifier.

(a)

(b)

Figure B.7. Simulated stability constant B for the (a) large and Small-u amplifiers and (b) the differential amplifier.

Figure B.8. The simulated 1 dB compression point at 1 GHz for the (a) Large-u amplifier, (b) Small-u amplifier.

Figure B.9. The simulated 1 dB compression point at 1 GHz for the differential distributed amplifier.

Figure B.10. The simulated 1 dB compression point at 10 GHz for the differential distributed amplifier.

Figure B.11. The simulated 1 dB compression point at 10 GHz for the (a) Large-u amplifier, (b) Small-u amplifier.

Figure B.12. The simulated 1 dB compression point at 25 GHz for the (a) Large-u amplifier, (b) Small-u amplifier.

Figure B.13. The simulated 1 dB compression point at 25 GHz for the differential distributed amplifier.

Figure B.14. The simulated 1 dB compression point at 40 GHz for the differential distributed amplifier.

Figure B.15. The simulated 1 dB compression point at 40 GHz for the (a) Large-u amplifier, (b) Small-u amplifier.

Figure B.16. The (a) input and (b) output referred 1 dB compression point for the large and Small-u distributed amplifiers and the differential distributed amplifier with respect to frequency.

Figure B.17. The simulated eye diagrams for an input 32 Gb/s data stream, (a) the ideal input eye, (b) the filtered input eye.

Figure B.18. The simulated output eye diagram for an input 32 Gb/s data stream.

Figure B.19. The simulated ideal input eye diagram for a 40 Gb/s data stream.

Figure B.20. The simulated eye diagrams for an input 40 Gb/s data stream, (a) the filtered input eye and (b) the output eye.

The InP differential distributed amplifier

This distributed amplifier was designed in TRW's InP process. The gain stage employed for the differential distributed amplifier used a cascode topology (see Figure B.22 for the circuit schematic and layout). The InP process reported an f_T and f_{max} of 150 GHz and therefore was capable of large bandwidth amplifiers. The goal for this amplifier was to obtain the largest bandwidth possible. The simulated two-port S-parameters of an eight stage differential distributed amplifier are shown in Figure B.23.

Figure B.21. The schematic of the gain stage for the InP differential amplifier.

Figure B.22. The layout of the gain stage for the InP differential amplifier.

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Figure B.23. The simulated Two-port S-parameters ($|S_{11}|$, $|S_{12}|$, $|S_{21}|$, $|S_{22}|$) for the eight stage InP distributed amplifier.