RECONFIGURABLE MATCHING NETWORKS FOR HIGH POWER GAN MICROWAVE AMPLIFIERS

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ABSTRACT

This thesis demonstrates the feasibility of using a GaN monolithic reconfigurable matching network to provide variable load impedance matching coverage for microwave power amplifiers operating in the X-band (8-12GHz). The National Research Council's GaN500 (0.5 micron) HFET process, fabricated at the Canadian Photonics Fabrication Center (CPFC), is employed throughout this work. An initial investigation of various switch topologies is first conducted, showing the advantages and limitations of using single and multi-transistor switch realizations for the development of a multi-stage programmable impedance tuner (PIT). Then, the design, optimization, fabrication and testing of a single stage of the proposed PIT structure are presented. The results show an extensive range of impedance coverage on the Smith Chart can be achieved, although this range is limited by losses. Finally, the co-integration of the resulting programmable tuners within a GaN power amplifier circuit is simulated, and its performance is studied.

ACKNOWLEDGMENTS

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On a personal note, I would like to express my sincerest gratitude to my father, sister, and grandmother for the continuous encouragement which helped me endure tough moments. Also, my cousin Karim, who has been an inspiration and example for me since I first moved to Canada for my undergraduate degree. Last but certainly not least, my finance Maha, whose love, understanding, and patience gave me the confidence and strength I needed to achieve success.

List of Abbreviations

AC	Alternating Current
BTS	Ground Base Transceiver Stations
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
CPFC	CPFC Canada Photonics Fabrication Center, belongs to NRC
CPW	Coplanar Waveguide
CG	Common Gate
CS	Common Source
DC	Direct Current
DK	Design Kit
DUT	Device Under Test
EM	Electromagnetic
EVM	Error Vector Magnitude
FET	Field Effect Transistor
f_{MAX}	Maximum Stable Frequency
FPGA	Field Programmable Gate Array
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
HPA	High-Power Amplifier
IC	Integrated Circuit
IL	Insertion Loss
IM	Intermodulation
IP3	Third-Order Intercept Point
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MEMS	Microelectro- Mechanical Switches
MESFET	Metal Semiconductor Field Effect Transistor
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
mm-wave	Millimeter-Wave
NOF	Number of Fingers
NRC	NRC National Research Council, Canada
OFDM	Orthogonal Frequency-Division Multiplexing
P_{1dB}	1-dB Compression Point

PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average-Power Ratio
PIT	Programmable Impedance Tuner
Q	Quality Factor
RF	Radio Frequency
RMS	Root Mean Squared
SOLT	Short-Open-Load-Thru
TE	Transverse Electric Mode
SP	Scattering Parameters
TEM	Transverse Electromagnetic Mode
TM	Transverse Magnetic Mode
TRL	Thru-Reflect-Load
UGW	Unit Gate Width
VNA	Vector Network Analyzer

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1.0 INTRODUCTION

1.1 MOTIVATION AND OVERVIEW

In today's cost-driven commercial and military industries, emphasis to develop low cost, small size and more versatile devices has never been higher. High power amplifiers (HPAs) are crucial transceiver components used in a wide variety of military and commercial applications, ranging from radar active array antennas to ground base transceiver stations (BTS). These amplifiers dominate a large portion of the overall transceiver power. Consequently, every measure must be taken to ensure optimum power transfer is achieved.

Impedance mismatches often occur between an antenna and a power amplifier as a result of varying operational conditions, temperature drift and aging [1]. These mismatches can affect the efficiency, power gain, maximum output power and linearity. Furthermore, optimal output impedances of power amplifiers vary for different operating frequencies and changing input power.

Thus, the need to achieve high-efficiency, broadband operation without redundant circuitry draws attention to developing reconfigurable impedance matching networks, or Programmable Impedance Tuners (PITs). Such reconfigurable networks can be programmed to deliver optimal impedance points for HPAs in order to operate at diverse wireless standards, as well as different signal modulation schemes such as OFDM and QAM.

Gallium Nitride (GaN) is an emerging process technology, which is a wide band-gap semiconductor. Inherently, it provides larger power handling capability for the same feature size when compared to CMOS. Also, GaN employs a High-Electron Mobility Transistor (HEMT) structure for active devices which have improved frequency performance when compared to LDMOS. Hence, it is an obvious choice when designing HPAs.

1.2 THESIS OBJECTIVES

The overall objective of this thesis is to demonstrate the feasibility of using a reconfigurable matching network that can provide large load matching coverage for PAs operating in the X-band (8-12GHz) using the GaN500 process, fabricated at the Canadian Photonics Fabrication Center (CPFC).

The specific objectives in pursuit of this goal are:

1. Investigate various switch topologies using GaN500 technology;
2. Design, optimize, fabricate and test candidate switch and programmable tuner structures;
3. Simulate the co-integration of the resulting programmable tuner with a GaN power amplifier and study its performance.

1.3 THESIS ORGANIZATION

Chapter 2 highlights key concepts on power amplifiers and impedance matching, as well as an overview on modeling losses in distributed circuits. A literature review on reconfigurable matching networks is also included in this chapter.

Chapter 3 discusses the design procedure of a single-stage PIT, which includes an investigation into various FET switch architectures. Characterizations of active devices and different components that will be designed are briefly discussed.

Chapter 4 presents test procedures and measurement results for small and large signal analysis of 3 separate circuits designed for this thesis, which include proof-of-concept single stage PITs, and common- gate configured active device.

Chapter 5 presents full post-layout simulation results for an eight-stage PIT with PA integration.

Chapter 6 concludes the thesis, summarizes the contributions to research and provides some suggestions for possible future work.

2.0 POWER AMPLIFIER CONCEPTS AND INVESTIGATION OF IMPEDANCE MATCHING NETWORKS

Although there will be no PA design carried out as part of this thesis, it is important to highlight conventional PA classes of operation and relevant figures of merit. Hence, the main power amplifier performance parameters such as power gain, efficiency and conduction angle are presented. Also, basic impedance matching techniques, as well as an overview on modelling losses in distributed transmission line circuits and FET switches will be discussed. A literature review on reconfigurable matching networks is finally included in this chapter.

2.1 POWER AMPLIFIERS

Power amplifiers are crucial components of radio transmitters, where they drive signals to the antenna on the transmit side of the radio. These amplifiers consume a large portion of the overall transceiver power, and hence require special design procedures to maintain high efficiency, achieve low power consumption and sufficiently high output RF power, while maintaining linearity.

Additionally, some complex modulation schemes like OFDM and QAM with large peak to average ratios require some threshold of linearity. Linearity and efficiency are often competing characteristics in a physical design of a PA. Consequently, designing for both can be a difficult task. Additionally, the PA must deliver enough power to compensate

for losses from degradation of signal and interference. Thus, the delivered power to the antennas is a significant parameter.

In addition to efficiency and linearity being competing characteristics, the load impedance (along with maximum delivered power) changes with various input powers. This trade-off occurs due to the physical limitations of transistors and the circuit topology. Traditional power amplifiers have output matching networks that would maximize the delivered power and efficiency at a single expected input power. However, modern devices may not always need to transmit at the same output power and therefore the input power can be backed off to conserve battery consumption. It is still desirable to maintain a constant efficiency despite input power changes. This type of situation presents a need for PAs to have a tunable gate bias and more importantly a tunable output matching network.

2.1.1 LINEARITY AND INTERMODULATION IN PAS

Non-linearities in PAs are generated from intrinsic properties of active devices, the circuit topology, and the limited supplies in the circuit. It can affect performance through gain compression, harmonics, and phase shift. Testing a circuit's linearity in a single carrier transmitter is carried out by applying a single tone and measuring the 1-dB compression point, which is simply the power level at the output (or input) where the output power is 1 dB less than it would have been in an ideally linear device. This is difficult to observe in the lab when using a highly linear technology such as GaN.

In today's modern broadband systems, issues with equalization, impulsive noise, and interference can be corrected using multi-tone systems. Such systems include orthogonal frequency-division multiplexing (OFDM) as well as Orthogonal Frequency-Division Multiple Access (OFDMA). This mitigates signal degradation due to signal compression, but now intermodulation (IM) distortion between carriers becomes a significant factor, especially third-order harmonics.

Therefore, the third-order intercept point (IP3) is used to measure the third-order IM products in multi-carrier systems. By introducing two fundamental tones *f1*, *f2* with equal power and observing the resulting 3rd order intermodulation tones (IM3) at $2f_2$-f_1 and $2f_1$-f_2, The IP3 can be extrapolated from the hypothetical intersection of fundamental and IM3. Distortions resulting from single tone compression differ from IM3 effects, yet a linear relationship is present in Equation 2.1 below [1].

$$P_{1dB} = IP3 - 9.66dB \quad (2.1)$$

P_{1dB}, IM3, and the relationship between them can be illustrated by plotting the fundamental output and IM output power as a function of input power [1], as shown in Figure 2.1.

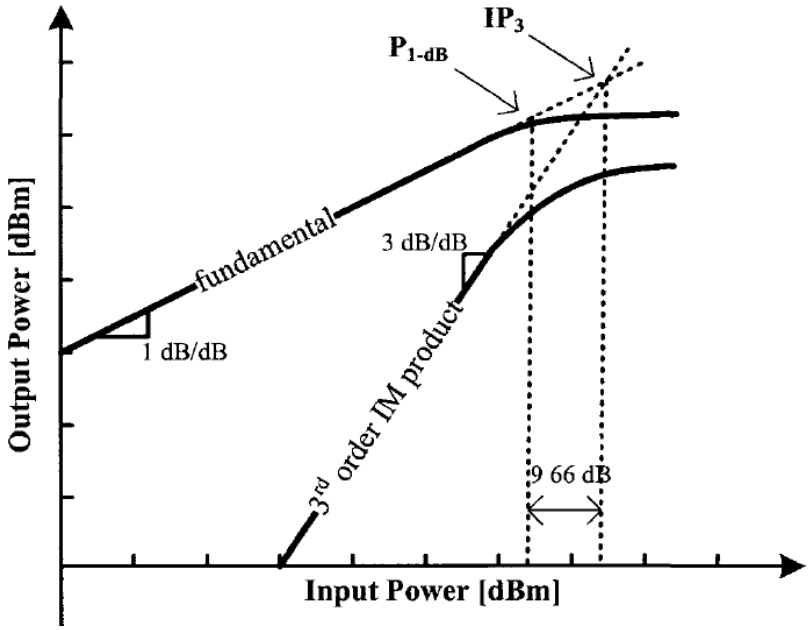


Figure 2.1: Fundamental and IM3 as a function of Input power [1].

2.1.2 Power-Added-Efficiency (PAE)

The ratio of the output RF power to the consumed DC power, efficiency (η), measures the PA's capability to convert power from DC to RF. However, it is not the best indication of a PA's usefulness as the amplifier can produce no signal gain, yet have high drain efficiency. Consequently, power-added-efficiency (PAE) is introduced in Equation 2.2 below to quantify the effectiveness of a PA.

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \eta\left(1 - \frac{1}{G}\right) \tag{2.2}$$

PAs reach peak efficiency when they achieve maximum current swing and drain voltage. But as the signal swing increases non-linear effects begin to appear. When designing with GaN technology, it becomes possible to operate at voltages in the 40V or greater, with significant current- carrying capabilities, all while maintaining linearity.

2.1.3 PA OPERATING CATEGORIES

Power amplifiers can be categorized into three groups: Linear (Class A), Non-linear (Class AB, B, C), and switching amplifiers (Class E, F, etc.). Each group presents advantages as well as drawbacks, so careful consideration must be paid when designing for each application. The highest achievable linearity with Class A amplifiers comes at the expense of efficiency, while switching amplifiers; linearity is traded for efficiency. Class AB offers greater efficiency compared to Class A, while still maintaining favorable linearity compared to Class B & C. These characteristics are shown in Figure 2.2.

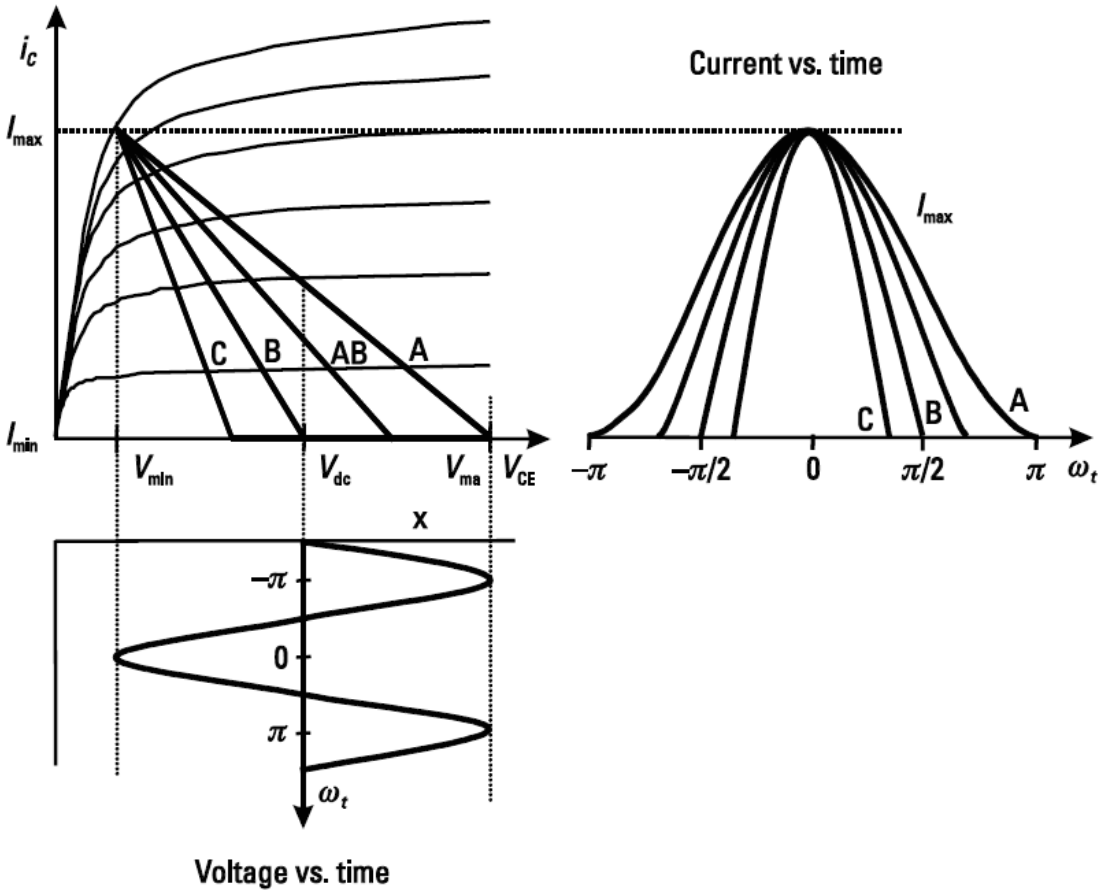


Figure 2.2: Current and Voltage excursions for classes of PAs [1].

2.1.4 OUTPUT POWER AND MATCHING

Amplifiers handling low input power usually do not suffer the effects of non-linearity. Thus, only conjugate matching is required to find the load impedance (R_L) which can deliver optimum power transfer and good noise behavior. This situation is shown in Figure 2.3. Conversely, HPAs require large-signal operation, and non-linearities are factored into the equation. Consequently, small signal output matching is not an appropriate design technique for maximizing output power.

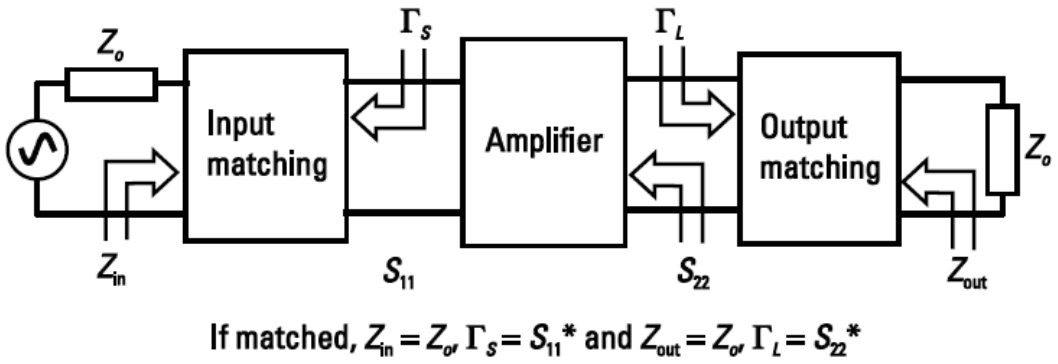


Figure 2.3: Block diagram of amplifier matching circuits [1].

A Load pull analysis is a standard technique used to determine the optimal load impedance (Γ_{opt}) needed during large signal operation to resonate out the effects of parasitic components. Γ_{opt} maximizes signal swing and produces a roughly constant ratio of RF power to DC power [2]. Improvements in gain performance when compared to small signal matching in a PA can be seen in Figure 2.4.

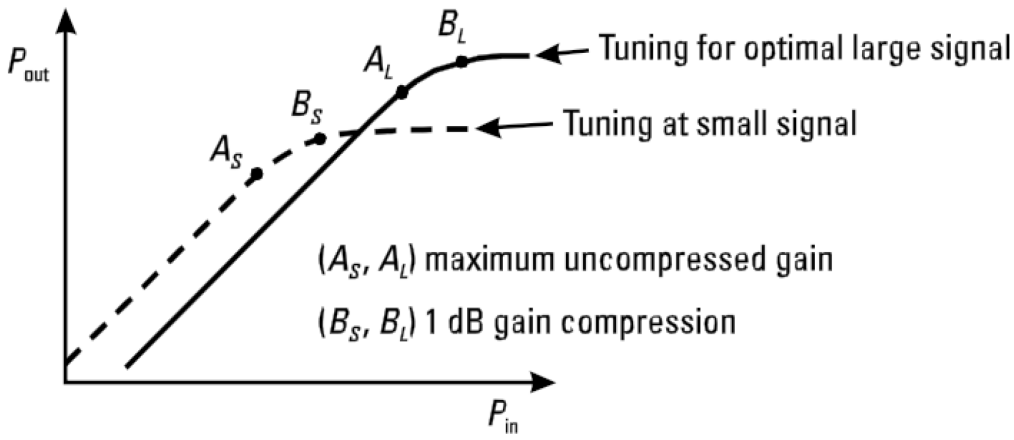


Figure 2.4: P_{out} vs P_{in} with small vs large signal matching [1].

Γ_{opt} is specific only for a particular operating frequency, and can also change with varying environmental conditions. Hence, multiple load pull iterations are needed during design to uncover multiple operating points for the PA, which are needed for reconfigurable matching discussed in a later section. A typical PA would display the gain, efficiency and linearity behavior versus power shown in Figure 2.5.

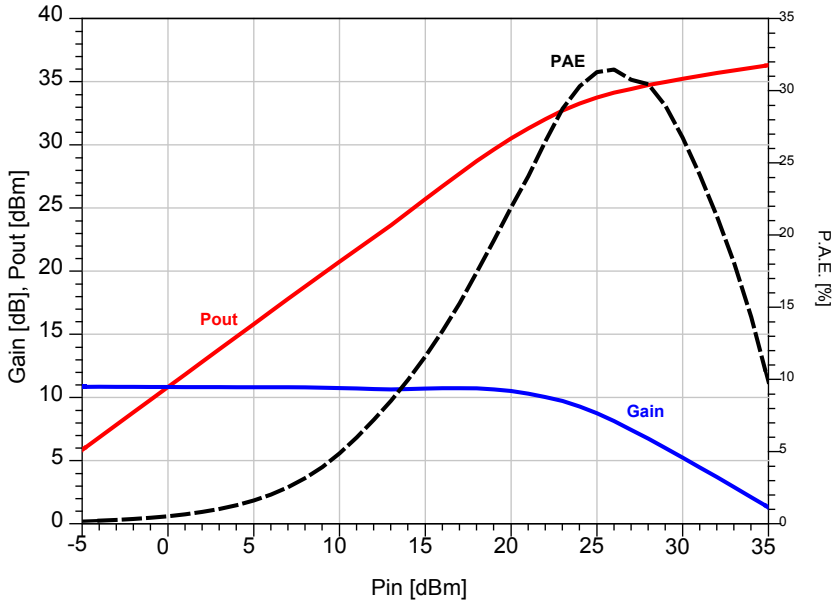


Figure 2.5: Typical performance characteristics of a PA.

2.2 IMPEDANCE MATCHING NETWORKS

There are several methods which can be used to design impedance matching networks, such as distributed transmission-line/stub matching, lumped element matching, and hybrid lumped-distributed matching. In most microwave applications, interconnect transmission lines have a characteristic impedance of 50Ω. Thus, the input and output ports need to match to 50Ω [3]. For the purposes of this research, only output matching of a typical PA is considered, as illustrated in Figure 2.6.

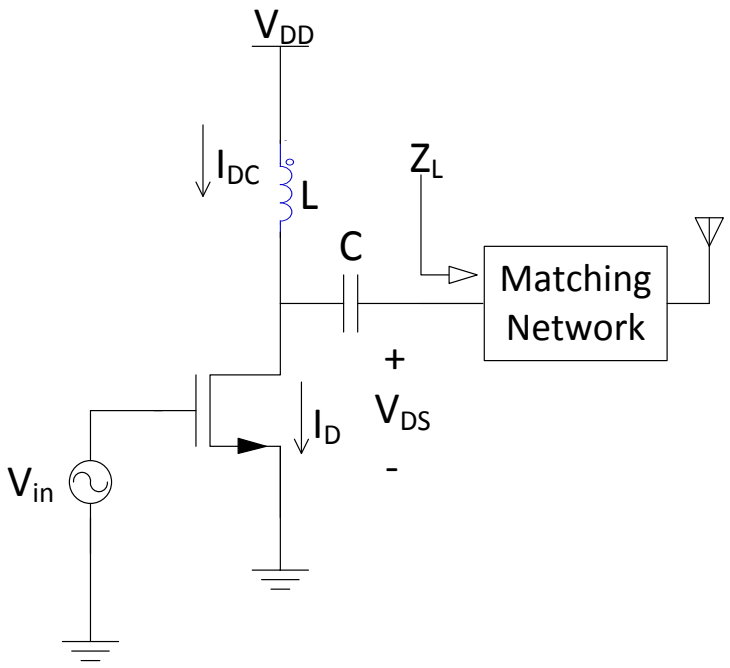


Figure 2.6: A typical common-source amplifier with output matching.

2.2.1 TRANSMISSION LINE MATCHING AND QUARTER-WAVELENGTH TRANSFORMERS

A standard microstrip line can be used as a stub in an open-circuit or a short circuited configuration as a distributed impedance matching stub. Alternatively, quarter wave

(λ/4) transformer sections can be employed, for which it is well known [4] that if the characteristic impedance of the line (Z_{ser}) is set to $\sqrt{Z_o Z_L}$, then the load Z_L is matched at the center frequency where the transformer length (l) corresponds to λ/4.

Stub matching essentially uses transmission lines placed in series/shunt (open and short) configurations as shown in Figure 2.7. Matching is carried out by choosing a suitable stub length. The main drawback of this method is the difficulty in realizing a reconfigurable implementation, which would require both the length and position of the stub to change.

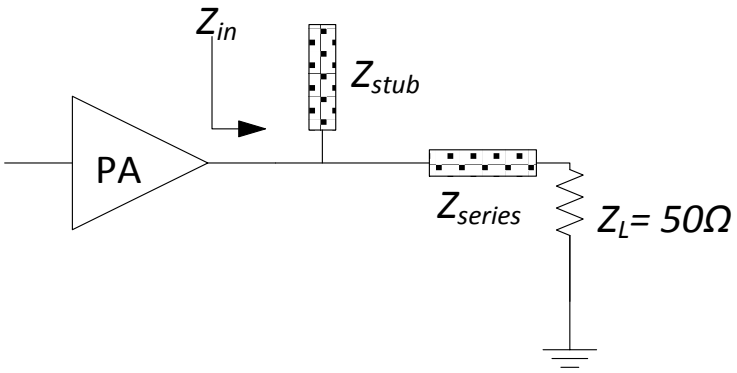


Figure 2.7: Transmission line (stub) matching.

2.2.2 LUMPED MATCHING

One of the most common matching techniques, lumped matching incorporates two reactive elements to match arbitrary load impedance, as shown in Figure 2.8. The drawbacks to using only two elements is that matching is only achieved for a narrowband of frequencies [4] and lumped elements have a limited upper frequency of operation.

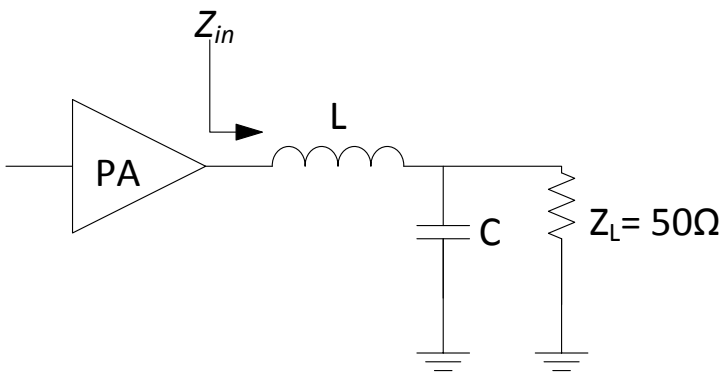


Figure 2.8: Lumped element matching.

2.2.3 HYBRID LUMPED-DISTRIBUTED MATCHING

As the frequency of operation increases, lumped inductors exhibit undesirable stray capacitance, excessive losses and spurious resonances [5]. Such effects can be mitigated by employing distributed circuit architectures and using transmission-line matching elements. Thus, for X-band applications, a hybrid method which combines lumped and distributed elements may be desirable. Figure 2.9 depicts an example of a matching circuit employing a lumped capacitor with a distributed transmission line matching element.

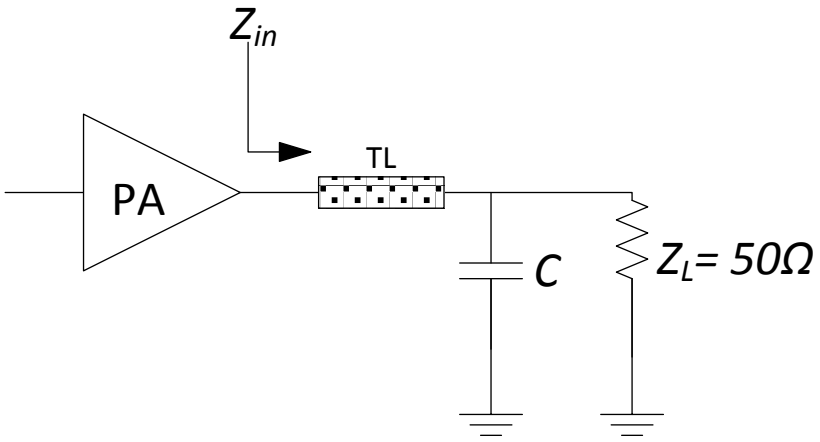


Figure 2.9: Hybrid lumped-distributed matching.

2.2.4 MULTI-STAGE MATCHING

The circuit topologies discussed so far include a single pair of series/shunt components and thus provide narrowband matching for PAs. However, the bandwidth of impedance matching can be significantly improved by adopting distributed concepts discussed in [6] [7]. In order to get a larger bandwidth and realize large impedance ratios, more elements are required in the matching networks [4].

Multi-stage circuitry illustrated in Figure 2.10 consists of series/shunt lumped elements, which can be studied as a series of cascaded lumped matching networks [7]. Ideally, the voltage transfer characteristics and of the circuit will continue to improve with additional stage added [6]. However, losses due to non-ideal components begin to significantly degrade performance.

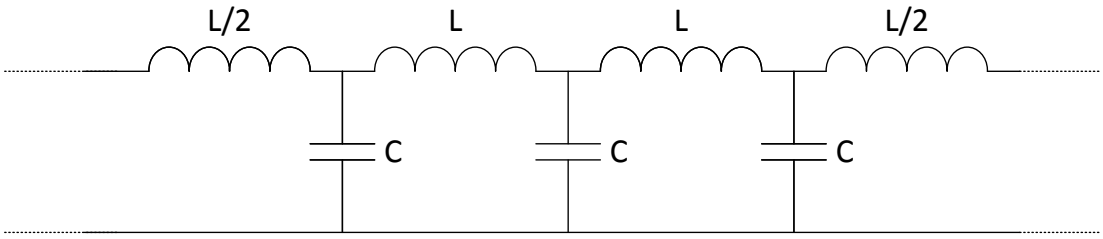


Figure 2.10: A multi-stage network using series and shunt impedances.

2.2.5 RECONFIGURABLE MATCHING TECHNIQUES

Over the years, various topologies have been studied [8] [9] [10] to provide maximum adjustability to matching networks, which can be measured by observing all the possible impedance points that can be produced by such networks on a smith chart. Some widely

used topologies include modifications of the hybrid lumped-distributed matching network.

Commonly used structures include employing switched capacitors or varactors to 'tune' various combinations of impedance. A reconfigurable network using switches will produce 2^n number of points on the Smith Chart, where *n* denotes the number of stages used. The effectiveness of this approach greatly depends on the choice of switches employed, as discussed in Section 3.3 of this thesis.

On the other hand, using varactors will provide continuous tuning and hence an infinite number of impedance points. However, the area covered on the smith chart will be limited by the achievable capacitance range of the varactors. The range of capacitance per stage offered by varactor based approaches ranges between C_{fix} + $C_{var(min)}$ and C_{fix} + $C_{var(max)}$, while switched based tuners can theoretically range from 0 to C_{fix}.

To demonstrate the difference in approach, two- 8-stage tuners illustrated in Figure 2.11 are simulated at 10GHz using 1pF fixed capacitance and either ideal voltage switches or sample MOS 0.5µm-wide varactors. From Figure 2.12, it is observed that while a switched capacitor PIT can only produce 2^8=256 points on the smith chart, its coverage is much greater than the continuously tunable impedance coverage obtained from varactor based PITs.

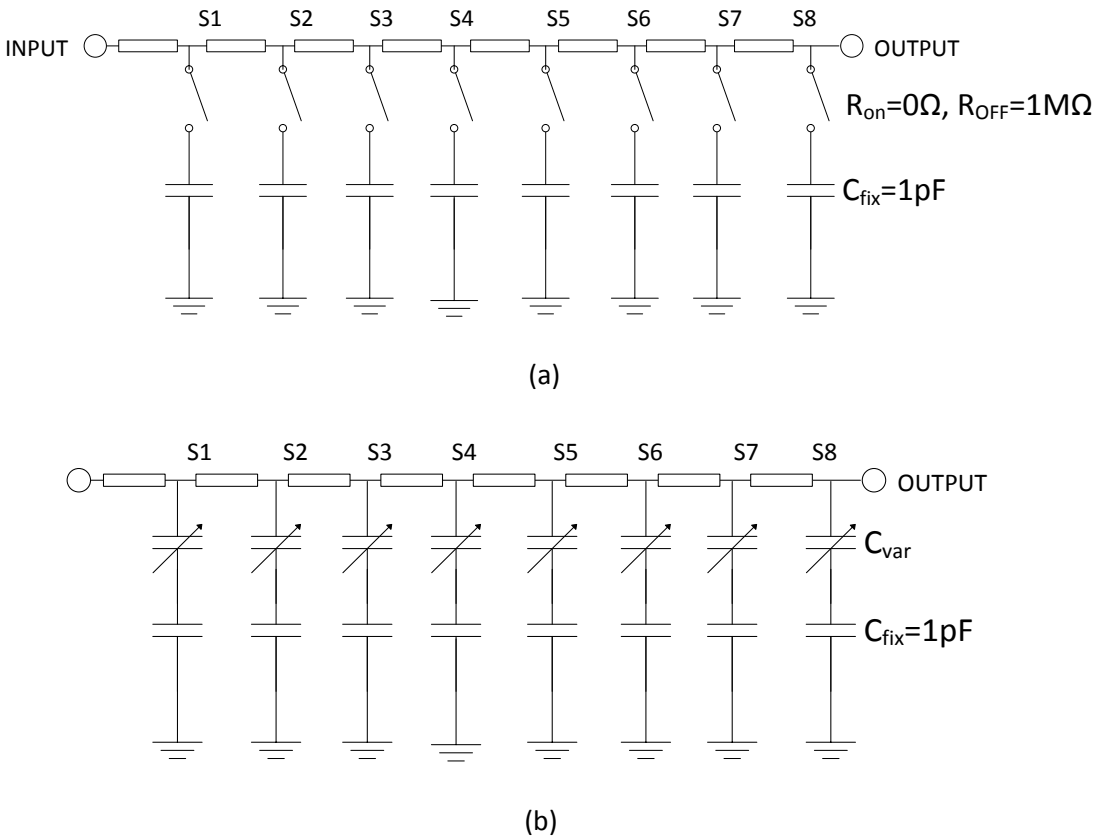


Figure 2.11: A reconfigurable distributed matching network using (a) ideal switches, (b) varactors

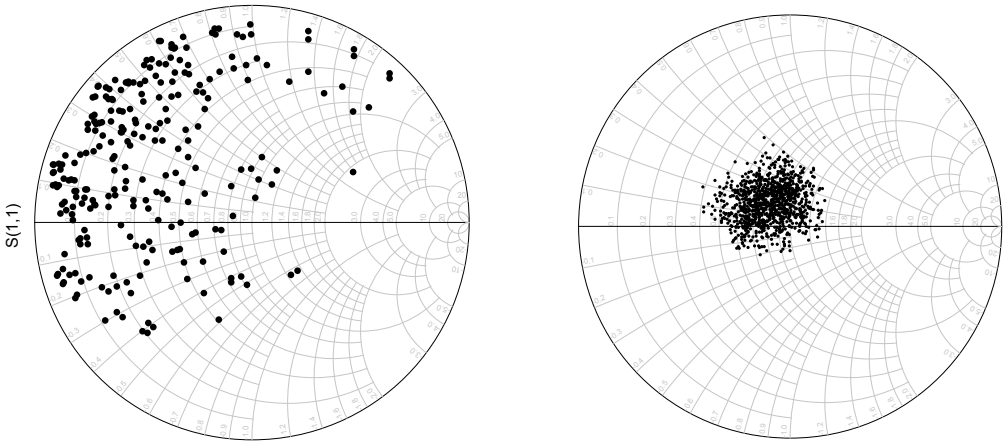


Figure 2.12: Typical Smith chart coverage for reconfigurable impedance matching using switches (left) or varactors (right).

2.3 MODELLING LOSSES IN MATCHING NETWORKS

Losses in a multi-stage network can be analyzed by considering it as a series of interconnected, cascaded two port sections such as the one illustrated in Figure 2.13. Such sections can be combinations of T-sections and π equivalent networks illustrated in Figure 2.14. This allows the study of the transmission properties of individual stages using two-port parameter extraction.

Figure 2.13: A Two-port network

By treating equivalent networks as a two port network, small signal s-parameters can be used to obtain impedance [Z] and admittance [Y] matrices [11]. As a result, losses in each series and shunt component can be directly calculated. The corresponding equations supporting Y and Z parameters are expressed as

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{2.3}$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{2.4}$$

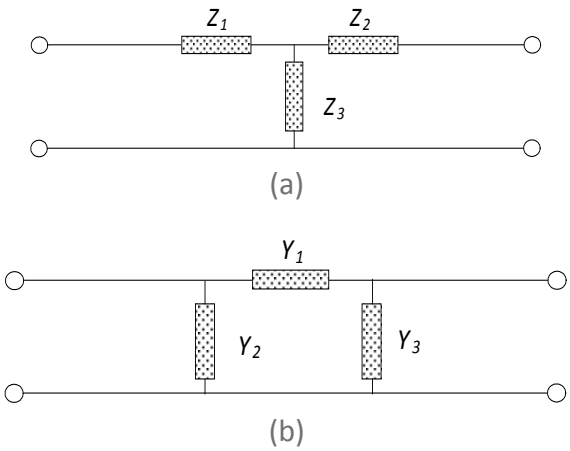


Figure 2.14: (a) T-section and (b) π-section networks [7].

Therefore, impedance of components in a T- section is described as:

$$Z_1 = z_{11} - z_{12} \tag{2.5}$$

$$Z_2 = z_{22} - z_{12} \tag{2.6}$$

$$Z_3 = z_{12} \tag{2.7}$$

Conversely, admittance is utilized in π- sections such that:

$$Y_1 = -y_{12} \tag{2.8}$$

$$Y_2 = y_{11} - y_{12} \tag{2.9}$$

$$Y_3 = y_{22} - y_{12} \tag{2.10}$$

2.3.1 CASCADING TWO-PORT NETWORKS AND THE TRANSMISSION MATRIX

ABCD Parameters (Transmission Matrices) are another form of useful matrices expressed through equation 2.11 below, which can be directly obtained from scattering parameters. Unlike Y and Z matrices, ABCD parameters inherently allow for cascading 2 port networks, as presented in Figure 2.15. Thus, through the study of an individual

stage, a full model of a distributed network consisting of *N*-identical stages can be realized. Additionally, this can be used in de-embedding techniques discussed in later sections.

$$\begin{bmatrix} v_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} v_2 \\ -I_2 \end{bmatrix} \tag{2.11}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} [\dots] \begin{bmatrix} A_N & B_N \\ C_N & D_N \end{bmatrix} \tag{2.12}$$

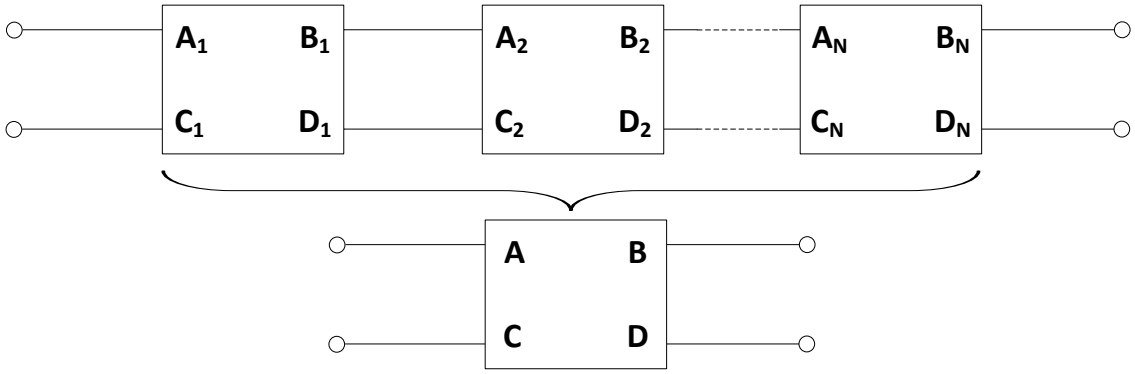


Figure 2.15: Using ABCD parameters to Cascade 2-Port Networks.

2.3.2 FET SWITCHES

As mentioned in section 2.2.5, switched capacitors are commonly used in PITs. Taking advantage of the availability of MMIC Field effect transistors (FET) models in any modern technology, it is possible to utilize them in an active switch configuration. By applying a negative gate bias voltage V_g, the drain- to-source resistance R_{ds} in a FET channel acts as a voltage-controlled resistor in parallel with a small capacitor. Conversely, the FET will exhibit a small on state resistance when positive bias is applied. Therefore, a low impedance state and high impedance state can mimic switch *ON* and *OFF* states re-

spectively. This situation is depicted in Figure 2.16. To produce an OFF state, a negative V_{gs} bias is applied such that threshold voltage (V_{th}) of the device is smaller in magnitude (i.e. $|V_{gs}| > |V_{th}|$). Otherwise, the FET switch is in a low impedance state.

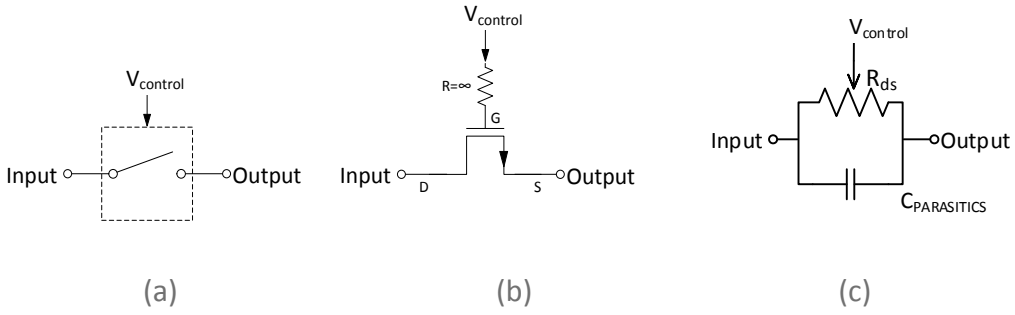


Figure 2.16: An ideal voltage controlled switch, (b) equivalent FET switch, and (c) equivalent switch model.

However, the intrinsic gate-to-source C_{gs} and drain-to-gate capacitances C_{gd} and device parasitics limit the performance of the FET switch at higher frequencies [5], leading to an overall $C_{PARASITIC}$ between the two ports. Some of the most important characteristics of FET switches are insertion loss (IL) and isolation. When the FET is in the ON state, it is important to insure drain-source insertion losses are at a minimum. Similarly, When the FET is OFF, high isolation is required to insure minimum leakage through the transistor occurs.

It is difficult to have a single series FET switch which will exhibit high isolation characteristics with low insertion loss. Section 3.3.3 will investigate how well GaN FETs can perform as switches.

2.3.3 ATTENUATION CHARACTERISTICS OF COPLANAR WAVEGUIDES

In a hybrid impedance matching network, coplanar waveguides (CPW) can be used instead of transmission lines to provide the required series matching impedance. When an mm wave propagates along a CPW, it suffers attenuation losses (α). To provide an accurate representation of losses through studied networks, and to attempt to minimize such losses, attenuation properties of CPWs are investigated.

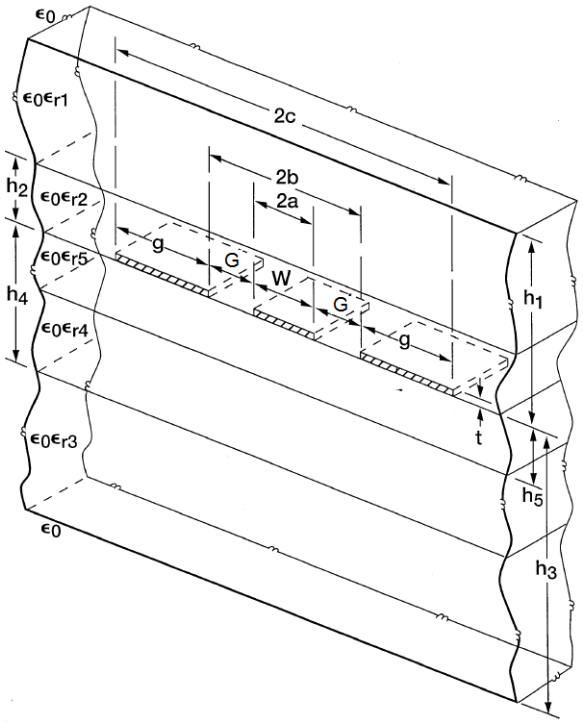


Figure 2.17: CPW with finite width ground planes on a dielectric substrate of finite thickness.

Attenuation losses are a result of conductor and dielectric non-idealities [12], and can be represented as:

$$\alpha = \alpha_{conductor} + \alpha_{dielectric} \tag{2.13}$$

There are various methods using for estimating α, such as the conformal mapping and Mode-Matching methods discussed in [12] which utilize substrate parameters in analytical expressions.

$$\alpha_{dielectric} = \frac{\pi}{\lambda_o}\frac{\varepsilon_r}{\sqrt{\varepsilon_{eff}}} q.tan\delta \text{ Nepers/m} \quad (2.14)$$

$$\alpha_{conductor} = \frac{R_c+R_g}{2Z_o} \text{ Nepers/m} \quad (2.15)$$

Where λ_o is the free space wavelength, ε_r is the relative permittivity of the substrate, $tan\delta$ is the dielectric loss tangent, ε_{eff} is the effective dielectric constant, q is the filling factor, R_c is the series resistance in ohms per unit length of the center strip conductor, and R_g is the distributed series resistance in ohms per unit length of the ground planes. The assumption made in deriving this expression is that the thickness of the CPW conductors is far greater than the skin depth δ in the metal.

Another approach described in [13] [11] involves the use of the complex propagation constant Υ, which can be described as:

$$\gamma = \alpha + j\beta \quad (2.16)$$

ABCD parameters can be exploited to extract the attenuation per unit length of a line from the propagation constant (Υ) using the following equations:

$$\gamma = \frac{cosh^{-1}(A)}{l}\frac{Nepers}{m} = 8.688\left(\frac{cosh^{-1}(A)}{l}\right) \text{dB/m} \quad (2.17)$$

$$\alpha = Real(\gamma) \text{ dB/m} \quad (2.18)$$

2.4 DESIGN CONCEPT

The proposed system level concept for this thesis is shown in Figure 2.18. It consists of a feedback network in order to transform the load impedance to predefined optimum impedance required by the unmatched PA. The RMS detectors and ADC are behavioral blocks that would complete the feedback loop, which is programmed by the FGPA as shown in Figure 2.18.

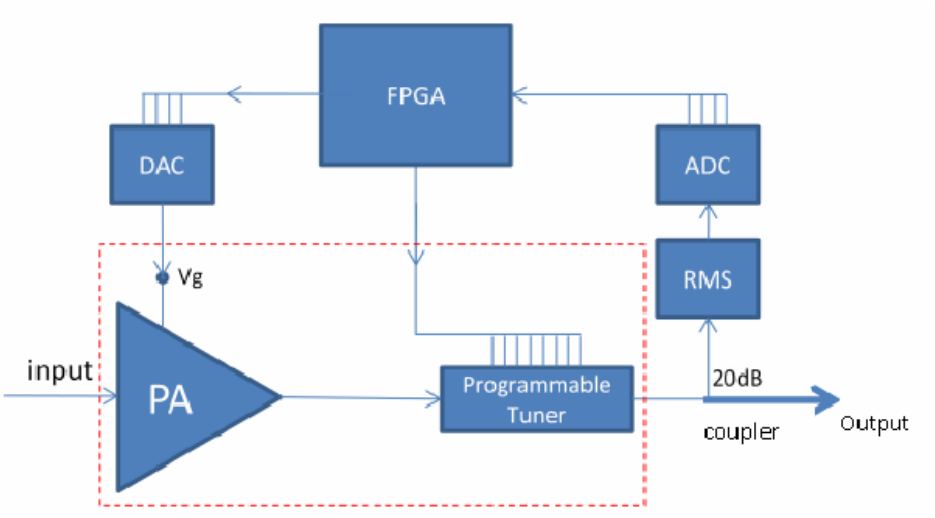


Figure 2.18: Full System Overview.

The proposed structure of the reconfigurable network will consist of switch capacitor elements using MIM capacitors and FET switches, evenly distributed along a co-planar waveguide (CPW) such that there is periodic loading impedance with each bit of switches turned on. Each bit is paired in order that there is symmetry in the design to avoid favoring sides on the CPW, which may launch higher order propagation modes. The conceptual layout is demonstrated in Figure 2.19, where voltages V1-V8 represent gate control voltages received from the FPGA control.

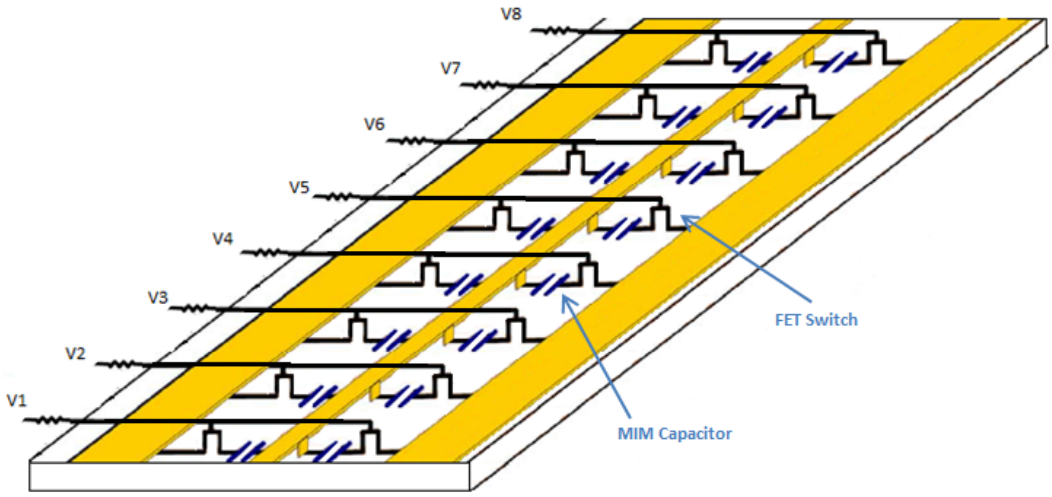


Figure 2.19: General Structure of proposed 8-bit PIT [10].

2.5 PREVIOUS WORK ON RECONFIGURABLE MATCHING NETWORKS

Constructing a reconfigurable matching network based on varactors in CMOS has been reported previously by several authors [14] [15] [16]. However, varactor-based tuners exhibit 1-5dB more loss and have lower tunability range when compared to switched capacitors [10]. Micro electro-mechanical systems (MEMS) have also been employed in high frequency reconfigurable tuners [17] [9] [18]. Their drawback, however, is economical since MEMS requires special integration and packaging techniques, which lead to increased cost per unit [10].

Table 2.1 summarizes a literature study comparing existing PITs reported. As can be seen the switched capacitor designs provide the greatest smith chart coverage, although insufficient information is available to quantify the associated loss penalties of such improved coverage. Programmable impedance networks using HEMT switches in various

configurations have been trialed in [19] [8], but these designs were not intended for high RF power applications.

Table 2.1: Summary of previous PIT designs.

	Technology	Tuner Structure	Impedance Points	Frequency Range	Smith Chart Coverage	*S21* at 10GHz
[14]	.13µm CMOS	Varactors	2^{22}	4-11GHz	10-20%	-5dB to -11dB
[10]	.13µm CMOS	Varactors/ Switched Capacitors	2^{20}	4-11GHz (Var.), 5-16GHz (S.C.)	15-25% (Var), 30-40% (S.C.)	-12dB to -15dB
[17]	MEMs	Switched Capacitors	2^{11}	75-110GHz	40-80%	-7dB
[9]	MEMs	periodic defected-ground Structures	2^{12}	24-60GHz	30-90%	-3.5dB

3.0 DESIGN & CHARACTERIZATION OF A SINGLE STAGE PROGRAMMABLE MATCHING NETWORK

This chapter is devoted to fulfilling the first two thesis objectives, namely the investigation of switch topologies and the development of a single stage of a PIT. First, some design considerations which affect performance, such as losses in NRC-GaN500 FET switches will be presented. This builds on background information presented in chapter 2; including characteristics of a multistage matching network. Then, the performance of various switch topologies will be assessed. Finally, a single stage (1-bit) variable impedance matching block will be design as a proof of concept of this thesis.

3.1 TARGET SPECIFICATIONS FOR A GAN PIT

The key target parameters that are used to assess the performance for a full 8-stage GaN PIT are summarized in Table 3.1. In order to highlight the large power handling capabilities of GaN, output power levels at IP3 should be greater than 40dBm. Next, the total insertion loss must be minimized for the desired 8-12GHz frequency range, but a 1.5dB maximum loss is deemed acceptable for the proposed monolithic PIT implementation. Providing a specification for smith chart coverage can be misleading since a PIT can provide wide matching across the smith chart, yet have low density of impedance points. Hence, it is specified that an 8-stage tuner providing 256 unique impedance should populate an area of the smith chart with $|\Gamma| \leq 0.45$.

Table 3.1: Design Specifications.

Parameter	Specification
Frequency Range	8-12GHz
IP3	> 35dBm
Insertion Loss	< 1.5dB
Smith Chart |Γ| coverage	≤ 0.45
Layout Area	> 2mm x 2mm

3.2 NRC-GAN500 PROCESS FEATURES AND LIMITATIONS

The National Research Center Canada (NRC) offers GaN foundry services, with available High-Electron Mobility Transistors (HEMTs) with 500nm long metal gates, two metal layers for interconnect, 50 Ω/sq Nichrome resistors and MIM capacitors of 0.58fF/μm^2 [20]. It is processed on 3-inch diameter epitaxial layers grown on insulating silicon carbide (SiC) wafers. Semi-insulating SiC is one of the most attractive substrate materials for electronic applications, because of the favorable combination of lattice mismatch, isolation, and thermal conductivity [21].

This process technology is specifically aimed towards design of high powered devices as it can handle drain voltages of up to 40V and deliver 5W/mm of power, albeit with a relatively low f_T and f_{max} of 13GHz and 60GHz respectively. Furthermore, these devices exhibit Breakdown voltages (V_{BKDN}) well beyond 100V, while the maximum V_{DS} it can handle is only 50V. Finally, the gate source voltage can operate between -8V < V_{GS} < 2V, with at least a threshold voltage of -4.6V needed to turn these devices on [21].

There is still work to be done in this process however as it lacks essential components desired for PIT design, such as the lack of varactor models. Moreover, the current version of the design kit only supports a limited number of active device sizes. The most

critical flaw to this version of the design kit lies within its FET models; they lack common-gate (CG) configured models, which are vital at revealing switch operation capabilities of these FETs.

3.3 GAN FET SWITCH CHARACTERIZATION

3.3.1 DC CHARACTERIZATION AND GATE BIASING

As described in Section 2.7, active devices will be utilized in the proposed switched- capacitor. It can be seen from Figure 3.1 that GaN FETs require reverse gate bias down to -5V to fully turn off. The reverse gate leakage is reported to be 10 µA/mm when biased at V_{GS}=-6V [20]. Throughout design and measurements, voltages of 2V and -7.5V are chosen for switching FETs between ON and OFF states respectively. In addition, the device exhibits a linear and ohmic relationship around 29-38Ω (obtained from the slope of the DC I-V curves) when gate bias voltages exceed 0.5V.

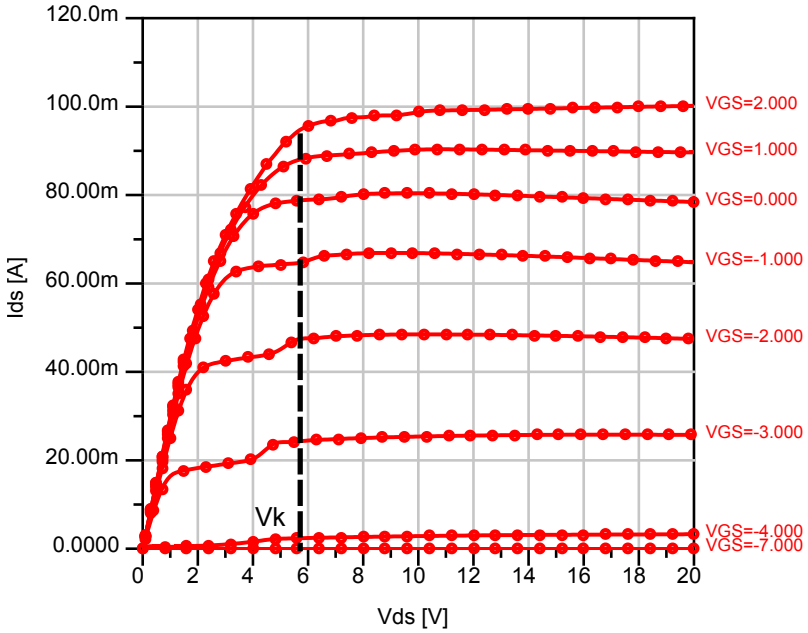


Figure 3.1: I-V Curves for a 4x25µm GaN500 FET.

When the impedance matching network is connected to a GaN HPA during large signal operation, the output RF signal from the PA will go through a coupling capacitor, thus the operating voltage at the input of the designed tuner is expected to swing around 0V, as illustrated in Figure 3.2.

However, if a large negative excursion of the signal is present at the input, then the gate-to-source voltage of the shunt FETs present in the PIT may become larger than its threshold voltage (V_{th}), causing the transistor to conduct and will result in RF signal clipping. Hence, there will be a maximum voltage swing allowed along the RF line to ensure proper FET switch operation is maintained.

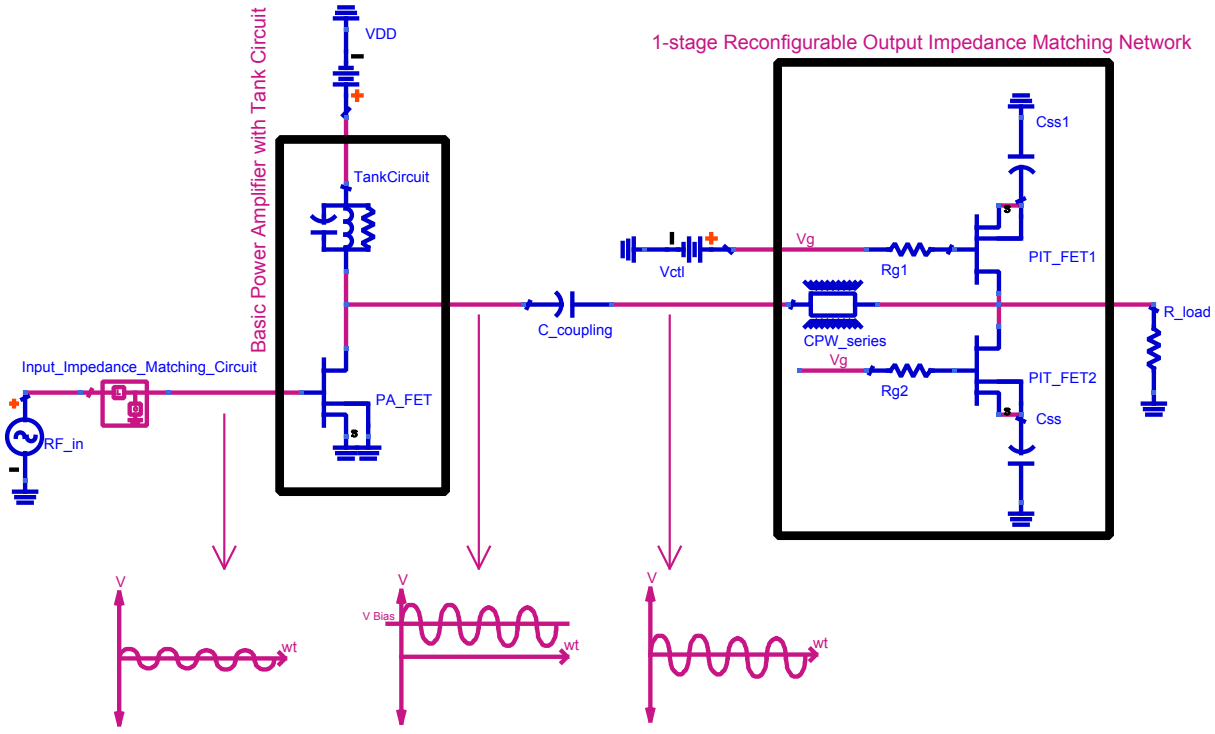


Figure 3.2: RF signal at different stages in an impedance-matched PA.

3.3.2 DEVICE PARASITICS AND EQUIVALENT SWITCH MODEL

Understanding the intrinsic properties of the FET switch is crucial. Not only do parasitics directly affect isolation and IL properties of the switch, but also add shunt impedance to the PIT. As mentioned in Section 2.3.2, the lumped element switch model can be simplified to an equivalent OFF state capacitance, and some variable drain-source resistance. In the OFF state, a FET switch can be represented as shown in Figure 3.3, where r_d is ideally infinitely large.

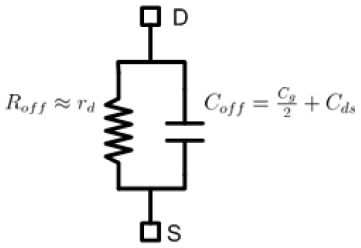


Figure 3.3: Equivalent circuit model of a FET switch in the off state [11].

For a 100µm wide NRC-GaN500 FET with 4 fingers, the total off-state parasitic capacitance can be estimated as follows [20]:

$$C_{ds} = 18.8fF, C_{gd} = 7.4fF, C_{gs} = 128fF$$

$$C_g = \frac{1}{\frac{1}{C_{gd}} + \frac{1}{C_{gs}}} = 7fF \quad (3.1)$$

$$C_{off} = C_{ds} + \frac{C_g}{2} = 22.3fF \quad (3.2)$$

The bias conditions used to obtain the provided linear model are not explicitly specified. In order to validate these values and obtain values corresponding to the desired drain and gate bias conditions, an equivalent switch model shown in Figure 3.4 is extracted

from the FET models provided in the DK. This is carried out by plotting the drain input impedance Z_{in} of the desired device using the 1-port test bench in Figure 3.5.

It is important to highlight that the simulated drain Z_{in} of the device represents the total gate-drain, gate-source and drain-source impedance of the device as viewed from the input of the drain. Initial values for model elements were obtained from linear model parameters in [20], with further tuning carried out for R_{DS} and C_{DS} to curve fit to original device FET Z_{in}, as shown in Figure 3.6. It is important to note that the effective R_{DS} (i.e. the real part of Z_{in}) changes from a larger value in the OFF state to a lower value in the ON state.

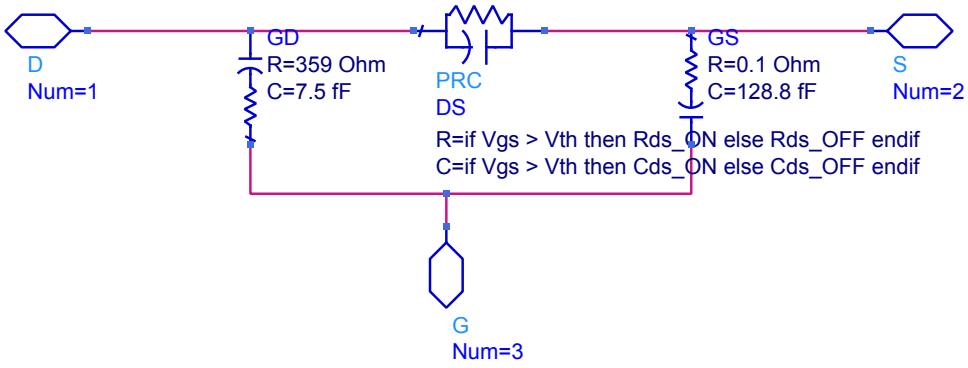


Figure 3.4: Equivalent Intrinsic linear model of a 100um FET.

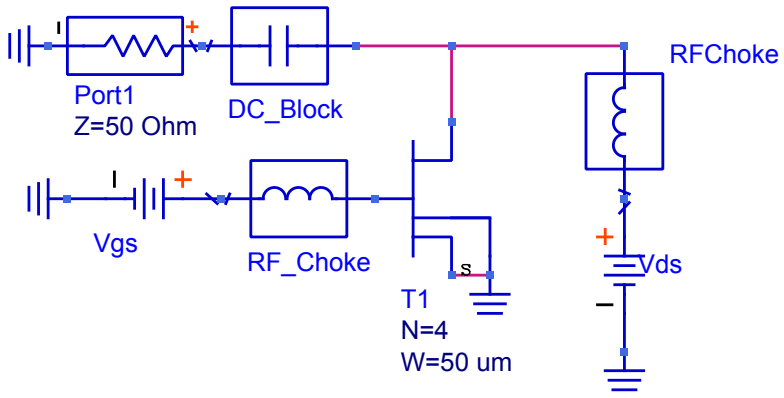
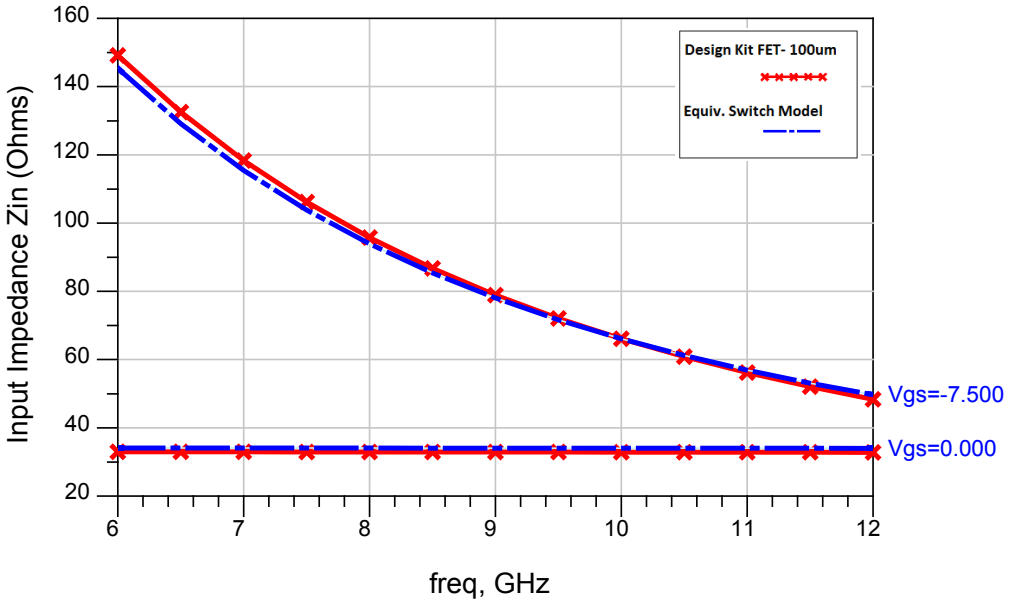
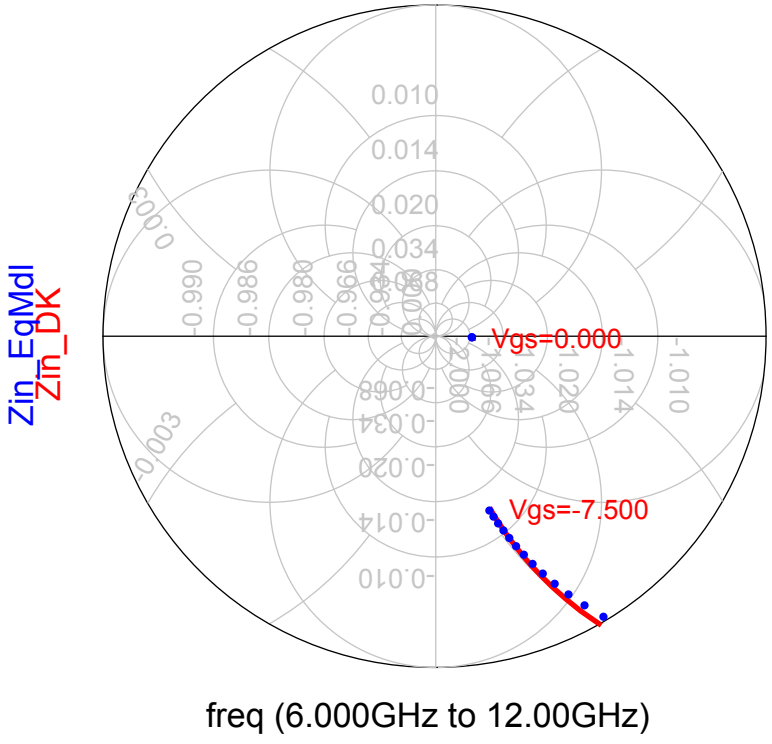


Figure 3.5 : 1-port s-parameter Testbench.



(a)



(b)

Figure 3.6: Frequency response of a GaN device and equivalent circuit model at V_{DS} = 0.1V (a) Drain input resistance; (b) Smith chart representation of Drain input impedance Z_{in}.

Figure 3.7 and Figure 3.8 reveal the changes in drain-source parasitics within the FET switch for different values of V_{DS}. This is particularly useful to demonstrate the variations in impedance loading during large signal voltage swing. While the validity of the foundry supplied model remains to be verified, it is clear that R_{DS} switches between low and high values in the ON and OFF states, respectively. The parasitic (effective C_{DS}) is seen to vary in the 50fF to 75fF range, which may lead to non-linear behavior of the switch operation.

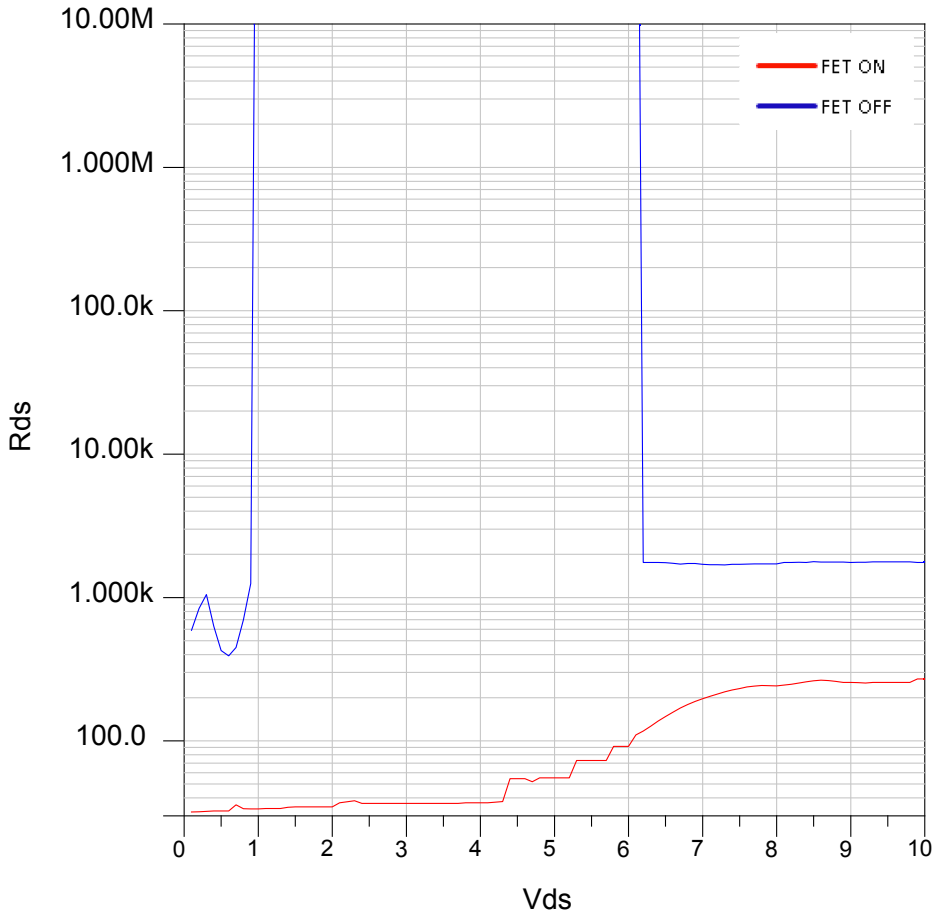


Figure 3.7: Simulated R_{DS} values vs. V_{DS} for a 100µm- wide GaN500 FET at 10GHz.

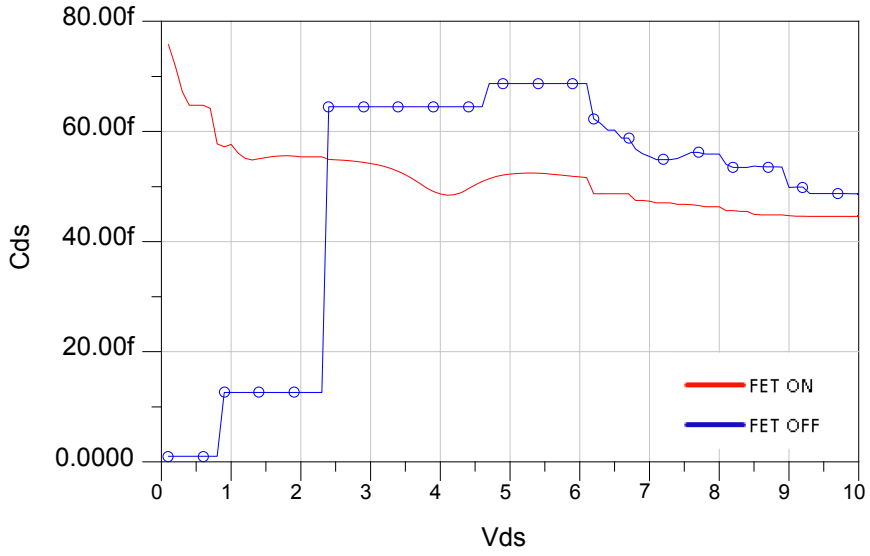


Figure 3.8: Simulated C_{DS} values vs. V_{DS} for a 100µm- wide GaN500 FET at 10GHz.

3.3.3 INSERTION LOSS AND ISOLATION

Referring to section 2.5, insertion loss and isolation of a switch can be simulated in a 2-port system by observing the return loss (S_{21}) between the drain and source. When switch FETs are OFF, isolation properties are expected to substantially deteriorate with increasing device size due to increasing C_{OFF}. In contrast, insertion loss should be independent of device size since R_{DS} dominates.

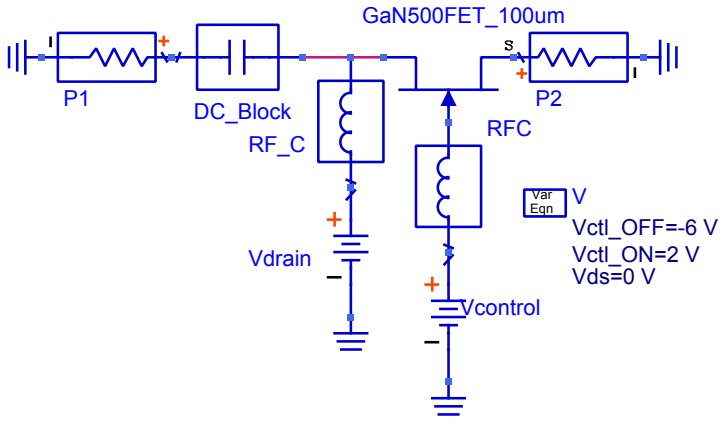


Figure 3.9: 2-port S-parameter test bench for measuring IL and isolation of a single series FET.

This is verified using the intrinsic linear model extracted in section 3.2. The linear model is scaled corresponding to various device widths available in the design kit. FET gates are biased such that the return loss (S_{21}) is simulated in the ON and OFF states between 8-12GHz, while V_{DS} is set to 0V. Figure 3.10 and Figure 3.11 demonstrate that as total device width (W_{TOT}) is increased, ON-state insertion loss performance improves while OFF-state isolation deteriorates.

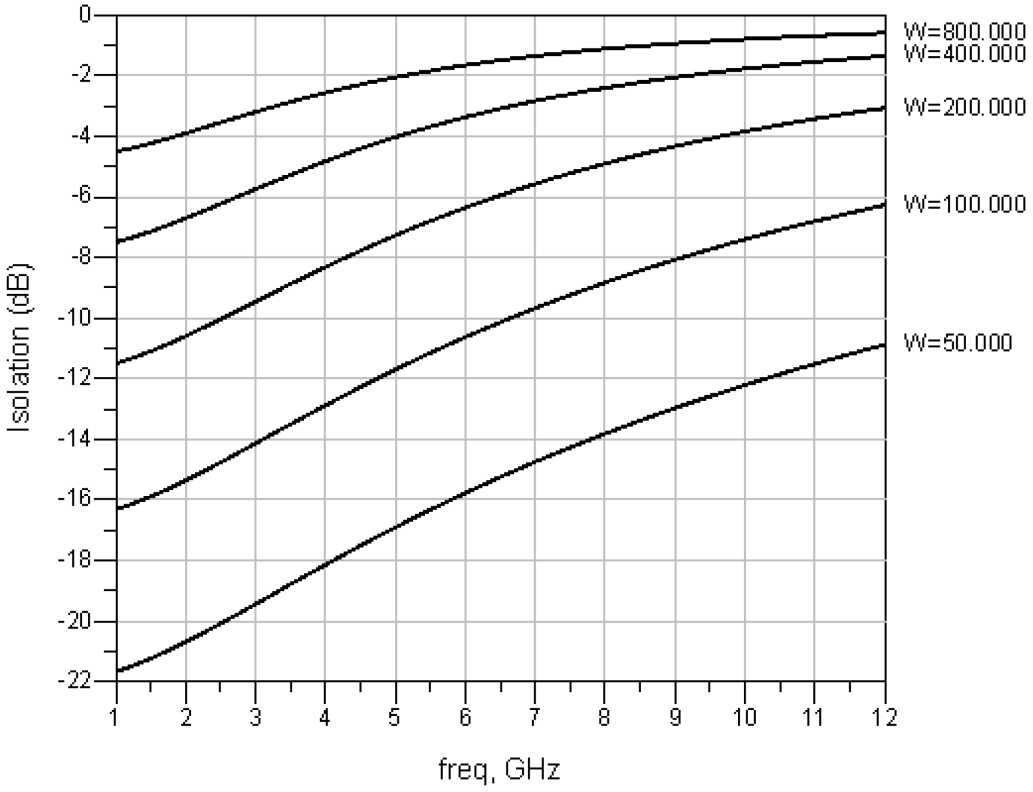


Figure 3.10: Simulated drain-source isolation (S_{21}) for various GaN pHEMT widths (FET-OFF).

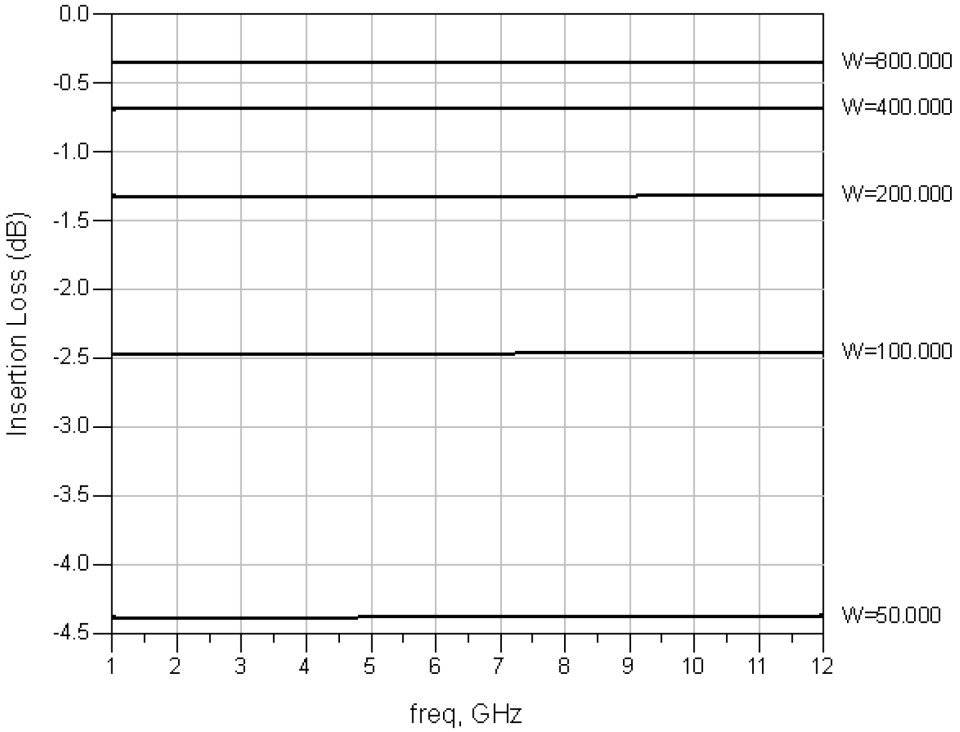


Figure 3.11: Simulated drain-source insertion loss (S_{21}) for various GaN pHEMT widths (FET-ON)

For a more compact layout and as a compromise between ON and OFF state performances, 4x25µm transistors were chosen as a base size for switches in schematic simulations.

3.4 SWITCH TOPOLOGY CONSIDERATIONS

There are various switch topologies which can be applied to reduce losses and improve isolation, such as an absorptive T type configuration shown in Figure 3.12. These implementations involve using series-shunt FET switch arrangements such that when in the off state, high isolation shunt FETs are turned on, while a low IL series FET is alternatively turned on. Another topology is the reflective π-type switch illustrated in Figure 3.13, which also utilizes series-shunt FETs, supplemented by using resistors in parallel.

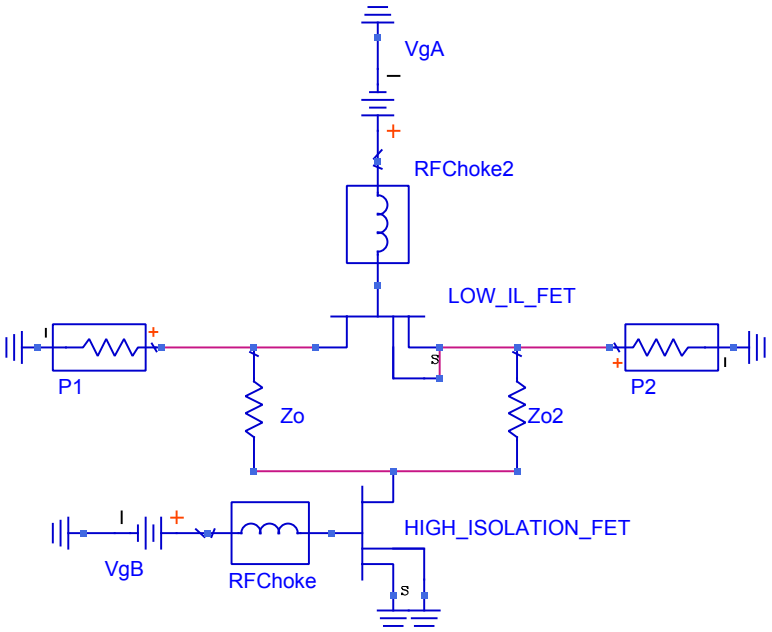


Figure 3.12 : T- type absorptive switch employing GaN FETs.

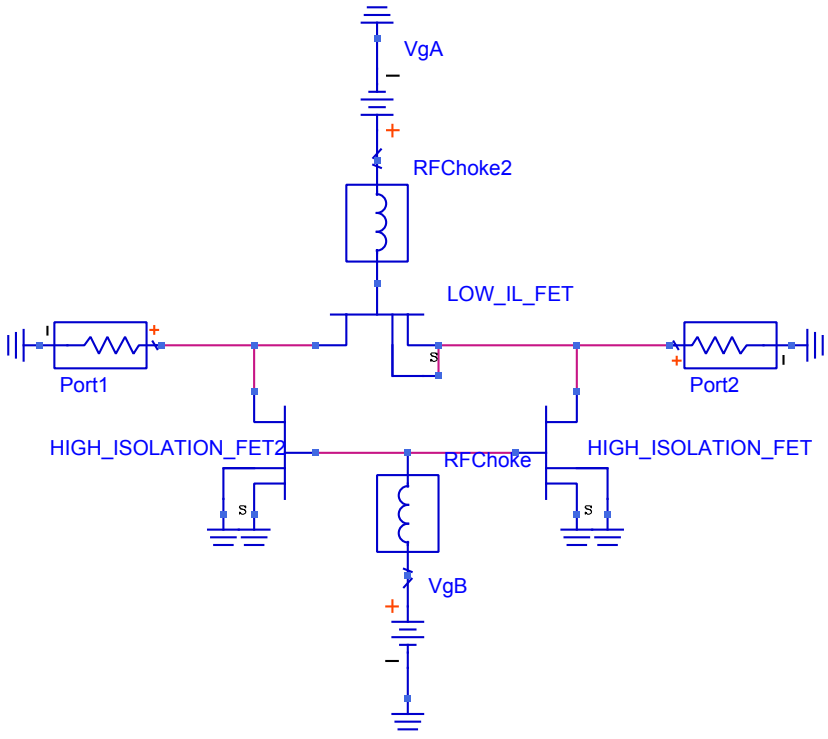


Figure 3.13: ∏-type reflective switch employing GaN FETs.

Using only 200µm wide FETs, the isolation and IL performance is simulated for these topologies and compared to a single series FET switch. Figure 3.14 and Figure 3.15 reveal that a ∏-type reflective switch will offers the best isolation properties and the worst insertion loss, while a single series switch will offer poor isolation and very good isolation. However, these configurations add complexity to the design, take up significant area and will be difficult to implement in an 8-stage network. Thus, for proof of concept, only a single series switch is used in the design.

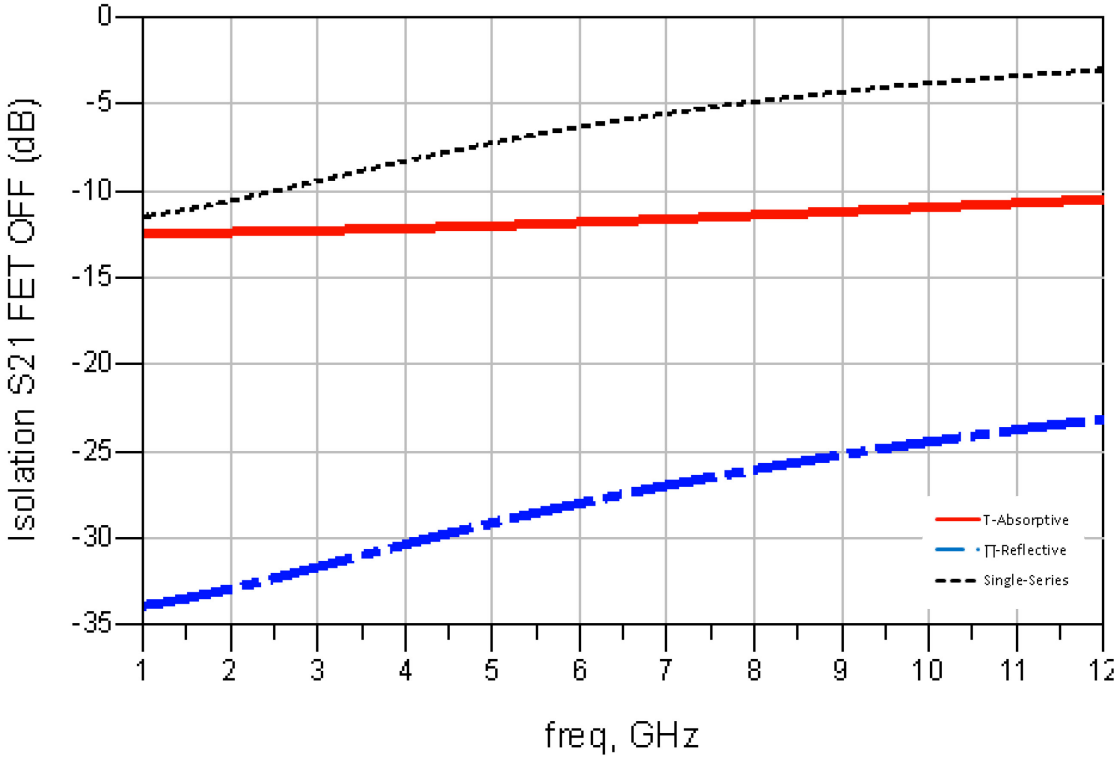


Figure 3.14: Isolation performance comparison.

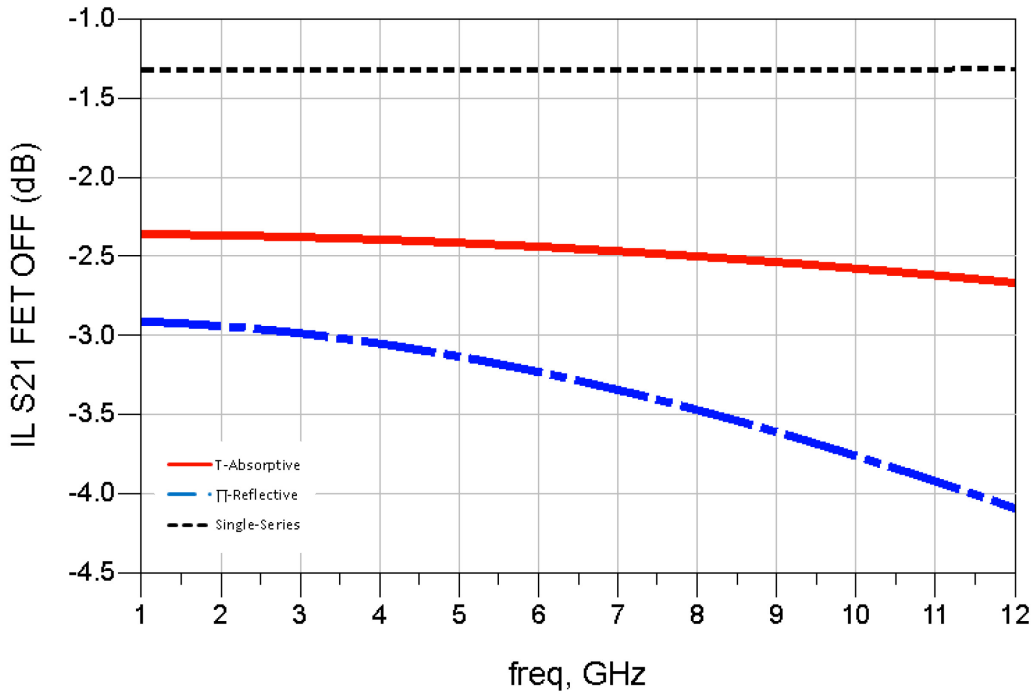


Figure 3.15: Insertion loss performance comparison.

3.5 LOADING CAPACITORS

Obtaining maximum impedance matching coverage from the PIT is highly dependent on the total shunt capacitance (C_{SHUNT}) that is loaded along the RF line. When the switch is turned on, the line is loaded with:

$$C_{SHUNT} = \left[\left(C_{DS} + {}^{C_g}/_{2}\right)^{-1} + {C_{SS}}^{-1}\right]^{-1} \tag{3.3}$$

Where C_{DS} and C_g are the drain source and gate capacitances of the FET respectively, and C_{ss} is the added loading capacitance in series with the FET switch. It can be deduced from equation 3.3 above that the maximum total shunt capacitance ($C_{SHUNT\,(MAX)}$) is limited by the device parasitic capacitance. Using a 100µm FET switch model, an optimum value for C_{ss} can be revealed using the test bench shown in Figure 3.16. A maximum

$C_{SHUNT\ (MAX)}$ of 242.8fF is achieved in the on state by adding 501.2fF in series with the FET, as shown in Figure 3.17.

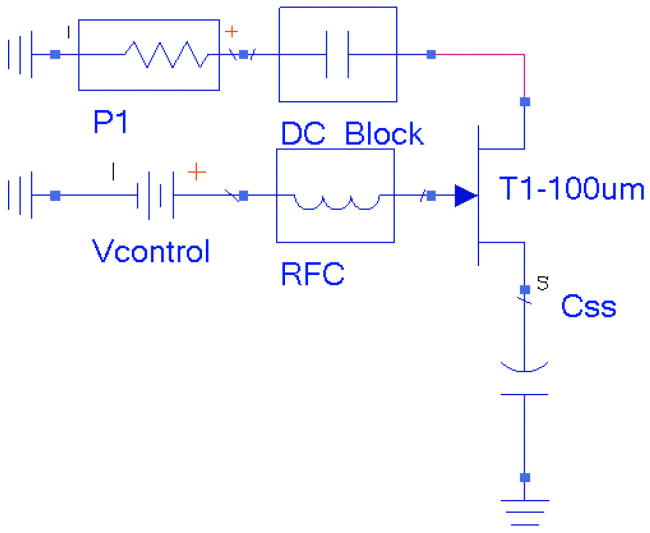


Figure 3.16: 1-port test bench used for calculating the ideal loading capacitance.

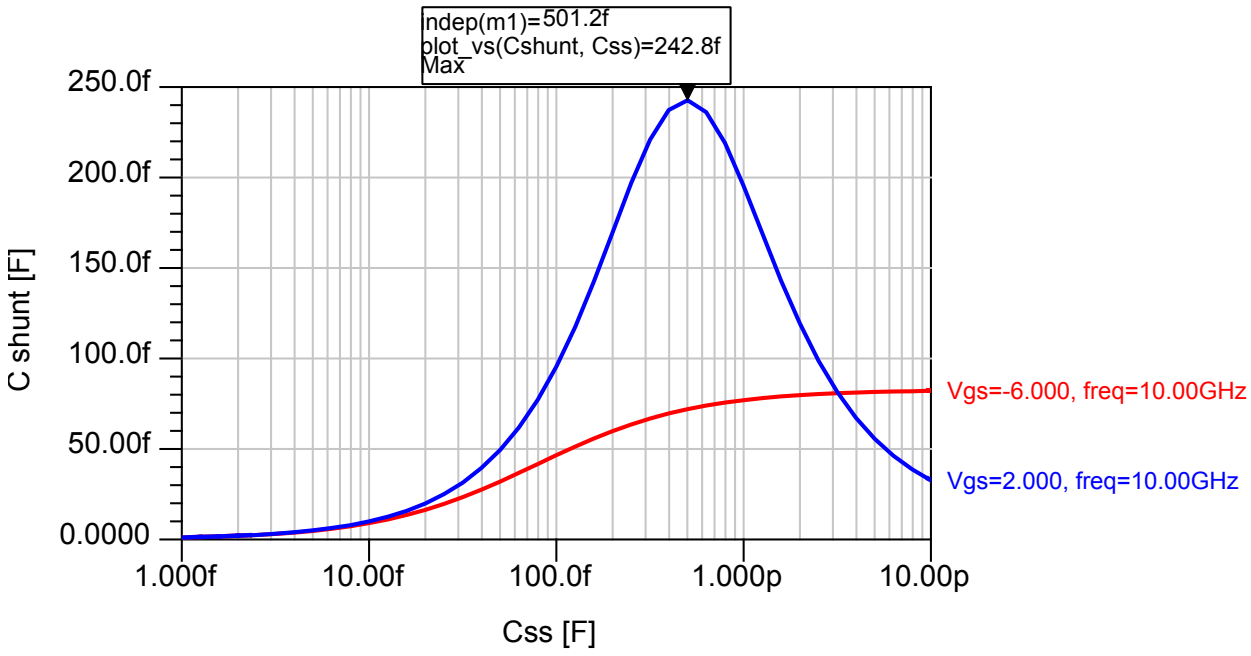


Figure 3.17: C_{SHUNT} as a function of C_{ss}.

In figure 2.19, it was established that for each stage in the PIT contains a pair of shunt switched capacitor branches. Thus, $C_{SHUNT\ (MAX)}$ for a single stage will be twice as large for the same C_{ss} on each branch.

To further understand the effect of adding shunt capacitance on smith chart impedance coverage, a simplified 1-stage PIT is built as shown in Figure 3.18 using MIM capacitors from the GaN design kit. The length of the CPW RF line is swept to create VSWR circles while MIM capacitor area is swept simultaneously to show matching range for different capacitor sizes when the switch is ON. It can be seen from Figure 3.19 that added capacitance area improves matching range up to an SWR=9, at which point adding further capacitance offers diminishing improvement. Hence, MIM capacitor area per switch/capacitor was chosen to be 20µmx20µm, which is equivalent to 241fF.

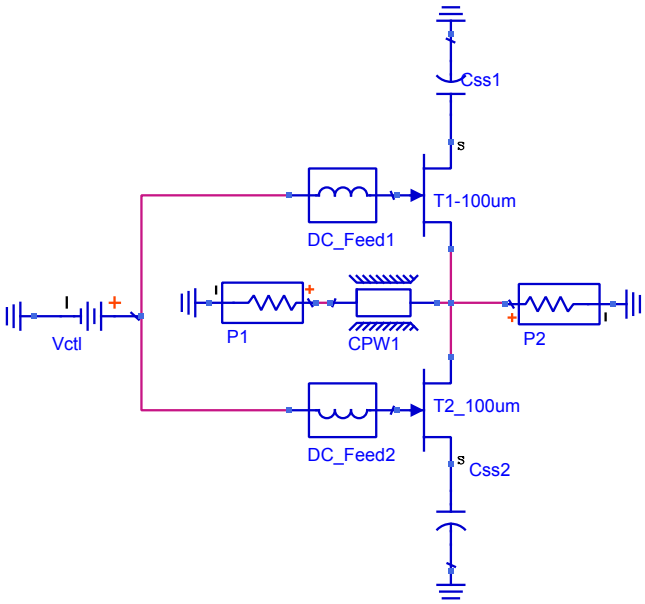


Figure 3.18: 1-stage PIT used for characterizing C_{ss}.

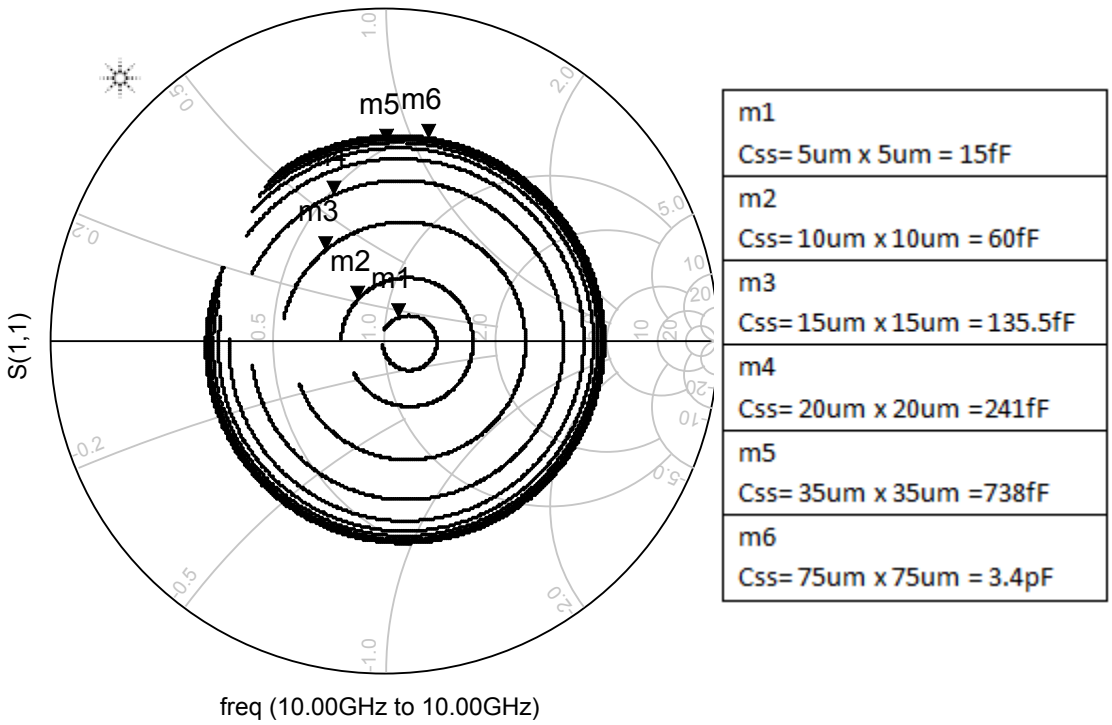


Figure 3.19: Maximum matching range of a 1-stage PIT vs. C_{ss}.

The placement of C_{ss} at either the drain or source of the FET switch should have no effect on matching range of the PIT. With layout area budgeting in mind, C_{ss} is kept between the source terminal to ground.

3.6 GATE RESISTORS

For the purpose of eliminating any possible drain- gate leakage current or loss, the gate terminal of the FET switch is fitted with a large resistor. By replacing the ideal gate RF choke in Figure 3.16 with a resistor, the optimum value can be found by sweeping against the drain input impedance Z_{in}. As simulated in Figure 3.20, the OFF-state switch Z_{in} will improve slightly for $R_g \geq 150\Omega$. For the final design, each FET gate is equipped with a 1.5kΩ nichrome resistor.

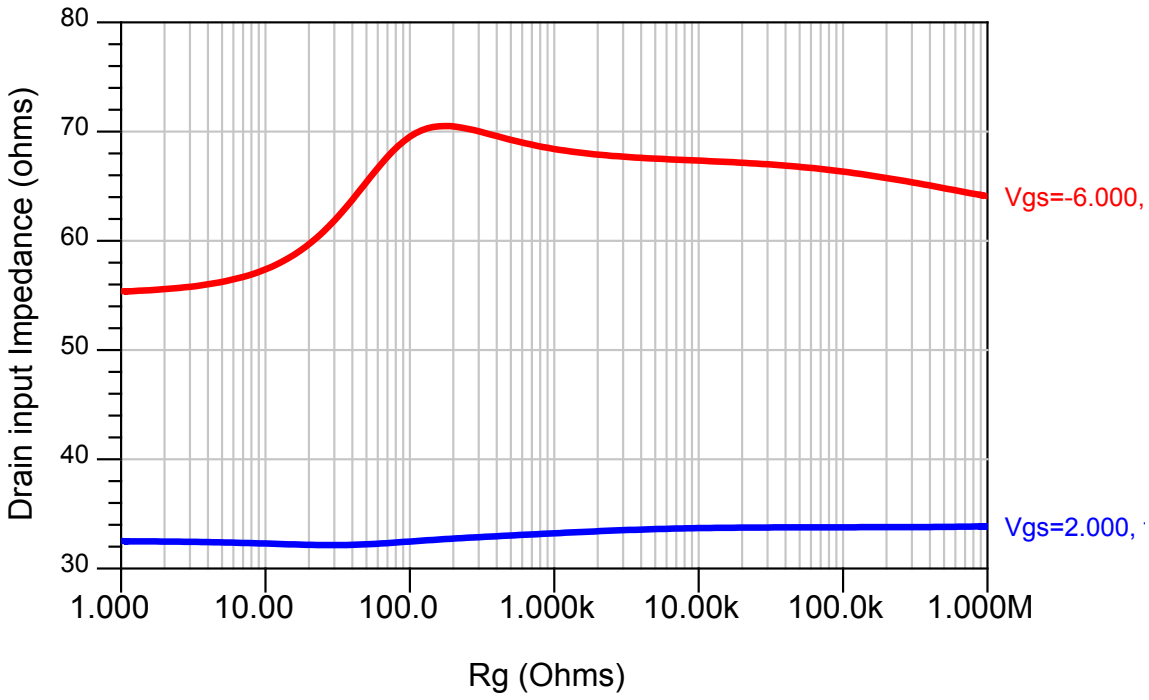


Figure 3.20: FET switch drain Z_{in} as a function of gate resistance R_g.

3.7 COPLANAR WAVEGUIDES FOR TRANSMISSION LINES

Since there are no through-substrate vias in the GaN 500 process, coplanar waveguides (CPW) are used instead of microstrip lines. Another advantage of CPW is the shielding provided by the ground planes. A 100µm long-kit CPW is simulated while characteristic impedance (Z_o) and attenuation loss in line (α) are calculated using ABCD parameters.

Z_o of the CPW is dictated by the width (W) of the line and the gap (G) between the line and ground planes, and can be related to be inversely proportional to W and directly proportional to G. Conversely, α is directly proportional to W and inversely proportional to G. Hence, an optimum width-gap value can be determined to obtain the lowest possible attenuation for Z_o of 50Ω. Table 3.2 exposes the optimal dimensions discovered

using the optimization tool in ADS for single metal and stacked metal layers available in GaN.

Table 3.2: Optimal dimensions for CPW in Figure 3.21 at 10GHz.

CPW Layer	1ME	2ME	1ME+2ME
G [µm]	39.5	39.5	45
W [µm]	94	94	60.5
Z_o [Ω]	50	50	50
α [dB/mm]	0.857	0.857	0.849

The maximum current carrying capacity for single-metal layer interconnects is 6mA/um width versus 12mA/um for a stacked metal interconnects [20, p. 21]. Thus, for 50Ω characteristic impedance, single metal interconnects can carry current up to 564mA versus 1.164A using stacked metal. Layouts of single and stacked metal CPWs incorporating optimized dimensions are constructed in ADS as shown in Figure 3.21.

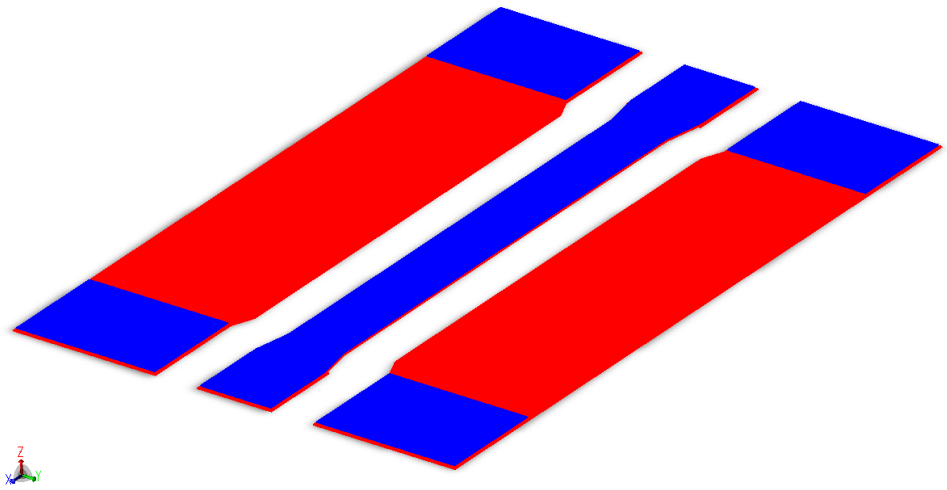


Figure 3.21: 3D layout view of a stacked-metal CPW with Z_o=50Ω and optimized for low attenuation.

Ground-signal-ground (GSG) probe pads are taken into consideration as they can add unwanted series capacitance on the line. Also, it is important to insure that ground planes have equipotential at any point along the CPW. Consequently, the use of air bridges spanning over the signal line will be accounted for. When loading the CPW section with a shunt switched capacitor, discontinuities will arise which will affect its transmission properties. To address this, tapered sections are added on each side of the line section, mirrored about the center x-axis of the line. An area of clearance is created on either side of the ground plane to allow for switch and capacitor Placement. EM Simulations are conducted on the resulting CPW layout in Figure 3.22 using Agilent Momentum 3D. Results in Figure 3.23 reveal 0.05-0.06dB in losses for this section. The short length of the PIT CPW may also explain the low losses exhibited by this structure.

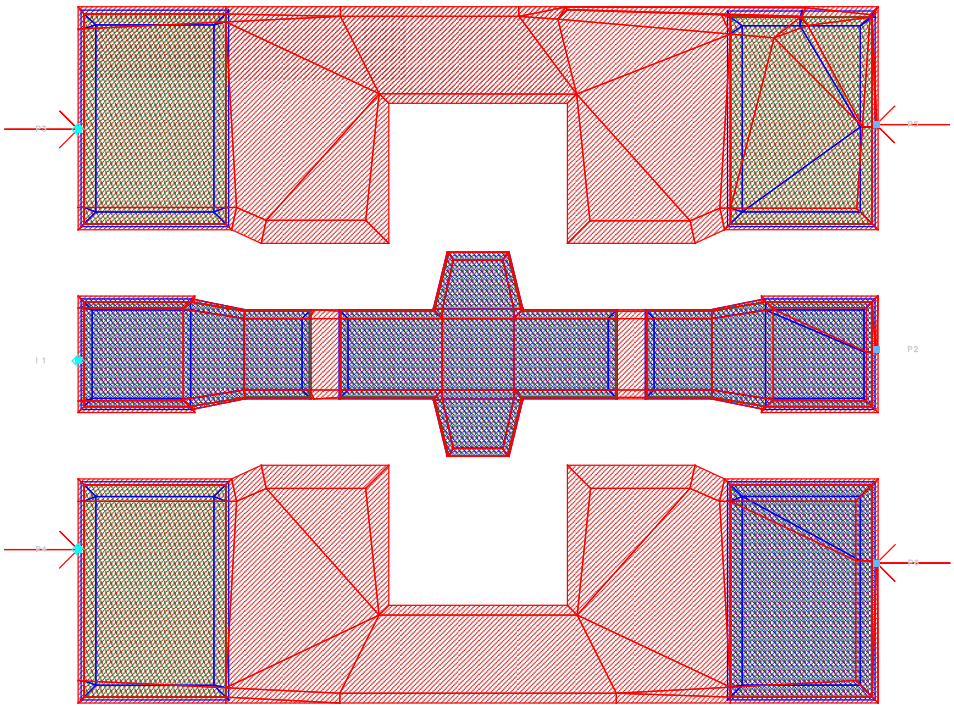


Figure 3.22: EM momentum simulation of constructed CPW structure.

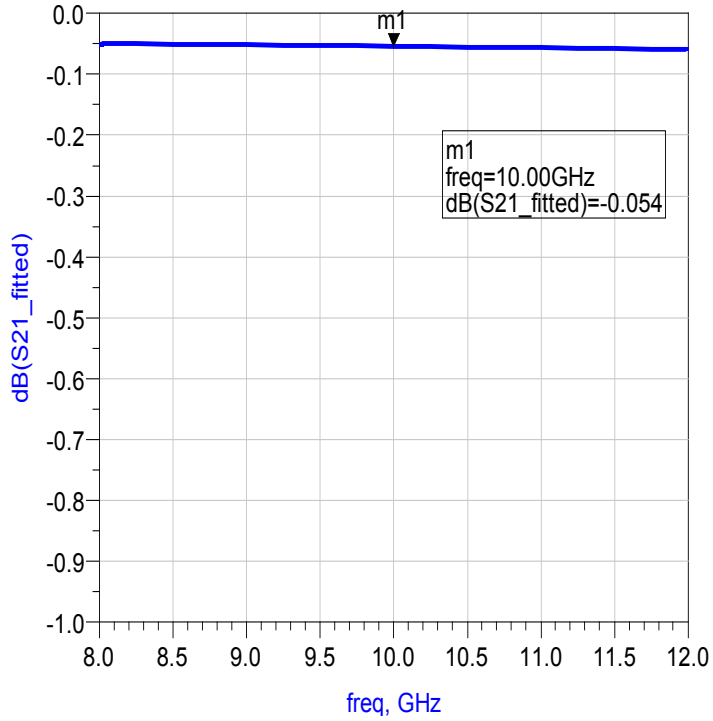


Figure 3.23: Simulated transmission coefficient for designed CPW in the X-band frequency range.

3.8 LAYOUT OF A SINGLE- STAGE PIT

After characterizing all components needed to provide tunable PA load impedance using simulated design kit components, an equivalent design layout is constructed as shown in Figure 3.24. To maintain equipotential of ground plains, airbridges are added on either side of the shunt switched capacitor section, with a slotted RF CPW line used to accommodate the Metal2 airbridge. Tapers are added along the shunt section to reduce discontinuity effects due to differences between the FET drain width and the CPW line width. Nichrome resistors are connected to the device gate control via minimum width (5µm) transmission line to reduce unwanted parasitic capacitances at the gate. Finally, MIM capacitors are divided between the devices' source terminals to ground.

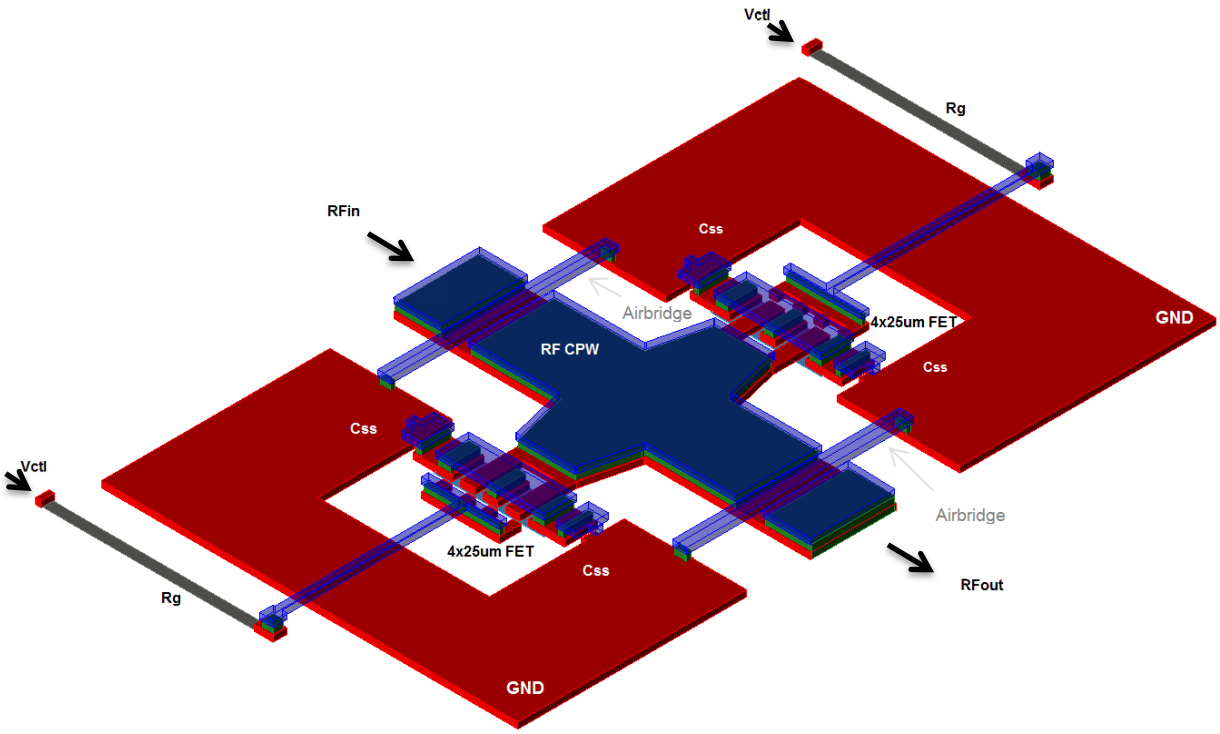


Figure 3.24: layout for a single-stage PIT employing a stacked metal CPW.

The layout was stripped of any active devices and an EM Momentum simulation is carried out for the structure. The resulting S-parameters are then used to co-simulate using the device model. The resulting change in return loss along the CPW is shown in Figure 3.25. When the device FET model is OFF, losses are very close to the Momentum results of the CPW structure in Figure 3.23. This confirms that the devices are exhibiting high isolation and there is low leakage in the OFF state.

The change in impedance matching point for the single stage PIT between the ON and OFF states can be seen in Figure 3.26, which indicates the matching capabilities of a single stage PIT over the X-band frequency range.

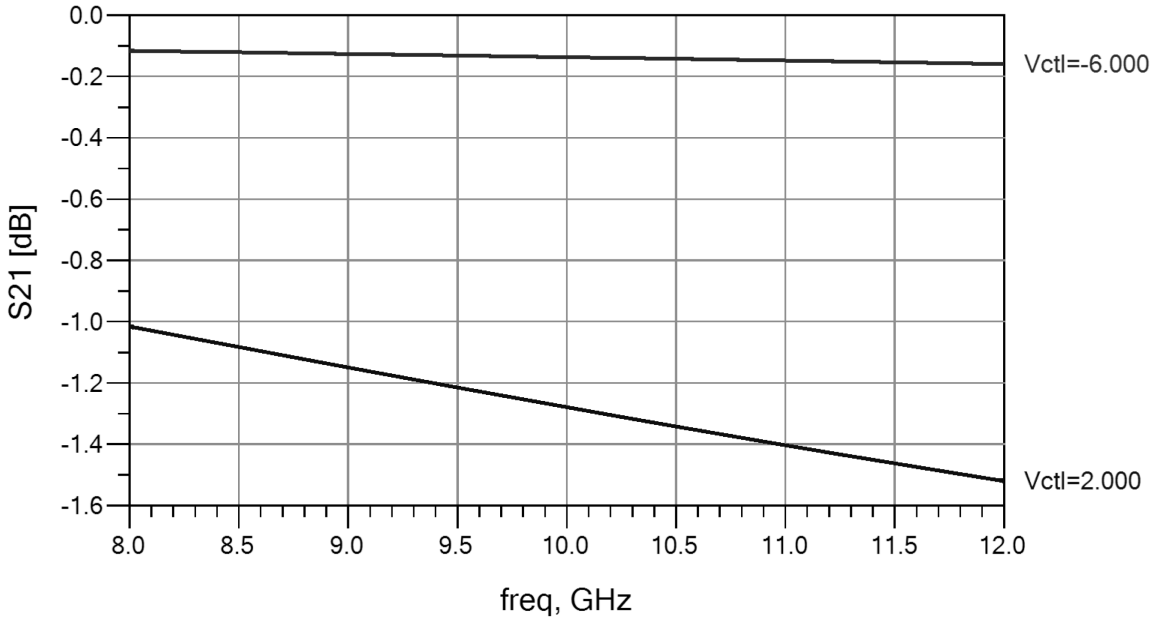


Figure 3.25: Co-simulated S21 for designed 1-stage PIT in the X-band frequency range.

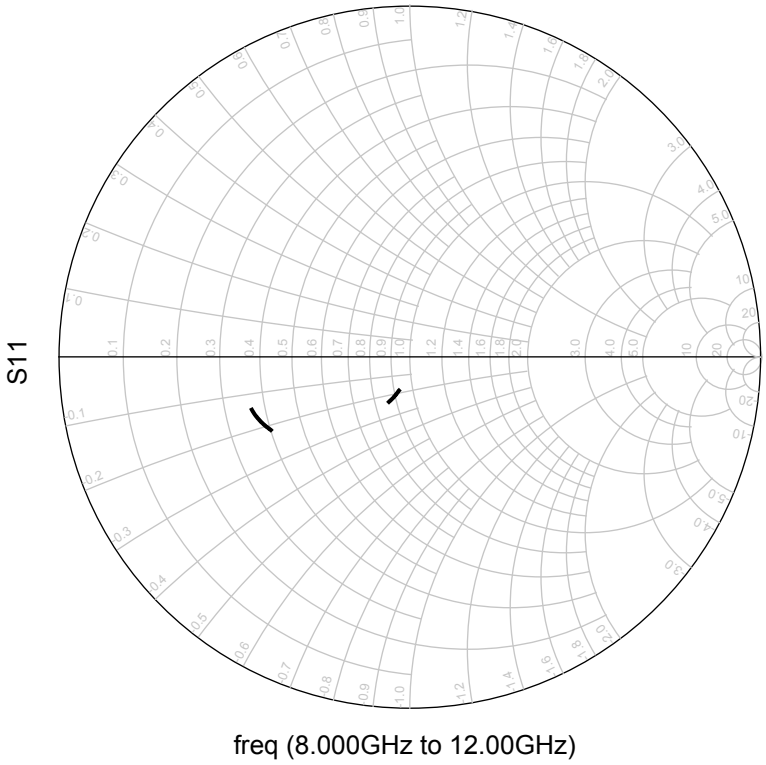


Figure 3.26: Co-simulated impedance matching coverage of PIT between the ON and OFF states.

3.9 CHAPTER CONCLUSION

This chapter presented the design of a single stage PIT section. FET switch characterization was carried out, and comparisons between T-reflective, ∏-absorptive and single series switch topologies were performed. Loading capacitor and gate resistor sizes were characterized. Co-planar waveguide sections were optimized to provide the lowest attenuation behavior. Schematic and layouts for a single stage PIT section was constructed and simulated using characterized components.

The outcome is a circuit sub-block, which provides substantial impedance changes between the two different states, serving as the basis for a full multi-stage PIT integrated on a GaN power amplifier chip. This sub-block was fabricated and its measured performance is presented in the following chapter.

4.0 MEASUREMENT RESULTS AND PERFORMANCE ANALYSIS

The proposed 1-bit PIT was fabricated in the NRC GaN500 process through the Canadian microelectronics corporation (CMC). This chapter presents the measured performance of the prototype PIT stage, also referred to as "IGNCUAEA", along with its testing methods.

In section 4.1, test structures on-board IGNCUAEA and their desired functionality are discussed, followed by a review of the applied de-embedding strategy in section 4.2. The measurement setup used to extract small signal performance metrics for the CG configured device and PIT structures is then introduced in section 4.3. Section 4.4 will present the small signal results obtained. Furthermore, techniques for measuring linearity and extrapolating for IP3 points are covered in section 4.5. Finally, the chapter concludes with a summary of all measurement results in section 4.6.

4.1 CHIP LAYOUT OVERVIEW

It is important to validate the integrity of the device models used. Consequently, the IGNCUAEA chip shown in Figure 4.1 was designed on a 2mm x 2mm die area. The purpose of this chip is to:

1. Verify common-source (CS) models for various FET device sizes;

2. Obtain a common-gate (CG) model for a 50µm-wide FET, which can be scaled and compared to the corresponding CS device models of different device sizes;
3. Study IL and isolation properties of devices from CG model up to 12GHz;
4. Determine the optimum ON and OFF state $V_{CONTROL}$ of switch FETs for best IL and isolation performance;
5. Investigate the losses through single stage PITs with different current carrying capabilities (different CPW metal layer compositions);
6. Extract equivalent lumped element model and ABCD parameters of the PIT;
7. Examine impedance matching points provided in ON and OFF states;
8. Estimate the linearity of designed PIT.

To satisfy these tasks, IGNCUAEA was populated with several test structures, as shown in Figure 4.2.

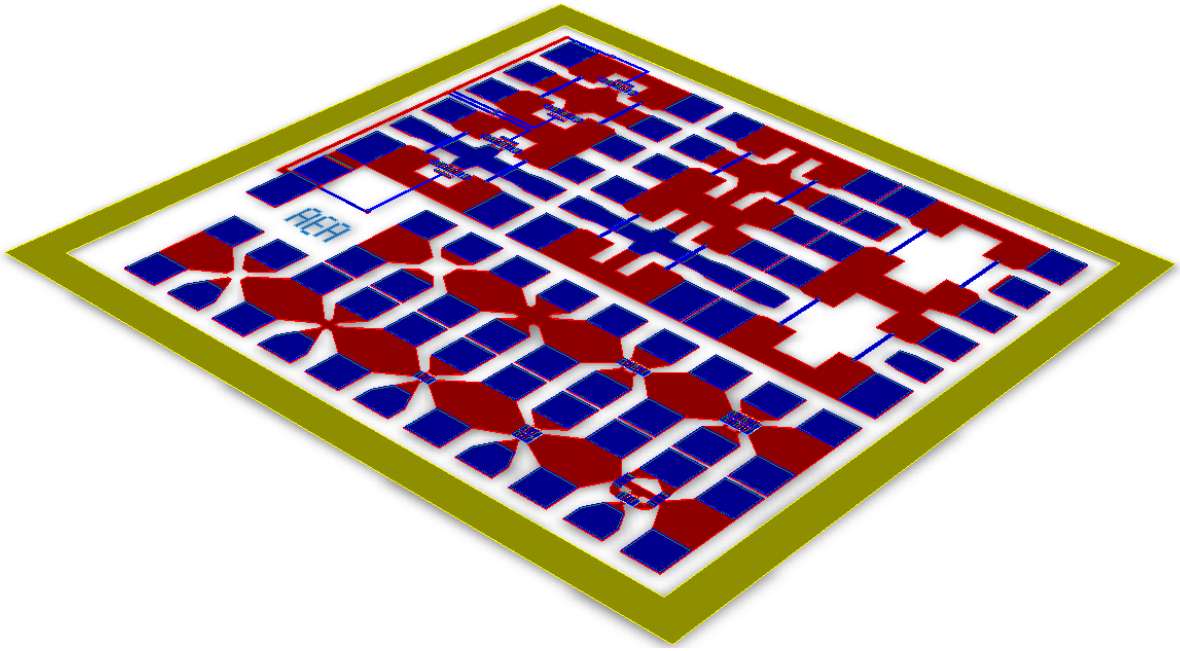


Figure 4.1: Full IGNCUAEA GaN chip layout (2mm x 2mm).

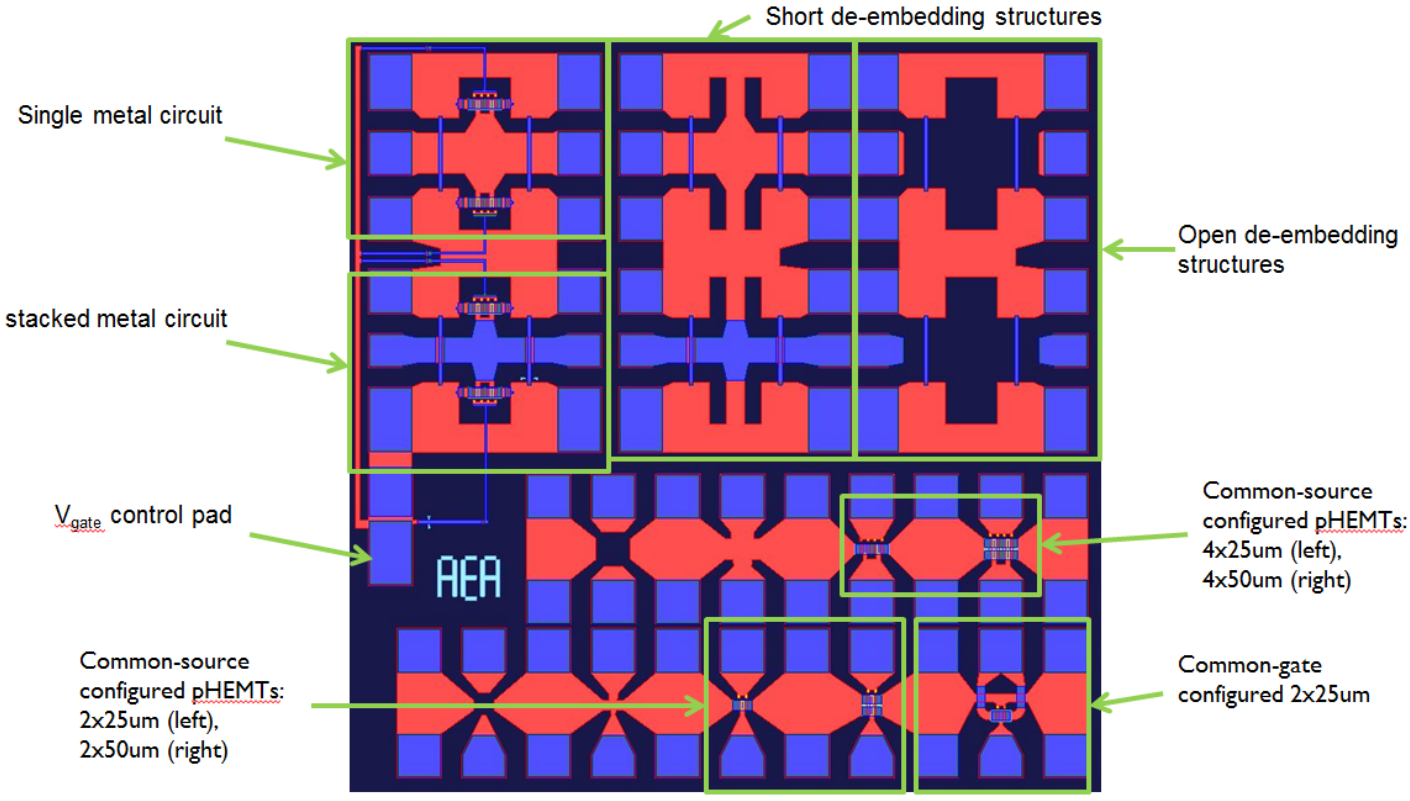


Figure 4.2: TOP view of IGNCUAEA chip.

4.2 PROBE PAD STRUCTURE AND DE-EMBEDDING STRATEGY

Ground-signal-ground probes landing pads are constructed in order to access on-wafer RF signal lines within the chip. There exist 14 pairs of GSG pads and a single-pin DC probe landing pad. All RF probe pads are designed to land 150µm ground GSG probes, as shown in Figure 4.3. The DC probe pad is 142.5µmx104µm as illustrated in Figure 4.4.

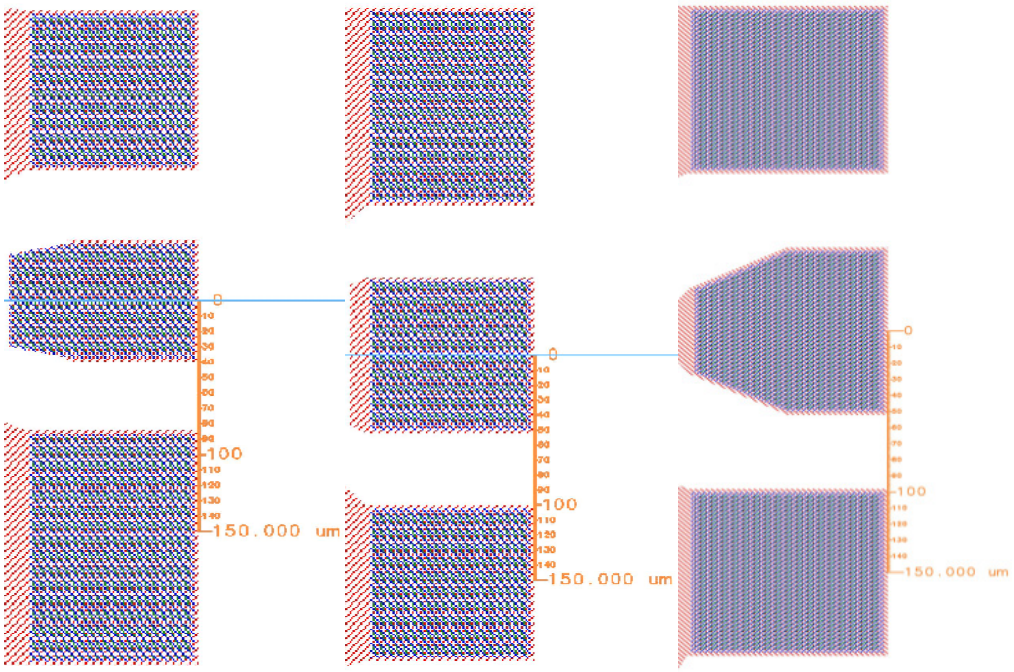


Figure 4.3: GSG pad structures on- board IGNCUAEA chip.

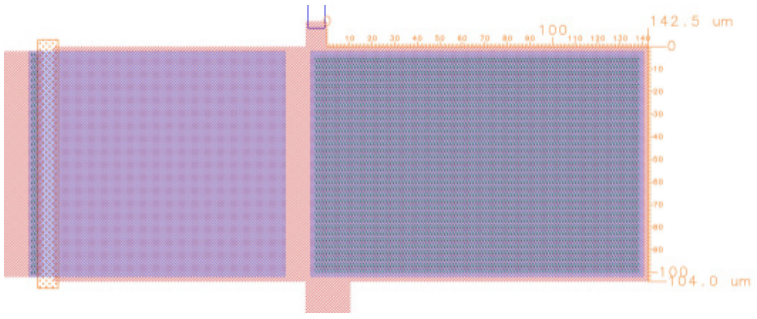


Figure 4.4: DC probe pad structure.

When using probes to access the desired structures on-board, the designed chip can exhibit undesirable reactive loading effects which may alter the measured values. Thus, de-embedding structures are necessary in order to ensure accurate measurements by negating the effects of landing pads or connectors.

The two-step de-embedding method described in [22] is employed, which utilizes 3 measurements for extracting DUT measurements: (a) Pad only, (b) Short, and (c) Pad with DUT. For each GSG pad, the process of de-embedding is carried out as follows:

1. A standard calibration substrate is used to calibrate the VNA down to the tips of the GSG probes.
2. Using a 2- port setup, each GSG probe pad pair is measured on the open de-embedding structures to obtain measurement [S_{PAD}]
3. Similarly, [S_{SHORT}] is measured from the short de-embedding structures and [S_{TOTAL}] can be measured from the DUT + Pad structures.
4. S-parameters are converted to Y-parameters to obtain [Y_{PAD}], [Y_{SHORT}] and [Y_{TOTAL}]
5. Mathematical extraction of DUT parameters is carried out as follows:

$$Y_{DUT} = [([Y_{TOTAL}] - [Y_{PAD}])^{-1} - ([Y_{SHORT}] - [Y_{PAD}])^{-1}]^{-1}$$

4.3 SMALL- SIGNAL MEASUREMENTS

4.3.1 SETUP AND PERFORMANCE METRICS

Small signal S-parameter (SP) measurements will be utilized to achieve goals 1-7 of section 4.1. A Vector Network Analyzer (VNA) equipped with two Ground-Signal-Ground (GSG) probes with 150µm pitch, will provide 2-port small signal SP measurements for the DUT. A DC power supply is connected to a single pin- DC probe in order provide bias voltages at V_{GATE} DC control pad. When measuring the 1-stage PIT structures, a 1-12GHz Bias-Tee and DC a power supply is connected at port1 between the VNA and the probes in order to provide the required drain voltage along the RF CPW.

4.3.2 COMMON GATE DEVICE TESTING

To access the common-gate circuit, the test die must be rotated 90^{o} clockwise from the orientation in Figure 4.2 . If placed correctly, then the CG circuit illustrated in Figure 4.5 can be located at the bottom left corner. In this test, the gate is permanently grounded and gate voltage control will be indirectly achieved through the source bias. V_s will be applied at port 2 using a bias- Tee instead of a DC probe, as shown in Figure 4.6 below. V_D and V_S are biased such that V_{GD} and V_{GS} will be at -5V for the OFF state. Conversely, V_D and V_S will remain at 0V for the ON state while measuring the s-parameter matrices of the device.

Table 4.1: CG device biasing voltages.

	V_D	V_S	V_G
ON	0V	0V	0V
OFF	+5V	+5V	0V

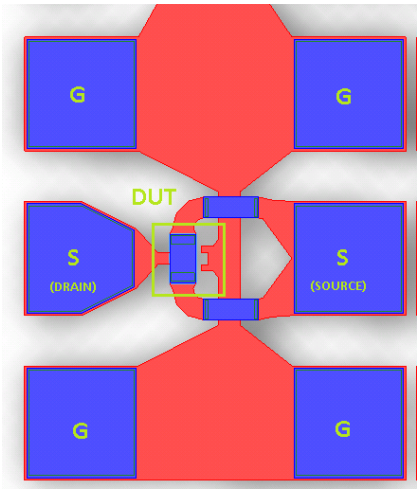


Figure 4.5: Common gate circuit

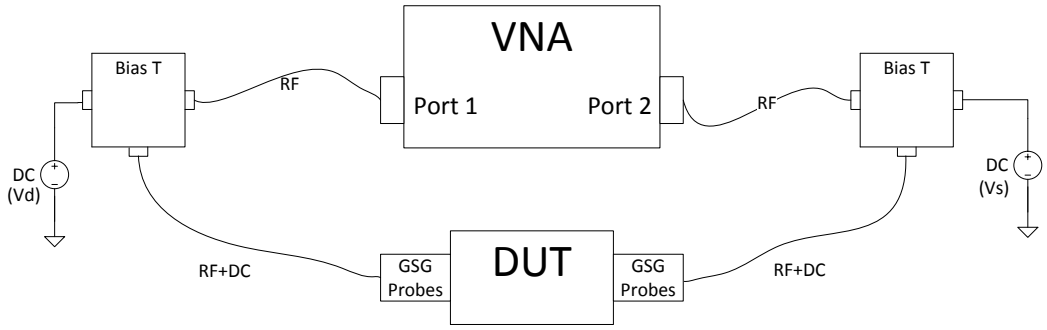


Figure 4.6: Common- gate circuit test bench.

4.3.3 MEASURING LOSSES IN A SINGLE STAGE PIT

In section 3.7, the Agilent ADS optimization tool was used to obtain optimal dimensions for which a CPW exhibits the least attenuation, while still maintaining a characteristic impedance Z_o =50Ω, and the most compact layout size. It was discovered that a stacked metal (1ME+2ME) CPW can achieve the same or better attenuation properties with

higher current carrying capabilities using smaller features than a single metal (1ME) CPW. However, airbridges that were later added to equalize ground plane potential will use the 2ME layer. As a result, the stacked metal CPW was slotted across the line at those locations. This will add discontinuities and added shunt capacitance which can cause different loading properties for the PIT section.

Figure 4.7 demonstrates the orientation used in measuring PIT sections included on IGNCUAEA, with annotation and proper orientation when measured. Figure 4.8 illustrates the setup used. Although the single metal and stacked metal circuits share the same V_{GATE} pad, they were tested separately.

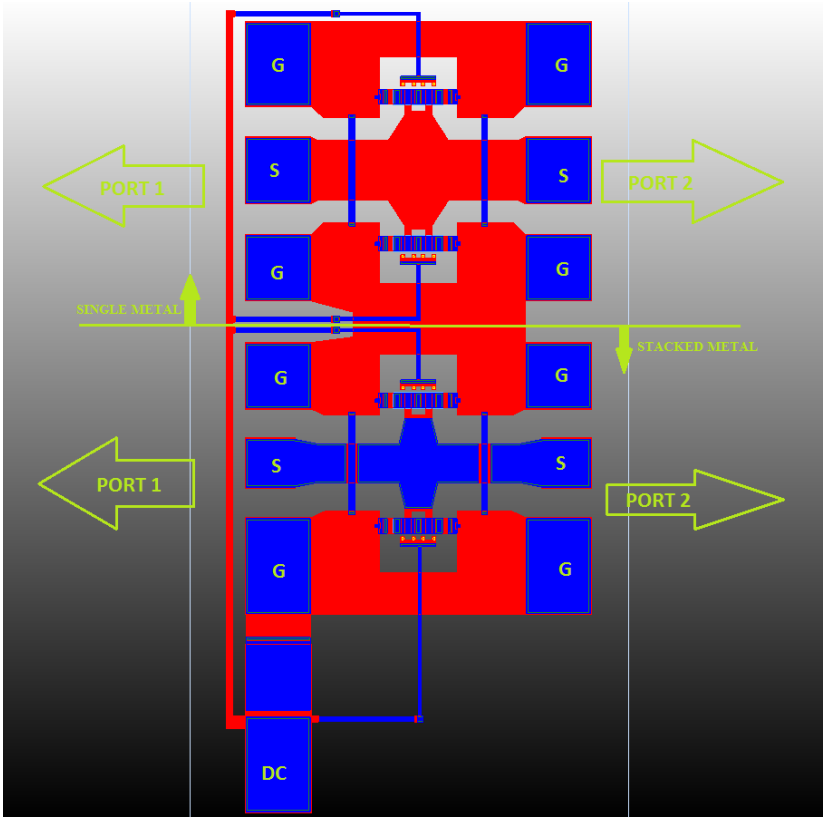


Figure 4.7: Single and stacked metal PIT sections onboard IGNCUAEA.

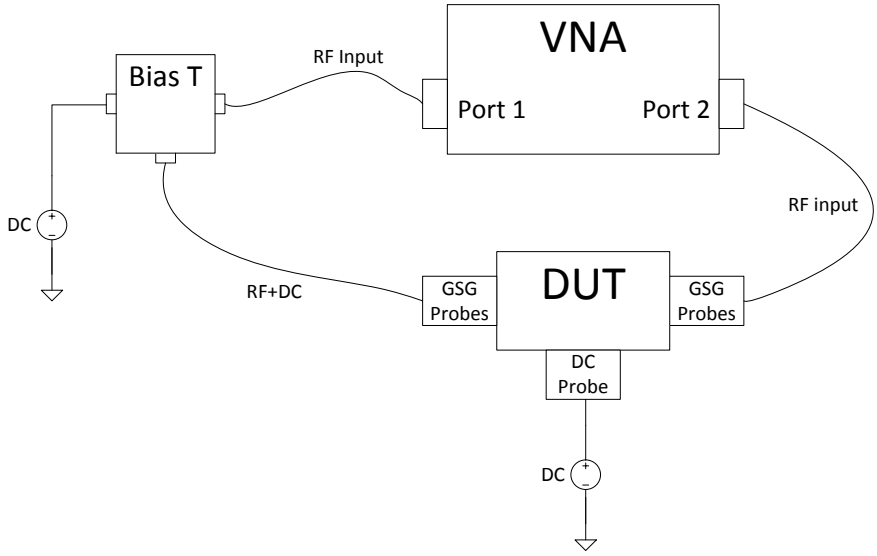


Figure 4.8: Test bench for common source testing of single and stacked metal circuits.

4.4 MEASURED RESULTS

4.4.1 COMMON GATE CONFIGURED FET RESULTS

Before testing the PIT structures, FET switch operation behavior must be verified in order to realize optimal bias voltages needed for turning switches ON and OFF. Thus, the corresponding IL and isolation of the CG configured 50um device are measured. In Figure 4.9 and Figure 4.10, results are compared to simulated results from the FET DK model provided by the NRC-CPFC. Some deviations of measured result from the simulated model are seen to exist, with the measured devices exhibiting better IL by 2.2dB-2.8dB and better isolation up to 7dB.

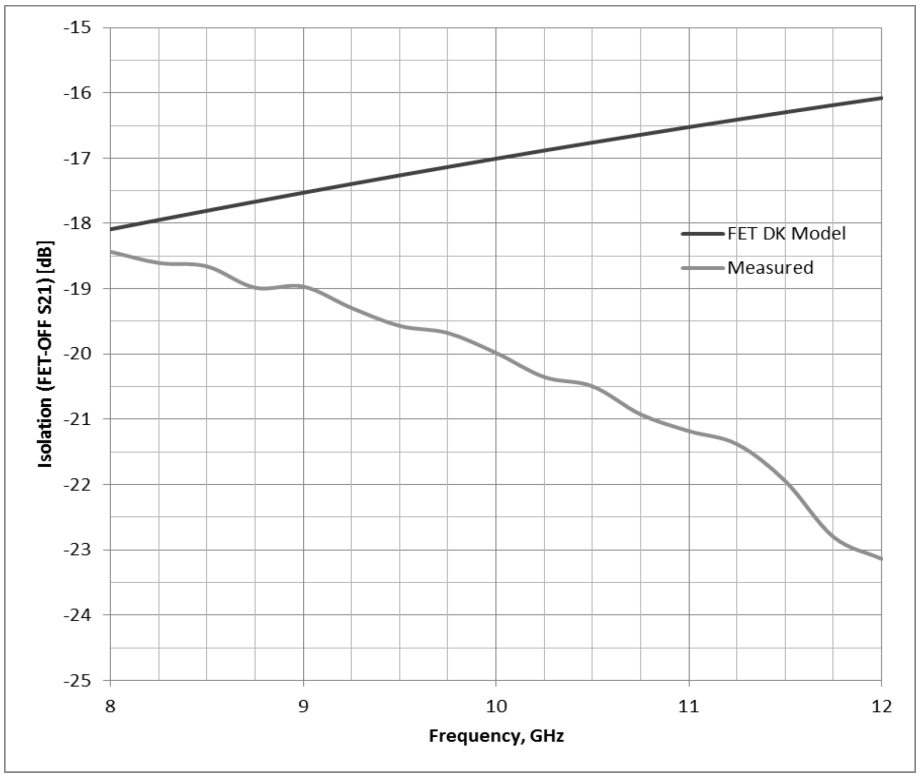


Figure 4.9: Measured vs. simulated isolation properties of a 50um GaN500 FET (OFF state).

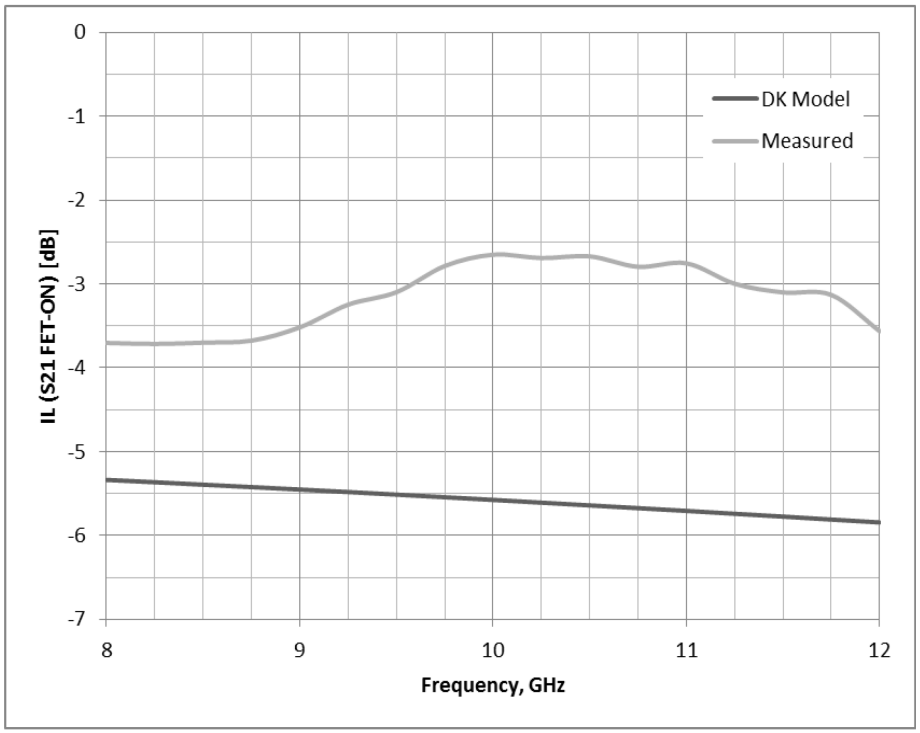


Figure 4.10: Measured vs. simulated IL properties of a 50um GaN500 FET (ON state).

4.4.2 SINGLE STAGE PIT MEASUREMENT RESULTS

The return losses measured from small signal measurements of the stacked metal PIT in the ON and OFF states were found to be consistent with co-simulated design results, as illustrated in Figure 4.11. It is worth noting that experimental results showed added ripple, which has been concluded to be a result of imperfectly calibrated VNA and test equipment. Furthermore, measured results from the single metal (1ME) PIT section results are very close to the stacked (1ME+1ME) PIT losses (not shown).

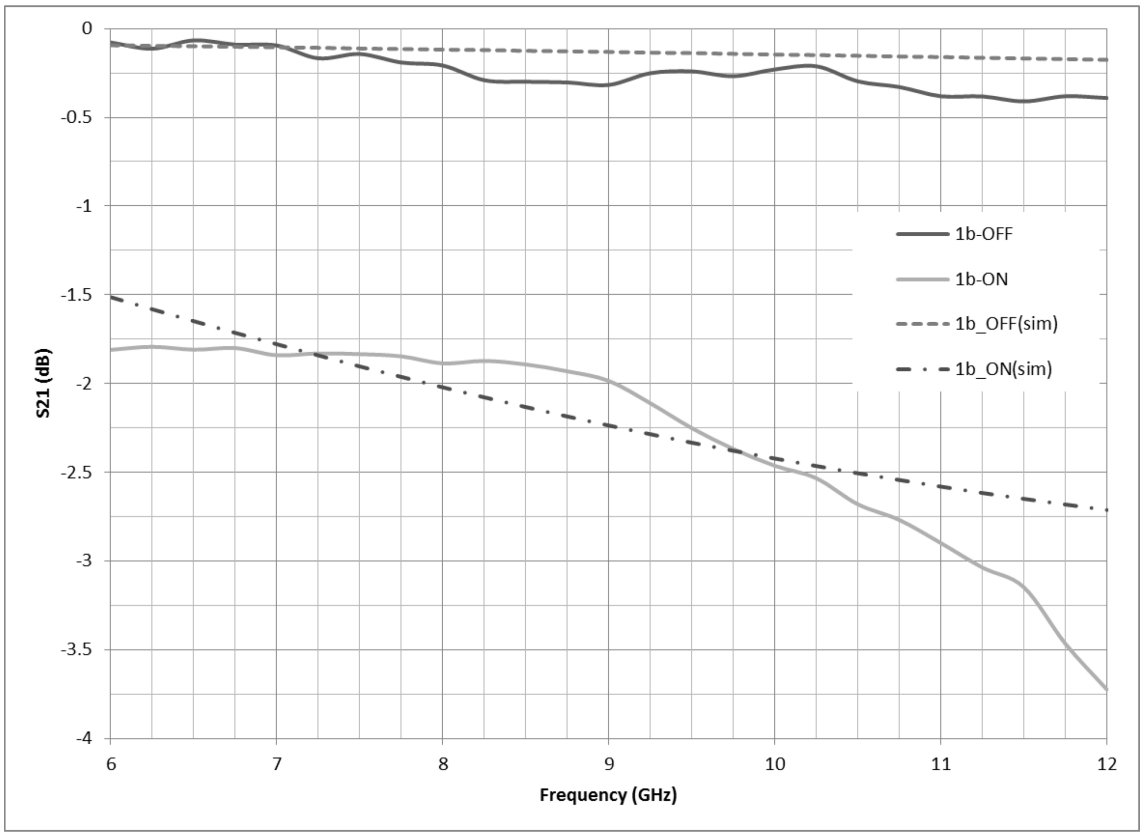


Figure 4.11: Measured vs. simulated small signal IL for a 1-stage PIT using stacked metal CPW.

The reflection (S11) curves of the measured PITs are given in Figure 4.12. They display a distinct change in impedance between ON and OFF states. Further, the measurements indicate a better than expected IL and isolation properties in the FET switches when

compared to co-simulated results in Figure 3.26. However, the smith chart matching point locations for the measured values exhibit extra phase shift than simulated values, which is a result of discrepancies between fabricated devices and the design kit models used in simulations. This of course is not detrimental to obtaining adequate smith chart coverage for a functional PIT. Finally, it was found that using V_{OFF} = -7V instead of -6V tends to provide better isolation.

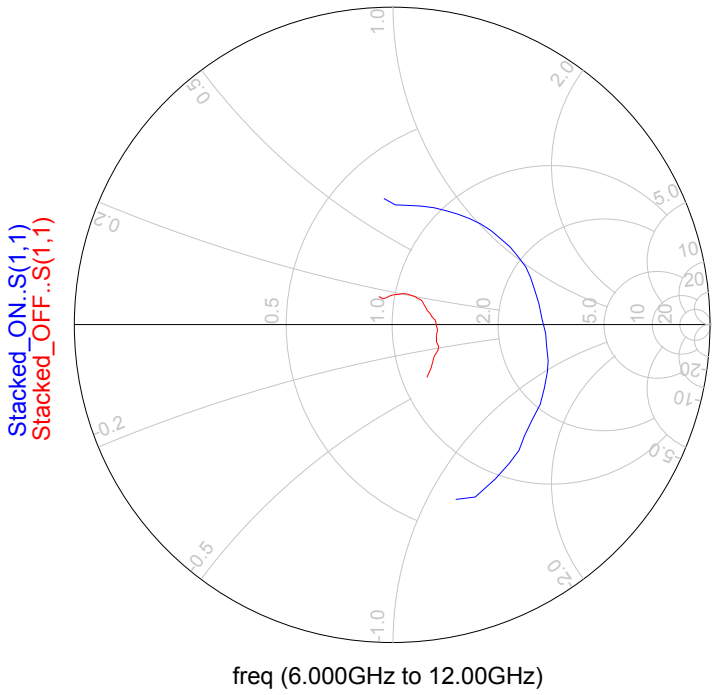


Figure 4.12: Smith chart plot of measured *S11* for stacked metal PIT.

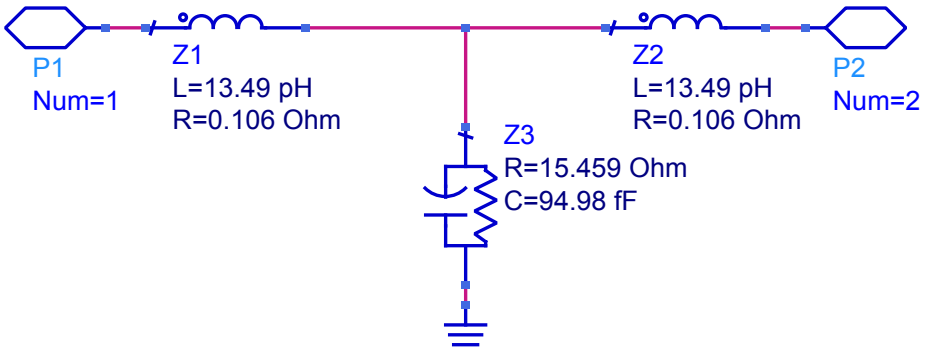
4.4.2 EQUIVALENT LUMPED ELEMENT MODEL EXTRACTION

Using techniques discussed in section 2.3 of this thesis, the ABDC matrix parameters and equivalent lumped element model were extracted from measured SP results at 10GHz.

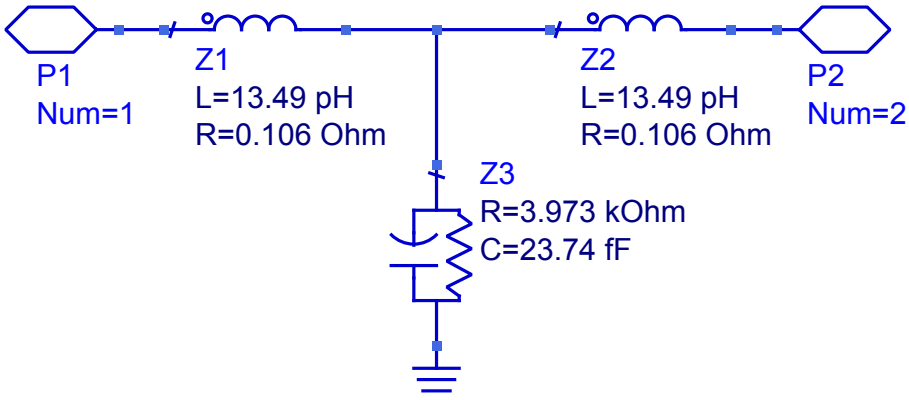
These are presented in Table 4.2. The T-section models in Figure 4.13 demonstrate the change in shunt loading impedance between the ON and OFF state.

Table 4.2: Extracted ABCD and Z-matrices for stacked metal PIT at 10GHz.

	ON (V=0V)	OFF (v=-7V)
ABCD matrix	$\begin{bmatrix} 0.862+0.08i & -0.210+9.481i \\ 0.015+0.027i & 0.862+0.08i \end{bmatrix}$	$\begin{bmatrix} 0.955+0.003i & 0.195+9.943i \\ 0.009i & 0.955+0.003i \end{bmatrix}$
Z matrix	$\begin{bmatrix} 15.565-22.842i & 15.459-27.928i \\ 15.459-27.928i & 15.565-22.842i \end{bmatrix}$	$\begin{bmatrix} 4.079-106.64i & 3.973-111.751i \\ 3.973-111.751i & 4.079-106.664i \end{bmatrix}$



(a)



(b)

Figure 4.13: Equivalent T-networks for stacked metal PIT in the (a) ON state, (b) OFF state.

4.5 LARGE SIGNAL LINEARITY SETUP AND MEASUREMENTS

One of the primary advantages that GaN technology offers over other process is the power handling capability at high frequencies, without suffering from compression. Measuring linearity using 1dB compression would not be appropriate in this situation since the power amplifier nonlinear characteristics are separate from these of the PIT. However, the linearity can be estimated through observation of IM3 components and extrapolation for the third-order intercept (*IP3)*. This can be done by applying 2 tones, f_1 and f_2, with equal power at the PIT input, and sweeping the power while observing the output power at frequencies $2f_1$-f_2 and $2f_2$-f_1. The two tones f_1 and f_2 are selected at 10GHz and 10.1GHz respectively, with IM3 products expected at 9.9GHz and 10.2GHz

The test bench setup for this measurement is shown in Figure 4.14, where 2 signal generators are connected via a combiner to the input of the PIT, while the output harmonics are observed through a spectrum analyzer.

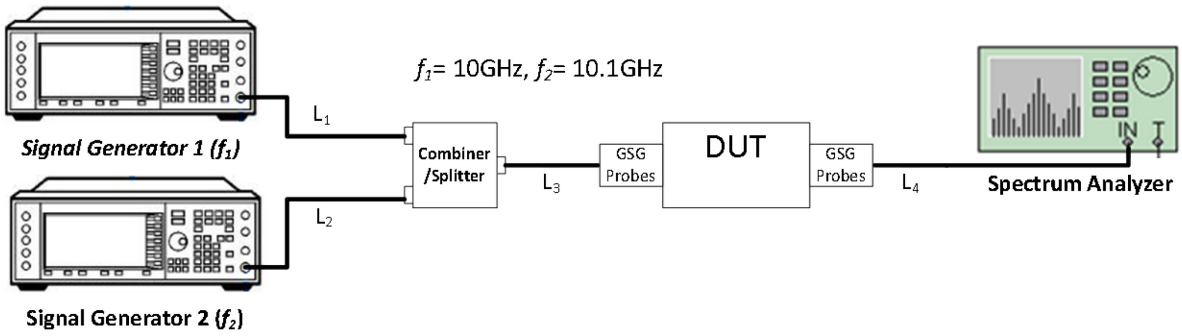


Figure 4.14: Harmonic Balance Test bench.

For the purpose of ensuring equal amplitudes for f_1 and f_2 at the input of the DUT, the losses in the combiner, probes and coax cables L_1-L_4 must be measured. This is done using the following steps:

1. Connect a signal generator directly to spectrum analyzer using coax line **L_1**, record power loss.
2. Repeat step 1 for L_2, L_3 and L_4.
3. Connect two signal generators to the spectrum analyzer using a combiner, L_1, L_2 and L_3. Record loss for f_1 and f_2 fundamentals. Losses for each test component are summarized in table 4.2 below.
4. Compensate for difference in loss between f_1 and f_2 in the combiner.
5. Land the GSG probes and sweep the input power, then record the output power of f_1, f_2, $2f_1$-f_2, $2f_2$-f_1
6. Extrapolating for 3rd order intercept

Component	Losses @10GHz (dBm)
L1	0.33
L2	0.83
L3	0.5
L4	1.5
L1+Splitter+L3	8.3
L2+splitter+L3	8.5
L1+Splitter+L3+probes+TL+L4	11.17
L2+splittler+L3+ probes+TL+L4	11.67

Table 4.3: Measured losses in large signal test environment

The power signal generators used were only able to output up to 16dBm of power, and third order harmonics were not detectable below 8dBm input due to a minimum detectable signal level of -106dBm on the spectrum analyzer. After correcting power levels to account for losses in the cables, probes and splitter at the output and input, the output fundamental tone 10GHz and the IM3 components were plotted in Figure 4.15 for the 1-stage stacked metal PIT, and trend lines were used to extrapolate and obtain corresponding linear equations. Solving the two equations indicated a 3rd- order intercept point (*IP3*) of **51.9dBm**.

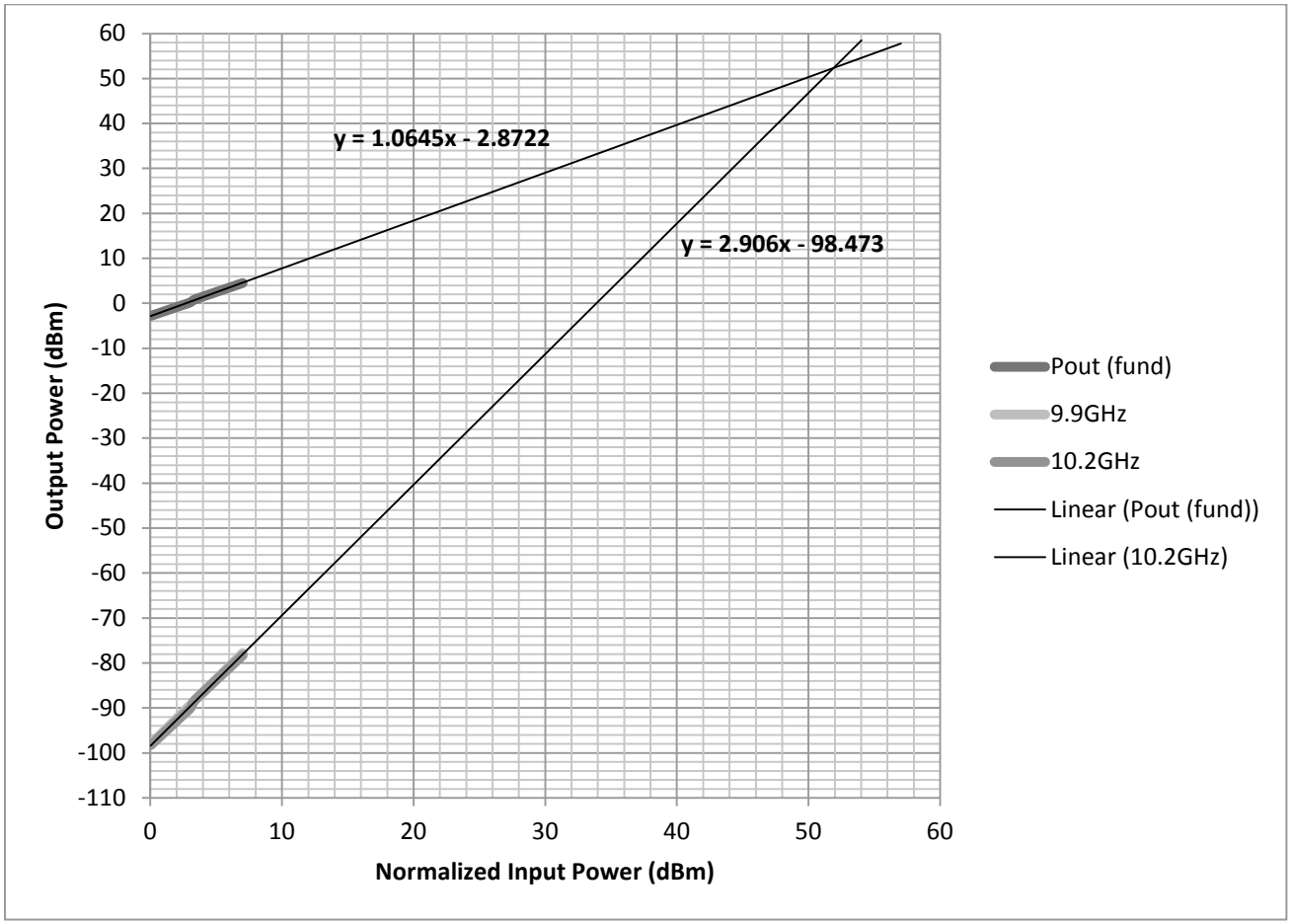


Figure 4.15: Measured fundamental output and IM3 vs. input power and extrapolated IIP3 for a 1-stage PIT

4.6 MEASUREMENT RESULTS SUMMARY

In this chapter, small- signal and large- signal measurements results of designed test structures onboard IGNCUAEA were carried out. Table 4.4 recapitulates I.L. and isolation measurements for a 50μm device in a common gate configuration for 8, 10 and 12GHz. Small signal results for the designed PIT section are summarized in Table 4.5. It should be noted that the high insertion loss through the switch does not necessarily violate the PIT specs given in Table 3.1 since the switches are only to turn on/off the shunt capacitances loading main line.

Table 4.4: Measured performance summary of 50um GaN500 FET switch

S21	8GHz	10GHz	12GHz
IL (dB)	5.4	5.6	5.9
Isolation (dB)	18.5	20	23.2

Table 4.5: Measured S21 Insertion loss of a single stage PIT

S21	8GHz	10GHz	12GHz
OFF	-0.25	-0.25	-0.3
ON	-1.8	-2.5	-3.75

The equivalent circuit model for the PIT was obtained, and it was discovered that in the ON state, an equivalent shunt capacitance and resistance of 95fF and 15.5Ω respectively is exhibited at 10GHz. Finally, IP3 of the PIT stage was estimated to be 51.9dBm. Therefore, using the relations given in chapter 2:

$$P_{1dB} = 42.24dBm = 16.75W \quad (4.1)$$

This high value of P_{1dB} is unrivalled in the reported impedance tuner realizations to date. The next chapter explores the usage of the core PIT building block in a full 8-bit PIT design.

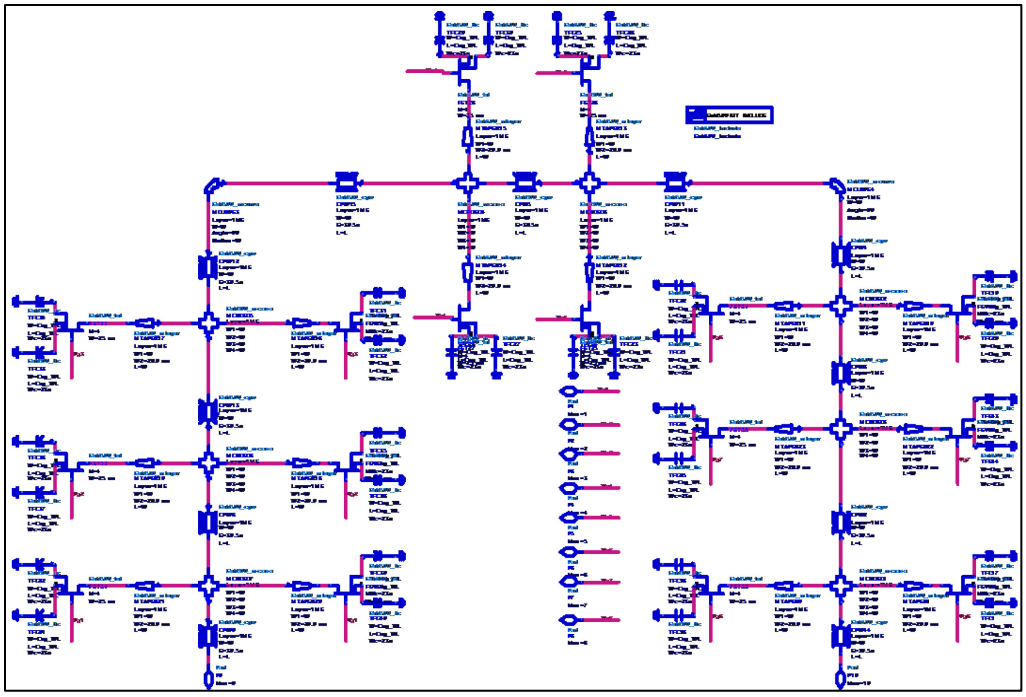
5.0 SIMULATING AN EIGHT-STAGE NETWORK

In this chapter, the proposed tuner's matching capability will be examined by observing the range of impedance coverage on a smith chart for select frequencies. Furthermore, performance degradation to a GaN class AB PA will be simulated when such a network is integrated. Hence, design specifications and results of the PA are put into consideration when tuner is designed.

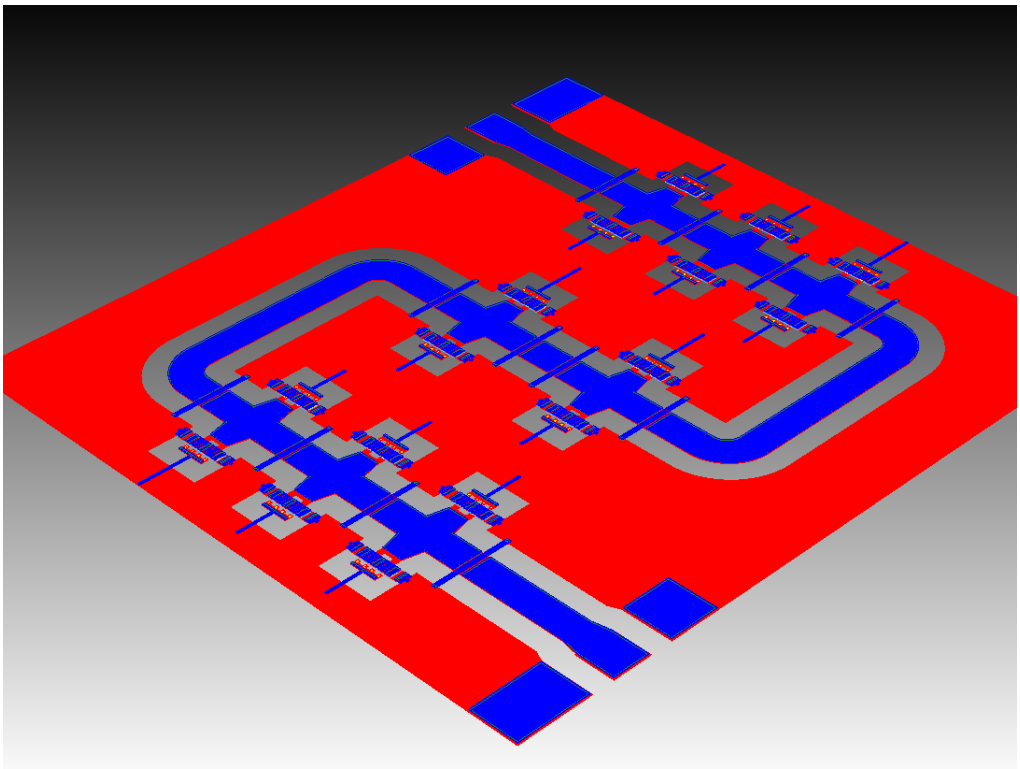
5.1 CIRCUIT DESCRIPTION

Using characterized devices and components of the design kit, the full 8-bit tuner schematic is constructed the conceptual design of Figure 2.19. In order to remain within the allowed 2mm x 2mm GaN chip area specifications, each switching stage is spaced using 250µm-long CPW sections. In addition, a folded geometry is employed. The resulting schematic in ADS is demonstrated in Figure 5.1(a) while the corresponding layout is given in Figure 5.1(b).

Source capacitors are divided evenly among both source terminals. Crosses, tapers and bends are utilized in the design to emulate layout design. A 10-pin schematic symbol is created for the design and a Monte Carlo simulation is carried out to test all the possible matching points produced when various combinations are attempted, as exhibited in Figure 5.2.



(a)



(b)

Figure 5.1: (a) Full circuit Schematic of 8-bit PIT, (b) corresponding layout.

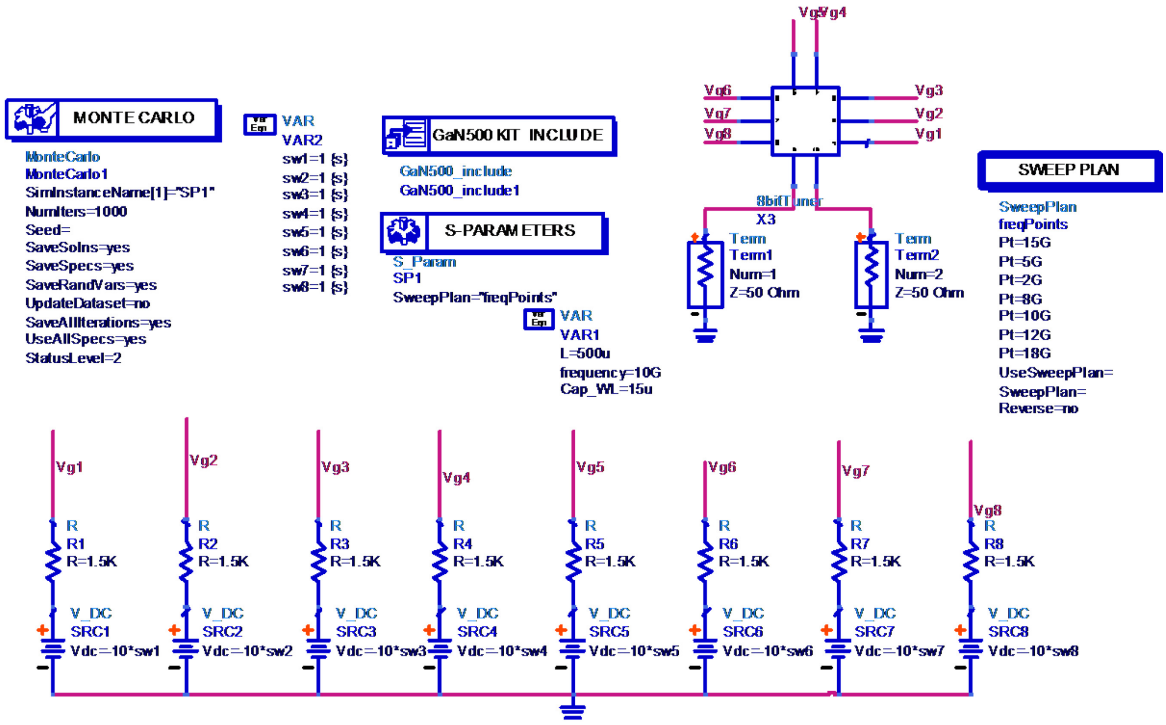


Figure 5.2: Monte Carlo Test bench of Tuner Schematic.

5.2 SCHEMATIC SIMULATION RESULTS

Z_{opt} for the power amplifier to be integrated with the programmable tuner was reported to be (36+j0) Ω [23]. Results from Monte Carlo simulations in figure 5.3 demonstrate that matching to this PA at 8-12GHz is possible. This is done by locating the matching point on the smith chart using a marker, referencing the Monte Carlo trial to a look up table, and determining the bit combination needed to achieve this matching. Figure 5.4 shows this procedure. For schematic design, it was determined that at V_1:V_8=1011 1101 can match to (35.827-j0.389) Ω. All schematic simulation results in this section will utilize this switch combination.

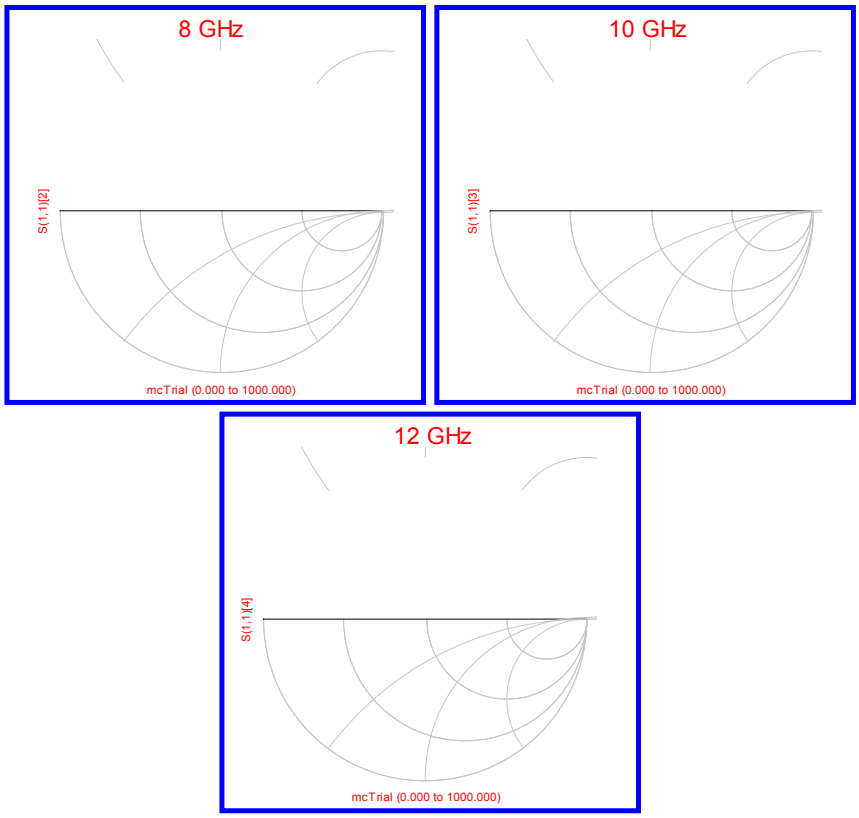


Figure 5.3: Smith chart coverage of schematic design for 8GHz, 10GHz, and 12GHz.

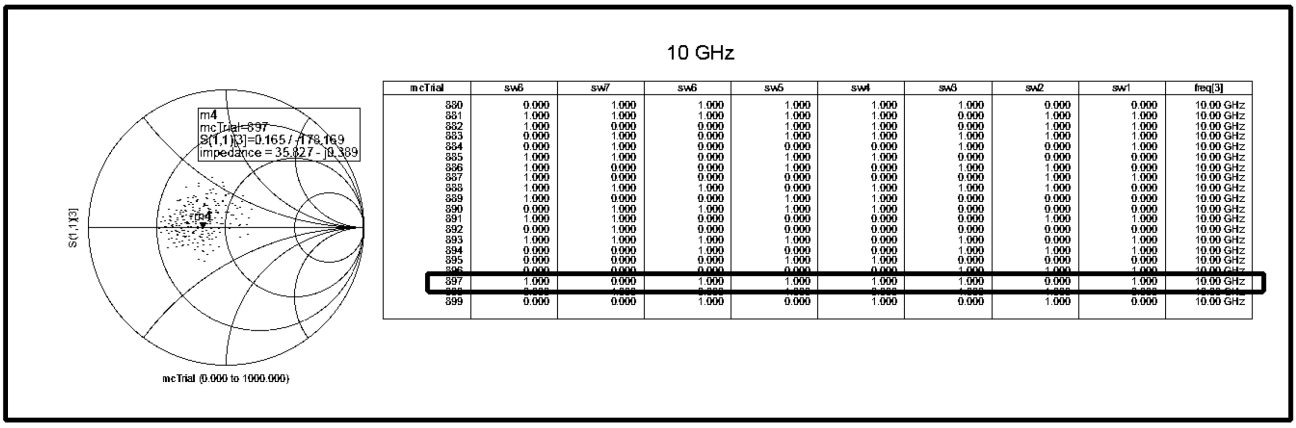


Figure 5.4: Locating desired Z_{opt} from Monte Carlo simulation results.

From Figure 5.5 provides the transmission loss through the entire 8-bit PIT. The insertion loss can be estimated to range from 0.85dB to 1.6dB over the 2-18GHz range. At 10GHz, the PIT introduces a loss of 1.4dB, which is within the target range specified in chapter 3.

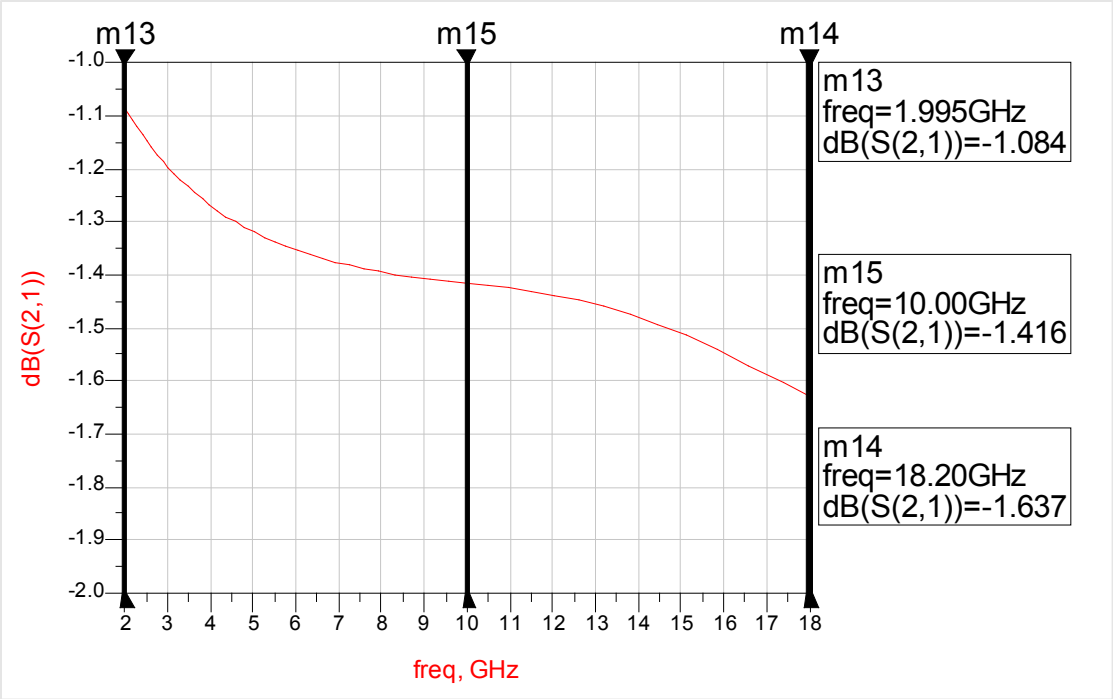


Figure 5.5: simulated Insertion Loss of an 8-bit PIT.

Stability of the tuner is also confirmed by verifying Kf>1 (StabFact) and B1-factor>0 (StabMeas) for the desired frequency range and can be shown in Figure 5.6.

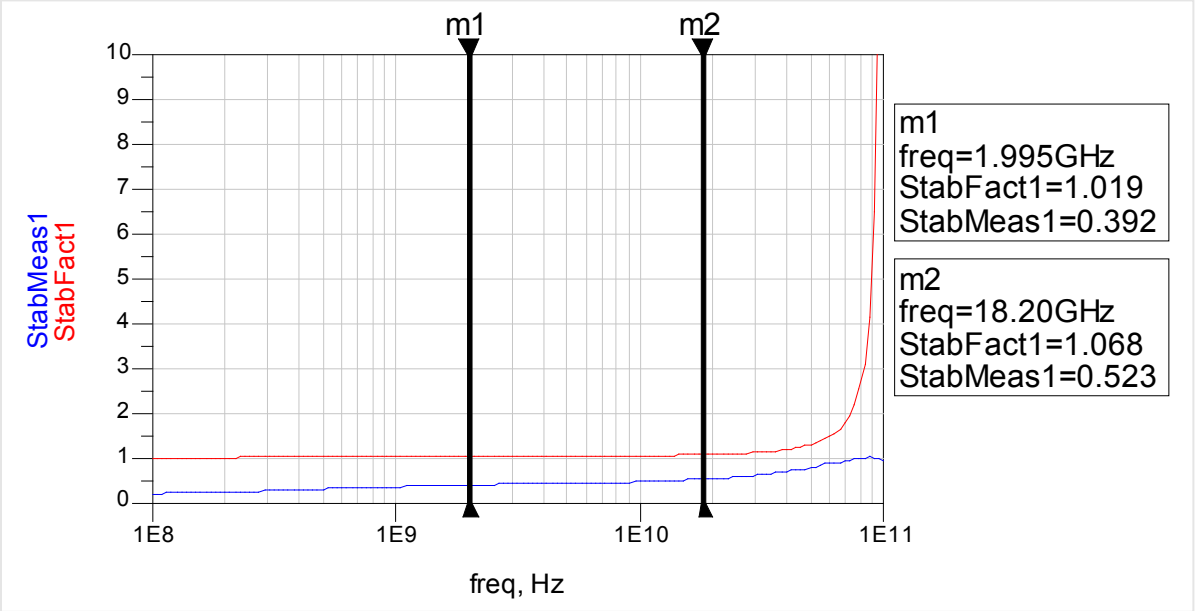


Figure 5.6: Stability of PIT design.

Linearity of the standalone PIT was measured using a 1-tone Harmonic balance test bench available in ADS. The input power is swept while the fundamental output power is observed for 1dB compression. However, the simulation failed to converge at output power of 37.2dBm (5.25W) without reaching compression point. This is shown in Figure 5.7.

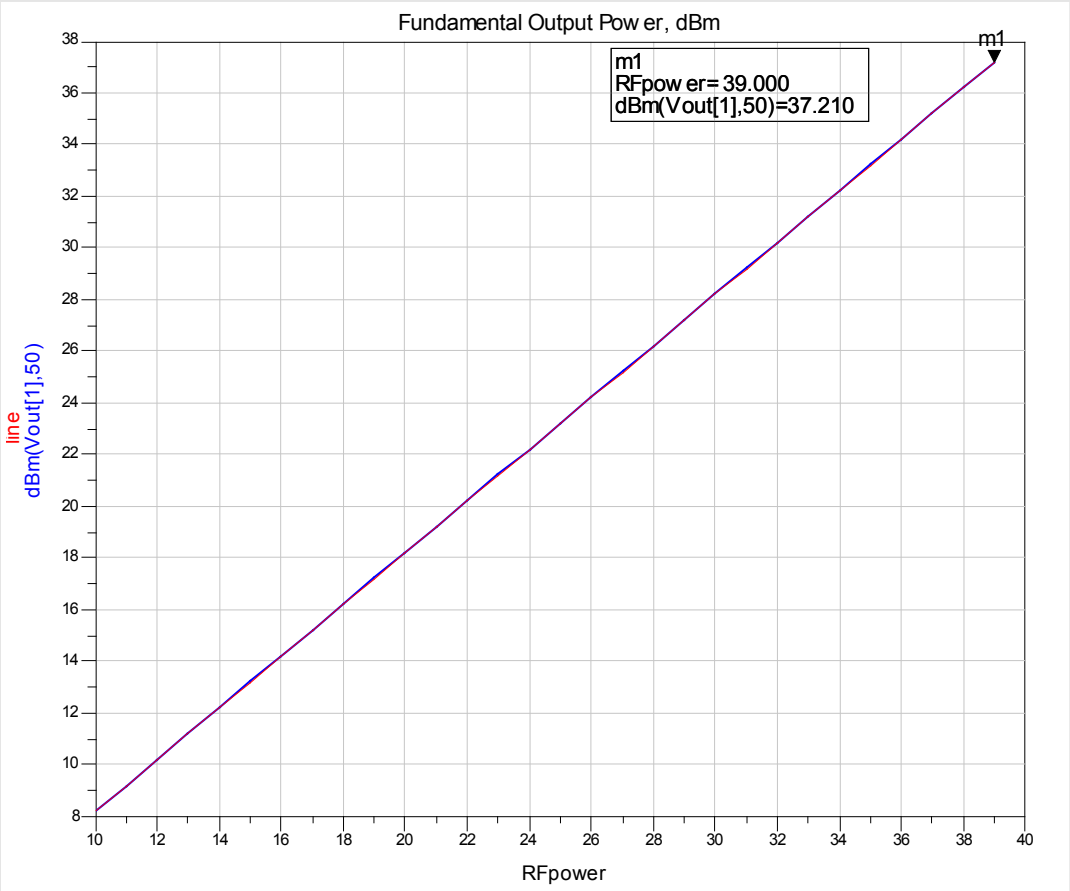


Figure 5.7: Linearity of PIT design.

5.3 CO-SIMULATION RESULTS

In this thesis, co-simulation refers to the combined EM simulation of the passive structure along with the active transistor device model. Figure 5.8 shows the result, which

exhibits only minimal changes from the schematic based performance determined in Figure 5.3.

Using a test bench similar to the one used for Monte Carlo simulations for schematic design, The Design was for smith chart coverage. Multiple design readjustments where done to achieve acceptable coverage over the desired range of frequencies.

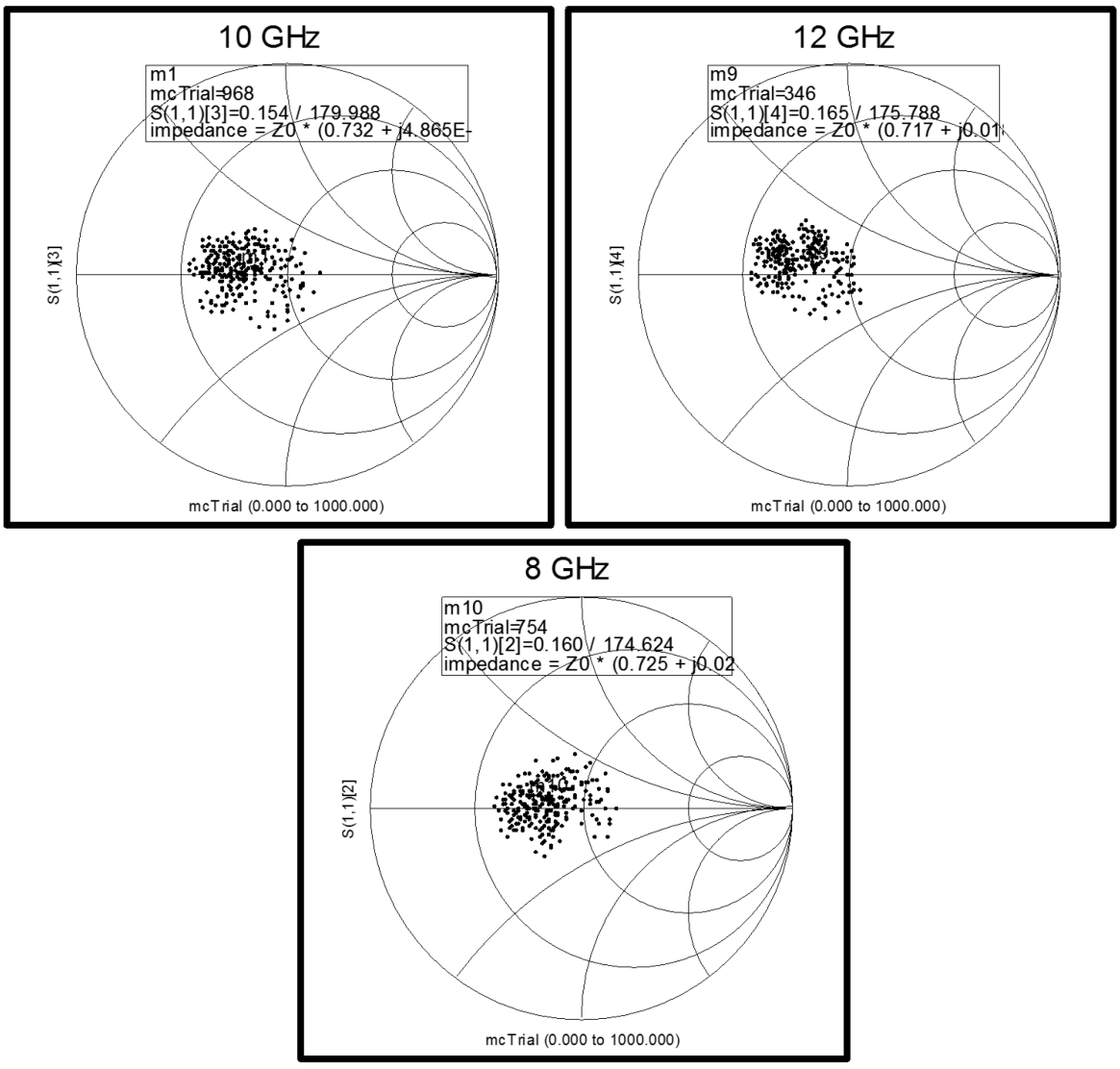


Figure 5.8: Smith Chart Coverage at 8GHz, 10GHz and 12GHz using co-simulation

Similar to simulations carried out for schematic design, plots for maximum gain, stability and line losses are generated and verified. Testing the co-simulated design for large signal linearity was not possible since EM-simulations were performed using small signal s-parameter simulations.

5.4 8-BIT PIT VALIDATION USING CASCADED MEASURED RESULTS

The small signal s-parameters obtained from measured results of the single stage PIT can be used to predict the impedance matching coverage when 8 stages are used. This is done by cascading measured values in ABCD parameter form, as described in section 2.3.1. The S_{11} coverage is shown in Figure 5.10 illustrates how the max VSWR obtainable is limited due to the small source shunt capacitance C_{ss} that was used in the fabricated design.

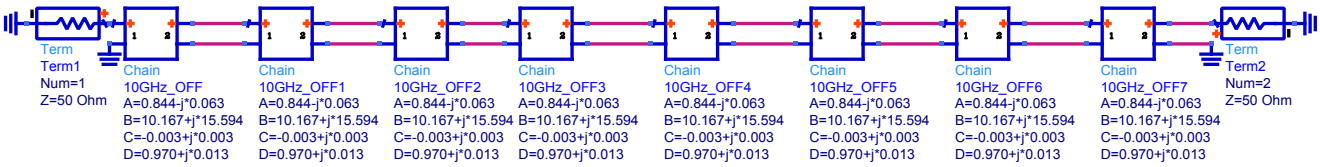


Figure 5.9: Predicting achievable 8-bit PIT coverage using cascaded measured parameters

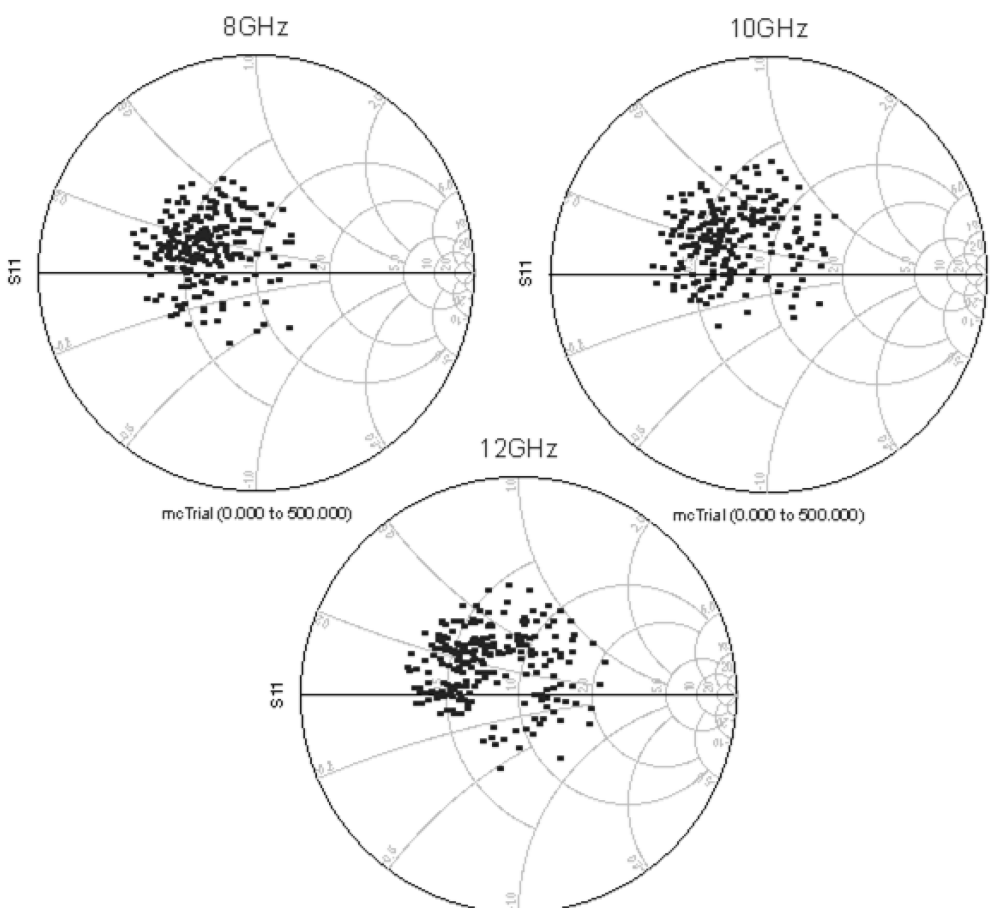


Figure 5.10: Matching coverage for an 8-bit cascaded PIT using measured parameters

5.5 POWER AMPLIFIER INTEGRATION

As a final demonstration of the functionality of the PIT developed in this thesis, an analysis will be made to match the output of the GaN power amplifier design referenced in [23]. Figure 5.11 shows the setup used. Figure 5.12 reveals that peak Power Added Efficiency (PAE) of 21% could be achieved at 25dBm of input power, with 8.4dB of gain and 32.1dBm of output power. The 1dB compression for the PA system is observed to be 24dBm of input power with a gain of 7.9dB, as shown in Figure 5.13. Finally, Table 5.1

displays how the designed PIT fares against an ideal matching network in terms of key PA specifications.

It is seen that use of the developed PIT caused a reduction of 10% in PAE, along with some decreases in PA gain and output power. Such a drop in PAE appears acceptable given that any other external impedance matching network would cause PAE penalty of its own, witout having the ability to reconfigure according to operating conditions.

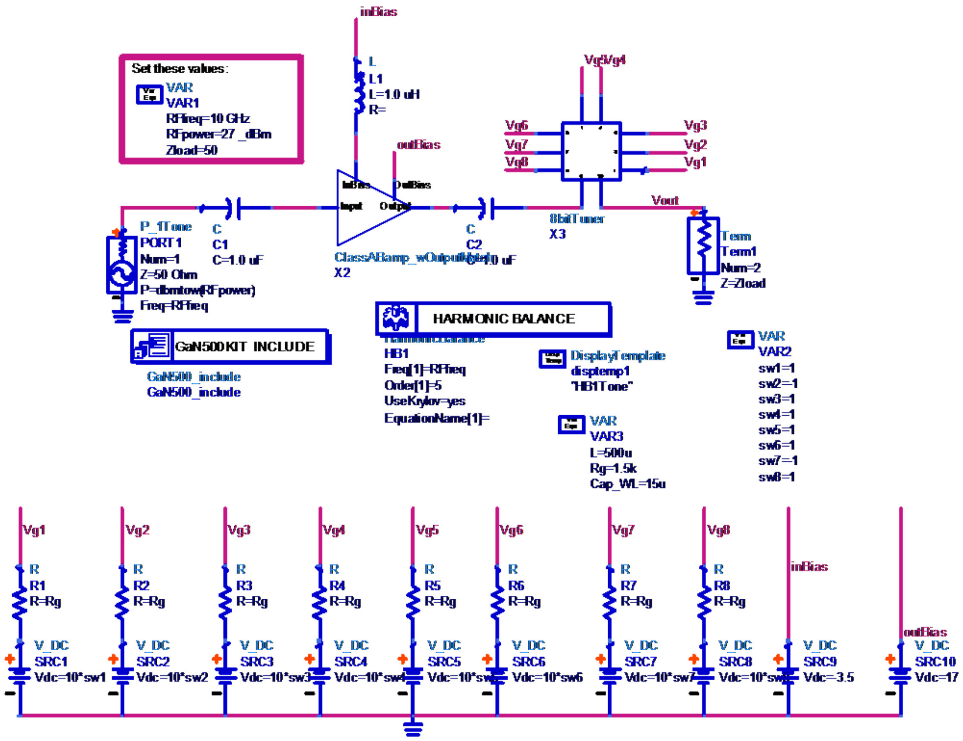


Figure 5.11: 1-Tone harmonic balance test bench for testing PA with developed PIT

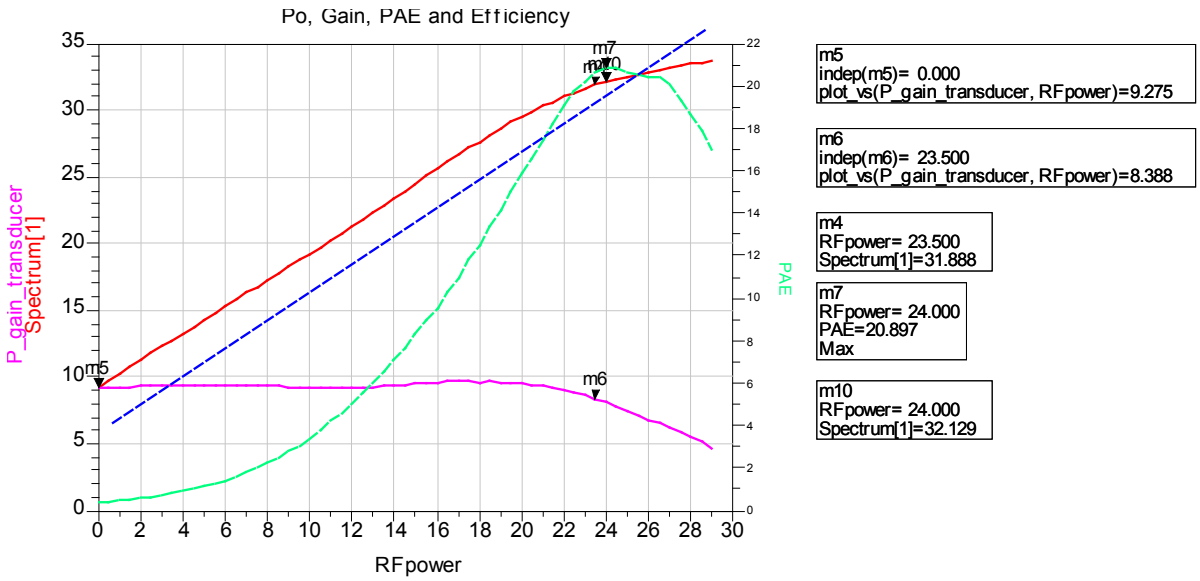


Figure 5.12: Sweeping input Power vs. PAE, Gain & Pout for PA+Tuner.

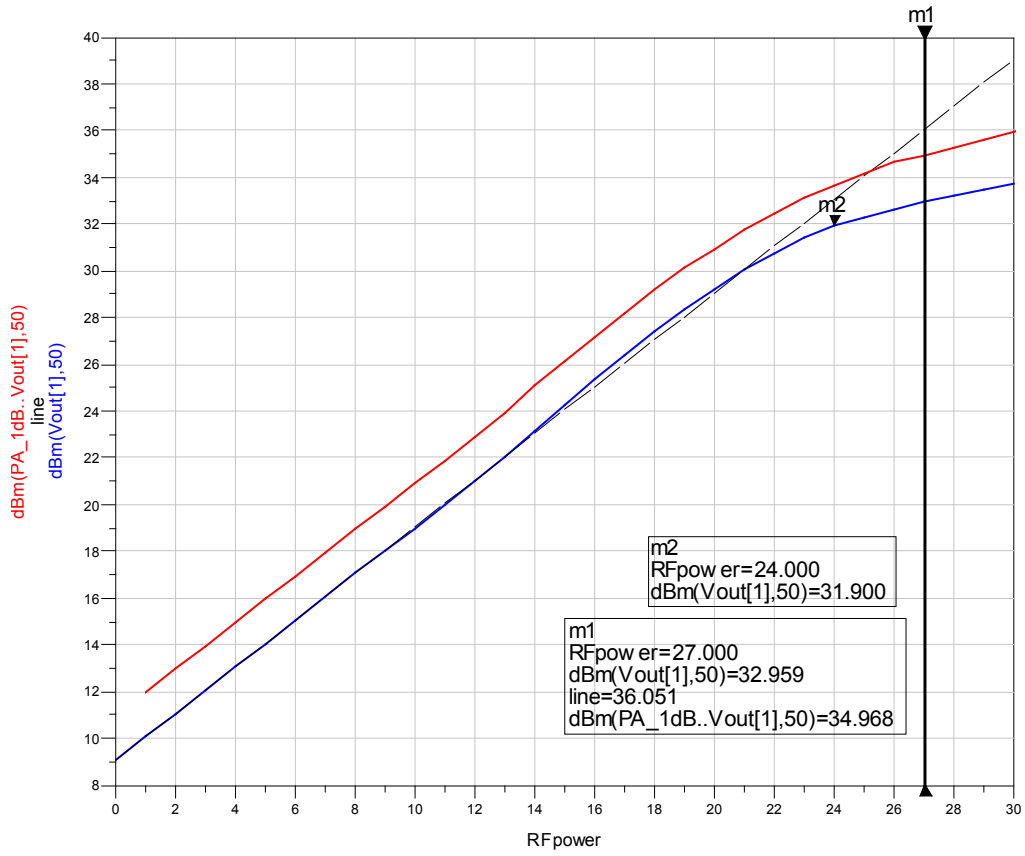


Figure 5.13: Linearity comparison of PA with and without including PIT.

Table 5.1: Comparison of PA performance using an ideal matching network vs. designed PIT.

Parameter	PA with ideal matching network	PA Matched with Tuner
Operating Frequency	10 GHz	
Output P1dB	32.7 dBm	31.9dBm
Gain at P1dB	9.7 dB	7.9dB
Peak Efficiency (PAE)	31.4 %	21%

6.0 CONCLUSIONS & FUTURE WORK

This thesis has presented the design, simulation, and measurement results of single-stage programmable impedance tuner (PIT) based on the use of 0.5µm Gallium Nitride (GaN) process technology. Several of the key figures of merit for a PIT, such as insertion loss, smith chart impedance matching coverage, and power handling capabilities (P_{IP3}), have been discussed and investigated in detail.

In summary, this work underlines the constraints in using GaN active transistor switches to provide variable load impedance. Characterization of FET switch properties and the use of various switch topologies were carried out in order to reduce losses and improve functionality of the PIT. A single stage PIT was successfully measured and the results have verified that the process is reliable. Actual measured values were reused to simulate the co-integration of resulting eight-stage PIT with a class AB- GaN power amplifier. Overall, the thesis objectives were achieved.

6.1 FUTURE WORK

Future work will include fabrication of a full 8-stage PIT based on results obtained from test structures onboard IGNCUAEA chip. Due to factors beyond the control of the author, fabrication an 8- stage PIT at the CPFC-NRC could not proceed as planned.

Furthermore, PA integration of the PIT and testing of several multifunctional system concepts: should be pursued adapting for a variable load presented by an antenna; ad-

aptation of the output matching impedance for changing environmental characteristics, etc.

The improvement of PIT insertion loss through the use of multiple- FET switch configurations designed in Chapter 3 should be fully investigated, as well as expansions to impedance matching coverage through the use of a better, more mature GaN process and improved design kits should be investigated.

In conclusion, through the examination of design constraints and performance requirements, the work in this thesis should aid in the design of GaN reconfigurable matching networks. Through the demonstrations of integration with the class- AB power amplifier, and the detailed design and analysis of a GaN hybrid lumped-distributed impedance tuner with GaN FET switches, it is the hope of this author that this work will enable multifunctional reconfigurable power amplifiers in the future.

APPENDIX A: SUPPLEMENTARY Z-PARAMETER AND ABCD-MATRIX EQUATIONS

$$z_{11} = \frac{A}{C}\ , \quad z_{12} = \frac{AD-BC}{C}\ , \quad z_{21} = \frac{1}{C}\ , \quad z_{22} = \frac{D}{C}$$

$$y_{11} = \frac{BC-AD}{B}\ , \quad y_{12} = \frac{BC-AD}{B}\ , \quad y_{21} = \frac{-1}{B}\ , \quad y_{22} = \frac{A}{B}$$

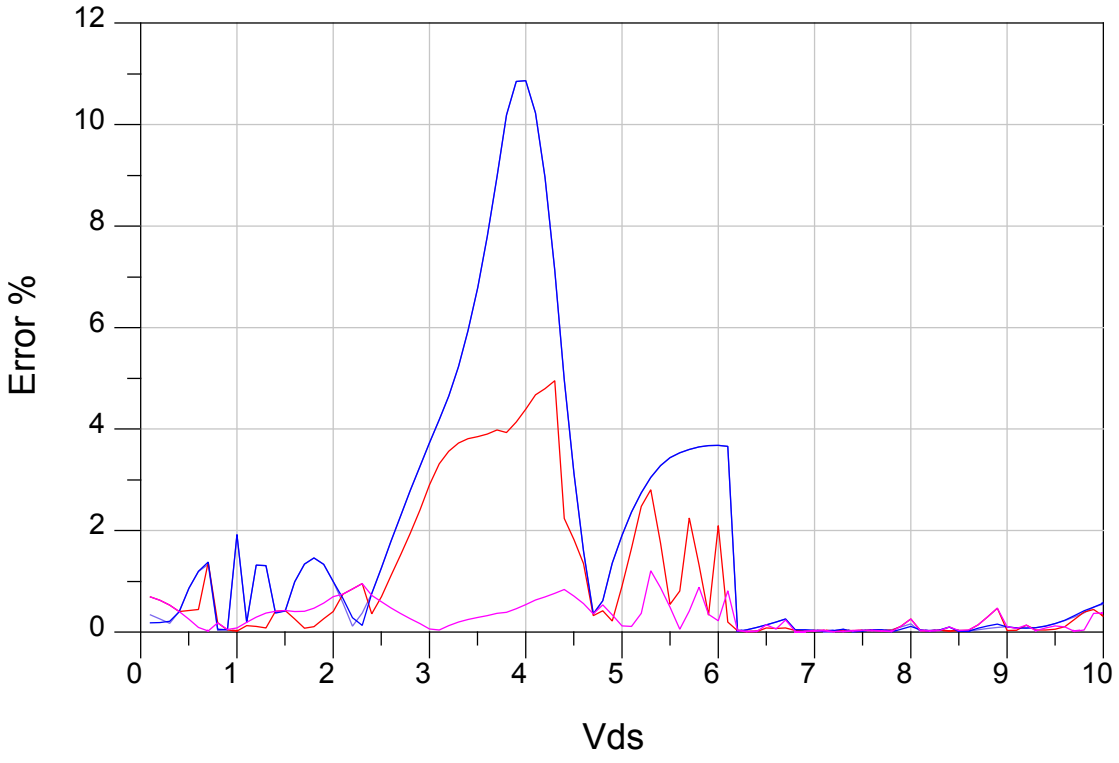
$$A = 1 + \frac{Z_1}{Z_3} = 1 + \frac{Y_2}{Y_3}$$

$$B = Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3} = \frac{1}{Y_3}$$

$$C = \frac{1}{Z_3} = Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3}$$

$$D = 1 + \frac{Z_2}{Z_3} = 1 + \frac{Y_1}{Y_3}$$

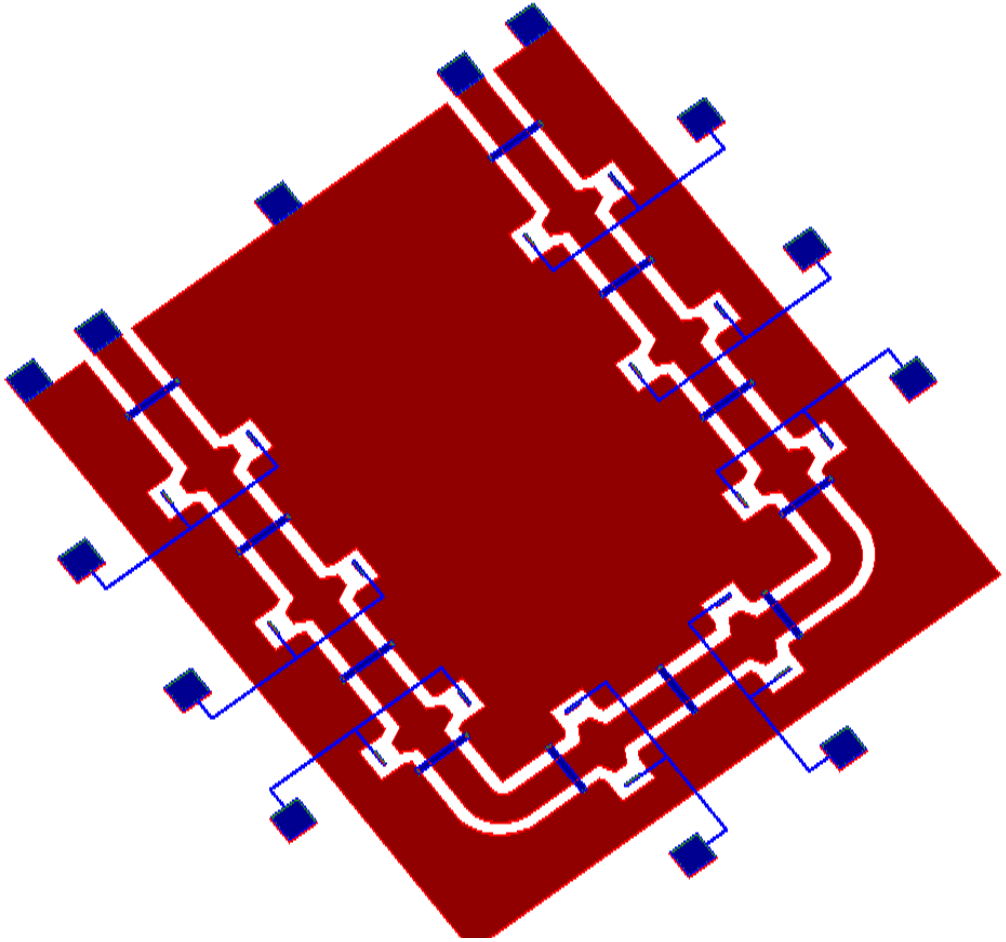
APPENDIX B: Z_{IN} CURVE FITTING OPTIMIZATION ERROR TOLERANCE

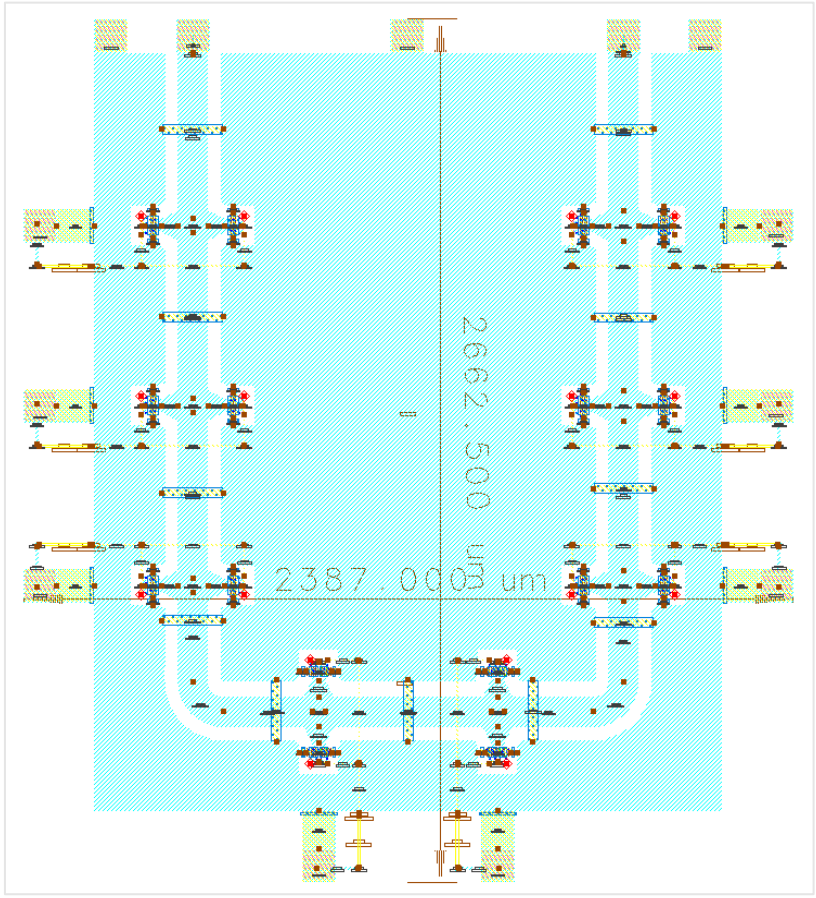


Meas Eqn

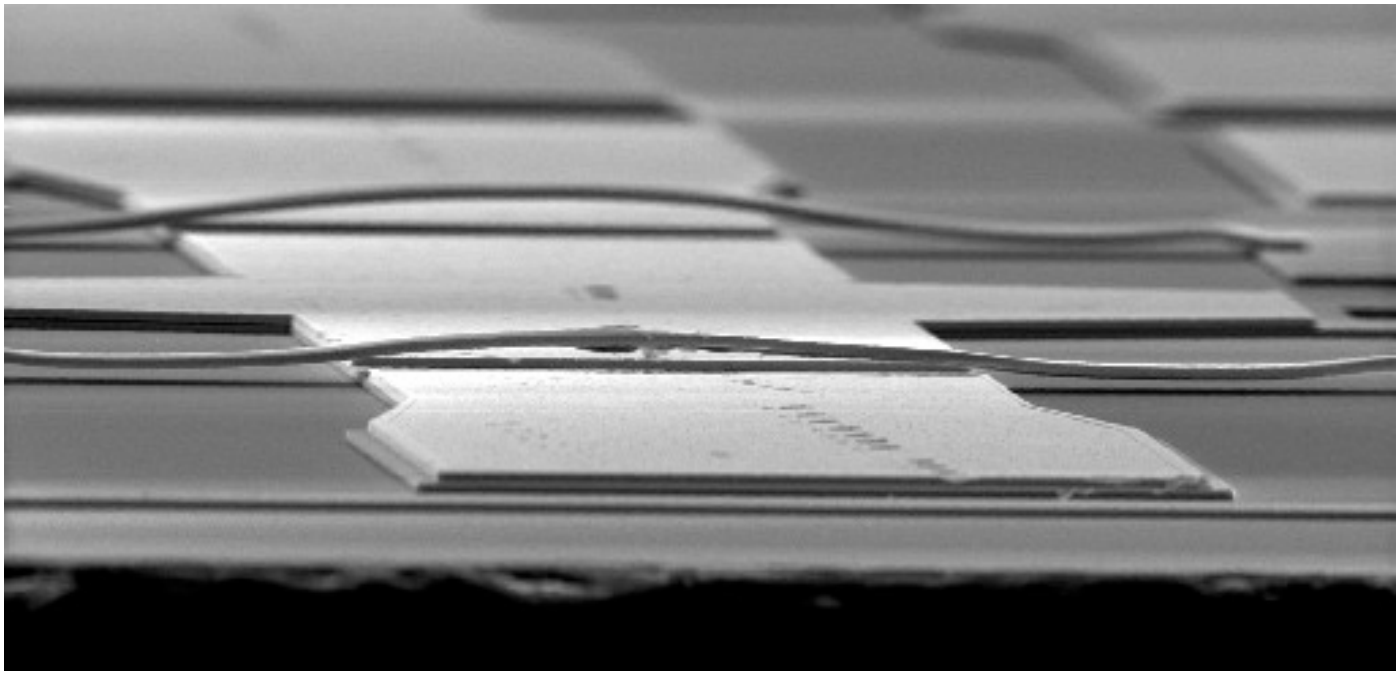
MeasEqn
Meas1
E1=abs(real(S(1,1))[0,0]-real(S(2,2))[0,0])
E2=abs(real(S(1,1))[1,0]-real(S(2,2))[1,0])
E3=abs(imag(S(1,1))[0,0]-imag(S(2,2))[0,0])
E4=abs(imag(S(1,1))[1,0]-imag(S(2,2))[1,0])

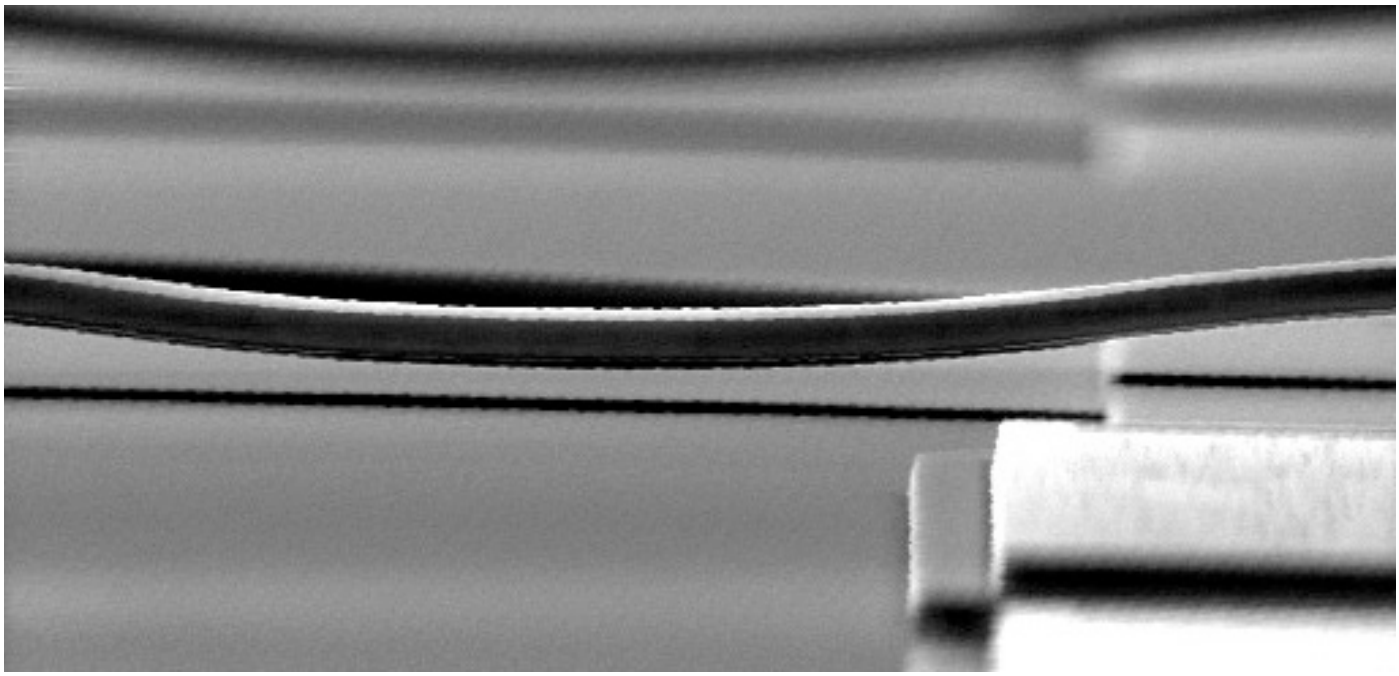
APPENDIX C: INITIAL DESIGN LAYOUT





APPENDIX D: IMAGES OF PIT STRUCTURES AND AIR-BRIDGES





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