NOTE TO USERS

TUNABLE FILTER AND RECEIVE SIGNAL STRENGTH INDICATOR FOR DETECTING WHITESPACE IN THE FREQUENCY SPECTRUM

By

Daniel J. Olszewski

A thesis
presented to Carleton University
in fulfilment of the
thesis requirement for the degree of
MASTER OF APPLIED SCIENCE
in
ELECTRICAL ENGINEERING

Ottawa, Ontario, Canada

Your file Votre référence
ISBN: 0-494-13448-8
Our file Notre référence
ISBN: 0-494-13448-8

Abstract

A tunable bandpass filter based on an active inductor and a receive signal strength indicator (RSSI) are designed to form a whitespace detector integrated circuit (IC) for finding unused frequency bands in the radio frequency (RF) spectrum. Theoretical equations are derived to predict the inductance and series resistance of the active inductor, and the center frequency and gain of the bandpass filter. The filter's tuning behavior, transient response and linearity, as simulated and measured for a fabricated IC, demonstrate circuit functionality between 70 MHz and 700 MHz. A procedure for assembling the RSSI using limiting amplifiers and rectifiers is developed. The RSSI's logarithmic input amplitude to output voltage characteristic and its transient settling response are simulated and tested. From these circuits, a system is simulated to demonstrate its ability to distinguish between occupied frequency bands and those that are vacant whitespace.

Acknowledgements

I would like to thank my supervisor, Dr. Leonard MacEachern, for his support and guidance throughout the completion of this research. I would also like to thank Dr. Samy Mahmoud who was instrumental in obtaining funding and space on campus, enabling the research.

Financial support for this research has been provided by the National Sciences and Engineering Research Council of Canada (NSERC), the National Capital Institute for Telecommunications (NCIT) and Carleton University. The integrated circuit for this research was fabricated at the Taiwan Semiconductor Manufacturing Company (TSMC) and subsidized by the Canadian Microelectronics Corporation (CMC). Agilent Technologies has supported the research with significant discounts on equipment used in testing the circuits.

I would especially like to thank Vladimir Vukovic for his work in designing the printed circuit board (PCB) for testing the integrated circuit (IC), Dr. Pedro Barrios of the National Research Council of Canada (NRC) for wire bonding the ICs to the PCBs and Nagui Mikhail for on-going technical assistance.

I am grateful for the members of my defence committee, Dr. Jim Wight, Dr. Calvin

Plett, Dr. Adrian Chan and Dave Dobson, who took the time out of their busy schedules to review my work.

I've had the great pleasure of working with a number of outstanding colleagues throughout this research to whom I'd like to extend thanks for all of their help and camaraderie. In particular, I'd like to thank Celine Fletcher, Fiona Shearer, Mark Houlgate, Sinisa Milicevic, Yasser Soliman, Jeff Slater and Ziad El-Khatib.

Table of Contents

List of Tables

List of Figures

List of Abbreviations

ASIC	Application Specific Integrated Circuit
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
DFT	Discrete Fourier Transform
DSP	Digital Signal Processing
DUT	Device Under Test
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
GaAs	Gallium Arsenide
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
IIP2	Input-Referred Second Order Intercept
IIP3	Input-Referred Third Order Intercept
IM2	Second Order Intermodulation
IM3	Third Order Intermodulation
ISM	Industrial, Scientific, Medical
LNA	Low Noise Amplifier
MIM	Metal Oxide Metal
PCB	Printed Circuit Board

PCS	Personal Communications Service
PDA	Personal Digital Assistant
POT	Potentiometer
PSS	Periodic Steady State
RF	Radio Frequency
RSSI	Receive Signal Strength Indicator
SDR	Software Defined Radio
SoC	System on Chip
UHF	Ultra High Frequency
VHF	Very High Frequency
WISP	Wireless Internet Service Provider
WLAN	Wireless Local Area Network

List of Symbols

A_{DC}	DC gain of the limiting amplifier
A_{RSSI}	Total gain of the receive signal strength indicator
A(s)	Gain of the limiting amplifier
β	3-dB bandwidth of the bandpass filter
C_C	Coupling capacitor
C_{db}	Drain to bulk capacitance of a transistor
C_{gs}	Gate to source capacitance of a transistor
C_{gd}	Gate to drain capacitance of a transistor
C_{in}	Input capacitance of the bandpass filter
C_{out}	Output capacitance for the RSSI
C_{ox}	Oxide capacitance of a transistor
C_{sb}	Source to bulk capacitance of a transistor
g_m	Transconductance of a transistor
I_{REF}	Current generated by the current sources on the PCB
I_1	Tuning current for the bandpass filter
I_2	Tuning current for the bandpass filter
N	Number of limiting amplifier stages in the RSSI
P_{dBm}	Signal power
P_{WATTS}	Linear signal power
P_{1dB}	1-dB compression point
Q	Quality factor
r_o	Output resistance of a transistor
R_{out}	Output resistance for the RSSI

R_S	Series resistance of inductor
R_{SET}	Resistance used to generate the currents on the PCB
τ	Settling time constant of the RSSI
t_{settle}	Settling time of the RSSI
μ_p	Hole mobility for a transistor
V_{DD}	Supply voltage
V_{peak}	Peak voltage amplitude
V_p	Peak to peak voltage amplitude
V_{RMS}	Root mean squared voltage amplitude
V_t	threshold voltage of a transistor
V_1	Tuning voltage for the bandpass filter
V_2	Tuning voltage for the bandpass filter
ω	Radian frequency ($\omega = 2\pi f$)
ω_0	Radian center frequency of the bandpass filter ($\omega_0 = 2\pi f_0$)
ω_{3dB}	Radian 3-dB bandwidth of the limiting amplifier ($\omega_{3dB} = 2\pi f_{3dB}$)
W/L	Width to length ratio of a transistor

Chapter 1

Introduction

1.1 Motivation

The radio frequency (RF) spectrum is becoming crowded with the growing number of wireless devices transmitting in it [1]. Frequency bands are generally licensed and regulated so that only the licensed user is allowed to transmit in the band at any time. This can lead to inefficient use of resources, since there may be times when the licensed transmitter is not using its frequency band. One solution to increase spectral efficiency is to allow unlicensed users to transmit in a frequency band when the licensed user is not transmitting. The Federal Communications Commission (FCC), which regulates the RF spectrum in the United States, has put forth a proposal that would allow spectrum sharing in the band of frequencies currently licensed for broadcast television transmitters [2]. This opens the door for unlicensed devices to transmit in licensed but unused frequency bands.

If these unused frequency bands, also known as "spectrum holes" or "whitespace" [3], can be detected and used by a wireless device, it can enable alternate users to transmit

in the same frequency band at different times without interfering with each other. These wireless devices could incorporate cognitive radios [6–10] that could adapt to a changing spectral environment and permit the device to change its transmitting frequency to whatever band is available at a given time. A part of the cognitive radio's sensing circuitry will be required to sense and detect whitespace. The focus of this thesis is on the design and implementation of a whitespace detector integrated circuit.

1.2 Thesis Overview

The goal of the whitespace detector integrated circuit discussed in this thesis is to tune to a variable frequency band and generate an output that indicates whether a signal or whitespace has been detected in that band. The two main components used to build the whitespace detector are a narrowband, tunable bandpass filter based on an active inductor, and a receive signal strength indicator (RSSI). The filter's role is to tune to a particular frequency band while the RSSI measures the power level of any signal that may be transmitting in that band. It is designed to operate in the broadcast television frequency band from 70 MHz to 700 MHz because the FCC has proposed to make these frequencies available to unlicensed users [2]. The whitespace detector is fabricated into an integrated circuit.

1.3 Thesis Organization

Chapter 2 discusses the motivation for designing the whitespace detector along with background information leading to the development of the proposed architecture and its

specifications. A literature review of tunable bandpass filters and RSSIs is also given.

Chapter 3 explains the design and implementation of the tunable bandpass filter that is based on an active inductor. Equations are derived to predict the inductor and filter's behavior. Simulation results, including small signal s-parameter, transient and linearity, are presented to show the filter's performance.

Chapter 4 presents the design and implementation of the receive signal strength indicator (RSSI). The theory behind the circuit's operation is explained, follow by simulation results showing its transient, steady-state and frequency-dependent behavior.

Chapter 5 describes how the bandpass filter and RSSI are combined to create the whitespace detector integrated circuit (IC). The complete IC layout is presented along with system simulation results of the whitespace detector.

Chapter 6 discusses the testing procedure and measurement results for the components of the fabricated whitespace detector IC. The design of a printed circuit board that is used to facilitate the testing of the circuit is included. Measurement results for the bandpass filter and RSSI are presented.

Chapter 7 concludes the thesis by summarizing the research accomplishments and contributions and by providing possible areas for future work and investigation.

Chapter 2

Background and Motivation

The motivation for the design of the whitespace detector circuit in this thesis comes from the desire to locate empty radio bands or "whitespaces". These whitespaces, which are also referred to as "spectrum holes" [3], can be used by wireless devices, enabling more efficient use of the radio frequency (RF) spectrum. With the rapid growth in the number of wireless devices transmitting in the radio spectrum, available frequency resources have become valuable. Recent spectrum auctions net millions or even billions of dollars, as organizations pay for the licenses to use bands of frequency. One of the larger auctions in 2001 netted over 16 billion dollars from various organizations for the rights to 35 MHz of the broadband PCS (Personal Communications Service) spectrum near 1.9 GHz in different regions of the United States [4]. The objective of whitespace detection is to enable time variant spectral use. This means that different transmitters can be using the same band of frequency at different times.

Over the past century, the use of transmitters in the RF spectrum has been strongly regulated [1]. In order to be allowed to transmit in many frequency bands, such as the broadcast television band below 900 MHz [2] and the broadband PCS band around 1.9

GHz [4], transmitters have to be licensed to do so. The exclusiveness of this regulation is to ensure that transmitters do not interfere with each other. However, having one exclusive user of a resource that is not necessarily being used all of the time is inefficient. Due to the number of users of the frequency spectrum, including satellite, radio and television broadcasters, and cellular phones, the lower frequency bands from 50 MHz to 5 GHz are heavily used. With the continued growth of the usage of wireless devices such as personal digital assistants (PDA) and wireless local area networks (WLAN), more spectrum space will be required but it is becoming more expensive to obtain. Due to the increase in potential users there is a looming RF spectrum resource crisis [1]. This may cause a paradigm shift, leading to the possibility of redefining the way the frequency spectrum is licensed and allocated. One possible solution is to allow unlicensed users to share portions of the frequency spectrum with those to whom it is licensed. This concept of sharing resources is a much more efficient way of handling the coming spectrum shortages and will encourage continued growth in wireless networks [5]. Frequency bands such as the 2.4 GHz ISM (industrial, scientific and medical) already work with unlicensed users in a shared frequency environment.

The Federal Communications Commission (FCC) has recently set forth a proposal that will encourage more efficient use of the radio frequency spectrum by allowing unlicensed broadband wireless devices to reuse the frequencies allocated to licensed users [2]. Specifically, the FCC's proposal would make the television broadcast bands between 76

MHz and 698 MHz available for unlicensed users. The FCC's motivation in this proposal is to promote new wireless applications in the frequency spaces that are made newly available to the unlicensed users. Their choice of the broadcast television bands is because these frequencies offer better propagation characteristics than the higher frequencies (2.4 GHz and 5 GHz bands) that are currently used by unlicensed broadband devices [2].

The potential applications using these newly available frequency bands can include those that are similar to Bluetooth and IEEE 802.11b (Wi-Fi) users. These include products such as wireless headsets for cellular phones, wireless Internet devices and wireless peripherals for computers, such as keyboards and printers [2]. Many of the potential products will be for low power and short distance applications such as laptops, PDAs, WLAN devices and other portable personal wireless devices. Another possible application will be for higher power and larger distances, such as providing fixed access broadband services to homes and businesses by wireless internet services providers (WISP) [2]. Any spectrum space that will be made available can lead to a large number of new unlicensed users.

The limitation to the shared spectrum is that the unlicensed users will only be allowed to transmit in a given frequency band when the licensed user of the band is not transmitting. Otherwise, the unlicensed device would cause interference to the band's primary user. Though the broadcast television bands are all licensed out, they are not all used in a given geographical region and at a given time. Any device that would

choose to use one of these frequency bands would first have to detect whether the band is presently being used or if it is available for use. Along with this detection of unused bands, an entire protocol must be developed to govern how the unlicensed users will use these frequency bands without causing interference for the licensed users. The unlicensed device would also have to monitor whether the licensed user has begun to transmit in the frequency band and, if so, the unlicensed device would have to find another vacant band. In order to determine whether a particular frequency band is available for its use, the FCC states that an unlicensed device would have to use "smart radio" technology to make such decisions [2]. These smart radio technologies have recently found great interest in the area of cognitive radios and software defined radios [6–10].

A software radio is a radio implemented predominantly in software. This manner of implementation allows the radio to be flexible and adaptable. For example, it can function over multiple bands and under multiple protocols. Most of the components of the radio run on a microprocessor [6]. For high performance applications, this is not always practical, leading to the design of the software-defined radio (SDR). In a SDR, the higher performance is achieved by implementing the radio with a combination of hardware and software. This can include application specific integrated circuits (ASIC), field programmable gate arrays (FPGA), digital signal processing (DSP) and software on a microprocessor [6].

From an SDR, a cognitive radio can be designed that has a level of reasoning that allows it to observe its environment and make decisions based on these observations and

its knowledge of its own hardware and software capabilities. Based on these decisions, the radio's behaviour can be changed to give the desired performance [7]. Where the typical radio simply transmits at a particular frequency, the cognitive radio can adapt [6]. This makes the cognitive radio more efficient and able to be used in more environments, especially changing ones. Its adaptability allows it to provide better service to its user, even learning the user's preferences as it goes [8]. A cognitive radio can work over a wide range of frequencies and under conditions that require spectrum sharing, as with the FCC's proposed sharing of the broadcast television band [2]. The cognitive radio must be able to adapt to operate at different frequencies and amplitude levels as well as have the intelligence to understand the protocols or rules that ensure that the radio does not create undesired interference in a band where somebody else is the primary user [6].

Though much of the intelligence of the cognitive radio is implemented with software, there are many specialized hardware components that make it a true System-on-Chip (SoC) design. It will likely combine various sensing circuitry with multi-band RF circuitry [9]. A large part of this sensing circuitry may be used to ensure that the radio will not cause interference for other users. One aspect of the sensing will be to locate spectrum holes [10].

The cognitive radios that will be incorporated into all unlicensed devices will require a means of sensing available frequency bands. These available bands, known as "spectrum holes" or "whitespaces", are licensed bands of frequency that are not used by the primary user at a particular time and in a given geographic location [3]. The FCC has suggested

several possible sensing methods, one of which applies to the whitespace detector circuit in this thesis. In this method, the unlicensed transmitter would check the particular channel for a signal above a certain threshold. If a signal is found above the threshold, it would then look for another channel; otherwise, it could transmit in the given channel. The detector would have to be sensitive to small signals but would not have to be concerned with decoding the signals, just locating them. They could, for example, locate the television carrier. As of the writing of this thesis, a decision has not been made by the FCC to determine the specifics of this threshold [2].

2.1 Proposed Whitespace Detector Architecture

The scope of this thesis encompasses the design of circuitry that will assist an unlicensed device in determining whether a given frequency band is being used or whether it is available. The circuitry is designed as an application specific integrated circuit (ASIC) and its function is to tune to a particular frequency channel and output a signal that can be used to decide if a signal is present in that channel or whether that channel is "whitespace". Since the goal of the whitespace detector is to detect the presence or absence of power in a band, and not to receive and decode information, a complete RF front end is not required. The whitespace detector, shown in Figure 2.1, has two main circuit components. The first is a tunable, high quality factor bandpass filter, which is used to tune to a particular frequency band and filter out all others. The second is a receive signal strength indicator (RSSI) whose role is to determine the power level of any signals in the band to which the filter has been tuned. Based on the RSSI output a

decision can be made as to whether the band is in use or if it is whitespace.

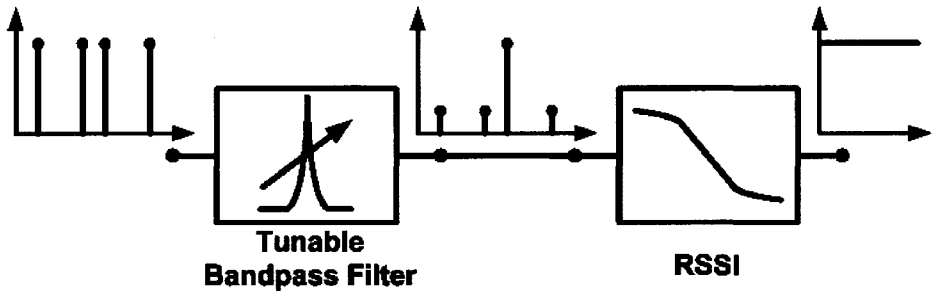

Figure 2.1: Block diagram of the proposed whitespace detector architecture.

At the input to the bandpass filter are all of the radio signals that are being transmitted in the area. The filter is tunable and has a high quality factor allowing it to be tuned to a particular, narrow frequency band. The signals in this band are amplified at the filter output while all other signals are suppressed. The RSSI then gives an output that is proportional to the power of the signal that is passed through the filter. When used to locate whitespace, the filter would tune to a channel that has no signal present to amplify and the RSSI would give on output indicating a very low or absent signal in that band. Some digital circuitry could then be used to interpret the RSSI output, having a threshold value for deciding if a signal was located in the band or if it is whitespace. Once a decision has been made for a particular channel, the filter can be retuned to another channel where another decision can be made. In this way, the whitespace detector can be tuned to each of the channels in a wide band and create a list of which channels are available whitespace and which channels are occupied and therefore, unavailable. This list can be continuously updated, or updated as required, to monitor the channels in case they become used by a primary user. Based on the

output of the whitespace detector and the frequency landscape provided by this list, an unlicensed device incorporating a cognitive radio can decide which frequency channel to use for its transmission.

The high quality factor bandpass filter is implemented in a 0.18 μm CMOS technology using a tunable active inductor which is based on the work presented in [11]. The advantage of this topology is that it permits the filter to be tuned to a wide range of frequencies while providing high precision due to the large quality factors achievable with the active inductor. The RSSI is also implemented in the 0.18 μm CMOS technology on the same ASIC as the filter. It is based on a logarithmic amplifier formed by cascaded stages of limiting amplifiers and rectifiers as presented in [12].

Prior to choosing this architecture for the whitespace detector, other alternative potential architectures were examined. One idea was to use a frequency synthesizer and mixer to downconvert the input band to a lower intermediate frequency (IF) and then measure the power at that frequency to see if the band is occupied. The frequency synthesizer would be tuned in order to select the radio frequency (RF) of the desired band to downconvert to the IF. This architecture is shown in Figure 2.2a.

The problem with this architecture is that all other frequencies around the RF also get downconverted to around the IF and it is difficult to measure the power only in the band of interest. To fix this problem, filtering can be used at the RF so that only the signals in the band of interest get downconverted to the IF. This leads to the modification of using a bandpass filter before the mixer, as shown in Figure 2.2b. The

filter would have a center frequency that is tuned so that it tracks with the frequency being downconverted by the mixer. As discussed in the beginning of Chapter 2, the FCC has proposed to open selected television bands for use by unlicensed users. This band of frequencies is approximately 70 MHz to 700 MHz and is the target frequency range for the proposed whitespace detector. The range of frequencies is large in comparison with any particular frequency in the band and would require a frequency synthesizer with a large tuning range in order to downconvert any channel in the band to the IF.

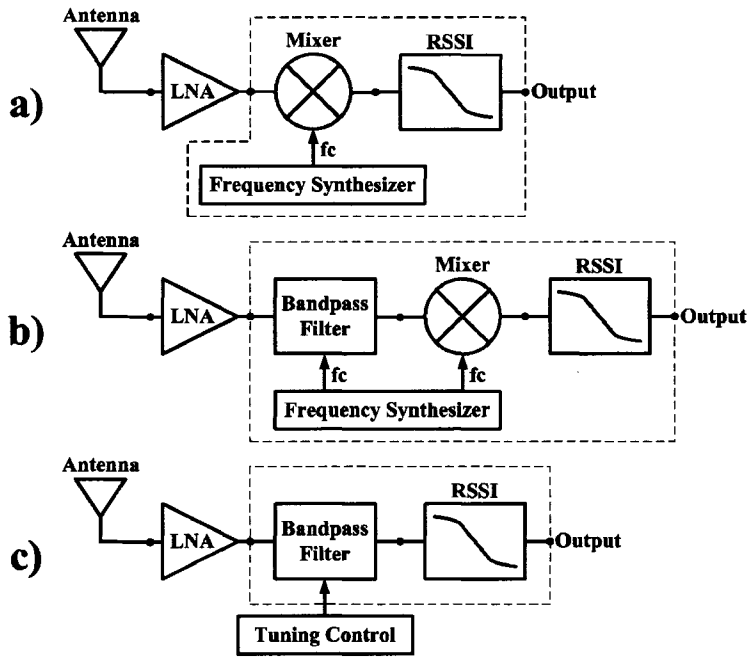

Figure 2.2: Progression of alternative topologies for the whitespace detector. The dashed lines enclose the part of the topology that would be implemented. a) A frequency synthesizer and mixer downconvert the input band to an IF where the power is measured. b) A narrowband filter isolates the band of interest before it is downconverted. c) A narrowband filter isolates the band of interest and the power in the band is measured at the RF without and downconversion.

To simplify the design of the whitespace detector, it was decided to eliminate the downconversion mixer and wide-tuning frequency synthesizer and perform the power

detection at the RF frequency. This leads to the architecture in Figure 2.2c which is implemented in this thesis as shown in Figure 2.1 with the tunable bandpass filter and RSSI as the power detection circuitry. A digital filter, such a finite impulse response (FIR) filter was considered to perform the filtering but the power consumption would be high. An analog filter that uses an on-chip spiral inductor would take up too much area and not have a quality factor large enough to perform the required filtering. The active inductor topology was chosen for the bandpass filter due to its large quality factor, tunability and low power consumption. The active inductor may contribute more noise than a passive inductor. However, this is not a primary concern since the whitespace detector aims only to detect the power of a signal in a band, and not to decode the information it carries.

2.2 Whitespace Detector Design Specifications

The FCC's proposed rules presented in [2] helped formulate the targeted specifications for the whitespace detector in this thesis. The specifications could be modified for other applications.

The broadcast television frequency band is separated into channels that are spaced by 6 MHz within the VHF and UHF frequency spectrum. These channels are designated as channels 2 to 69 and use the following frequencies: 54-72 MHz, 76-88 MHz, 174-216 MHz and 470-806 MHz [2]. The FCC has restricted the channels that will be available to unlicensed users to those summarized in Table 2.1 [2].

From this information, the targeted specifications for the whitespace detector are to

Table 2.1: Available Television Channels for Unlicensed Users

Channels	Frequencies	Restrictions
5 - 6	76 MHz - 88 MHz	
7 - 13	174 MHz - 216 MHz	
14 - 20	470 MHz - 512 MHz	(in some locations)
21 - 36	512 MHz - 608 MHz	
38 - 51	614 MHz - 698 MHz	

operate in a frequency band from 70 MHz to 700 MHz and be able to tune to 6 MHz channels. An unlicensed device operating in this band could use one of the available channels or multiple, adjacent unused channels for higher bandwidth applications [2]. When tuned to a 6 MHz channel, the whitespace detector must give an output that allows a decision to be made as to whether the channel has a signal present or whether the channel is whitespace. The signal it may find in the channel could be transmitted by the licensed television station in that band or another unlicensed device that found whitespace and is now using it to transmit. In either of these cases, the decision would be that the band being examined is not available whitespace.

Regulations would have to be developed to govern how unlicensed devices can use whitespace. For example, there could be rules on the bandwidth they are permitted to use. The system designed in this thesis is intended to work with 6 MHz channels, but this does not have to be the bandwidth limitation. If users require less bandwidth, they could use a whitespace detector that is capable of locating smaller chunks of available spectrum. Similarly, if the user requires more bandwidth, its whitespace detector would have to look for a larger chunk of whitespace. The channel searching bandwidth of the whitespace detector could be designed to meet the bandwidth needs of the individual

users or it could be made adjustable. The 6 MHz target bandwidth for the whitespace detector in this thesis is a lower limit since larger bandwidths can also be achieved.

Television receivers must be able to receive signals as low as -83 dBm and as high as -15 dBm [13]. The FCC had not yet set a signal strength threshold for allowing unlicensed transmission at the time of this work [2]. Therefore, the lower limit of the television signals are used as a guideline for determining the specification for the signal range over which the whitespace detector will operate. Since the whitespace detector is simply looking for the presence or absence of a signal, the upper end of the range is not as important for signal detection. Once a signal of appreciable strength is located it does not really matter how strong the signal is but rather that it is present. However, the large signals are a potential concern for reasons of linearity and issues that may arise with blockers. For reference, -83 dBm to -15 dBm signals are equivalent to peak input voltages ranging from 22.4 μV to 56.2 mV, in a 50 Ω system, based on

$$P_{dBm} = 10log\left(\frac{(V_{peak})^2}{2R(10)^{-3}}\right) \tag{2.2.1}$$

from [14, p.3]. Blockers are high power signals in a frequency band that is close to the band being examined for whitespace. Their high power and close proximity make them difficult to suppress with a filter. The filter would require a very large quality factor to suppress the blocker and be able to detect a potential signal of interest. The implication of this for the design of the whitespace detector is that potential bands of whitespace can go undetected if they are in close proximity to a large blocker. A discussion of the issues with blockers is presented in Section 3.3.8.

The whitespace detector in this thesis is designed to be a 50 Ω system. Though television systems operate in a 75 Ω environment, 50 Ω is used to simplify testing of the whitespace detector in a 50 Ω test environment.

Based on the overall specifications for the whitespace detector, the targeted specifications for the two major circuits are set. Table 2.2 summarizes the targeted performance specifications for the design of the tunable bandpass filter.

Table 2.2: Specifications for the Design of the Tunable Bandpass Filter

Specification	Targeted Performance
Center Frequency Range	70 MHz to 700 MHz
3 dB Bandwidth at Center Frequency	< 6 MHz
Minimum Input Signal (Sensitivity)	-83 dBm (22.4 μV_{peak} in 50 Ω system)
Linearity (IIP3)	High
Power Consumption	Low
Circuit Area	Small

Table 2.3 summarizes the targeted performance specifications for the design of the RSSI. The RSSI's input is the output of the bandpass filter. Its main specification is to provide a logarithmic input-to-output relationship over the range of output voltages from the tunable bandpass filter. Simulation results of the bandpass filter output presented in Chapter 3 provide the dynamic range specification shown in Table 2.3. The output range of the bandpass filter is found to be -60 dBm to -10 dBm.

Table 2.3: Specifications for the Design of the Receive Signal Strength Indicator

Specification	Targeted Performance
Frequency Range	70 MHz to 700 MHz
Input Dynamic Range	-60 dBm to -10 dBm
Power Consumption	Low
Circuit Area	Small

The overall performance of the whitespace detector will be judged on its ability to distinguish between a signal or whitespace in a 6 MHz channel.

2.3 Literature Review of Active Inductor Based Band-pass Filters

Integrated circuits such as oscillators, filters and amplifiers may employ inductors. Typically, these inductors are implemented using large, on-chip spiral structures, or discrete off-chip components are used. Recent research has examined on-chip active inductors as a substitute to off-chip inductors or spiral inductors. Active inductors offer higher achievable on-chip inductances and higher quality factors while requiring a significantly smaller chip area than conventional spiral inductors [15, 16]. In addition, both the inductance and quality factor of active inductors can be tuned. Active inductors have the limitations of poor linearity and higher noise than traditional inductors [11, 17], making them not suitable for applications where there are tight requirements in these areas. The advantages and disadvantages of active inductors compared to on-chip passive inductors are summarized in Table 2.4.

Table 2.4: The Advantages and Disadvantages of Active Inductors Compared to On-Chip Spiral Inductors

Advantages	Disadvantages
Higher inductance values	Lower linearity
Higher quality factors	Higher noise
Smaller chip area	Higher power
Tunable inductance and quality factor	

Work has been done to create active inductors from transistors in GaAs technologies

[16, 18, 19], bipolar [20] and CMOS technologies [11, 15–17, 21–29]. Tunable oscillators using active inductors are presented in [23, 24]. In [23], the inductance of the active inductor is tuned from 9.6 nH to 56 nH with quality factors greater than 100, allowing the oscillator to function from 1.73 GHz to 2.07 GHz. Varying bias currents to the active inductor in [24], tunes the oscillator's frequency from 450 MHz to 1.16 GHz. A low noise amplifier (LNA) is presented in [25] that uses a CMOS active inductor load and it is compared to an LNA with a spiral inductor load that uses 25% more chip area. The design of a CMOS broadband amplifier with high quality factor active inductors is presented in [26]. Much research describes the use of active inductors in implementing tunable bandpass filters [11, 17, 22, 27–29].

The realization of integrated on-chip filters are a challenge in the complete integration of RF front ends due to the low quality factor and large size of on-chip inductors. In [30–32], tunable bandpass filters are presented that use on-chip spiral inductors and quality factor enhancing circuitry. These circuits have the advantage of being tunable in both frequency and quality factor but still rely on large, on-chip inductors. The on-chip, tunable bandpass filters in [11, 17, 22, 27–29] can be tuned in both center frequency and quality factor while being much smaller due to the use of active inductors.

The performance of several recent active inductor designs presented in the literature is summarized in Table 2.5. Table 2.6 summarizes the performance of bandpass filters that have been built using active inductors and presented in recent publications. The author of [11, 21, 22] has done work on single-ended and differential CMOS active inductors and

has also shown their application in bandpass filters and amplifiers. The inductor and bandpass filter presented in [11] is the basis for this thesis work. A goal of these works is to create active inductors with larger quality factors. An extra transistor is added to the feedback path of the active inductor presented in [11] to act as Q-enhancement circuitry. The inductor achieves quality factors up to 434 compared to those below 10 for similar architectures without the Q-enhancement circuitry. Linearity remains a limitation in this design and a maximum output voltage of only 4.5 mV is achieved with less than 1 % total harmonic distortion. The same author presents a fully-differential active inductor in [21].

Table 2.5: Performance of Active Inductors Presented in the Literature

Ref.	Tech.	Power	Inductive Bandwidth	Inductance Range	R_S	Quality Factor	Max. Output Voltage
[11]	0.35 μm CMOS	0.6 mW	6.8 MHz - 2.97 GHz	30.9 nH @ 1 GHz	1.16 Ω @ DC	434 @ 1 GHz	4.5mV
[21]	0.35 μm CMOS	1.2 mW	10 MHz - 2.8 GHz	70 nH $\pm$20%	N/A	1970 @ 1.08GHz	30mV_{pp}
[20]	0.18 μm BiCMOS	15 mW	N/A	up to 40 nH	N/A	up to 10	N/A
[19]	1μm GaAs MESFET	90 to 240mW	100 MHz - 1 GHz	65 nH to 110 nH	-5.6 to 20.8 Ω	N/A	N/A
[22]	0.8 μm CMOS	N/A	up to 1 GHz	100's of nH	N/A	> 100	13.5mV

In [20] a bipolar active inductor designed in a BiCMOS technology is presented. Though the quality factor of this inductor would not be large enough for a high precision bandpass filter, its feasibility for tuning the input and output impedance of RF circuits in a multi-mode transceiver is presented. An active inductor designed in a GaAs MESFET

technology is presented in [19]. It can achieve low series resistances and a wide range of inductances but it requires at least six times more power than the other designs.

Table 2.6: Performance of Active Inductor Based Band Pass Filters Presented in the Literature

Ref.	Description	Tech.	Power	Center Frequency Range	Filter Quality Factor	IIP3 or DR
[11]	C_{filt} = 0.7pF	0.35 μm CMOS	0.6 mW	0.93 - 1.03 GHz	> 25	DR = 30dB @ 1GHz, Q=25
[29]	Differential	0.35 μm CMOS	17 mW	400 MHz - 1.1 GHz	2 to 80	IIP3 = -15dBm @ Q = 40
[22]	C_{filt} = 0.7pF	0.8 μm CMOS	N/A	around 500 MHz	80 @ 500 MHz	N/A
[17]	6th order G_m-C	0.5 μm CMOS	90 mW	around 70 MHz	350 @ 70 MHz	IIP3 = -10dBm

In [22] the bandpass filter based on a CMOS active inductor is shown to have a high quality factor of 80 operating with a center frequency around 500 MHz. In [11], a similar topology is used in a smaller, 0.35 μm CMOS technology for a filter operating around 1 GHz and using 0.6 mW of power. Both of these designs use a capacitor in series with the input of the inductor to create the bandpass filter.

A differential bandpass filter in [29] is shown to achieve quality factors up to 80 and a 700 MHz frequency range around a nominal frequency of 900 MHz. It requires 28 times more power than the filter in [11] but can achieve an IIP3 of -15 dBm, using symmetrical and unbalanced differential pairs. Input and output buffers are designed to interface the fabricated circuit with 50 Ω test equipment.

The sixth order filter in [17] operates around 70 MHz and can reach a quality factor of 350. Its IIP3 of -10 dBm is 5 dB better than the next best filter presented but it

requires 5 times more power. The improved performance and higher power are due to the fact that it is a sixth order filter based on three cascaded second order filters. Automatic tuning circuitry is also designed for the filter. It consumes an additional 30 mW of power but allows the filter to be automatically tuned in both frequency and quality factor.

2.4 Literature Review of Receive Signal Strength Indicators

Table 2.7 shows the performance of several receive signal strength indicators (RSSI) presented in the literature. These designs have a similar architecture to the RSSI presented in this thesis, being built as a logarithmic amplifier with cascaded limiter and rectifier stages. In [12], two similar RSSIs are presented for application in Bluetooth receivers, operating at the Intermediate Frequency (IF) of 3 MHz. One is designed in a 0.5 μm CMOS technology and the other in a 0.35 μm CMOS technology. The design in the 0.35 μm technology requires 25% less power and has a 27% higher 3 dB bandwidth. The advantage of these designs is their ability to work with low power. Special limiting amplifiers and rectifier topologies were designed to operate with low supply voltages.

The RSSI presented in [33] uses almost twice the power of the first design. However, its dynamic range is 10 dB larger and its input sensitivity is 18 dB lower. It can also operate up to a higher frequency of 70 MHz and has ± 2 dB better logarithmic linearity. For low voltage operation, the limiters in this design use folded diode loads versus conventional cascode diode loads. The rectifiers use an open-loop current mode

Table 2.7: Performance of Received Signal Strength Indicators Presented in the Literature

Ref.	Tech.	Power	Area	Gain/Stage # of Stages Total Gain	Input Dynamic Range	3 dB Band-width	Error
[12]	0.35 μm CMOS	3.2 mW	0.48 mm^2	9.3dB $\times$ 7 = 65 dB	-60 dBm to 5 dBm	23MHz	$\pm$3dB
[12]	0.5 μm CMOS	4.3 mW	0.49 mm^2	9.3dB $\times$ 7 = 65 dB	-60 dBm to 5 dBm	18MHz	$\pm$3dB
[33]	0.6 μm CMOS	6.2 mW	0.4 mm^2	12dB $\times$ 7 = 84 dB	-78 dBm to -3 dBm	70MHz	$\pm$1dB
[34]	0.35 μm CMOS	69 mW	N/A	12dB $\times$ 7 = 84 dB	-83 dBm to -3 dBm	110MHz	$\pm$0.7dB
[35]	0.6 μm CMOS	15 mW	0.36 mm^2	80dB	68 dB	292MHz	$\pm$1dB

structure to achieve low power operation from a 2 V supply or less.

The RSSI presented in [34] requires more than 20 times the power of the lowest power design, though it also includes a programmable gain amplifier. Its quoted area includes pads and other circuitry and thus is not suitable for comparison. The advantages of this design are its wider dynamic range of 80 dB, lower input sensitivity of -83 dBm, higher 3 dB bandwidth of 110 MHz and better logarithmic accuracy of $\pm$0.7 dB. A problem that is identified and resolved in this design is the large gain variation of 6 dB to 15 dB in the gain stages of the RSSI due to process variations. This problem is fixed with the design of gain control bias circuitry, at the expense of more power and area.

The final RSSI in Table 2.7, presented in [35], operates up to a higher frequency of 292 MHz and occupies a similar area than the others. It uses almost 5 times more power than the lowest power design. A problem presented with this design is that measured results only show the RSSI operating down to -50 dBm while simulations works down

to -100 dBm. No explanation is presented for this inconsistency.

2.5 Chapter Summary

The concept of the whitespace detector is introduced in this chapter. It is a circuit that can be used to locate unused bands in the frequency spectrum. These vacant bands are licensed to particular users but they can be shared with unlicensed users. Spectrum sharing can increase the efficiency of spectrum use. Various architectures for the whitespace detector are examined and the one chosen for implementation uses a tunable bandpass filter based on an active inductor, along with a receive signal strength indicator. This circuit will tune to a chosen frequency band and determine if that band is in use based on the received signal strength within that band. Specifications for the performance of these circuits are laid out for operation of the whitespace detector in the television frequency band from 70 MHz to 700 MHz. The Federal Communications Commission has proposed making these licensed frequencies available for use by unlicensed users. A literature review of the state-of-the-art in active inductor-based bandpass filters and receive signal indicators is presented. This leads toward the development of the chosen topology for the application in the whitespace detector.

Chapter 3

Tunable Bandpass Filter with Active Inductor

A key component required for the implementation of the whitespace detector circuit is an on-chip, tunable bandpass filter with a high quality factor. For applications in the broadcast television frequency bands that the Federal Communications Commission (FCC) proposes to release to secondary users, the filter must be able to tune to channels from 70 MHz to 700 MHz [2]. Within this frequency band, the television channels are spaced by 6 MHz. In order to accurately tune to a particular channel, the 3 dB bandwidth of the band pass filter response is desired to be 6 MHz or less. This requires a quality factor as high as 120 for operation at 700 MHz. At 70 MHz, a quality factor of 12 is required to give a 6 MHz dB bandwidth. The filter should be sensitive to signals as low as -83 dBm as set in the specifications in Chapter 2.

The topology used to implement the bandpass filter is based on a CMOS transistor-only active inductor [11]. This topology offers a number of advantages over alternative inductor implementations. For one, it can be created on-chip, as opposed to using

off-chip discrete inductors. The transistor-only active inductor requires a significantly smaller die size when compared to conventional on-chip spiral inductors and can achieve higher inductance values. For example, a 9 nH planar spiral inductor can require an area of 36000 μm^2 [36], while active inductors, such as the one designed for this thesis, can achieve hundreds of nanohenries in less than five percent of the area. In addition to the large size of on-chip spiral inductors, they also have the disadvantages of being difficult to model in simulations and having low quality factors. In contrast, the transistor-based active inductor is more easily modelled and can achieve high quality factors that can be into the hundreds [11]. When used in a bandpass filter, these high quality factors allow for a very sharp filter response. The active inductor offers tunability in both inductance and quality factor, allowing the frequency, gain and bandwidth of the bandpass filter to be adjusted. This makes the CMOS transistor-only active inductor an appropriate choice for designing the on-chip bandpass filter for the whitespace detector circuit. Active inductors suffer from poorer noise performance than passive inductors, but in this application, it is not as much of a concern since determining the presence or absence of a signal is the objective, not determining the information carried by the signal. Active inductors also have the potential to have problems with linearity and instability when their high quality factors lead to high gain [37].

The active inductor that is implemented in the whitespace detector's tunable bandpass filter follows from the work in [11]. The active inductor presented in this thesis is created in a 0.18 μm CMOS technology instead of a 0.35 μm technology and it is used to

make a bandpass filter with a 630 MHz frequency tuning range, compared to 100 MHz in [11].

In Section 3.1, theory to predict the performance of the active inductor and tunable bandpass filter is developed. Sections 3.2 and 3.3 discuss the circuit design, implementation, layouts and simulation results of the active inductor and bandpass filter, respectively. The performance of the circuits is summarized and compared to the literature in Section 3.4.

3.1 Active Inductor and Tunable Bandpass Filter Theory

3.1.1 Active Inductor Theory

The basis for the active inductor design is a gyrator circuit [37]. The advantage of the gyrator is that it can be implemented on an integrated circuit using transistors. The transistors act as transconductors and adjustments to their bias points allow their transconductances to be tuned [37]. A conceptual representation of a gyrator based on two transconductors is shown in Figure 3.1. Transconductor 1 provides a negative transconductance, g_{m1}, meaning its current flows into the transconductor when a positive voltage is applied at its input. Transconductor 2 provides a positive transconductance, g_{m2}, meaning its current flows out of the transconductor when a positive voltage is applied at its input [11]. When a grounded capacitor, C, is connected to the output of the gyrator in Figure 3.1, the input impedance of the gyrator can be expressed as

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} = \frac{sC}{g_{m1}g_{m2}}. \tag{3.1.1}$$

This input impedance looks like an inductor with one terminal attached to ground, having an inductance given by

$$L = \frac{C}{g_{m1}g_{m2}} \tag{3.1.2}$$

as shown in [37].

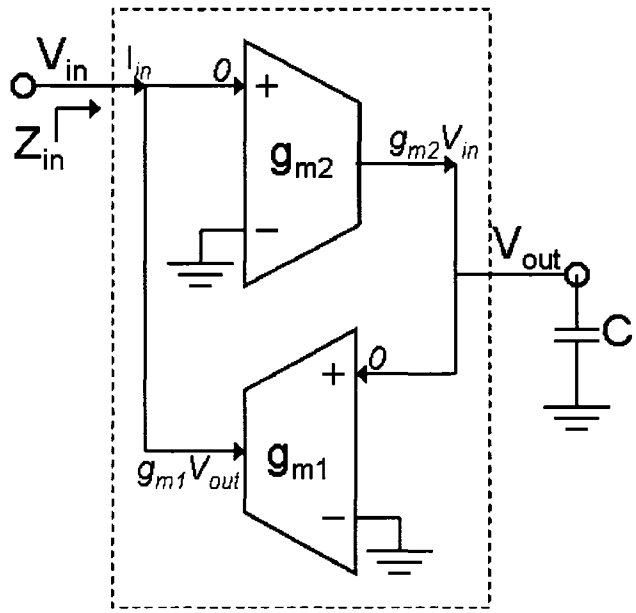

Figure 3.1: Gyrator block diagram.

In a CMOS technology, the two transconductors in Figure 3.1 can be implemented using a number of combinations of PMOS and NMOS transistors. To form the negative transconductor, the transistor can be connected in a common-source amplifier configuration. Common-drain or common-gate configurations can be used to implement the positive transconductor [11]. The schematic for the whitespace detector's active inductor can be seen in Figure 3.2. A PMOS common-source amplifier, M2, is selected for the negative transconductor and a PMOS common-gate amplifier, M3, is chosen for the

positive transconductor. The third transistor, M1, in Figure 3.2 is an NMOS transistor that is used to reduce the series resistance of the inductor by increasing the loop gain [11]. This allows the achievable quality factor of the inductor to be increased.

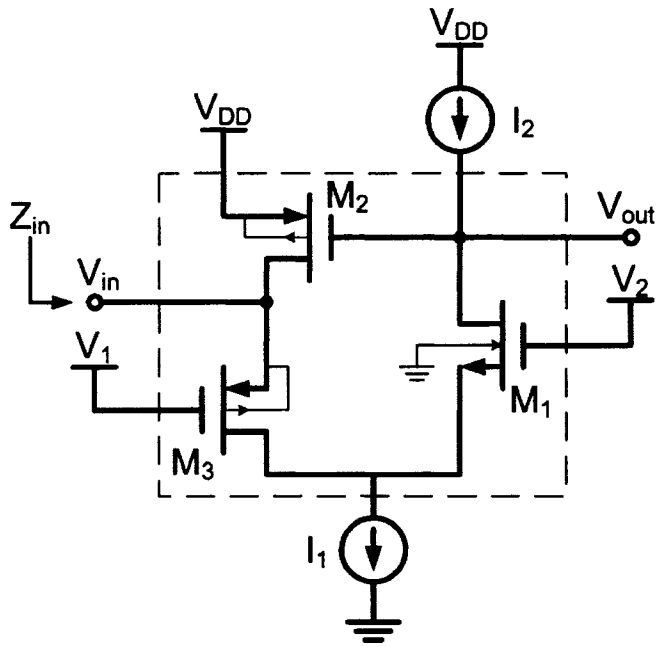

Figure 3.2: The active inductor circuit.

The simplified, generic formulas for the input impedance and inductance of the gyrator-based active inductor can be seen in Equations 3.1.1 and 3.1.2, respectively. A more accurate relation for the input impedance of the active inductor in Figure 3.2 can be derived using the high frequency small signal representation of the circuit. A schematic of the small signal model can be seen in Figure 3.3. Transistors M2 and M3 have their bulk connected to their source, removing any capacitance between these nodes. The capacitances connected to the bulk of M1 are considered.

The circuit in Figure 3.3 can be rearranged and simplified as shown in Figure 3.4.

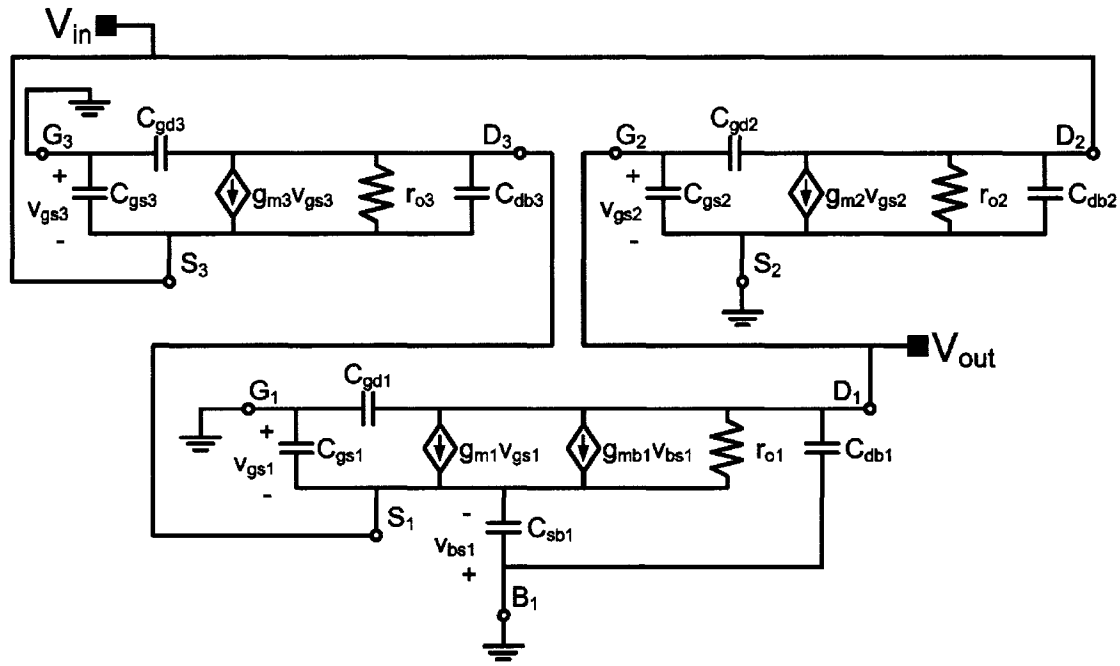

Figure 3.3: High frequency small signal model of the active inductor.

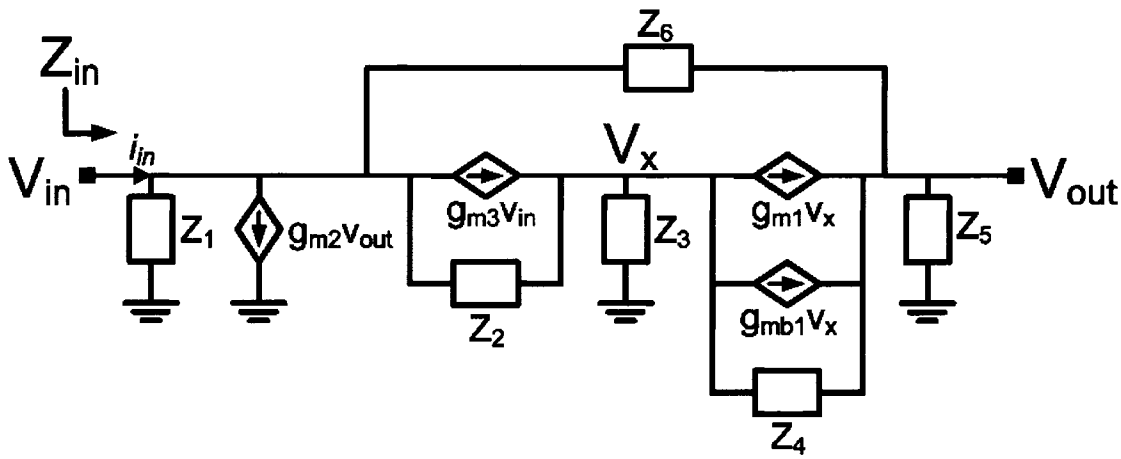

Figure 3.4: High frequency small signal model of the active inductor with simplified impedances.

In this circuit, V_{in} = -V_{gs3}, V_{out} = V_{gs2} and V_x = -V_{gs1} = -V_{bs1}. The impedance blocks, which are the combination of parallel resistors and capacitors, are represented by Equations 3.1.3 through 3.1.8.

$$Z_1(s) = \frac{r_{o2}}{s(C_{db2} + C_{gs3})r_{o2} + 1} \tag{3.1.3}$$

$$Z_2(s) = \frac{r_{o3}}{sC_{db3}r_{o3} + 1} \tag{3.1.4}$$

$$Z_3(s) = \frac{1}{s(C_{gd3} + C_{sb1} + C_{gs1})} \tag{3.1.5}$$

$$Z_4(s) = r_{o1} \tag{3.1.6}$$

$$Z_5(s) = \frac{1}{s(C_{db1} + C_{gd1} + C_{gs2})} \tag{3.1.7}$$

$$Z_6(s) = \frac{1}{sC_{gd2}} \tag{3.1.8}$$

To determine the inductance of the circuit, the input impedance, $Z_{in} = v_{in}/i_{in}$, can be found by solving the nodal equations for the circuit in Figure 3.4. These are given by Equations 3.1.9, 3.1.10 and 3.1.11 for nodes V_{in}, V_x and V_{out}, respectively.

$$-i_{in} + \frac{v_{in}}{Z_1} + g_{m2}v_{out} + g_{m3}v_{in} + \frac{v_{in} - v_x}{Z_2} + \frac{v_{in} - v_{out}}{Z_6} = 0 \tag{3.1.9}$$

$$-g_{m3}v_{in} + \frac{v_x - v_{in}}{Z_2} + \frac{v_x}{Z_3} + g_{m1}v_x + g_{mb1}v_x + \frac{v_x - v_{out}}{Z_4} = 0 \tag{3.1.10}$$

$$\frac{v_{out}}{Z_5} + \frac{v_{out} - v_{in}}{Z_6} - g_{m1}v_x - g_{mb1}v_x + \frac{v_{out} - v_x}{Z_4} = 0 \tag{3.1.11}$$

The nodal Equations 3.1.9 through 3.1.11 are solved for the input impedance of the active inductor using the Maple mathematical software tool. A few simplifications are made to this expression, yielding Equation A.1.1 in Appendix A. These simplifications include removing non-dominant capacitances from impedance equations 3.1.3 through

3.1.8. In Equation 3.1.3, $C_{gs3} \gg C_{db2}$, allowing C_{db2} to be eliminated from the equation. Similarly, C_{sb1} is removed from Equation 3.1.5 and C_{db1} is removed from Equation 3.1.7, since they are orders of magnitude smaller than the other capacitances in these equations. Equation 3.1.4 reduces to $Z_2(s) = r_{o3}$ since the imaginary term in the denominator is much less than 1 for frequencies below 50 GHz. Further simplification involved eliminating any terms that were added together which were more than 100 times smaller than the dominant term in the addition. The resulting simplifications give the more manageable Equation A.1.1. The substitution of simulated operating point values into this equation and the original, non-simplified equation result in an inductance calculation that matches within a few percent for frequencies in the hundreds of MHz range. This shows that the above simplifications that are made are acceptable.

The imaginary part of the impedance from equation A.1.1 gives the inductance of the active inductor and the real part gives its series resistance. Simplified versions of these equations are derived in Appendix A. The imaginary part of the impedance can be simplified, giving the inductance of

$$L = \frac{r_{o1}(C_{gd1} + C_{gs2} + C_{gd2})(1 + r_{o3}[g_{m1} + g_{mb1}]) + r_{o3}(C_{gs1} + C_{gs2} + C_{gd3})}{r_{o1}g_{m2}(g_{m1} + g_{m3}r_{o3}[g_{m1} + g_{mb1}])}. \quad (3.1.12)$$

The real part, when simplified, gives the series resistance expressed as

$$R_S = \frac{1}{r_{o1}g_{m2}(g_{m1} + g_{m3}r_{o3}[g_{m1} + g_{mb1}])}. \quad (3.1.13)$$

For the frequency range of this application (in the 100s of MHz), these simplified equations are accurate to within four percent of the full equation that is derived from the nodal Equations 3.1.9 to 3.1.11.

With further approximation, these equations can be simplified to a form that corresponds closely to the gyrator theory presented in [37] and the inductance and series resistance equation presented in [11]. For the series resistance equation, this can be done by ignoring g_{mb1} then simplifying based on the fact that $g_{m1} < g_{m1}g_{m3}r_{o3}$. These simplifications result in the series resistance of

$$R_s = \frac{1}{r_{o1}r_{o3}g_{m1}g_{m2}g_{m3}} = \frac{g_{ds1}g_{ds3}}{g_{m1}g_{m2}g_{m3}}. \tag{3.1.14}$$

This is equivalent to the equation presented in [11]. The simplifications leading to Equation 3.1.14 result in up to a 30% loss of accuracy. Equation 3.1.14 is useful for predicting trends in the resistance but for a more accurate calculation of the series resistance, Equation 3.1.13 must be used.

The inductance Equation 3.1.12 can be simplified more by using numerical analysis to eliminate the non-dominant terms in the numerator and simplifying the denominator in the same way that is done for the series resistance equation. The result of these simplifications is

$$L = \frac{C_{gd1} + C_{gs2} + C_{gd2}}{g_{m2}g_{m3}}. \tag{3.1.15}$$

This equation loses up to 50% of the accuracy of Equation 3.1.12 but allows trends to be easily identified and examined. This equation agrees with the one described in [11] except that Equation 3.1.15 accounts for additional capacitances, leading to a more accurate calculation. Though Equation 3.1.15 is useful for examining trends in the inductance, the more accurate Equation 3.1.12 is used to calculate inductance to compare with simulated results in Section 3.2.2.

The quality factor of the inductor can be calculated as

$$Q = \frac{|Im(Z_{ind})|}{|Re(Z_{ind})|} = \frac{\omega L}{R_s} \tag{3.1.16}$$

using the inductance, L, and series resistance, R_s [14].

In order to examine the trends of how the bias currents and voltages in the active inductor effect its inductance and resistance, Equations 3.1.14 and 3.1.15 are used. These simplified equations are reasonable for examining trends.

The capacitances, $C_{gd1} + C_{gs2} + C_{gd2}$, in Equation 3.1.15 are the dominant capacitances at the output of the active inductor as seen in Figure 3.3. These capacitances are related to the size of transistors, M1 and M2, and will vary little during the normal operation of the active inductor. Therefore, the main parameters that allow for the tuning of the active inductor are the transconductances, g_{m2} and g_{m3}. For the PMOS transistors, M2 and M3, which are operating in saturation, the transconductance can be described by

$$g_m = \sqrt{2\mu_p C_{ox} \frac{W}{L} I_D} \tag{3.1.17}$$

where the hole mobility, μ_p, and oxide capacitance, C_{ox}, of the transistors are fixed by the technology while the dimensions of the transistor, W/L, are fixed at the time of the design. This means that the transconductance of the circuit can be varied by changing the DC drain current, I_D, of the transistor. Therefore, the transconductance is proportional to the square-root of the drain current. Since the drain currents in both M2 and M3 are the same, it can be related to the transconductances as

$$g_{m2} g_{m3} \propto I_D. \tag{3.1.18}$$

Examining Equation 3.1.15 leads to the conclusion that the inductance of the active inductor, L, is inversely proportional to the drain current, I_D, in transistors M2 and M3, shown as

$$L \propto \frac{1}{I_D}. \tag{3.1.19}$$

Based on Figure 3.2, the drain current of transistors M2 and M3 can be related to the two bias currents by

$$I_D = I_1 - I_2. \tag{3.1.20}$$

This means that increasing I_1 while keeping I_2 constant will increase I_D and reduce the inductance of the active inductor. Increasing I_2 while keeping I_1 constant will reduce I_D and increase the inductance.

The tuning trend for the series resistance can be seen by examining Equation 3.1.14. In this equation, $g_{ds1} = 1/r_{o1}$ and $g_{ds3} = 1/r_{o3}$ will effect tuning. Changes in g_{m1}, g_{m2} and g_{m3} caused by tuning the bias currents to set the inductance will also effect R_s. With the bias currents and inductance fixed, the series resistance can be tuned by varying g_{ds1} or g_{ds3}. Changing the control voltages, V_1 and V_2 in Figure 3.2 causes a change in the drain to source voltages of transistors M1 and M3, which alters g_{ds1} and g_{ds3} [11]. Assuming that the transistors are in saturation, the relationship between their drain current, I_D, and their gate to source voltage, V_{GS}, can be given by

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_t)^2. \tag{3.1.21}$$

The tuning voltages, V_1 and V_2, are connected to a transistor gate. If this gate voltage is increased while the bias current is held constant, the source voltage increases

so that V_{GS} remains constant and Equation 3.1.21 remains unchanged. The drain voltage does not change so this results in a change in V_{DS}. Since the drain current is constant, this causes r_o and hence g_{ds} of the transistor to change. The overall effect is this: increasing V_{DS} causes a decrease in g_{ds}, which causes a decrease in the series resistance, R_S, of the inductor based on Equation 3.1.14. This increases the quality factor of the inductor. In theory, an infinite quality factor can be obtained by continually reducing R_S but there are limits to the control voltages in order to leave enough voltage headroom for the current sources that bias the active inductor [11]. As described earlier, the addition of the NMOS transitor, M1, allows higher quality factors to be achieved. This can be seen in Equation 3.1.14 where M1 adds a factor of g_{ds1}/g_{m1}. This is always less than 1 because $g_{m1} \gg g_{ds1}$.

3.1.2 Bandpass Filter Theory

The active inductor circuit is shown to have an input impedance that can be represented by an inductor in series with a resistor. A second-order bandpass filter can be created if a capacitor is placed in series with the input of the active inductor and the output is taken from V_{out} in Figure 3.2 [11]. If this is done, the bandpass filter can be represented as shown in Figure 3.5. The inductor, L, and resistor, R_s, represent the inductance and series resistance of the active inductor, respectively.

Solving for V_{out}/V_{in} from Figure 3.5 gives

$$\frac{V_{out}}{V_{in}} = \frac{R_s}{sL + R_s + 1/sC} = \frac{sR_sC}{s^2LC + sR_sC + 1} \tag{3.1.22}$$

which is the transfer function of the bandpass filter with $s = j\omega$.

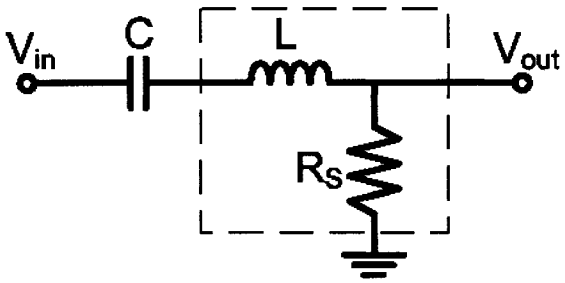

Figure 3.5: Schematic representation of the bandpass filter.

Equation 3.1.22 can be rearranged to the form shown in Equation 3.1.23 [38].

$$\frac{V_{out}}{V_{in}} = \frac{s(R_s/L)}{s^2 + s(R_s/L) + 1/LC} = \frac{a_1 s}{s^2 + s(\omega_0/Q) + \omega_0^2} \tag{3.1.23}$$

From this transfer function, the center frequency, ω_0, quality factor, Q, and 3-dB bandwidth, β, can be found as Equations 3.1.24, 3.1.25 and 3.1.26, respectively.

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.1.24}$$

$$Q = \frac{\omega_0 L}{R_S} = \frac{1}{R_S}\sqrt{\frac{L}{C}} \tag{3.1.25}$$

$$\beta = \frac{\omega_0}{Q} = \frac{R_S}{L} \tag{3.1.26}$$

It is shown in Equation 3.1.19 that the inductance is inversely proportional to the drain current in transistors M2 and M3. By applying this to Equation 3.1.24, the relationship

$$\omega_0 \propto \sqrt{I_D} \tag{3.1.27}$$

can be deduced. The center frequency of the bandpass filter is proportional to the square-root of the drain current in transistors M2 and M3. Thus, the bias currents can be used to tune the center frequency of the bandpass filter.

To tune the quality factor of the bandpass filter based on Equation 3.1.25, R_S can be tuned by varying the input control voltages. This also tunes the 3 dB bandwidth of the filter.

3.2 Implementation and Simulation of the Active Inductor

The gyrator-based active inductor from Figure 3.2 is implemented in a 0.18 μm CMOS technology. The schematic implementation of the circuit is shown in Figure 3.6.

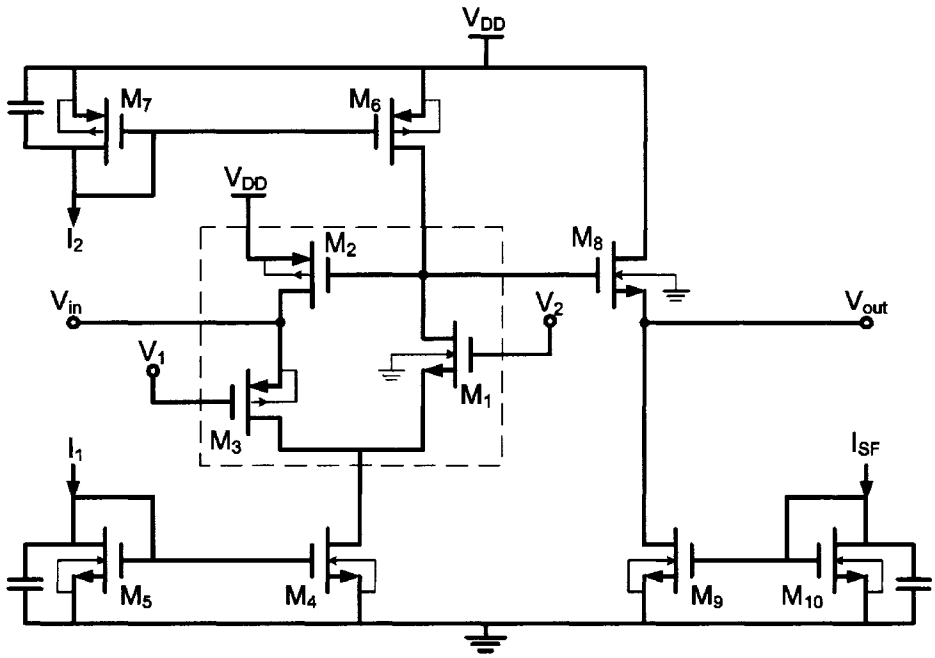

Figure 3.6: Schematic of the active inductor circuit. The core of the active inductor is inside the dashed box.

As discussed in Section 3.1, the core of the active inductor is formed by the negative transconductor, M_2, and the positive transconductor, M_3. M_1 is added to increase the quality factor of the active inductor by reducing its series resistance. The bias current,

I_1 is created by the NMOS current mirror formed from transistors M_4 and M_5. M_6 and M_7 make up a PMOS current mirror that is used to provide the bias current, I_2. The inductance of the active inductor can be tuned by varying the bias currents, I_1 and I_2. The quality factor can be tuned by varying the control voltages, V_1 and V_2. The input to the active inductor is at the source of M_3. When the active inductor is used to create a bandpass filter, the input capacitor is placed in series with this terminal. The output is taken from the gate of M_2. The source follower, M8, and its bias transistors, M9 and M10, are added to the output of the active inductor to provide isolation when interfacing the bandpass filter to other circuits. This extra transistor adds more parasitic capacitances that alter the effective inductance of the circuit, however it lowers the impact that different loads may have on the inductance. Each of the current mirrors has a 950 fF MIM (metal-oxide-metal) capacitor attached between the transistor gates and ground to reduce noise that can be injected on the bias lines. The noise on the bias line comes from any transistors that form current mirrors that feed the circuit. Any time the current is ratioed up, the noise is as well. Noise is also coupled in from the substrate ground as the current bias line travels a long distance on top of it across the chip. The current source that is used to provide the bias current can also contribute noise. Much of this noise is random with respect to frequency and the capacitor forms a low-pass filter that alleviates the high frequency noise. The size of the capacitor is chosen to remove as much noise as possible without being too large to fit in the available chip space.

The sizes of the transistors that make up the active inductor in Figure 3.6 appear in Table 3.1. The starting point for the sizes of active inductor's core transistors, M_1 to M_3, comes from the paper that is the basis for the active inductor design [11]. The design in this paper is done using a 0.35 μm CMOS technology whereas the active inductor designed for the whitespace detector is done in a 0.18 μm CMOS technology. As a result, the transistor widths are scaled proportionally. From the starting point, the transistor sizes are adjusted based on S-parameter simulation results performed in Cadence. These simulations, which are described in more detail in Section 3.2.2, examine the inductance of the active inductor. The transistor sizes are adjusted so that their capacitances and transconductances result in the desired range of inductance values when biasing to the active inductor is tuned.

Table 3.1: Transistor Sizes in the Active Inductor

Transistor	# of Fingers × Width/Finger = Total Width (μm)	Length (μm)
M1	2 × 3.05 = 6.1	0.18
M2	2 × 5 = 10	0.18
M3	4 × 4.75 = 19	0.18
M4	4 × 5 = 20	0.50
M5	4 × 5 = 20	0.50
M6	4 × 5 = 20	0.50
M7	4 × 5 = 20	0.50
M8	2 × 1.6 = 3.2	0.18
M9	4 × 5 = 20	0.50
M10	4 × 5 = 20	0.50

A small width of 3.2 μm and a minimum length of 0.18 μm is chosen for the source follower transistor, M_8, so that its input capacitance does not overwhelm the other capacitances that control the inductance of the active inductor. M_8 is biased with a

current of 250 μA provided from I_{SF}. The bias transistors that form the current mirrors of the active inductor, M_4 to M_7, M_9 and M_{10}, have non-minimum lengths to provide more constant current mirroring even if V_{DS} on both halves of the current mirror is different. A discussed in [38, p.405], a longer channel transistor gives the current mirror a higher output resistance. This means that the transistor's current remains more constant even if its V_{DS} varies. The current mirror transistors have large widths to ensure that they remain in saturation while providing the required range of currents and without requiring too much voltage headroom. I_1 can range from approximately 5 μA to 200 μA while I_2 can range from approximately 2 μA to 30 μA.

3.2.1 The Active Inductor Layout

The layout of the active inductor is shown in Figure 3.7. All of the input and output ports are labelled, as well as each of the components. The transistors that form the current mirror pairs (M_4 and M_5, M_6 and M_7, M_9 and M_{10}) are laid out with interdigitated fingers. This one-dimensional matching technique allows the transistors to be better matched against temperature and doping gradients. It can also be noted that the filtering capacitors on the bias lines take up the majority of the area. This is why their size is limited to 950 fF. From the layout of the active inductor, an extracted version of the schematic is generated. This extracted representation of the circuit includes parasitic capacitances. All simulations that are described in the sections that follow are performed using this post-layout representation of the circuit.

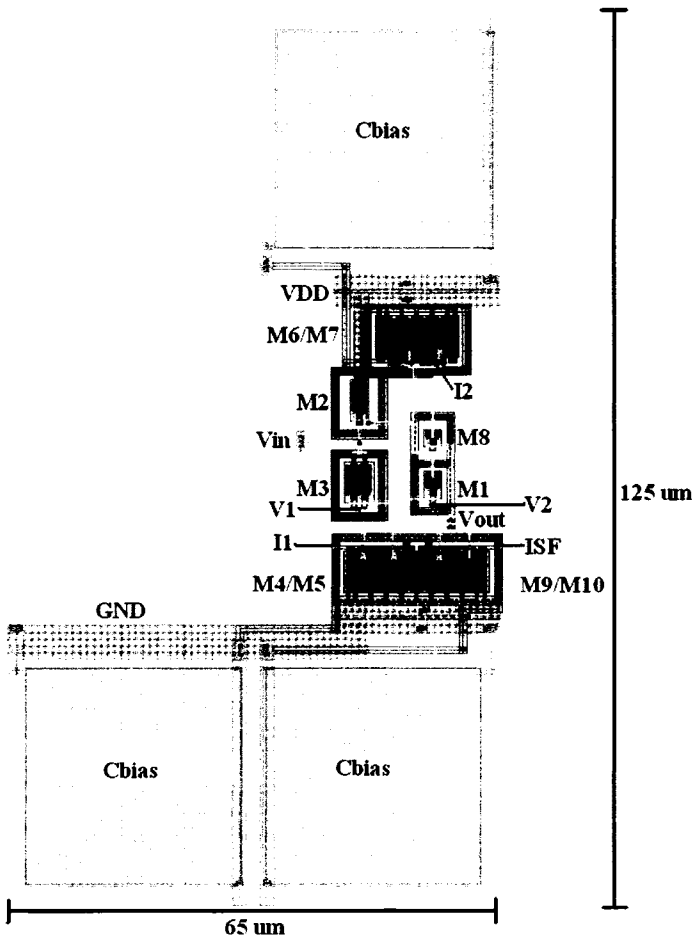

Figure 3.7: The active inductor layout with ports and components labelled. For this layout and all layouts shown in this thesis, there is a layout key in Figure B.1 of Appendix B to identify all layers used in the layout.

3.2.2 Simulating the Inductance of the Active Inductor

S-parameter simulations* are run on the active inductor circuit in Figure 3.6 when extracted with parasitic capacitances to examine the input impedance of the circuit. A schematic of the testbench used to perform S-parameter simulations is shown in Figure 3.8. The 50 Ω ports provide the measurement signals and the coupling capacitors, C_C, ensure the proper biasing is maintain within the device under test (DUT).

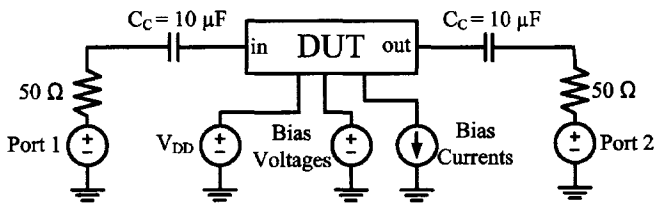

Figure 3.8: Test bench used for running S-parameter simulations.

Using the test bench in Figure 3.8 with the active inductor as the DUT, the frequency of the input signal for Port 1 is swept from 10 MHz to 10 GHz. The S-parameter results return the input impedance looking into the active inductor from Port 1. As expected, based on equations 3.1.12 and 3.1.13, the input impedance is made up of an inductive component and a small resistive component. These form the inductance and resistance of the active inductor. As described in Section 3.1, the inductance can be tuned by changing either of the bias currents, I_1 or I_2. In order to show the obtainable range of the inductance, a simulation is run where I_1 is varied from 20 μA to 200 μA. I_2 is held constant at 10 μA and the two control voltages are set to V_1 = 60 mV and V_2 = 1.05 V. The results of this simulation are shown in Figure 3.9.

*All simulations were done in SpectreRF ver. 5.0.33.021904 using BSIM3 v3.2 transistor models [39] in Cadence dfII ver. 2004a.

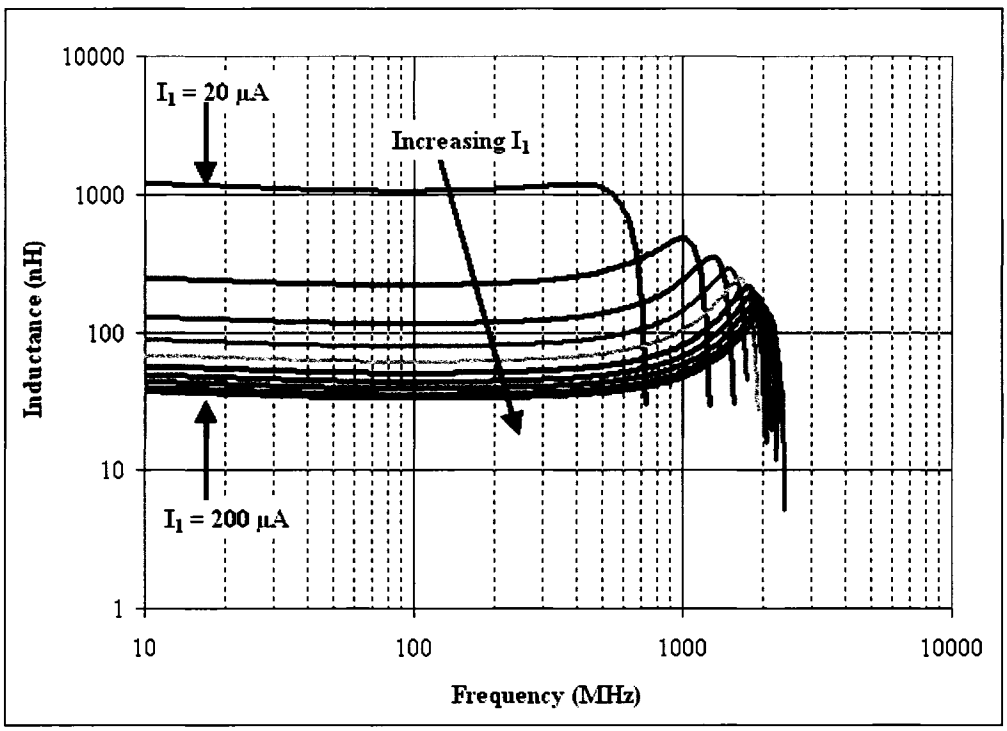

Figure 3.9: The inductance of the active inductor for values of I_1, swept in 20 μA steps.

Figure 3.9 shows that, at lower frequencies, the inductances can be tuned from 30 nH to over 1 μH. The tunable inductance range can span from 20 nH to 2 μH when I_1 is tuned from 5 μA to 200 μA and I_2 is tuned from 2 μA to 30 μA. This gives the range of inductances required for the filter to be tuned to the specified frequencies of 70 MHz to 700 MHz. At higher frequencies, the active inductor reaches its self-resonant frequency and becomes capacitive instead of inductive. At self-resonance, the circuit may become unstable and start to oscillate, if it has enough gain at the self-resonant frequency. This potential instability issue is a large-signal behavior and is discussed in Section 3.3.9. The S-parameter results presented in this section show the inductor's small-signal behavior and are used to demonstrate the tuning range of the inductance. The large signal issues such as the potential instability at self-resonance are not addressed here.

The simulated inductance can be compared to the theoretical inductance equation developed in Section 3.1. The two curves in Figure 3.10 illustrate this comparison of inductance while the drain current of transistors M_2 and M_3 are tuned. The drain current is tuned based on Equation 3.1.20, keeping I_2 fixed and varying I_1.

The top curve is the simulated inductance of the three transistors that make up the active inductor. This simulation does not include the source follower load and bias circuitry but instead assumes that the bias currents, I_1 and I_2, are ideal. The transistors are extracted components but do not include parasitic interconnect capacitances. The inductance values are measured at 100 MHz and plotted versus the transistor drain current. The lower curve is the theoretical inductance of the circuit based on Equation

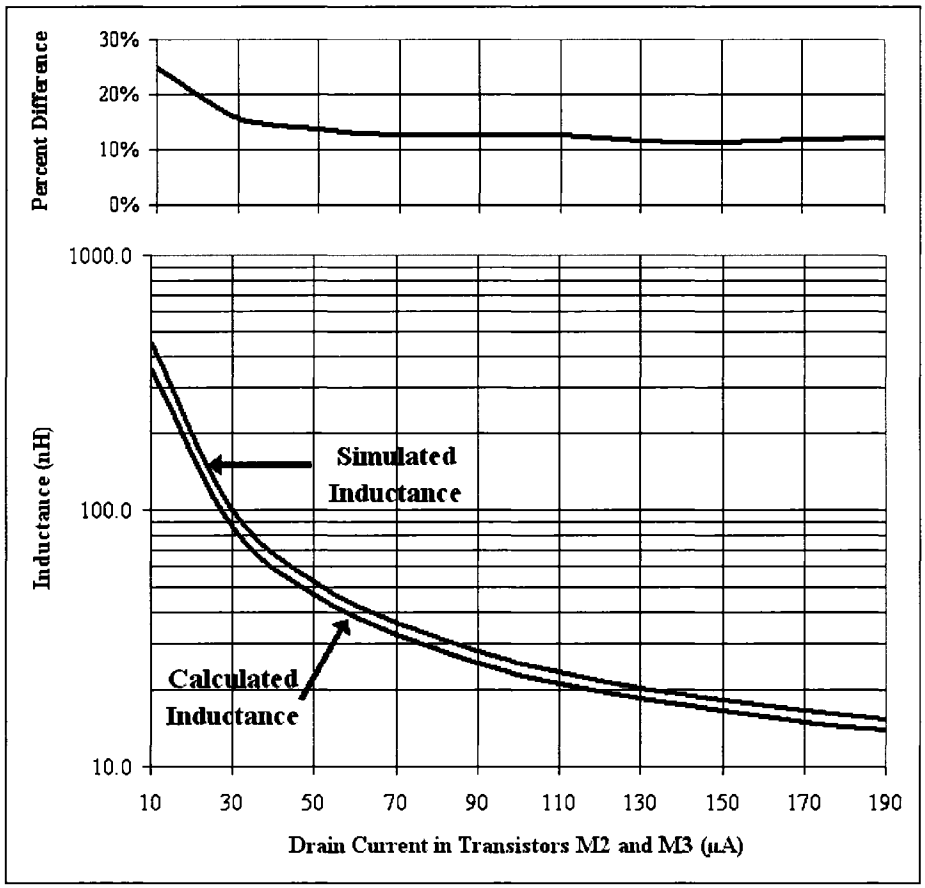

Figure 3.10: Comparison of the theoretical and simulated inductance of the active inductor. The theoretical and simulated inductance curves are on the bottom. The top curve is the percentage difference between the theoretical and simulated inductance.

3.1.12. This equation is derived by assuming that the bias currents I_1 and I_2 are ideal. It does not account for any parasitic capacitances in the circuit. In this way, a direct comparison can be made to the theoretical expression in Equation 3.1.12.

The simulated and theoretical curves compare well with each other, following an identical trend with respect to the drain current. The inductance of the active inductor is inversely proportional to the drain current through transistor M_2 and M_3. For inductances below 50 nH, the simulated results are approximately 12% higher than those expected from theory, as shown in the upper, percentage error curve in Figure 3.10. A possible explanation for this difference is the fact that the theoretical derivation uses square law models and assumes that all transistors are in saturation. In simulation, the models are numerical and not identical to the analytical small-signal models used to develop the theory. It is found through DC operating point simulations that the NMOS transistor, M_1, actually operates in the subthreshold region and just out of saturation. The results, however, remain very close and follow the same trend, allowing the inductance to be predicted based on the DC operating parameters of the transistors.

When the complete active inductor circuit is simulated with extracted parasitic capacitances, the real bias circuitry and the source follower load, the simulated inductance increases by a factor of approximately 2.2. This requires an adaptation of the theory to account for the real operation environment of the active inductor. While examining Equation 3.1.12 during the two simulated cases (with and without parasitic capacitances, bias circuitry and source follower load), it is seen that the transistor transconductances

and resistances change very little in each case. Though the transistor capacitances themselves do not change, additional capacitance is added from interconnect parasitics, the bias transistors and the load. This additional capacitance is large enough to cause a significant increase in the value of the inductance. The main contribution is additional capacitance connected to the output terminal of the active inductor. Sources of this additional capacitance include the gate to drain and gate to source capacitances of M_8, the source follower at the output, and the gate to drain capacitance of M_6, the PMOS current source transistor. These capacitances are in parallel with the $C_{gd1} + C_{gs2} + C_{gd2}$ term in Equation 3.1.12. This term is found to have a capacitance of around 16.2 fF. The additional capacitance from the source follower, current source and parasitic capacitances, which will be referred to as C_a, is found to add an additional 16.2 fF. This doubles the overall capacitance to 32.4 fF. Similarly, additional capacitance should be added to the approximately 19.7 fF of the $C_{gs1} + C_{gs2} + C_{gd3}$ term due to parasitic capacitance and the gate to drain capacitance of M_4, which will be referred to as C_b. This gives an additional 10.3 fF bringing the total capacitance on this node to 30 fF. However, this term has only a very small contribution to the inductance in Equation 3.1.12. Equation 3.1.12 can be adapted to include C_a and C_b giving

$$L = \frac{r_{o1}(C_{gd1} + C_{gs2} + C_{gd2} + C_a)(1 + r_{o3}[g_{m1} + g_{mb1}]) + r_{o3}(C_{gs1} + C_{gs2} + C_{gd3} + C_b)}{r_{o1}g_{m2}(g_{m1} + g_{m3}r_{o3}[g_{m1} + g_{mb1}])}. \tag{3.2.1}$$

Based on the doubling of capacitance caused by C_a in the dominant term of Equation 3.2.1, the inductance also doubles as the equation dictates. However, this doubling is

not as large as the factor of 2.2 increase seen in the simulated results. This discrepancy causes the simulated inductance from the full circuit to be about 20% higher than that predicted by the adapted equation versus the 12% difference when the active inductor is examined with ideal current sources and no parasitic or load capacitances. These new results are shown in Figure 3.11. The loss of accuracy shows that adding the extra capacitance helps the accuracy of the equation to a certain extent but not fully. A possible explanation for the larger inductance in simulation is that the current mirror sources have a finite output resistance. This will lower the resistances in Equation 3.2.1 which has the effect of raising the inductance. Other parts of the bias and load transistors that are not modelled can also contribute to the difference. The theory is about 20% off in predicting the simulated inductance. However, the theory predicts the trend of inductance versus drain current well over the range of drain current from 10 μA to 190 μA.

3.2.3 Simulating the Series Resistance of the Active Inductor

The series resistance of the active inductor determines its quality factor. The lower the series resistance, the higher the quality factor as seen in Equation 3.1.16. The series resistance can be controlled by the bias voltages V_1 and V_2. The series resistance of the active inductor can be seen as the real part of the input impedance from an S-parameter simulation using the testbench in Figure 3.8. Figure 3.12 shows the series resistance of the inductor when the control voltage, V_1, is tuned from 0 to 100 mV. The other control voltage, V_2, is held constant at 1.2 V and the bias currents are set to $I_1 = 80$ μA and I_2

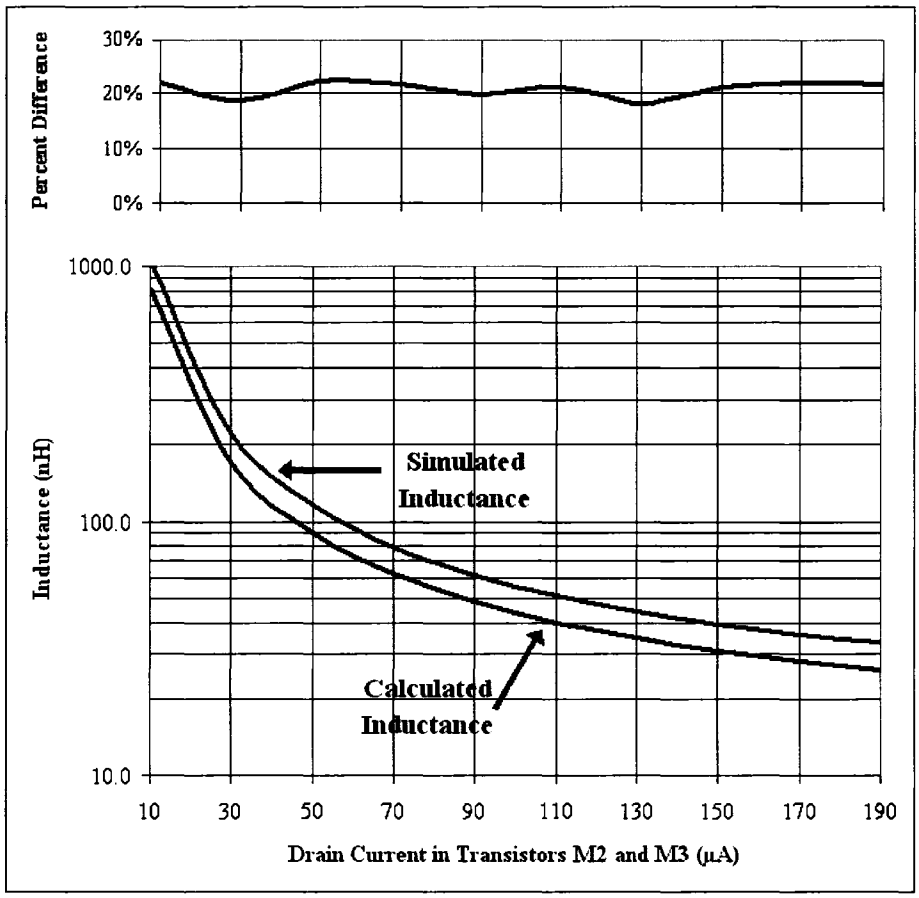

Figure 3.11: Comparison of the theoretical and simulated inductance of the active inductor including biasing, load and parasitic capacitances. The theoretical and simulated inductance curves are on the bottom. The top curve is the percentage difference between the theoretical and simulated inductance.

= 15 μA. It can be seen that increasing V_1 causes the series resistance to be reduced, as expected, due to increasing V_{DS} of transistor M_3. Simulations also show a similar effect where the series resistance can be reduced by reducing V_2, which again increases V_{DS3} as well as V_{DS1}.

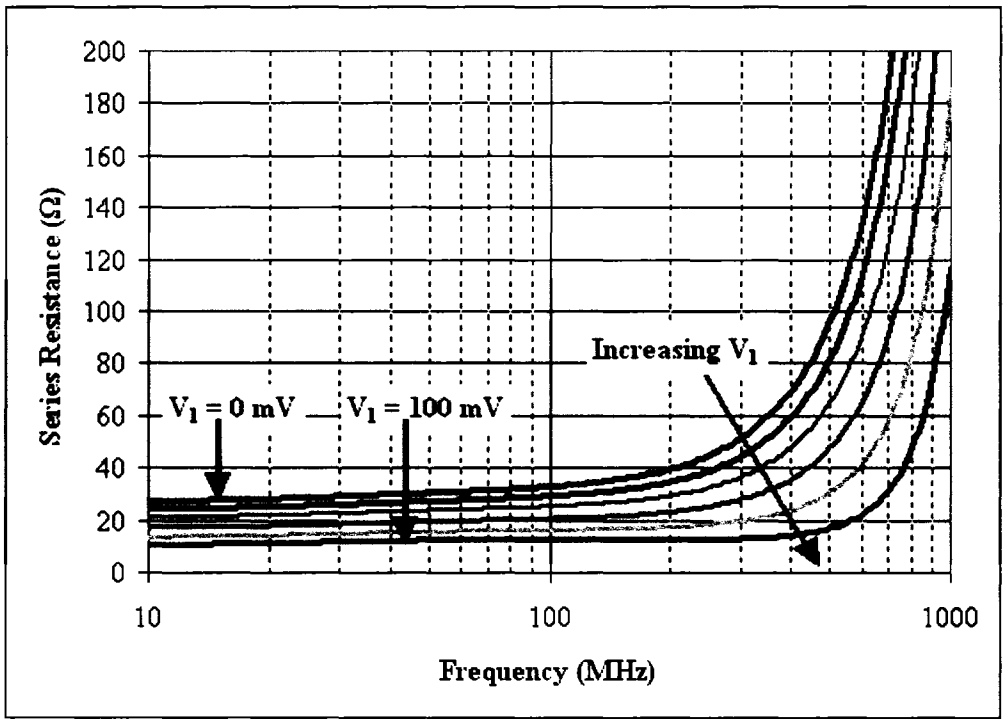

Figure 3.12: The series resistance of the active inductor for values of V_1, swept in 20 mV steps.

A plot of the series resistance can be seen in Figure 3.13 for two simulated and two theoretical cases. Each of these resistances is plotted against the control voltage, V_1, at 100 MHz. R_{SIM1} is for the simulation of the active inductor with real current biases, the source follower load and parasitic capacitors. R_{SIM2} is for the simulation with ideal current sources and no parasitic capacitances. The theoretical curve, R_{CALC1}, represents

Equation 3.1.13.

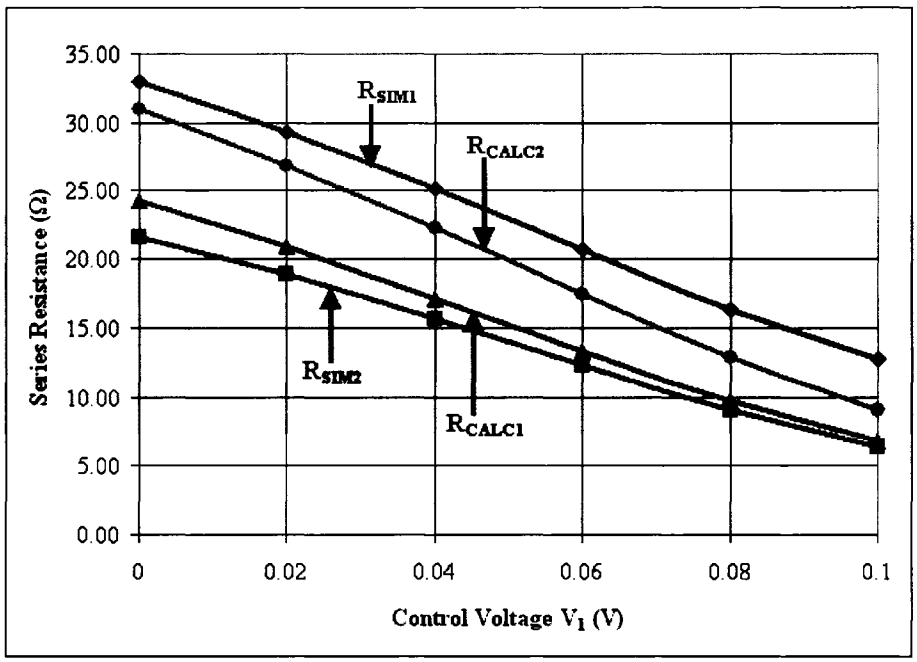

Figure 3.13: Comparison of the theoretical and simulated series resistance of the active inductor.

The simulated results in R_{SIM2} are between 0.5 to 3 Ω off the theoretical prediction in R_{CALC1}, getting closer as the series resistance gets smaller. This shows that the theory models the simulation well. Both of these cases show that the series resistance has a linear relationship with the control voltage. The results in R_{SIM1} also show the same trend and follow the linear relationship. However, they are shifted up by about 10 Ω. Again, this difference can be attributed to the additional bias circuitry. The bias transistors, M_4 and M_6, have respective finite output resistances, r_{o4} and r_{o6}. If r_{o4} is treated as being in parallel with r_{o3} and r_{o6} in parallel with r_{o1} the effective size of r_{o1} and r_{o3} is reduced. From DC operating point results, r_{o6} could reduce r_{o1} to about 0.8 of

its size and r_{o4} could reduce r_{o3} to about 0.9. With this adjustment, the curve R_{CALC2} is obtained in Figure 3.13. It results in an increased resistance that follows the same linear trend as the simulated results. The results from R_{CALC2} differ by about 2 to 4 Ω from R_{SIM1}.

3.3 Implementation and Simulation of the Bandpass Filter

For the application as part of the whitespace detector for locating spectrum holes in the broadcast television band, the tunable bandpass filter must tune from 70 MHz to 700 MHz while achieving a sufficiently high quality factor to provide a 3 dB bandwidth of less than 6 MHz. Based on Equation 3.1.26, a quality factor of 12 is required at 70 MHz and a quality factor of 120 is required at 700 MHz, in order to meet the 6 MHz bandwidth requirement. Simulation results in Section 3.2 show that the inductance of the active inductor can be tuned from 30 nH to 1 μH by tuning the bias current I_1. Simulations also show that the inductance can be increased above 1 μH to about 3 μH if the bias currents, I_1 and I_2, are lowered below those shown in the simulations in Section 3.2. Based on these results and the specifications, the series capacitance at the input of the bandpass filter is chosen to be C_{in} = 1.55 pF. Referring to Equation 3.1.24, this capacitance gives a center frequency of 738 MHz when the inductance is tuned to 30 nH and 74 MHz when it is tuned to 3 μH, allowing the range of desired frequencies to be reached. The following subsections show simulation results for the tuning characteristic of the bandpass filter. All simulations are done with the extracted circuits and parasitic

capacitances. An input and output buffer are included in all simulations to interface the filter to a 50 Ω environment, which is representative of the equipment required to test the circuit once it is fabricated. These buffers are described in more detail in Chapter 5. Though television systems operate in a 75 Ω environment, 50 Ω is used to simplify testing of the bandpass filter in a 50 Ω test environment. In a real application, the filter would be completely integrated behind another circuit that would match to a 75 Ω or 50 Ω environment, as required.

3.3.1 The Bandpass Filter Layout

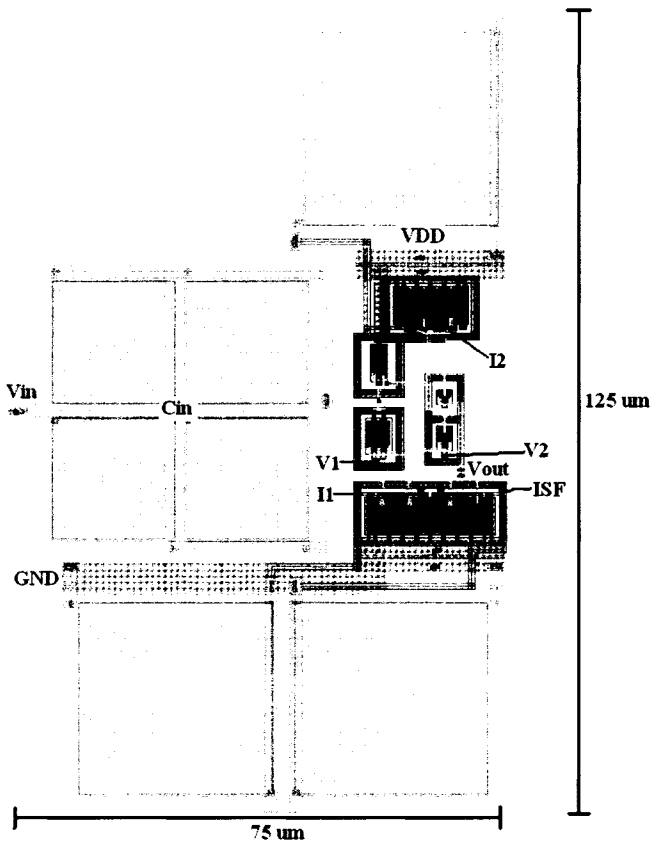

Figure 3.14: The bandpass filter layout with input and output ports labelled. (Refer to the layout key in Figure B.1 of Appendix B to identify all layers used in the layout.)

The layout of the bandpass filter is shown in Figure 3.14. All of the input and output ports are labelled. This layout is built from the active inductor layout in Figure 3.7, with the addition of the input capacitor labelled C_{in}. This is a 1.55 pF MIM (metal-insulator-metal) capacitor. As with the active inductor, all simulations of the bandpass filter are performed with the circuit that is extracted from the layout with parasitic capacitances.

3.3.2 Tuning of the Bandpass Filter's Center Frequency and Quality Factor

The bandpass filter response can be tuned using four parameters. These are the two bias currents, I_1 and I_2, and the two bias voltages, V_1 and V_2, which control the active inductor. The filter center frequency can be tuned across the entire 70 MHz to 700 MHz frequency band and beyond by changing the inductance of the active inductor. The center frequency gain and 3 dB bandwidth of the filter is tuned by changing the quality factor of the active inductor. The gain can be tuned to above 50 dB with 3 dB bandwidths that are less than 1 MHz. The two bias currents predominantly control the center frequency while the two bias voltages control the gain and bandwidth. However, the currents do effect the gain and bandwidth and the voltages do effect the center frequency, but to a lesser degree.

S-parameter simulations of the bandpass filter are used to show its tuning behavior. The test bench used for bandpass filter simulations is shown in Figure 3.15. It is powered by a supply voltage of $V_{DD} = 1.8$ V. The biasing voltages and currents are controlled in

the test bench. These are also the tuning parameters, I_1, I_2, V_1 and V_2. The simulation uses the complete whitespace detector circuit that is extracted from the layout with parasitic capacitances. The input and output buffers are part of this complete circuit and are used to interface the bandpass filter with the 50 Ω input and output ports. Also forming part of the circuit, and shown in the test bench, are coupling capacitors, C_C. Bondwire models, along with capacitances that represent the integrated circuit and printed circuit board pads, are included in the test bench for all input and output signals, including the supply and ground. A more detailed discussion of the whitespace detector as a system, along with the input and output buffers and bondwire discussion is provided in Chapter 5. The input signal is given at Port 1 and the output is taken at Port 2.

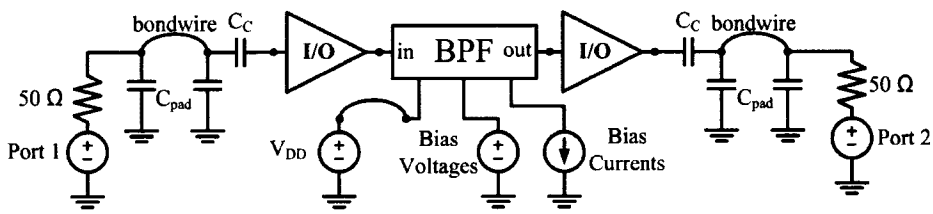

Figure 3.15: Test bench used for running simulations on the bandpass filter.

As an example, Figure 3.16 shows the S21 characteristic of the filter when simulated using the bandpass filter test bench. For this simulation the frequency of the small signal input is swept at Port 1. The S21 plot shows the gain of the circuit from the input Port 1 to the output Port 2 where the gain is described by

$$Gain(S21) = 20log\frac{V_{out}}{V_{in}}. \tag{3.3.1}$$

In this example, the bandpass filter is tuned to 199 MHz. Table 3.2 summarizes the

tuning parameters and the performance of the filter in this situation.

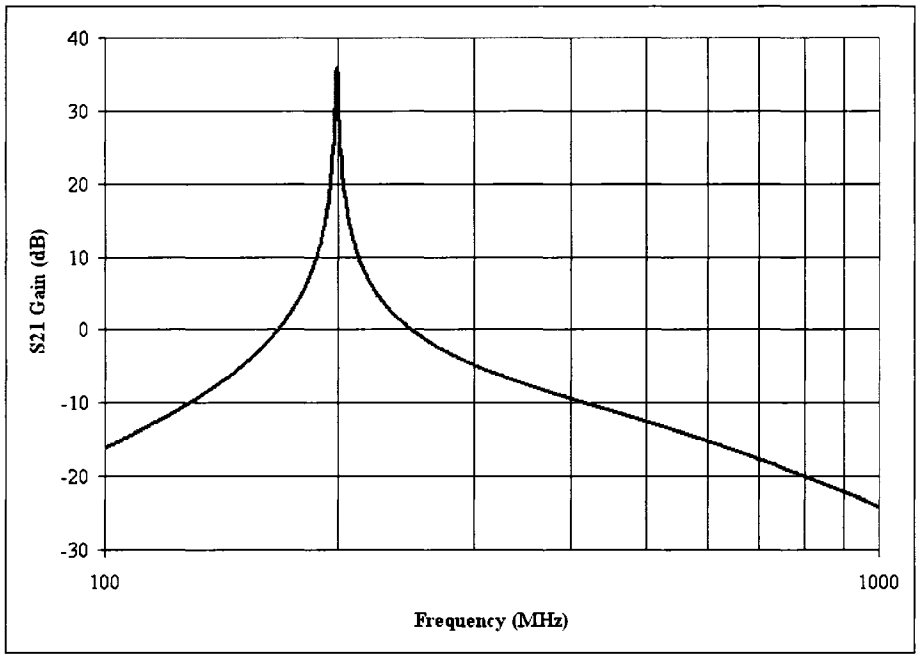

Figure 3.16: S21 of the whitespace detector's bandpass filter when tuned to 199 MHz.

Table 3.2: Tuning the the Bandpass Filter at 199 MHz

Tuning Parameters	I_1	27 μA
	I_2	5.1 μA
	V_1	0.06 V
	V_2	1.05 V
Performance	Center Frequency	199 MHz
	Gain at Center Frequency	35.9 dB
	3 dB Bandwidth	1.27 MHz

Post-layout S-parameter simulation results show how the bandpass filter can be tuned. The S21 simulation results in Figure 3.17 show how the center frequency of the bandpass filter can be tuned by changing one of the bias currents, I_1, while keeping the other tuning parameters constant. Larger currents result in the filter being tuned to higher frequencies. As the current tunes the frequency away from its ideal point, the

quality factor of the bandpass filter decreases. The quality factor can be increased to a desirable level by tuning one of the control voltages.

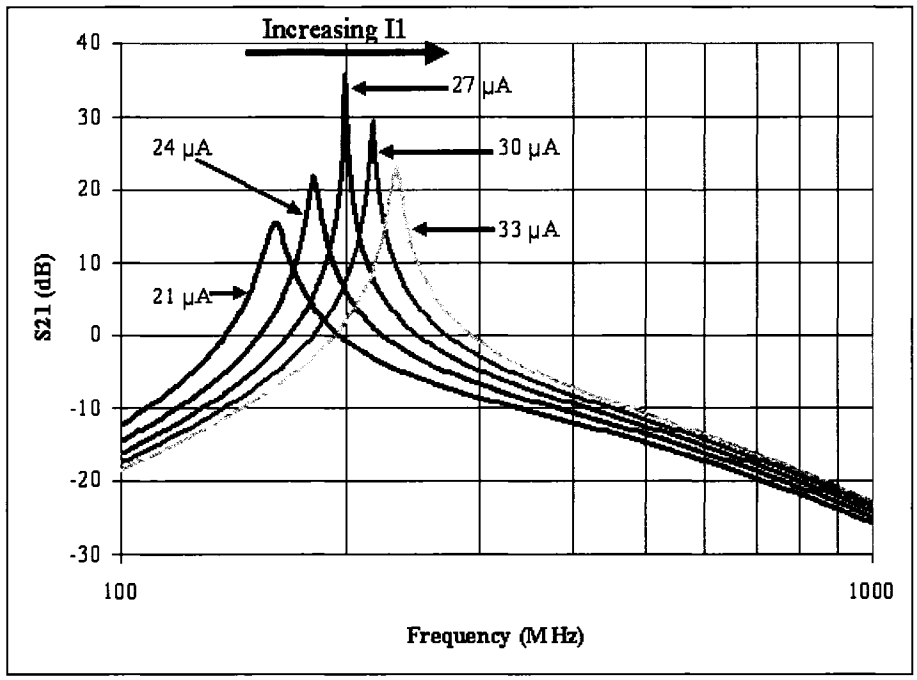

Figure 3.17: Tuning of the bandpass filter center frequency with I_1. I_1 is increased from 21 μA to 33 μA in increments of 3 μA.

Figure 3.18 shows the effect of tuning the control voltage, V_1, on the quality factor of the bandpass filter, while all other parameters are held constant. The plot shows that increasing V_1 from 0 to 60 mV causes the quality factor to increase.

To demonstrate how the filter can be tuned to isolate signals in the broadcast television bands, Figure 3.19 shows the filter tuned to 5 different frequencies with 6 MHz separation. Table 3.3 shows how the tuning parameters are set to achieve these S21 characteristics, using the test bench in Figure 3.15. Large pass band gains can be achieved at each frequency by simultaneously tuning I_1 and I_2. For increasing the frequency, both

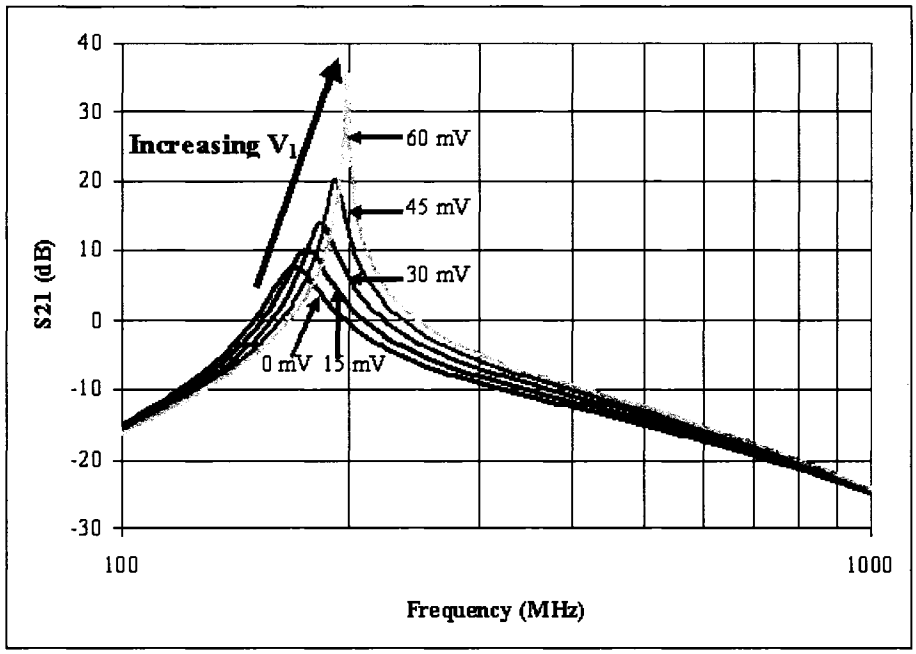

Figure 3.18: Tuning of the bandpass filter quality factor with V_1. V_1 is increased from 0 to 60 mV in increments of 15 mV.

I_1 and I_2 increase though I_1 increases at a greater rate than I_2. The net effect is that I_1 - I_2, or the transistor drain current in the active inductor, increases as well, following Equation 3.1.20. The tuning voltages can be used to tweak the pass band gain as required. When tuned to a particular channel, the gain at the center of the channel is about 15 dB above the gain at the edge of an adjacent channel, showing how the filter can filter one 6 MHz channel from adjacent channels.

Table 3.3: Tuning of the Bandpass Filter to 6 MHz Channels

Frequency (MHz)	Gain (dB)	I_1 (μA)	I_2 (μA)	V_1 (V)	V_2 (V)
199.2	35.9	27	5.1	0.06	1.05
205.1	37.3	28	5.3	0.059	1.05
211.3	35.7	28.9	5.7	0.06	1.05
217.3	35.7	29.9	6.0	0.06	1.05
222.8	36.1	30.9	6.2	0.059	1.05

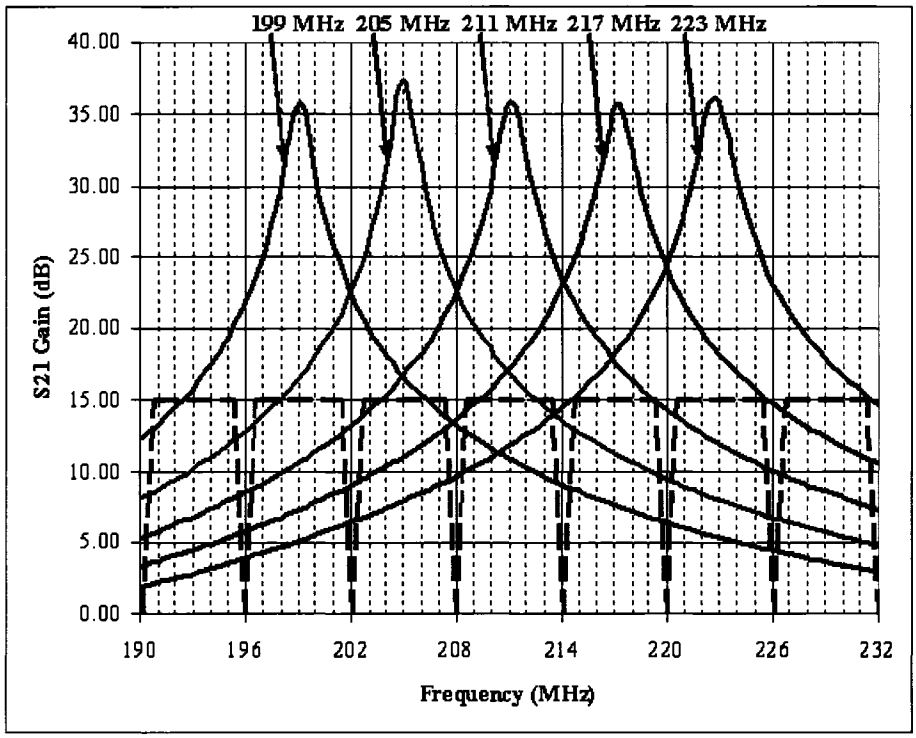

Figure 3.19: S21 of the whitespace detector's bandpass filter when tuned to 6 MHz channels. The dashed boxes represent the 6 MHz television bands.

Figure 3.20 shows the filter response when tuned to several frequencies across the entire band of broadcast television channels available for the desired application. The tuning parameters required to give these results are shown in Table 3.4. The filter can be tuned to all frequencies across the band of 70 MHz to 700 MHz. The achievable center frequency gain is above 30 dB but at low frequencies it is more difficult to reach high gains. This is due to the fact that the larger inductance required for these frequencies is also accompanied by a larger series resistance. Quality factors up to 150 are achieved, enabling 3-dB bandwidths below 6 MHz.

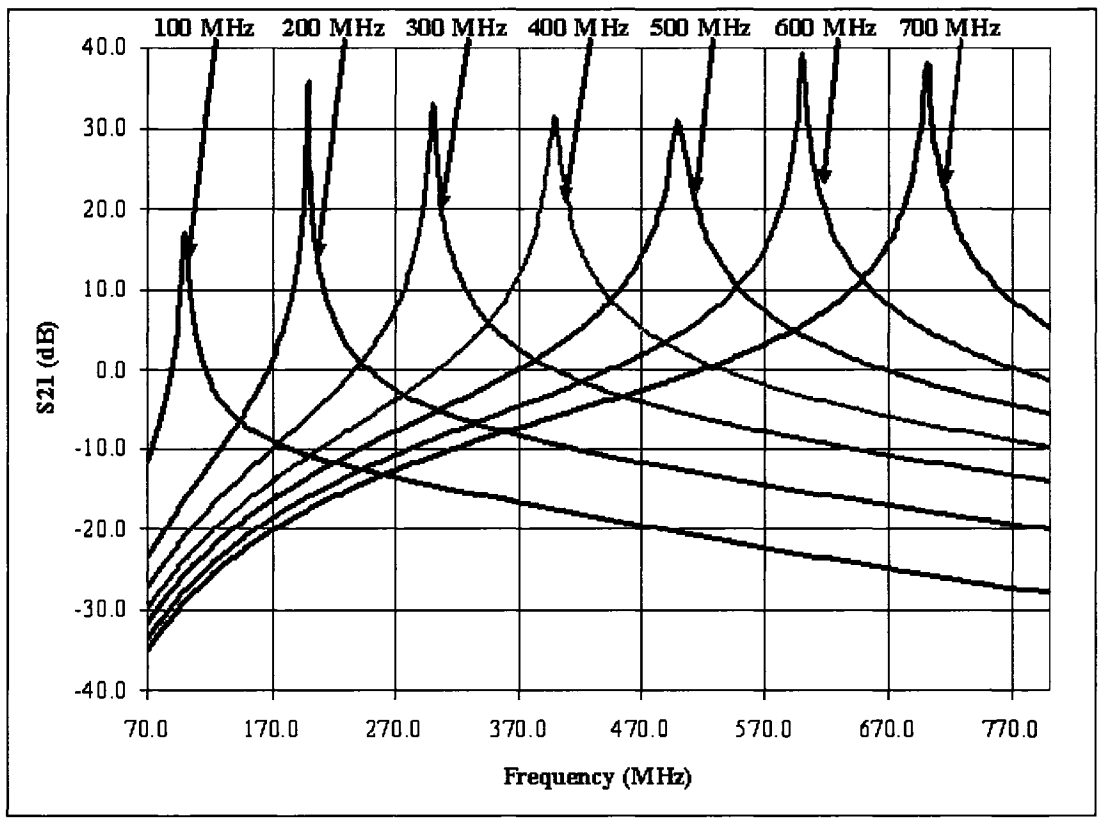

Figure 3.20: S21 of the whitespace detector's bandpass filter when tuned to frequencies across the entire TV band.

Table 3.4: Tuning of the Bandpass Filter to Frequencies Across the TV Band

Frequency (MHz)	Gain (dB)	f_{3dB} (MHz)	Quality Factor	I_1 (μA)	I_2 (μA)	V_1 (V)	V_2 (V)	$I_D = I_1 - I_2$ (μA)
100.0	17.2	3.7	27	11.2	3.5	0.5	1.05	7.7
199.1	35.9	1.3	153	27	5.1	0.06	1.05	21.9
299.9	33.2	3.5	86	45.8	9.5	0.06	1.05	36.3
399.0	31.4	6.4	62	69	13	0.06	1.05	56
498.9	31.0	8.9	56	95	17	0.15	1.05	78
599.8	39.0	4.0	150	136	19	0.06	1.05	117
699.8	37.7	5.2	135	185	24	0.06	1.05	161

3.3.3 Analysis of the Bandpass Filter's Center Frequency Tuning

The center frequency of the bandpass filter from S-parameter simulations is found to be within 5% of the value Equation 3.1.24 predicts for a given inductance. The difference between the simulated and expected results are shown in Figure 3.21 with the simulated center frequency being higher than the predicted one at low frequencies and lower at high frequencies. Over the full range, the simulated frequency is less than 5% off the predicted value.

The measured center frequency values come from setting the tuning parameters as they are in Table 3.4. For the calculation of the center frequency using Equation 3.1.24, the capacitance of C_{in} = 1.55 pF is used. The simulated and expected inductance of the active inductor have already been compared in Section 3.2. For this reason the inductance used in the equation is taken by simulating the active inductor on its own, when its tuning parameters are set to match those in Table 3.4. Thus this comparison is used to prove the validity of Equation 3.1.24. Equation 3.3.2 shows a sample calculation

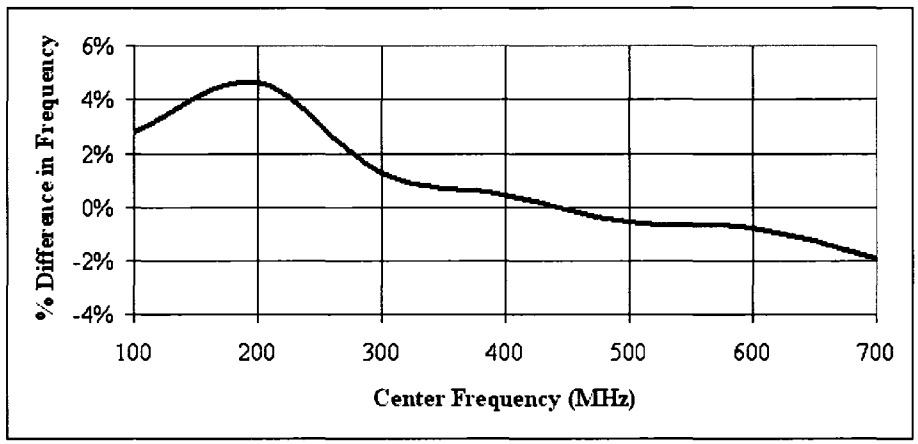

Figure 3.21: A comparison of the simulated and predicted bandpass filter center frequency, demonstrating the validity of Equation 3.1.24.

of the center frequency, using the measured inductance of L = 187 nH at 300 MHz.

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(187nH)(1.55pF)}} = 295.6\text{MHz} \tag{3.3.2}$$

The drain current passing through transistors M_2 and M_3 for each of the tuning cases is shown in Table 3.4, based on Equation 3.1.20. The relationship derived in Equation 3.1.27 states that the center frequency of the bandpass filter should be proportional to the square-root of the drain current of transistors M_2 and M_3. Based on the post-layout S-parameter simulation results in Table 3.4 for the center frequency versus drain current, the graph in Figure 3.22 is obtained.

The square-root proportionality trend is also shown in Figure 3.22. The simulated results match the trend within 3% for frequencies above 400 MHz. The results begin to deviate from this trend at lower frequencies and are off by as much as 50% at 100 MHz. This is an observed trend that attempts to model the relationship between the drain current of the transistors in the active inductor and the center frequency of the bandpass

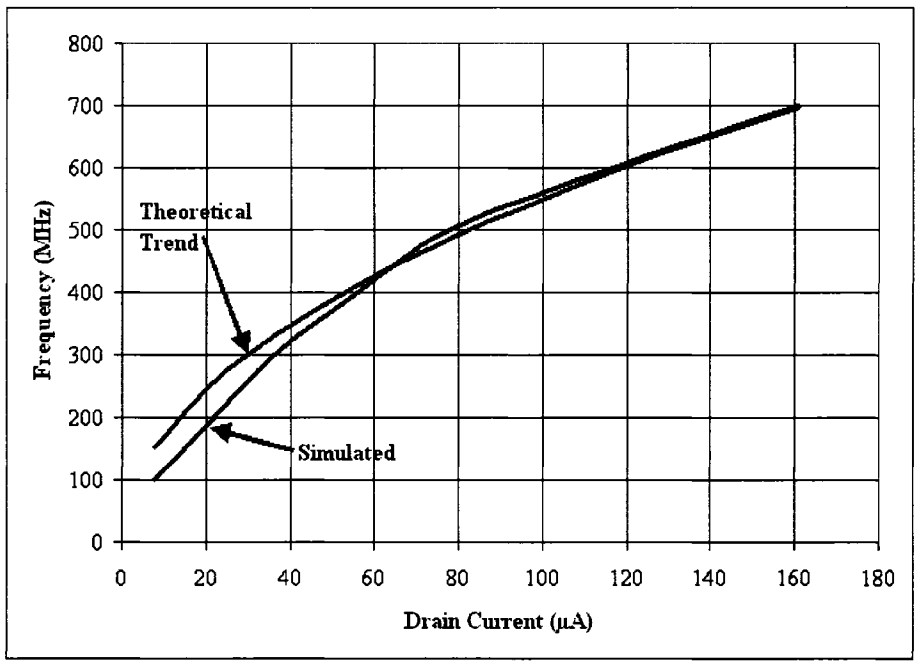

Figure 3.22: Center frequency of the bandpass filter versus transistor drain current.

filter. The trend is not as accurate for modelling the relationship at low frequencies as it is at high frequencies. The expression for the theoretical trend line can be given by

$$f_0 = k\sqrt{I_D} = 55\sqrt{I_D} \tag{3.3.3}$$

where f_0 is the bandpass filter center frequency in MHz, I_D is the drain current in μA and the constant, k, is in units of MHz/$\sqrt{\mu A}$. The trend in Equation 3.3.3 can assist in predicting the center frequency of the bandpass filter from the value of the input currents. It can be observed from Table 3.4 that, in order to achieve a high quality factor at a given frequency, both the bias currents, I_1 and I_2, must be tuned in tandem to set the required transistor drain current. It is found that increasing one without the other makes it more difficult to achieve the desired gain and leads to potential instability problems with the

active inductor. This is discussed further in Section 3.3.9. To further assist in predicting the bias currents required to achieve a high quality factor at a particular frequency, the current tuning trends in Figure 3.23 are observed from the simulated results in Table 3.4.

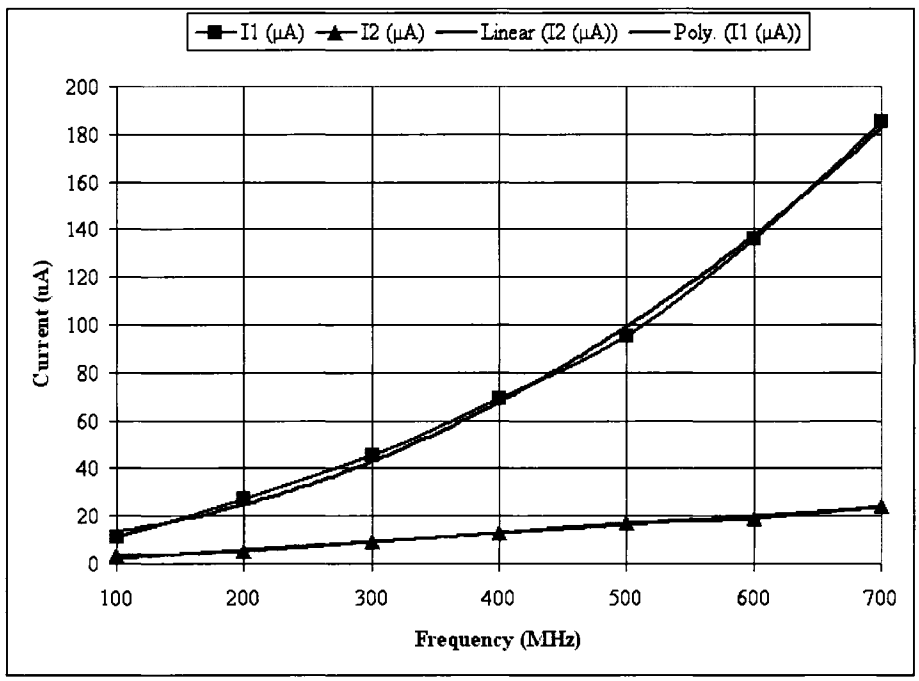

Figure 3.23: Required bias currents for a given bandpass filter center frequency.

The value of I_1 required follows very closely to a second order polynomial versus frequency and can be described by

$$I_1 = 0.0003125 f_0^2 + 0.0225 f_0 + 10. \tag{3.3.4}$$

The required value of I_2 follows a very linear trend versus frequency that can be estimated by

$$I_2 = 0.035 f_0 - 1. \tag{3.3.5}$$

In both equations, the current is in μA and the frequency is in MHz. The derivation of these equations can be found in Appendix A.2. They are valid for the typical transistor models* used and show the trends observed for the relationship between the bias currents and the filter's center frequency.

3.3.4 Analysis of the Bandpass Filter's Quality Factor Tuning

A comparison of the calculated and simulated series resistance of the active inductor is made in Figure 3.13 as the control voltage, V_1 is tuned. The quality factor of the bandpass filter is simulated using the same tuning setup of $I_1 = 80$ μA, $I_2 = 15$ μA and $V_2 = 1.2$ V. V_1 is swept from 0 V to 0.1 V. This is done with an S-parameter simulation using the test bench in Figure 3.8. The simulated quality factor of the bandpass filter is shown in Figure 3.24, labelled as Q_{SIM}. This quality factor is measured in the S-parameter simulation as f_0/f_{3dB}.

These simulated results are compared to the theoretical curve, labelled Q_{CALC}. Q_{CALC} is calculated using Equation 3.1.25 where C = 1.545 pF is the input capacitance of the bandpass filter, R_S is the calculated series resistance shown as R_{CALC2} in Figure 3.13 and L is the inductance calculated using Equation 3.1.15. The calculations predict a quality factor that is approximately 12 % higher than the simulated results. In the simulations, the quality factor is measured using S-parameters where the signal passes through an input buffer before the bandpass filter and an output buffer after the bandpass filter. These buffers allow the filter to interface with a 50 Ω environment but

*The transistor models are BSIM3 v3.2 for the TSMC 0.18μm CMOS technology [39].

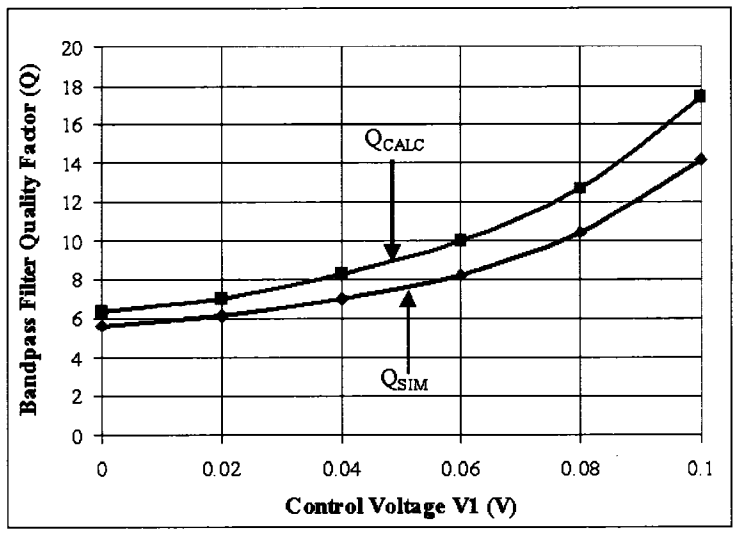

Figure 3.24: Comparison of the calculated and simulated quality factor of the bandpass filter when tuning the control voltage, V_1.

also add attenuation that lowers the gain and quality factor of the filter. This is not accounted for in the theoretical calculations.

Both the theoretical and simulated quality factors show an increasing trend with increasing V_1, as expected based on the discussion of the series resistance trends in Section 3.1. Increasing V_1 reduces the series resistance, which in turn increases the quality factor. In theory, the quality factor can continue to be increased as the series resistance is made to approach zero. In reality, this is not possible. Figure 3.25 shows simulation results of the quality factor being increased to about 100 at which point it cannot be increased any further. This is done by increasing V_1 while $I_1 = 95$ μA, $I_2 =$ 17 μA and $V_2 = 1.05$ V. This quality factor of 100 is from S-parameter simulations and is still overly optimistic. When large signal, transient simulations are run, as discussed in Section 3.3.6, the achievable quality factor is not as high. As V_1 is increased from 0

V to 0.5 V, the center frequency of the bandpass filter increases by 8 % showing that it is not strongly dependent on the control voltage.

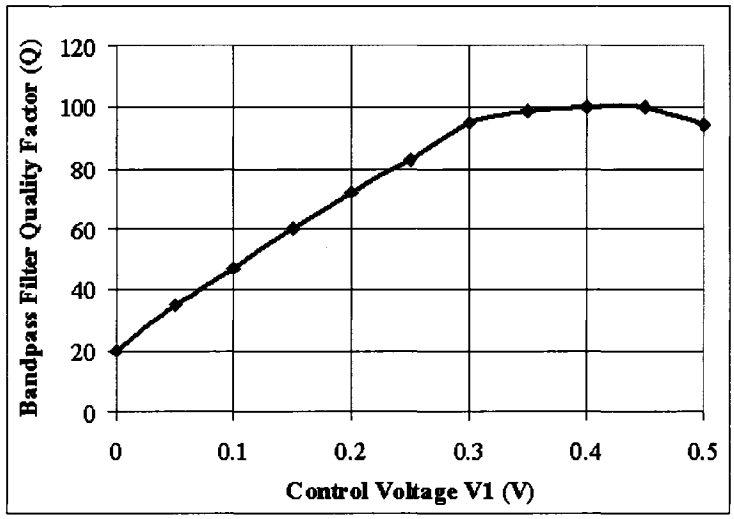

Figure 3.25: The simulated quality factor of the bandpass filter when tuning the control voltage, V_1.

3.3.5 Tuning Algorithm

From the theory discussed in Section 3.1 and simulation results viewed in Section 3.3, the tuning trends of the bandpass filter can be summarized. Table 3.5 summarizes the effect of each of the four tuning parameters on the center frequency and quality factor of the bandpass filter. Each of the parameters is increased over its valid and useful range of values.

As seen in Table 3.5, the tuning of the bandpass filter center frequency is predominately controlled by adjusting the two bias currents while adjusting the two bias voltages primarily controls the quality factor. Adjusting the currents does effect the quality factor as the quality factor increases until the currents reach the point where the optimum

Table 3.5: Effect of Each Tuning Parameter on the Center Frequency on Quality Factor of the Bandpass Filter

Tuning Parameter	Increasing over valid range of:	Center Frequency (f_0)	Quality Factor (Q)
I_1	5 μA to 200 μA	**Increases**	Increases until optimal f_0 then decreases
I_2	2 μA to 30 μA	**Decreases**	Increases until optimal f_0 then decreases
V_1	0 V to 0.5 V	Small Increase	**Increases**
V_2	0.9 V to 1.2 V	Small Decrease	**Decreases**

center frequency is reached for the given combination of the tuning parameters. Adjusting the voltages does effect the center frequency, though only to a small degree relative to the change in quality factor. The overall tuning of the filter is non-trivial due to the interdependencies of the tuning parameters. However, with a thorough understanding of the impact that each of the tuning parameters has, a procedure or algorithm for tuning the filter can be developed.

A basic method for tuning the center frequency of the bandpass filter while simultaneously achieving high gain and narrow bandwidth at the center frequency is summarized in Figure 3.26.

The bias voltages are initially set to a point that is known to provide acceptably small series resistance for the active inductor. For V_1, this is below 100 mV and for V_2, this is about 1 V. From simulations, it is found that V_2 can be kept constant at 1.05 V and V_1 can be used for tuning the quality factor in order to reduce the number of tuning parameters to three. To get a close estimate of the bias currents required to have

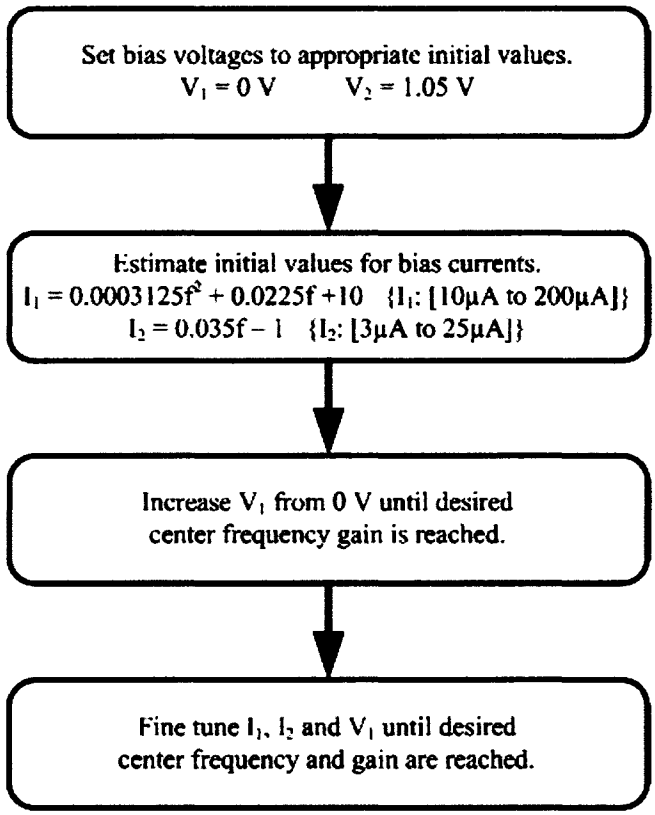

Figure 3.26: Flowchart outlining the procedure used to tune the center frequency and center frequency gain of the bandpass filter.

a particular center frequency, Equations 3.3.4 and 3.3.5 are used to estimate I_1 and I_2. The range of bias currents required to tune the center frequency of the bandpass filter over the specified range of 70 MHz to 700 MHz is approximately 10 μA to 200 μA for I_1 and 3 μA to 25 μA for I_2. The low end of the currents tune to the low end of the frequency range while the high currents tune to the high frequencies. After selecting the bias currents, V_1 can be increased from 0 V until the desired gain is achieved at the center frequency. This is usually below 100 mV but may be higher (up to approximately 500 mV) for low center frequencies. As will be discussed in Section 3.3.9, increasing the gain too far can lead to instability in the active inductor. At this point, the center frequency and quality factor will be close to the desired values and can be fine tuned by making small adjustments to I_1, I_2 and V_1 as required.

3.3.6 Transient Simulations

Up until this point, the performance of the active inductor-based bandpass filter has been examined using post-layout S-parameter, small signal simulations. This is to provide an understanding of the filter's tuning behavior. For practical purposes, larger signals have to be examined through transient time domain simulations. As described in the specifications in Chapter 2, the signal strengths at the whitespace detector input will use television receiver signal strengths as a guideline. These can be as low as -83 dBm and as high as -15 dBm [13]. This gives a starting point for the range of signal strengths that the whitespace detector will have to deal with. Assuming a 50 Ω system, as will be used when testing the circuit, -83 dBm and -15 dBm are respectively equivalent to

peak voltages ranging from 22.4 μV to 56.2 mV, as discissed in Chapter 2. Ideally, the bandpass filter should work for input voltages across this entire range. For the practical application of the whitespace detector, it is important to look at inputs that are at the threshold of being an acceptable signal. For this reason, the lower range of input voltages will be examined with the bandpass filter. Without any additional circuitry such as some automatic gain control circuitry, the bandpass filter would not be able to operate properly with peak input signals as high as 50 mV peak. A voltage gain of 35 dB (or 56 V/V) would cause the peak output voltage to be 2.8 V when the peak input voltage is 50 mV. With a 1.8 V supply and the potential for the filter to be operating with higher gains, this is clearly impossible without additional circuitry. As such, an input range of 10 μV peak to 10 mV peak is chosen for the operation of the bandpass filter, with the nominal input being 100 μV peak.

To demonstrate the transient performance of the bandpass filter, a simulation is run with the filter tuned as in the example in Table 3.2. This transient simulation is run using the same test bench in Figure 3.15 that is used for S-parameter simulations. Based on a post-layout S-parameter simulation, the filter's center frequency is 199 MHz and it has a voltage gain of 35.9 dB at its center frequency. The transient simulation is done using the complete extracted version of the whitespace detector circuit. For this reason the signal passes through input and output buffers before and after the bandpass filter as will be described in Chapter 5. These add attenuation to the signal but are required to interface the circuit to the printed circuit board that is used for testing. These

simulations also include bondwire models and pad capacitances from the chip and the board. All of these additions to the simulation account for the non-ideal appearance of the signals.

The transient simulation results in Figure 3.27 are for a peak input voltage of 100 μV. It shows the output waveform for signals at 198 MHz, 195 MHz and 192 MHz. The largest transient gain is achieved at 198 MHz. A large gain of 31.5 times is seen at 198 MHz, giving a peak output voltage of 3.15 mV, while less gain is seen at the adjacent frequencies. There is a drop of 8.2 dB in the voltage gain when moving to the adjacent channel of 192 MHz. Further away from the center frequency, the gain is reduced even more. At 150 MHz, the gain is -4.7 dB. This shows the successful functionality of the bandpass filter in the time domain. The transient results are summarized in Table 3.6 while Figure 3.28 shows the output amplitude from the filter and output buffer at various frequencies.

Table 3.6: Transient Output Response of the Bandpass Filter

Input Frequency (MHz)	Input Amplitude (mV)	Output Amplitude (mV)	Voltage Gain (V/V)	Voltage Gain (dB)
198	0.1	3.15	31.5	30.0
195	0.1	2.41	24.1	27.6
192	0.1	1.23	12.3	21.8
150	0.1	0.058	0.58	-4.7

The small signal S-parameter simulation results for this tuning scenario show that the center frequency of the filter is at 199 MHz. The transient results with a 100 μV input show that the largest gain is at a center frequency of 198 MHz. This shows a difference in the small signal and large signal operation of the filter. When the filter

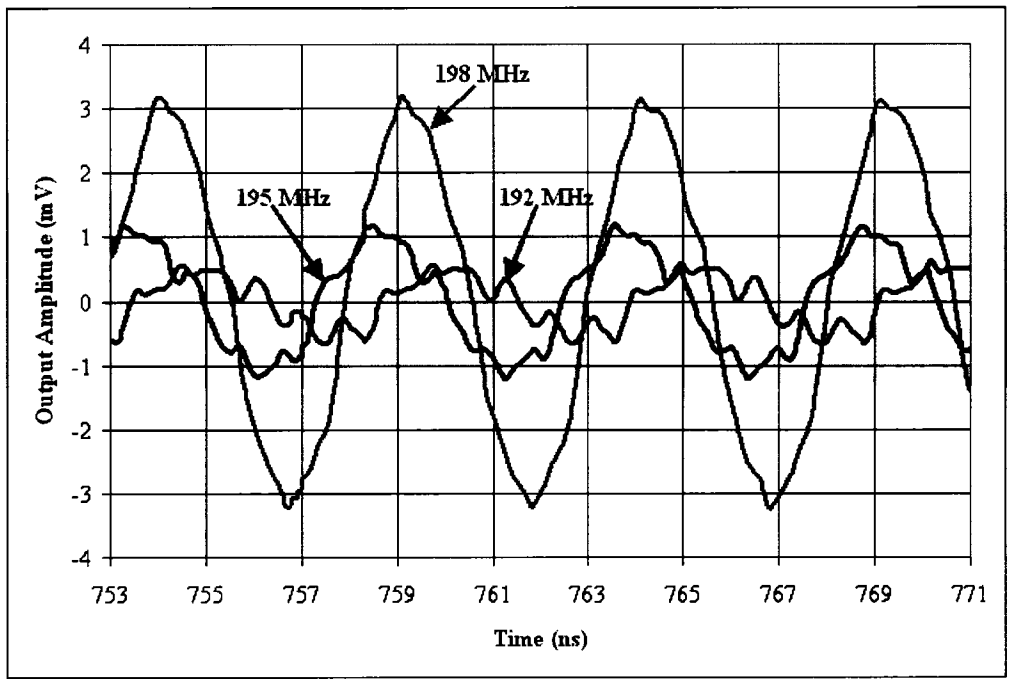

Figure 3.27: Transient output waveforms from the bandpass filter after passing through the output buffer.

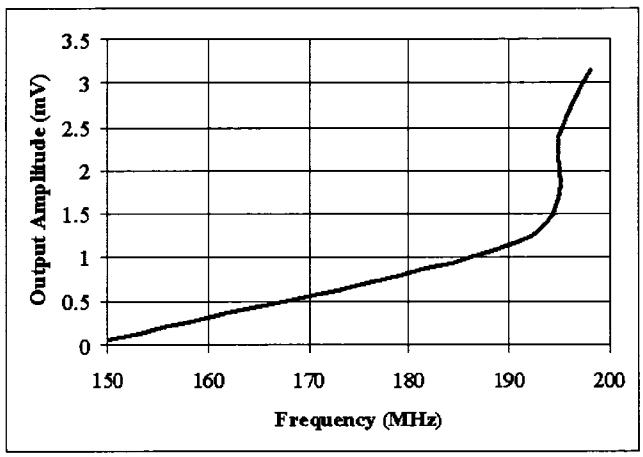

Figure 3.28: The output amplitude of the bandpass filter at various frequencies when tuned to 199 MHz.

is tuned for high gain, its center frequency and quality factor become very sensitive to changes in the filter's operating point. Large input signals and the resulting larger output signals can shift the operating point and thus de-tune the filter from its optimal center frequency and gain. For the simulation being considered, the voltage gain at the center frequency is about 6 dB lower than the results from S-parameter simulations. This shows that the quality factor has also been de-tuned by the bias point changes due to large signal operation.

The signals at 195 MHz and 192 MHz in Figure 3.27 show signs of ground and supply bounce in the circuit. The simulations are run with bondwire models that represent the bondwires that are used to connect each pad on the integrated circuit with the pads on the printed circuit board that is used to facilitate the testing of the circuit. The bondwires are inductive and this inductance combined with the constantly changing current through the supply and ground results in fluctuations in the supply and ground voltage seen by the bandpass filter. This fluctuation, or bouncing, is transferred to the output of the filter, causing the distortion seen in Figure 3.27. When similar simulations are run without the bondwire models, this distortion is no longer seen. More parallel bondwires cause the inductance to decrease and also result in less distortion. Since the ground bounce is comparable in amplitude to the output signals at 195 MHz and 192 MHz, its impact can be more easily seen. Less distortion is seen on the 198 MHz signal because it is amplified to be more significant than the effect of the ground bounce.

3.3.7 Sensitivity and Small Input Signals

The sensitivity of the bandpass filter describes its ability to detect small input signals in the presence of noise. In Chapter 2, the minimum input voltage is specified to be 22.4 μV_{peak}. To test the bandpass filter's sensitivity, simulations are run with a smaller voltage of 20 μV_{peak} at 198 MHz, which would be just under the threshold of a detected signal. The filter is tuned to 198 MHz. These simulations show the lower limit of the filter's sensitivity. The simulations are performed using the test bench in Figure 3.15. The following subsections describe simulations results for two scenarios that can effect the filter's sensitivity to small signals. The first is when the effects of ground bounce are included in the simulation and the second is when the effects of input noise are included. These two scenarios are examined independent of each other.

In the Presence of Ground Bounce

As discussed in Section 3.3.6, ground bounce caused by the inductance of bondwires impairs the quality of small input signals. Using the test bench in Figure 3.15, a 20 μV_{peak} signal at 198 MHz is input into the bandpass filter when it is tuned to 198 MHz. Bondwire models on the supply, ground and all of the input and outputs add the effect of ground bounce to the simulation. The input and output signals from this transient simulation are shown in Figure 3.29.

The ground bounce effect on the input signal is between 100 μV_{peak} and 200 μV_{peak}, overwhelming the 198 MHz signal at 20 μV_{peak}. The 198 MHz signal cannot be distinguished on the input signal in the plot. However, at the output of the filter, the 198

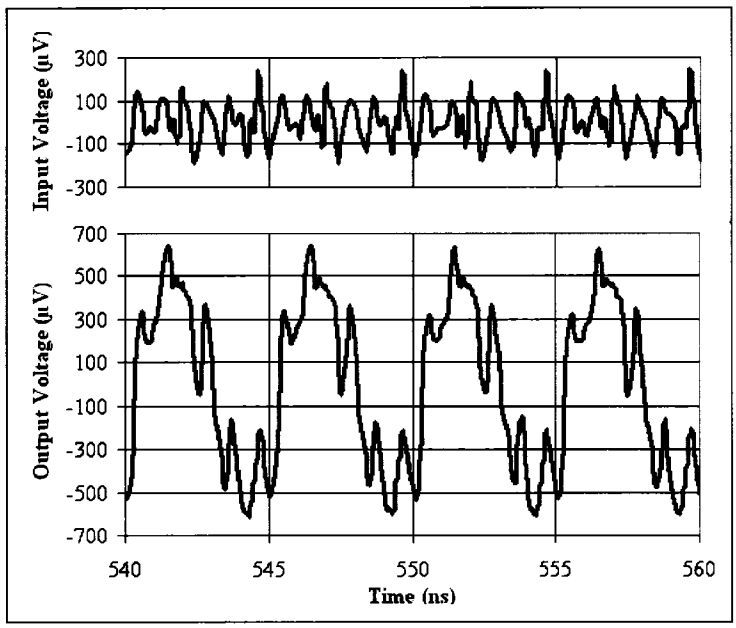

Figure 3.29: Input and output signals of the bandpass filter in the presence of ground bounce.

MHz signal is amplified by the filter and is clearly present. The ground bounce effect is still visible, causing distortion at the output, but now the 198 MHz signal is dominant. This shows that the bandpass filter is capable of amplifying the desired signal despite significant ground bounce effects.

In the Presence of Input Noise

The effect of input noise on the bandpass filter is tested with transient simulations using the test bench in Figure 3.15 with the addition of a noise source that is added to the signal source. In addition, no bondwire models are included in the simulation so the effect of input noise can be viewed in isolation. The noise source is an additive white noise source and it is set to have a peak amplitude of 40 μV_{peak}, twice the size of the input signal of 20 μV_{peak}. This represents noise that can be expected at the filter's input.

Through noise analysis simulations, the input buffer driving the bandpass filter is found to produce 24 μV_{peak} in a 10 MHz to 1 GHz bandwidth. Also, the thermal noise in the 70 MHz to 700 MHz bandwidth is calculated to be approximately 16 μV_{peak} as shown in Equations 3.3.6 and 3.3.7 [14]. This gives the total value of 40 μV_{peak}.

$$\begin{aligned} Noise\ Floor &= -174dBm/Hz + 10log_{10}(BW) \\ Noise\ Floor &= -174dBm/Hz + 10log_{10}(700MHz - 70MHz) \\ Noise\ Floor &= -86dBm \end{aligned} \tag{3.3.6}$$

$$\begin{aligned} -86dBm &= 10log\left(\frac{(V_{peak})^2}{2(50\Omega)(1mW)}\right) \\ V_{peak} &\approx 16\mu V \end{aligned} \tag{3.3.7}$$

Transient results of this simulation are shown in Figure 3.30. The top curve shows the input signal in the presence of the additive noise at the input. In the top curve, the 198 MHz signal can be seen with a large amount of noise. The lower curve shows the output of the bandpass filter where the 198 MHz signal has been amplified from the noise to 330 μV_{peak} and is clearly visible.

The simulation results with the effect of ground bounce and with the effect of input noise show that the bandpass filter is capable of detecting signals at the specified sensitivity level in the presence of these impairments and amplifying them to an appropriate level for driving the receive signal strength indicator. Due to the narrow bandwidth of the bandpass filter in this application, broadband input noise is not a big concern unless it is large signal noise. The simulations show that the effects of ground bounce have more of an impact on the transient performance of the bandpass filter and attempts are made to minimize it by using as many bondwires in parallel as possible to reduce their inductive effect. On the integrated circuit, six bondwires are used for ground and six

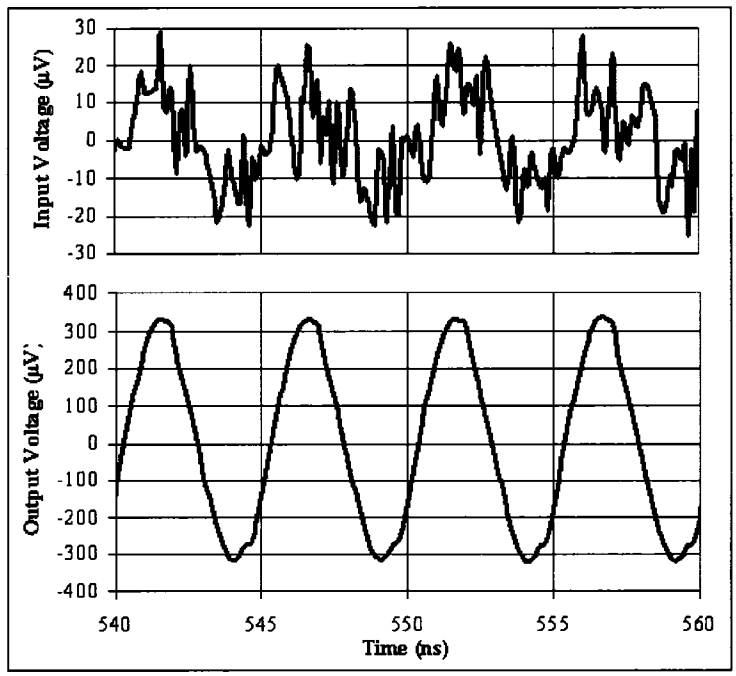

Figure 3.30: Input and output signals of the bandpass filter in the presence of noise.

are used for the supply.

3.3.8 Linearity and Large Input Signals

Due to the high gain of the bandpass filter, linearity becomes an issue for larger input signals. This is a common limitation of high quality factor active inductors [11, 17]. As described in Section 3.3.6, this is why the bandpass filter would have trouble operating with peak input signals over 50 mV. Though the bandpass filter still operates with input signals up to 10 mV, non-linearity does have an effect, lowering the gain and overall performance of the filter. This is an artifact of a high gain filter that is limited by four stacked transistors. These transistors make up the active inductor and its current sources. Each of these transistors requires enough voltage headroom so that $V_{DS} > V_{GS}$

- V_t and the transistor remains in saturation. As the transistor drops out of saturation, the circuit becomes non-linear. Since the 1.8 V supply is dropped across four transistors, it is more difficult for them to keep enough headroom. This becomes more of a problem with the high gain of the filter since output signal is larger and this takes up more of the voltage headroom.

The linearity of the bandpass filter can be quantified by its 1-dB compression point (P_{1dB}) and its third order intercept point (IP3). With the filter tuned to have a gain of approximately 20 dB at 200 MHz, a periodic steady state (PSS) simulation is run in Spectre using the test bench in Figure 3.15. For the IP3 to be measured, two input tones are used at 198 MHz and 202 MHz and the input power is swept from -70 dBm to -40 dBm. From this simulation, the linearity plot in Figure 3.31 is obtained. It shows an input-referred 1-dB compression point of -56 dBm and an input-referred third order intercept point (IIP3) of -46 dBm, which is approximately 10 dB higher, as expected [14, p.32].

Due to the nature of the television spectrum in which the bandpass filter is designed to operate, the second order intercept point (IP2) is also an important measure of linearity. Second-order intermodulation (IM2) can cause signals at two frequencies, f_1 and f_2, to create an IM2 tone at $f_1 + f_2$ or $f_2 - f_1$. Due to the wide bandwidth of 70 MHz to 700 MHz used in this application, it is possible that the two tones will generate an IM2 tone that is in band. This IM2 tone could be falsely detected as a signal.

As with the IP3 simulation, a PSS simulation is run on the bandpass filter to measure

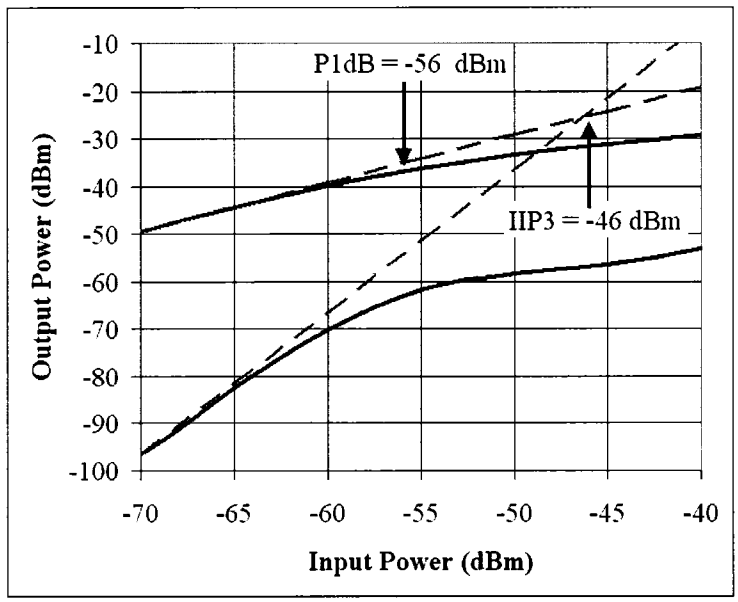

Figure 3.31: 1-dB compression point and third order intercept point of the bandpass filter when tuned for 20 dB gain at 200 MHz.

its IP2 when it is tuned to have approximately 20 dB of gain at 183 MHz. Two input tones are applied at 91 MHz and 92 MHz, which generate an IM2 tone at 183 MHz. These simulation conditions are used to later compare with measured results in Section 6.2.3. The input power of the two input tones is swept from -70 dBm to -30 dBm and the output power is measured at the frequency of one of these fundamental tones and at the frequency of the IM2 tone. These two curves are plotted in Figure 3.32. The intercept point of these curves is the second order intercept point. The simulated input-referred second order intercept (IIP2) is found to be -45 dBm. This value is comparable to the IIP3 value showing that both second and third order intermodulation are of equal importance to this application.

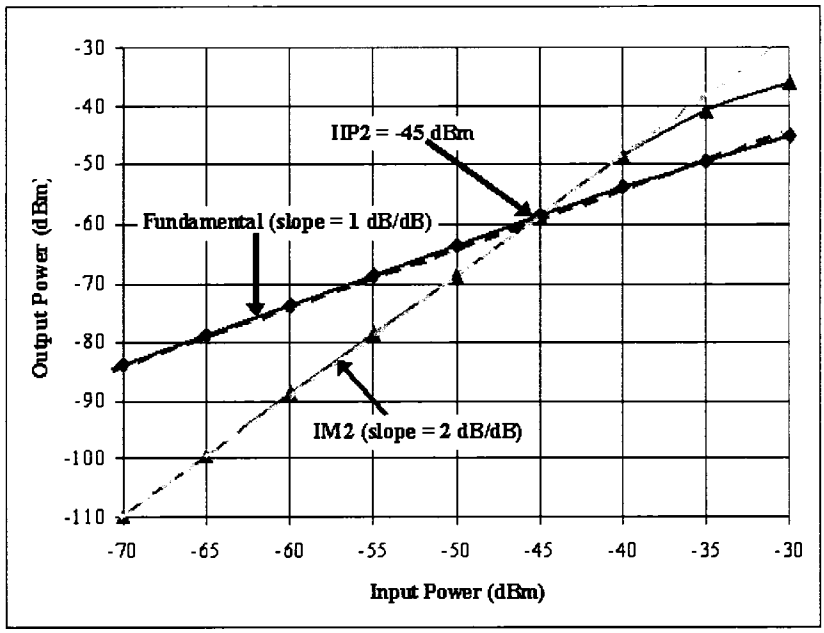

Figure 3.32: Second order intercept point of the bandpass filter when tuned for 20 dB gain at 183 MHz.

At the 1-dB compression point of -56 dBm the filter's gain is beginning to be non-linear. Using

$$\begin{aligned} P_{dBm} &= 10log\left(\frac{P_{Watts}}{1mW}\right) \\ P_{Watts} &= \frac{(V_{pp})^2}{8R}, \end{aligned} \tag{3.3.8}$$

the input voltage swing, V_{pp}, at the 1 dB compression point is found to 1.0 mV peak-to-peak. This is assuming a 50 Ω system, as will be used when testing the circuit. With a voltage gain of 20 dB, this results in an output voltage of 10 mV peak-to-peak. For higher input voltages, the gain will begin to diminish, resulting in a smaller increase in output voltage. As the gain at the center frequency of the filter is increased beyond 20 dB, the linearity degrades and the 1 dB compression point decreases.

The maximum amplitude of the signal at the output of the bandpass filter is approximately 160 mV peak-to-peak. Buffering is required at the output of the filter in order to

drive an off-chip 50 Ω load for testing. This buffering, which is discussed in Chapter 5, causes the signal to attenuate such that the maximum output signal is approximately 50 mV peak-to-peak under normal operation. Linearity is a known limitation with active inductors in general. Possible solutions to this limitation with respect to the whitespace detector application are discussed in the "Future Work" section of Chapter 7.

Issues With Blockers

Another problem caused by the nonlinear behavior of the bandpass filter that can cause the whitespace detector to miss the detection of whitespace in a band of interest is the presence of blockers. Blockers are high power signals in a frequency band that is close to the band to which the filter has been tuned. If the power of the blocker is higher than the 1-dB compression point of the bandpass filter, it can saturate the circuit and make it unable to detect the smaller, desired signal of interest [14, p.40]. Figure 3.33 helps illustrate this problem with blockers in the context of the tunable bandpass filter.

In Figure 3.33 there is a signal in the 174 MHz to 180 MHz television band that has a power of -83 dBm which is at the threshold of a detectable signal and whitespace. The whitespace detector bandpass filter would be tuned to this frequency to decide whether or not this band is whitespace. There is also a blocker signal transmitting in the 512 MHz to 518 MHz band which is at the maximum possible signal level of -15 dBm. Since this signal is well above the -56 dBm input-referred 1-dB compression point of the filter, it will cause the filter to become saturated. This will prevent the whitespace detector from determining whether or not there is whitespace in the band of interest. The nonlinearity

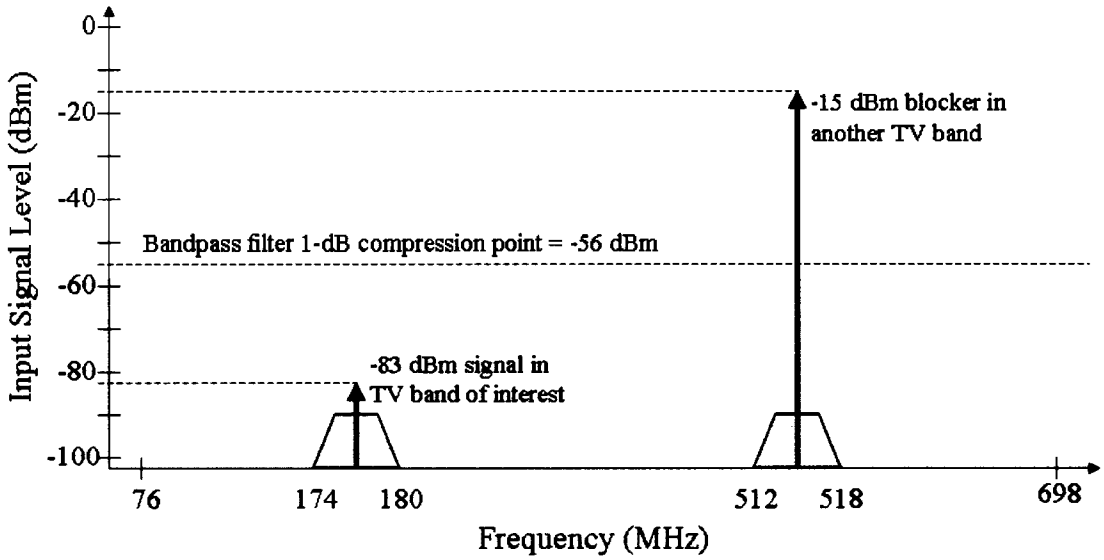

Figure 3.33: Minimum desired signal in the TV band of interest and a blocker in another TV band.

of the bandpass filter limits the ability of the overall whitespace detector design to handle large blockers.

3.3.9 Stability

The nature of the gyrator circuit used to create the active inductor in the tunable bandpass filter leads to potential instability in the circuit. The stability of gyrator circuits is discussed in [37] where it is explained that the feedback capacitance from the output to the input of the active inductor is responsible for this limitation. Since the feedback is necessary to the design of the active inductor, it can not be eliminated. In this design, the feedback capacitance is C_{gd2}. It can cause instability by creating an underdamped response in the filter [37]. There is also an inverse relationship between the damping factor of the circuit and its quality factor [37]. This causes high quality

factors to result in more underdamping and potential instability. As stated in [37], low self-resonant frequencies in the active inductor, formed by the inductance and parallel input capacitance, also increase the potential for instability.

Transient simulations of the bandpass filter using the test bench shown in Figure 3.15 show that it is stable for most combinations of tuning parameters that are expected to be used. However, there are limited cases where the filter may go unstable. An example of this is seen when the filter quality factor is tuned to be too high. As described in Section 3.1, increasing the control voltage, V_1, from 0 V decreases g_{ds3}. This reduces the series resistance of the active inductor and increases its quality factor and the bandpass filter gain at the center frequency. Figure 3.34 shows this trend when the other tuning parameters are held constant at $I_1 = 34\ \mu A$, $I_2 = 7\ \mu A$ and $V_2 = 1.05$ V. However, when V_1 reaches 45 mV, the gain at the center frequency begins to drop. This point coincides with the point where the transient response of the filter goes unstable. The unstable transient output response is shown in Figure 3.35. In this case, V_1 has been set to 80 mV. The unstable oscillation has a peak to peak amplitude of 120 mV at the output of the bandpass filter and is at a frequency of 173 MHz.

According to [37] the damping factor is inversely proportional to the input resistance of the active inductor. This resistance is in parallel with the resonator that determined the self-resonant frequency of the active inductor. A smaller input resistance in parallel with the resonator helps to keep stable. This effect is seen in simulation when a stabilizing resistor is placed in parallel with the input resistance, effectively lowering it. In

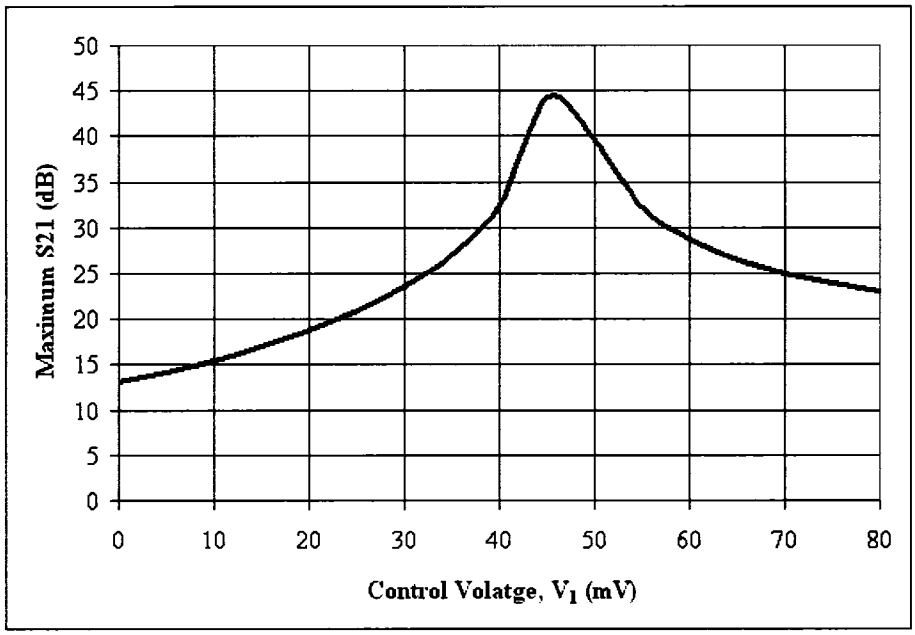

Figure 3.34: Maximum S21 gain at center frequency of bandpass filter as a function of the control voltage, V_1.

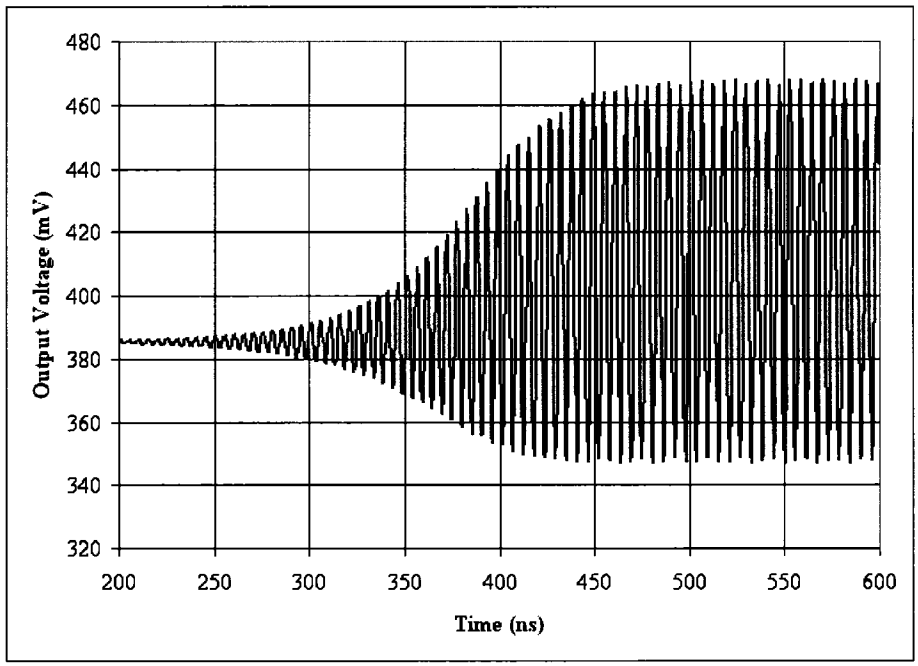

Figure 3.35: Unstable transient response at the output of the bandpass filter.

the tuning situation above where the filter became unstable, the presence of the resistor parallel to the input kept it stable. The drawback is that by increasing the damping factor, the quality factor of the filter is lowered. This lowers the precision of the bandpass filter, limiting it from reaching its maximum performance.

Since the degradation in the performance of the bandpass filter is undesirable, another option for controlling the stability is examined. For most normal operating conditions, the filter is stable and only certain tuning combinations cause instability. These combinations can be avoided in the tuning of the filter so that it does not enter an unstable situation. One potential instability situation occurs for very high gains that require very accurate tuning. It may be anticipated that when the chip is tested, such tuning will not be achieved and the instability will not be an issue. Other potential unstable situations occur for tuning combinations that do not lead to desirable center frequency and gain situations. For example, instability is seen when I_1 is tuned to the high end of the range and I_2 is tuned to the low end of the range. Under normal tuning situations, these currents should track and never be at the opposite extremes.

Should an unstable tuning situation be inadvertently reached, it is fortunate that it can be identified and avoided within the operation of the whitespace detector. The instability results in a large oscillating signal at the output of the bandpass filter. The receive signal strength indicator (RSSI) circuit will identify this signal as being larger than normal and that can give an indication that the bandpass filter has been tuned into an unstable region. When this condition is found, the filter tuning can be adjusted

so that it will return to stable operation.

A design decision was made not to limit the quality factor and precision of the filter with the stability resistor but to tune the filter in such a way so as to avoid instability situations.

3.4 Performance Summary and Comparison to the Literature

In Section 2.3 a performance summary of active inductors and active inductor based bandpass filters in literature is given. The performance of the active inductor and bandpass filter in this thesis is summarized and compared to literature in Tables 3.7 and 3.8. The reference for this thesis is denoted by a *. These two tables are the same as those in Section 2.3 with the addition of the results from this thesis.

Table 3.7: Active Inductor Performance Summary and Comparison of the Literature with Simulated Results

Ref.	Tech.	Power	Inductive Bandwidth	Inductance Range	R_S	Quality Factor	Max. Output Voltage
[11]	0.35 μm CMOS	0.6 mW	6.8 MHz - 2.97 GHz	30.9 nH @ 1 GHz	1.16 Ω @ DC	434 @ 1 GHz	4.5mV
[21]	0.35 μm CMOS	1.2 mW	10 MHz - 2.8 GHz	70 nH $\pm$20%	N/A	1970 @ 1.08GHz	30mV_{pp}
[20]	0.18 μm BiCMOS	15 mW	N/A	up to 40 nH	N/A	up to 10	N/A
[19]	1μm GaAs MESFET	90 to 240mW	100 MHz - 1 GHz	65 nH to 110 nH	-5.6 to 20.8 Ω	N/A	N/A
[22]	0.8 μm CMOS	N/A	up to 1 GHz	100's of nH	N/A	> 100	13.5mV
*	0.18 μm CMOS	below 0.4 mW	up to 700 MHz	30 nH to 3 μH	< 5 Ω	> 100	14mV_{pp}

As shown in Table 3.7, the active inductor presented in this thesis has a lower power dissipation in comparison with those presented in the literature. This power is less than 0.4 mW and varies with the tuning of the inductor. This power does not include the power required for current mirror biasing and the source follower output buffer. It is based on the currents I_1 and I_2 from the 1.8 V supply. The worst case inductive bandwidth is lower than those presented in the literature. The upper limit of the bandwidth shows the inductor's self-resonant frequency. The lower inductive bandwidth is seen when the inductance is tuned to its maximum value. When the inductance is tuned to a lower value, the inductive bandwidth is as high as 2 GHz, which is comparable to those in the literature for similar inductance values. The inductance tuning range of the active inductor in this thesis is much wider than the other results from the literature in Table 3.7. The lower end of this range, in the tens of nanohenries is comparable to the other designs. However, at the high end, it can be tuned to much larger inductances in the low microhenries range. These inductances allow the bandpass filter to be tuned to its lower frequencies. The series resistance and quality factor of this design are comparable to the other designs and due to the tunability, very small series resistances and very high quality factors can be achieved. The maximum output voltage of 14 mV peak-to-peak is seen at the output of the active inductor's source follower. This is at the 1 dB compression point when the gain of the filter is set to 20 dB. This compares well with the other designs. A higher maximum voltage up to 50 mV peak-to-peak can actually be achieved but the linearity is worse at this point.

Table 3.8: Active Inductor Based Bandpass Filter Performance Summary and Comparison

Ref.	Description	Tech.	Power	Center Frequency Range	Filter Quality Factor	IIP3 or DR
[11]	C_{filt} = 0.7pF	0.35 μm CMOS	0.6 mW	0.93 - 1.03 GHz	> 25	DR = 30dB @ 1GHz, Q=25
[29]	Differential	0.35 μm CMOS	17 mW	400 MHz - 1.1 GHz	2 to 80	IIP3 = -15dBm @ Q = 40
[22]	C_{filt} = 0.7pF	0.8 μm CMOS	N/A	around 500 MHz	80 @ 500MHz	N/A
[17]	6th order G_m-C	0.5 μm CMOS	90 mW	around 70 MHz	350 @ 70MHz	IIP3 = -10dBm
*	C_{filt} = 1.55pF	0.18 μm CMOS	below 1.6 mW	70 MHz - 700 MHz	> 100	IIP3 = -43dBm @ Gain = 20dB

As shown in Table 3.8, the bandpass filter in this design uses significantly less power than the designs in [17, 29] and comparable power to the design in [11]. This power includes the active inductor plus the addition of current mirror biases and the source follower output buffer power consumption. The bandpass filter in this thesis has a wider tuning range than the other bandpass filters. It is designed for more of a broadband application as opposed to a narrowband one. The filter can achieve comparable quality factors to other designs. Its IIP3 is lower than the other designs showing that it has more limitations in the area of linearity.

Table 3.9 shows the specifications and the performance achieved in simulations of the tunable bandpass filter. The specifications are achieved, though the linearity could be improved further. Linearity and stability are two areas for future work and improvement with regards to the design of the tunable bandpass filter.

Table 3.9: Specifications and Performance of the Tunable Bandpass Filter

Specification	Targeted Performance	Performance Achieved
Center Frequency Range	70 MHz to 700 MHz	Achieved
3 dB Bandwidth at Center Frequency	< 6 MHz	Achieved
Minimum Input Signal (Sensitivity)	-83 dBm (22.4 μV_{peak} in 50 Ω system)	Achieved
Linearity (IIP3)	High	P_{1dB} = -56 dBm @ Gain = 20 dB, 200 MHz
Power Consumption	Low	< 1.6 mW including biasing and source follower
Circuit Area	Small	50 μm × 70 μm including biasing and source follower

3.5 Chapter Summary

The design of the tunable bandpass filter for the whitespace detector is presented in this chapter. Its role is to tune to a narrow frequency band and filter out all other frequencies. It is built using a high quality factor active inductor. Equations to predict the inductance and series resistance of the active inductor are developed. This theory is extended to the center frequency and quality factor of the bandpass filter. Trends for the tuning of the active inductor and bandpass filter using bias controls are also analyzed.

The circuit implementation and layouts of the circuits are discussed. Simulations show that the inductance and series resistance of the active inductor follow the predicted trends. Small signal simulations are used to analyze the tuning of the bandpass filter's center frequency and quality factor and to ultimately develop an algorithm for tuning the filter. Large signal simulations show the filters transient behavior. The filter's sensitivity, linearity and stability are simulated and analyzed.

The performance of the active inductor and bandpass filter is compared to other designs in literature and is found to have a larger tuning range and comparable quality factors. The circuit suffers from poor linearity which is a common problem for active inductors. The bandpass filter's performance is suitable for the application in the whitespace detector and it meets the required specifications.

Chapter 4

Receive Signal Strength Indicator

The principle behind the whitespace detector is to tune a filter to selected channels and then measure the power of the signal within each of these channels. If the signal level is below a certain threshold, it is decided that no signal is present in that channel. The role of the Receive Signal Strength Indicator (RSSI) circuit is to measure the signal level at its input, which comes from the channel selected by the bandpass filter. The RSSI takes the form of a piece-wise linear logarithmic amplifier [12]. The amplitude of the RF input to the RSSI can vary exponentially but is then translated into a linear output. Hence, the output has a logarithmic relationship to the amplitude of the input signal. As specified in Chapter 2, the RSSI input signal strength can vary from -60 dBm to -10 dBm. This corresponds to the output signal range from the bandpass filter. The RSSI must also work over a frequency range from 70 MHz to 700 MHz.

A block diagram of the RSSI that is designed for this thesis is shown in Figure 4.1. It takes a differential RF input voltage signal while the output is a DC current. An output voltage is obtained by passing the current through a resistor. The main building blocks of the RSSI are limiting amplifiers, rectifiers and a low pass filter. A limiting

amplifier amplifies its input signal as long as the input is relatively small. Once the input amplitude gets larger, the gain is reduced and the output signal is limited and gets clipped. The rectifier circuit takes a differential AC input and rectifies it, creating an output that is either always positive or always negative. A low pass filter at the output of the rectifiers filters any high frequency components, leaving a signal that is close to a DC value. In the case of the full-wave rectifiers and low pass filter that have been designed, the magnitude of the DC component of the output is inversely proportional to the amplitude of the input signal.

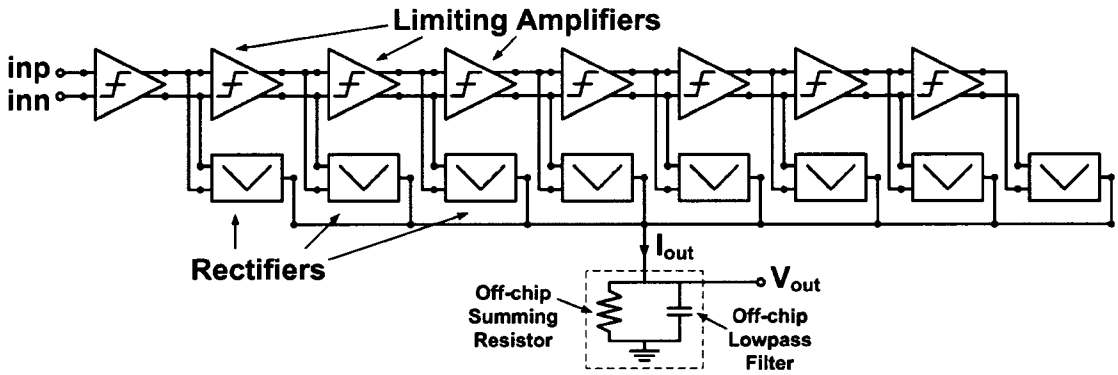

Figure 4.1: Receive signal strength indicator schematic.

In order to form the logarithmic amplifier from these components, several limiting amplifiers are cascaded. Each subsequent limiting amplifier provides more gain to the signal so that the signal that has passed through several amplifiers is limited. The signal from the output of each of the cascaded limiting amplifiers is input into its own rectifier circuit. Each rectifier outputs a current that has a DC component that is inversely proportional to its input amplitude. The signal that has passed through more limiting amplifiers is larger in amplitude and therefore generates a current with a smaller DC

component at the output of the rectifier. All of the rectifier output currents are summed together across a resistor. A capacitor is connected across the resistor, acting as a low pass filter that removes the high frequency signal, leaving a signal that is a DC value.

A more detailed description of how the RSSI and its building blocks work follows in the discussion in Section 4.1. The implementation and simulation results for these circuits are presented in Section 4.2. In Section 4.3 the simulated performance of the RSSI is summarized and compared to other RSSIs in literature.

4.1 Receive Signal Strength Indicator Theory

This section describes the theory behind the functionality of the the circuits that make up the receive signal strength indicator. The limiting amplifier and rectifier theory are discussed in Section 4.1.1 and Section 4.1.2, respectively. This is followed, in Section 4.1.3, with the description of how these circuits are used to build up the RSSI and the theory behind how it works.

4.1.1 The Limiting Amplifier

The circuit schematic of a limiting amplifier is shown in Figure 4.2. It consists of an NMOS differential pair, M_1 and M_2, and NMOS load transistors, M_3 and M_4. It is biased by a current mirror that is shared by all of the identical limiting amplifiers that make up the logarithmic amplifier. M_5 is the half of the current mirror that provides the current to the limiting amplifier.

In order to determine the overall gain of the logarithmic amplifier and the number

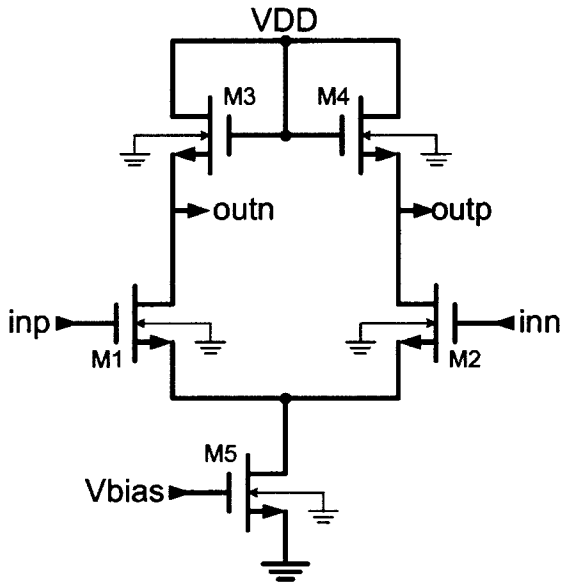

Figure 4.2: Schematic of the limiting amplifier.

of required limiting amplifier stages, the gain of an individual limiting amplifier must be determined. For this analysis, M_5 is treated as an ideal current source and the node at its drain is considered a virtual ground because M_5 has a large output impedance. Due to the differential input and output of the amplifier in Figure 4.2, the gain of the amplifier can be determined by analyzing the small-signal model for transistors M_1 and M_3. This small-signal schematic can be seen in Figure 4.3. Since the node at the drain of M5 is treated as a virtual ground the effect of the bulk to source voltage of M_1 is ignored.

The circuit in Figure 4.4 is a simplified version of that shown in Figure 4.3. Here, $V_{in} = V_{gs1}$ and $V_{out} = -V_{gs3}$. The resistor, R_1 is the parallel combination of r_{o1} and r_{o3}. C_1 is the combination of C_{gs1} and the Miller capacitance from C_{gd1}. C_2 is the combination of C_{gs3}, C_{db3}, C_{db1} and the Miller capacitance from C_{gd1}.

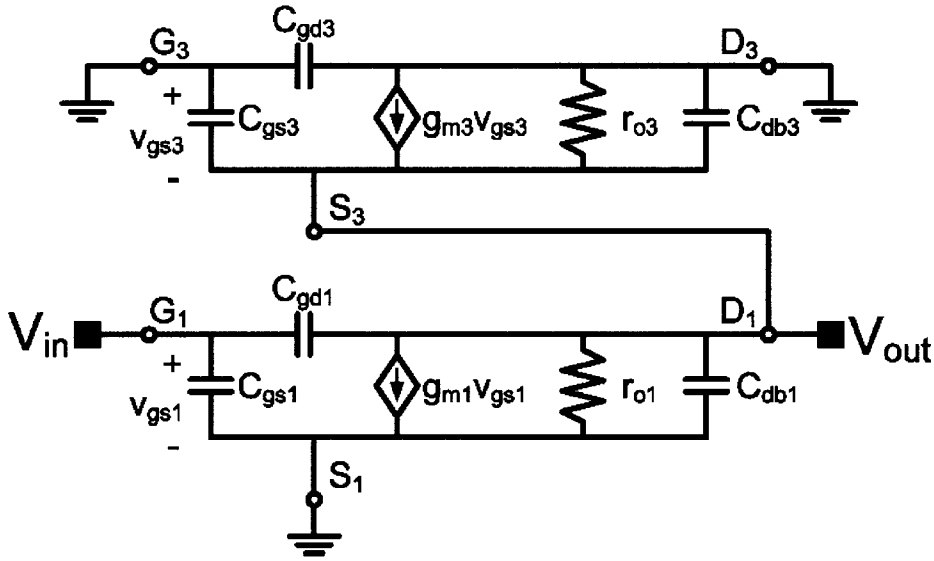

Figure 4.3: Small-signal schematic of the limiting amplifier.

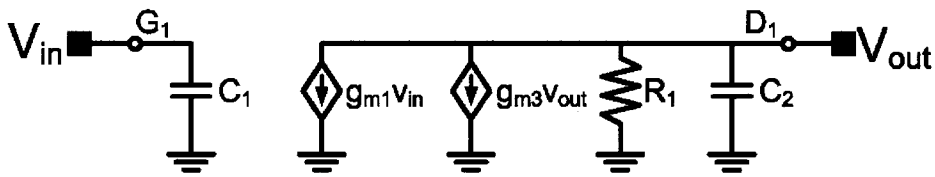

Figure 4.4: Simplified small-signal schematic of the limiting amplifier.

The DC gain of the circuit can be derived by ignoring the capacitances in Figure 4.4 and solving the nodal equation at the V_{out} node to give

$$A_{dc} = \frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{g_{m3} + \frac{1}{R}} \tag{4.1.1}$$

where R is given by

$$R = \frac{r_{o1} r_{o3}}{r_{o1} + r_{o3}}. \tag{4.1.2}$$

If it is assumed that $g_{m3} \gg \frac{1}{R}$, then the gain can be simplified further to

$$A_{dc} = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{(W/L)_1}{(W/L)_3}} \tag{4.1.3}$$

as shown in [12]. This gain is positive because it accounts for the differential nature of the limiting amplifier. Since the transconductance for an NMOS transistor in saturation can be approximated by

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}, \tag{4.1.4}$$

the gain can be related to the ratio of the square-root of differential pair and load transistor sizes [12]. This means that the gain can be controlled by setting the sizes of these transistors.

The high frequency gain of the limiting amplifier can be determined by adding the capacitance, C_2, in parallel with the resistance, R, to Equation 4.1.1. This yields

$$A(s) = \frac{-g_{m1}}{g_{m3} + \frac{sRC_2+1}{R}} = \left(\frac{-g_{m1}}{g_{m3} + \frac{1}{R}}\right)\left(\frac{1}{1 + sC_2(g_{m3} + \frac{1}{R})^{-1}}\right) \tag{4.1.5}$$

where C_2 is given by

$$C_2 = C_{gs3} + C_{db3} + C_{db1} + C_{gd1}(1 - 1/A_{dc}). \tag{4.1.6}$$

C_2 combines a number of capacitances in parallel, including the Miller effect on C_{gd1}. The 3-dB bandwidth of the limiting amplifier occurs at the pole in Equation 4.1.5 and can be written as

$$\omega_{3dB} = \frac{g_{m3} + \frac{1}{R}}{C_2}. \tag{4.1.7}$$

4.1.2 The Rectifier

The circuit schematic for the rectifier is shown in Figure 4.5. It consists of stacked differential pairs, M_1 to M_6, in a Gilbert cell configuration that is connected in such a way as to create a four-quadrant MOS multiplier [40]. The PMOS transistors, M_7 and M_8, form the loads of the circuit. M_8 and M_9 act as a current mirror to provide the output current of the rectifier. The rectifier is biased by a current mirror that is shared by all of the identical rectifiers in the RSSI. M_{10} is the half of the current mirror that is in each rectifier.

The role of this rectifier circuit is to take an AC input voltage and generate two rectified output currents, one that is always positive and one that is always negative relative to the common mode current. The output currents have a DC component that is proportional to the amplitude of the input voltage when it is the positive rectified signal, and is inversely proportional when it is the negative rectified signal. Using a low pass filter on one of these output currents removes the high frequency component, leaving a DC current that is either proportional or inversely proportional to the amplitude of the input voltage.

The following describes the ideal operation of the rectifier in Figure 4.5. The idealized

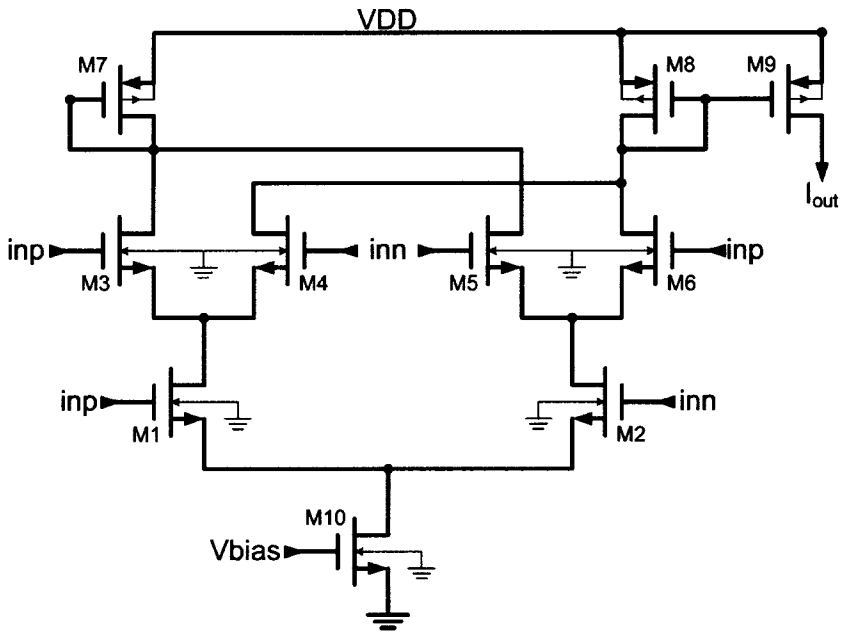

Figure 4.5: Schematic of the rectifier.

theoretical waveforms in Figure 4.6 help in the description.

The top waveform is the positive differential input voltage (inp). The upper waveform from the bottom graph is the rectified current through transistor M_7 that is always greater than $I_{max}/2$ and positive with respect to the common mode output current. The lower waveform is the current through transistor M_8 that is always less than $I_{max}/2$ and negative with respect to the common mode output current. This is the current that gets mirrored into M_9 and becomes the output current that goes to the summing resistor and low pass filter. The maximum current, I_{max}, is the bias current provided by the current mirror transistor, M_{10}. The plot also shows the average currents through M_7 and M_8. The output current that is mirrored from transistor M_8 to M_9 is summed with the currents from other rectifiers and passed through an output resistor and low pass

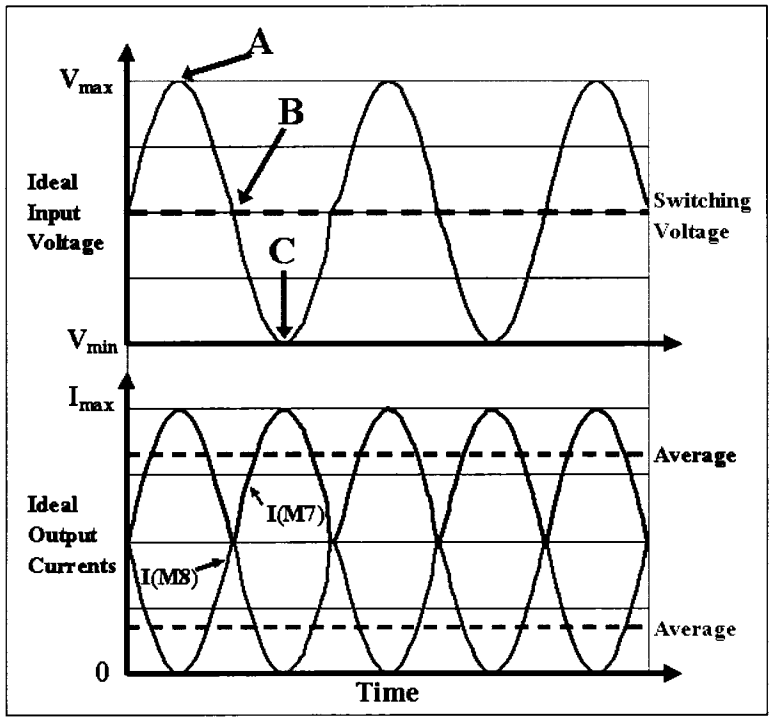

Figure 4.6: The ideal theoretical transient response of the full-wave rectifier.

filter capacitor. This resistor and capacitor create a DC voltage that is proportional to the average current through M_8.

Three points, A, B and C, are labelled in Figure 4.6. "A" corresponds to the maximum input voltage, "B" corresponds to the common mode point voltage when the input is switching and "C" corresponds to the minimum input voltage. At point "C", inn is at its maximum. The circuits in Figure 4.7 A, B and C correspond to these three conditions for the input voltage. The rectifier steers the bias current through various paths to the load transistors based on the differential input voltage it sees. When the input voltage is high, as in condition "A", transistors M_1 and M_3 are on and all of the current is steered through M_7. Similarly, when the input voltage is low and inn is high, as in condition "C", transistors M_2 and M_5 are on and all of the current is also steered through M_7. In both of these cases, no current is steered through M_8 to the output of the rectifier. When the input voltage reaches its switching point at condition "B", the current is split evenly through four paths so that each path takes a quarter of the current. Half of the current flows through M_7 and half flows through M_8. As the input voltage switches, the current through M_7 switches between I and I/2 and the current through M_8 switches between 0 and I/2. Both currents change at twice the frequency of the input signal.

As the input voltage switches, it currents transition between states "A", "B" and "C". When the input voltage amplitude is small, as in Figure 4.8A, it spends more time near the switching point of condition "B". The resulting currents are therefore closer

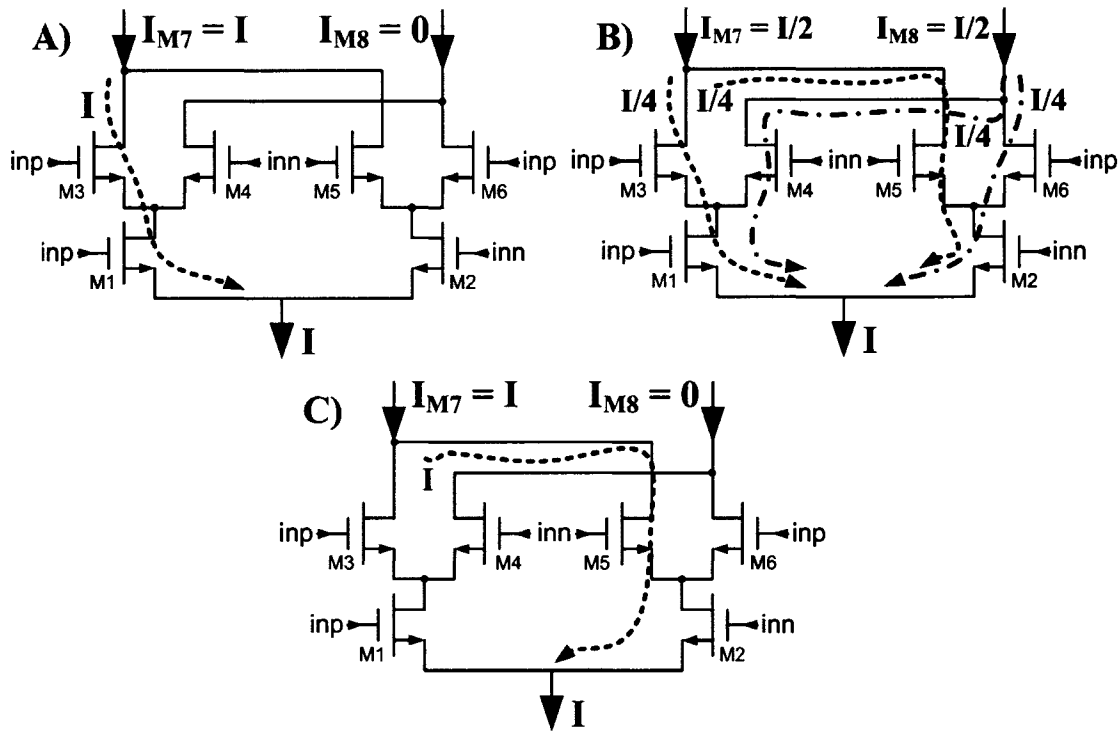

Figure 4.7: Current steering in the rectifier. A: When the input voltage to the rectifier is at its maximum, M_1 and M_3 steer all of the current through M_7 and none of it through M_8. B: When the input voltage to the rectifier is at its switching point, a quarter of the current is steered through each of the four paths causing half of the current to go through M_7 and half of it through M_8. C: When the input voltage to the rectifier is at its minimum (and inn is at its maximum), M_2 and M_5 steer all of the current through M_7 and none of it through M_8.

to being split half and half between M_7 and M_8. When the input voltage amplitude is large and limited, as in Figure 4.8B, it spends a larger percentage of its period near its maximum and minimum points of conditions "A" and "C". The resulting current through M_7 is closer to the maximum current and the current through M_8 is closer to zero.

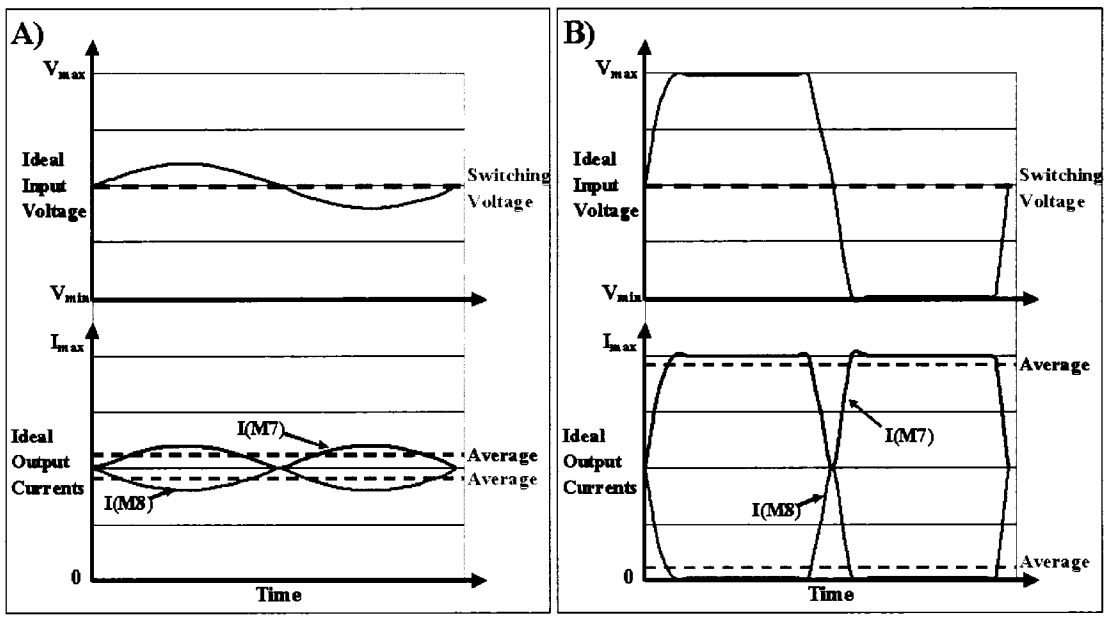

Figure 4.8: Theoretical transient input voltage and output current of the rectifier. A: When the amplitude of the input voltage is small, the currents through both M_7 and M_8 are close to $I_{max}/2$. B: When the amplitude of the input voltage is large and voltage-limited, the current through M_7 is close to I_{max} and the current through M_8 is close to zero.

The overall result is that for large input signals, the DC component of the output current of the rectifier that flows through M_8 is close to zero while for small input signals it is close to half the bias current. This results in the inversely proportional relationship between the input voltage and output current.

4.1.3 The RSSI

The receive signal strength indicator (RSSI) is built from cascaded limiting amplifiers, rectifiers, and an output low pass filter as shown in Figure 4.1. Based on the specifications and the performance of the sub-blocks, the number of stages required for the RSSI can be determined. The number of stages is denoted as N and is represented in Figure 4.9. The input dynamic range for the RSSI gives the lowest possible input signal amplitude with which the RSSI is expected to perform. This smallest signal amplitude is denoted as $V_{in,min}$. The total gain of the RSSI, A_{RSSI}, is the gain required such that $V_{in,min}$ results in an output after the final stage limiter of the RSSI that just begins to clip. This output is denoted as $V_{out,clip}$ and can be determined from the performance of a limiter. Based on this, the total gain of the RSSI can be written as

$$A_{RSSI} = \frac{V_{out,clip}}{V_{in,min}}. \tag{4.1.8}$$

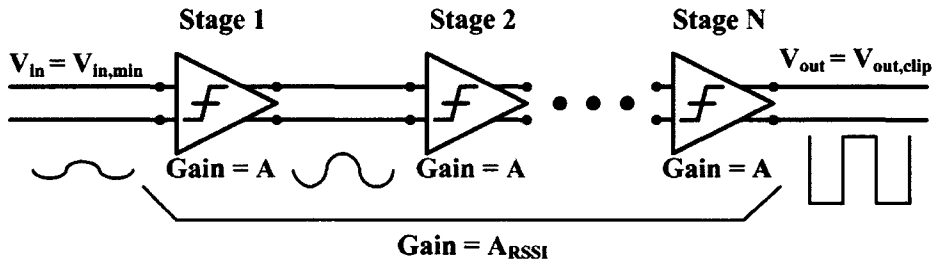

Figure 4.9: Block diagram showing the important values used to calculate the required number of limiting amplifier stages, N. This occurs when the input is $V_{in,min}$ and the output is $V_{out,clip}$. In this scenario, the gain of each limiter is A and the overall gain of the N stages is A_{RSSI}.

Knowing $V_{in,min}$ from the specification and $V_{out,clip}$ from the performance of the limiting amplifier, A_{RSSI} can be determined. The gain, A, of each limiting amplifier

stage is derived in Section 4.1.1. When the input level is $V_{in,min}$ and the final output level is $V_{out,clip}$, all of the limiting amplifier stages are providing their full amount of gain, A, and the maximum gain of the RSSI, A_{RSSI}, [12] is given by

$$A_{RSSI} = A^N \tag{4.1.9}$$

where N is the number of stages that can now be determined.

There is a rectifier at the output of each of the N limiting amplifiers stages. The input to the nth rectifier is the limiter output signal, V_n. As discussed in Section 4.1.2, the output of each rectifier is a rectified current. For the nth rectifier, the DC component of this current will be denoted by I_n. The output currents from each rectifier are summed through the output resistor, R_{out}, to produce the DC output voltage, V_{out}. The output voltage can be described by

$$\begin{aligned} V_{out} &= I_{out} R_{out} \\ V_{out} &= R_{out} \sum (I_n). \end{aligned} \tag{4.1.10}$$

For the ideal situation, a large input to the RSSI causes all of the limiters to clip their outputs. This is depicted in Figure 4.10A. Due to the inverse relationship between the input amplitude and the DC component of the output current, as discussed in Section 4.1.2, all of the rectifiers have an output current of $I_n = 0$. This means the total output current through the summing resistor is $I_{out} = 0$ and the output voltage is $V_{out} = 0$.

In the other extreme case, shown in Figure 4.10B, the input to the RSSI is very small and all limiting amplifiers provide full gain until the final one just begins clipping. This will result in the maximum output current, $I_{out,max}$, and the corresponding maximum output voltage, $V_{out,max}$. The size of the output resistor is chosen from these values

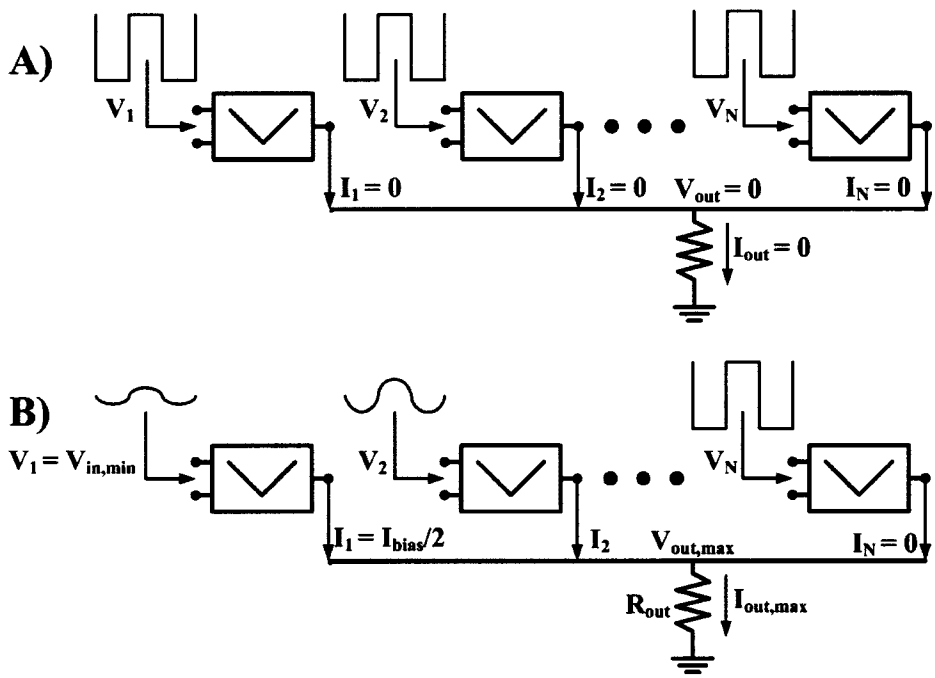

Figure 4.10: Depiction of the output currents from the rectifiers. In A, the input to each of the rectifiers is the clipped output from a limiter. The resulting output current of each rectifier is zero. In B, the input to the first rectifier is $V_{in,min}$. This scenario gives the maximum total output current of $I_{out,max}$. Knowing $V_{out,max}$, the value of the output resistor, R_{out} can be calculated.

based on

$$R_{out} = \frac{V_{out,max}}{I_{out,max}}. \tag{4.1.11}$$

In the case of this design, the maximum theoretical output voltage is $V_{out,max} = 1.8$ V. $I_{out,max}$ is the sum of the DC components of each of the rectifier output currents, I_1 to I_N. As discussed in Section 4.1.2, I_1 will be equal to half the bias current since the input to rectifier 1 is very small. I_N will be close to zero since the input to rectifier N is very large.

In summary, based on the input values from the specification along with the performance of the limiting amplifiers and rectifiers, the RSSI can be assembled by determining the required number of stages and the value of the output summing resistor.

4.2 Implementation and Simulation of the Receive Signal Strength Indicator

This section describes how the receive signal strength indicator (RSSI) is implemented in the 0.18 μm CMOS technology. The implementation is based on a combination of theory from Section 4.1 and simulations. Simulation results showing the performance of the circuits is also presented. The implementation and simulations of the limiting amplifier and rectifier are discussed in Section 4.2.1 and Section 4.2.2, respectively. This is followed, in Section 4.2.3, with the implementation and simulation results of the RSSI.

4.2.1 The Limiting Amplifier

The circuit schematic of the limiting amplifier shown in Figure 4.2 is implemented in a 0.18 μm CMOS technology. The transistor sizes are summarized in Table 4.1.

Table 4.1: Transistor Sizes in the Limiting Amplifier Shown in Figure 4.2

Transistor	# of Fingers $\times$ Width/Finger = Total Width (μm)	Length (μm)
M1	$4 \times 5 = 20$	0.18
M2	$4 \times 5 = 20$	0.18
M3	$1 \times 1 = 1$	0.18
M4	$1 \times 1 = 1$	0.18
M5	$12 \times 5 = 60$	0.50

The width of the current tail transistor, M_5, is chosen to provide 300 μA of current to each limiting amplifier and it is in a 1:6 ratio within a current mirror. The length of M_5 is non-minimal to lower the effect of V_{DS} on the current. As explained in Section 3.2, the longer transistor length gives the current mirror a higher output resistance that allows it to provide a more constant current over a wider range of V_{DS} [38, p.405]. The sizes of the NMOS differential pair transistors, M_1 and M_2, and the NMOS loads, M_3 and M_4, are chosen to give the desired gain for the limiting amplifier. Based on Equation 4.1.3, theory predicts that for these transistor sizes the DC gain should be $A_{dc} = 4.47$ V/V or 13 dB. For a low input amplitude and at low frequencies, transient simulation results on the limiting amplifier show the low frequency gain to be about 3.44 V/V or 10.73 dB. Part of this discrepancy is due to the finite load impedance of the amplifier. When this is accounted for using Equation 4.1.1 and Equation 4.1.2, a more accurate DC gain is calculated to be 3.98 V/V or 12 dB. These calculations can be seen in Equations 4.2.1

and 4.2.2 using the DC operating parameters of the amplifier.

$$R = \frac{r_{o1}r_{o3}}{r_{o1} + r_{o3}} = \frac{(15.6k\Omega)(44.5k\Omega)}{15.6k\Omega + 44.5k\Omega} = 11.6k\Omega \tag{4.2.1}$$

$$A_{dc} = \frac{g_{m1}}{g_{m3} + \frac{1}{R}} = \frac{(2.24mA/V)}{476\mu A/V + 86.2\mu A/V} = 3.98V/V \tag{4.2.2}$$

The Limiting Amplifier Layout

The layout of the limiting amplifier is shown in Figure 4.11. All of the input and output ports are labelled, as well as each of the components.

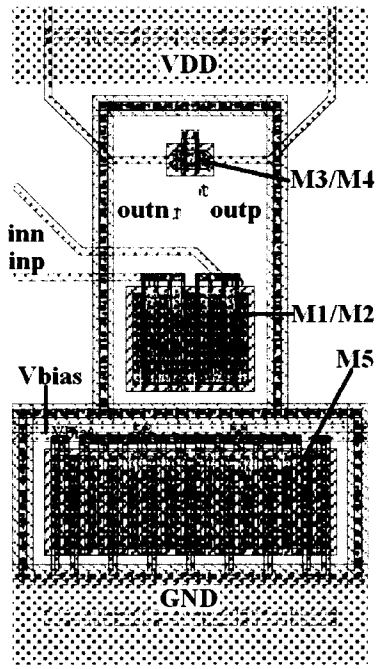

Figure 4.11: The layout of a limiting amplifier. (Refer to the layout key in Figure B.1 of Appendix B to identify all layers used in the layout.)

The transistors that form the differential pair (M_1 and M_2) are laid out with interdigitated fingers. This one-dimensional matching technique allows the transistors to be better matched against temperature and doping gradients. Since the RSSI requires

several limiting amplifiers, the layout is designed so it can be placed in an array that makes efficient use of area and allows each of the limiter sub-blocks to be connected together.

From the layout of the limiting amplifier, an extracted version of the schematic is generated. This extracted representation of the circuit includes parasitic capacitances. All high frequency simulations that are described in the following section are performed using this post-layout representation of the circuit.

Limiting Amplifier Simulation Results

The voltage gain of the limiting amplifier that is extracted from the layout is determined from transient simulations using the test bench shown in Figure 4.12. $V_{DD} = 1.8$ V, the bias current is set to provide 300 μA and a peak input voltage of 1 mV is used. The limiting amplifier is loaded with another limiting amplifier to represent a realistic load capacitance.

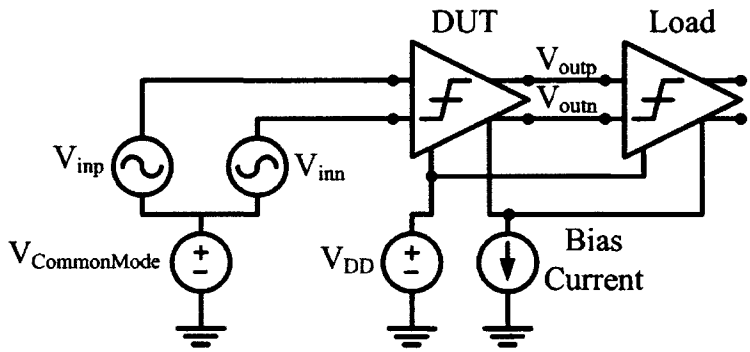

Figure 4.12: The test bench for running transient simulations on the limiting amplifier.

The voltage gain is calculated as $20\log(V_{outp}/V_{inp})$. Figure 4.13 shows this voltage gain versus frequency. Figure 4.13 also shows the theoretical expectation for the voltage

gain based on Equation 4.1.5. The values for this calculation are taken from the DC operating parameters for the circuit. Additional capacitance is added to the value of C_2 to account for the input capacitance of the second limiting amplifier which is loading the first one. The simulated gain is about 1.25 dB below the theoretical expectation.

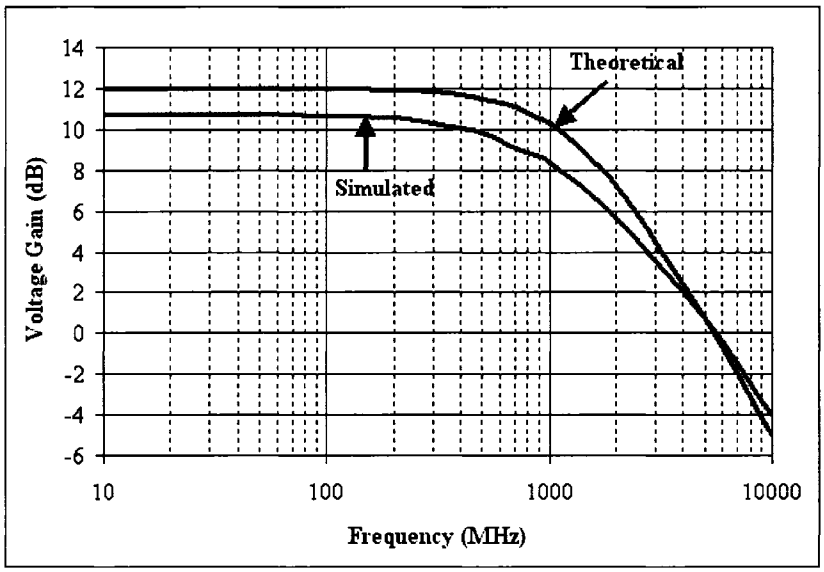

Figure 4.13: The Theoretical and Simulated Gain of the Limiting Amplifier

From Equation 4.1.7, the 3 dB frequency of the amplifier is expected to be 1.42 GHz. From the simulation results, it turns out to be 1.17 GHz. The desired range of operation for the limiting amplifier is 70 MHz to 700 MHz, as is required for the whitespace detector. This band falls below the 3 dB frequency of the amplifier but there is a 1.5 dB degradation in gain across the band. This performance degradation is a compromise with the added power that would be required to increase the 3 dB frequency. The performance variation over frequency has to be accounted for in the overall design of the receive signal strength indicator.

The limiting amplifier provides linear gain for low input signals but begins to limit or clip the output as the input gets larger. Figure 4.14 shows the input to output characteristic of the limiting amplifier for a 100 MHz signal. The linear gain is seen for peak-to-peak differential inputs below 200 mV. After 200 mV, the output begins to clip. For inputs above 600 mV differential, there is very little increase in output voltage as it eventually levels off to about 1.3 V peak-to-peak differential. At this point, the limited output signal is a square wave.

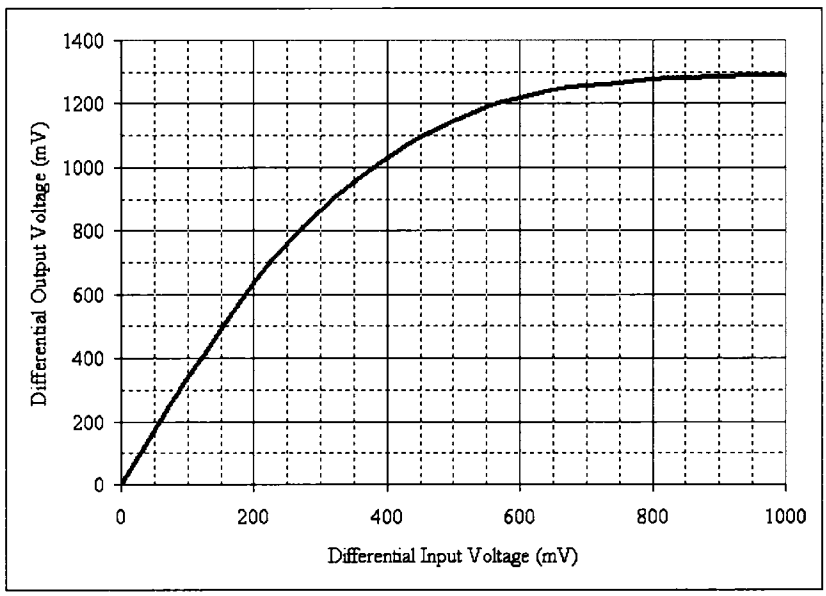

Figure 4.14: The input to output characteristic of the limiting amplifier.

4.2.2 The Rectifier

The circuit schematic for the rectifier shown in Figure 4.5 is implemented in the 0.18 μm CMOS process. The transistor sizes are summarized in Table 4.2.

The width of the current tail transistor, M_{10}, is chosen to provide 50 μA of current

Table 4.2: Transistor Sizes in the Rectifier Shown in Figure 4.5

Transistor	# of Fingers × Width/Finger = Total Width (μm)	Length (μm)
M1	1 × 4 = 4	0.18
M2	1 × 4 = 4	0.18
M3	1 × 4 = 4	0.18
M4	1 × 4 = 4	0.18
M5	1 × 4 = 4	0.18
M6	1 × 4 = 4	0.18
M7	2 × 6 = 12	0.60
M8	2 × 6 = 12	0.60
M9	2 × 6 = 12	0.60
M10	2 × 5 = 10	0.50

to the rectifier through a current mirror with a 1:1 ratio. M_{10} has a channel length that is larger than the minimum available. As explained in Section 3.2, this longer length results in a higher output resistance for the current mirror [38, p.405]. The higher output resistance means that the current mirrored by the current mirror remains more constant even if both halves of the current mirror have a different V_{DS}. The sizes of the differential pairs transistors, M_1 to M_6, and the PMOS load transistors, M_7 to M_9, are chosen from iterative transient simulations using the test bench in Figure 4.15.

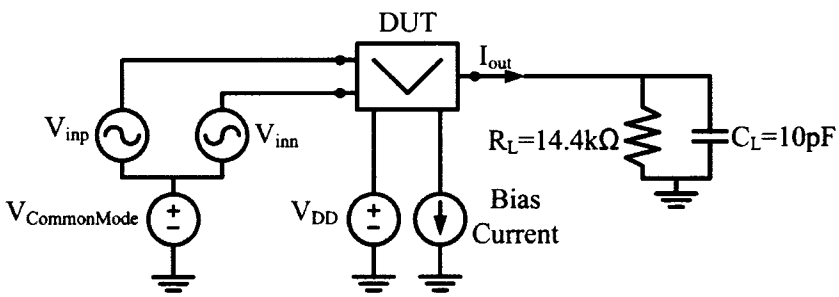

Figure 4.15: The test bench for running transient simulations on the rectifier.

In these simulations, a parametric sweep of the input amplitude to the rectifier is

done which represents the range of amplitudes expected from the output of the limiting amplifiers. The parametric sweep is run multiple times while the widths of the rectifier's transistors are varied from 2 μm to 16 μm. This is done while attempting to achieve an output current with a DC component that is close to zero when a large, limited input signal is applied. Also, the goal is to achieve an output current with a DC component that is close to half the bias current when the input amplitude is very small. The final transistor values shown in Table 4.2 provide results that meet these objectives.

The Rectifier Layout

The layout of the rectifier is shown in Figure 4.16. All of the input and output ports are labelled, as well as each of the components.

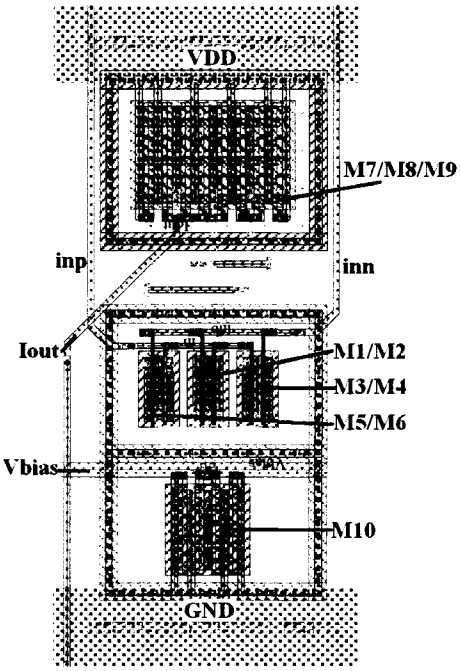

Figure 4.16: The layout of a rectifier. (Refer to the layout key in Figure B.1 of Appendix B to identify all layers used in the layout.)

The transistors that form the differential pairs (M_1 and M_2, M_3 and M_4, M_5 and M_6) and PMOS load (M_7 to M_9) are laid out with interdigitated fingers. This one-dimensional matching technique allows the transistors to be better matched against temperature and doping gradients. Since the RSSI requires several rectifiers, the layout is designed so it can be reused for each rectifier and they can be butted up next to each other to make efficient use of area. Their output current nets are connected together.

As with the limiter circuit, all simulations performed on the rectifier use the version of the schematic that is extracted from the layout with parasitic capacitances.

Rectifier Simulation Results

The theoretical functionality of the rectifier described in Section 4.1.2 can be compared to what is seen in post-layout simulations using the test bench shown in Figure 4.15. Figures 4.17, 4.18 and 4.19 show the rectifier input voltages and output currents when the peak-to-peak single-ended input voltages are 40 mV, 350 mV and 700 mV, respectively. In each of the three cases, the trends predicted in theory are observed. For the low amplitude (40 mV) input voltage in Figure 4.17, both the output current through M_8 and the current through M_7 remain close to half of the bias current of 50 μA since the differential inputs do not vary much about the switching point. Figure 4.18 shows that, for a medium sized (350 mV) input, the output current fully switches so that all of the current flows through M_7 for approximately half the duty cycle, during which time none of it leaves the output through M_8. The average output current is still above zero. In Figure 4.19, the input voltages are limited square waves that cause hard switching in

the rectifier. This results in an average output current that is very close to zero and the full current flows through M_7 for the majority of the time. Hence, the rectifier functions as expected for the entire range of possible input amplitudes.

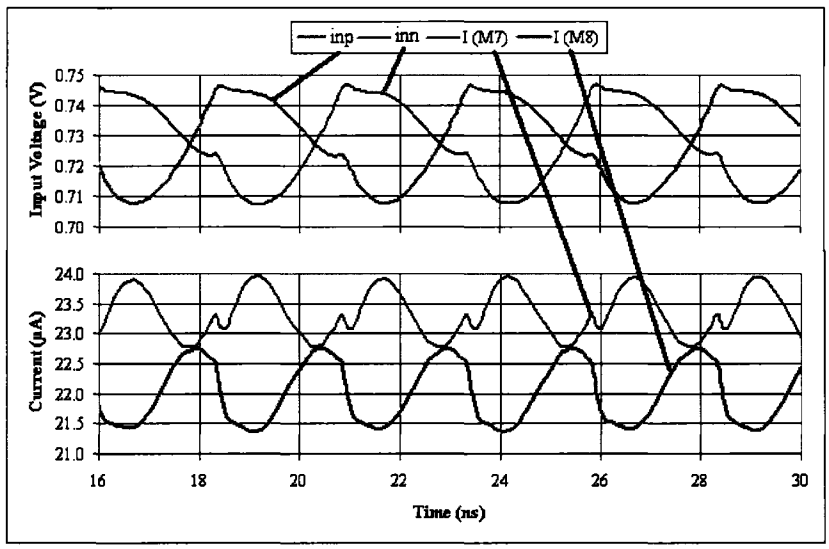

Figure 4.17: Transient response of the rectifier for a 40 mV (small) peak-to-peak single-ended input voltage.

Figure 4.20 shows simulation results for the output current from eight rectifier stages that have input signals from subsequent cascaded limiters. As such, the input amplitude to each subsequent rectifier is larger that the previous one. The figure also shows total current that is the summation of all of the rectifier output currents. This is for a 200 MHz input signal.

For small input signals, like the 40 mV one into rectifier stage 3, the current is close to half of the bias current or 25 μA and for large input signals, like the 700 mV one into rectifier stage 8, it approaches 0 μA. The current does not exactly reach the upper and lower limits, having a maximum of about 22 μA and a minimum of about 1.6 μA.

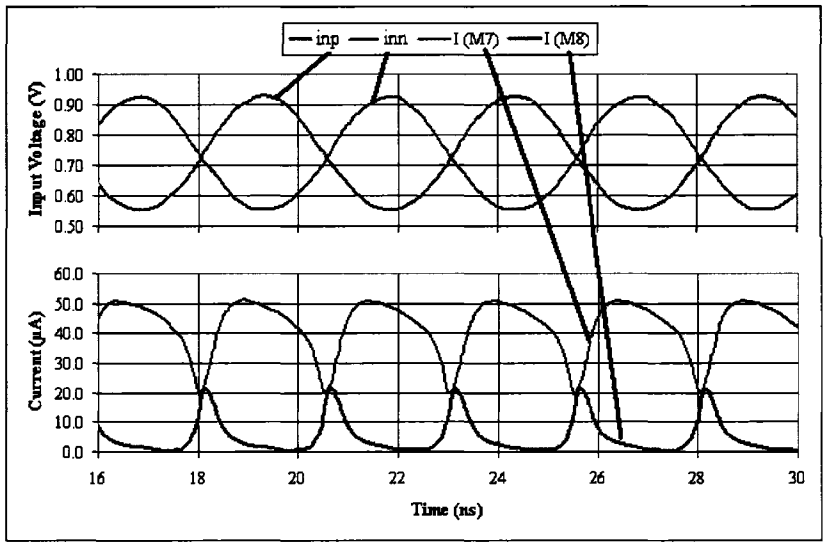

Figure 4.18: Transient response of the rectifier for a 350 mV (medium) peak-to-peak single-ended input voltage.

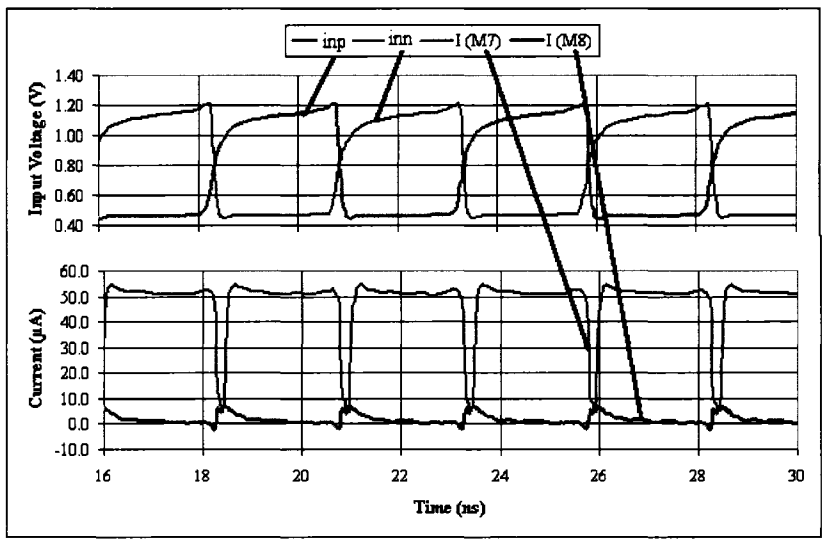

Figure 4.19: Transient response of the rectifier for a 700 mV (large) peak-to-peak single-ended input voltage.

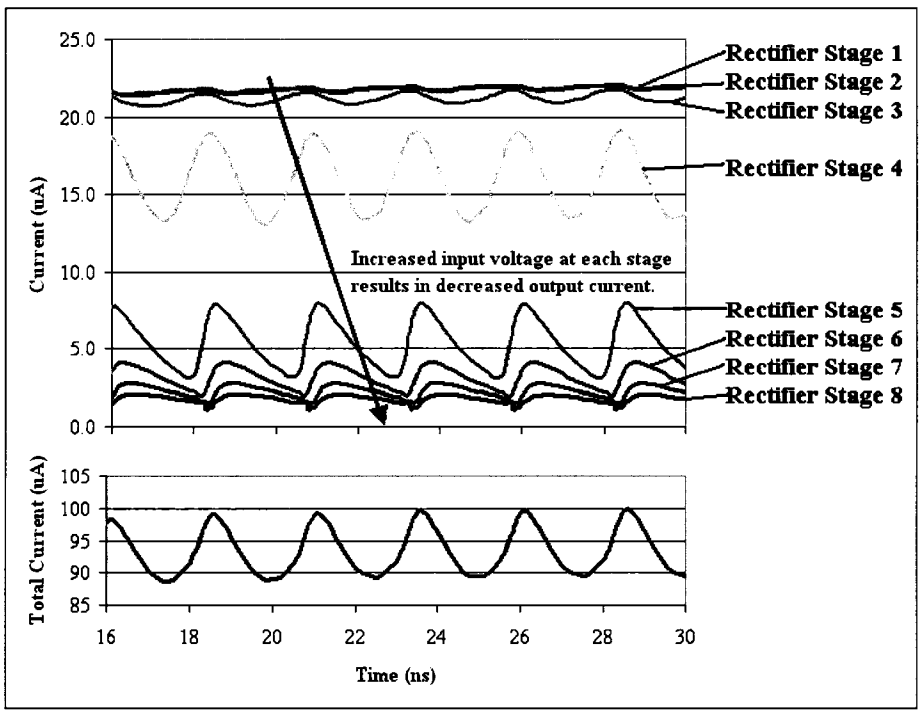

Figure 4.20: Output currents of each rectifier stage and the total output current. As the amplitude of the input signal increases at each subsequent stage, the rectifiers average output current decreases. For small amplitude input signals, the average current is close to $I_{bias}/2$ while for large amplitude signals, it is close to zero.

The fact that the bias and output current mirrors have less than a perfect 1:1 ratio is the cause of the maximum current not reaching exactly its full value. The current mirror formed from transistors M_8 and M_9 is susceptible to variations in the current being mirrored since M_8 always has a small V_{DS} of about 0.6 V, while the V_{DS} of M_9 varies with the output voltage for a range as large as 0.2 V to 1.7 V. Since the rectifier has four levels of stacked transistors, the headroom (V_{DS}) for the bias current tail is lower than the diode-connected half of the current mirror. This causes less than 100% of the current to be mirrored since that current mirroring is effected by inequalities in V_{DS}. The minimum current situation does not quite reach zero because this requires a perfect square wave with zero rise and fall times at the input to the rectifier to keep it fully switched to the off position. This signal comes from the limiting amplifier, which clips the signal but does not give a perfectly ideal square wave.

The total output current in Figure 4.20 is the summation of all of the rectifier currents combined. At 200 MHz, the average total current has a DC component of about 95 μA. It also has a high frequency ripple. When converted to a voltage by the resistor, this ripple is minimized with the addition of a parallel 10 pF capacitor that acts as a low pass filter.

Figure 4.21 shows the average current output from the rectifiers across a range of frequencies. The value of I_{max} is the current produced by the first rectifier when a minimum input voltage of 1 mV peak-to-peak is applied. It has a 5% variation versus frequency between 100 MHz and 700 MHz. I_{min} is the current produced by the final

rectifier stage when its input is fully clipped. As described above, this current should be zero but the limiting amplifier does not give the ideal square wave with zero rise and fall times that is required for this to happen. As the frequency is increased, the limiting amplifier gives an output that is fully switched for a lower percentage of its duty cycle, resulting in an increased current. At higher frequencies, this increase of current is seen at each rectifier stage, resulting in the increasing current trend of 18% from 100 MHz to 700 MHz, seen in $I_{total,max}$. $I_{total,max}$ is the maximum output current of all the rectifier stages combined. This occurs when the minimum input voltage of 1 mV peak-to-peak is applied to the first stage. When the maximum input voltage is applied, $I_{total,min}$ is lowest, ideally approaching zero.

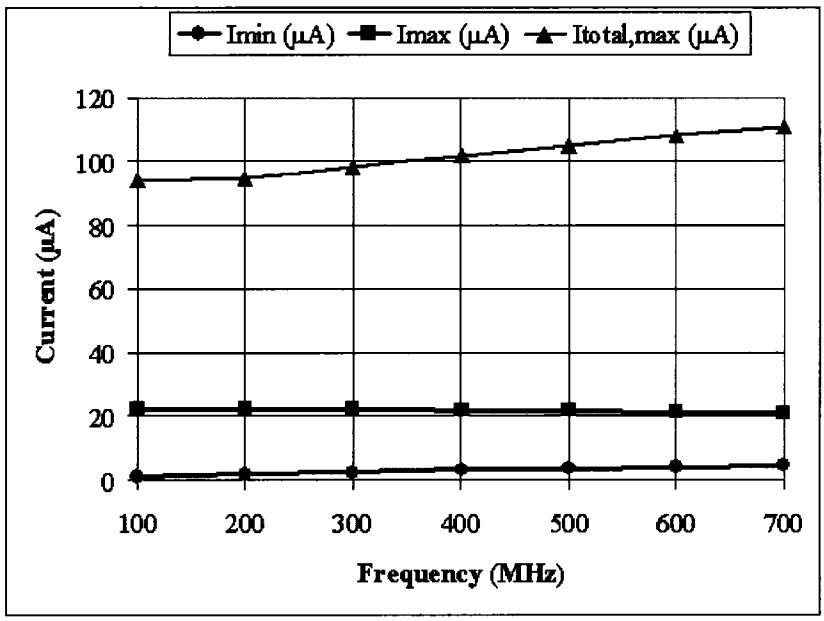

Figure 4.21: Minimum, maximum and total maximum output current of the rectifiers at various frequencies.

4.2.3 The RSSI

The receive signal strength indicator (RSSI) is assembled based on the performance of the limiting amplifiers and rectifiers, as well as the output amplitude range of the bandpass filter, as discussed in the theory in Section 4.1.3. First, the appropriate number of limiting amplifier stages is determined based on the minimum input voltage, $V_{in,min}$, from the specifications, along with the limited output voltage, $V_{out,clip}$, and gain, A, of the limiting amplifier found from simulations in Section 4.2.1.

From the design of the bandpass filter in Section 3.3, it is found that the filter output amplitude can vary from approximately 1 mV to 100 mV peak-to-peak. In a 50 Ω system, which represents the environment under which the circuit is tested, this works out to be equal to power levels from -56 dBm to -16 dBm using

$$\begin{aligned} P_{dBm} &= 10\log_{10}\left(\frac{P_{Watts}}{1\text{mW}}\right) \\ P_{Watts} &= \frac{V_{RMS}^2}{R} \\ V_{RMS} &= \frac{V_{p2p}}{2\sqrt{2}} \end{aligned} \tag{4.2.3}$$

To give some design margin, the RSSI is designed to work from -60 dBm to -10 dBm, as outlined in the specifications in Chapter 2. This sets the minimum input voltage to $V_{in,min} = 632\ \mu V_{p2p}$.

Figure 4.14 shows that the maximum, clipped output voltage, $V_{out,clip}$, from a limiting amplifier is about 1.3 V peak-to-peak. The overall required gain of the RSSI, A_{RSSI}, can be calculated as

$$A_{RSSI} = \frac{V_{out,clip}}{V_{in,min}} = \frac{1.3V_{p2p}}{632\mu V_{p2p}} = 2057V/V. \tag{4.2.4}$$

This gain is calculated when the smallest input signal to the first limiter stage (632

μV_{p2p}) causes the final limiter stage to start clipping and produce its maximum output (1.3 V_{p2p}). 2057 V/V of voltage gain is equivalent to 66.3 dB.

From Section 4.2.1, the simulated gain of a limiting amplifier, A, at low frequencies is shown to be 10.73 dB. At 700 MHz, the high end frequency for the whitespace detector application, it is 9.2 dB. Using this worst case value and the total desired gain of the RSSI, the number of limiter stages required for the RSSI is calculated by rearranging Equation 4.1.9 to give

$$N = \frac{10log(A_{RSSI})}{10log(A)} = \frac{A(dB)_{RSSI}}{A(dB)_{limiter}} = \frac{66.3dB}{9.2dB} = 7.2. \tag{4.2.5}$$

The number of limiter stages chosen to implement the RSSI is rounded up from 7.2 to 8.

The size of the output resistor, R_{out}, is determined based on Equation 4.1.11. Ideally, $V_{out,max}$ is 1.8 V but in reality, it does not get higher than about 1.6 V due to the voltage required to keep M_9 of the rectifier in saturation. $I_{out,max}$ is taken from Figure 4.21 at 700 MHz to be 111 μA. The selected resistor size for the RSSI is 14.4 kΩ as calculated by

$$R_{out} = \frac{1.6V}{111\mu A} = 14.4k\Omega. \tag{4.2.6}$$

A 10 pF capacitor is placed in parallel with the output resistor to act as a low pass filter, reducing high frequency ripple on the output voltage line. This ripple is caused by the operation of the rectifier circuit and the capacitor filters it so that the output voltage becomes the average value of what is output from the rectifiers. The value of the capacitance is chosen as a compromise between ripple on the output signal and the

response time of the RSSI.

The RSSI Layout

The layout of the receive signal strength indicator is shown in Figure 4.22. All of the input and output ports are labelled, as well as the main sub-circuits. It is built by hierarchically placing the eight limiting amplifier and rectifier circuits. One current mirror provides the biasing to all of the limiters and another provides biasing to all of the rectifiers. There are also capacitors on the bias lines to provide filtering and there is a resistor divider at the input to create the proper common mode bias. These two design considerations are discussed in more detail in Chapter 5. The output resistor and capacitor are placed off-chip on a printed circuit board that is discussed further in Chapter 6. This is to save space on the integrated circuit since these components are large. It also gives the flexibility to change the size of these components when the circuit is tested. All the simulations performed on the RSSI use the version of the schematic that is extracted from this layout with parasitic capacitances.

RSSI Simulation Results

Transient simulations are performed on the RSSI that is extracted with parasitic capacitances using the test bench in Figure 4.23. In this test bench, a voltage supply of V_{DD} = 1.8 V is provided along with bias currents of 50 μA that are mirrored to the limiters and rectifiers. The input signal is provided using a 50 Ω port to imitate the sources that are used to test the fabricated circuit. This source is AC coupled to the circuit and on-chip resistor dividers set the bias voltage at the inputs. The simulations are

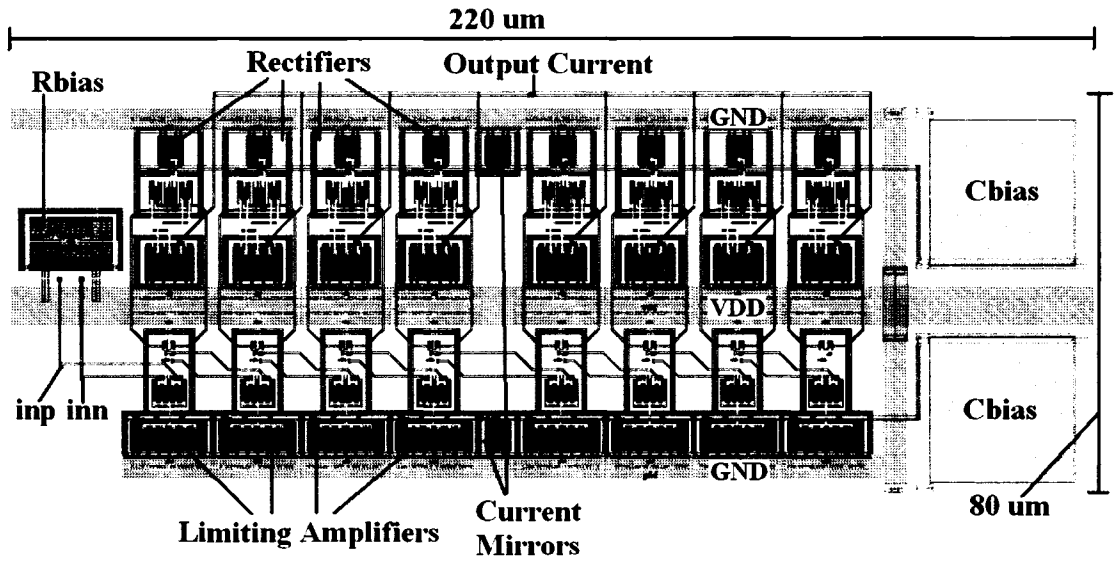

Figure 4.22: RSSI layout. (Refer to the layout key in Figure B.1 of Appendix B to identify all layers used in the layout.)

performed single-ended even though the circuit has differential inputs. The integrated circuit only has a single ended input since there is not enough space for the extra pads required for the differential input. As a result, the single-ended signal is applied to one of the differential inputs while the other input is internally biased at its common-mode value. The output current from the RSSI is sent through the 14.4 kΩ output resistor and low pass filter to generate the output voltage.

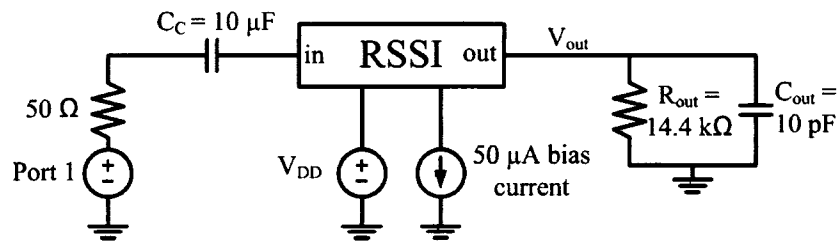

Figure 4.23: The test bench used to run transient simulations on the RSSI.

Using this test bench for transient simulations, a number of results can be examined.

The main result of interest from the RSSI is its input to output response. The output voltage, V_{out}, is expected to descend linearly with an exponentially increasing input amplitude. Results for the receive signal strength indicator input amplitude to output voltage response for various input frequencies are shown in Figure 4.24. These results are obtained by doing a parametric analysis in which the output voltage is measured for various input amplitudes and frequencies. The results show the logarithmic output response of the RSSI. The input amplitude level increases exponentially while the output voltage decreases linearly. The response is linear for input amplitudes between -60 dBm and -10 dBm, which is the desired range based on the output signal levels from the bandpass filter.

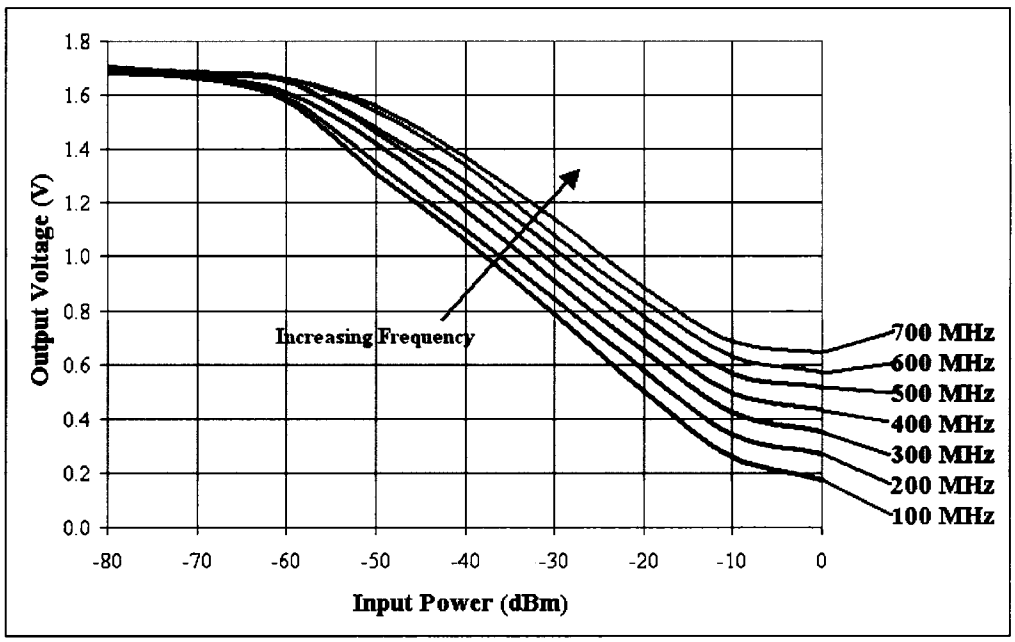

Figure 4.24: The RSSI input versus output characteristic at various frequencies.

It can be seen in Figure 4.24 that at the lower frequencies, the output uses almost

the entire range of output voltages while at higher frequencies it does not use the full available voltage range. At 700 MHz, the minimum voltage value reaches about 0.65 V, while at 100 MHz, it reaches 0.2 V. This performance degradation at high frequencies can be explained by a variety of reasons. These include the fact that the limiting amplifier gain is lower by about 1.5 dB at 700 MHz when compared to 100 MHz. This means that for the same input amplitude at each of these frequencies, the output amplitude of the limiting amplifiers will be lower at higher frequencies. This causes the rectifiers to output more current since they are being switched less strongly and the output voltage ends up being higher. It is also shown in Figure 4.21 that the rectifiers do not switch off their minimum current as fully at the higher frequencies, even when the input to the rectifier is fully switched and clipping.

The specified range of inputs to the RSSI is -60 dBm to -10 dBm. The RSSI should ideally have a logarithmic input to output response over this range. Since the x-axis of the graph in Figure 4.24 is in dBm and the y-axis is linear, the logarithmic input to output response is seen as a linear function. The curves in this graph appear to be linear over the desired -60 dBm to -10 dBm range. Any error in the linearity of these curves can be quantified as the RSSI error. This is the amount of dB the RSSI curve deviates from being linear versus the input power. A graph of the RSSI error at 100 MHz, 400 MHz and 700 MHz operation is shown in Figure 4.25. As seen in this plot, the RSSI error increases with frequency. At 100 MHz, it is at worst $\pm$ 0.4 dB. At 400 MHz, it is at worst $\pm$ 1.2 dB. At 700 MHz, it is at worst $\pm$ 2.9 dB.

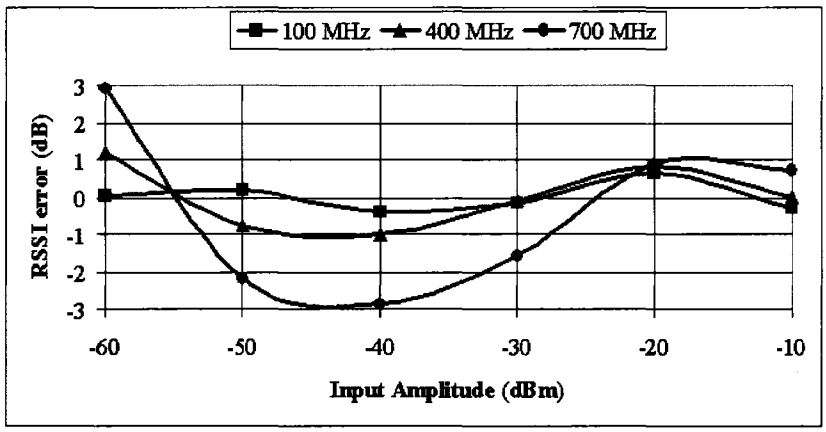

Figure 4.25: The RSSI output error with respect to the ideal logarithmic input to output relationship.

Another result that can be measured from simulations is the response or settling time required for the RSSI to settle to its final voltage value when the amplitude of the input is suddenly changed. The response time is a function of the resistor and capacitor that form the output low pass filter, along with any other parasitic resistance or capacitance on the output node coming from the pads on the chip and the printed circuit board. An equation that estimates the settling time can be derived from

$$V_c = V_0 e^{\frac{-t}{\tau}} \tag{4.2.7}$$

that describes the voltage on a discharging capacitor. V_0 is the initial voltage, V_c is the voltage at time, t, and τ = RC is the time constant.

The settling time can be defined as the time required for the output voltage to settle to within 1% of its final value. This means that $V_c/V_0 = 0.01$ and Equation 4.2.7 can be written as

$$0.01 = e^{\frac{-t_{settle}}{\tau}}. \tag{4.2.8}$$

Substituting τ = RC, this can be rearranged to

$$t_{settle} = -(RC)\ln(0.01) \tag{4.2.9}$$

where R and C are, respectively, the total resistance and capacitance on the output node.

The settling time of the RSSI can be estimated using the output resistance of R = 14.4 kΩ and the output capacitance 10 pF plus 0.85 pF to represent the capacitance of the pads on the chip and the printed circuit board. Using these values in Equation 4.2.9 gives an estimated RSSI settling time of t_{settle} = 718 ns.

A sample simulation result for the RSSI output voltage is shown in Figure 4.26. Initially, a 200 MHz input signal is given to the RSSI with an amplitude of 10 mV peak-to-peak. After 800 ns, the amplitude is increased to 100 mV peak-to-peak, resulting in a lower output voltage, as expected. This plot shows that it takes the RSSI approximately 700 ns to settle to its new output value when it experiences an input change. This is within 3% of the settling time predicted with Equation 4.2.9.

4.3 Performance Summary and Comparison to the Literature

In Section 2.4 a performance summary of receive signal strength indicators (RSSI) in literature is given. The performance of the RSSI in this thesis is summarized and compared to the literature in Table 4.3. The reference for this thesis is denoted by a *. This table is the same as the one in Section 2.4 with the addition of the results from this thesis.

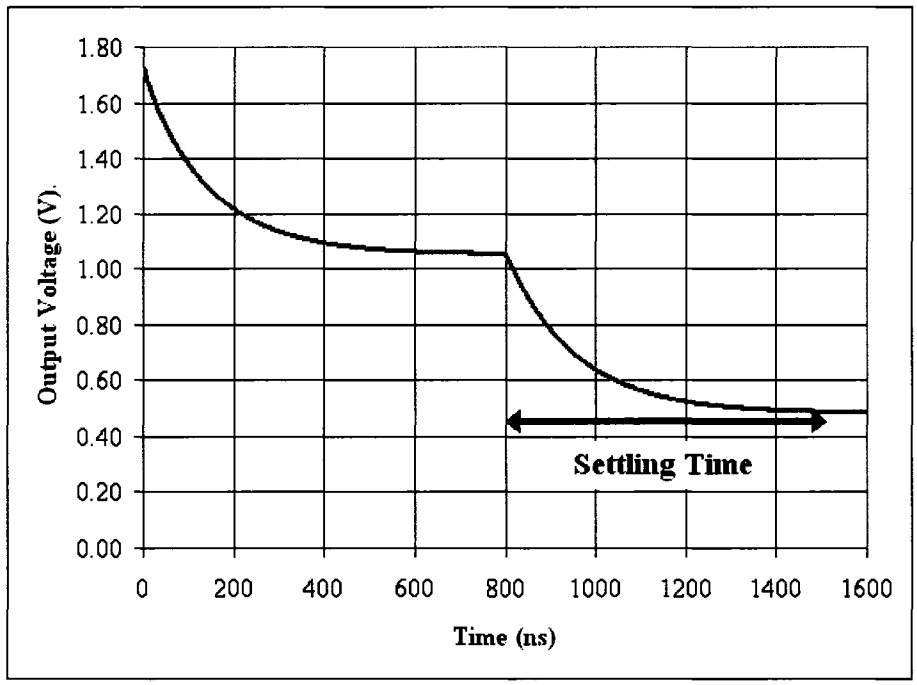

Figure 4.26: The output voltage response of the RSSI.

Table 4.3: Received Signal Strength Indicator Performance Summary and Comparison

Ref.	Tech.	Power	Area	Gain/Stage # of Stages Total Gain	Input Dynamic Range	3 dB Band-width	Error
[12]	0.35 μm CMOS	3.2mW	0.48 mm^2	9.3 dB $\times$ 7 = 65 dB	-60dBm to 5dBm	23MHz	$\pm$3dB
[12]	0.5 μm CMOS	4.3mW	0.49 mm^2	9.3 dB $\times$ 7 = 65 dB	-60dBm to 5dBm	18MHz	$\pm$3dB
[33]	0.6 μm CMOS	6.2mW	0.4 mm^2	12 dB $\times$ 7 = 84 dB	-78dBm to -3dBm	70MHz	$\pm$1dB
[34]	0.35 μm CMOS	69mW	N/A	12 dB $\times$ 7 = 84 dB	-83dBm to -3dBm	110MHz	$\pm$0.7dB
[35]	0.6 μm CMOS	15mW	0.36 mm^2	80 dB	68dB	292MHz	$\pm$1dB
*	0.18 μm CMOS	1.6mW	0.02 mm^2	9.2 dB $\times$ 8 = 73.6 dB	-60dBm to -10dBm	1.17GHz	$\pm$2.9dB

As shown in Table 4.3, the RSSI in this thesis is designed using a CMOS technology with smaller gate lengths than the others in the comparison. This allows the design to be created in a much smaller area. The area for this design accounts for the eight limiting amplifiers and eight rectifiers that make up the RSSI. These components combine to consume 1.6 mW of power from a 1.8 V supply, which is less than the other designs being compared. The gain of each limiting stage of 9.2 dB at the higher frequencies and the total gain of 73.6 dB is comparable to other designs, falling in the middle of the results from the literature. The input dynamic range of this RSSI is smaller than the other designs because it is designed to cover the bandpass filter output range. The limiting amplifiers that form this RSSI have a higher 3 dB bandwidth than those in the other designs, allowing them to operate at the higher frequencies required for the intended application. The RSSI error of ± 2.9 dB is comparable to the other designs, though it is at the high end. This is when operating at the maximum frequency of 700 MHz. When operating down to 100 MHz, the RSSI error is better than the other designs at ± 0.4 dB.

Table 4.4 shows the specifications and the performance achieved in simulation of the receive signal strength indicator. All of the specifications are achieved. The performance at the high end of the frequency range can be improved further. This is an area for future work and improvement with regards to the design of the RSSI.

Table 4.4: Specifications and Performance of the Receive Signal Strength Indicator

Specification	Targeted Performance	Performance Achieved
Frequency Range	70 MHz to 700 MHz	Achieved but lower at higher frequencies
Input Dynamic Range	-60 dBm to -10 dBm	Achieved
Power Consumption	Low	1.6 mW
Circuit Area	Small	80 μm $\times$ 180 μm

4.4 Chapter Summary

The design of the receive signal strength indicator (RSSI) for the whitespace detector is presented in this chapter. Its role is to provide an output voltage that has a linear relationship to the logarithm of its input amplitude. This output is an indication of the measured signal strength. It is built from limiting amplifiers, rectifiers, a summing resistor and a bandpass filter. Theoretical equations for the gain and bandwidth of the limiting amplifiers are developed along with a theoretical explanation of the functionality of the rectifiers. A design procedure for choosing the number of stages for the RSSI and the components for the output low pass filter is given.

The circuit implementation and layouts of the sub-blocks are shown. An RSSI is assembled based on the presented design procedure and the simulation results of the limiting amplifiers and rectifiers. The input to output response of the RSSI is simulated over a range of input amplitudes and frequencies. From this response, the accuracy and settling time of the RSSI are determined. The performance of the RSSI is compared to other RSSI in literature and found to use lower power, require a smaller area and operate up to higher frequencies than the other presented designs. Though its dynamic

range is smaller than other RSSIs, its performance is suitable for the application in the whitespace detector and it meets the required specifications.

Chapter 5

Whitespace Detector System

The whitespace detector system is implemented as an integrated circuit using a 0.18 μm CMOS technology. The two main components of the whitespace detector are the high quality factor bandpass filter based on the tunable active inductor and the receive signal strength indicator (RSSI) circuit. The design of these circuits is detailed in Chapter 3 and Chapter 4, respectively. Figure 5.1 is a block diagram representation of the whitespace detector, showing the bandpass filter and RSSI, along with input and output (I/O) buffers and biasing circuitry. The input and output buffers interface the on-chip circuits with the off-chip, 50 Ω equipment that is used to test them. The biasing circuitry directs off-chip bias currents to the appropriate on-chip circuits. The blocks within the dashed box in Figure 5.1 are the on-chip components of the whitespace detector. The RF input signal is provided to the bandpass filter through an input buffer and the RF output of the filter can be monitored through an output buffer. The RSSI output current, I_out_RSSI, feeds into an off-chip summing resistor and lowpass filter, which converts the current to a voltage.

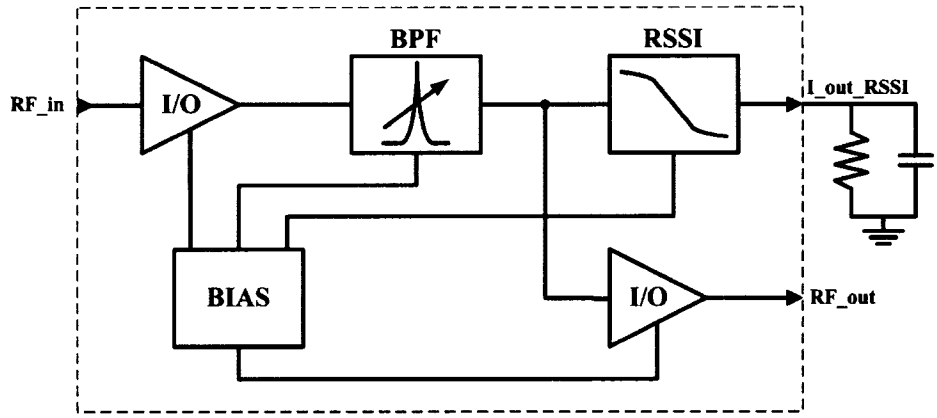

Figure 5.1: Block diagram of the whitespace detector implemented on the integrated circuit. The dashed line indicates the chip boundary.

5.1 The Input and Output Buffers

A buffer is required to interface between the input and output of the bandpass filter and the off-chip, 50 Ω environment. The source follower at the output of the bandpass filter does not have the drive strength to overcome the output capacitance caused by the on-chip output pad and the printed circuit board that is used for testing. The input of the bandpass filter requires a buffer for interfacing because its input impedance is very low when tuned to a particular frequency. Without a buffer, the 50 Ω source driving the filter would not properly transfer the signal to the filter. The filter input impedance varies from tens of Ohms to thousands of Ohms across the 70 MHz to 700 MHz band and changes whenever the bandpass filter tuning is changed. The input impedance of the filter is shown in Figure 5.2 for the situation when the filter is tuned to 200 MHz. The input impedance at 200 MHz is approximately 20 Ω. Due to the wide variation in input impedance across the 70 MHz to 700 MHz band, a specific input matching

network is not suitable. Instead, an input buffer that has high input impedance and very low output impedance is desired. At the input, this allows a parallel 50 Ω resistor to give a broadband 50 Ω match to interface the circuit input with off-chip circuits. The noise impact of the 50 Ω resistor is not a concern since the high quality factor of the bandpass filter allows it to be filtered away. The low output impedance of the buffer allows for the maximum signal transfer to the bandpass filter. One such circuit that has these input and output characteristics is a voltage follower [41]. The voltage follower circuit, as described in [41], is implemented as the input buffer to the bandpass filter. Due to its low output impedance, the same buffer is also used as the output buffer for the bandpass filter output, which interfaces it to the 50 Ω load.

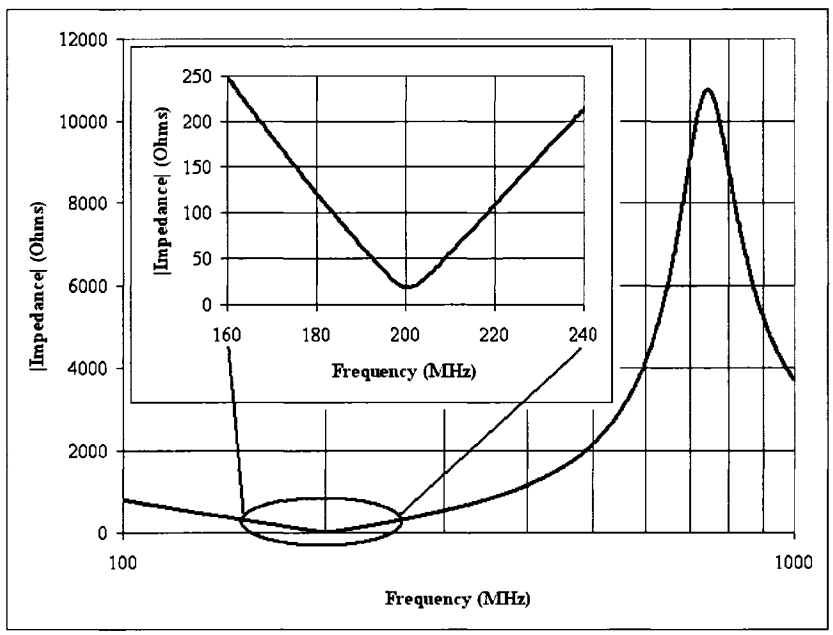

Figure 5.2: Input impedance of the bandpass filter when tuned to 200 MHz.

A schematic of the voltage follower circuit can be seen in Figure 5.3. It consists of

two cascaded source followers; an NMOS one (M1) and then a PMOS one (M2). The source followers are biased in such a way that the NMOS bias current is related by a scaling factor, α, to the PMOS current. The choice of this ratio is what gives the voltage follower its very low output impedance [41]. The effective g_m of the combination of transistors M1 and M2 can be expressed by

$$g_m = \frac{g_{m1}g_{m2}}{g_{m1} - \alpha g_{m2}}, \tag{5.1.1}$$

the simplified equation described in [41]. Based on this equation, g_m can be made very large by setting $\alpha = g_{m1}/g_{m2}$. Since the output impedance of the source follower is inversely proportional to its transconductance, the result is a very small output impedance. M3 and M4 form a current mirror that provides the biasing for M1 while M5 and M6 form the current mirror that provides the biasing for M2. The design parameters for the buffer are summarized in Table 5.1.

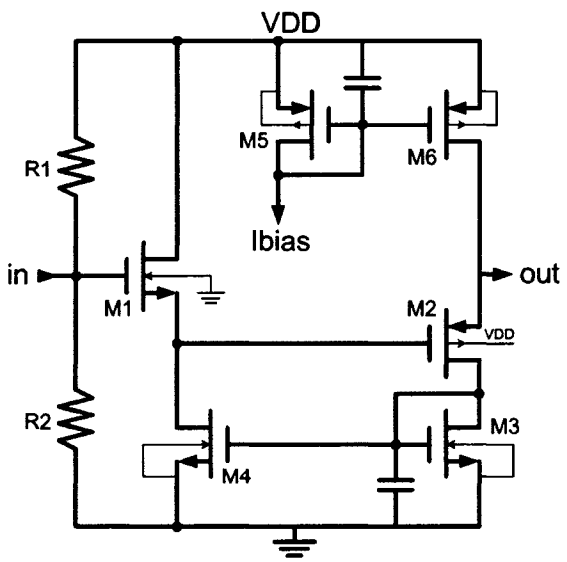

Figure 5.3: The voltage follower circuit that is used as the input and the output buffer.

Table 5.1: Design Parameters of the Input and the Output Buffer Shown in Figure 5.3

Transistor Dimensions	(# of Fingers × Width/Finger) / Gate Length
$(W/L)_1$	20×5 μm / 0.18 μm
$(W/L)_2$	72×7 μm / 0.18 μm
$(W/L)_3$	28×7 μm / 0.5 μm
$(W/L)_4$	34×7 μm / 0.5 μm
$(W/L)_5$	8×7 μm / 0.5 μm
$(W/L)_6$	40×7 μm / 0.5 μm
Other Components	**Value**
R_1	1.94 kΩ
R_2	9.69 kΩ
I_{bias}	700 μA

5.1.1 The Input and the Output Buffer Layout

The layout of the circuit that is used as both the input and output buffer is shown in Figure 5.4. All of the input and output ports are labelled, as well as each of the components.

The two source follower transistors, M_1 and M_2, have widths of 100 μm and 504 μm, respectively. These large widths and bias currents of of 3.5 mA are required to achieve the desired impedance characteristics for the buffer. The transistors are segmented into fingers to make the layout more compact. The transistors that form the current mirror pairs (M_3 and M_4, M_5 and M_6) are laid out with interdigitated fingers to be better matched against temperature and doping gradients. Wide metal widths are required to accommodate the high current. Current carrying metal is sized to have a current density of 1 mA/μm. Since the transistors are segmented into many fingers, no one finger has to carry more than 175 μA of current. The input resistor divider that sets the input bias level to 1.5 V, is formed from resistors R_1 and R_2. They are made from unit sized

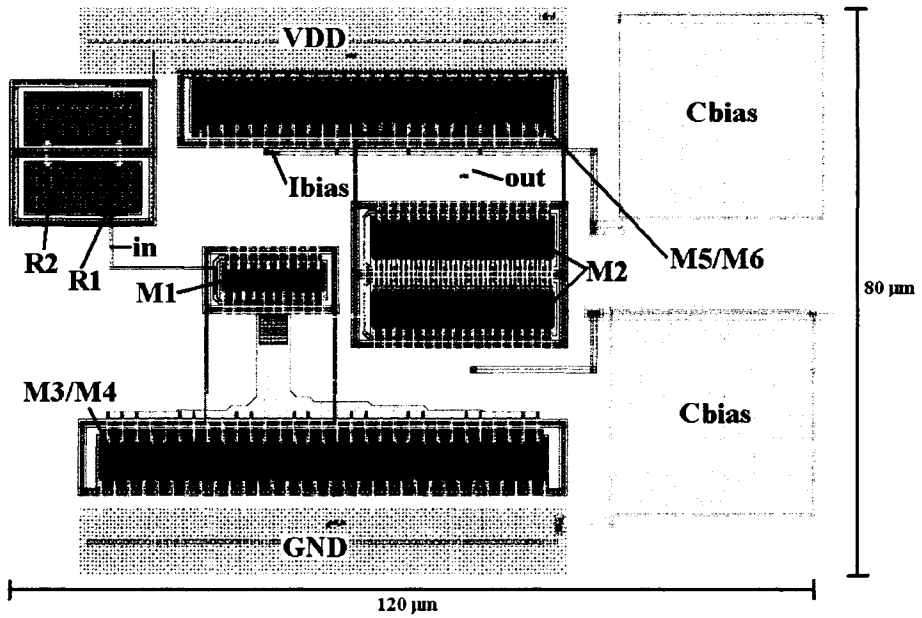

Figure 5.4: The layout of the input and output buffer with ports and components labelled. (Refer to the layout key in Figure B.1 of Appendix B to identify all layers used in the layout.)

resistors of 0.97 kΩ such that R_1 requires two units to make 1.94 kΩ and R_2 requires ten units to make 9.7 kΩ. These resistor segments are laid out with dummy resistors on either side. These techniques help to match the resistors. It can also be noted that there are 950 fF filtering capacitors on the bias lines.

From the layout of the input and output buffer, an extracted version of the schematic is generated. This extracted representation of the circuit includes parasitic capacitances and it is used when simulating the buffer performance.

5.1.2 Input and Output Buffer Simulations

The test bench used to simulate the input and output buffer is shown in Figure 5.5. It has 50 Ω ports at the input and output that are AC coupled with 10 μF capacitors. It

runs from a supply of V_{DD} = 1.8 V and uses a 700 μA bias current. This test bench is used to perform S-parameter, transient and periodic steady state (PSS) simulations.

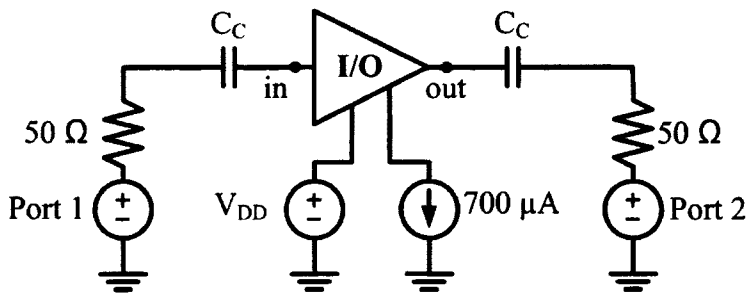

Figure 5.5: The test bench used to simulate the input/output buffer.

Figure 5.6 shows the input and output impedance of the buffer from S-parameter simulations. The buffer has a large input impedance (greater than 1.6 kΩ from 100 MHz to 1 GHz) and a very low output impedance. At the high end of desired frequencies of 700 MHz, the output impedance is less than 13 Ω and at low frequencies it is below 5 Ω. Based on these results, the buffer meets the required criteria of having a high input impedance and a very low output impedance.

Transient simulations show that the voltage gain of the buffer varies from -4 dB to -6 dB across the 70 MHz to 700 MHz band. This loss is acceptable for the system design. A plot showing the linearity of the buffer from a two-tone periodic steady state (PSS) simulation is shown in Figure 5.7. Two input tones at 200 MHz and 205 MHz result in a 1 dB compression point (P1dB) of -10.5 dBm and a input referred third order intercept (IIP3) of 6.6 dBm. The buffer's 1-dB compression point is 40 dB above that of the bandpass filter. As a result the buffer's linearity is not a big concern and the bandpass filter limits the linearity of the system.

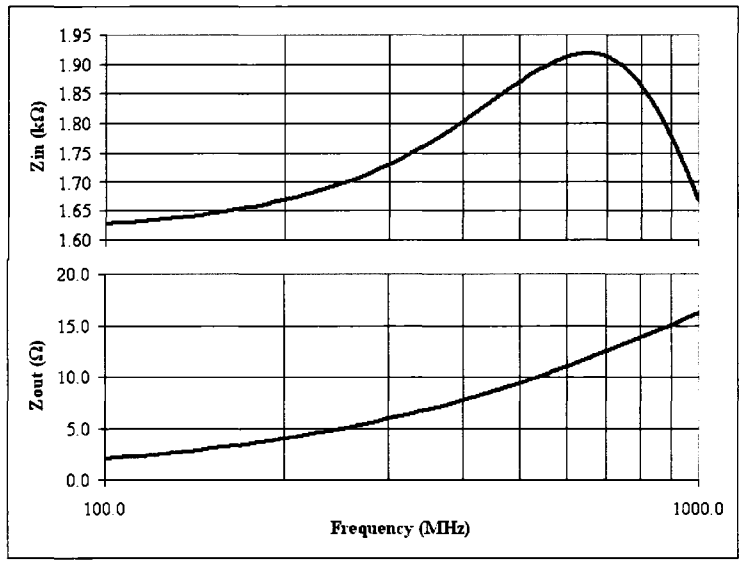

Figure 5.6: Input and output impedance of the voltage follower buffer.

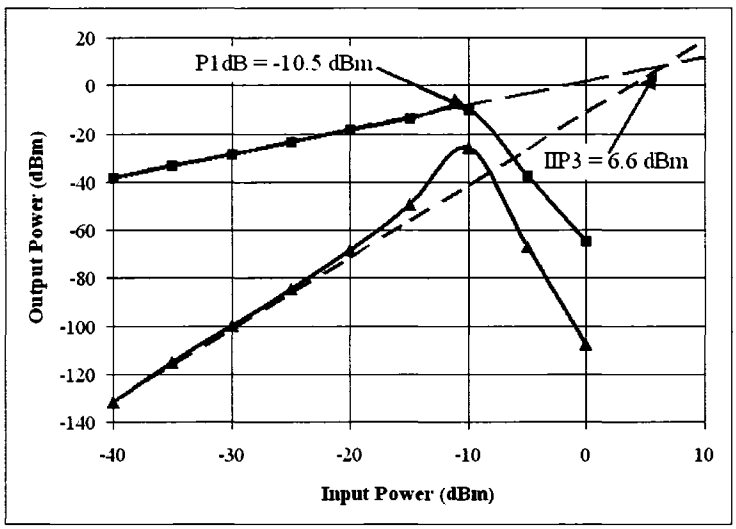

Figure 5.7: Linearity of the voltage follower buffer showing the 1 dB compression point (P1dB) and the input referred third order intercept point (IIP3).

5.2 Biasing Circuitry

The BIAS block in Figure 5.1 consists of several current mirrors such as the one shown in Figure 5.8. These current mirrors receive bias currents from off-chip, which are mirrored and routed to all of the other circuits on the chip. This provides all of the current biasing to the chip. Depending on the direction of current flow, NMOS or PMOS transistors are used. In general, the current mirror transistors have widths that are proportional to the amount of current they are providing. Their lengths are set at 1 μm, which was found through simulations to give current mirrors having equal currents flowing in both halves of the current mirror even if their V_{DS}'s are not equal. As explained in the discussion of the current mirrors in the individual circuit blocks, this is due to the fact that the larger than minimum length gives a larger output resistance which results in a more constant current with respect to V_{DS} [38, p.405]. The capacitor connected between the gates of the transistors and ground is a 950 fF MIM (metal-insulator-metal) capacitor that filters out noise on the bias lines.

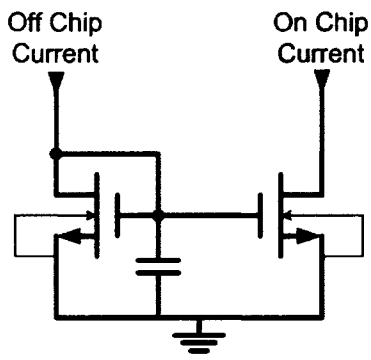

Figure 5.8: Example of current mirror for providing bias currents.

Resistor dividers, such as the one made from R_1 and R_2 in Figure 5.3, are used to

provide voltage biasing to the RSSI and buffer circuits. The on-chip polysilicon resistors are matched in the circuit layout and act as a voltage divider. The resistor sizes are chosen to provide the desired DC bias voltage at the input node to the circuit. In the case of the input buffer, shown in Figure 5.3, the resistor divider is made up of a 1.94 kΩ resistor on top and a 9.69 kΩ resistor on the bottom. This sets the bias point at 1.5 V from a 1.8 V supply and keeps transistors M1 and M4 of the input buffer in Figure 5.3 in saturation. The resistors draw 154 μA of current from the 1.8 V supply. The resistor sizes are chosen as a compromise between area used and power consumed. When seen in parallel with the 50 Ω resistor used for matching, these cause the effective resistance to be approximately 49 Ω.

Similarly, a resistor divider is used at the input to the RSSI. Its top resistor is 1.39 kΩ and its bottom resistor is 926 Ω. The resistor divider sets the bias point at the input of first limiting amplifier in the RSSI to 0.72 V when the supply voltage is 1.8 V. These resistors draw 777 μA of current from the 1.8 V supply and give an effective resistance of approximately 46 Ω when seen in parallel with the off-chip 50 Ω matching resistor at the input to the RSSI. Larger resistors could be used, at the expense of area, to reduce the current the resistor divider consumes and improve the 50 Ω input impedance. The input to the RSSI allows it to be tested individually, without the bandpass filter.

In cases where the DC bias point at the output of one circuit is not at the required value of the DC bias point for the input of the next circuit, DC coupling capacitors are required. This is seen when interfacing between the bandpass filter and RSSI in Figure

5.1 as well as interfacing between the input and output of the chip and the off-chip test environment. 11.3 pF on-chip MIM capacitors are used for this role. The capacitors are small enough so that they fit on the integrated circuit and large enough that their impedance is sufficiently small at low frequencies. At 100 MHz, the impedance is 140 Ω and since it appears in series with the large input impedance of the gate of a transistor, it does not have a big impact on the overall impedance.

For the situation where the bandpass filter is interfaced to the RSSI, level shifting circuitry was examined as an alternative to using coupling capacitors and resistor dividers but was not used in the final design. This is because the output bias point of the bandpass filter varies depending on where it is tuned and the level shifting circuitry would transfer this bias change to the RSSI. Thus, the RSSI would be biased differently for different bandpass filter tuning. The use of coupling capacitors was seen as the simpler solution in the implementation of the design.

5.3 Whitespace Detector System Layout

The layout of the complete whitespace detector integrated circuit (IC) is shown in Figure 5.9. It is implemented in a 0.18 μm CMOS technology and designed using Cadence CAD tools. From this layout, an IC is fabricated for testing.

The whitespace detector system layout is hierarchically built from the circuit layouts of the blocks shown in Figure 5.1 that have been discussed in earlier chapters. These circuits, including bandpass filter, RSSI, input and output buffers and the bias control block, are labelled in Figure 5.9. Also labelled are the coupling capacitors, C_C that

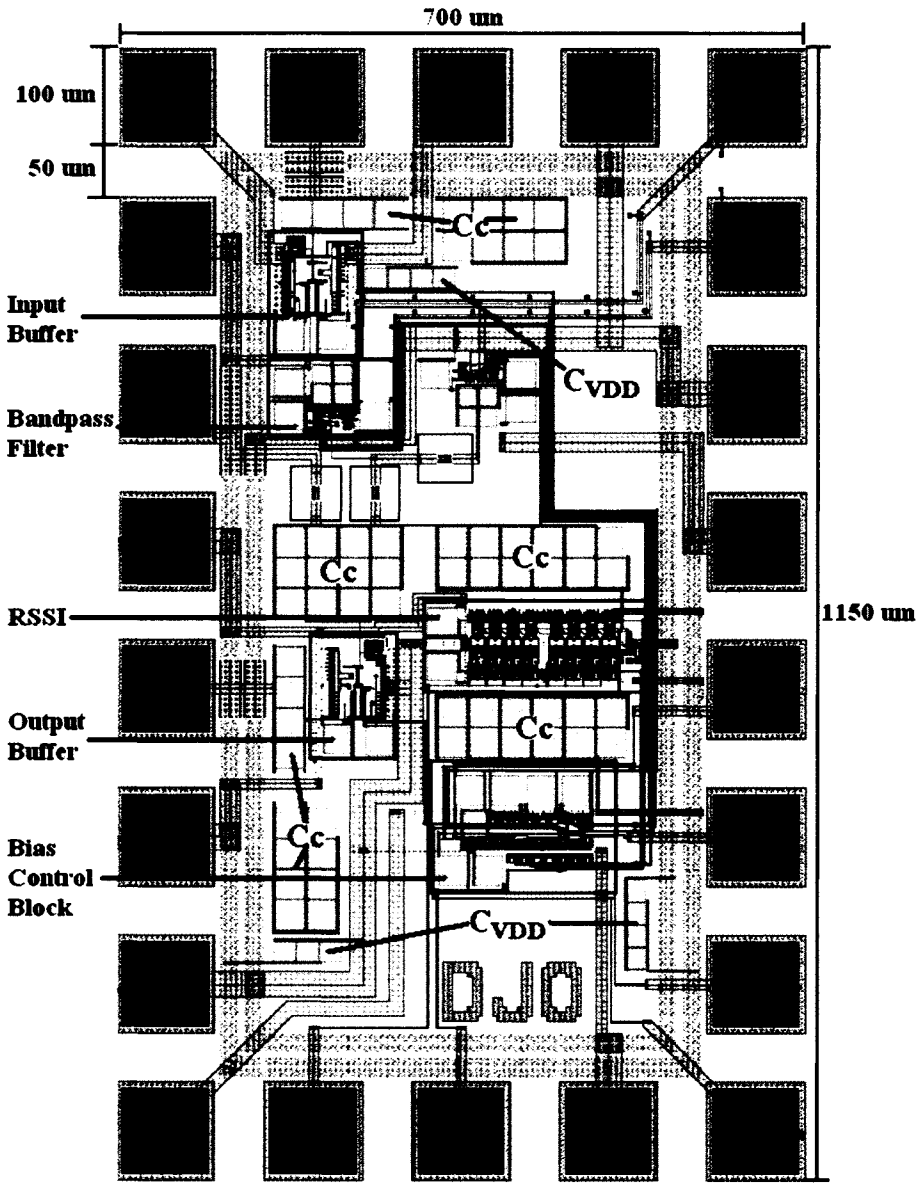

Figure 5.9: The layout of the whitespace detector integrated circuit. (Refer to the layout key in Figure B.1 of Appendix B to identify all layers used in the layout.)

are used to interface between circuits while allowing the proper bias voltages. The capacitors labelled C_{VDD} are connected between the supply and ground and are used to filter noise on the supply. The large rings that go inside the pads are for the 1.8 V supply and ground. These rings and wide metal power routing give a low resistance path for the supply and ground to the circuits on the IC. There are six ground and six supply pads so that multiple bondwires can be used in parallel to reduce the overall bondwire inductance, as is discussed further in Section 5.4. The input and output pins are summarized in Table 5.2 with their nominal DC operating voltages and currents. For inputs and outputs that have variable voltages and currents depending on the circuits operation, the ranges are shown in Table 5.2.

Table 5.2: Summary of the Input and Output Pins of the Whitespace Detector Integrated Circuit

Pin Name	Type	Nominal Voltage	Nominal Current
VDD × 6	Voltage Supply	1.8 V	20.9 mA to 21.6 mA
GND × 6	Ground	0 V	21.5 mA to 21.9 mA
RF_in	RF Input	0 V (AC coupled)	0 A
RSSI_in	RF Input	0 V (AC coupled)	0 A
RF_out	RF Output	0 V (AC coupled)	0 A
Iout_RSSI	Output Current	0.2 V to 1.7 V	14 μA to 118 μA
V_1	Input Bias Voltage	0 V to 0.5 V	0 A
V_2	Input Bias Voltage	0.9 V to 1.2 V	0 A
I_1	Input Bias Current	1.07 V to 1.37 V	5 μA to 200 μA
I_2	Input Bias Current	1.14 V to 1.34 V	2 μA to 30 μA
Ibias_50u	Input Bias Current	1.07 V	50 μA
Ibias_700u	Input Bias Current	0.67 V	700 μA

5.4 System Testbench

From the layout of the whitespace detector integrated circuit (IC) seen in Figure 5.9 a schematic is extracted including parasitic capacitances. This extracted version of the entire chip is used for system testing of the whitespace detector. A schematic of the test bench used for testing the whitespace detector IC in Cadence, using SpectreRF, is shown in Figure 5.10. This test bench is set up to model the test conditions that are encountered during the testing of the fabricated chip.

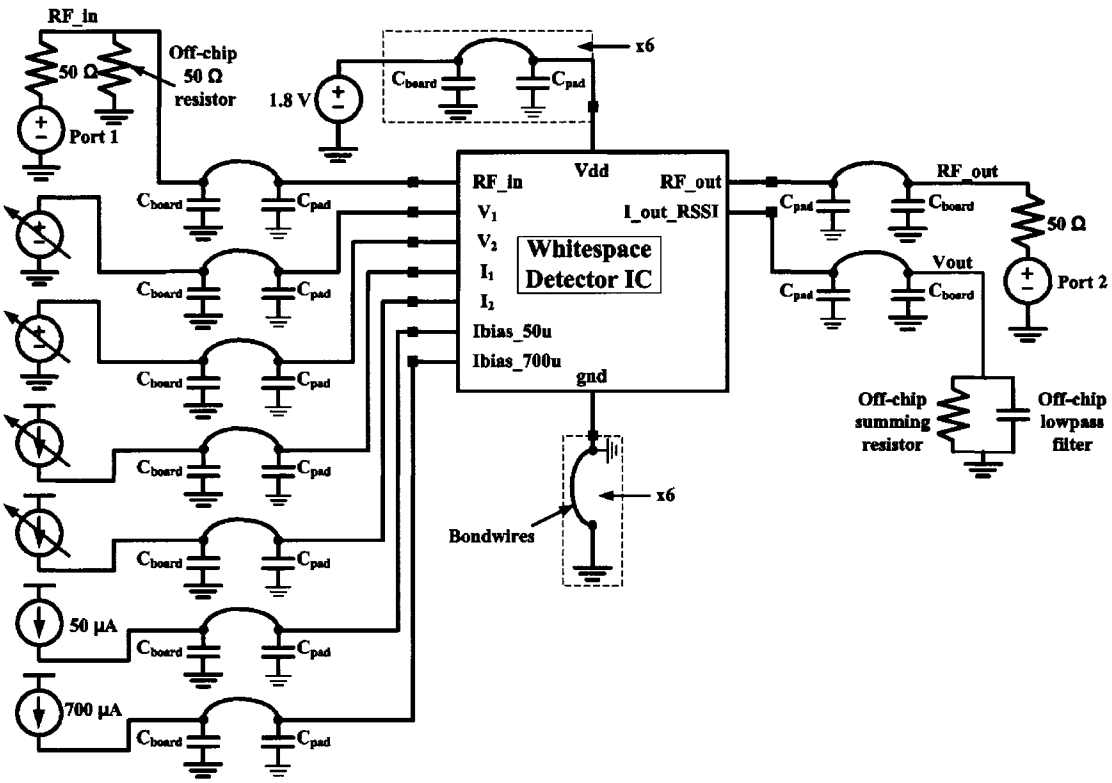

Figure 5.10: Test bench for simulating the whitespace detector IC in Cadence.

Each input and output signal has a parallel capacitance, C_{pad}, representing the pad capacitance for each pad on the chip. From the parasitic extraction of the layout, this is

found to be about 350 fF. Another capacitance, C_{board} = 500 fF, represents the capacitance associated with the printed circuit board (PCB) that is used to facilitate testing of the chip. Between these two capacitances is a bondwire model which represents the bondwire that connects the chip pad to the board pad. This model has an inductance of approximately 1 nH/mm. The bondwire inductance causes ground and supply bounce in the circuit, which is modelled in simulations. When the inputs to the circuits switch, this results in current switching on the voltage supply and ground. This causes fluctuations in the voltage supply and ground based on the equation V = L × di/dt, where L is the bondwire inductance and di/dt is the current switching. The bondwire inductance is proportional to the length of the bondwire. The bondwires in the simulation are modelled as being 4 mm long. The chip layout and printed circuit board design is done in such a way as to minimize the bondwire length on the critical RF signals. For this reason, the RF signals will have bondwires that are shorter than 4 mm when tested. Other, less critical signals, such as bias lines, may have longer bondwires up to 8 mm. Bondwire inductance is especially critical on the ground and 1.8 V supply lines due to the ground bounce that it may enable. For this reason, six ground pads and six supply pads are used to allow for multiple bondwires in parallel. This reduces the overall inductance and reduce the effects of ground bounce.

The whitespace detector has several bias voltages and currents that are provided by off-chip sources. These sources are generated on the PCB. The fixed current source of 50 μA is used to bias the circuits in the receive signal strength indicator (RSSI) and the

source follower in the bandpass filter. The 700 μA current source is used to bias the input and output buffers. The two variable current sources and the two variable voltage sources provide the biasing and tuning to the bandpass filter's active inductor.

The RF input signal is provided to the circuit by a 50 Ω port which represents the 50 Ω test equipment. A 50 Ω resistor is placed in parallel with the RF input, representing the resistor that is placed on the PCB to give a broadband 50 Ω match. The RF output of the bandpass filter that comes through the output buffer can be monitored by another 50 Ω port at the output. The output current of the RSSI creates the DC output voltage of the whitespace detector as it flows through the 14.4 kΩ summing resistor on the PCB. The 10 pF parallel capacitor acts as a low pass filter on the output voltage signal, removing high frequency ripple.

This test bench is used to perform system level tests on the whitespace detector. These tests are described in Section 5.5.

5.5 System Testing Simulations

The following describes a system test scenario that was performed on the whitespace detector integrated circuit using a Cadence simulation of the test bench shown in Figure 5.10. In this simulation, the whitespace detector circuit is tested with extracted parasitic capacitors and bondwire models to simulate the bonding to the test PCB. The RF input source is configured as eleven sinusoidal signals, representing a part of the broadcast television band around 200 MHz. Each of the signals has a peak amplitude of 50 μV (-86 dBV) and the signals are spaced by 6 MHz, as is done with television channels.

Some channels are turned on (50 μV) while others are turned off (0 μV). An additive white noise source is also connected to the RF input with a peak noise amplitude of 50 μV. This is to simulate the effect of input noise on the system.

The top graph in Figure 5.11 shows the discrete Fourier transform (DFT) of the input signal. This shows the spectrum of the input signals. There are signals present at 174 MHz, 180 MHz, 204 MHz, 210 MHz, 222 MHz, 228 MHz and 234 MHz. The amplitude of each of the input signals is -86 dBV. The DFT noise floor is approximately -120 dBV.

The next step in this scenario is to tune to each channel and take an output measurement to determine if a signal is present or absent in that channel. If no signal is found in that channel, that channel is deemed to be whitespace. For simulation purposes, five adjacent channels are examined: 198 MHz, 204 MHz, 210 MHz, 216 MHz and 222 MHz. Of these channels, no signal is present in the 198 MHz and 216 MHz channels. These should be detected as whitespace. Following the tuning procedure described in Section 3.3, the values of the tuning parameters required to tune to each of the five channels are determined. These tuning values are shown in Table 3.3 from S21 simulations of the bandpass filter, which are shown in Figure 3.19. As discussed in Section 3.3, the center frequency shown in this table in each tuning case is about 1 MHz higher than the center frequency where the maximum transient output signal is seen. This is why the transient system simulation described here uses the tuning values seen in Table 3.3 to tune to 198 MHz, 204 MHz, 210 MHz, 216 MHz and 222 MHz. For example, in one

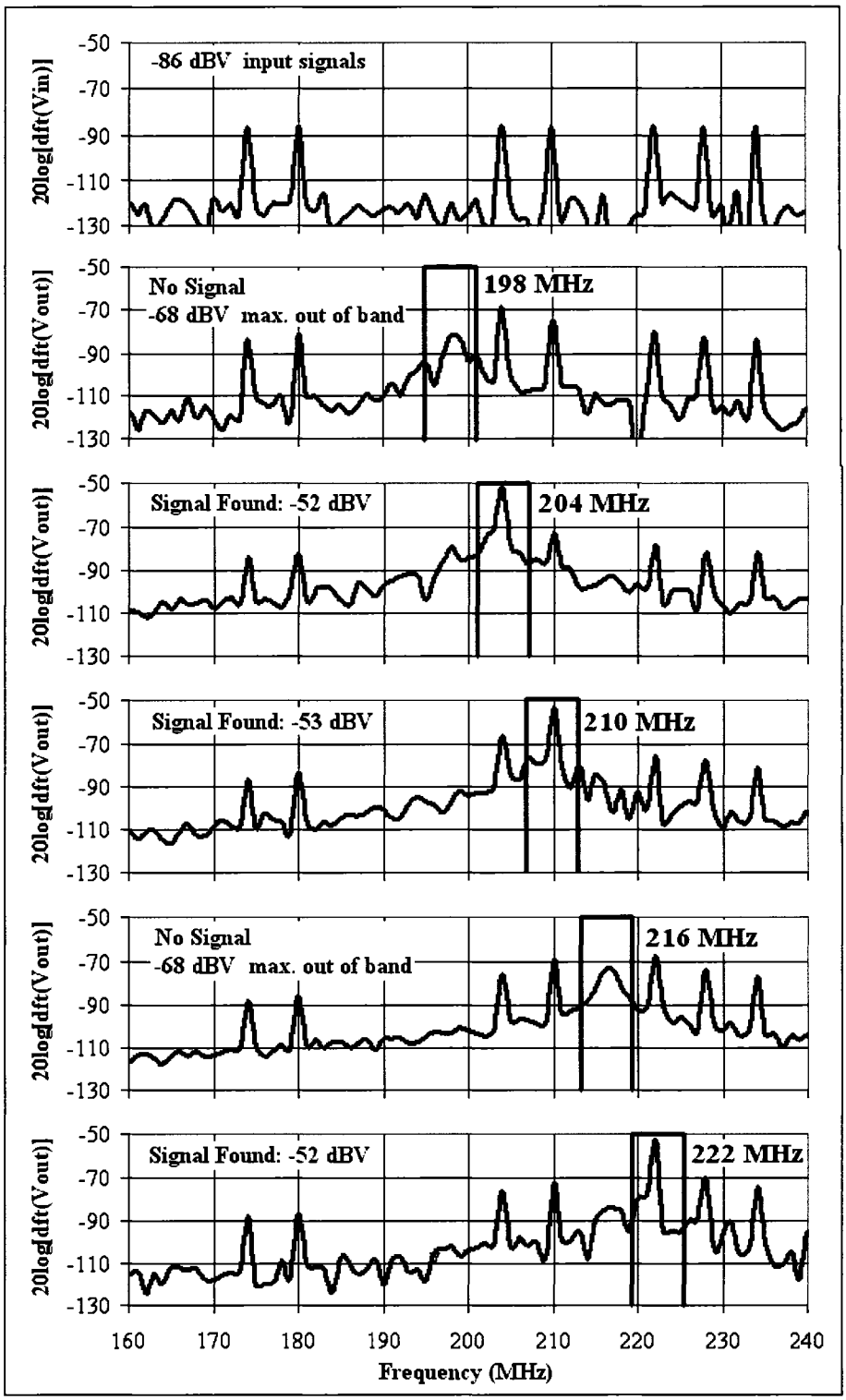

Figure 5.11: Discrete Fourier transform of the input signal and output signal in several tuning configurations.

tuning configuration, the S21 simulation shows the center frequency to be 199.1 MHz. Transient results show that the maximum gain is at 198 MHz. In the system simulation, the 199.1 MHz tuning configuration is used to locate the signal at 198 MHz

A transient simulation was run on the whitespace detector integrated circuit with the described input spectrum. The bandpass filter is initially tuned to 198 MHz then every 1.5 μs the tuning is changed to the next channel in the sequence. Figure 5.11 shows the discrete Fourier transform (DFT) of the input signal in the upper graph and the DFT of the output signal when tuned to each of the five channels, in the five lower graphs. The input magnitude of each channel is at -86 dBV. In the cases where the whitespace detector tunes to a channel with a signal, the output magnitude in this channel is about -52 dBV, showing approximately 34 dB of gain. In the worst case, an adjacent channel has an output that is 14.2 dB below the selected channel, showing the filters ability to suppress adjacent channels. In the cases where the whitespace detector tunes to an empty channel, the output DFT shows the highest signal of -67.6 dBV from an adjacent channel. This is still 14.8 dB below a case where there is a detected signal, meaning that this will not be mistaken for a detected signal.

The transient output voltage from the receive signal strength indicator (RSSI) is plotted in Figure 5.12. This plot shows the output versus time as the bandpass filter tuning is changed every 1.5 μs. As can be seen, a lower voltage around 0.95 V results when a signal is detected while a higher voltage of about 1.35 V is seen when whitespace has been detected. With a difference of 0.4 V, a comparator circuit will be able to

distinguish between the presence and absence of a signal.

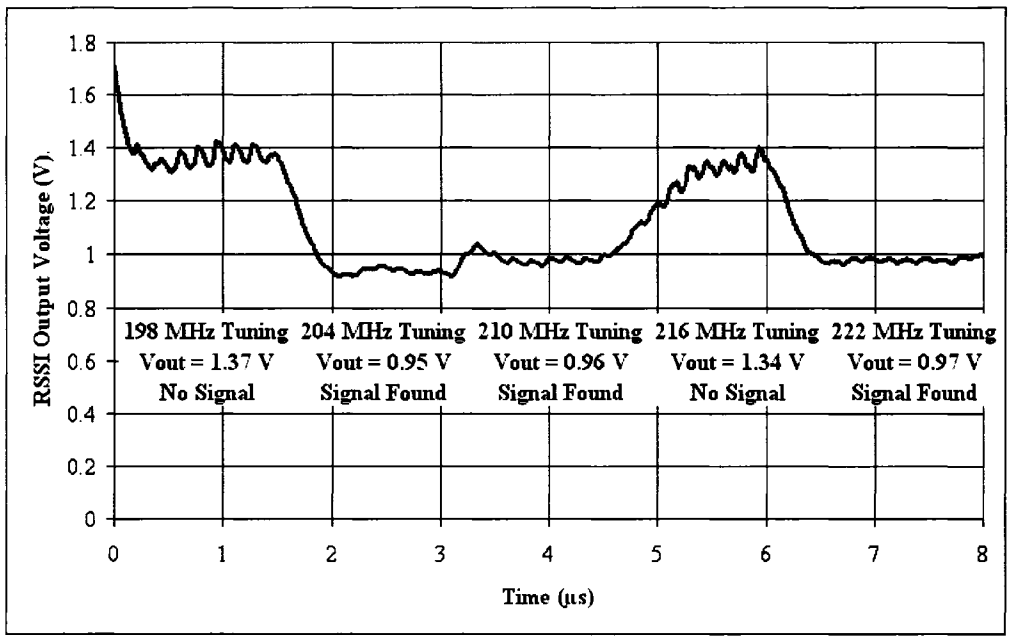

Figure 5.12: The transient output voltage of the RSSI as the bandpass filter is tuned to subsequent channels.

The output voltage signal in Figure 5.12 has ripple on it. The ripple is due to the normal operation of the rectifiers that supply the current to the output node. The amplitude of this ripple can be controlled by the size of the output capacitor forming the low pass filter on the output voltage line. A larger capacitor reduces the ripple but also slows the settling response of the output voltage, as described by Equation 4.2.9 and discussed during the RSSI design in Chapter 4. With a 10 pF capacitor in simulations, the largest ripple is about 60 mV. The time required for the output voltage to settle to its final value when the filter is switched is about 500 ns to 700 ns.

5.6 Chapter Summary

This chapter describes how the whitespace detector system is assembled into an integrated circuit (IC). The whitespace detector system has two main components, the tunable bandpass filter and RSSI. The IC also requires input and output buffering that interfaces the on-chip circuits with the off-chip, 50 Ω test environment. These buffer are designed to have high input and low output impedances. The IC also has an on-chip biasing network that allows off-chip currents to be routed to the required circuits in order to bias them. The layout for the complete integrated circuit is created with a perimeter of bond pads that are used to bond the fabricated circuit to a printed circuit board that is used to facilitate testing. From simulations, the expected voltages and currents for each of the input and output pads is obtained to give a starting point for testing the fabricated circuit.

Simulations are run on the full whitespace detector system that is extracted from the layout with parasitic capacitances. The test bench for this simulation accounts for pad capacitances and bondwire inductances on each of the input and output nodes. The system simulation shows the whitespace detector working for a scenario with an input that consists of various channels with transmitted signals and others that are whitespace. The whitespace detector is tuned to each channel and it gives an output that distinguishes between the channels that are being used and the ones that are whitespace.

Chapter 6

Measurement Results

The whitespace detector integrated circuit (IC) was fabricated in a 0.18 μm CMOS technology. A photograph of the IC is shown in Figure 6.1. This chapter describes the test procedure and measurement results obtained from testing the prototype circuit. To facilitate the testing of the IC, it is bonded to a printed circuit board (PCB). The design of the PCB is discussed in Section 6.1. The whitespace detector IC is designed so that the system can be tested as a whole but the bandpass filter and receive signal strength indicator can also be tested individually and independently of each other. Sections 6.2 and 6.3 describe the measurement results of each of these circuits.

6.1 Printed Circuit Board

A printed circuit board (PCB) designed specifically for the whitespace detector integrated circuit (IC) is used to facilitate its testing. The whitespace detector IC has 22 pads, which makes it difficult to test with inexpensive wafer probes. Testing with a PCB is a most cost effective solution. The PCB is more versatile than wafer probing since testing is not restricted to a location where a probing station is available. Special

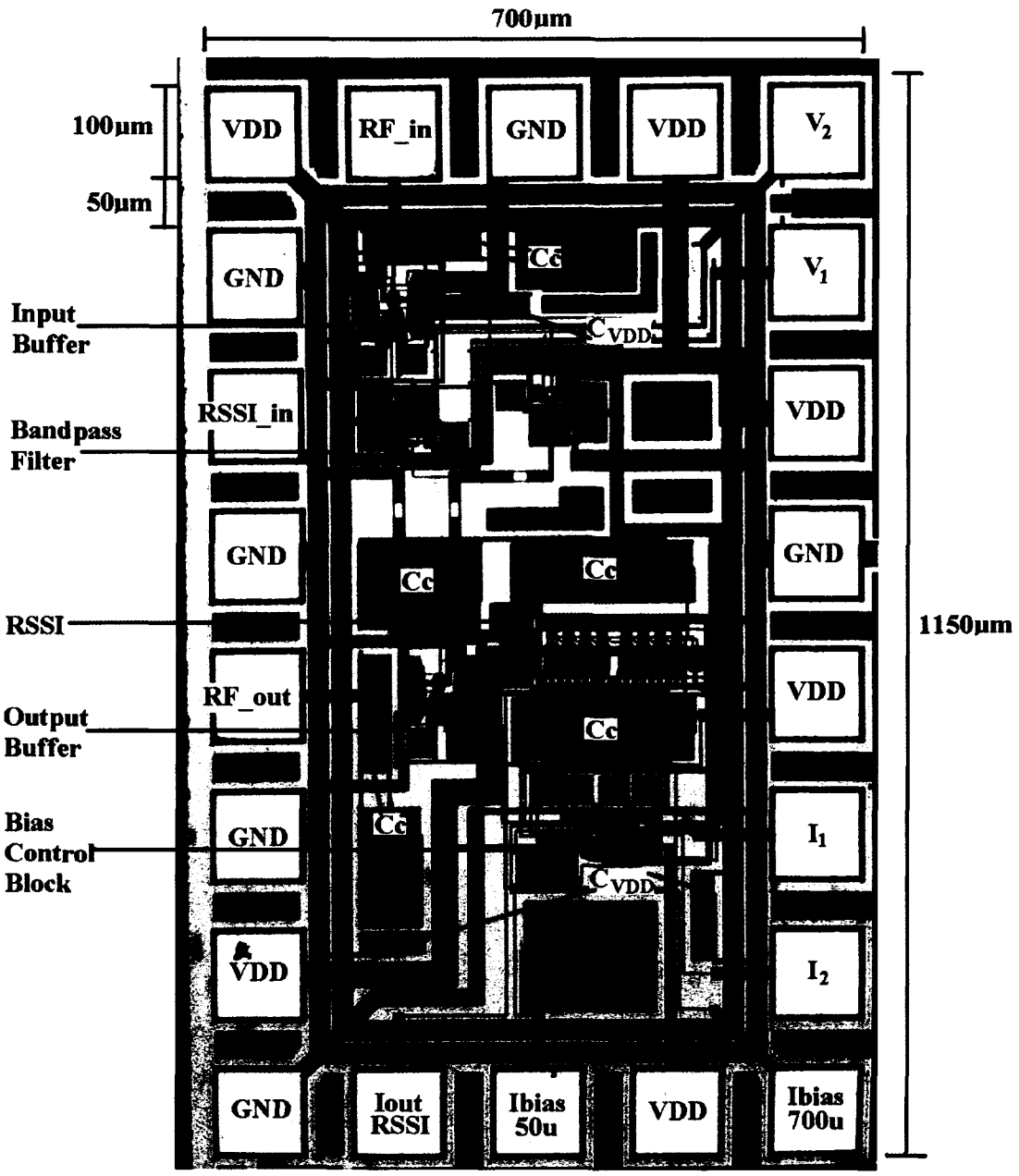

Figure 6.1: Photograph of the whitespace detector integrated circuit with inputs, outputs and main circuit blocks labelled.

circuitry for matching, electrostatic discharge (ESD) protection and bias control can be conveniently added to the PCB.

A layout of the PCB, including metal traces and footprints for components was designed*. The PCB is two inches by three inches in size and has gold-plated copper metal traces on an FR4 substrate. The top and bottom view of the PCB layout are shown in Figure 6.2.

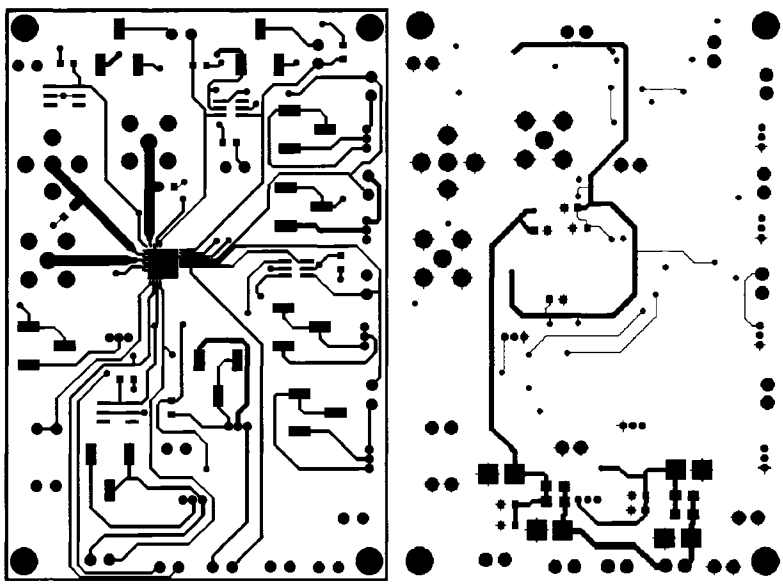

Figure 6.2: The top and bottom view of the PCB layout.

After the fabrication of the PCB, the whitespace detector IC was fastened to its footprint pad using a conductive silver epoxy. Each pad on the IC was bonded to a pad on the PCB using gold bondwires that have lengths of a few millimeters. Next, the components were soldered to the PCB. These components, including SMA connectors, resistors, capacitors and current sources, form the circuitry that is discussed in the

*The PCB was designed by Vladimir Vuckovic with input from the author of this thesis.

following subsections. A photograph of the PCB with all its components is shown in Figure 6.3. Each of the input and output connectors, as well as the main visible circuit components are labelled on the photograph.

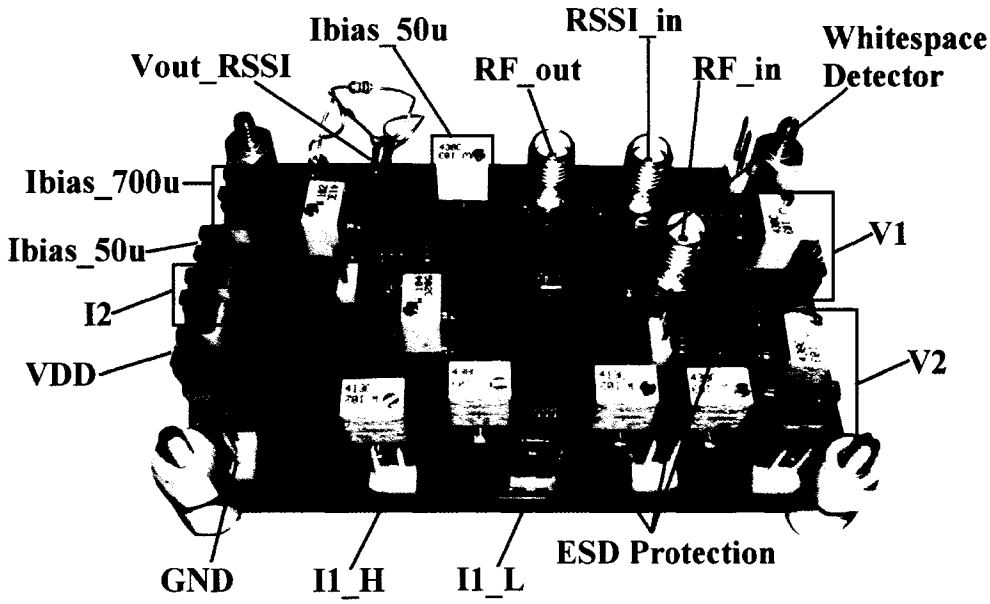

Figure 6.3: Photograph of the PCB with input and output pins and circuitry labelled.

6.1.1 The Power Supply Decoupling Circuitry

The power to the integrated circuit (IC) and printed circuit board (PCB) is provided by an external voltage source when the IC is tested. For the performance of the circuits on the IC, it is important that they have a clean DC voltage supply. However, the external voltage source can be noisy and the cables used to connect the power supply to the PCB can pick up noise from signals that are transmitted through the air. To reduce this noise, power supply decoupling circuitry is used between the supply and ground on the PCB. These are respectively labelled VDD and GND in Figure 6.3. The circuit used for

the power supply decoupling is shown in Figure 6.4.

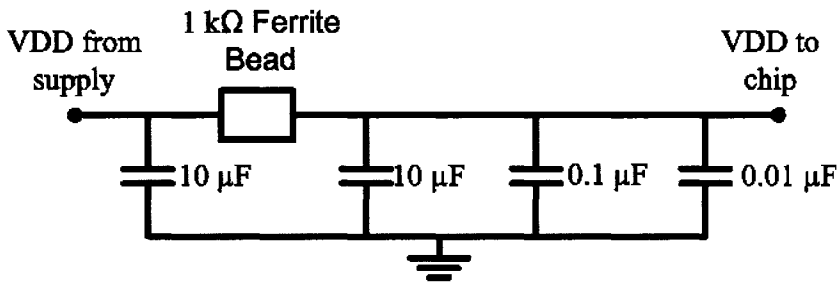

Figure 6.4: Power supply decoupling circuitry.

The circuitry is designed to filter noise from the power supply while allowing a clean DC signal to pass. The ferrite bead has a series inductance that performs this function by acting as a large impedance at high frequencies (1 kΩ at 100 MHz) and a small impedance (0.45 Ω) at DC [42]. Following this, a network of capacitors provides a low impedance path to ground for high frequency signals on the supply, acting as a low pass filter to further ensure that a clean DC signal is provided to the chip. In addition to this capacitor network, there are also four 0.1 μF capacitors between the supply and ground which are located close to the IC. All of the power supply decoupling circuitry is on the bottom of the PCB.

6.1.2 Bias Current Generation and Tuning Circuitry

Four bias currents are required for the IC. These currents are shown in Table 6.1 and the circuitry for generating them is identified in Figure 6.3. Two of these currents are fixed while two are variable. Off-chip current sources can be used to provide these bias current by connecting to the header pin that is attached to the appropriate bias current line. This requires four costly pieces of test equipment. An alternative method is also

available to generate the bias currents on the PCB. The circuitry for doing this is shown in the schematic in Figure 6.5.

Table 6.1: Currents Generated on the PCB and Potentiometers (POT) Required to Generate Them.

Current Name	Current Value	POT Required (max. resistance)
Ibias_700u	700 μA	1 kΩ
Ibias_50u	50 μA	10 kΩ
I2	2 μA - 50 μA	100 kΩ
I1	10 μA - 400 μA	10 kΩ (for 10 μA - 200 μA) 1 kΩ (for 20 μA - 400 μA)

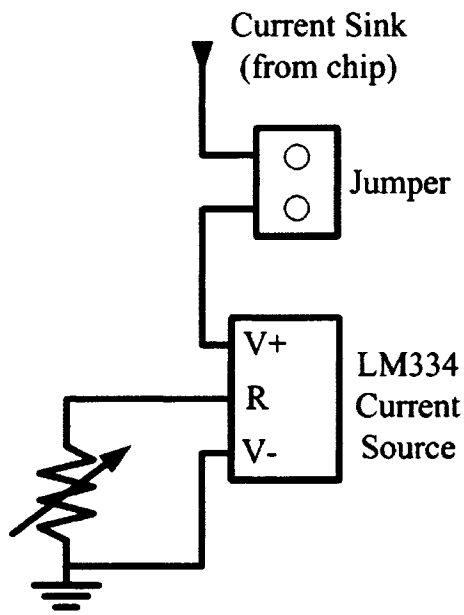

Figure 6.5: Bias current generation and tuning circuitry.

The LM334* is a current source chip that generates a current that is related to the resistance across its R and V- terminals, as shown in Figure 6.5. This relationship from [43] is written as

$$I_{REF} = \frac{227\mu V/T}{R_{SET}} = \frac{68mV}{R_{SET}} \tag{6.1.1}$$

*The LM334 is manufactured by the National Semiconductor Corporation.

where I_{REF} is the current generated by the source and R_{SET} is the resistance between the R and V- terminals. At a temperature of T = 298 Kelvin, the numerator is 68 mV.

The resistance R_{SET} is implemented with a potentiometer which can be tuned to give a wide range of resistances. Based on the minimum value of current required, the appropriate size of potentiometer is determined using Equation 6.1.1. The maximum resistance of the potentiometers are shown in Table 6.1 for the currents that they help generate. A sample calculation for determining the size of potentiometer required is shown in Equation 6.1.2.

$$R_{SET} = \frac{68mV}{I_{REF}} = \frac{68mV}{2\mu A} = 34k\Omega \tag{6.1.2}$$

For the current, I2, the minimum current required is I_{REF} = 2 μA. This requires a resistance of R_{SET} = 34 kΩ. In order to ensure that the potentiometer can be tuned to this resistance, it must have a larger maximum resistance than this. Therefore a 100 kΩ potentiometer is chosen for generating I2. The resistance of the potentiometer can be tuned down to 100's of Ωs, ensuring that the maximum current for I2 can also be generated.

I1 is a special case because it requires a large range of currents from 10 μA to 400 μA. For this reason, two current sources are used and the appropriate one is connected to generate the desired current. A 10 kΩ potentiometer allows the low range of currents, from 10 μA to 200 μA, to be generated and a 1 kΩ potentiometer allows the high range, from 200 μA to 400 μA, to be generated.

The current generated by the current source circuitry is passed into the IC by placing

a jumper from the current source pin to the pin that connects into the IC.

6.1.3 Bias Voltage Generation

The whitespace detector integrated circuit requires two off-chip tunable bias voltages, V1 and V2, which are shown in Figure 6.3. These voltages are used for bias tuning in the active inductor-based bandpass filter. As with the current sources, the bias voltages can be generated by external equipment. They can also be generated, as in Figure 6.6, using a potentiometer as a voltage divider. 10 kΩ potentiometers enable the bias voltages to be tuned from 1.8 V to zero volts.

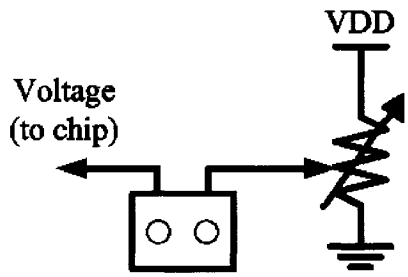

Figure 6.6: Bias voltage generation and tuning circuitry.

6.1.4 Electrostatic Discharge Protection

Electrostatic discharge (ESD) protection circuitry is used on the PCB to connect to all input bias lines of the integrated circuit that go to the gate of a transistor. This is to protect the IC against large voltages that can damage the transistors. The circuitry used for the ESD protection is shown in Figure 6.7 [44]. Under normal operation, the two diodes are reverse biased and the bias voltage or current feeds the chip as expected. If a large positive ESD voltage is on the bias line, the upper diode becomes forward

biased and the line is discharged to the supply. Similarly, a large negative ESD voltage forward biases the lower diode and the voltage is discharged through ground. If excess charge is built up on the VDD supply, the zener diode discharges it to ground.

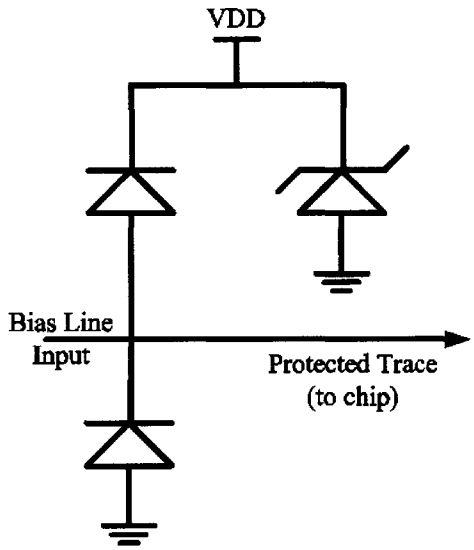

Figure 6.7: ESD protection circuitry located on the printed circuit board.

ESD protection is not implemented on the IC due to space limitations and uncertainty in the reliability of the available ESD protection circuitry in the supplied Cadence design kit. Typically, on-chip ESD protection is more effective. Fortunately, no ESD issues were observed during testing.

6.1.5 Output Low Pass Filter

The final notable circuit on the PCB is the low pass filter connected to Vout_RSSI in Figure 6.3. This filter consists of a parallel resistor and capacitor. The resistor is the summing resistor that converts the output current from the receive signal strength indictor (RSSI) into the output voltage and the capacitor removes ripple from this

voltage. During the design of the RSSI, a 14.4 kΩ resistor and a 10 pF capacitor were used. The components on the PCB fit into sockets so that these component values can be used or they can be swapped for other components if required.

6.2 Bandpass Filter Measurements

6.2.1 The Tunable Response of the Bandpass Filter

The filter response of the tunable bandpass filter is measured from its S21 S-parameter response using a network analyzer. This measurement shows the gain of the filter versus frequency from its input, RF_in, to its output, RF_out. In order to measure the filter's response, test equipment is set up as shown in Figure 6.8.

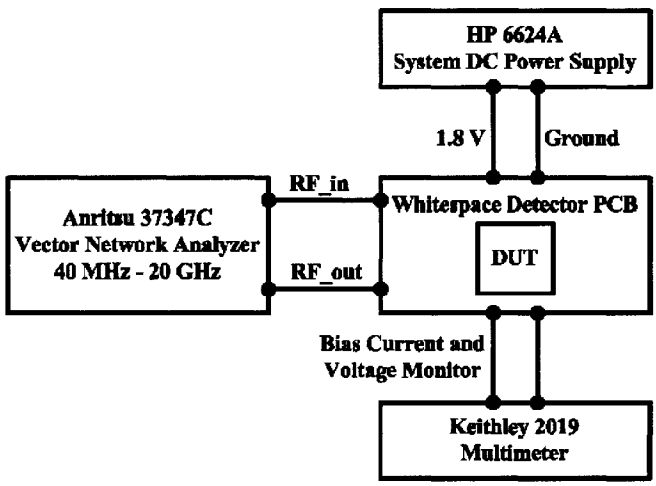

Figure 6.8: The equipment setup that is used to measure the S21 response of the bandpass filter.

The whitespace detector integrated circuit (IC) is the device under test, labelled DUT in the diagram. It is bonded to the whitespace detector PCB. Power and ground are provided to the PCB and IC from the HP 6624A System DC Power Supply. As

described in Section 6.1, the bandpass filter bias currents, I_1 and I_2, and bias voltages, V_1 and V_2, are generated on the PCB. The Keithley 2019 Multimeter is used to monitor the bias currents and voltages as they are tuned. The S21 response of the bandpass filter is measured by the Anritsu 37347C Vector Network Analyzer. The input of the bandpass filter, RF_in, is connected to Port 1 of the network analyzer and the output of the bandpass filter, RF_out, is connected to Port 2 of the network analyzer. Prior to testing the circuit, the network analyzer is calibrated over the frequency band of interest; 50 MHz to 1 GHz.

The plot in Figure 6.9 demonstrates the bandpass filter S21 response when the filter is tuned to have a center frequency of 183 MHz and a 3 dB bandwidth of less than 500 kHz. In order to achieve this response, the filter's tuning parameters are set to $I_1 = 55.2$ μA, $I_2 = 4.7$ μA, $V_1 = 650$ mV and $V_2 = 857$ mV. This high quality factor response shows that the filter works as designed at this frequency.

The next test demonstrates the tunability of the bandpass filter. With the other tuning parameters held constant ($I_2 = 4.7$ μA, $V_1 = 650$ mV, $V_2 = 857$ mV), the bias current, I_1, is tuned from 45.9 μA to 77.2 μA, allowing the filter response to be tuned from 177 MHz to 201 MHz while maintaining a high quality factor. These results are shown in Figure 6.10. The filter center frequency is tuned to 177 MHz, 183 MHz, 189 MHz, 195 MHz and 201 MHz, which correspond to the center frequency of the broadcast television bands for channels, 7 through 11. Each response has a high quality factor and in the worst case, the gain at the edge of an adjacent channel is 18 dB below the gain

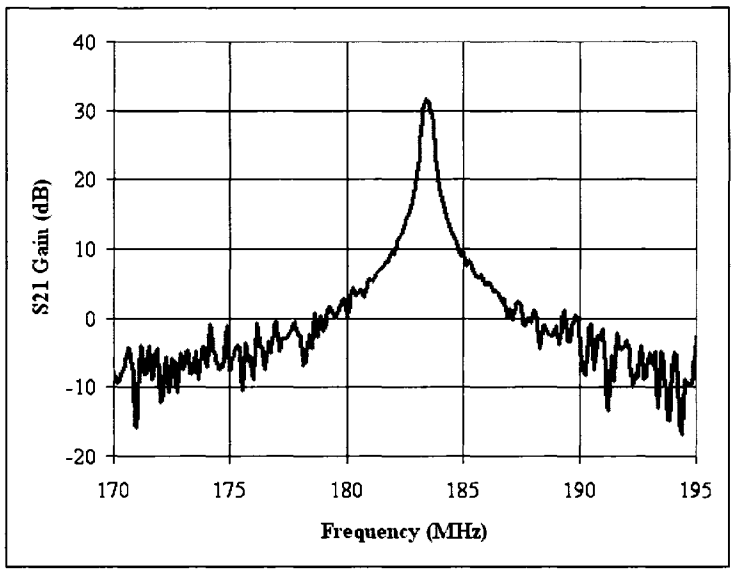

Figure 6.9: The measured S21 response of the bandpass filter when tuned 183 MHz.

at the center of the channel. In the best case this difference is 26 dB. This performance is close to and marginally better than the performance seen in simulations around the same frequency range. For the simulated results shown in Figure 3.19, the difference between the gain at the center of the band and that at the edge of the adjacent band is 15 dB. The difference relates to the accuracy of the tuning. By tuning the quality factor this value can be adjusted.

The bandpass filter is tested and shown to be able to tune to frequencies across the desired band of 70 MHz to 700 MHz. This is done by adjusting the drain current in the transistors of the active inductor by tuning the bias currents I_1 and I_2. Figure 6.11 shows the center frequency of the bandpass filter measured from the S21 results on the network analyzer as the drain current is tuned.

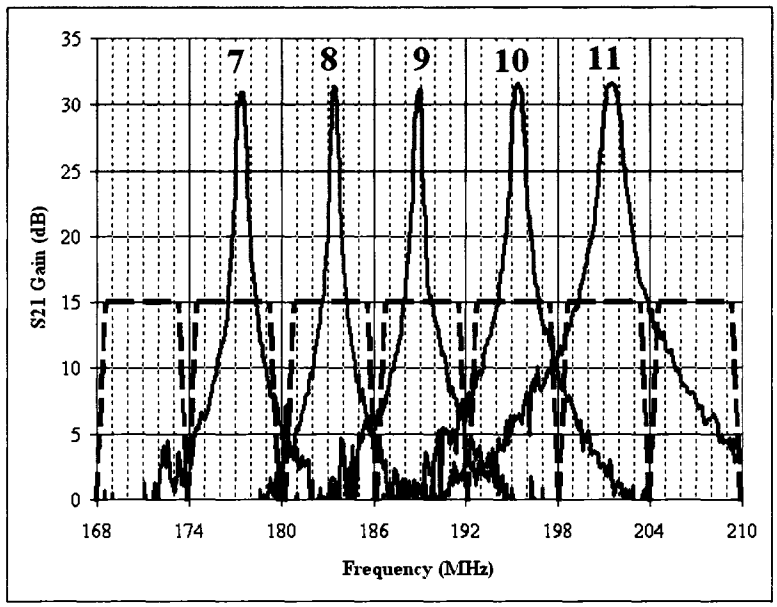

Figure 6.10: The measured S21 responses of the bandpass filter when tuned to five adjacent television channels.

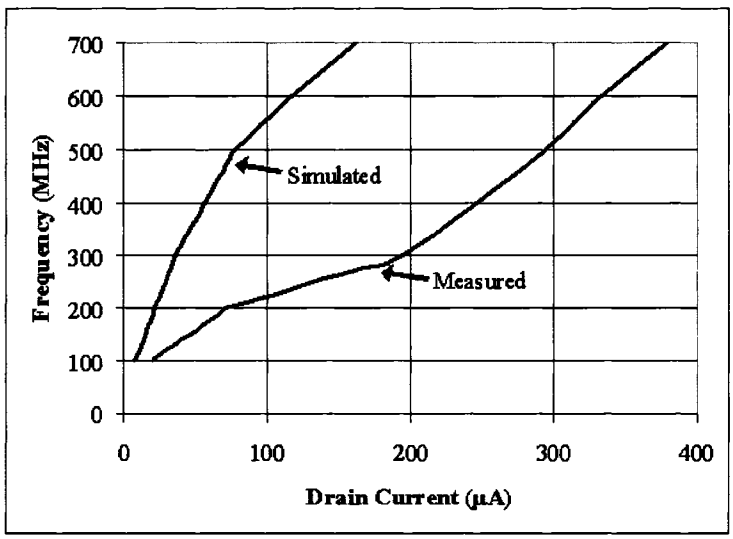

Figure 6.11: The measured and simulated center frequency of the bandpass filter versus the tuned drain current in the active inductor.

On the same graph, the simulated results are shown. Both the measured and simulated bandpass filter achieve the desired range of center frequencies and the frequency increases with increasing drain current. The measured results show that about three times more current is required to achieve the same center frequency. The fact that all center frequency tunings can be achieved despite this discrepancy is an advantage of the tunable nature of the circuit. The larger current required for a particular center frequency means that the overall inductance of the active inductor is higher than expected for a particular current. The higher current compensates for this by increasing the transconductances of the active inductor transistors which lowers the inductance, because it increases the denominator of Equation 3.2.1. The higher inductance can be caused by larger than expected transistor or parasitic capacitances, made up of the terms $(C_{gd1} + C_{gs2} + C_{gd2} + C_a)$ and $(C_{gs1} + C_{gs2} + C_{gd3} + C_b)$ in the numerator of Equation 3.2.1.

From S21 measurements on the network analyzer the tuning of the quality factor and gain of the bandpass filter can be seen when one of the control voltages is tuned. The tuning controls are set to $I_1 = 43\ \mu A$, $I_2 = 6.7\ \mu A$ and $V_2 = 858$ mV while V_1 is tuned from 0 to 90 mV. The graph in Figure 6.12 shows how the gain at the center frequency (which also indicates the quality factor of the filter) increases with the increasing control voltage until 65 mV where it levels off at a center frequency gain of approximately 20 dB. This is the same result as seen when the filter is simulated.

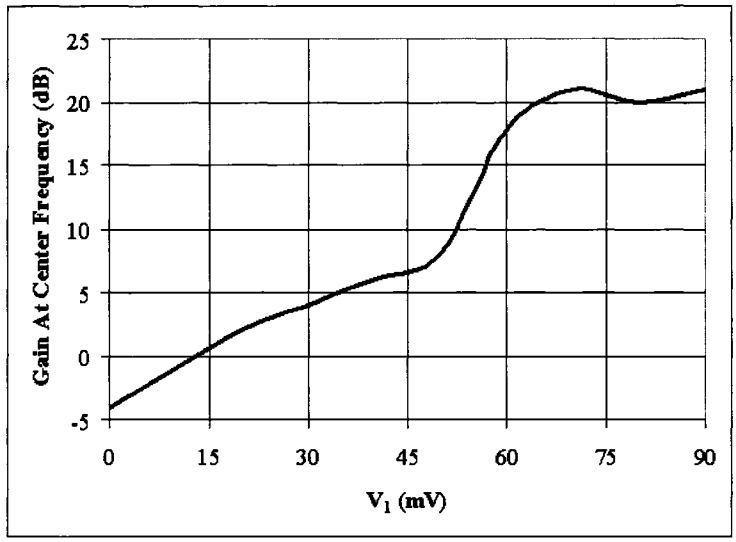

Figure 6.12: The gain at the center frequency of the filter from S21 measurements on the network analyzer as V_1 is increased.

6.2.2 The Transient Response of the Bandpass Filter

The transient, large-signal response of the bandpass filter is measured using the test equipment set up as shown in Figure 6.13. The 1.8 V supply voltage and ground are provided to the device under test by the HP 6624A System DC Power Supply while the bias currents and voltages for the circuit are monitored using the Keithley 2019 Multimeter. The Agilent E82570 PSG Analog Signal Generator provides the input signal for the test but the lowest signal level that it can provide is -20 dBm. The bandpass filter's operation range is for lower input level so the HP 8495B Variable Attenuator is connected in line with the input signal to provide attenuation. It provides a variable attenuation of 0 to 70 dB in increments of 10 dB. The signal from the attenuator is sent into the RF input to the bandpass filter, which is RF_in of the IC DUT on the whitespace detector PCB. The output signal of the bandpass filter, RF_out, is measured

by the Agilent infiniium 54855A DSO 7 GHz Oscilloscope.

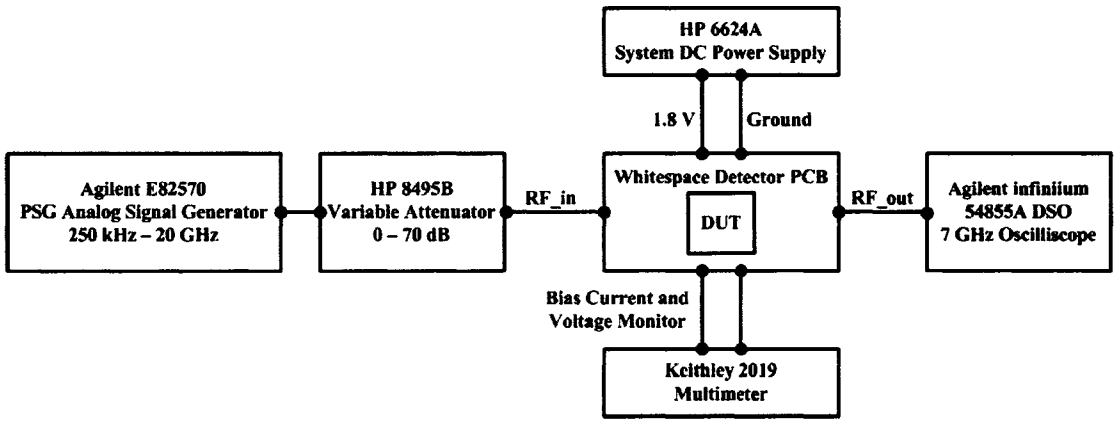

Figure 6.13: The equipment used for transient measurements of the bandpass filter.

The filter is tuned, following the tuning procedure described in Section 3.3.5, to have a center frequency of 170 MHz with a low gain of approximately 6 dB. When -50 dBm (2 mV_{p2p}) input signal is given at 170 MHz, the output on the oscilloscope shows a 4 mV_{p2p} (-44 dBm) signal at 170 MHz. This is shown as the top waveform in Figure 6.14. If the input signal is adjusted to 165 MHz, the output on the oscilloscope is barely discernable above the noise as shown in the middle waveform in Figure 6.14. This shows that the filter works to selectively transmit signals at the tuned frequency while filtering them out at other frequencies. The bottom waveform in Figure 6.14, shows the output when the gain at the center frequency is increased and the center frequency is tuned to 189 MHz. With the increased gain, the maximum signal seen at the output of the bandpass filter and the output buffer is approximately 6 mV_{p2p} (-40.5 dBm). This shows that the poor linearity of the bandpass filter limits the maximum output voltage. The linearity measurement results are discussed in Section 6.2.3. It should also be noted that the

small output voltages of the bandpass filter are not much larger than the noise produced by the system, though they are large enough to measure results.

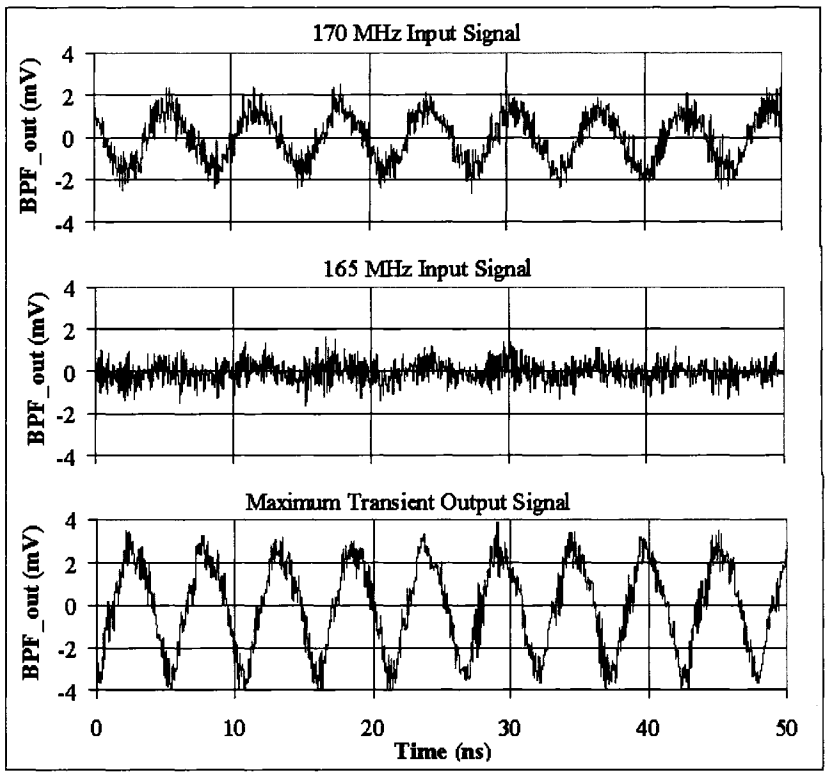

Figure 6.14: Transient output signals from the bandpass filter. TOP: 170 MHz signal with the filter tuned to 170 MHz. MIDDLE: 165 MHz signal with the filter tuned to 170 MHz. BOTTOM: 189 MHz signal with the filter tuned to 189 MHz and higher gain.

6.2.3 Bandpass Filter Linearity

The S21 response of the bandpass filter shows how the filter works under ideal circumstances and when signals are small. Since the filter is required to have a high quality factor that provides high gain, non-linear distortion occurs when larger input signals are seen by the filter. This non-linearity is measured using two-tone tests that show the filter's second-order intercept point (IP2) and third order intercept point (IP3). In order

to perform these tests, test equipment is set up as shown in Figure 6.15.

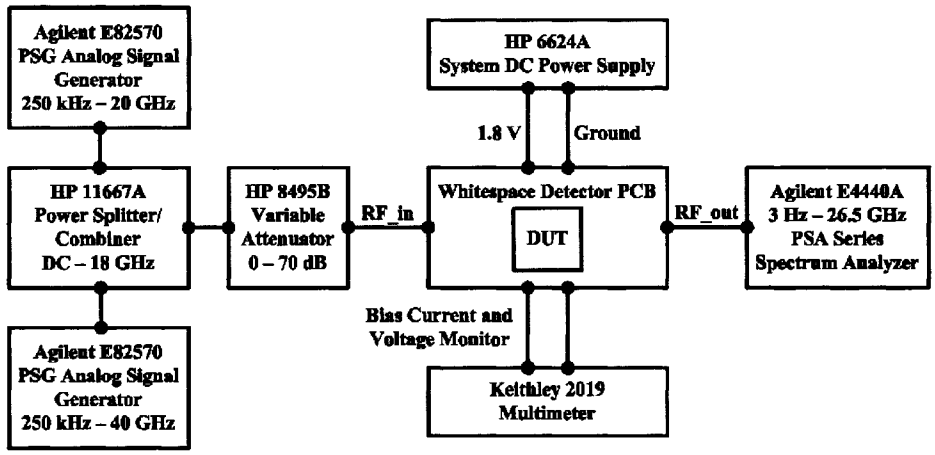

Figure 6.15: The equipment setup used to measure the linearity of the bandpass filter.

Two RF input tones are required in order to perform the two-tone test. Each of these tones is generated by an Agilent E8257D PSG Analog Signal Generator. The two tones are combined together using the HP 11667A Power Splitter/Combiner. The tones are then passed through the HP 8495B Variable Attenuator that can provide up to 70 dB of attenuation. This is required to generate input signals for the bandpass filter that are small enough to not cause non-linear distortion at the lowest range of input powers. The tones are input into RF_in of the bandpass filter and the output is taken from RF_out and is measured on the Agilent E4440A PSA Series Spectrum Analyzer.

Before beginning the tests, the setup is calibrated to account for loss in the combiner. Measurements show that the signal generated by the 250 kHz - 40 GHz signal generator experiences 6.5 dB of loss before it reaches the DUT. The signal from the 250 kHz to 20 GHz signal generator experiences 7 dB of loss. These losses are accounted for during all linearity measurements.

The Third Order Intercept Point (IP3)

When the bandpass filter is used for the application of the whitespace detector, there are certain scenarios when non-linearities can lead to a signal being falsely detected. These false-positive scenarios mean that no signal is present in the channel of interest but non-linearities in the bandpass filter make it seem like there is a signal present in the channel. One such scenario is caused by third-order intermodulation (IM3). When two frequency tones, f_1 and f_2, are applied to the filter, non-linearity can cause IM3 tones at frequencies of $2f_1 - f_2$ and $2f_2 - f_1$. If these tones are large enough and fall at the tuned frequency, they can cause this false positive scenario.

To test this scenario, the bandpass filter is tuned to a center frequency of 189 MHz and having a center frequency gain of 31 dB. This corresponds to the broadcast television channel 9 that operates from 186 MHz to 192 MHz. Two tones are applied in the adjacent channel at 192 MHz and 195 MHz. These can generate an IM3 tone at the center frequency of 189 MHz. Due to the high, narrowband gain of the filter, it was not possible to measure an increase in the intermodulation tone, right at the center frequency. Test results show that the center frequency signal level remains at approximately -50 dBm, even when one would expect to begin seeing the IM3 tone increasing at the center frequency.

In order to work around this situation and actually see the intermodulation tone, the same test is run again but the two input frequencies are chosen to give an IM tone at one channel away from the bandpass filter's tuned center frequency. At this point, the

gain is lower such that increases in the intermodulation tone can be seen and measured. This effectively runs the same test but with a lower gain. The input tones of 196 MHz and 197 MHz are used to create an IM3 tone at 195 MHz. The results of this test are shown in Figure 6.16.

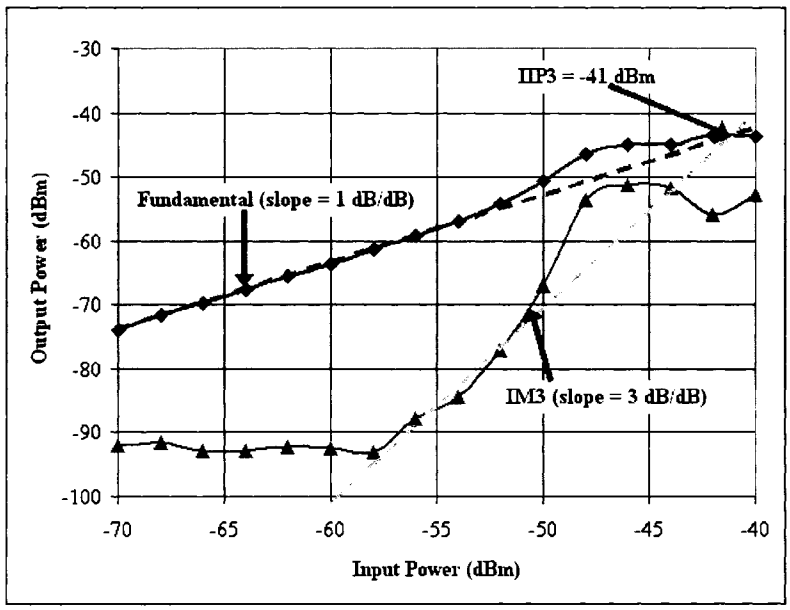

Figure 6.16: Measured third-order intercept results for the bandpass filter when 196 MHz and 197 MHz input tones create an IM3 tone at 195 MHz.

The input power of the two tones at 196 MHz and 197 MHz is swept from -70 dBm to -40 dBm and the output power is measured at 196 MHz for the fundamental output and 195 MHz for the IM3 output. The upper curve is the output power of the fundamental tone which has a linear slope of 1 dB/dB for low input signals. The lower curve shows the IM3 tone's output power. At low input signals, this tone can not be seen above the noise floor of about -92 dBm. Once it becomes apparent, it increases by 3 dB/dB. The input-referred third-order intercept point (IIP3) is found at the intersection point of the

1 dB/dB sloped line from the fundamental tone and the 3 dB/dB sloped line from the IM3 tone. From this test, IIP3 is shown to be -41 dBm, which demonstrates the poor linearity of the filter for "large" input powers. The filter may be linear at the low power range.

For comparison, the bandpass filter is simulated under the same conditions used for the test measurement. The filter is tuned to have approximately 31 dB of gain at the center frequency of 189 MHz. The input power of the two signals at 196 MHz and 197 MHz are swept from -70 dBm to -30 dBm while the IM3 output power is measured at 195 MHz. This is done using a periodic steady state (PSS) simulation and the results are shown in Figure 6.17. The simulation results also show the filter's poor linearity with IIP3 = -40 dBm compared to -41 dBm in the measured scenario shown in Figure 6.16.

The Second Order Intercept Point (IP2)

Another false-positive situation can arise due to second-order intermodulation (IM2). This is where two tones at frequencies f_1 and f_2 mix together to create an IM2 tone at $f_1 + f_2$ or $f_2 - f_1$. In circuits whose operation is limited to a narrow band of frequencies, these IM2 terms usually fall out of band and can be filtered. The application of the whitespace detector is from 70 MHz to 700 MHz. This band is wide enough that two tones within the band can mix to create an IM2 tone that is also in the band and cannot be filtered.

As is the case when testing the third order intermodulation, the high gain of the

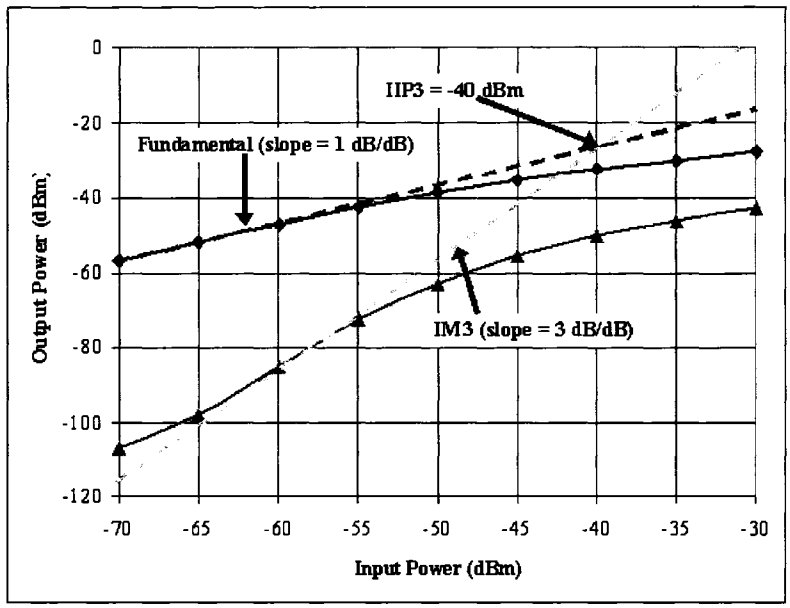

Figure 6.17: Simulated third-order intercept results for the bandpass filter when 196 MHz and 197 MHz input tones create an IM3 tone at 195 MHz.

filter makes it not possible to measure meaningful results if the two tones are mixed so that the IM2 tone falls right at the center frequency to which the filter is tuned. For this reason, the filter is tested with tones that cause the IM2 tone to be generated one channel away from the center frequency. Here, the lower gain permits measurements to be taken. The filter is tuned with a gain of 31 dB at 189 MHz. The two tones are applied with the frequencies f_1 and f_2 set to 91 MHz and 92 MHz. This creates the IM2 tone at 183 MHz. The results from these measurements are shown in Figure 6.18.

The input power of the two tones at 91 MHz and 92 MHz is swept from -60 dBm to -30 dBm and the output power is measured at 92 MHz for the fundamental output and 183 MHz for the IM2 output. The curve showing the fundamental tone has a linear slope of 1 dB/dB for low input signals. The curve showing the IM2 tone's output power

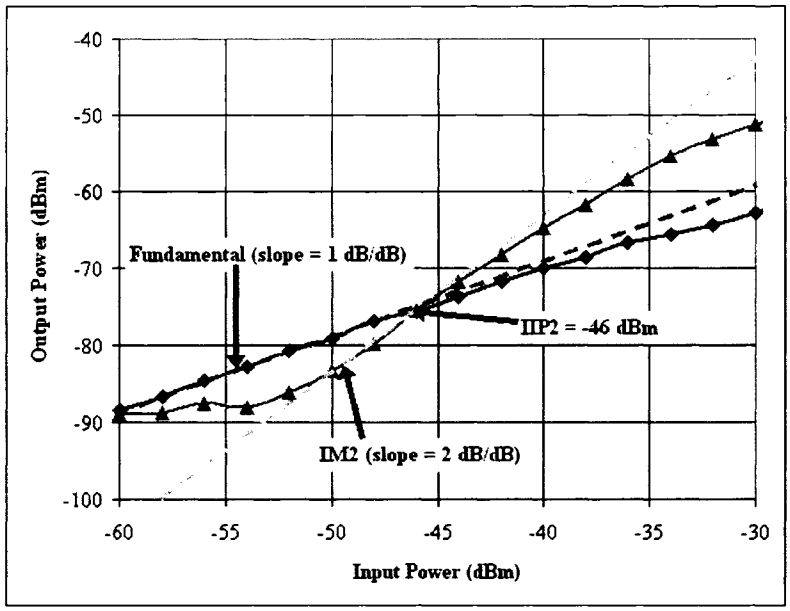

Figure 6.18: Measured second-order intercept results for the bandpass filter when 91 MHz and 92 MHz input tones create an IM2 tone at 183 MHz.

increases by 2 dB/dB after the signal level rises above the noise floor. The input-referred second-order intercept point (IIP2) is found at the intersection point of the 1 dB/dB sloped line from the fundamental tone and the 2 dB/dB sloped line from the IM2 tone. For this test, IIP2 is shown to be -46 dBm.

For comparison, the bandpass filter is simulated under the same conditions used for the test measurement. The filter is tuned to have approximately 31 dB of gain at the center frequency of 189 MHz. The input power of the two signals at 91 MHz and 92 MHz are swept from -70 dBm to -30 dBm while the IM3 output power is measured at 183 MHz. This is done using a periodic steady state (PSS) simulation and the results are shown in Figure 6.19. The simulation results also show the poor linearity of the bandpass filter with IIP2 = -45 dBm as compared to -46 dBm in the measured scenario

that is shown in Figure 6.18.

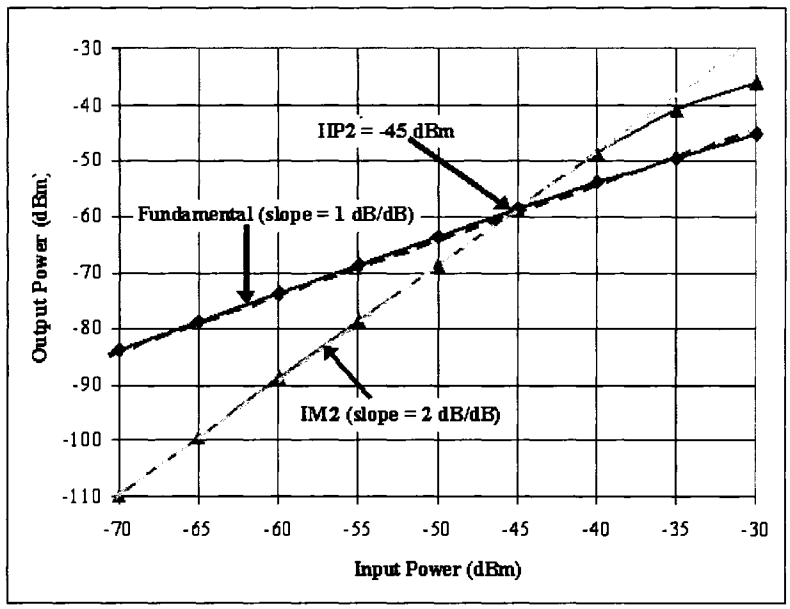

Figure 6.19: Simulated second-order intercept results for the bandpass filter when 91 MHz and 92 MHz input tones create an IM2 tone at 183 MHz.

6.3 Receive Signal Strength Indicator Measurements

The performance of the receive signal strength indicator (RSSI) is tested using the equipment set up as shown in Figure 6.20. As with the bandpass filter testing, the 1.8 V supply voltage and ground are provided by the HP 6624A System DC Power Supply while the bias current for the circuit is monitored using the Keithley 2019 Multimeter. To test the input amplitude to output voltage characteristic of the RSSI, a signal generator is used to provide the radio frequency (RF) input signal. The Agilent E82570 PSG Analog Signal Generator is used for this purpose. The lowest signal level that the signal generator can provide is -20 dBm. The RSSI is designed to work with signal levels as

low as -60 dBm. To provide these lower signal levels, the HP 8495B Variable Attenuator is connected in line with the input signal. It provides a variable attenuation of 0 to 70 dB in increments of 10 dB. The output signal from the attenuator is sent into the RF input to the RSSI, which is RSSI_in of the IC DUT on the whitespace detector PCB. The output voltage of the RSSI, Vout, is measured by the Agilent infiniium 54832D MSO 1 GHz Oscilloscope.

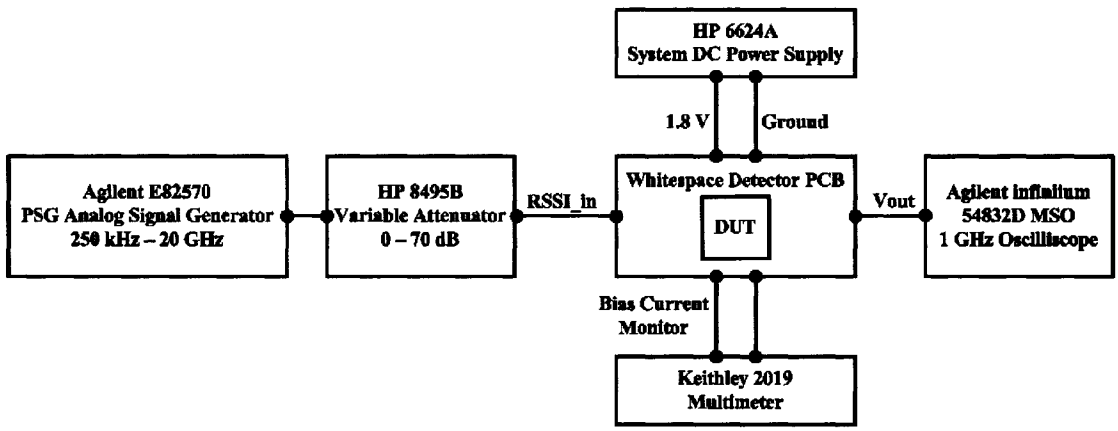

Figure 6.20: The equipment setup that is used to measure the input amplitude to output voltage characteristic of the RSSI.

6.3.1 RSSI Input Amplitude to Output Voltage Characteristic

The input amplitude to output voltage characteristic of the RSSI is measured using the test setup shown in Figure 6.20. Measurements of the output voltage, Vout, are taken as the amplitude and frequency of the input signal to the RSSI are varied. This results in the family of input amplitude versus output voltage curves shown in Figure 6.21. These curves are for input signals with frequencies from 100 MHz to 700 MHz.

The curves in Figure 6.21 show the inverse relationship between the input amplitude

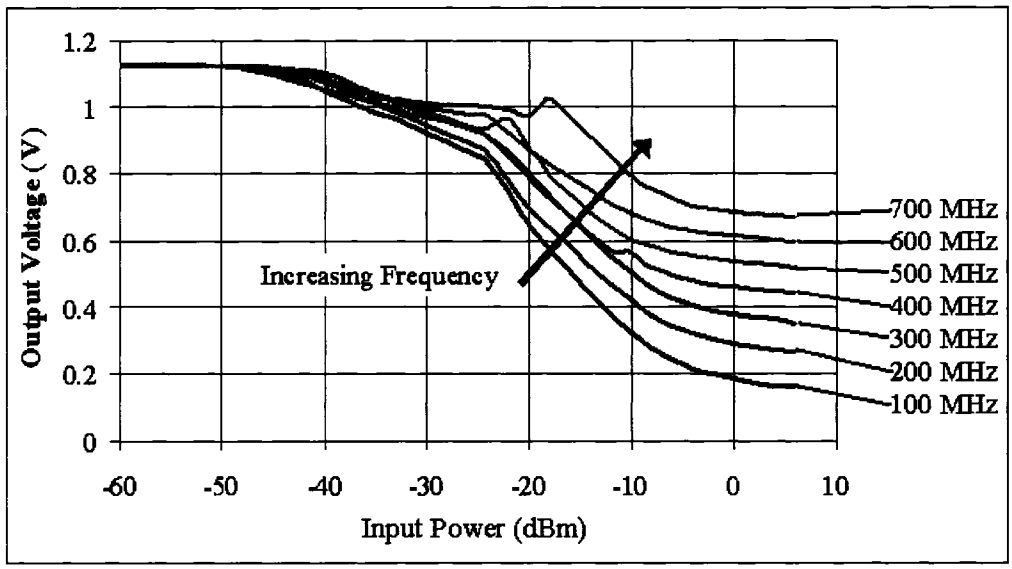

Figure 6.21: The measured RSSI input amplitude versus output voltage characteristic at various frequencies.

and output voltage as expected from simulations. Also as expected, the lower frequency curves have a greater variation. For larger input signals from -20 dBm to -10 dBm, the curves are fairly linear as designed and above -10 dBm they begin to flatten out. This is the same as was seen in simulations. For lower input signals, between -50 dBm and -20 dBm, the slopes of the curves change and level off to 1.15 V at about -45 dBm. The circuit is designed to operate with input signals as low as -60 dBm though the test results show a difference in the output voltage only down to -45 dBm. This and the non-linear shape of the curves in certain regions can be due to the RSSI's sensitivity not being low enough for small amplitude signals. This can cause noise to have a greater impact on the voltage levels. A -45 dBm input signal is equivalent to 3.6 mV peak-to-peak looking into the 50 Ω load impedance at the input of the RSSI. This is not large and it is reasonable to hypothesize based on the measurements that noise in the circuit

could have a comparable amplitude. This noise gets amplified by the RSSI and causes the RSSI output voltage to look the same as the lowest possible detectable signal. With a very low input signal, the RSSI output in simulations is pulled up as high as 1.7 V but due to the noise when testing, the level can only get pulled up as high as 1.15 V.

Figure 6.22 shows the input amplitude to output voltage response of the measured and simulated RSSI for a 200 MHz input signal. The simulated response is much more linear. For signals above -40 dBm (6.3 mV peak-to-peak), the simulated and measured results track each other with a maximum deviation of approximately 25 %. For signals below -40 dBm, the measured results level off at 1.15 V, which is suspected to be due to noise that overwhelms the input signal, as previously discussed.

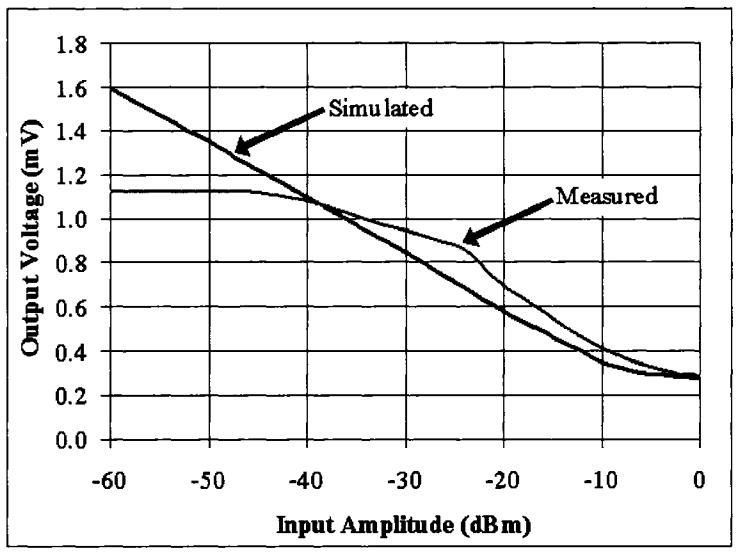

Figure 6.22: The measured and simulated RSSI input amplitude versus output voltage characteristic at 200 MHz.

6.3.2 RSSI Settling Response to an Input Amplitude Step

The input amplitude to output voltage curves in Figure 6.21 show the output voltage of the RSSI under various frequency and input amplitude combinations, when the voltage has settled. The measurements in this Section show the output transient voltage when an abrupt step occurs in the RSSI input amplitude. This abrupt change in input amplitude can model a change in the tuning of the bandpass leading to a channel with a higher or lower transmitting signal. It can also model a channel that is being monitored as whitespace, when the licensed user suddenly begins to transmit again. The RSSI response must be fast in order to capture this change so that the device using the whitespace detector can decide on the proper course of action.

The settling response test is done using the test bench shown in Figure 6.20. In order to capture the transition in the RSSI output voltage that gives its step response, the following steps are taken. The signal generator is set to give a 200 MHz signal at -30 dBm. The oscilloscope measures the output voltage to be 809 mV. The time scale on the oscilloscope is set to a large value of 50 ms. At a moment in time, the signal from the signal generator is manually increased to -10 dBm. This causes the RSSI output voltage on the oscilloscope to transition to 380 mV. Once this transition is seen, the image on the oscilloscope is stopped and frozen. Now, the transition is zoomed into in order to see the step response of the RSSI. This manual measurement procedure gives results that are satisfactory for the purpose of demonstrating the desired step response. The step response of the RSSI for this scenario is shown in Figure 6.23. The settling

time of the RSSI is measured as the time required for the output voltage to settle to within 1% of its final value. On the oscilloscope this is measured to be 10.1 μs.

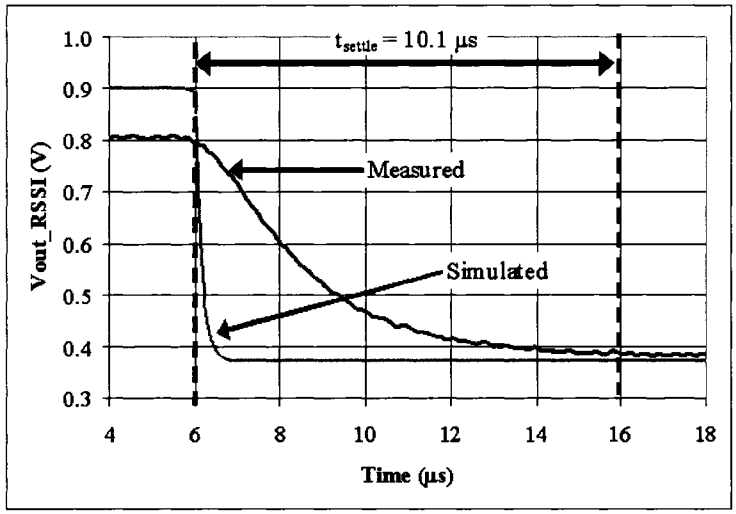

Figure 6.23: The measured and simulated step response of the RSSI to a changing input amplitude.

For comparison, the simulated settling response of the RSSI is also shown in Figure 6.23 for the same amplitude and frequency input signals that are used for the measured results. The simulated settling time is 700 ns, which is more than ten times faster than the measured results. This result is based on an output capacitance of 10.85 pF, as discussed in Chapter 4. The discrepancy can be due to capacitance in the cables used to measure the output voltage. The cable that is used has two alligator clips that connect to the RSSI output terminal and ground and lead to a BNC connector that connects to the oscilloscope. In Chapter 4, Equation 4.2.9 is used to calculate the settling time based on the output capacitance and resistance and is shown to predict the simulated settling time well. Using this equation, the total output capacitance in the test environment

is estimated to be 152 pF, which is greater than the output capacitance of the circuit alone.

6.4 Chapter Summary

This chapter describes the measurement results obtained from testing the whitespace detector integrated circuit (IC). The IC is bonded to a printed circuit board (PCB) that is designed specifically for the whitespace detector. The PCB facilitates the testing of the circuit while providing power supply decoupling and ESD protection. It also allows several bias currents and voltages for the circuit to be easily generated and tuned.

The whitespace detector is designed so that its two main components, the tunable bandpass filter and the receive signal strength indicator, can be tested individually from each other or together as a system. The bandpass filter test results show that its center frequency and quality factor can be tuned with the same trends that are predicted from theory and simulations. The filter's center frequency can be tuned across the whole range of desired frequencies from 70 MHz to 700 MHz. Measurements also show that its quality factor can be increased and decreased using the control voltages as predicted in theory and simulations. Transient measurements of the bandpass filter are shown. The linearity of the filter is found to be a limitation to its performance, as seen in simulations and discussed in previous works of literature [11,17]. The maximum signal levels seen at the output of the bandpass filter are approximately -40 dBm. This non-linearity issue is an area for future work in improving the bandpass filter.

The input amplitude to output voltage characteristic of the RSSI is measured over

the 70 MHz to 700 MHz frequency band and shown to follow the trends expected from simulations and theory. The settling response of the RSSI is measured for an input signal that has a sudden change in amplitude. Measurements show that the RSSI's dynamic range is lower than simulated, limiting its signal detection range to -45 dBm to 0 dBm. This, in combination with the bandpass filter's linearity limitation, make it difficult to measure results for the whitespace detector system as a whole. As independent circuits, measurement results show that both the tunable bandpass filter and the RSSI work.

Chapter 7

Conclusion

An integrated circuit (IC) that can be used to detect whitespace in the radio frequency (RF) spectrum was developed and tested. The whitespace detector IC was designed to operate in the broadcast television frequency band from 70 MHz to 700 MHz. The goal of whitespace detection is to locate unused bands of frequency so that they can be reused in order to increase the efficiency of the RF spectrum. The whitespace detector was constructed from a high quality factor, tunable bandpass filter and a receive signal strength indicator (RSSI).

The tunable bandpass filter is based on an active inductor. Equations were developed to predict the inductance and series resistance of the active inductor, as well as the center frequency and quality factor of the bandpass filter. Simulation results demonstrated the filter's ability to have its center frequency tuned across the 70 MHz to 700 MHz band. The trends for the tuning of the filter were analyzed. An analysis was also presented on the bandpass filter's performance with regards to transient simulations, linearity, noise and stability. The performance of the filter that was fabricated on the integrated circuit was tested. Simulation and measurement results showed agreement for linearity results

and tuning trends. Though linearity was found to be a limitation for the bandpass filter for larger input signals, its ability to tune across the desired frequency band with a high quality factor response was demonstrated.

The RSSI was built as a logarithmic amplifier from cascaded limiting amplifiers and rectifiers. A design procedure for constructing the RSSI from these sub-circuits was developed. The sub-circuits and the RSSI were simulated, showing that the RSSI has the desired logarithmic input amplitude to output voltage characteristic for input signals ranging from -60 dBm to -10 dBm, across the frequency band from 70 MHz to 700 MHz. The RSSI's settling response to a changing input signal was also examined. Test results of the RSSI showed its settling response and input to output characteristic. The measured input to output characteristic demonstrated the RSSI working for input signals ranging from -45 dBm to 0 dBm, over the 70 MHz to 700 MHz frequency band.

The bandpass filter and RSSI were assembled to form the whitespace detector. Simulations demonstrated the system's ability to distinguish between channels that have a signal present and those that are whitespace. Due to the bandpass filter's linearity limitations and the RSSI's low signal sensitivity limitations, measurement results did not show the two components working as a system. Improvements to these limitations are areas for future work.

7.1 Contributions to Research

The contributions in this thesis where improvements have been made to existing research include the following:

- More accurate equations than those presented in [11] for modelling the inductance and series resistance of the active inductor were derived in Section 3.1.1.
- An active inductor-based tunable bandpass filter with a wider center frequency tuning range of 70 MHz to 700 MHz was designed and is presented in Chapter 3.
- An algorithm for tuning the bandpass filter was developed as shown in Section 3.3.5.
- An RSSI was designed to work over a wide frequency band of 70 MHz to 700 MHz and is presented in Chapter 4.
- The settling time of the RSSI in response to a changing input amplitude was characterized as a performance parameter for working in a whitespace detector in Section 4.2.3.

A primary contribution of this thesis is that:

- A low power and small sized integrated circuit for detecting whitespace in the frequency spectrum was design using a tunable bandpass filter and a receive signal strength indicator.

7.2 Advantages and Disadvantages of the Design

Based on the design, simulation and measurement of the whitespace detector, an evaluation of its advantages and disadvantages can be made. Table 7.1 summarizes the

main advantages and disadvantages of the whitespace detector and its building block components, the tunable bandpass filter and receive signal strength indicator.

Table 7.1: Advantages and Disadvantages of the Whitespace Detector and its Sub-circuits

Advantages	Disadvantages
Small Integrated Circuit Size: Bandpass Filter: 50μm $\times$ 70μm RSSI: 80μm $\times$ 180μm System(including pads): 1150μm $\times$ 700μm	Nonlinearity of the bandpass filter may cause false signal detection, leading to lowered efficiency in whitespace detection.
Low Power Consumption: Bandpass Filter: 1.6 mW RSSI: 1.6 mW	Large blocker signals can saturate the bandpass filter, potentially hiding whitespace, due to the nonlinearity of the filter.
The filter has wide band center frequency tunability from 70 MHz to 700 MHz.	The bandpass filter tuning parameters must have high precision in order to keep the filter's center frequency and quality factor locked.
The RSSI's fast acquisition time of less than 1 μs gives potential for fast sweeping of the frequency band.	Measurement results show that the RSSI's input dynamic range is limited by its sensitivity to low input signals.
Low power and small circuit area allow multiple circuits to be placed in an array for improved system performance.	

7.3 Future Work

There are several areas for future work to improve the performance and enhance the whitespace detector. Investigation can be made to improve the linearity of the bandpass filter, giving it the ability to work with larger input signals. Test results show that the RSSI does not work for input signals that are below -40 dBm, so improvements can be made here. The whitespace detector can be enhanced with circuitry that automatically controls its tuning and circuitry that interprets and allows adaptation to the output

detection signal.

7.3.1 Bandpass Filter Linearity

The non-linearity of the bandpass filter is a limitation of this design, and active inductors in general [11, 17]. The high quality factor and gain of the filter at its center frequency contribute to the linearity problem. Another contribution is the fact that the transistors in the active inductor are stacked four-high and require significant voltage headroom for all of them to remain in saturation. An area to investigate to improve the linearity is to work with an increased supply voltage, though this would result in higher power and make the circuit more difficult to integrate into systems that are moving towards lower supply voltages. Attempts were made to adjust the transistor sizes in the active inductor but this did not improve linearity. A new topology may be needed for the active inductor that provides better linearity.

If only small improvements could be made to the linearity of the bandpass filter, alternate system considerations would be required for the whitespace detector. For example, some sort of automatic gain or attenuation control circuitry could be used before the bandpass filter to limit input signal levels to those that are within the linear region of the bandpass filter. This circuitry could use the receive signal strength indicator to monitor the output level from the bandpass filter and feedback a signal that tells whether the attenuation at the input should be increased or decreased.

7.3.2 RSSI Sensitivity

Simulations show that the RSSI has the desired logarithmic input amplitude to output voltage response for input signals from -60 dBm to -10 dBm. Measurement results show that the RSSI's input sensitivity only goes down to -45 dBm. Input signals below this appear to be overwhelmed by noise. Though care was taken to limit the effect of ground bounce, this could also be a source of the problem and further investigation could be done into limiting it. A possible solution may be to have a broadband low noise amplifier before the RSSI. This would limit the noise into the RSSI while providing gain to the signal that is output from the bandpass filter. Improving the sensitivity of the RSSI, along with improved linearity of the bandpass filter would allow the whitespace detector system to be tested to view similar results to the simulations shown in Section 5.5.

7.3.3 RSSI Voltage Offsets

The input dynamic range of the RSSI can be limited by offsets in the output voltage of its limiting amplifier stages. Further work can be done to investigate this issue as a possible improvement to the dynamic range. Since the amplifier stages are DC coupled, any output offset of a given stage gets transferred as a DC input to the following stage. The stage then provides gain to this DC input, resulting in further offset in the following stage. The overall result is that, after several limiting amplifier stages, the offset has accumulated so that latter stages in the RSSI no longer contribute to the RSSI output. This effectively reduces the number of stages in the RSSI and lowers its dynamic range.

7.3.4 Bandpass Filter Tuning Control

The tuning of the bandpass filter is accomplished by manually adjusting the bias control currents and voltages of the filter. Future work could include the design of additional circuitry to control the tuning of the bandpass filter. This additional tuning control circuitry could use the tuning algorithm described in Section 3.3.5 as the starting point for its implementation. It could be implemented using custom analog or digital circuitry or a Field Programmable Gate Array (FPGA). The tuning control circuitry could monitor the signals at the output of the bandpass filter and receive signal strength indicator. Using knowledge from these signals and the tuning algorithm, the bandpass filter's tuning parameters could be altered to adapt the tuning characteristics of the filter to meet the required needs. The circuitry may need to incorporate a phase-locked loop to track and lock the center frequency of the bandpass filter.

7.3.5 Whitespace Detection Interpreter

Simulation results in Section 5.5 show that the RSSI gives an output voltage that can be used to distinguish between a detected signal and whitespace. Future work could include the design of circuitry that interprets this output voltage and makes a decision as to whether whitespace or an occupied channel has been detected. This circuitry could involve a comparator that makes this decision by comparing the RSSI output voltage with a threshold value. An analog to digital converter could convert the output voltage to digital signals so that some digital circuitry can interpret if whitespace has been detected. Along with making a decision on the detection of whitespace, the circuitry

could feed back signals to any automatic gain controller that is used to limit the gain before the bandpass filter. The interpretation and decision making circuitry would have to account for variations in the RSSI response over frequency when making its decisions.

Appendix A

Equation Derivations

A.1 Active Inductor Input Impedance Equation

Equation A.1.1 describes the input impedance of the active inductor. Individual terms from this equation are shown in Equations A.1.2 through A.1.7.

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} = \frac{1 + sA + s^2B}{C + sD + s^2E + s^3F} \tag{A.1.1}$$

$$\begin{aligned} A = {} & r_{o1}(C_{gd1} + C_{gs2} + C_{gd2}) + r_{o3}(C_{gs1} + C_{gs2} + C_{gd3}) \\ & + r_{o1}r_{o3}(g_{m1} + g_{mb1})(C_{gd1} + C_{gs2} + C_{gd2}) \end{aligned} \tag{A.1.2}$$

$$B = r_{o1}r_{o3}(C_{gs1} + C_{gd3})(C_{gd1} + C_{gs2} + C_{gd2}) \tag{A.1.3}$$

$$C = r_{o1}g_{m2}(g_{m1} + g_{m3}r_{o3}[g_{m1} + g_{mb1}]) \tag{A.1.4}$$

$$\begin{aligned} D = {} & r_{o1}(g_{m1}[C_{gd1} + C_{gs2}] + g_{m2}C_{gd2} + g_{mb1}C_{gs2}) + r_{o3}g_{m3}C_{gs2} \\ & + r_{o1}r_{o3}(g_{m1}g_{m3}[C_{gd1} + C_{gs2}] + g_{m3}g_{mb1}[C_{gd1} + C_{gs2}] + g_{m2}C_{gd2}[g_{mb1} + g_{m1}]) \end{aligned} \tag{A.1.5}$$

$$
\begin{aligned}
E = {} & r_{o1}(C_{gs2}C_{gs3} + C_{gd2}C_{gs3} + C_{gd1}C_{gs3} + C_{gs1}C_{gs2} + C_{gs2}C_{gd3}) \\
& + r_{o1}r_{o3}(g_{m1}[C_{gs2}C_{gd2} + C_{gd2}C_{gs3} + C_{gs2}C_{gs3} + C_{gd1}C_{gs3}] \\
& + g_{m2}[C_{gd2}C_{gd3} + C_{gs1}C_{gd2}] + g_{mb1}[C_{gs2}C_{gs3} + C_{gd2}C_{gs3}] \\
& + g_{m3}[C_{gs2}C_{gd3} + C_{gd1}C_{gd3} + C_{gs1}C_{gd1} + C_{gs1}C_{gd2} + C_{gd2}C_{gd3} + C_{gs1}C_{gs2}])
\end{aligned}
\tag{A.1.6}
$$

$$
\begin{aligned}
F = {} & r_{o1}r_{o3}(C_{gd1}C_{gs3}C_{gd3} + C_{gs2}C_{gd2}C_{gd3} + C_{gd1}C_{gd2}C_{gd3} \\
& + C_{gs1}C_{gd1}C_{gd2} + C_{gs1}C_{gs2}C_{gd2} + C_{gs1}C_{gd1}C_{gs3} + C_{gs1}C_{gd2}C_{gs3} \\
& + C_{gs2}C_{gs3}C_{gd3} + C_{gd2}C_{gs3}C_{gd3} + C_{gs1}C_{gs2}C_{gs3})
\end{aligned}
\tag{A.1.7}
$$

In order to derive simplified equations for the inductance and series resistance of the active inductor from Equation A.1.1 a numerical analysis of the equation is performed. Using DC operating point simulations, the values of the coefficients, A through F, are calculated and their relative sizes compared. This is shown in Table A.1.

Table A.1: Numerical Evaluation of Equation A.1.1

Term	Magnitude at 100 MHz	Magnitude Relative to Largest Term
ωA	10^{1}	1
ω^2B	10^{-1}	0.01
C	10^{-1}	1
ωD	10^{-3}	0.01
ω^2E	10^{-4}	0.001
ω^3F	10^{-5}	0.0001

Table A.1 shows that the term containing A is 100 times larger than the other term in the numerator. The term containing C is at least 100 times larger than all of the other terms in the denominator. This is valid for the 70 MHz to 700 MHz range of frequencies over which the inductors is used. From this information, Equation A.1.1 can be further reduced to

$$
Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} = \frac{1 + sA}{C} \tag{A.1.8}
$$

with less than one percent loss of accuracy.

The real part of Equation A.1.8 can give a simplified equation for the series resistance of the active inductor, which is shown as

$$R_S = \frac{1}{C} = \frac{1}{r_{o1}g_{m2}(g_{m1} + g_{m3}r_{o3}[g_{m1} + g_{mb1}])}. \quad \text{(A.1.9)}$$

The imaginary part of Equation A.1.8 can give a simplified equation for the inductance of the active inductor, which is shown as

$$L = \frac{A}{C} = \frac{r_{o1}(C_{gd1}+C_{gs2}+C_{gd2})+r_{o3}(C_{gs1}+C_{gs2}+C_{gd3})+r_{o1}r_{o3}(g_{m1}+g_{mb1})(C_{gd1}+C_{gs2}+C_{gd2})}{r_{o1}g_{m2}(g_{m1}+g_{m3}r_{o3}[g_{m1}+g_{mb1}])}. \quad \text{(A.1.10)}$$

Through factoring, Equation A.1.10 can be rearranged to give

$$L = \frac{r_{o1}(C_{gd1} + C_{gs2} + C_{gd2})(1 + r_{o3}[g_{m1} + g_{mb1}]) + r_{o3}(C_{gs1} + C_{gs2} + C_{gd3})}{r_{o1}g_{m2}(g_{m1} + g_{m3}r_{o3}[g_{m1} + g_{mb1}])}. \quad \text{(A.1.11)}$$

A.2 Derivation of the Bias Current Versus Frequency Trends

The following is the derivation of curves of best fit to describe the trends of the required bias currents, I_1 and I_2, versus the center frequency of the bandpass filter. These curves are shown with simulated results in Figure 3.23. For these derivations, all currents are in μA and all frequencies, represented by f_0, are in MHz. The curves of best fit represent the trends observed using the typical BSIM3 v3.2 transistor models for transistors in the TSMC 0.18μm CMOS technology [39].

The bias current, I_1, that is required to tune to a particular center frequency follows a second order polynomial trend with respect to the center frequency. From simulated

results in Table 3.4, three frequency/current pairs are taken to determine the coefficients A, B and C, in the polynomial given by

$$Af_0^2 + Bf_0 + C = I_1. \tag{A.2.1}$$

These pairs are: (200 MHz, 27 μA), (400 MHz, 69 μA) and (600 MHz, 136 μA). Substituting these pairs into Equation A.2.1, gives Equations A.2.2, A.2.3 and A.2.4.

$$A(200)^2 + B(200) + C = 27 \tag{A.2.2}$$

$$A(400)^2 + B(400) + C = 69 \tag{A.2.3}$$

$$A(600)^2 + B(600) + C = 136 \tag{A.2.4}$$

Equation A.2.4 minus Equation A.2.3 gives

$$200000A + 200B = 67. \tag{A.2.5}$$

Equation A.2.3 minus Equation A.2.2 gives

$$120000A + 200B = 42. \tag{A.2.6}$$

Equation A.2.5 minus Equation A.2.6 gives

$$80000A = 25. \tag{A.2.7}$$

Solving Equation A.2.7 gives A = 0.0003125. Substituting A into A.2.6 gives B = 0.0225. Substituting A and B into A.2.2 gives C = 10. With these three coefficients, the second order polynomial that describes the best fit curve for I_1 can be written as

$$I_1 = 0.0003125f_0^2 + 0.0225f_0 + 10 \tag{A.2.8}$$

where I_1 is the bias current in μA and f_0 is the frequency in MHz.

The bias current, I_2, that is required to tune to a particular center frequency follows a linear trend with respect to the center frequency. From simulated results in Table 3.4, two frequency/current pairs are taken to determine the coefficients D and E, in the linear given by

$$I_2 = Df_0 + E. \tag{A.2.9}$$

These pairs are: (300 MHz, 9.5 μA) and (400 MHz, 13 μA). Substituting these pairs into Equation A.2.9, gives Equations A.2.10 and A.2.11.

$$9.5 = D(300) + E \tag{A.2.10}$$

$$13 = D(400) + E \tag{A.2.11}$$

Isolating E in Equation A.2.10 and Equation A.2.11 and equating them gives

$$9.5 - 300D = 13 - 400D. \tag{A.2.12}$$

Solving Equation A.2.12 gives D = 0.035. Substituting D into A.2.10 gives E = -1. With these two coefficients, the linear equation that describes the line of best fit for I_2 can be written as

$$I_2 = 0.035f_0 - 1. \tag{A.2.13}$$

where I_2 is the bias current in μA and f is the frequency in MHz.

Appendix B

Layout Key

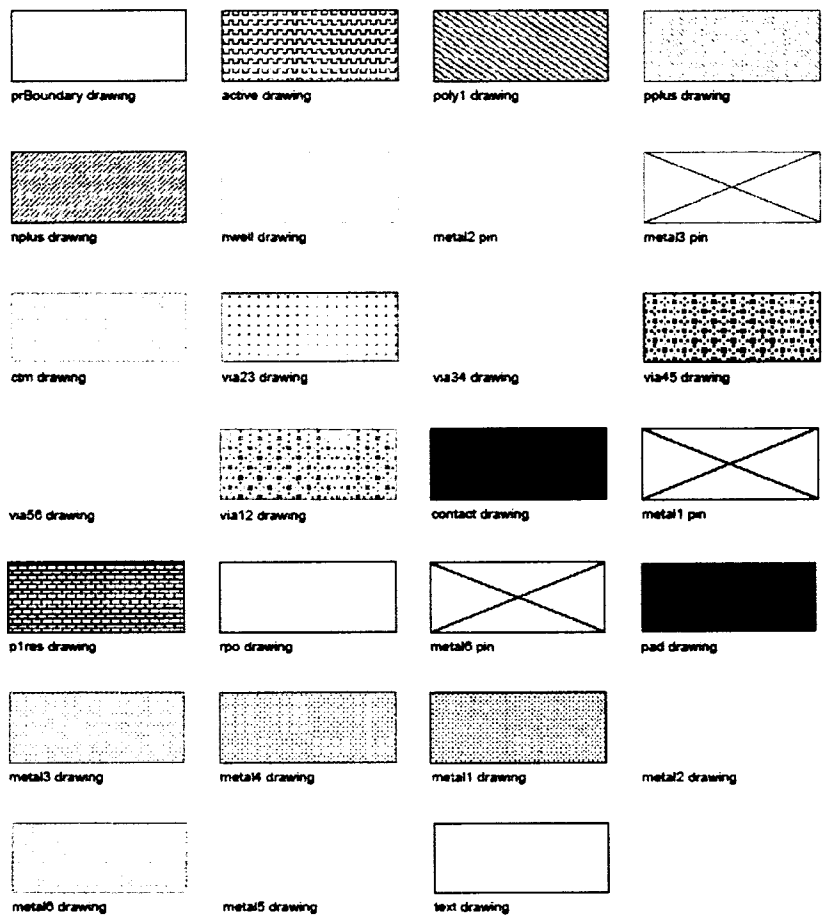

Figure B.1: The layout key showing all layers used in the whitespace detector layout.

Bibliography

[1] G. Staple and K. Werbach, "New technologies and regulatory reform will bring a bandwidth bonanza," *IEEE Spectrum*, pp. 48–52, March 2004.

[2] Federal Communications Commission (FCC), "FCC-04-113 Notice of Proposed Rule Making: In the Matter of Unlicensed Operation in the TV Broadcast Bands and Additional Spectrum for Unlicensed Devices Below 900 MHz and in the 3 GHz Band." [Online]. Available: http://hraunfoss.fcc.gov/edocs_public/attachmatch/FCC-04-113A1.pdf, 2004.

[3] Motorola, Inc., "A White Paper on the Exploitation of "Spectrum Holes" to Enhance Spectrum Efficiency." Through personal communication with Dr. Leonard MacEachern, October 2002.

[4] Federal Communications Commission (FCC), "Public Notice: C and F Block Broadband PCS Auction Closes." [Online]. Available: http://wireless.fcc.gov/auctions/35/releases/da010211.pdf, 2001.

[5] B. Aazhang, J. Lilleberg, and G. Middleton, "Spectrum sharing in a cellular system," *IEEE Eighth International Symposium on Spread Spectrum Techniques and Applications*, pp. 355–359, 2004.

[6] J. Mitola, "Cognitive radio for flexible mobile multimedia communications," *IEEE International Workshop on Mobile Multimedia Communications*, pp. 3–10, November 1999.

[7] J. Neel, R. M. Buehrer, J. H. Reed, and R. P. Gilles, "Game theoretic analysis of a network of cognitive radios," *The 2002 45th Midwest Symposium on Circuits and Systems*, vol. 3, pp. 409–412, August 2002.

[8] T. Costlow, "Cognitive radios will adapt to users," *IEEE Intelligent Systems*, vol. 18, p. 7, May-June 2003.

[9] J. Mitola, "Cognitive INFOSEC," *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 1051–1054, June 2003.

[10] S. Haykin, "Cognitive radio: Brain-empowered wireless communications," *IEEE Journal on Selected Areas in Communications*, vol. 23, pp. 201–220, February 2005.

[11] A. Thanachayanont, "CMOS transistor-only active inductor for IF/RF applications," *IEEE International Conference on Industrial Technology*, vol. 2, pp. 1209–1212, 2002.

[12] H. Kim, M. Ismail, and H. Olsson, "CMOS limiters with RSSIs for bluetooth receivers," *Midwest Symposium on Circuits and Systems*, vol. 2, pp. 812–815, August 2001.

[13] J. Norsworthy, "Broadband tuners for modern systems," *RF Design*, pp. 67–72, June 2001.

[14] J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*. Boston: Artech House, first ed., 2003.

[15] C.-C. Hsiao, C.-W. Kuo, C.-C. Ho, and Y.-J. Chan, "Improved quality-factor of 0.18-μm CMOS active inductor by a feedback resistance design," *IEEE Microwave and Wireless Components Letters*, vol. 12, pp. 467–469, December 2002.

[16] V. L. Belini and M. Romero, "Design of active inductors using CMOS technology," *15th Symposium on Integrated Circuits and Systems Design*, pp. 296–301, September 2002.

[17] Y. W. Choi and H. C. Luong, "A high-Q and wide-dynamic-range 70 MHz CMOS bandpass filter for wireless receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, pp. 433–440, May 2001.

[18] C. Leifso, J. W. Haslett, and J. G. McRory, "Monolithic tunable active inductor with independent Q control," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, pp. 1024–1029, June 2000.

[19] C. Leifso and J. W. Haslett, "A fully integrated active inductor with independent voltage tunable inductance and series-loss resistance," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 671–676, April 2001.

[20] M. Madihian, "A band selection/switching technique for multi-mode wireless front-end transceivers," *Proceedings of the 2001 SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference*, vol. 1, pp. 257–260, August 2001.

[21] A. Thanachayanont, "Low voltage CMOS fully differential active inductor and its application to RF bandpass amplifier design," *2001 International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers*, pp. 125–128, April 2001.

[22] A. Thanachayanont and A. Payne, "VHF CMOS integrated active inductor," *Electronic Letters*, vol. 32, pp. 999–1000, May 1996.

[23] Y.-H. Cho, S.-C. Hong, and Y.-S. Kwon, "A novel active inductor and its application to inductance-controlled oscillator," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, pp. 1208–1213, August 1997.

[24] A. Thanachayanont and A. Payne, "CMOS floating active inductor and its applications to bandpass filter and oscillator designs," *IEE Proceedings - Circuits, Devices and Systems*, vol. 147, pp. 42–48, February 2000.

[25] A. Pascht, J. Fischer, and M. Berroth, "A CMOS low noise amplifier at 2.4 GHz with active inductor load," *2001 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 1–5, September 2001.

[26] J.-N. Yang, Y.-C. Cheng, and C.-Y. Lee, "A design of CMOS broadband amplifier with high-Q active inductor," *The 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications*, pp. 86–89, July 2003.

[27] A. Thanachayanont, "Low voltage low power CMOS inductorless RF bandpass filter with high image rejection capability," *The 2002 45th Midwest Symposium on Circuits and Systems*, vol. 3, pp. 548–551, August 2002.

[28] Y. Wu, X. Ding, M. Ismail, and H. Olsson, "RF bandpass filter design based on CMOS active inductors," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 50, pp. 942–949, December 2003.

[29] Y. Wu, M. Ismail, and H. Olsson, "A novel CMOS fully differential inductorless RF bandpass filter," *The 2000 IEEE International Symposium on Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva*, vol. 4, pp. 149–152, May 2000.

[30] F. Dulger, E. Sanchez-Sinencio, and J. Silva-Martinez, "A 1.3-V 5-mW fully integrated tunable bandpass filter at 2.1 GHz in 0.35-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 918–928, June 2003.

[31] S. Pipilos, Y. Tsividis, J. Fenk, and Y. Papananos, "A Si 1.8 GHz RLC filter with tunable center frequency and quality factor," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1517–1525, October 1996.

[32] D. Li and Y. Tsividis, "Design techniques for automatically tuned integrated gigahertz-range active LC filters," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 967–977, August 2002.

[33] P.-C. Huang, Y.-H. Chen, and C.-K. Wang, "A 2-V 10.7-MHz CMOS limiting amplifier/RSSI," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1474–1480, October 2000.

[34] C.-P. Wu and H.-W. Tsao, "A 110 MHz 84 dB CMOS programmable gain amplifier with RSSI," *2003 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 639–642, June 2003.

[35] C.-C. Lin, K.-H. Huang, and C.-K. Wang, "A 15 mW 280 MHz 80 dB gain CMOS limiting/logarithmic amplifier with active cascode gain-enhancement," *ESSCIRC 2002. Proceedings of the 28th European Solid-State Circuit Conference*, pp. 311–314, September 2002.

[36] S. Kodali, T. Kim, and D. J. Allstor, "On-chip inductor structures: a comparative study," *ISCAS '03. Proceedings of the 2003 International Symposium on Circuits and Systems*, vol. 1, pp. I–93 – I–96, May 2003.

[37] T. Bakken and J. Choma, "Gyrator-based synthesis of active on-chip inductances," *Analog Integrated Circuits and Signal Processing*, vol. 34, pp. 171–181, March 2003.

[38] A. S. Sedra and K. C. Smith, *Microelectronic Circuits.* New York: Oxford University Press, fourth ed., 1998.

[39] Taiwan Semiconductor Manufacturing Co., Ltd (TSMC), "TSMC 0.18UM LOGIC 1P6M SALICIDE 1.8V/3.3V SPICE MODELS," *Document No. TA-10A5-6001 (T-018-LO-SP-001) Rev 1.11*, June 2002.

[40] S. Khorram, A. Rofougaran, and A. Abidi, "A CMOS limiting amplifier and signal-strength indicator," *Symposium on VLSI Circuits - Digest of Technical Papers*, pp. 95–96, June 1995.

[41] K. Manetakis and C. Toumazou, "A new high-frequency very low output-impedance CMOS buffer," *1996 IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 485–488, May 1996.

[42] Murata Manufacturing Company, "On-Board Type (DC) EMI Suppression Filters." [Online]. Available: http://www.murata.com/catalog/c31e13.pdf#page=25, 2005.

[43] National Semiconductor Corporation, "LM134/LM234/LM334 3-Terminal Adjustable Current Sources." [Online]. Available: http://cache.national.com/ds/LM/LM134.pdf, 2005.

[44] R. J. Baker, H. W. Li, and D. Boyce, *CMOS Circuit Design, Layout and Simulation.* New York: IEEE Press, 1998.