Fabrication of Long Range Surface Plasmon Polariton Bragg Waveguide Biosensors on Cytop and Multilayer Substrates

By
Howard J. Northfield

A Thesis submitted to the Faculty of Graduate and Postdoctoral Affairs in partial fulfillment of the requirements for the degree of Master of Applied Science in Electrical Engineering

18/9/2015

Ottawa-Carleton Institute for Electrical and Computer Engineering
School of Information Technology and Engineering
Carleton University
Ottawa, Ontario, Canada

Abstract

This thesis documents the micro-fabrication of a Long Range Surface Plasmon Polariton (LRSPP) biosensor device design that incorporates Bragg grating waveguides. The majority of the work involved the fine tuning of the bi-layer lithography, ultra-violet (UV) exposure and metal deposition micro-fabrication procedures. The goal was to resolve very fine features, accurately produce thin metallization and achieve a high quality metal surface. Repeatable resolution of Bragg gratings having a step-in-width from 8µm to 2µm, a 50% duty cycle and a period of 1690nm to 1800nm, was achieved with bi-layer lithography and UV exposure. A gold thickness of 35nm±5% and surface roughness of better than 2nm rms and average was achieved using thermal vacuum chamber deposition. The fabrication was performed on two different substrates; Cytop and a prefabricated Ta_2O_5/SiO_2 multilayer stack.

Acknowledgments

I would like to thank my thesis supervisors Dr. Niall Tait and Dr. Pierre Berini for the opportunity to contribute to the optical biosensor project, a fascinating introduction to the field of micro-fabrication, and for their consultation and direction. Very much appreciation extended to my project colleagues, Sa'ad Hassan who acted as a close mentor for much of the project, and Norm Fong and Wei Ru Wong for much consultation. I would like to particularly thank the staff of the Carleton micro-fabrication facilities, Angela McCormick, Rob Vandusen, and Rick Adams for their training, assistance and consultation on the fabrication techniques, and with equipment operation. Appreciation also to personnel at the University of Ottawa opto-electronic facilities, Ewa Lisicka and Anthony Olivieri, for time spent assisting with equipment usage and a special note of thanks to my wife Angela for copy editing.

Table of Contents

List of Figures

List of Tables

1.0 Introduction

1.1 Optical Biosensors

The biosensor is an integrated device that is used for the detection of an analyte, a biochemical of interest. The biosensor uses a biochemical reaction, such as antibody-antigen binding or an enzyme-substrate reaction, to immobilize the analyte onto a sensing surface for the transduction of the analyte's presence to a detectable output [1] [2]. The demand for biosensors has arisen from the nature of biochemical analyses; many involve time consuming, expensive and complicated methods performed by specialized technicians in laboratory settings. The analytical techniques often involve labelling the samples fluorescently or radioactively [3]. The development of the biosensor has introduced a direct, label-free analysis technique in a compact, robust, sensitive device, which provides accurate analysis rapidly, and is useful in a number of disciplines [1]. The direct label-free detection generally does not require pre-analysis sample preparation which reduces procedural complexity and time, and can perform real-time monitoring and routine analysis of many samples [1] [4]. Optical biosensors use optical principles for the transduction of the analyte immobilization into a detectable and measurable output. The analyte immobilization to the detection surface causes a change of the physical optical parameters of the sensing surface such as absorption, fluorescence, luminescence or refractive index. This results in a change in the characteristics of the supported light such as intensity, phase or polarization [3] [4]. There are a number of optical transduction designs including optical fibers, integrated interferometers (Mach-Zehnder Interferometers), waveguide based surface plasmon, resonant mirror, grating coupler, and bidiffractive couplers [4].

Recently there is much interest in waveguide based surface plasmon optical biosensors that functionalize a special mode derived from the surface plasmon, the long range surface plasmon polariton (LRSPP). Surface plasmons (SP) are electromagnetic surface waves with a field maximum in the surface that is exponentially evanescent perpendicular to the surface. When appropriately subject to light, the SP's couple with photons and a strong increase in the surface electromagnetic field occurs, a resonant amplification [5]. The resonant amplification is known as surface plasmon resonance (SPR). More specifically, SPR is due to the generation of charge density oscillations called surface plasmon polaritons (SPPs) at the interface of two media with dielectric constants of opposite signs, such as a metal and a dielectric. The SPP's are transverse-magnetic polarized optical waves bound to a metal-dielectric interface [6].

SPR biosensors have become one of the foremost sensor types for direct, label-free biochemical detection. The application principle is a refractive index change due to the analyte contact with the metal surface of the sensor [7]. The propagation constant of the SPP is extremely sensitive to changes in the refractive index of the dielectric medium and this is the fundamental detection principle of the SPR biosensor [8] [9]. Effectively the characteristics of the evanescent SPP wave are altered as it propagates along the waveguide and probes the medium, the analyte, in contact with the metal. [10]. A special SP mode is the LRSPP which can be generated with a particular waveguide configuration, discussed in detail later in the chapter. The field of the LRSPP has been shown to be an order of magnitude larger than that of SPs, offering deeper penetration into the analyte. The LRSPP also shows less attenuation loss hence longer propagation along the waveguide offering greater sensitivity. The characteristics of the LRSPP therefore are considered to result in improved detection performance over sensors that employ the SP [11].

The plasmon polariton Bragg grating (PPBG) waveguide that supports the LRSPP mode offers benefits over other LRSPP waveguide designs. The resolution of an SPR sensor depends upon the accuracy to which the position of the resonance can be determined [7]. The Bragg grating wavelength, effectively the waveguide "resonance", is defined by the design of the grating and is well known. A shift from the Bragg wavelength, due to a refractive index change, can therefore be well recognized. The LRSPP of the PPBG is optimally excited by a TM-polarized optical beam via end-fire coupling. In this arrangement the beam is focused onto the end of the metal waveguide (the facet). End-fire coupling can be efficient and can be easier to implement than other excitation methods (such as prism coupling [10] [11]). However, it does require access to high-quality end facets, which can be difficult or inconvenient to create in some structures [12].

The benefits of the PPBG LRSPP waveguide over other SPR waveguide configurations have motivated the pursuit of biosensor architecture with LRSPP supporting, PPBG waveguides. This project involves the fabrication of LRSPP optical biosensor devices that incorporate Bragg grating waveguides designed for operation in the short-wavelength-infrared (SWIR, 900nm to 1700nm), specifically for Bragg wavelengths (λ_B) from 1260nm to 1600nm.

1.1.1 Long Range Surface Plasmon Polaritons Optical Biosensors

Surface plasmon polaritons (SPPs) are transverse magnetic (TM) optical surface waves that propagate along the interface of a metal and dielectric. SPPs are very sensitive to surface properties making them of interest in biochemical sensing but are characterized by high attenuation. Long Range SPPs (LRSPPs) have an attenuation of 2 to 10 times less than SPPs and can be supported by certain metal-dielectric configurations [12]. The optical biosensing waveguide design, fabricated in this project, supports a particular LRSPP and evolves from a series of variations of metal-dielectric configurations.

1.1.1.1 Surface Plasmon Polaritons (SPP): The Single Metal-Dielectric Interface

Surface polaritons are the result of the coupling of electromagnetic radiation to surface dipole excitations which propagate as a wave along the interface between two media. A surface plasmon polariton occurs at the interface between a dielectric and an electron plasma, where, if a metal is subject to infrared wavelengths it behaves nearly like a plasma of free electrons [13]. The single interface configuration, illustrated in Figure 1, supports only one bound (nonradiative) mode. A surface electromagnetic mode is generally defined as a particular electromagnetic wave that is supported at the interface between two media [14] [15]. This SPP is transverse magnetic (TM), that is $E_X=H_Y=H_Z=0$. The SPP amplitude is a maximum at the interface and decays away exponentially as it extends into each medium [14] [12]. Figure 1 shows in red the distribution of the main transverse (to propagation) electric field component E_Y of the single SPP mode. The propagation of the SPP is in the positive z direction out of the page. This configuration has high propagation attenuation limiting its use for application [12].

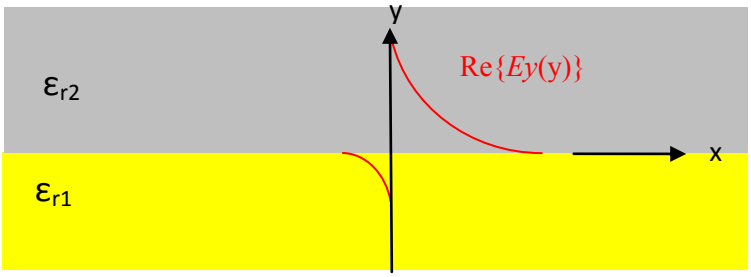


Figure 1: Single Metal Dielectric Interface

A cross-section of an infinite metal slab overlain by an infinite, homogenous, dielectric. The metal is of permittivity ε_{r1} and the dielectric of permittivity ε_{r2}. The Ey field distribution of the only supported SPP is shown in red. The propagation direction (z) is out of the page. Figure adapted from [12].

1.1.1.2 Long Range Surface Plasmon Polaritons (LRSPP): The Symmetric Metal Slab and the s_b Mode

The metal slab configuration, illustrated in Figure 2, is of a metal of finite thickness, infinite width and infinite length bound above and below by infinite dielectric. It is referred to as a symmetric metal slab configuration if the upper and lower bounding dielectrics are of the same permittivity value. As the thickness of the metal of the single interface of Figure 1 is reduced to "thin", the SPP's of the single interface couple, resulting in two bound TM supermodes. The two modes are referred to as asymmetric bound (a_b), and symmetric bound (s_b), indicating the variation of the main transverse electric field component (E_y) across the structure. The a_b mode has greater surface sensitivity but very high attenuation. The s_b mode is has a stronger field and longer propagation characteristics and is the LRSPP mode of the thin metal slab. The symmetric dielectric permittivity of the structure is not a physically mandatory requirement for the coupled modes but, with the symmetry, the s_b mode remains nonradiative (purely bound) for thickness approaching zero. For asymmetric permittivities, the s_b mode

remains bound only to a cut-off thickness. This configuration also exhibits propagation attenuation as with the single interface. Roughness of the metal-dielectric interface adds to the propagation attenuation [12].

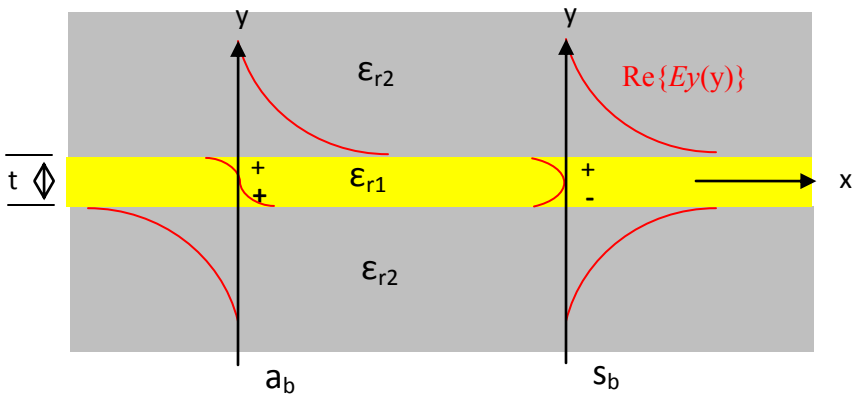


Figure 2: Symmetric Metal Slab
A cross-section of a metal slab of finite thickness, infinite width and infinite length. The metal is of permittivity ε_{r1} overlain and underlain by an infinite, homogenous, dielectric of permittivity ε_{r2}. The E_Y field distribution of the two bound SPP's is shown in red. The propagation direction (z) is out of the page. Figure adapted from [12].

1.1.1.3 Long Range Surface Plasmon Polaritons (LRSPP): The Metal Stripe and the ss_b^0 Mode

If the symmetric metal slab configuration is changed to having a metal limited in width, as shown in Figure 3, it gives two-dimensional confinement and a different mode spectrum. If the metal is reduced to a dimension of w/t>>1, the configuration is that of a metal stripe. At this dimension four fundamental bound (nonradiative) modes result from the SPP coupling. The four bound fundamental modes supported by the metal stripe are referred to as aa_b^0, as_b^0, sa_b^0, and ss_b^0. The nomenclature used here is an extension to that of the slab; the letters respectively represent the symmetry with the confined electric field components E_y and E_x, the subscript indicates if bound

(nonradiative) or leaky, and the superscript is the order of the mode [16]. With the metal stripe, as with the metal slab, the E_y field component dominates for all modes. But, with the finite width of the structure, higher-order modes can also be supported. So unlike the symmetric metal slab all field components are always nonzero so the modes are not purely TM but TM in character [12]. Of particular interest is the ss_b^0 mode. The ss_b^0 mode in the thin symmetric metal stripe is the fundamental long-range mode and, following convention, is termed a LRSPP [12]. The ss_b^0 mode:

- Has a Gaussian-like field distribution in the plane transverse to the direction of propagation, making end-fire excitation particularly easy and efficient [12] [16].
- Has high surface sensitivity [17].
- Has reduced attenuation with reduced metal thickness [12]. Mode power attenuation (MPA) of around 5.5dB/mm for LRSPP's at 1310nm have been measured for metal stripe waveguides nominally 35nm thick and 5μm in width [18].
- Becomes less bound (leaky), with reduced metal thickness [16]. An unfavourable characteristic due to a reduction in surface sensitivity.
- As with the slab waveguide, has increased attenuation with increased surface roughness [12].

The metal stripe LRSPP characteristics therefore:

- Allows for longer waveguides and greater device sensitivity [12].
- Constrain the metal stripe design with a trade-off between the degree of attenuation and confinement of the LRSPP [12].
- Require close attention to the tolerance of the metal thickness and the quality of the metal surface roughness during fabrication.

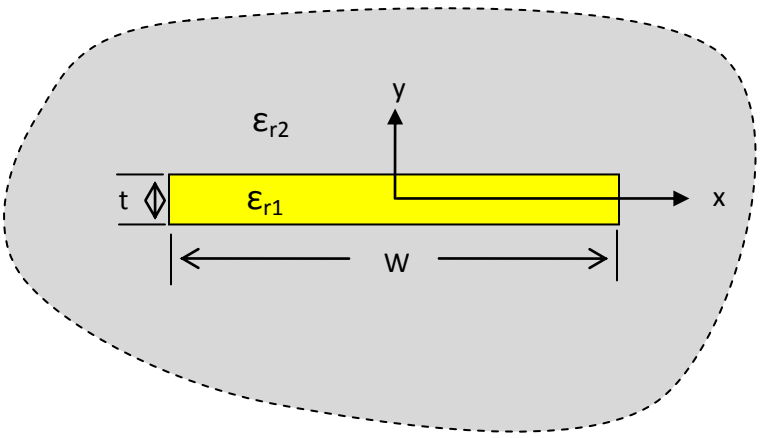


Figure 3: Thin Finite Width Metal Wave Guide
A cross-section of a metal slab of finite thickness, finite width and infinite length in the propagation direction (z) out of the page. The metal is of permittivity ε_{r1} surrounded by an infinite, homogenous, dielectric of permittivity ε_{r2}. Figure adapted from [12].

1.1.2 Bragg Grating LRSPP Biosensors

The optical biosensors in this project adopt the metal stripe model of the waveguide configurations and thereby support the ss_b^0 mode LRSPP. Gold is used as the material for the metal stripe for fabrication reasons, chemical characteristics, and biological compatibility [18]. The LRSPP biosensors here are very similar in architecture to the LRSPP biosensor devices previously studied by [18] [19] [20], the main difference is the presence of step-in-width patterned metal stripe plasmon polariton Bragg grating (PPBG) waveguides, hereafter referred to as PPBG waveguides. The PPBG is illustrated in Figure 4. Table 1 presents the values of the PPBG dimensions indicated in Figure 4. The columns of Table 1 are in the order of the waveguide layout on the Bragg biosensor devices fabricated in this project. The range of the parameters listed in Table 1 define a range of PPGS's with operating Bragg wavelengths (λ_B) centred, in increments of 10 nm, around 1310 nm for the C5 devices and 1550 nm for the C8 devices.

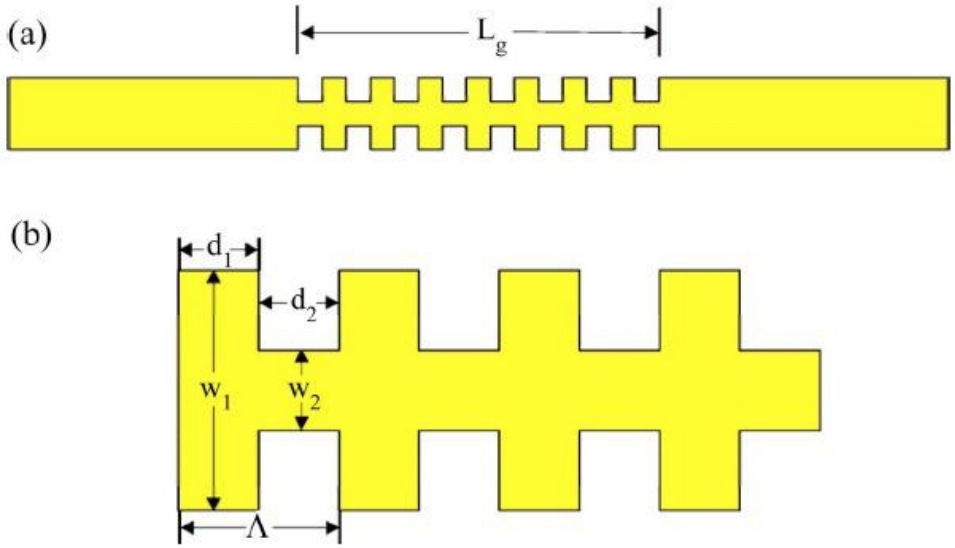


Figure 4: The Step-in-Width Bragg Grating Metal Stripe

a) Plan view a metal stripe with a step-in-width Bragg grating segment of length L_g

b) Plan view of a step-in-width Bragg grating with dimensional annotation. The period Λ is equal to $d_1 + d_2$. Illustration from [21].

Table 1 Dimensions of C5W2_1310 and C8W2_1550 Bragg grating metal stripes

	WAVEGUIDE POSITION ON A DEVICE																				
	Cladded			**Etched**															**Cladded**		
	1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*	*16*	*17*	*18*	*19*	*20*	*21*
DEVICE NAME	**C5W$_2$_1310** $W_1 = 5$ (um), $W_2 = 2,3,4$ (um)																				
λ_B	1260	1380	SW	1270	1290	1330	1350	1370	SW	1260	1310	1380	SW	1360	1340	1320	1300	1280	SW	1310	SW
Λ (nm)	1420	1550		1430	1450	1500	1520	1540		1420	1470	1550		1530	1510	1490	1460	1440		1470	
d_1, d_2 (nm)	710	775		715	725	750	760	770		710	735	775		765	755	745	730	720		735	
DEVICE NAME	**C8W$_2$_1550** $W_1 = 8$ (um), $W_2 = 2,3,4,5$ (um)																				
λ_B	1500	1600	SW	1510	1530	SW	1570	1590	SW	1500	1550	1600	SW	1580	1560	SW	1540	1520	SW	1550	SW
Λ (nm)	1690	1800		1700	1720		1770	1790		1690	1750	1800		1780	1760		1730	1710		1750	
d_1, d_2 (nm)	845	900		850	860		885	895		845	875	900		890	880		865	855		875	
L_g (mm) varies with waveguide to give a certain number of grating periods. L_g for the 1310 waveguide of the C5W$_2$_1310 devices ($W_2 = 2,3,4$): C52 = 1.2, C53 = 1.5, C54 = 2.1 L_g for the 1550 waveguide of the C8W$_2$_1550 devices ($W_2 = 2,3,4,5$): C82 = 1.4, C83 = 1.74, C84 = 1.74, C85 = 2.0																					
λ_B = Bragg wavelength, SW = Straight Waveguide (no Bragg gratings)																					

The PPBG performs as a distributed Bragg stack reflector. When an electromagnetic stimulus is applied at one end (the input) of the PPBG waveguide, in the direction of the length of the waveguide, reflections occur at each grating period. For wavelengths near the Bragg wavelength (λ_B), constructive interference occurs to give a reflection at the input. Other wavelengths are transmitted to the opposite end (the output) of the waveguide. Figure 5 shows an example of a reflectance spectrum at the input of a PPBG waveguide. See Figure 6 for an example of a transmittance spectrum at the output of a PPBG waveguide.

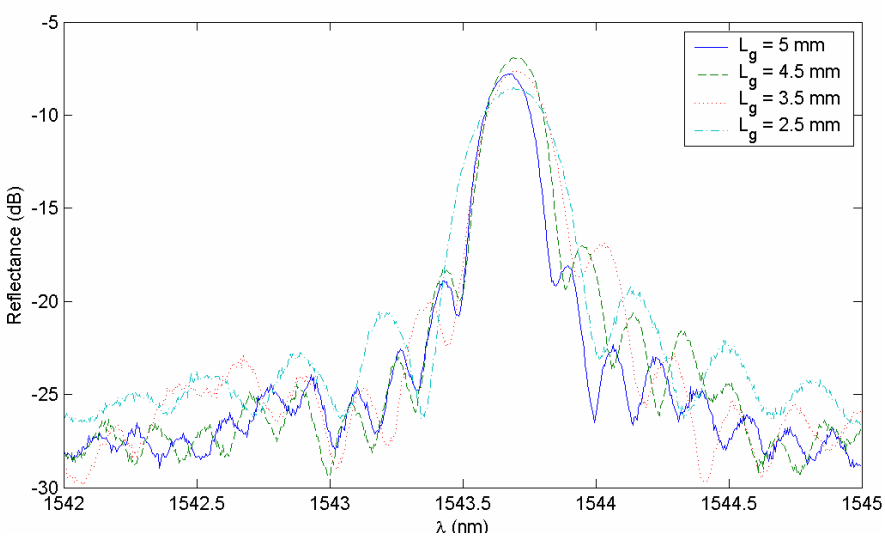


Figure 5: Reflectance Spectrum

Reflectance spectrum measured from a C83 step-in-width Bragg grating waveguide. From [21].

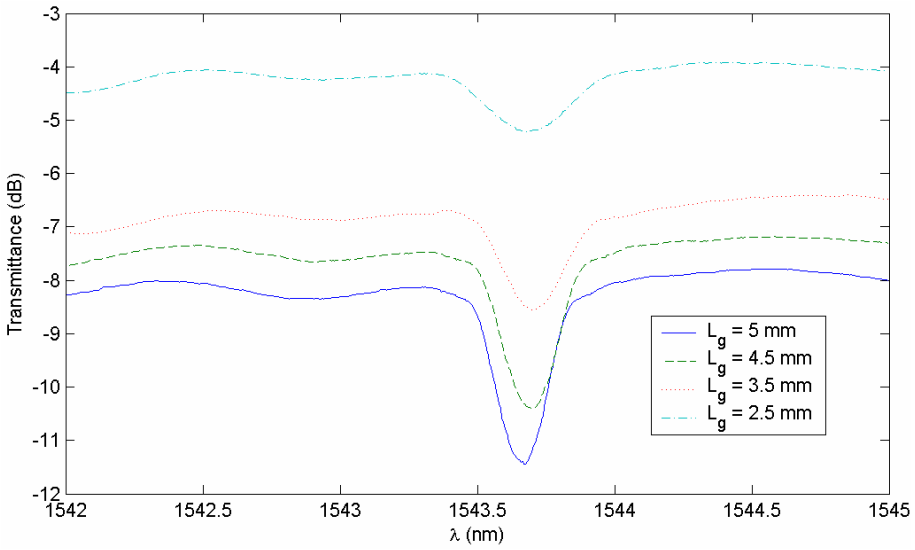


Figure 6: Transmittance Spectrum

Transmittance spectrum measured from a C83 step-in-width Bragg grating waveguide. From [21].

1.3 Device Operation & Structure

1.3.1 Device Operation

The optical biosensor devices involved in this thesis function with an arrangement of reference and sensing optical waveguides that operate in the infrared electromagnetic spectrum. Refer to Figure 7 for a close representation of the optical biosensor device. The reference waveguide is protected from the biochemical material of interest, either by being covered (clad) with the upper dielectric, or post fabrication is treated with a blocking chemical so that the biochemical material of interest, the target analyte, does not adhere to it. The sensing PPBG metal stripe is exposed in a channel, illustrated in Figure 8, and post fabrication is chemically prepared to attract the analyte. The preparation of the waveguide involves first the application of a self-assembled monolayer (SAM) that binds to the gold waveguide surface and acts as a facilitator for subsequent functionalization. To the SAM is then applied a target specific receptor that functionalizes the surface to attract (if present in the test fluid) the analyte of interest to the waveguide [18]. The adhering of target analyte to the waveguide causes a change in the refractive index [4] [10] [11], in general a complex parameter (ñ). A change in refractive index translates to a change in the propagation constant of the LRSPPs supported by the waveguide [4] [17] since:

- The relative permittivity of the waveguide is a function of refractive index, by the relation $\varepsilon_r = \tilde{n}^2 = (n - jk)^2$, where n is the real part of the refractive index, and k is the extinction coefficient [12] [22].
- The normalized attenuation constant (α/β_o) and the normalized phase constant (β/β_o) are a function of the relative permittivity of the waveguide [17]. Here $\beta_o = 2\pi/\lambda_o = \omega/c_o$ is the phase constant of plane waves in free space, λ_o is the wavelength in free space, and c_o is the speed of light in free space [12].
- The normalized propagation constant is composed of the normalized attenuation constant and the normalized phase constant as $\gamma_e = \alpha/\beta_o + j\,\beta/\beta_o$ [12].
- As a note, the normalized attenuation constant and the normalized phase constant together define the dispersion characteristics of a supported mode of the waveguide.

With a change in the refractive index due to the presence of the target analyte, the PPBG biosensor, as a transducer, generates a detectable output. The reference and sensing PPBG waveguides are subject to the same LRSPP generating optical stimulus, such as a TM-polarized optical beam via end-fire coupling [12]. If the target analyte has adhered to the sensing PPBG waveguide a change in the transmittance characteristics is measured with respect to the reference PPBG waveguide, most notably a shift in the Bragg wavelength λ_B and also but less pronounced a change in the dip of the transmittance spectrum.[17].

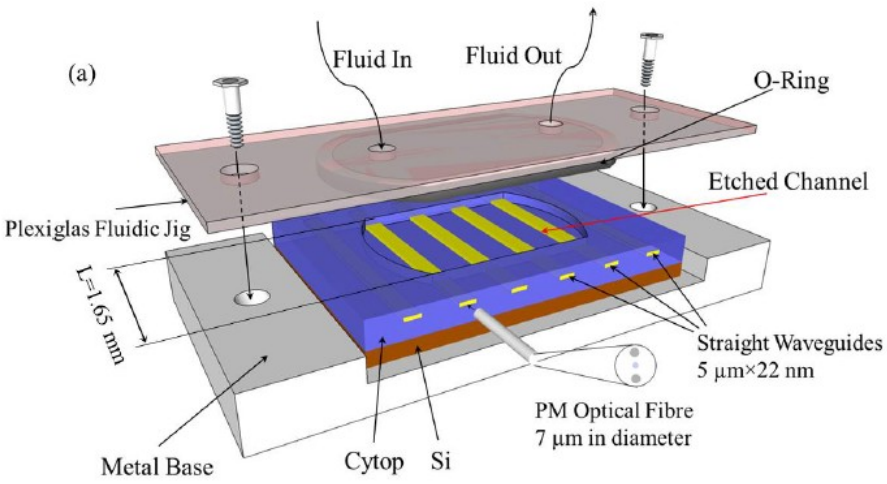


Figure 7: Optical Biosensing Device Example

LRSPP sensing waveguides shown in etched channels for exposure to the fluid test analyte. Reference waveguides are embedded in the Cytop cladding. Illustration from [23].

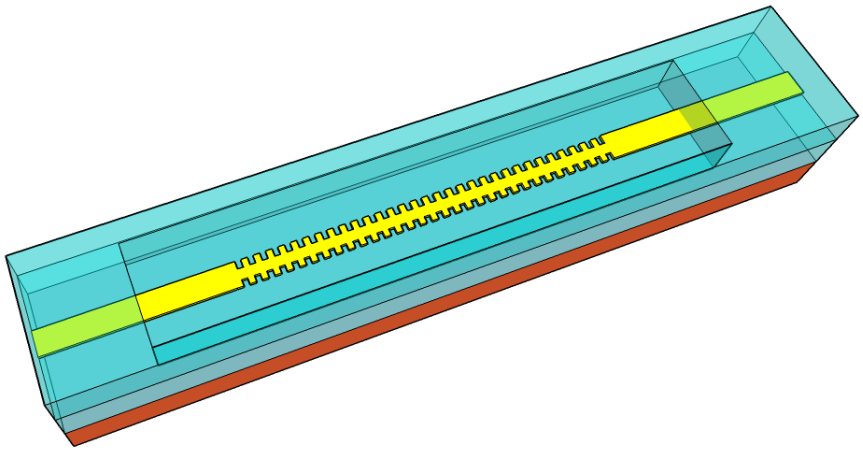


Figure 8: An Exposed PPBG Waveguide.
Illustration from [17].

1.3.2 Device Structure

Fabricated in this project were two variations of the same optical LRSPP biosensor design incorporating the same metal stripe waveguides but with a different composition of surrounding material.

1.3.2.1 Waveguides on Cytop

Figure 9 illustrates the cross-section of a portion of the “full Cytop” biosensor device as fabricated in this project. The full Cytop biosensor device has the lower and upper cladding around the metal stripe waveguide composed of Cytop. That is, the dielectric surrounding the metal stripe has the same relative permittivity, the ideal condition for the transmission of metal stripe bound LSRPPs [24]. Cytop is the trade name of a commercially available amorphous perfluoropolymer. Cytop is produced by and is a

registered trademark of Asahi Glass Corporation (AGC), AGC Chemicals Fluoroproducts Division, Tokyo, Japan. One of the main reasons for the selection of Cytop as the metal stripe cladding is that it has a refractive index (n) of 1.3348 at 1300nm, very close to that of water [17] [25]. Additionally it is resistant to water, oil and many chemicals (such as those use in fabrication lithography) and can be applied by spin coating. More details of 2 variations of Cytop used are included in Chapter 2. The operational biosensing procedure involves the filling of the fluidic channels of the sensing waveguides with a water based solution containing the target analyte. With the refractive index of Cytop being almost that of water, this provides the effect that the surrounding background of the sensing waveguide is nearly optically the same as that of the reference waveguide. Once the sensing channels are filled with test solution, the waveguides are subject to the LRSPP generating optical stimulus. The character of the resulting optical response indicates if the biomaterial of interest is present in the test solution.

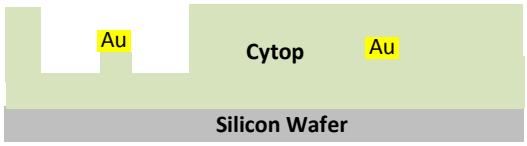


Figure 9: Full Cytop LRSPP Biosensor
A cross-section of a portion of the "full Cytop" biosensor. The waveguides are underlain by a cladding of Cytop. The waveguide overlain by Cytop is the reference waveguide. The exposed waveguide, on a pedestal of Cytop in an etched channel, is the sensing waveguide. Not drawn to scale.

1.3.2.2 Waveguides on Ta_2O_5/SiO_2 Multilayer Stack Substrate

The fabrication of devices with metal stripe waveguides on Cytop presents some process complexities, discussed in detail in Chapter 2. The substitution of the lower Cytop cladding by a rigid, multilayer stack, of alternating Ta_2O_5 and SiO_2 layers, is to alleviate the various fabrication difficulties; discussed in detail in Chapter 3. The biosensing functionality of the multilayer stack device is exactly the same as that of the full Cytop device. Figure 10 illustrates the cross-section of a portion of the multilayer stack biosensor device. Figure 11 is a detailed cross-section of the Ta_2O_5/SiO_2 multilayer stack.

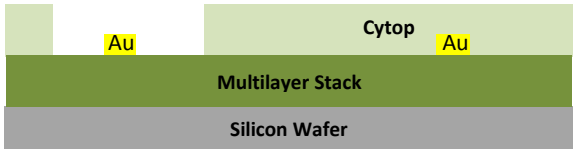


Figure 10: Multilayer Stack Cytop LRSPP Biosensor

A cross-section of the multilayer stack biosensor. The waveguides are underlain by the Ta_2O_5/SiO_2 multilayer stack. The waveguide overlain by Cytop is the reference waveguide. The exposed waveguide, in an etched channel, is the sensing waveguide. Not drawn to scale.

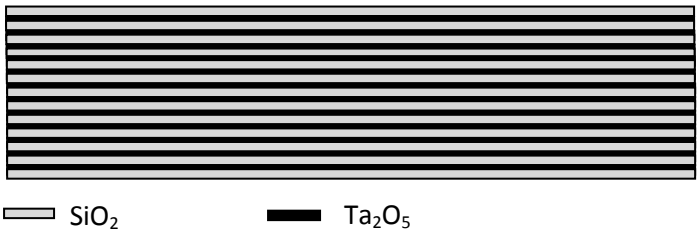


Figure 11: The Multilayer Stack

A cross-section of the multilayer stack. The multilayer stack consists of a top layer of SiO_2 (optical thickness 668.514nm) underlain by 12 alternating layers of Ta_2O_5 (optical thickness of 432.421nm) and SiO_2 (optical thickness of 904.375nm). Not drawn to scale.

The concept of a distributed multilayer stack below a metal stripe to support LRSPPs was studied by [26] and very recently by [27]. In these studies the multilayer is referred to as a 1D, or finite, photonic crystal (PC). To support the propagation of the LRSPP, the multilayer must simulate a uniform substrate with a dielectric constant equal to that of the cladding, or at least nearly so [27]. The thickness and dielectric constant of the individual layers of the multilayer are chosen to provide a stop band of a desired bandwidth, at a desired centre wavelength (CWL). The choice of layer parameters effectively tunes the in-plane wave vector such that the evanescent field of the LSRPP in the multilayer is similar in decay to that in the upper cladding, see Figure 12. Additionally, in-plane phase matching is accomplished through the choice of thickness of the upper SiO_2 layer [personal communication with Berini].

The multilayer wafer used in this project, comprised of a multilayer stack on a silicon substrate, was prepared externally by Iridian Spectral Technologies, Ottawa. The multilayer stack was designed to produce a normal incidence stop band notch with a mean centre wavelength (@-3dB) of 1340 nm and a bandwidth of 156 nm. The requested fabrication specifications of the multilayer stack were:

- A top layer of SiO_2 (668.514 nm optical thickness)
- 12 alternating layers of SiO_2 (904.375 nm optical thickness) and Ta_2O_5 (432.421 nm optical thickness.)
- A centre wavelength (CWL): 1340 (+10/-10) nm
- Bandwidth @ -3dB: 156 (+5/-5 nm)

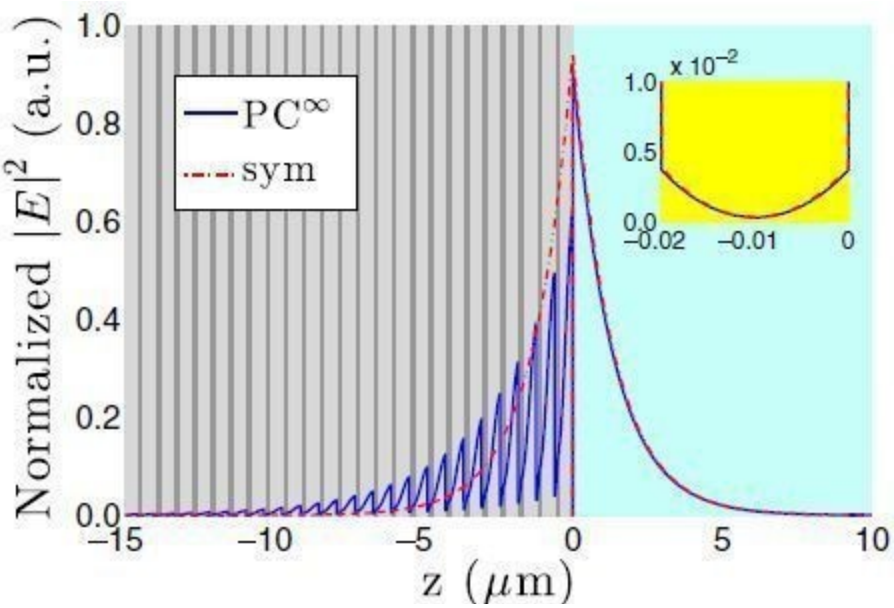


Figure 12: Electric Field in a Multilayer Structure

Normalized electric field intensity profile of the resonant mode of the photonic crystal (PC)-based structure (solid blue line) and the LRSP mode of the symmetric structure (dash-dotted red line). Inset: the zoomed intensity profile in gold. The z axis is normal to the plane of the structure, and the (top) gold-water interface is at z = 0. Illustration and caption text from [27]

1.4 Thesis Objectives & Structure

The thesis objective was to refine an existing optical biosensor fabrication process to produce a device that incorporates LRSPP PPBG waveguides. Some of the features on the LRSPP PPBG design are very small and push the limits of the fabrication methods used, methods that are desired to realized time and cost savings over other fabrication options. Provided is a detailed presentation of the fabrication process. Included is discussion and analysis of the various changes and refinements made to the previous biosensor fabrication processes. Also given is a detailed description of the subtleties in the various fabrication stages required to realize the very fine detail. Chapter 2 describes the fabrication of the full Cytop devices. Chapter 3 details the fabrication of the devices incorporating the multilayer stack lower layer. Chapter 4 presents conclusions and suggestions for future work. The appendices include a tabular summary of the full fabrication process for both the full Cytop and multilayer devices.

2.0 Fabrication of Bragg Waveguides on Cytop

With repeatable success, the micro-fabrication of appropriately dimensioned C82, step-in-width Bragg grating waveguides on Cytop, was achieved in this project. The dimensions of the Bragg gratings, refer to Figure 4 and Table 1, were near the limits of what the fabrication techniques used could successfully accomplish. The determination of the appropriate process parameters was through a refinement of existing procedures that were identified and documented by [28] [29] [30]. The previous fabrication procedures, as documented, were found not to acceptably resolve the required Bragg grating dimensions.

The individual stages in the fabrication of a Cytop based, LRSPP biosensor device, are illustrated in Figure 13 and Figure 14. The stages are discussed in detail in the following sections of the chapter. The procedural discussions are focussed on the fabrication of PPBG waveguide based biosensors using the mask labelled as “Bragg Gratings”, but is also applicable to the waveguide patterns on the masks labelled as “Biosensor”, and “New Biosensor 2014”. The discussions briefly mention the fabrication background of the individual stages, with a deeper analysis of the failures and successes and the reasoning for the sequence of changes in the fabrication steps, taken in the pursuit and accomplishment of acceptable final results.

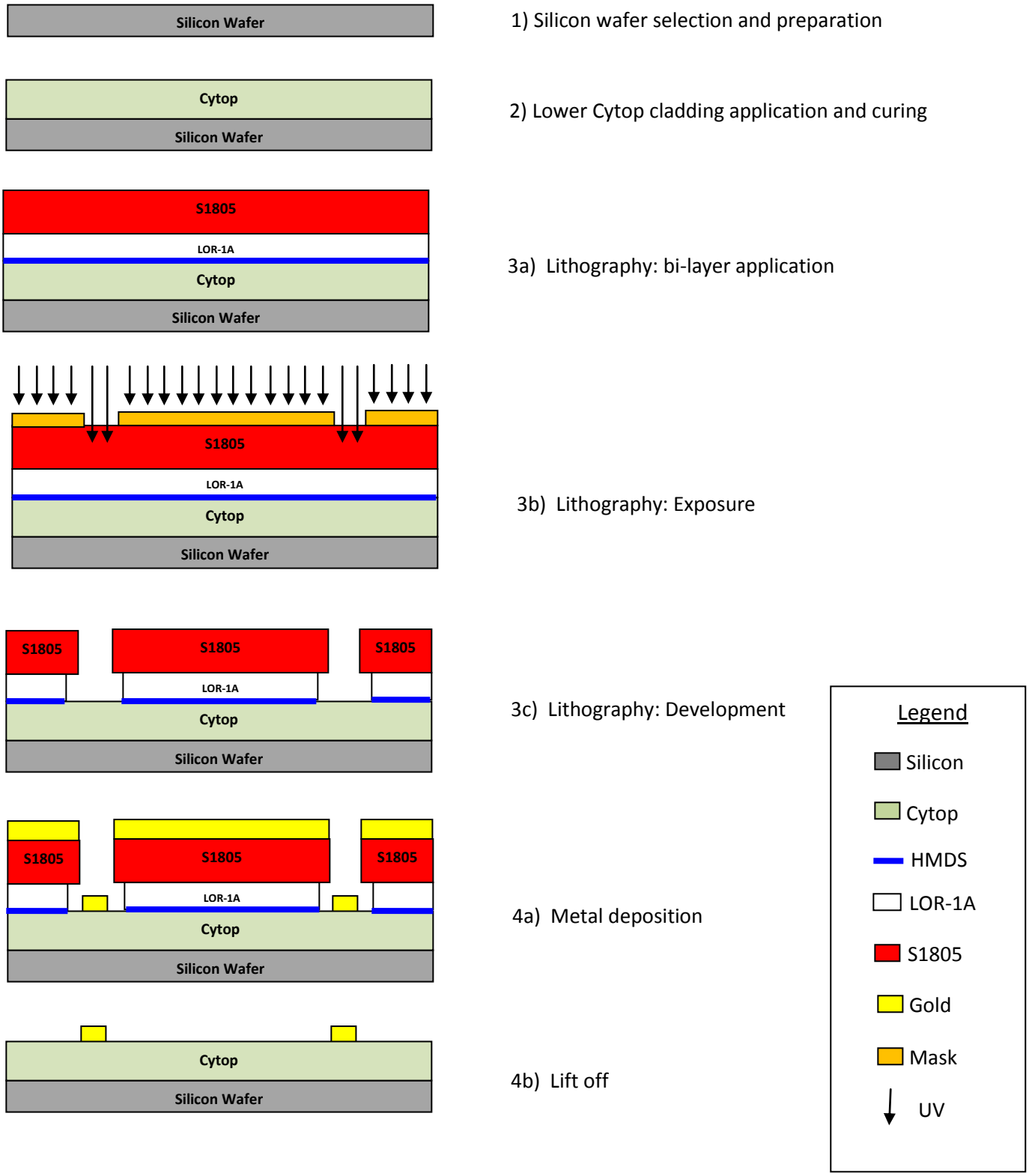
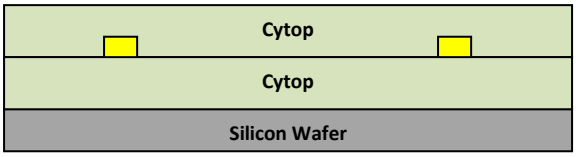
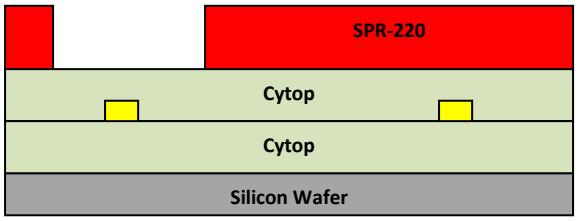


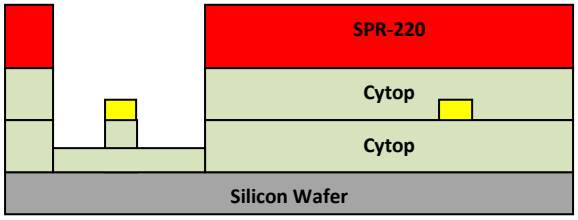
Figure 13: Full Cytop LRSPP Biosensor Device Fabrication Process



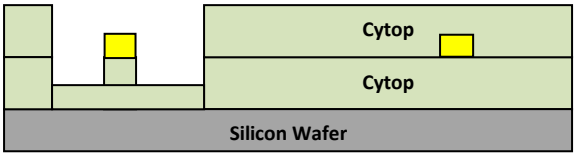
5) Upper Cytop cladding application and curing



6) Channel etch mask: photoresist application, exposure and development



7) Channel cavity etching



8) Etch mask removal; End of Fabrication

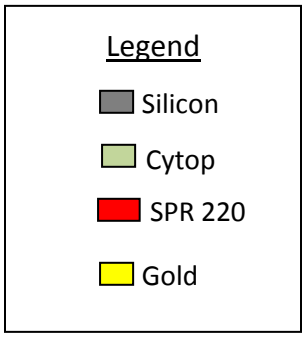


Figure 14: Full Cytop LRSPP Biosensor Device Fabrication Process continued

2.1 Fabrication of Bragg Waveguides on Cytop Details

2.1.1 Silicon Wafer Substrate Selection and Preparation

The silicon wafer selection and preparation was entirely adopted from the previous work of [28] [30] and [31].

2.1.1.1 Silicon Wafer Selection

The purpose of the silicon wafer used in the fabrication was as a structural base to support the final structure. No doping or etching of the actual silicon was performed. As such, whether the wafer was p-type or n-type was not expected to affect the quality or performance of the final product. The important criterion was the physical integrity of the wafer; good surface quality and flat. To ensure good surface quality and flatness, recycled wafers were not used for product samples, and only selectively for test samples. Note that “product sample” here refers to a 4-inch wafer subject to the complete fabrication process, intended for dicing and functional characterization. Optimally a wafer of the <100> crystallographic orientation was preferred as it facilitates crystallographic alignment with the waveguide mask and lends to cleaner device edges from the dicing process. The lithographic waveguide mask pattern was four inches in diameter, as such, four inch wafers were used for product samples. Two inch wafers were typically used for the investigation of particular process steps. This reduced consumption of materials such as Cytop and photoresist, which are quite expensive. To help confirm results, multiple wafers, four 2-inch or two 4-inch, were always processed concurrently. Fabrication of multiple wafers in this quantity had negligible impact on the time requirement.

2.1.1.2 Silicon Wafer Preparation

Preparing the chosen silicon wafer for use involves labelling and surface cleaning.

Silicon wafer labelling simply involves scribing the backside of the chosen wafer with a tracking reference number. This was performed with a diamond tipped scribing tool. Care was taken here to minimize the pressure used to label the wafer so not to break it, yet thorough enough that it was legible. The label was typically placed above the bottom flat of the wafer.

Hydrofluoric acid cleaning or "HF dip" was performed as the first of two surface preparation steps. The purpose of the HF dip was to remove any native oxide that has grown on the wafer, remove any inorganic contaminants, and additionally it was determined, through atomic force microscopy (AFM), to smooth the wafer surface. A solution of 10% HF was used. The wafer was immersed until completely hydrophobic; i.e. the HF solution does not adhere to the surface of the wafer. To achieve a hydrophobic condition, 50 seconds in the HF solution was usually sufficient. After the HF dip, the wafer was immersed and rinsed in de-ionized (DI) water for approximately 2 minutes then dried with compressed Nitrogen.

The second and last activity of the wafer preparation was an oxygen plasma cleaning or plasma preening. This was performed with a Plasma Preen II-862 plasma etching system. The purpose of this activity was to remove any substances that may be present on the wafer not removed by the HF cleaning, such as organic or polymeric material. A sequence of 5 minutes etching, 5 minutes off for cooling, and another 5 minutes etching was performed using the system with the standard (oxygen) settings of; power at 750 watts, oxygen flow of 300 sccm and pressure of 5 mTorr.

The sequence of performing the HF prior to the plasma preening was adopted from the previous projects. Alternatively, performing the plasma preening prior to the HF dip is probably a more effective order. This would remove organics prior to the HF dip that may inhibit a complete HF cleaning and leave less SiO_2 on the silicon surface prior to the next procedure.

2.1.2 Lower Cytop Cladding Application and Baking

The lower Cytop cladding preparation was adapted with modest modification from the previous work of [28] [30] [31].

2.1.2.1 First Lower Cladding Layer

The first Cytop layer, applied directly on the Silicon wafer, was of M-grade Cytop diluted to 5% weight Cytop with CT SOLV 180. M-grade CYTOP (CTL-809M) contains silane groups (SiH_4) that act as an adhesion promoter to Silicon and other inorganic material [32]. This was a thin layer of approximately 400nm for adhesion [28].

- Spin: 10 seconds@500 rpm + 20 seconds@1000 rpm
- Baking: 30 minutes @ 50°C

2.1.2.2 Second to Fourth Lower Cladding Layer

The second, third and fourth Cytop layers, are of undiluted S-grade Cytop (at 9% weight Cytop). S-grade CYTOP (CTX-809SP2) for the bulk of the Cytop cladding. S-grade Cytop does not contain silane groups (which binds with water) and makes it more resilient to degradation from water exposure [32]. Each spin achieves layer of approximately 2.3µm in thickness [28].

- Spin: 10 seconds@1000 rpm + 20 seconds@1500 rpm
- Baking (layer 2 and 3): 30 minutes @ 50°C
- Baking (layer 4): 50°C to 200°C @ 10°C/hr for minimum 18hrs (this is explained in more detail in Section 2.1.2.3)

2.1.2.3 Edge Bead Removal

An edge bead removal (EBR) procedure was introduced after the fourth layer (third S-grade), prior to the last lower clad layer. An edge bead is a build-up of the spun on material at the edge of the wafer. The edge bead can be 10–30 times thicker than the applied film in the central regions of the wafer [33]. The edge bead can compromise the overall thickness and uniformity of the spun films. Other stages in the fabrication process can be affected such as during contact exposure where the edge bead topography can cause poor contact with the mask.

Edge bead removal can be performed by mechanical scraping, chemical dissolving or etching. The EBR procedure chosen was a Reactive Ion Etch (RIE) in the March Systems Jupiter II plasma etcher with a 90mm diameter stainless steel (EBR mask) plate centered on the wafer. Edge bead removal etching parameters and settings used are listed in Table 2.

Table 2 Cytop Edge Bead Removal and March RIE System Parameters

Cytop Edge Bead Removal - March RIE System Parameters **Only performed on 4 inch wafers**	
Action	**Details**
Etch Time	10 minutes for 4 inch wafer
Power	200 Watts
Oxygen Flow	220 - 225 sccm
Oxygen Pressure	350 - 450 mTorr

Heat is generated during etching. The base plate in the March RIE after a 10 minute, 200W etch, was found to be as high as 60°C. When the EBR procedure was performed after a soft baking of the fourth lower cladding layer, the EBR mask was found to stick slightly to the Cytop on the wafer and a less complete etch of the wafer perimeter was observed. With a slow ramp hard baking of the wafer prior to the EBR procedure no sticking to the mask was observed and a more complete perimeter etching was realized; attributed to harder Cytop (less solvent present). This long slow hard bake does add an extra day to the fabrication process but has the additional benefit of an intermediate baking for improved Cytop cladding quality. With the hardened Cytop cladding, 10 minutes at 200 watt power was found to cleanly etch away the perimeter Cytop down to the wafer surface, and the EBR plate did not stick to the Cytop cladding on the wafer. If multiple edge bead removal runs were to be performed a 10 minute cooling period between runs was included.

The edge bead mask can be displaced from the center of the wafer during the etching process; blown by the pressure of the oxygen flowing in. To test that the mask would remain centered, a short, 30 second run at 200 watts was performed to ensure the mask was pressed securely enough, and that the wafer did not move. If the mask continued to slip while the wafer was located in the center of the etch chamber, moving the wafer to the 10 o'clock location in the chamber found that the mask would stay in place; this location was least in-line with the oxygen in-flow port.

2.1.2.4 Last Lower Cladding Layer

The last (fifth) Cytop layer applied to finish the lower cladding was of M-grade Cytop diluted to 5% weight Cytop with CT SOLV 180. M-Grade was used here to provide improved adhesion for the metallization to be applied in the next stage of the fabrication. Diluted M-grade was to produce a smoother surface. This was a layer of approximately 0.8µm in thickness [28].

- Spin: 20 seconds@1000 rpm
- Baking: (30 min @ 50°C) + (50°C to 200°C @ 150°C/hr) + (2.5+ hrs @ 200°C)
- or Baking: 50°C to 200°C @ 10°C/hr for minimum 18hrs

2.1.2.5 Lower Cytop Cladding Application and Baking Summary

Table 3 summarizes the lower Cytop cladding procedure.

Table 3 Lower Cytop Cladding Preparation Summary

Lower Cytop Cladding Preparation Summary	
Activity	**Details**
Layer 1 Spin coat 5% diluted M grade Cytop	10 sec@500 rpm/20 sec@1000 rpm
Baking	50°C for 30 min
Layer 2 Spin coat 9% S grade Cytop	10 sec@1000 rpm/20 sec@1500 rpm
Baking	50°C for 30 min
Layer 3 Spin coat 9% S grade Cytop	10 sec@1000 rpm/20 sec@1500 rpm
Baking	50°C for 30 min
Layer 4 Spin coat 9% S grade Cytop	10 sec@1000 rpm/20 sec@1500 rpm
Baking	50°C to 200°C @ 10 °C/hour for 18+ hrs
Edge Bead Removal (EBR)	RIE: 10 minutes @ 200W Perform a 30 second initial test run to ensure the EBR mask remains centered
Layer 5 Spin coat 5% diluted M grade Cytop	20 sec@1000 rpm
Baking	(30 min @ 50°C) + (50°C to 200°C @ 150°C/hr) + (2.5+ hrs @ 200°C) or 50°C to 200°C @ 10°C/hr for minimum 18hrs
Thickness	8.0µm (determined by etch depth)
Note: All baking performed on hot plate	

2.1.2.6 Lower Cladding Layer General Comments

It is generally prudent to do at least a quick 50x optical examination of the wafer after every baking to ensure that there are no inclusions (bubbles), contamination, and associated cracking in the Cytop cladding.

Gas bubble inclusions were typically not a problem with the lower cladding application process outlined here, as 30 minutes at 50°C is the ideal Cytop degassing procedure [34].

Contamination can simply not be tolerated. Foreign material included in the Cytop will of course generally compromise the final device but additionally nucleate cracking in the upper cladding and cause waveguide damage. Contamination (dried chemical bits, lint) was found to be an issue at the Carleton fabrication facilities in that the Cytop baking location was in the high traffic area of the spinner. For the long ramp bakes, a glass cover elevated on a couple of glass slides, placed over the wafer on the hot plate, was found to effectively solve the problem.

The presence of Cytop cracking at the completion of the lower cladding was a non issue, even around any contamination bits. Hard baking above the glass transition temperature (Tg) of 108°C was allowable during the lower cladding process since there was no metallization (this is discussed in more detail in Section 2.1.5). Hard baking above Tg causes the Cytop to flow and any cracks are effectively annealed.

Figure 15 is a profilometer analysis of an etched channel in a Cytop cladding, prepared using the application procedure of Table 3, showing the final aggregate thickness to be 8μm.

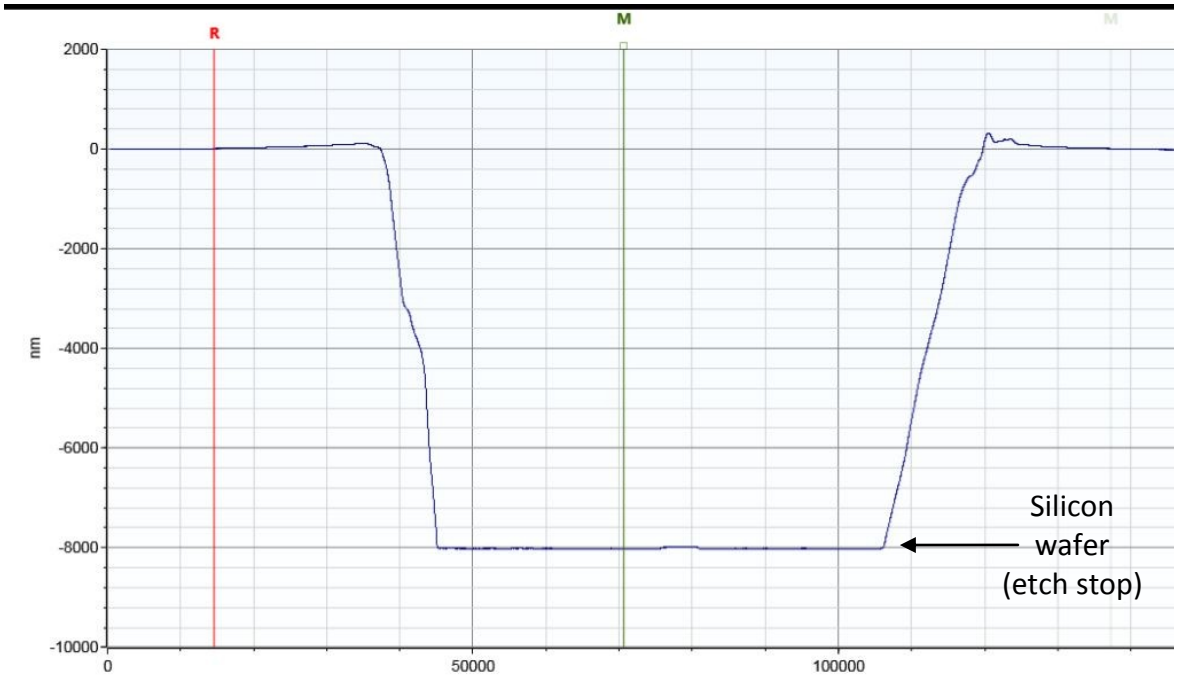


Figure 15: Profilometer Profile of Etched Channel in a Cytop Lower Cladding

2.1.3 Lithography

The basis of the bi-layer lithography procedure was adopted and modified from the previous work of [28] [30] and [31]. The documented lithographic procedures would not resolve the dimensions of C82 Bragg gratings (845nm – 900nm), refer to Table 1. Additionally, the metal quality of the previous lithographic procedures was found to have some quality problems (tearing, winging). These deficiencies were resolved by very subtle parameters changes to which the process was found to be extremely sensitive.

Once the lower Cytop cladding was complete the wafer was ready for the bi-layer lithography stage. Bi-layer lithography is a process of applying two (bi) layers of chemicals onto a substrate into which a pattern is chemically etched. Thereafter a metallization is applied, the bi-layer lithographic material is removed, and the metal pattern is subsequently adopted onto the substrate.

Much of the time spent for this project was in the determination of optimum parameters for bi-layer lithography application (specifically the LOR), the exposure time and development time to adequately resolve C82 Bragg gratings. Additional efforts were also spent on various HMDS application alterations. As a starting point, the bi-layer process from [30] was used and is summarized in Table 4.

Table 4 Initial Bi-Layer Lithography Process

Initial Bi-Layer Lithography Process per [30]	
Activity	**Details**
Cytop roughing	March RIE: 20 sec. for 2" wafers or 30 sec. for 4" wafers
Apply HMDS	Spin: (10 sec. @ 1000 rpm) + bake: (60 sec. @ 105°C)
Apply LOR (PMGI)	Spin: (10 sec. @ 500 rpm + 10 sec. @ 1000 rpm) + bake: (3 min. @ 180°C)
Apply PR (S1805)	Spin: (10 sec. @1000 rpm + 30 sec. @ 4000 rpm) + bake: (3 min. @ 115°C)
UV expose	6 to 12 seconds
Develop (MF-321)	2.5 minutes (75nm undercut)
Note: All baking performed on hot plate	

2.1.3.0 Lithographic Analysis: General

In the pursuit of quality patterning through lithography, the separate stages of the lithographic process; LOR application, PR application, amount of UV exposure, and development time (all performed the same day) are intimately bound. The parameters of one impact the parameters of another. A change of one can affect the final results as equally as a change in another. That is to say:

- Optimum bi-lithography parameters (type of PR and LOR, spin cycles, bake temperature and bake times) depend on feature dimensions
- Optimum exposure energy depends on bi-lithography parameters
- Optimum development time depends on exposure and bi-lithography parameters

Hence an isolated analysis of one of the lithographic steps was difficult because its contribution to the aggregate lithographic success depends on the other stages. A parameter isolating and iterative process was required to ultimately define the complete set of parameters to produce results that gave adequate Bragg gratings features.

2.1.3.1 Surface Preparation: Cytop Roughening

The first activity of the lithographic process was to roughen the surface of the Cytop lower cladding substrate. Roughening the Cytop improves the adhesive properties of the surface for the following lithographic chemical to be applied. The procedure, adopted and unchanged from [30], was performed in the March Systems Jupiter II plasma etcher. The system parameters for roughening are summarized in Table 5.

Table 5 Pre Lithography Cytop Roughening with March RIE System Parameters

Pre Lithography Cytop Roughening - March RIE System Parameters	
Action	**Details**
Etch Tim	20 sec. For 2 inch wafer, 30 sec. for 4 inch wafer
Baking	100 Watts
Oxygen Flow	220 - 225 sccm
Oxygen Pressure	350 - 450 mTorr

2.1.3.2 HMDS

Hexamethyldisilazane (HMDS) was used to promote lithographic resist adhesion to the substrate. Previously, the HMDS was applied with a spinning and curing procedure [28] [30]. With the acquisition of a Yield Engineering Systems (YES), LP-III, HMDS Vapour Prime Oven by the Carleton facilities, spinning and curing of HMDS was not the method of application used here. Application of HMDS was done in the YES HMDS oven. The oven temperature was set to 98°C, sufficiently below the glass transition temperature of Cytop, to ensure flowing of the lower cladding on the sample did not occur. The HMDS application cycle was approximately 30 minutes in duration.

In an effort to improve qualities in other stages of the process (gold adhesion and gold roughness), various alterations to the HMDS application stage were performed. The impetus for this included:

- "LOR resists have excellent adhesion to most semiconductor, ... substrates. Primers such as HMDS are typically NOT required to promote adhesion with LOR" [35]
- "... increasing the HMDS flow rate increased impurities such as C and H and the surface roughness ..." [36]
- "HMDS vapours ... will penetrate the resist film during resist coating. During the subsequent soft bake, this excess of HMDS releases ammonia which diffuses into the resist and chemically modifies the resin near the substrate, and also may cause cross-linking of the resin. As a result, the development rate decreases, and through-development may become impossible [37]

- “We strongly recommend to apply HMDS from the vapour phase onto heated substrates” [37]
- “In the case of spin-coating the HMDS .... After resist coating during the soft bake, this excess of HMDS releases ammonia which diffuses into the resist and cross-links the resin near the substrate. As a consequence, thorough development sometimes becomes impossible.” [38]

It was inferred from these articles that HMDS:

- was not required for LOR adhesion,
- could affect surface roughness
- can change the development rate of LOR deposited on the HMDS
- could cause residual cross-linked LOR to be present (under the metallization)
- should only be applied as a vapour onto heated substrates (in an oven system)

With this technical information and with process refinements desired at a certain time in the project (improved gold surface quality), numerous tests were performed altering the HMDS process stage:

- Omitting the application of HMDS caused poor LOR adhesion and subsequent PR adhesion
- Changing the temperature of the HMDS oven significantly changed the current lithographic development results
- Post baking the sample after HMDS oven application caused poor LOR quality and significantly changed the current lithographic results
- HMDS application by spinning using the methods of [28] [30] significantly changed the current lithographic development results

After the various HMDS process alterations it was concluded/accepted that:

- HMDS must be applied prior to LOR application or the LOR simply does not adhere to the Cytop substrate.
- For consistent and acceptable lithographic results the HMDS was best applied using the vapour prime oven system.

2.1.3.3 Lift-Off Resist

The initial lift-off resist (LOR) used was Microchem's PMGI SF2. As discussed by [30]; PMGI as an LOR, provides superior lithographic results due to the low dissolution rate. The purpose of the LOR is twofold:

- To “undercut”: To laterally dissolve away underneath the overlying photoresist during the development stage so the metallization during deposition does not stick to the side walls of the bi-layer. Additionally, it was important that the LOR was completely dissolved away, or cleared, down to the substrate in the lithographic patterning to ensure good metal to substrate contact and adhesion during deposition.
- To “lift-off”: To completely dissolve away after metal deposition. This removes the bi-layer leaving only the metallization (in the pattern of the lithography) on the substrate. This will be discussed further Section 2.1.4.2.

During the lithographic process testing, the LOR was not assessed on its own, rather the composite lithographic results (during development or post development) were always optically analysed. The optical analysis and quality assessment of the lithography is discussed in more detail in Section 2.1.3.6

Using the initial PMGI based bi-layer lithography process outlined in Table 4, Bragg biosensor samples were prepared. Typical results were well developed Bragg gratings (correct duty cycle) but overdeveloped (too wide) center channel as illustrated in Figure 16.

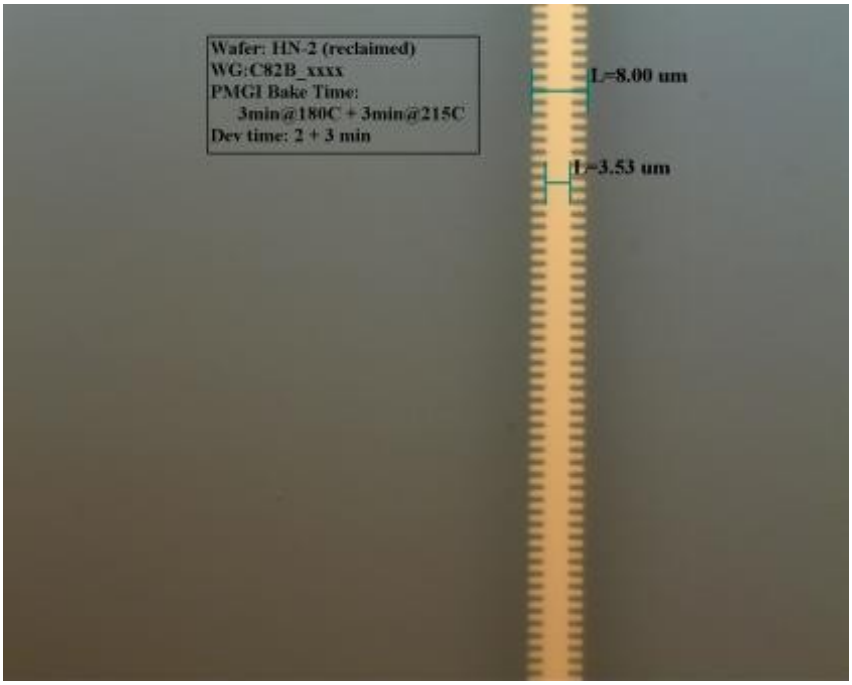


Figure 16: C82B Bragg Grating Using Original PMGI Bi-Layer Process.
Good grating duty cycle, good gold adhesion, over-developed channel dimension.

Consultation and literature investigation into the development times of the photoresist S1805, as applied similarly to the tests, indicated that normal development time is around 60 seconds [39] [40]. Additionally, extended exposure to developer can cause even unexposed S1805 to dissolve. Using around 60 seconds development resulted in underdeveloped Bragg gratings (too thin) and a well developed (correct width) center channel, yet a marked improvement in features. The results, illustrated in Figure 17, were found to be consistently of poor waveguide quality in the form of:

- Fully torn waveguides on lift off
- Partially torn wave guides “mouse bites” on lift off
- Winging; high topography of metallization build up at the edges of the waveguides (observed under dark field)

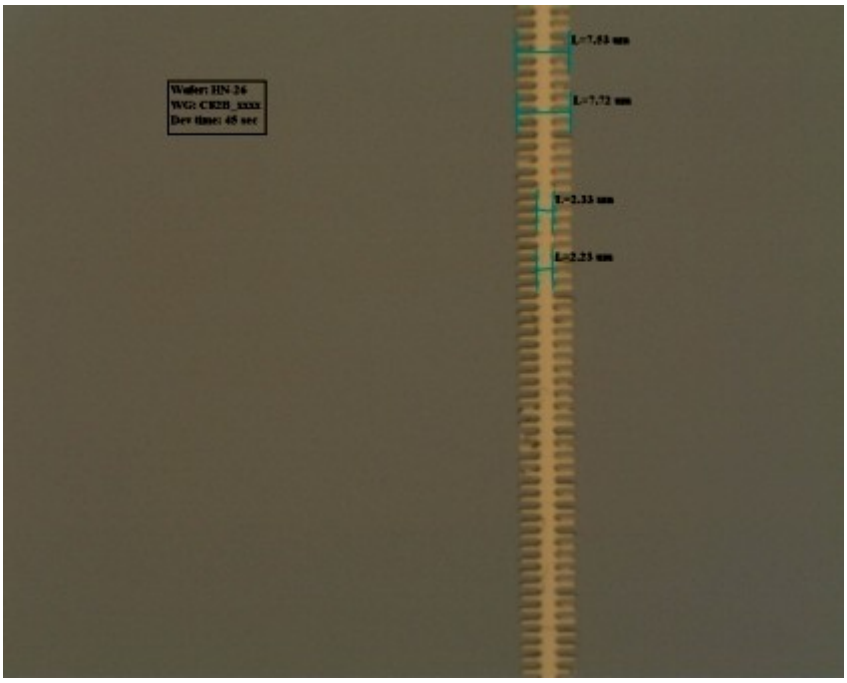


Figure 17: C82B Bragg Grating Using Original PMGI Bi-layer Process with Short Development Time
A 45 second development time gave poor grating duty cycle, good channel dimension and poor gold quality.

Efforts made to resolve the poor Bragg waveguides generated with PMGI, without acceptable success, were:

- Changing PMGI curing time and temperature; in an attempt to change dissolution rate.
- Changing lithographic development times.
- Changing UV exposure times (optimal exposure time at this point was not identified).
- Note: S1805 photoresist application procedure was never changed (at any time in the project.

The low dissolution rate of the PMGI, indicated by [30] to be 75nm in 2.5 min or 0.5nm/sec was then considered in conjunction with the development time being used. At this dissolution rate and a 60 second development time, a 150nm thick layer of PMGI would possibly not even be fully penetrated, suggesting insufficient undercut and PMGI remaining in the waveguide channels on the Cytop substrate. Additionally SEM images were taken of select samples. The SEM image of Figure 18 shows negligible undercut in a 40 second development time. The torn waveguides and metallization winging observed were attributed to this.

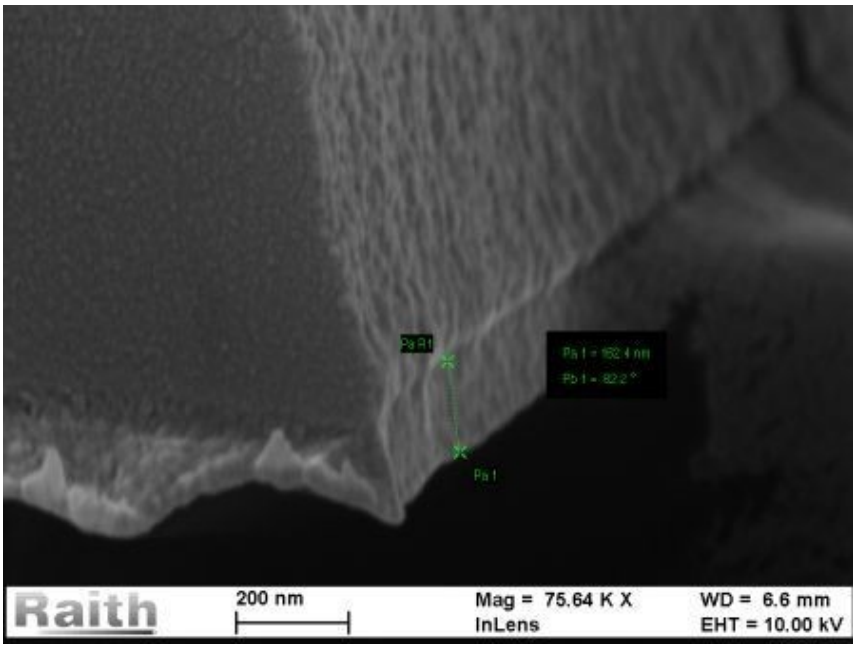


Figure 18: SEM Image of Original PMGI Bi-layer
S1805 on PMGI (162nm thick) showing very little undercut after 40 seconds development. Courtesy Wei Ru Wong

Hereafter, Microposit LOR-1A was used as per [28] as the lift-off resist and resulted in immediate improvement in waveguide appearance and gold adhesion quality as show in Figure 19.

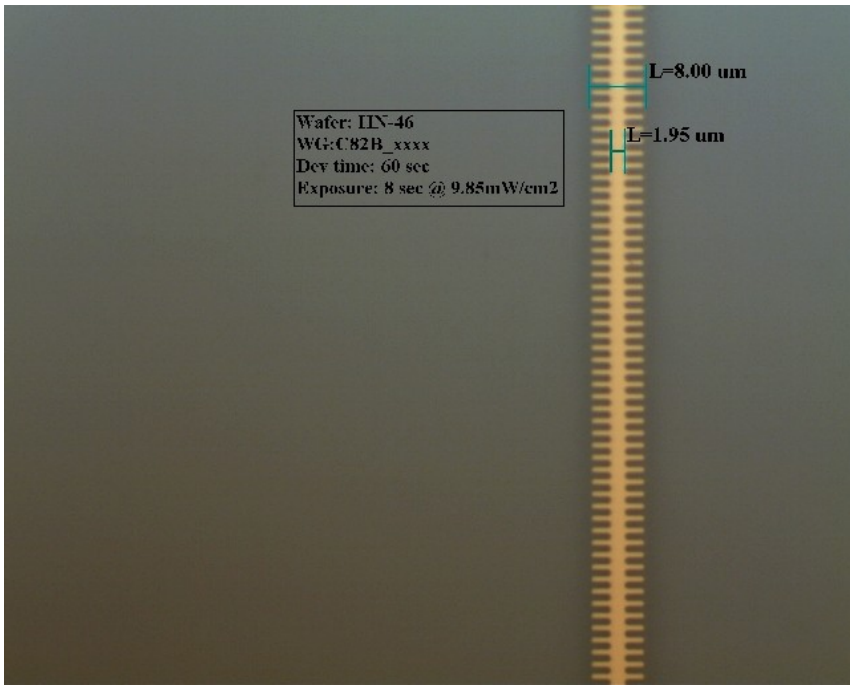


Figure 19: C82B Bragg gratings Using S1805/LOR-1A Bi-Layer Underdeveloped gratings, good channel dimensions and good gold quality. Exposure of 8 seconds at 9.85mW/cm^2= 78.8mJ/cm^2. Development in MF321 for 60 seconds.

Table 6 shows the LOR-1A application procedure used for the remainder of the project.

Table 6 LOR-1A Lift-Off Resist Application Summary

LOR-1A Lift Off Resist Application Summary per [28]	
Action	**Details**
Pipette dispensing	Cover entire wafer with LOR-1A solution
Spin coat	(10 sec. @1000 rpm) + (30 sec. @ 4000 rpm)
Bake	Hot plate for 3 minutes @ 180°C

A general note about the baking method of the samples during the lithographic procedure is important early in the lithographic discussion. The baking was performed on DATAPLATE brand programmable hot plates. These hotplates are not particularly designed for the precision curing of silicon wafers, rather for the heating of solutions in beakers. Examination with an infrared thermometer gun showed a difference in the temperature at the centre of the hot plate and that displayed on the hot plate console. The temperature difference had to be accounted for during the lithographic procedure. Also, a variance of temperature in a 4-inch diameter area centered on the hot plate was observed to exist. Additionally, the hot plate surface is not entirely flat. When a 4-inch wafer is placed on the hot plate the entire wafer does not touch the hot plate surface. These hot plate characteristics were considered to be a factor of lithographic feature inconsistency on the 4-inch samples. It is considered that better baking surfaces would generally improve lithographic results.

2.1.3.4 Photoresist

The photoresist (PR) layer of the bi-layer lithographic stack is the top layer. The photoresist is sensitive to UV light. When exposed to UV light, a positive PR becomes soluble in the developer. The type of PR used and the application procedure was directly from [28] [30] [31]. The PR used was Microposit S1805 positive photoresist. The photoresist was applied (to the LOR layer) as presented in Table 7. The PR application procedure was unchanged for the duration of the project.

Table 7 S1805 Photoresist Application Summary

S1805 Photoresist Application Summary per [28] [30] [31]	
Action	**Details**
Pipette dispensing	Cover entire wafer with S1805 solution
Spin coat	(10 sec. @1000 rpm) + (30 sec. @ 4000 rpm)
Bake	Hot plate for 3 minutes @ 115°C

2.1.3.5 Exposure

The ultra-violet (UV) exposure of the bi-layer lithography was performed with a Karl Suss MA6 system. The system performs contact exposure. Contact exposure, as opposed to projection exposure (used in industry today), is the process of directly placing the mask against the sample. UV light is then shone upon the mask and where the UV light passes through the mask the PR below is "exposed". Note that the LOR layer is unaffected by the UV exposure. Contact exposure requires that the sample is flat and without topography so there are no air spaces between the mask and the sample; this will compromise the definition of the mask pattern transfer. Choice of a quality silicon wafer at the start of the process (Section 2.1.1.1) and edge bead removal (Section 2.1.2.3) helps to accommodate this requirement.

To produce deposition features that are consistent with those on the mask, especially fine features of dimensional order of the wavelength of the UV spectrum being used, the quantity of energy of UV exposure is a very important criterion. The energy is quantified in units of millijoules per square centimeter (mJ/cm^2). The system generates UV radiation intensity peaks at I-line (365nm), H-line (405nm) and G-line (435nm). As a standard operating procedure of the Carleton facilities, the power of the I-line and H-line wavelengths are calibrated regularly and recorded. In this project the H-line power was also calibrated just prior to exposure and this was used as the metric for exposure energy consistency. The required energy for appropriate photoresist exposure required in previous biosensor projects was somewhat loosely defined:

- An exposure time of 6 seconds [28].
- An exposure time of 7 to 8 seconds, or an energy of 80 - 180mJ/cm^2 [30].
- An exposure time of 12 seconds [31].

Identifying the correct amount of UV energy that correctly exposed the PR of the bi-layer lithography was a main activity of the Bragg grating lithographic process.

Additional information identified to assist in the starting point for a setting of the exposure power was found:

- "For S1805, ... (spun to 4000 rpm) ... use an exposure dose of 50 mJ/cm^2 @ 405 nm" [39]
- "Shipley 1800 resist has a fairly large exposure window. ... determine the H-line (405nm) intensity ... Select an exposure time to give a H-line dose of between 50 and 100 mJ/cm^2 ... Optimum exposure dose depends on resist thickness, feature size, and feature shape. For very small features, testing a range of exposures will likely be needed to determine the optimum dose." [40]

With this, many iterations of exposure power and development times were pursued and the deposition results analysed. The criteria for judging the appropriate exposure energy was optical analysis of the dimensional quality of the C82B Bragg gratings, after deposition, at 1000x magnification, recall dimensions Table 1. The concluding optimal exposure times determined for specific Cytop cladding thicknesses are summarized in Table 8. The uncertainty ranges indicated in Table 8 were derived from exposure tests using exposure energy increments of 0.5 mJ/cm^2. Outside of these ranges under or overdevelopment was observed. The exposure energy increments were only ever taken to a minimum of 0.5 mJ/cm^2.A good quality C82 Bragg grating, on a full lower Cytop cladding, from an H-line exposure of 114.5 mJ/cm^2 is shown in Figure 20.

Table 8 UV Exposure Energy Summary

UV Exposure Energy Summary	
Wafer Characteristics	**UV Exposure Energy (H-line; 405nm)**
No Cytop (Litho on silicon)	118±0.5 mJ/cm^2
Half lower cladding (~4µm)	116±0.5 mJ/cm^2
Full lower cladding (8µm)	114±0.5 mJ/cm^2

The exposure is reported in millijoules per square centimetre (mJ/cm^2). This is consistent with technical documentation regarding lithographic exposure and it makes the exposure value more portable to other systems. That is, if reported in seconds, for example 10 seconds on the Carleton system will give a different exposure energy than

10 seconds on another system due to the likelihood that different systems may have a projection bulb of a different power. In fact, the Carleton exposure system mercury bulb went from an H-line power of 10.00mW/cm^2 in May 1014 to 8.35mW/cm^2 in June 2015; simply wearing out in time. Hence, an 11.40 second exposure would be 114mJ/ cm^2 in May 2014 (ideal for lithography on a full lower Cytop cladding) but only 95mJ/cm^2 in June 2015 which would yield significantly underdeveloped C82B Bragg gratings. Of course for an exact inter system portability the power intensity of the full spectrum (G-line, H-line and I-line) of the exposure lamp must be considered.

Different exposure energies were found be optimal depending on what was below the bi-layer. The lower energy was found to be best when there is a distance (a lower Cytop cladding thickness) between the bi-layer and the reflective silicon substrate; this is attributed to additional exposure energy from back reflection. The higher exposure energy was found to give better results when the bi-layer was directly on the silicon substrate, attributed to less back reflection. It was observed that Bragg gratings generated directly on the silicon wafer had straighter gratings. When generated on a full lower cladding, more angular gratings were observed. Specifically, the different exposure times were used for the following different fabrication scenarios:

- 118mJ/cm^2 with no Cytop, deposition directly on the silicon wafer. Typically on 2-inch wafers during gold and roughness and thickness tests.
- 116mJ/cm^2 with a thin Cytop lower cladding composed of only three layers; a bottom M-grade, a middle S-grade and a top M-grade layer. Done to minimize the consumption of Cytop where an optically infinite lower cladding is not required. Typically on 2-inch wafers during gold adhesion tests.
- 114mJ/cm^2 with a full Cytop lower cladding. Typically on 4-inch product samples.

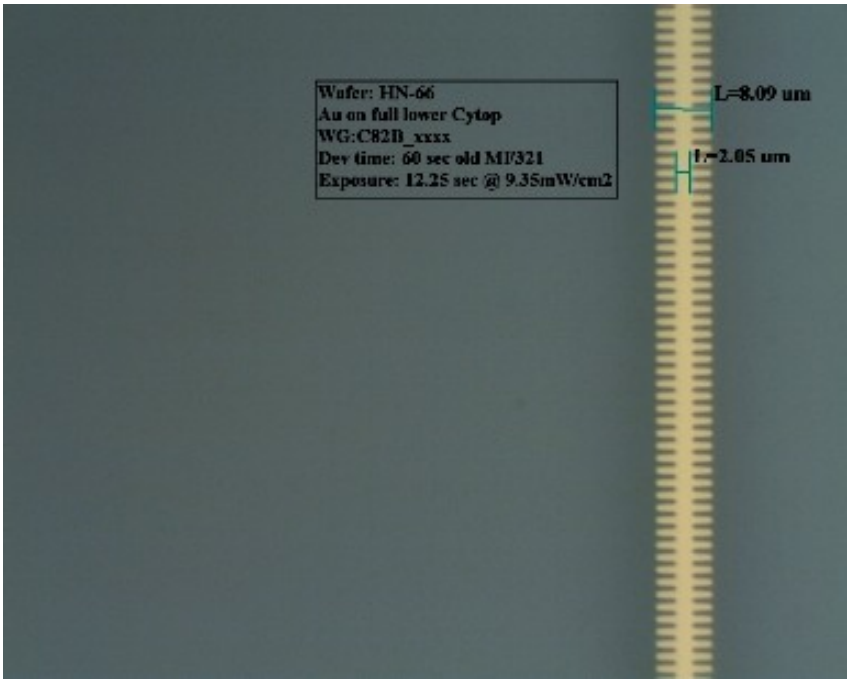


Figure 20: C82B Bragg Waveguide Showing Adequately Developed Gratings

On 2 inch wafer with full Cytop lower cladding. Bi-Layer Lithography with S1805 and LOR-1A Exposure of 12.25 seconds at 9.35mW/cm^2 = 114.5mW/ cm^2. Development in MF321 for 60 seconds.

Rounding of the ends and crotches of the Bragg gratings were always observed on the lithographic patterning, where on the exposure mask the ends and crotches of the Bragg gratings are square. Corner rounding of small mask features in a lithographic pattern is unavoidable. Rounding is a result of the diffraction limitation of image formation for features with dimensions near the resolution limit of the exposure wavelength [41]. Recall that the C82B Bragg gratings are 845nm to 900nm in width and the UV exposure H-line wavelength is 405nm. The rounding had a more pronounced effect on the lower

amplitude gratings of the C52, C53 and C54 Bragg waveguides (especially the C54) when subject to the lithographic process that resulted in acceptable C82 Bragg gratings. The C54 gratings had the appearance of being completely eroded away, possibly due to the C54 gratings having lengths of 500nm which is close to the wavelength of the exposing UV light. In general, the lithographic procedure that resulted in favourable C82 gratings did not result in acceptable features of the other Bragg gratings. The C82 gratings ultimately were the focus of assessing the success of a lithographic trial. The C54 gratings were ignored early in the project and are considered to be irresolvable by the lithographic capabilities at the Carleton fabrication facilities. Suggested tests to resolve the definition of the C54 Bragg gratings would be using bi-layer lithography with shorter wavelength exposure or alternatively e-beam lithography. Figure 21 illustrates the typically very poor resolving of the C54 gratings.

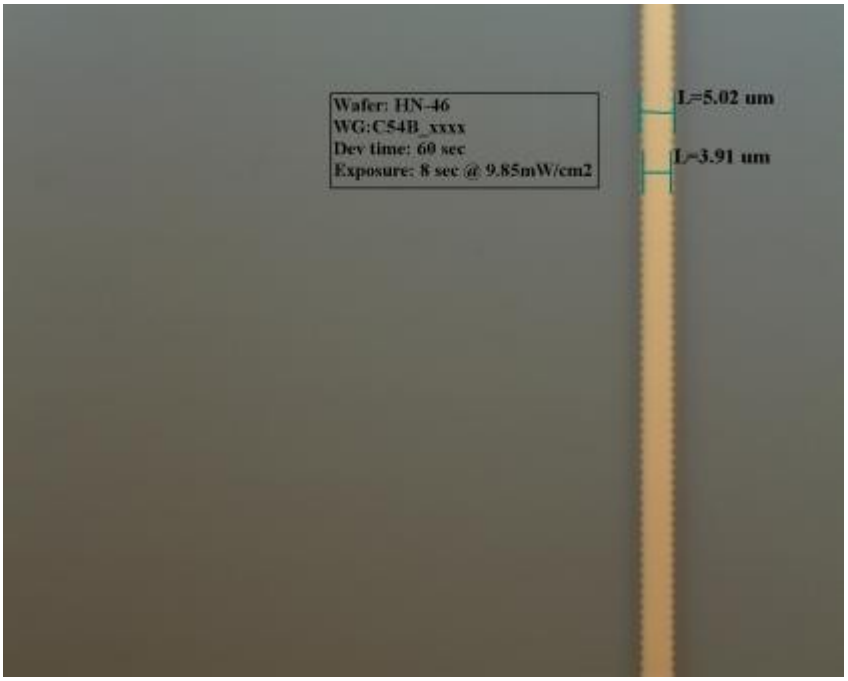


Figure 21: C54B Bragg Waveguide on 2 Inch Wafer
Non-existent gratings. On half lower cladding of Cytop. Bi-layer lithography with S1805 and LOR-1A. Exposure of 8.00 seconds at 9.85mW/cm^2 = 78.8mW/cm^2. Development in MF321 for 60 seconds.

2.1.3.6 Development

Development of a UV exposed bi-layer lithographic stack is the process of chemically dissolving away the exposed (positive) photoresist and the lift-off resist directly underlying, to leave the imprinted mask pattern ready for deposition. Factors which affect the rate of the bi-layer dissolution include:

- Lift off resist: type, thickness, temperature of baking, length of bake time. UV exposure has no effect on the lift off resist. Other factors include ambient room temperature and humidity during the photoresist preparation.
- Photoresist: type, thickness, temperature of baking, length of bake time, UV exposure energy. Other factors include ambient room temperature and humidity during the photoresist preparation.

As per [28] [30] [31], the developer always used here was Microposit MF-321 developer. MF-321 is 1.91 percent tetramethylammonium hydroxide (TMAH) solution with surfactant, the TMAH concentration is low compared to other TMAH based developers available. The developer concentration sensitivity is illustrated in one particular development test performed when analyzing the S1805/PMGI bi-layer development characteristics. The MF-321 was diluted by 50% with de-ionized water and no pattern development was observed (of the S1805) after 14 minutes. Then, subject to 60 seconds of full strength MF-321 full pattern development was observed to be complete. Note, that for each development, fresh MF-321 was not used. A two litre volume supply was repeatedly used and the number of uses tracked. Even, after many uses the same MF-321 gave consistent 60 second development results.

The development was performed by securing the sample in a wafer holding wand and immersing the sample in a beaker for a stop watch controlled time. It was found that for best results:

- Use a 60 second MF-321 immersion time.
- Use a large beaker was used to allow ample room to agitate the sample.
- Use a large volume of MF-321. Certainly over a litre for 4 inch wafers.

- Perform very rapid agitation equally up and down and side to side with light waving on the face of the wafer. This was found to give the most uniform results across the wafer.
- Ensure the wafer is securely set in the wafer wand, if it falls out the development is probably compromised.

The MF-321 development was followed immediately by immersion in de-ionized water for around 2 minutes then rinsing with de-ionized water and finally a nitrogen blow dry.

The procedure for identifying the ideal development time was simply adjusting it and observing the results. Typically the UV exposure time was the only other parameter changed in a development time test. Hence, an iterative process of exposure time adjustment and development time adjustment was performed until the best C82 feature resolution was realized.

The optical analysis of the development progress (and general assessment of the lithographic process) was performed in a UV filtered environment at maximum magnification of 500 times. A non-UV filtered 1000x magnification photo microscope was available, but if used during the development stage it would further expose the PR and no further development was possible. Desired lithographic qualities were; proper Bragg grating dimensions (of C82B gratings) and adequate undercut (shown in Figure 13, illustration 3c). The assessment of sufficient undercut was very difficult, especially to the novice eye. Optical determination of sufficient undercut is performed under the microscope by moving the focal plane from the pattern of the PR on top to below and observing the emergence of a rim around the PR pattern. The rim is the edge wall of the LOR underneath. With the dimensions of the Bragg gratings and especially if a thick layer of Cytop was present, this method was often inconclusive. Hence, to fully assess the results of the lithographic process used, gold deposition was typically performed, and the quality of the gold patterning was simply assessed.

Once the lithographic development is complete, the bi-layer lithography stage is complete and the sample is ready for the deposition stage.

2.1.3.7 Cytop Bi-Layer Lithography Procedure Summary

The bi-layer fabrication process for the Cytop based LRSPP biosensor is summarized in Table 9. With this bi-layer lithographic procedure C82 Bragg gratings are resolved very well. The procedure applied to the "Biosensor" and "New Biosensor 2014" waveguide mask patterns also generates excellent lithographic results. Note that features on the "Biosensor" and "New Biosensor 2014" masks are larger than those of the C82 Bragg waveguide gratings.

Table 9 Bi-Layer Lithography Procedure Summary

Bi-Layer Lithography Procedure Summary	
Action	**Details**
RIE Roughening (March)	20 sec for 2" wafer, 30 sec for 4" wafer
HMDS application	HMDS oven at 98°C
LOR-1A pipette dispensing	Cover entire wafer with LOR-1A solution
LOR-1A spin coat	(10 sec. @1000 rpm) + (30 sec. @ 4000 rpm)
LOR-1A Bake	Hot plate for 3 minutes @ 180°C
S1805 Pipette dispensing	Cover entire wafer with S1805 solution
S1805 spin coat	(10 sec. @1000 rpm) + (30 sec. @ 4000 rpm)
S1805 bake	Hot plate for 3 minutes @ 115°C
UV expose	per Table 8
MF-321 development	60 seconds
DI rinse and Nitrogen dry	2 DI minutes immersion + DI spray gun rinse + Nitrogen gun blow dry
Optical examination in UV filtered environment	At 500x: look for proper lithographic development; features and undercut
Note: All baking performed on hot plate	

2.1.4 Metallization: Deposition and Lift-Off

2.1.4.1 Deposition

The metal deposition was performed in a Balzers Model BA-510 vacuum evaporator system. The controller of the system is an Infinicon IC/4 Plus. Note that the controller was replaced and reprogrammed on Feb 12 2014. The metal deposition procedure summarily involves two stages:

- The samples were mounted in the system's vacuum chamber and a minimum 4 hours "pump down" was performed to a maximum pressure of $1x10^{-6}$ Torr. Typically the pump down was allowed to run overnight, and a pressure of $1.5x10^{-7}$ to $3.5x10^{-7}$ Torr was achieved.
- Perform the metal deposition when the appropriate pressure was achieved, or the next day.

To avoid degradation of the lithographic patterning the sample should be placed into the deposition vacuum chamber directly after the lithographic development stage. In this project, specifically, the samples were placed in the deposition system chamber immediately after lithographic development.

There are two physical methods available for metal evaporation in the Balzers system; e-beam and thermal. For the first few samples, and with technical assistance, e-beam deposition was used. For a good overview of the e-beam deposition method see [30]. The e-beam deposition method is involved to set up and run and consumes more gold. The thermal method is simple to set up and requires less gold. Thermal evaporation involves placing the gold in a tungsten "boat" through with a current is run. The tungsten boat is heated through ohmic resistance, the gold melts, and the resulting gold evaporation rate can be controlled by manually adjustment of the current. During the early stages of the project, gold deposition was performed to more definitively establish the success of the lithographic procedure. E-beam deposition on test samples, that were likely to be of poor feature quality, was considered to be resource inefficient.

Thermal evaporation was therefore used for the duration of the lithographic testing until quality lithography was achieved.

Once acceptable lithographic results were achieved e-beam deposition was reintroduced to the fabrication procedure. The preceding biosensor efforts of [28] [29] [30] [32], used the e-beam deposition method. Gold thickness and roughness is very important for the propagation of LRSPP's. The target thickness requirement is 35nm, 40nm is too high and 30nm is too low. For roughness a root mean square (rms) of 0.7nm and average of 0.5 achieved by [30] is acceptable. The e-beam samples were analysed by Atomic Force Microscopy (AFM) for gold thickness and roughness determination. See Figure 22 for the AFM results of e-beam deposition.

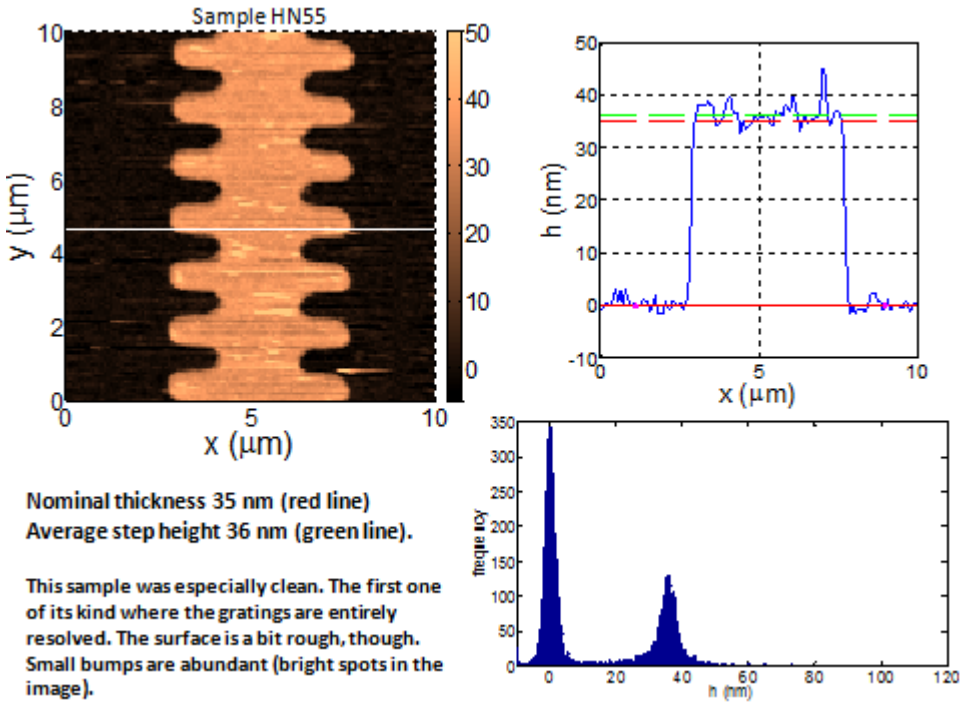


Figure 22: AFM Analysis of Bragg Waveguide

Full Cytop lower cladding on 2- inch wafer showing good nominal gold height and poor surface quality. Bi-Layer Lithography with S1805 and LOR-1A. Exposure of 9.00 seconds @ 9.75mW/cm^2 = 87.75mW/cm^2. Development time of 60 seconds in MF321. Gold deposition method is E-beam at 0.5 Å/s with tungsten crucible and using "old" gold. Courtesy Behnood Ghamsari

The AFM results show excess roughness, and also gold contamination. The roughness and contamination (thought to be carbon) was persistent in many trials and observed by others performing the same procedure. Attempts were made to improve the surface quality, with no success, including:

- New tungsten crucible
- New gold: 7 pellets required in a new e-beam crucible @ 0.47g each.
- Changing deposition rates; 0.5 Å/s, 1.0 Å/s, 0.2 Å/s
- The “no-spit” e-beam method of [30]

Ultimately the e-beam deposition method was abandoned and thermal deposition was used. With the adoption of the thermal deposition method the deposition parameters and procedure had to be fully assessed for the thin, 35nm deposition requirements. Early attempts gave poor gold thickness, roughness and variance across the sample surfaces. To address the poor variance of the gold thickness a rotational wafer mounting method was adopted. There are two physical methods available for securing the samples in the Balzers evaporation chamber:

- The lift-off plate is fixed and sits centrally in the chamber in a horizontal orientation. There is a hole in the center, oriented directly above the evaporation source to allow evaporate to deposit on a crystal thickness detector. The samples are magnetically fixed to the rim area of the plate.
- On rotation plates that roll around at a programmable rate near the top of the chamber. The plates lean inward at approximately 45 degrees toward the evaporation source. The samples are set into or are magnetically fixed to the plates.

With the use of rotation mounting the variance of gold thickness was found to be within 10% of nominal across 4 inch sample. Use of the rotation mounting introduced unacceptable metal thicknesses; up to 60nm was observed when targeting 35nm. This required the recalibrating of the deposition system for rotation mounting. It was observed that even location on the mounting plate had up to a 10% difference in the

gold thickness. Specifically, if a 2-inch wafer is placed at the centre or the edge of the mounting plate a difference in deposition thickness was observed.

Adjusting the “tooling factor” was required. The tooling factor is a percentage value entered into the Balzers controller. The requirement for a tooling factor is that the samples in the chamber are offset from the crystal detecting the thickness. Hence, the evaporated metal thickness realized by the crystal and samples is different by some percentage; the tooling factor is that percentage. The tooling factor value is unique for a particular deposition arrangement; source type and sample securing method. The process for arriving at the tooling factor is iterative and the formula for calculating the tooling factor for a particular deposition run is:

New tooling factor = (actual thickness/intended thickness) x tooling factor used

A correct tooling factor value is essential for achieving the desired metal thickness during the deposition procedure. Many deposition test runs were performed to arrive at a tooling factor of 188% for thermal evaporation and rotation plate sample mounting. For the thickness tests the deposition performed was dominantly gold on chrome on silicon, without Cytop. Omitting the Cytop lower cladding makes for a shorter sample preparation time and cleaner profilometry data. Gold deposition thickness was analysed with the Carleton fabrication profilometer, Carleton Chemistry AFM, University of Ottawa AFM and profilometer, and by SSW (Western University, London, Ontario) AFM services.

Once acceptable gold thickness was achieved the gold roughness was the focus. To resolve dimensions of the desired gold roughness, on the order of 1nm, AFM analysis must be used. AFM examinations of various stages of the fabrication process up to gold

deposition were performed. AFM surface evaluations were performed of; the factory wafer, post HF cleaning, post plasma preening, the Cytop deposition surface, variations of HMDS/LOR-1A preparation, and RIE roughened and non-roughened Cytop. All showed that the deposition surface roughness of the process was acceptable. The remaining variable was the gold deposition. Effectively, in the deposition procedure the only controllable parameter is the deposition rate, and a few operational tricks. Using a very low deposition rate of 0.1 Å/s was found to give acceptable gold surface roughness quality and additionally improve the gold thickness variation on the samples.

Operational suggestions for the Balzers evaporator to give good target thickness (of 35nm) and low surface roughness using a low (0.1Å/s) deposition rate are listed below. Familiarity with the operation of the Balzers deposition system is assumed here. It is important to note that on 4-inch wafers the Bragg gratings will not sufficiently adhere to the Cytop substrate. On 2-inch wafers the Bragg gratings will adhere very well to the Cytop substrate. The adhesion difference is qualitatively attributed greater tensile stresses, and expansion-contraction properties of the Cytop on the larger size wafer. This caused the gold to tear from the Cytop during lift-off. As a result, for deposition on 4-inch wafers patterned with Bragg grating a 3 Å chrome adhesion layer must be deposited prior to the gold deposition. The following steps apply to the brief initial chrome deposition and the following, longer gold deposition.

Deposition procedural suggestions:

- A pre-deposition burn in. The intention is to burn off any contaminants that may have collected on the gold sample and tungsten boat during handling. Heat the metal prior to the deposition at a high variac setting of 65 volts (giving approximately 5 amps) for one minute.
- A pre-deposition stabilizing period. Performed after the burn in to prevent an initial puff of evaporate that could potentially compromise the metal surface quality. Turn the variac down to approximately where a 0.1 Å/s deposition rate

will result; approximately 52 volts (giving approximately 4.5 amps). Leave for one minute.

- Deposition; open the shutter slowly, start a stopwatch and monitor the deposition thickness display. The Infinicon controller displays the deposition rate to an accuracy of only one decimal. Monitoring the displayed deposition rate is not sufficiently accurate to achieve 0.1 Å/s. To accurately achieve a deposition rate of 0.1 Å/s the thickness display must be monitored. Through very tight variac control, and a stop watch, the thickness display must be maintained to increment at (approximately) 6Å per minute. For a gold target thickness of 350Å the gold deposition will then take approximately 1 hour.

Table 10 summarizes important activities and parameters in the deposition procedure. The gold and the chrome deposition had the same system parameters.

Table 10 Thermal Gold Deposition with Rotation Mounting Summary

Thermal Gold Deposition with Rotation Mounting Summary	
Activity	**Details**
Important set up particulars	Zero deposition thickness on controller. Start rotation.
Burn in and stabilization	(65 volts for 1 min.) + (53 volts for 1min.) + open shutter
Chrome deposition[1] (set material on controller)	Thickness of 3 Å @ 0.1 Å /sec. Tooling factor = 188
Important set up particulars	Zero deposition thickness on controller.
Burn in and stabilization	(65 volts for 1 min.) + (53 volts for 1min.) + open shutter
Gold deposition (set material on controller)	Thickness of 350Å @ 0.1 Å /sec. Tooling factor = 188
[1]For Bragg grating lithography on a 4-inch wafer a chrome layer is required for adhesion	

2.1.4.2 Lift Off

Lift off follows the metal deposition and is the process of removing the LOR (and everything above it) resulting in only the metal patterning of the lithography on the substrate. Lift off is best performed immediately after the metal deposition to avoid delamination of the features. The lift off procedure used was always performed immediately after the samples were removed from the Balzers deposition chamber. The lift-off procedure must adequately remove all residues and potential contamination but not so aggressively as to damage the desired metallization patterning. The basic lift off procedure used in this project was identical to that used by [28] [30] [31].

Some lift-off procedural suggestions are listed below:

- Get the 1165 lift off baths heating before starting the deposition, ideally at a location near the deposition system. The baths will then be at the appropriate temperature when the deposition is complete.
- Do not be too concerned of incomplete lift off after the first ultrasonic cleaning. Remaining gold will all very likely come off during the second ultrasonic cleaning. Do not exceed 10 seconds, excessive ultrasonic cleaning will cause waveguide delamination.
- Perform the second ultrasonic cleaning for 5 seconds. Inspect for residual gold particles, if none, no need to perform for an additional 5 seconds.
- During the inspection of the sample for residual gold particles, keep the sample in the 1165 bath, do not let the 1165 completely run off the sample, or worse dry off. If the sample becomes dry of 1165 while gold particles are present they will adhere and will not be removed by the subsequent IPA bath.
- Residual gold particles are unwanted; they will compromise the final device and nucleate cracking of the upper cladding to follow. If residual gold particles still exist after the second 10 second ultrasonic cleaning, they must be manually swabbed off. This must be done gently or the swabbing will damage the waveguide metallization.

The last step of the lift off process is to dehydrate the samples. The wafers were placed in an oven set at 100°C for 15 minutes. The lift off procedure is summarized in Table 11.

Table 11 Post Deposition Lift-Off Summary

Post Deposition Lift Off Summary	
Activity	**Details**
Immersion in clean 1165	10 minutes @ 80°C
Put clean beaker in water filled Ultrasonic	10 seconds (maximum)
Immersion in dirty 1165	10 minutes @ 80°C
Put dirty beaker in water filled Ultrasonic	5 second + 5 seconds (maximum)
Inspection	While immersed in 1165 solution. Remove any remaining gold particles by gentle swabbing.
IPA rinse	10 minutes immersion@ room temperature
DI rinse	10 minutes immersion, followed by DI flush with spray gun
Sample drying	Nitrogen gun blow
Dehydration	15 minutes at no more than 100°C

2.1.4.3 Post Lift-Off Optical Analysis

After the lift-off procedure a detailed optical analysis of the sample should be performed and a determination made whether the quality would support a final product. Suggested optical analysis and assessment is:

- At 50x magnification:
  Look for Cytop degradation in the form of cracking, inclusions, and contamination bits. Most importantly the quality of the metallization; look for waveguide and general metallization damage. This was typically observed as poor adhesion in the form of significant tearing.
- At 1000x magnification and dark field:
  Look for proper feature dimensions, adhesion of fine features (Bragg gratings) and satisfactory gold quality (no small scale tearing and winging).

2.1.4.4 Post Lift-Off Waveguide Height Analysis

Prior to starting the application of the upper cladding the waveguide thickness should be determined. A profilometer is used to measure the height of the waveguides. The profilometer system used in the Carleton facilities is a Tencor P-1 Long scan profiler. The Tencor P-1 system was tested with calibration standards having step heights of 1000A

and 500A and an accuracy of at least ±5% was indicated. The accuracy of the system in the 35nm step height range is accepted to be at least ±5%. The Tencor does not have the resolution to accurately determine surface roughness of the order of a few nanometers. The profile scan parameters used to evaluate the waveguide height were:

- Profile length of 50µm
- Scan speed of 2µm/second
- Sensor weight of 15mg. This was particularly important. When scanning on Cytop if a weight of 50mg was used a very noisy profile was generated. This was attributed to the sensor possibly dragging through the surface of the Cytop. Also a heavier sensor weight may scratch or tear the gold features.

2.1.4.5 Post Lift-Off Discussion

After lift-off there is an exposed pattern of thin 35nm metallization on an 8µm thick Cytop layer. Due to the nature of the Cytop substrate the metallization is susceptible to deformation. This will be discussed in greater detail Section 2.1.5.1. Also, physical surface contact can cause abrasion and scratching and damage to the waveguides. If the sample will not be further processed immediately it is best placed in a 100°C oven for safe keeping and further solvent evaporation.

An observation of wafers subject to a long post-lift off bake is worth mention at this point. Samples HN-123 and HN-124 were part of a lower cladding baking test and were subject to slower, longer and higher temperature baking during the lower cladding preparation. These samples should have had less solvent content than samples prepared with the normally used lower cladding application procedure of Table 3. Immediately after lift-off the metallization thickness was profiled to be 325 Å. The samples were then put in the 100°C oven for 8 days after which the metallization was profiled to have a height of 400 Å; an increase in thickness of approximately 75Å. If these observations were accurate, as were believed to be, this is significant. The

apparent increase in gold thickness is attributed to solvent evaporation out of the Cytop substrate causing bulging of the waveguides upwards, observed and discussed also by [30]. If this is indeed the case, then is would suggest that an extended solvent evaporation after the lower cladding application and prior to the lithographic stage would be of benefit to reducing possible waveguide deformation.

2.1.5 Upper Cytop Cladding Application and Baking

2.1.5.1 Cytop Characteristics: Glass Transition, Baking and Solvent

The upper Cytop cladding is applied to an 8μm thick layer of the Cytop lower cladding that has somewhat fragile gold metallization upon it. This substrate makes the preparation of the upper cladding more complicated than the rather benign activity of the lower cladding application directly on silicon, because of physical characteristics of Cytop and its solvent.

- Cytop has a glass transition temperature (Tg) of 108°C. If a layer of Cytop is subject to a temperature above Tg it will flow to an extent, and a thin metal on the surface will experience deformation as shown in Figure 23.
- Cytop does not permanently harden (through polymer cross-linking, or other chemical reaction). It is always susceptible to dissolution in its solvent. Hence, when the first layer of the upper cladding (containing solvent) is applied to the baked lower Cytop cladding (solvent free) upon which metal is patterned, the solvent will get underneath the metal; solvent ingress. If the sample is then heated too aggressively the solvent will degas out aggressively and deform the metallization, see Figure 24. Correspondence with the manufacturer indicates that a Cytop variety which hardens through chemical reaction or an additive to cause chemical reaction hardening of Cytop is not available.
- The Cytop solvent, CT SOLV 180, has low volatility with a boiling point of 180°C. This imposes the requirement of longer, thorough solvent evaporation periods.

These physical properties of Cytop then impose the following conditions on the application of the upper cladding:

- Extended baking times required, to drive off the low volatility solvent, since the baking temperature cannot exceed 108°C. As a precaution do not exceed 100°C
- Slow rates of temperature increase required to ensure ingress solvent is slowly released.

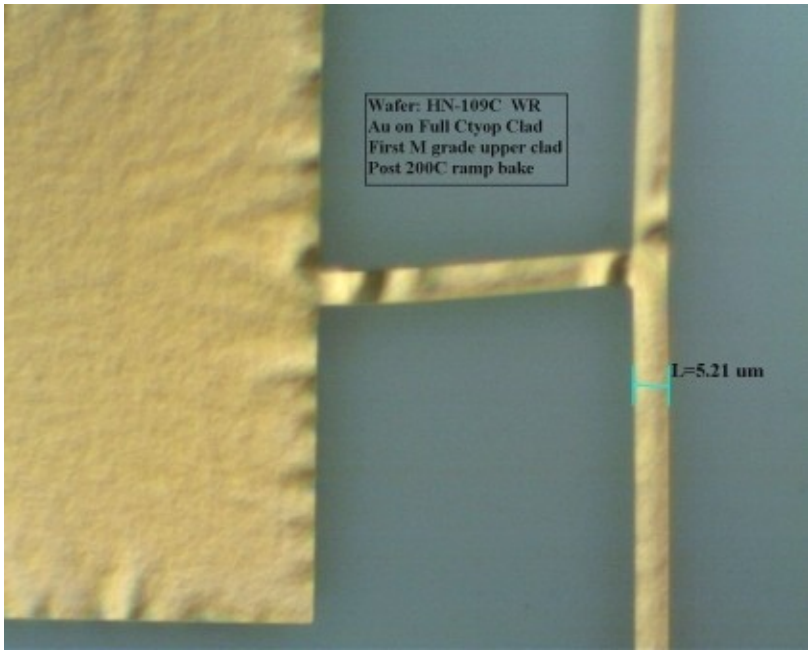


Figure 23: Metallization Damage Due to 200°C Bake
Four inch wafer with full Cytop lower cladding. Extensive cracking after first upper cladding layer applied and slow baked. Second layer slow ramp baked and then fast ramp from 70°C to 200°C and back to room temperature after which all Cytop cracking annealed.

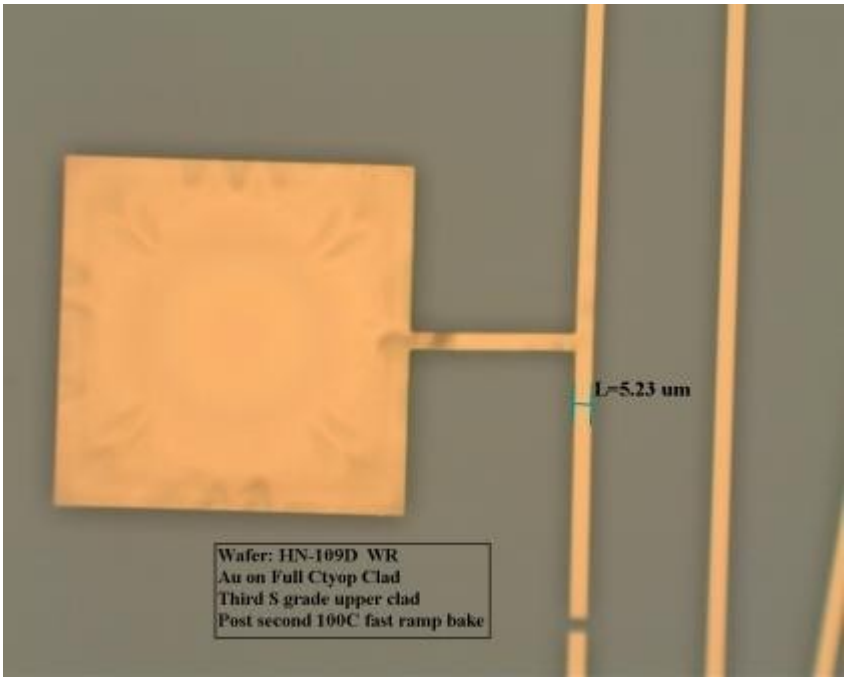


Figure 24: Metallization damage due to fast ramp bake to 100°C
Damage contributed to fast expulsion of ingress solvent.
Four inch wafer with full Cytop lower cladding and third upper cladding layer applied. Fast baked from 50°C to 100°C @ 50°C/hr. Cytop cracking also present.

2.1.5.2 Cytop Cracking

An additional critical and somewhat unresolved problem is that Cytop, upon drying, can crack; it effectively experiences mud cracking. Cracking is especially pronounced if contamination bits are included in the Cytop. Cytop cracking was common on 4-inch wafers where on 2-inch wafers cracking was found to be insignificant. The development of cracks in the upper cladding during the application procedure is problematic for two reasons:

- The cracking propagates downward to the lower cladding damaging the waveguides on the surface of the lower cladding, see Figure 25.
- Raising the temperature above Tg to flow the Cytop and anneal the cracking is not a viable option with the presence of waveguides.

The extent of the of the cracking was not such that all features were subject to damage. See Figure 26 for an example of a crack free feature showing good gold quality after application of the first upper cladding layer.

Attempts were made to address the cracking, without significant success, as follows.

- Using the existing upper cladding spin application procedures as defined by [30] [31] with different baking procedures as outlined in [34].
- Applying the existing lower cladding spin application procedure with different baking procedures as outlined in [34]. This unsuccessful procedure is summarized in Table F11 in Appendix F.

At the time of writing, a crack free upper cladding was being observed through the exclusive use of the first layer bake listed in Table 12 but with a reduced maximum temperature of 85°C. Other possible solutions for the cracking are presented as suggestions in the future work discussion in Section 4.2.

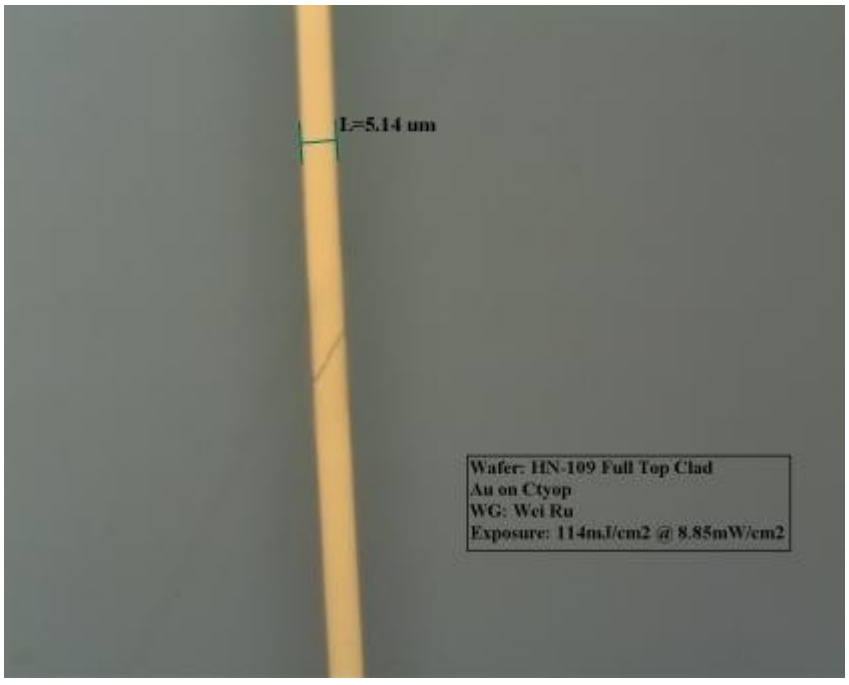


Figure 25: Metallization Damage Due to Cytop Cracking
After slow ramp bake of first lower clad layer. Four inch wafer with full Cytop lower cladding.

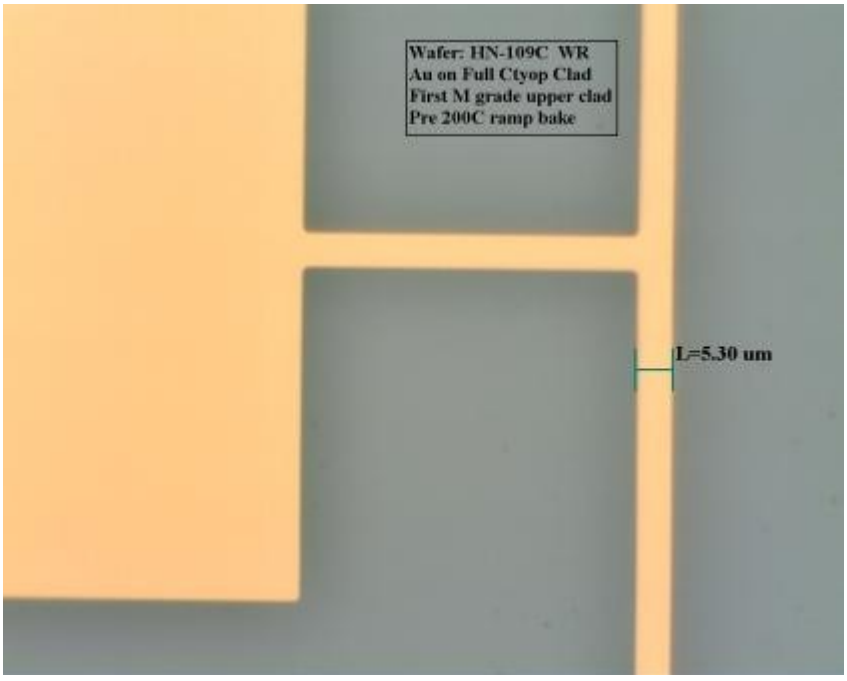


Figure 26: Metallization High Quality Gold After Long Slow Ramp Bake of First Upper Cladding Layer
On 4 inch wafer with full Cytop lower cladding. Sample has extensive cracking causing splitting in many waveguides rendering the wafer of too poor quality to continue to completion. Cracking occurred after first upper clad layer application.

2.1.5.3 Upper Cytop Cladding Application and Baking Summary

The upper cladding application procedure as outlined by [31] involved the application of 6 layers. This procedure was found, through SEM analysis, to give a total upper cladding thickness of 6µm. At least 8µm is required for the upper cladding thickness. A nine layer upper cladding process was thereafter used with a similar baking procedure to [31] and with post channel etch profilometry was found to provide a thickness of 9.2µm. This upper cladding application procedure, summarized in Table 12, gave low metal deformation from solvent ingress, yet was still prone to some cracking. Tabular

summaries of the lower and upper cladding application procedures as performed by [28] [30] [31] [42] and here are listed in Appendix F.

Table 12: Upper Cytop Cladding Application and Baking Summary

Upper Cytop Cladding Application Summary	
Activity	**Details**
Spin (all layers): 9% S-Grade Cytop	10 seconds @ 1000 rpm + 20 seconds @ 4000 rpm
Bake: 1st layer	50°C to 100°C @ 5°C/hr (more than 13 hours)
Bake: 2nd layer	50°C to 100°C @ 10°C/hr (more than 8 hours)
Bake: 3rd to 9th layers	(30 min @ 50°C) + (50°C to 100°C @ 25°C/hr) + (2 hours @ 100°C) or (if end of day in fabrication lab do an overnight bake) 50°C to 100°C @ 10°C/hr (more than 8 hours)
Optical examination	After each bake cycle: microscope surface analysis
Thickness	9.2µm (determined by etch depth)
Note: All baking performed on hot plate	

2.1.6 Channel Etch Mask Application and Lithography

The procedure for the application of the channel etch layer on to the upper Cytop cladding, and subsequent lithography, was adopted from [28] [30], and slightly modified through personal communication with Hassan [31]. The development of this procedure included consideration of upper cladding damage in the form of cracking. The procedure was not observed to cause cracking in the upper cladding. Table 13 summarizes the channel etch mask application and lithography.

Table 13 Channel Etch Mask Application and Lithography Summary

Channel Etch Mask Application and Lithography Summary	
Activity	**Details**
RIE roughening (March)	20 seconds for 2" waver, 30 seconds for 4" wafer
HMDS application	Oven at 98°C
Spin coat SPR-220	30 sec. @ 1000 rpm + 10 sec. @ 2300 rpm
SPR 220 out gassing	30 minutes @ room temperature
SPR 220 curing	room temperature to 100 °C + 15 min. @100°C + 100°C to room temperature
channel mask alignment	Align to waveguide mask alignment marks on wafer
channel mask exposure	870 mJ/cm^2
SPR 220 curing	sit at room temp overnight
SPR 220 curing	90 seconds @ 115°C
SPR 220 Development	MF-24A for 4 minutes (for H-line exposure of 870 mJ/cm^2)
Post development rinse	2 minutes immersion in DI water
Development inspection	Make absolutely sure channels are cleared of etch mask
Note: All curing performed on hot plate	

It is particularly critical that the channels are completely clear of SPR 220 in the channel mask preparation process; this can be tricky. A simple assessment of the extent of development is a hand held visual inspection that the channel features (when dry) are shiny, which indicates full clearing, not cloudy or fogged. Under UV filtered microscope inspection a number of observations can be of assistance in determining clearing of the PR:

- Look for the fringing. Fringing is a prismatic colouring due the refraction of light through thin residual PR near areas of full clearing. But, if the PR is not cleared down to the substrate at all, no fringing will be evident.
- The presence of cracks across the channels, observed as straight parallel straight lines, indicates fully undeveloped channels.
- Late in development, observe with microscope the edge of the wafer, at the thick SPR 220 edge bead. Move inward across the channels near the edge and fringing will be observed. Then, examine the central areas of the sample for the existence of similar fringing.

The SPR 22O layer is thick, approximately 10µm [28], and the channel feature dimensions area relatively large. Over development is not a great concern. Observation showed that from 1 minute to 5 minutes the channel edges were not observed to be degraded. A sample with a 2.5 minute development time was determined, through a

very unsuccessful channel etching effort, to have been significantly underdeveloped. Particular attention spent on the development of a later sample found 4 minutes development was required to fully clear the channels if exposed with energy of 870mJ/cm^2.

2.1.7 Channel Etching

The objective of the channel etching procedure is to remove particular areas of Cytop cladding and expose the underlying waveguides to a height of ideally 400nm. That is, etching through the entire thickness of the upper Cytop cladding, as applied with the procedure of Table 12, and 400nm into the lower cladding. Great care must be taken to avoid over etching during the channel etching procedure.

Channel etching was performed in the March RIE system using an O_2 flow 0f 220 sccm, a pressure of approximately 350 mTorr and various powers and duration. The etch rate in the March RIE chamber is assumed to be non-uniform. In an effort to evenly distribute the etching rate, etching at particular power and duration was done in a series of four etch runs. In each etch run of a series the sample was positioned at a different location in the etch chamber; north, east, south and west. The sample was always in the same orientation in each etch run. It is important that profilometer analysis of channel waveguide height is performed regularly during the etching procedure to ensure over etching does not occur. The etch procedure performed is given in Table 14. The times at which profilometry was performed during etching need not be limited to those listed. Final profilometer analysis, with the Tencor P-1 system at the Carleton fabrication facilities, showed an average channel etch depth of approximately 9.7µm, and a very good waveguide etch height distribution of

approximately 500nm over a 4" wafer. Photographs of the Tencor profilometer screen were not captured of the final results of the upper cladding etching activity.

Table 14 Channel Etch Sequence for an 9.7µm Cytop Etch Depth

Channel Etch Sequence for 9.7µm Cytop Etch Depth March RIE: O2 flow 220 sccm, Pressure 350 mTorr		
Etch Series	**Details**	**Location in Etch Chamber**
1 Total 100W-min = 16	2 minutes @ 200W	N
	2 minutes @ 200W	E
	2 minutes @ 200W	S
	2 minutes @ 200W	W
	Profilometer waveguide height examination	
2 Total 100W-min = 6	1.5 minutes @ 100W	N
	1.5 minutes @ 100W	E
	1.5 minutes @ 100W	S
	1.5 minutes @ 100W	W
	Profilometer waveguide height examination	
3 Total 100W-min = 3	45 seconds @ 100W	N
	45 seconds @ 100W	E
	Profilometer waveguide height examination	
	45 seconds @ 100W	S
	45 seconds @ 100W	W
	Profilometer waveguide height examination	
4, 5, 6, 7 Total 100W-min = 8	60 seconds @ 50W	N
	Profilometer waveguide height examination	
	60 seconds @ 50W	E
	Profilometer waveguide height examination	
	60 seconds @ 50W	S
	Profilometer waveguide height examination	
	60 seconds @ 50W	W
	Profilometer waveguide height examination	
Total power time = 33 100W-min		

If the total etching power and time is normalized to a unit of 100W-minutes it is found to be 33 100W-minutes. For a total etch depth of 9.7µm this gives the etch rate for the March RIE of 294nm per 100W-minute at an O_2 flow of 220 sccm. Note this value is an aggregate and was not believed to be linear in a power selection.

An additional etch rate test was performed on upper Cytop claddings applied as per Table 3 (the lower cladding application procedure). Three etch sequences resulted in a median etch depth of 8.5µm, and waveguide heights of approximately 500nm. Table E1 of Appendix E lists the etch procedure that generated the median etch depth (on sample HN-112). Normalizing the total etching power and time to a unit of 100W-minutes gives 27 100W-minutes for the etches. For a total etch depth of 8.5µm this gives the etch rate for the March RIE of 315nm per 100W-minute at an O_2 flow of 220 sccm. This etch sequence and the previous indicates the etch rate for Cytop is between 294nm and 315 nm per 100W-min (around 305nm per 100W-min). A value of 981nm per minute was determined by [28] for an O_2 flow of 100 sccm and at 200W power. Figure 27 and Figure 28 are screen photographs of the of the Tencor P-1 profilometer showing an exposed waveguide and etched channel (on sample HN-109).

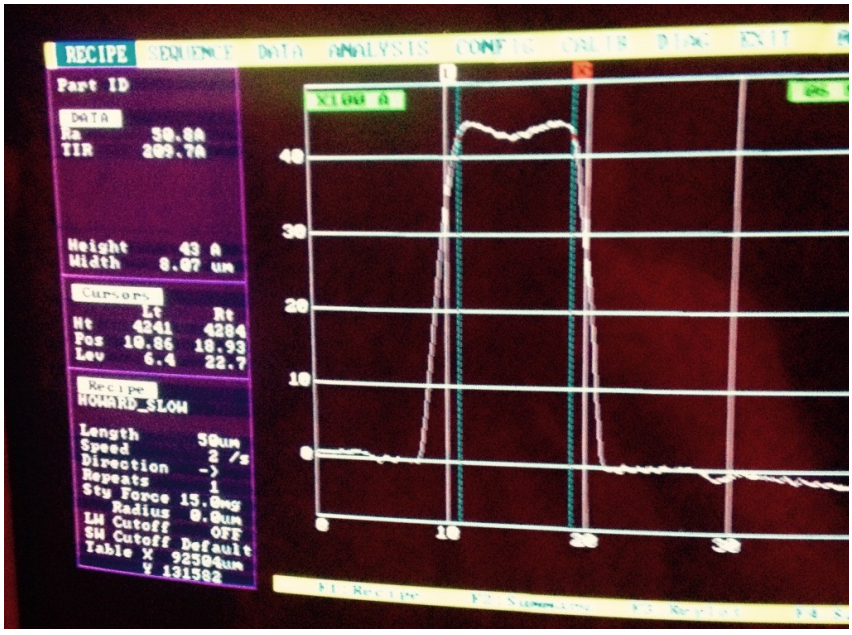


Figure 27: Profilometer Profile of an Exposed Waveguide
Waveguide etch height approximately 430nm. Profilometer display of the Tencor P-1 at the Carleton facilities.

2.1.8 Etch mask removal and Dicing Preparation; End of Fabrication

2.1.8.1 Etch Mask Removal

Once channel etching has successfully been accomplished the etch mask must be removed. This is a basic sequence of immersing in acetone, followed by IPA, followed by de-ionized water rinse, as described in [30] and discussed through private communication with Hassan [31].

Table 15 Channel Etch Mask Removal

Channel Etch Mask Removal	
Activity	**Details**
Acetone clean	Acetone bath at room temperature for 10 minutes
IPA clean	IPA bath at room temperature for 10 minutes
DI rinse	De-ionized water bath at room temperature for 10 minutes
DI flush	De-ionized water gun rinse for 1 minute
Sample dehydration	In oven for 15 minutes at 95°C to 100°C

2.1.8.2 Channel Depth Analysis

It is important to know the depth of the etched channels. Once the channel etch mask is removed a profilometer profile across a channel, or channel edge, gives the depth of the channel etch. Figure 28 shows the profilometer profile of an etched channel from the etching sequence of Table 14. The image is a photograph of the screen display of the Tencor P-1 profilometer at the Carleton fabrication facilities.

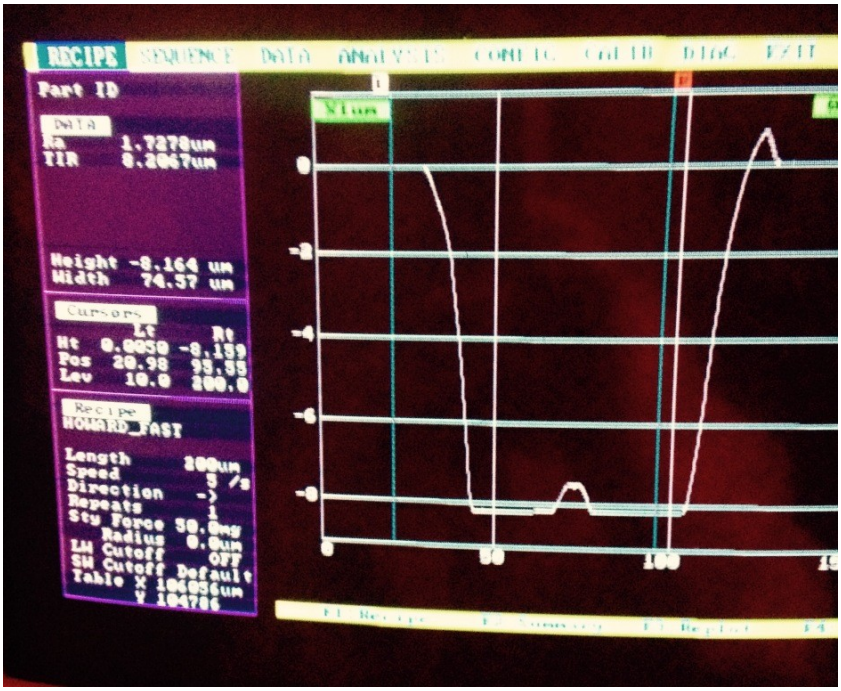


Figure 28: Profilometer Profile of an Etched Channel in Cytop
Channel etch depth indicates approximately 8.2µm. Note exposed waveguide at centre of channel. The wing on the top right of the channel is an artifact of the profilometer sensor rising out of the deep channel. Profilometer display of the Tencor P-1 at the Carleton facilities.

2.1.8.3 Dicing Preparation

Once the etch depth has been evaluated the sample must be prepared for dicing. This is a procedure of SPR 220 application and curing per [30].

Table 16 Dicing Preparation

Dicing Preparation	
Activity	**Details**
HMDS application	Oven at 98°C
Spin coat SPR-220	(30 sec. @ 1000 rpm) + (10 sec. @ 2300 rpm)
SPR 220 out gassing	30 minutes @ room temperature
SPR 220 curing	(room temperature to 100 °C) + (20 min. @100°C) + (100°C to room temperature)
Note: All curing performed on hot plate	

At this point the full Cytop LRSPP biosensor fabrication is concluded. The wafers are ready for packaging and delivery.

2.2 Summary

The fabrication procedure of gold stripe, step-in-width Bragg gratings on Cytop for an LRSPP optical biosensing device was performed. Through procedural refinements, repeatedly acceptable dimensions were accomplished for "C82" PPBG waveguides that have a grating step-in-width from 8µm to 2µm, and a period of 1690nm to 1800nm. For the PPBG waveguides to support and propagate LRSPP's the thickness and surface roughness of the gold is important. Repeatedly achieved was an appropriate gold thickness of 35nm±5% and surface roughness of better than 2nm rms and average. The activity was a refinement of the previous optical biosensor fabrication procedures of [28] [29] [30] that, as documented, were found not to resolve the very fine dimensions or give the metal quality required for LRSPP Bragg waveguides. Samples using the Biosensor and New Biosensor mask patterns were also produced on a Cytop substrate with very good quality.

Persistent cracking of the upper Cytop cladding resulting in waveguide damage was, at the time of writing, preventing the production of a top quality product for device behaviour quantification. As a result, PPBG on Cytop characterization analysis is not included in this thesis, though the cracking of the Cytop upper cladding was being addressed and encouraging results were being observed. A solution to the waveguide damage, due to cracking of the upper Cytop cladding, is a rigid lower cladding, onto which the gold waveguide patterning is deposited. This is achieved through the use a rigid “multilayer” substrate of alternating Ta_2O_5/SiO_2 and is discussed in Chapter 3.

3.0 Fabrication of Bragg waveguides on Ta_2O_5/SiO_2 Multilayer Wafer Overview

The Ta_2O_5/SiO_2 multilayer wafer, hereafter referred to as "multilayer wafer", is an alternative substrate wafer introduced as an effort to simplify the full Cytop based LRSPP biosensor fabrication procedure discussed in the previous chapter. Effectively, the lower cladding is replaced by a multilayer stack of alternating Ta_2O_5 and SiO_2 layers. This architecture is not subject to some of the fabrication difficulties inherent in the full Cytop design.

The individual stages in the fabrication of a multilayer based LRSPP biosensor device are illustrated in Figure 29 and Figure 30. The stages are further discussed in the following sections of the chapter. This multilayer LRSPP biosensor fabrication procedure is adapted from the full Cytop based LRSPP biosensor fabrication procedure of chapter 2.

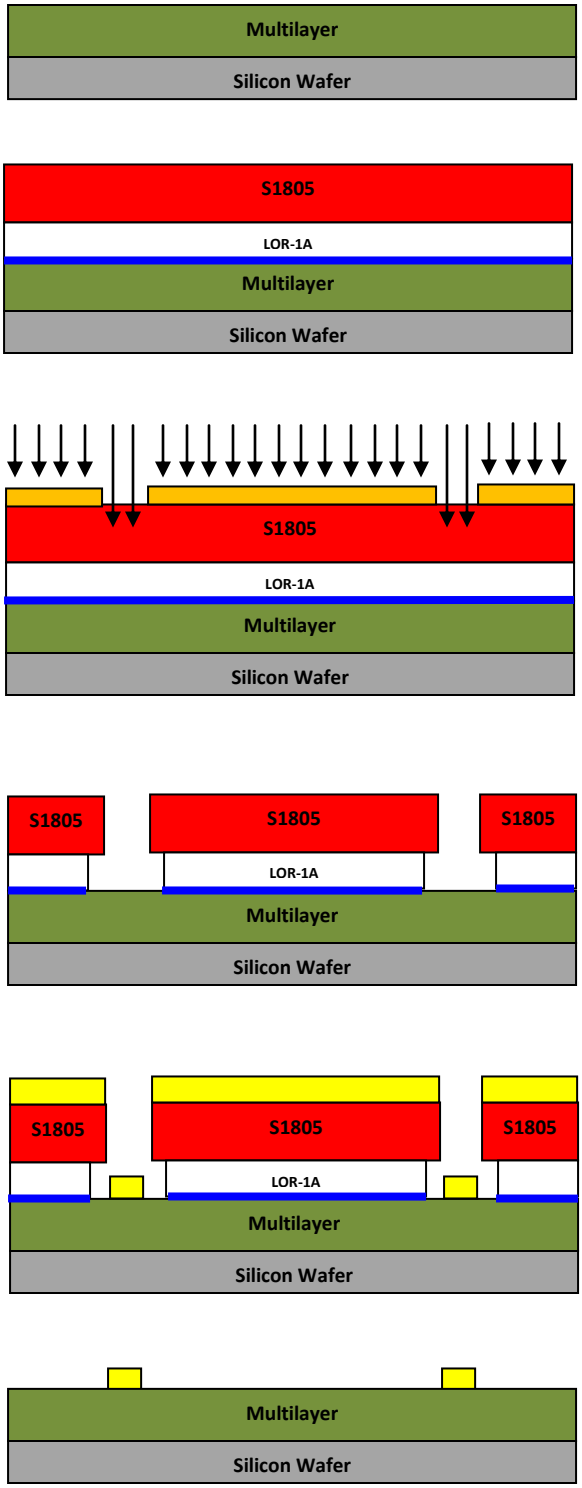
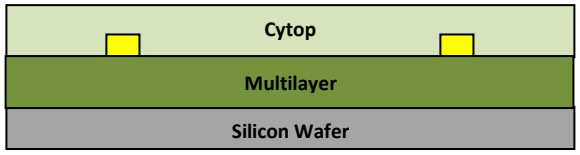
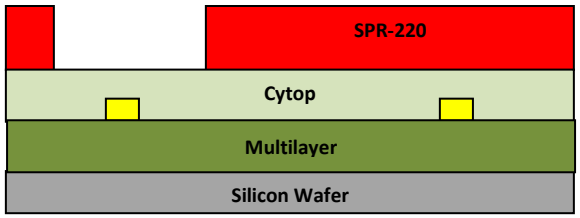


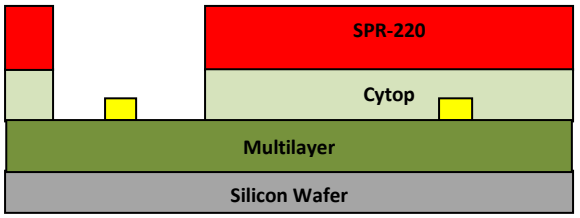
Figure 29: Multilayer Based LRSPP Biosensor Device Fabrication Process



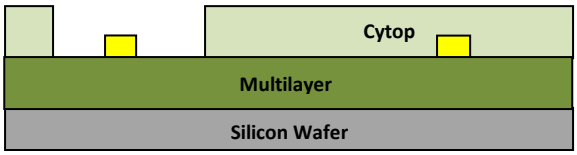
4) Upper Cytop cladding application and curing



5) Channel etch mask: photoresist application, exposure and development



6) Channel cavity etching



7) Etch mask removal; End of Fabrication

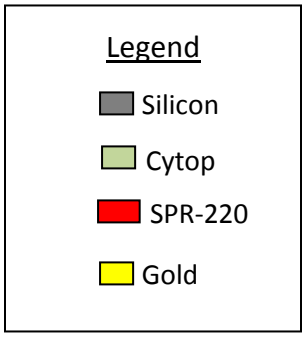


Figure 30: Multilayer Based LRSPP Biosensor Device Fabrication Process continued

3.1 Fabrication Details

3.1.1 Multilayer Wafer Selection and Preparation

3.1.1.1 Multilayer Wafer Selection

The multilayer wafers used in this project were custom manufactured by Iridian Spectral Technologies, Ottawa, Canada specifically for the biosensor project. For biosensor multilayer fabrication, the multilayer wafer is specifically the only type of substrate wafer used. As a quality check another 4-inch silicon sample was always processed concurrently with the multilayer wafer.

3.1.1.2 Multilayer Wafer Preparation

Preparing the chosen silicon wafer for use involves labelling and surface cleaning.

The multilayer wafer labelling procedure was exactly as described in Section 2.1.1.2. This procedure was performed with special care, as well as all other stages of the multilayer fabrication, as these wafers are expensive.

Hydrofluoric acid cleaning must not be performed on the multilayer wafers. HF will damage the Ta_2O_5/SiO_2 multilayer.

The only surface preparation activity performed on the multilayer wafer was oxygen plasma cleaning. The procedure was exactly as described in Section 2.1.1.2.

3.1.2 Lower Cytop Cladding Application and Baking

The multilayer wafers do not need a Cytop lower cladding. The Ta_2O_5/SiO_2 multilayer stack of the multilayer wafer optically substitutes as the lower Cytop cladding previously applied on the full Cytop LRSPP biosensor product.

3.1.3 Lithography

3.1.3.1 Bi-Layer Application, Exposure and Development

For multilayer wafers the lithographic bi-layer was applied directly to the multilayer surface. The lithographic procedure for the multilayer process was exactly the same as for the Cytop lower clad process of Section 2.1.3, except roughening of the surface of the multilayer substrate was not required and a descum was performed. To account for back reflection during exposure, the (lower) H-line energy of 114mJ/cm^2 was used, and was found to give very acceptable features.

3.1.3.2 Lithographic Pattern Cleaning: Descum

After lithographic development some residual PR and LOR may remain in the lithographic channels. This contamination can adversely affect metal quality of the subsequent deposition. The contamination can be removed by RIE, termed a “descum”. Prior to loading the multilayer samples into the metal deposition system an RIE was performed with a Technics Planar Plasma Etcher for 60 seconds at 100W power. A descum cannot be performed on the Cytop lower clad devices as the etching adversely affects the Cytop substrate [28] [29].

3.1.3.3 Multilayer Bi-Layer Lithography Procedure Summary

Table 17 summarizes the bi-layer lithography procedure for multilayer wafers.

Table 17 Multilayer Bi-Layer Lithography Procedure Summary

Multilayer Bi-Layer Lithography Procedure Summary	
Action	**Details**
HMDS application	HMDS oven at 98°C
LOR-1A pipette dispensing	Cover entire wafer with LOR-1A solution
LOR-1A spin coat	(10 sec. @1000 rpm) + (30 sec. @ 4000 rpm)
LOR-1A Bake	Hot plate for 3 minutes @ 180°C
S1805 Pipette dispensing	Cover entire wafer with S1805 solution
S1805 spin coat	(10 sec. @1000 rpm) + (30 sec. @ 4000 rpm)
S1805 bake	Hot plate for 3 minutes @ 115°C
UV expose (H-line)	114mJ/cm^2 (H-line)
MF-321 development	60 seconds
DI rinse and Nitrogen dry	2 minutes DI immersion + DI spray gun rinse + Nitrogen gun blow dry
Optical examination in UV filtered environment	At 500x magnification: look for proper lithographic development; features and undercut
Descum	60 seconds @ 100W

3.1.4 Metallization: Deposition and Lift-Off

3.1.4.1 Deposition

The metal deposition procedure for the multilayer process was almost the same as for the Cytop lower clad process. The only, but important difference was that a thin chrome layer for adhesion was always required prior to gold deposition since the deposition substrate was SiO_2. For the metal deposition procedural details refer to Section 2.1.4.1. Table 18 summarizes the gold deposition procedure for multilayer wafers.

Table 18 Multilayer Thermal Gold Deposition with Rotation Mounting Summary

Multilayer Thermal Gold Deposition with Rotation Mounting Summary	
Activity	**Details**
Important set up particulars	Zero deposition thickness on controller. Start rotation.
Burn in and stabilization	(65 volts for 1 min.) + (53 volts for 1min.) + open shutter
Chrome deposition[1] (set material on controller)	Deposition rate of 3 Å @ 0.1 Å /sec. Tooling factor = 188
Important set up particulars	Zero deposition thickness on controller.
Burn in and stabilization	(65 volts for 1 min.) + (53 volts for 1min.) + open shutter
Gold deposition (set material on controller)	Deposition rate of 350Å @ 0.1 Å /sec. Tooling factor = 188
[1] A chrome layer is always required for gold adhesion on the multilayer wafer	

3.1.4.2 Lift-Off

The lift-off procedure for the multilayer process is exactly the same as for the Cytop lower clad process of Section 2.1.4.2. Refer to Table 11 for the lift-off procedure summary for multilayer wafers.

3.1.4.3 Post Lift-Off Optical Analysis and Waveguide Height Analysis

Post lift-off, and prior to starting the application of the upper cladding, an optical examination should be performed and the waveguide thickness should be determined through profilometry. Refer to Sections 2.1.4.3 and 2.1.4.4 for details of the procedures. Figure 31, Figure 32, Figure 33, Figure 34 and Figure 35 show typical Bragg waveguide quality on the multilayer wafer. The high quality of the resolution of the C83, C84, C85, C52 and C53 Bragg gratings were not concurrently observed with the Cytop based samples. This was qualitatively attributed to:

- the absolutely consistent thickness of the multilayer stack on which the lithography is performed making the amount of exposure back reflection consistent across the wafer.
- Different (lower) reflective properties of the wafer that reduces back reflection.

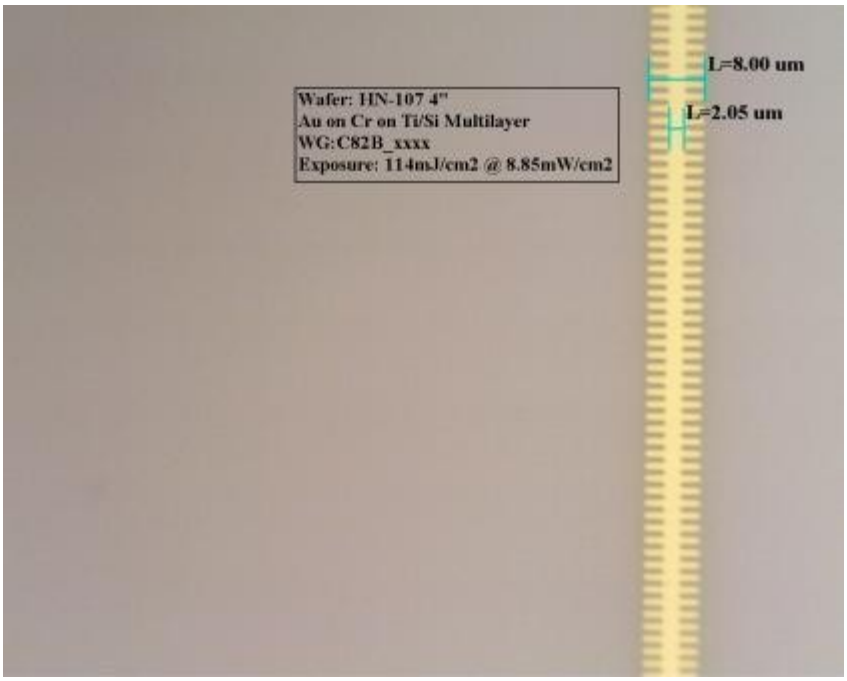


Figure 31: C82B Bragg Waveguide on Multilayer Wafer

Very good grating dimensions. Bi-Layer Lithography with S1805 and LOR-1A. Exposure of 114mW/cm^2. Development in MF321 for 60 seconds.

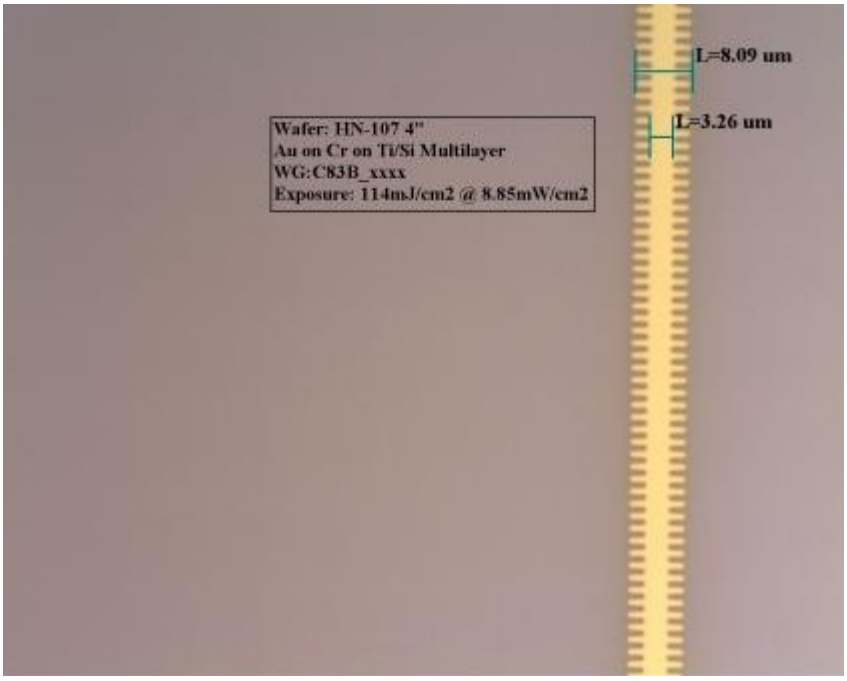


Figure 32: C83B Bragg Waveguide on Multilayer Wafer

Good grating dimensions. Bi-Layer Lithography with S1805 and LOR-1A. Exposure of 114mW/ cm^2. Development in MF321 for 60 seconds

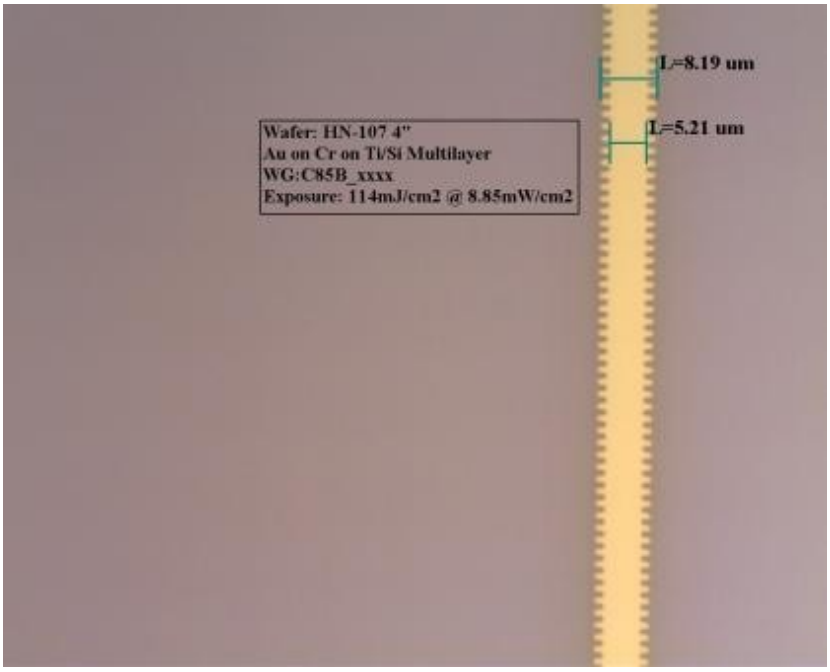


Figure 33: C85B Bragg Waveguide on Multilayer Wafer
Good grating dimensions. Bi-Layer Lithography with S1805 and LOR-1A. Exposure of 114mW/cm^2. Development in MF321 for 60 seconds.

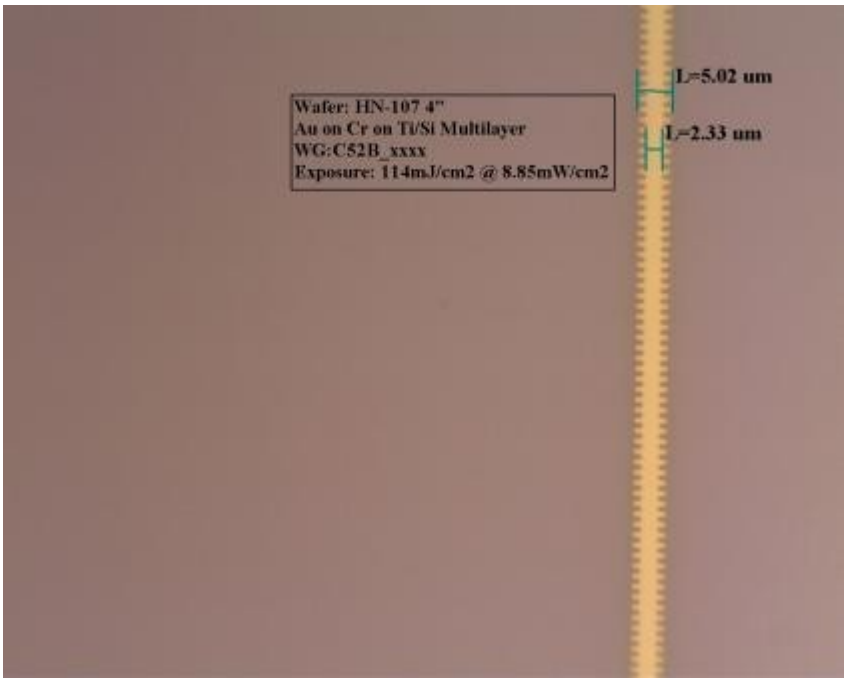


Figure 34: C52B Bragg Waveguide on Multilayer Wafer
Good grating dimensions. Bi-Layer Lithography with S1805 and LOR-1A. Exposure of 114mW/cm^2. Development in MF321 for 60 seconds.

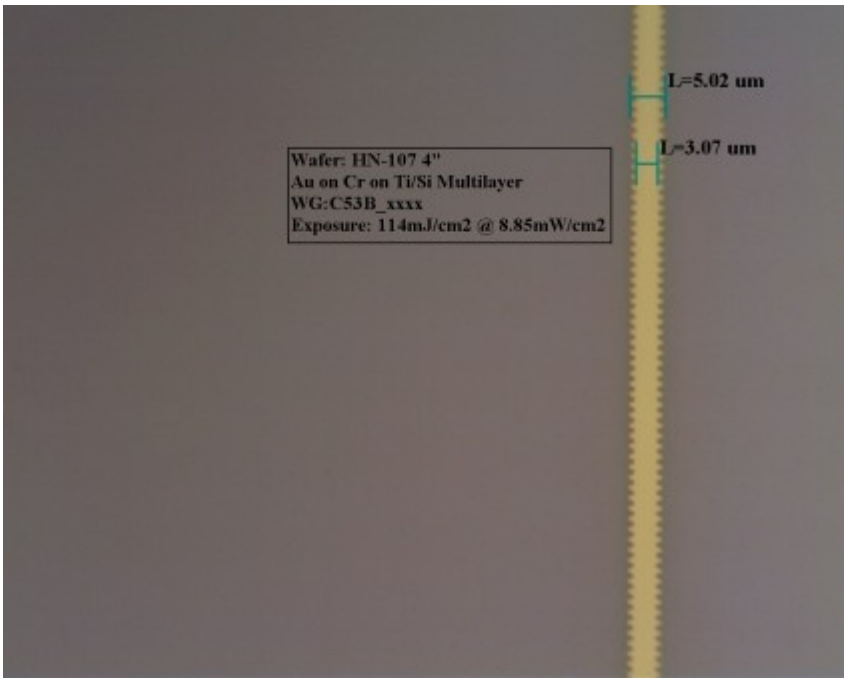


Figure 35: C53B Bragg Waveguide on Multilayer Wafer
Fair grating dimensions. Bi-Layer Lithography with S1805 and LOR-1A. Exposure of 114mW/cm^2. Development in MF321 for 60 seconds.

3.1.5 Upper Cytop Cladding Application and Baking

The application of a Cytop cladding over the waveguides is required in the multilayer fabrication process to realize LRSPP waveguides. It is at this stage of the process that the rigid Ta_2O_5/SiO_2 multilayer stack is a particular benefit. The multilayer stack on which the waveguide metallization resides:

- Does not flow (at 200°C).
- Is not susceptible to cracking.
- Is not susceptible to Cytop solvent ingress.

With the relaxation of these “Cytop” restrictions, the lower cladding application procedure of Section 2.1.2 was used to apply the multilayer Cytop cladding and excellent results were achieved. As an additional simplification, the edge bead removal step was omitted since the Cytop cladding was not to be patterned with detailed lithography therefore not requiring optimal mask contact during later exposure. Table 19 summarizes the Cytop upper cladding application procedure for multilayer wafers. A quick 50x optical examination of the wafer after every baking is suggested to monitor the cladding integrity; no inclusions (bubbles), contamination, and associated cracking. The Cytop cracking is less of a concern here since a final 200°C bake is permissible and any cracks that may occur in the Cytop are annealed.

Table 19 Multilayer Upper Cytop Cladding Preparation Summary

Multilayer Upper Cytop Cladding Preparation Summary	
Activity	**Details**
Layer 1 Spin coat 5% diluted M grade Cytop	10 sec@500 rpm/20 sec@1000 rpm
Baking	50°C for 30 min
Layer 2 Spin coat 9% S grade Cytop	10 sec@1000/20 sec@1500 rpm
Baking	50°C for 30 min
Layer 3 Spin coat 9% S grade Cytop	10 sec@1000 rpm/20 sec@1500 rpm
Baking	50°C for 30 min
Layer 4 Spin coat 9% S grade Cytop	10 sec@1000 rpm/20 sec@1500 rpm
Baking	50°C for 30 min
Layer 5 Spin coat 5% diluted M grade Cytop	20 sec@1000 rpm
Baking	50°C to 200°C @ 10°C/hr for minimum 18hrs

3.1.6 Channel Etch Mask Application and Lithography

The application of the channel etch layer and lithography is exactly the same as for the full Cytop process of Section 2.1.6. Again, a particularly important aspect of this stage is to ensure that the channels are completely cleared of PR after development. Refer to Table 13 for a summary the multilayer channel etch mask application and lithography procedure.

3.1.7 Channel Etching

The channel etching procedure is greatly simplified since the metallization resides on a layer of SiO_2 which is not etched by the oxygen RIE. Effectively the metallization is on an etch stop. The great care required when the waveguides are on a Cytop layer is relaxed. Subjecting the sample to at least 27.0 100W-minutes per Section 2.1.7 was used as an initial etching guideline. Table 20 summarizes the multilayer channel etching sequence used. One possible source of error here could be etching for an extended time and etching away the 10µm thick channel etch mask. This was not performed nor was the time required to do this quantified.

Table 20 Multilayer Upper Cladding Channel Etch Sequence

Channel Etch Sequence for Multilayer Upper Cladding March RIE: O2 flow 220 sccm, Pressure 350 mTorr		
Etch Series	**Details**	**Location in Etch Chamber**
1	4 minutes @ 200W	N
	4 minutes @ 200W	E
	4 minutes @ 200W	S
	4 minutes @ 200W	W
	Profilometer waveguide height and channel depth examination	

3.1.8 Etch mask removal and Dicing Preparation; End of Fabrication

Etch mask removal and dicing preparation is exactly the same as for the full Cytop devices. See Section 2.1.8 for the etch mask removal and dicing preparation procedure.

Figure 36 and Figure 37 illustrate a typical pre and post-etch surface of the same location on a multilayer wafer. There is no observable difference in the images except for the etched channel in the upper left of Figure 37.

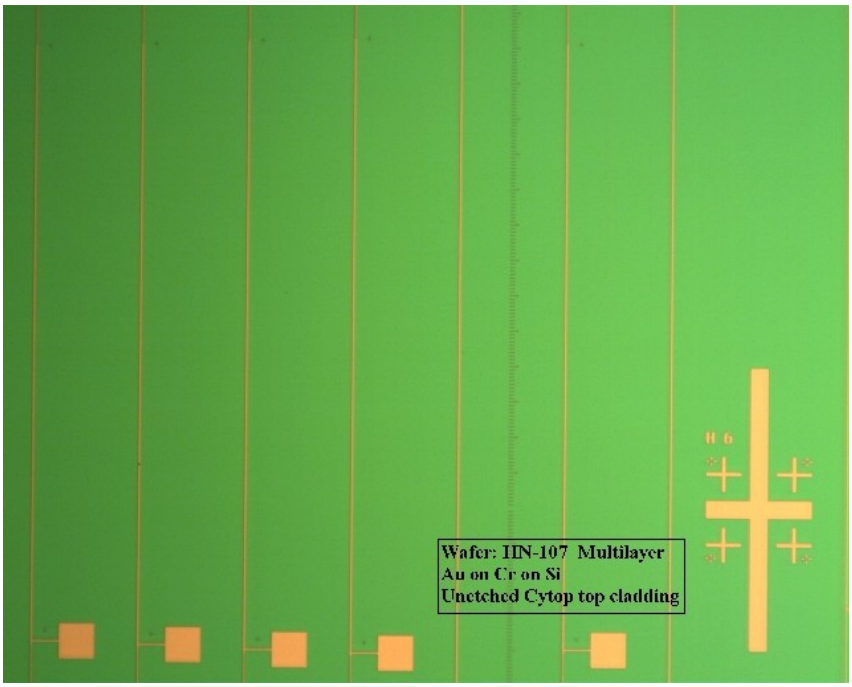


Figure 36: Multilayer Wafer Showing Good Pre-Etch Quality Cytop
Bi-Layer Lithography with S1805 and LOR-1A. Exposure of 114mW/cm^2. Development in MF321 for 60 seconds.

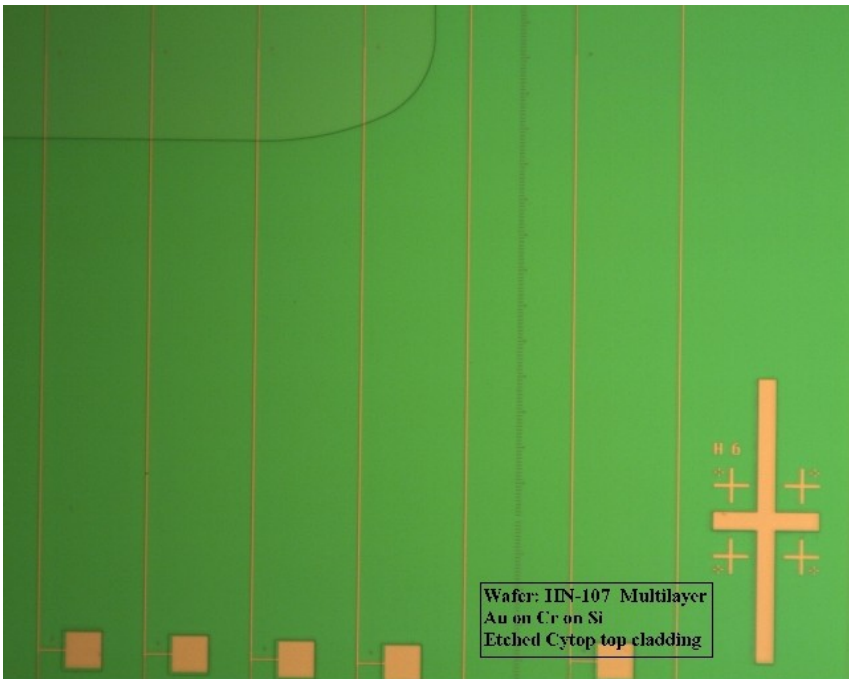


Figure 37: Multilayer Wafer Showing Good Post-Etch Quality Cytop
Bi-Layer Lithography with S1805 and LOR-1A. Exposure of 114mW/cm^2. Development in MF321 for 60 seconds.

Figure 38 and Figure 39 illustrate the pre and post-etch surface of the same location of a multilayer wafer. In Figure 39 there is clearly Cytop cracking generated in the etching process nucleated from a bit of contamination. This was the only cracking observed on the sample, yet it shows the multilayer process is not completely immune to Cytop cracking

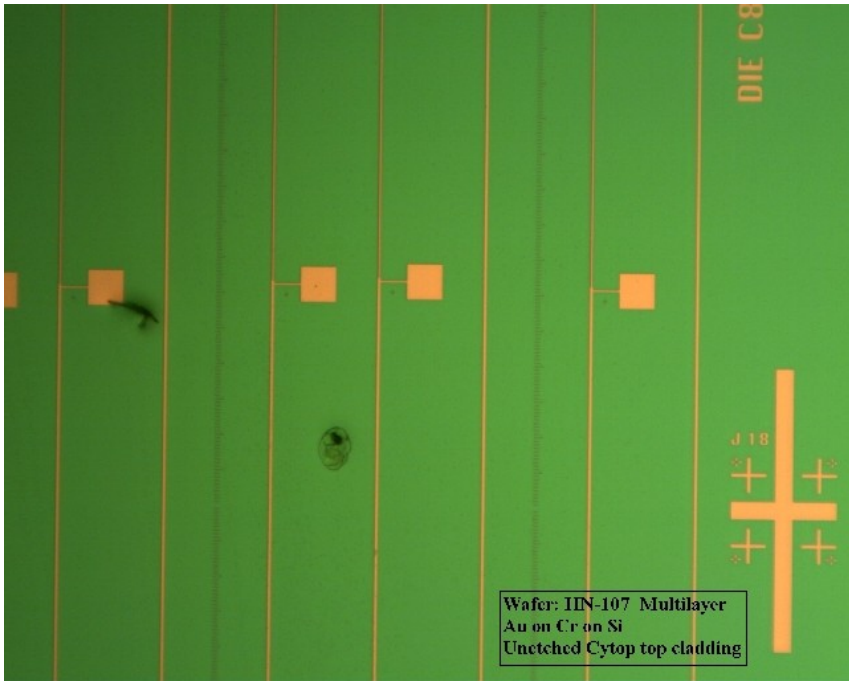


Figure 38: Multilayer Wafer Pre-Etch Showing Surface Contamination

Bi-Layer Lithography with S1805 and LOR-1A. Exposure of 114mW/cm^2. Development in MF321 for 60 seconds.

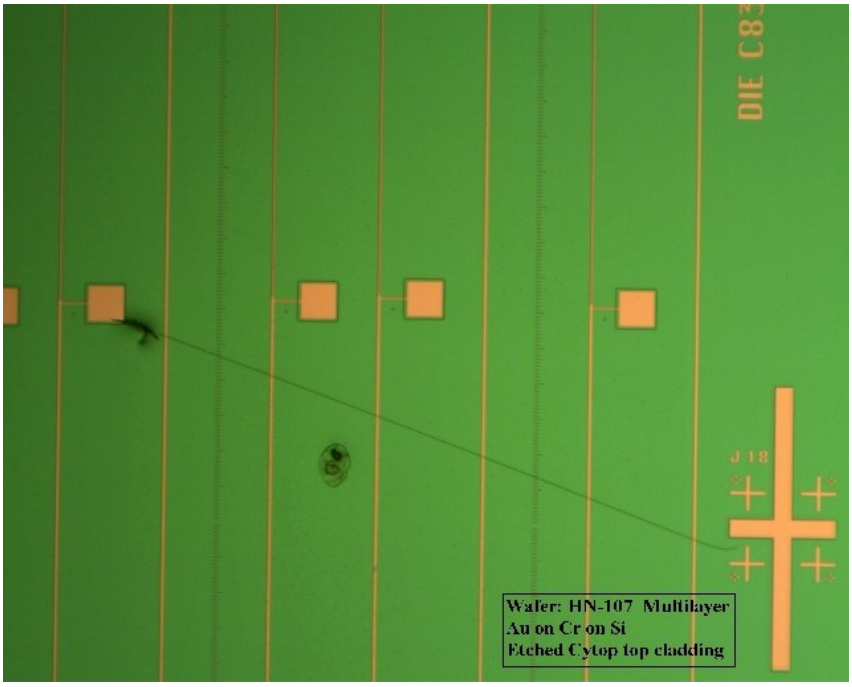


Figure 39: Multilayer Wafer Post-Etch Showing Surface Contamination Nucleating Cytop Cracking

Bi-Layer Lithography with S1805 and LOR-1A. Exposure of 114mW/cm^2. Development in MF321 for 60 seconds.

3.2 Summary

The fabrication of an LRSPP optical biosensing device on a multilayer substrate of alternating Ta_2O_5/SiO_2 was performed. Achieved was a very good quality of the C82 Bragg gratings and acceptable quality for all other Bragg gratings, except C54 which could not be resolved. Concurrently acceptable resolution of different dimension Bragg waveguide gratings was not observed on the full Cytop product and is qualitatively attributed to different (reduced) back reflection properties of the multilayer substrate to the UV exposure radiation and additionally the very planar quality of the multilayer. Samples using the Biosensor and New Biosensor mask patterns were also produced on the multilayer substrate with very good quality.

The use of a multilayer substrate introduced significant fabrication process simplifications and product quality improvements over the use of Cytop as substrate. Since the gold waveguides reside on a rigid, hard, SiO_2 surface:

- Cracking of the upper Cytop cladding did not result in waveguide damage.
- Cracking of the upper Cytop cladding could be annealed by a high temperature bake.
- Exposure of waveguides through etching was greatly simplified.

The multilayer wafer has introduced an undesirable side effect of the dicing procedure. Dicing by saw is performed by an external service and results in device end facets that are rough and chipped. The rough facets make it difficult to prepare the device for end-fire coupling required for the LRSPP excitation of the Bragg waveguides and characteristic testing. As such, characterization analysis of PPBG's on multilayer substrate is not included in this thesis. This complication is being actively worked at the time of writing.

4.0 Conclusions and Future Work

4.1 Conclusions

4.1.1 Cytop Based LRSPP Biosensor Fabrication

This project involved refining stages of previous Cytop based LRSPP biosensor fabrication methods documented in [28] [29] [30] [31]. The efforts resulted in two significant successful outcomes.

- Lithography: the resolution of C82B Bragg gratings can, with high quality and repeatability, be generated on an 8µm thick Cytop layer with a bi-layer lithographic fabrication method.
- Deposition: the deposition of gold to a tolerance of 35nm±5% with an acceptable surface roughness quality, of less than 2nm rms and average, was achieved through thermal vacuum chamber deposition.

The lithographic parameters to acceptably resolve the C52, C53, C83, C84 and C85 dimensions were not determined, but will be close to those that realize C82 gratings. It is concluded that the C54 gratings cannot be resolved with the lithographic capabilities of the Carleton fabrication facilities. The process parameters that resolve the C82 grating also resolve the features of the Old Biosensor and New Biosensor (Wei Ru) masks extremely well.

Later stages in the fabrication have persisting process challenges:

- Upper cladding application: cracking of the Cytop during the application of the upper cladding was observed. Cracking is undesirable as it damages the existing waveguides. The Cytop cracking occurred even with a lengthy procedure of multiple applications of thin layers and long baking times, see Table 12.
- Channel etching: avoiding over etching into the lower Cytop cladding during the channel etch procedure. This is a very delicate activity.

4.1.2 Multilayer Based LRSPP Biosensor Fabrication

An additional activity was to fabricate the LRSPP biosensor devices on Ta_2O_5/SiO_2 multilayer stack wafers. With very minor alteration of the refined Cytop based fabrication method, the fabrication of multilayer based devices was achieved, with greater ease and very acceptable quality. The multilayer fabrication process offers at least a time saving of six days in Cytop application, and the material cost saving of a lower Cytop cladding. The net cost difference this realizes, when the price of the multilayer is considered, has not been quantified.

4.1.3 General Concluding Comments

The bi-layer lithography and deposition refinements to produce acceptable Bragg grating features involved close attention to narrow tolerances, equipment operation subtleties and process execution details.

- Specific type of bi-layer materials used.
- Application method and curing times of bi-layer materials used.
- Temperatures; of curing hot plates and HMDS application oven.
- Amount of UV exposure; ± 0.5 mJ/cm^2.
- Lithographic development procedure; agitation method and immersion time.
- The operational procedure used with the metal deposition system.
- The lift-off procedure.

4.2 Future Work

4.2.1 Cytop Based LRSPP Biosensor Fabrication

Suggested future lithography efforts would be:

- Identifying the bi-layer lithography parameters to resolve the finer Bragg gratings of the C52, C53, C83, C84, and C85 waveguides. This may include testing with a bottom anti reflective coating (BARC) applied to the silicon wafer substrate.
- Resolving of the finest Bragg gratings C54. Required here would be lithographic techniques using shorter exposure wavelengths or a completely alternative e-beam lithography.

Thorough analysis of the problem of Cytop cracking during upper cladding application is required. To identify a time effective procedure that results consistently in both no cracking and no waveguide deformation during upper cladding application would be extremely valuable. This would require a focused analysis of the effects of different upper cladding application parameters such as temperature ramp times and lengths of baking. A suggestion is to try drier Cytop, especially for the first and maybe second layer application of the upper cladding. The Asahi Cytop catalogue [43] lists only the availability of 7% and standard 9% Cytop by weight. A higher concentration would have to be special ordered or prepared. The less solvent in the application layer it is assumed:

- would tend to cause less solvent ingress into the existing Cytop layer below and less likely to cause waveguide deformation during baking
- would lend to less of a propensity to crack during baking

To improve both the upper cladding application and channel etching procedures, pursue the development of a rigid, crack, and etch resistant top layer on the lower cladding. This would be the single solution to cracking damage and deformation of the metallization during upper cladding application, and over etching during the channel etch. This investigation was performed by [32] with reported fabrication success but with associated degradation of the optical characteristics of the devices.

4.2.2 Multilayer Based LRSPP Biosensor Fabrication

The fabrication process performed on the multilayer wafer substrate was considered very successful and no future fabrication work is identified as critical. As indicated in the Cytop based future work, a continuing activity applicable to the multilayer product would be to determine the lithographic parameters to better resolve the C52, C53, C83, C84 and C85 Bragg gratings.

5.0 References

[1] Cooper, J.C., Hall, E.A.H. “The nature of biosensor technology”, Institute of Biotechnology, University of Cambridge, November 1987

[2] Velasco-Garcia, M.N.” Optical biosensors for probing at the cellular level: A review of recent progress and future prospects”, Seminars in Cell & Developmental Biology, Volume 20, Issue 1, Pages 27–33, February 2009, Elsevier Ltd., 2009

[3] Zinoviev, K. E., González-Guerrero, A.B., Domínguez, C., Lechuga, L.M. ” Integrated Bimodal Waveguide Interferometric Biosensor for Label-free analysis”, Journal of Lightwave Technology, Vol. 29, Issue 13, pp. 1926-1930, 2011

[4] Lechuga, L.M. Modern Biospecific Analytical Techniques”, Chapter 5, Optical Biosensors, edited by L. Gorton , Elsevier Science, pp. 209-250, April 1, 2005

[5] Raether, H. "Surface Plasmons on Smooth and Rough Surfaces and on Gratings" (Springer, 1988).

[6] Homola, J., Yee, S. S., and Gauglitz, G. “Surface plasmon resonance sensors: review,” Sens. Actuators B 54, pp. 3-15, 1999.

[7] Nenninger, G. G., Tobiška, P., Homola, J., and Yee, S. S. “Long-range surface plasmons for high-resolution surface plasmon resonance sensors,” Sens. Actuators B 74, 145–151 (2001).

[8] Homola, J. "Present and Future of Surface Plasmon Resonance Biosensors, " Analytical and Bioanalytical Chemistry, vol. 377, pp. 528-539, 2003.

[9] Cooper, M. A., "Label-free screening of bio-molecular interactions", Anal Bioanal Chem 377:834–842, 2003.

[10] Homola, J, “Surface plasmon resonance sensors for detection of chemical and biological species”, Chem. Rev. (Washington, D.C.) 108, 462–493 (2008).

[11] Wijaya, E, et al., "Surface Plasmon Resonance-based Biosensors: From the Development of Different SPR Structures to Novel Surface Functionalization Strategies," Current Opinion in Solid State and Material Science, vol. 15, no. 5, pp. 208- 224, 2011.

[12] Berini, P. “Long-range surface plasmon polaritons”. Advances in Optics and Photonics Vol. 1, Issue 3, pp. 484-588, 2009.

[13] Boardman, A.D. “Electromagnetic Surface Modes”, Wiley, New York, 1982.

[14] Yang, F., Sambles, J.R., Bradberry, G.W. “Long-range surface modes supported by thin films”, Physical Review B, vol.44, no.11, p.5855, 1991.

[15] Burke, J.J., Stegeman, G.I. “Surface-polariton-like waves guided by thin, lossy metal films”, Physical Review B, vol.33, no.8, p.5186, 1986.

[16] Charbonneau , R., Berini, P, Berolo, E., Lisicka-Shrzek, E. “Experimental observation of plasmon-polariton waves supported by a thin metal film of finite width”, Optics Letters, Vol. 25, Issue. 11, 2000

[17] Gazzaz, K., Berini, P. “Theoretical biosensing performance of surface plasmon polariton Bragg gratings", APPLIED OPTICS, Vol. 54, No. 7, pp. 1673-1680, March 2015

[18] Asiri, H., Khan, A., Lisicka-Skrzek, E., Tait, R.N., Berini, P. “Fabrication of Surface Plasmon Waveguides in CYTOP”, Proc. of SPIE Vol. 8412 84120X-1 (2012)

[19] Chiu, C., Lisicka-Skrzek, E., Tait, R. N., Berini, P. "Fabrication of surface plasmon waveguides and devices in CYTOP with integrated microfluidic channels", Journal of Vacuum Science and Technology B, Vol. 28 (4), 729 - 735. (2010)

[20] Daviau, R., Khan, A., Lisicka-Skrzek, E., Tait, R.N., Berini, P. “Fabrication of surface plasmon waveguides and integrated components on Cytop”, Microelectronic Engineering 87, 1914–1921, (2010)

[21] Jetté-Charbonneau, S., Charbonneau, R., Lahoud, N., Mattiussi, G., and Berini, P. “Demonstration of Bragg gratings based on long-ranging surface plasmon polariton waveguides,” Opt. Express 13, 4674–4682 (2005).

[22] Yariv, A., Yeh, P. “PHOTONICS – Optical Electronics in modern Communications” 6th edition, Oxford University Press, 2007

[23] Krupin, O., Asiri, H., Wang, C., Tait, R.N., Berini, P. "Biosensing Using Straight Long-Range Surface Plasmon Waveguides", Optics Express, vol. 21, pp. 698-709 , 2013.

[24] Berini,P. "Plasmon-Polariton Waves Guided by Thin Lossy Metal Films of Finite Width: Bound Modes of Symmetric Structures," Physical Reviews B, vol. 61, pp. 10484- 10503, 2000.

[25] Fong, M., Tait, R.N., Berini, P. “Fabrication of surface plasmon waveguides on thin CYTOP membranes”, J. Vac. Sci. Technol. A, Vol. 27, No. 4, Jul/Aug 2009

[26] Konopsky, V. N., Alieva, E. V. “Long-range propagation of plasmon polaritons in a thin metal film on a one-dimensional photonic crystal surface,” Phys. Rev. Lett. 97, 253904 (2006).

[27] Delfan, A., Degli-Eredi, I., Sipe, J.E. "Long-range surface plasmons in multilayer structures", Journal of the Optical Society of America B, Vol. 32, No. 8, pp. 1615-1623, August 2015.

[28] Chiu, C. “Fabrication of Surface Plasmon Waveguide Devices in CYTOP with Microfluidic Channels”, M.A.Sc. Thesis, University of Ottawa, (2009)

[29] Daviau, R. “Fabrication of Surface Plasmon Waveguides on Cytop”, M.A.Sc. Thesis, University of Ottawa (2009)

[30] Asiri, H. “Fabrication of Surface Plasmon Biosensors in Cytop”, M.A.Sc. Thesis, University of Ottawa (2012)

[31] Hassan, S. “Microfabrication of Plasmonic Devices: PPBG Biosensor in Cytop, Intensity Modulator, and Atomically Flat Nanohole Array”, M.A.Sc. Thesis, University of Ottawa (2014)

[32] Hanif, R. “Microfabrication of Plasmonic Biosensors in CYTOP Integrating a Thin SiO2 Diffusion and Etch-barrier Layer”, M.A.Sc. Thesis, University of Ottawa (2011)

[33] Mack, C.A. “Fundamental Principles of Optical Lithography: The Science of Microfabrication”, Chapter 1, John Wiley & Sons, 2007.

[34] “Example of CYTOP Curing Conditions”, Technical Documents, AGC Chemicals Fluoroproducts Division, Asahi Glass Co. LTD, Tokyo, Japan.

[35] “LOR™ Lift-Off Resists”, MicroChem Corp., 2001

[36] G. Y. Yeom et al., "Plasma-Enhanced Chemical Vapor Deposition of SiO2 Thin Films at Atmospheric Pressure by Using HMDS/Ar/O2," Journal of the Korean Physical Society, Vol. 53, No. 2, August 2008, pp. 892-896

[37] "Lithography Trouble Shooter: Questions and Answers Around the Most Common Problems in Micro-Structuring", MicroChemicals GmbH, http:// www.MicroChemicals.eu, 2012

[38] "HMDS", Microchemicals GmbH, http://www.microchemicals.com/products/adhesion_promotion/hmds.html

[39] "CNS STANDARD OPERATING PROCEDURE SOP112: Lift-off Photoresist Processing", Harvard University, Centre for Nanoscale Technologies, http://wcam.engr.wisc.edu/Public/Reference/Lithography/Harvard%20CNS%20lift off%20and%20bilayer%20process.pdf, July 2011.

[40] "CNS STANDARD OPERATING PROCEDURE SOP093", Shipley 1800 Series Photoresist Processing, Harvard University, Center for Nanoscale systems, 2010.

[41] Mack, C.A. "Fundamental Principles of Optical Lithography: The Science of Microfabrication", Ch. 8, John Wiley & Sons, 2007.

[42] Banan, B., Tait, R.N., Liboiron-Ladouceur, O., Berini, P. "Fabrication of metal strip waveguides for microwave and optical transmission", submitted to J. Vac. Sci. Technol.

[43] "Amorphous Fluoroploymer CYTOP", Asahi Glass Co., Ltd, http://www.agccytop.com/, January 2009

Appendix A Summary of Wafers Processed

Table A1 Cytop Based Biosensor Wafer Summary		
Lithographic tests for Cytop-Gold adhesion improvement and Bragg Grating resolution		
Wafer (diam)	**Particulars Tested**	**Results Summary**
HN-1 (2”)	Cytop application testing (May 20, 2014)	Flip removing from spinner: End
HN-2 (2”)	Cytop application testing	Good. To be continued (TBC)
HN-3 (4”)	Cytop application testing	Broken during spinning: End
HN-4 (4”)	Altering development times	E-beam - over deposition: End
HN-5 (4”)	Altering development times	E-beam - over deposition: End
HN-6 (4”)	Existing fabrication procedure	Poor features. Processed to completion
HN-7 (4”)	Existing fabrication procedure	Wafer broken during dicing preparation
HN-8 (4”)	Existing fabrication procedure	Wafer broken during dicing preparation
HN-9 (4”)	Existing fabrication procedure	Poor features. Processed to completion
HN-10 (4”)	Existing fabrication procedure	Poor features. Processed to completion
HN-11 (4”)	Existing fabrication procedure	Poor features. Processed to completion
HN-12 (2”)	PMGI development time	No gold adhesion
HN-13 (2”)	MF-321 development time	No gold adhesion
HN-14 (2”)	MF-321 development time	Poor feature dimensions
HN-15 (2”)	MF-321 development time	Poor feature dimensions
HN-16 (2”)	MF-321 development time	Fair feature dimensions and good adhesion
HN-17 (2”)	MF-321 development time	Fair feature dimensions and good adhesion, SEM
HN-18 (2”)	MF-321 development time	Fair feature dimensions and good adhesion
HN-19 (2”)	MF-321 development time	Good feature dimensions and good adhesion
HN-20 (4”)	Current fabrication procedure	Fair C82B features. Processed to completion
HN-21 (4”)	Current fabrication procedure	Fair C82B features. Processed to completion
HN-22 to HN-26: no Cytop, no gold deposition		
HN-22 (2”)	S1805 only; development time	Good C82 lithographic features
HN-23 (2”)	S1805 only; development time	Good C82 lithographic features
HN-24 (2”)	S1805 only; development time	Good C82 lithographic features
HN-25 (2”)	S1805 only; development time	Good C82 lithographic features
HN-26 to HN-29: no Cytop, Au deposition on Silicon (generally poor gold adhesion)		
HN-26 (2”)	Existing lithographic procedure	Fair C82B gold features, poor lift-off
HN-27 (2”)	Existing lithographic procedure; no HMDS	Fair C82B gold features, poor lift-off
HN-28 (2”)	Existing lithographic procedure; LOR-1A	very good C82B gold features, very good lift-off
HN-29 (2”)	Existing lithographic procedure; descum	Fair C82B gold features, poor lift-off
HN-30 (2”)	Exposure and development times	Low exposure: underdeveloped
HN-31 (2”)	Exposure and development times	Low exposure: underdeveloped
HN-32 (2”)	Exposure and development times	Low exposure: underdeveloped
HN-33 (2”)	Exposure and development times	Low exposure: underdeveloped
HN-34 (2”)	PMGI non-ramped to high temp	PMGI ruined, no gold adhesion
HN-35 (2”)	PMGI non-ramped to high temp	PMGI ruined, no gold adhesion
HN-36 (2”)	PMGI non-ramped to high temp	PMGI ruined, no gold adhesion
HN-37 (2”)	PMGI non-ramped to high temp	PMGI ruined, no gold adhesion

Table A2
Cytop Based Biosensor Wafer Summary

Lithographic tests for Cytop-Gold adhesion improvement and Bragg Grating resolution

Wafer (diam)	Particulars Tested	Results Summary
HN-2 (2″)	PMGI baking and development time	No gold adhesion
HN-12 (2″)	PMGI baking and development time	No gold adhesion
HN-38 (2″)	MF-321 concentration & dev. Time	Poor gold adhesion, underdeveloped
HN-39 (2″)	MF-321 concentration & dev. Time	No gold adhesion
HN-40 (2″)	MF-321 concentration & dev. Time	Very poor gold adhesion, underdeveloped
HN-41 (2″)	MF-321 concentration & dev. Time	No gold adhesion
HN-42 (2″)	PMGI baking	Visibly poor post baking; reclaimed
HN-43 (2″)	PMGI baking	Visibly poor post baking; reclaimed
HN-44 (2″)	PMGI baking	Visibly poor post baking; reclaimed
HN-45 (2″)	PMGI baking	Visibly poor post baking; reclaimed
HN-2 (2″)	PMGI baking and development time	Gold adhesion poor, overdeveloped features
HN-12 (2″)	PMGI baking and development time	No gold adhesion
HN-41A (2″)	MF-321 development time	No gold adhesion
HN-41B (2″)	MF-321 development time	Overdeveloped, poor adhesion
Abandon PMGI for LOR-1A Sept 3, 2014		
HN-42 (2″)	Existing litho procedure with LOR-1A	Good lift off, underdeveloped (Bragg gratings)
HN-43 (2″)	Existing litho procedure with LOR-1A	Good lift off, underdeveloped (Bragg gratings)
HN-44 (2″)	Existing litho procedure with LOR-1A	Good lift off, underdeveloped (Bragg gratings)
HN-45 (2″)	Existing litho procedure with LOR-1A	Broken
HN-46 (2″)	Exposure time	Very Good lift off, underdeveloped
HN-47 (2″)	Exposure time	Very Good lift off, underdeveloped
HN-48 (2″)	Exposure time	Very Good lift off, underdeveloped
HN-49 (2″)	Exposure time	Very Good lift off, underdeveloped, SEM
HN-50 (4″)	Full current fabrication procedure	Very good features, high gold thickness
HN-51 (4″)	Full current fabrication procedure	Very good features, high gold thickness
HN-52 (2″)	Exposure energy, deposition (e-beam)	Underdeveloped, Gold: poor surface quality, ok thickness, AFM
HN-53 (2″)	Exposure energy, deposition (e-beam)	Underdeveloped, Gold: poor surface quality, ok thickness, AFM
HN-54 (2″)	Exposure energy, deposition (e-beam)	Underdeveloped, Gold: poor surface quality, ok thickness, AFM
HN-55 (2″)	Exposure energy, deposition (e-beam)	Underdeveloped, Gold: poor surface quality, ok thickness, AFM
HN-56 (2″)	deposition (e-beam) on silicon	Very poor gold adhesion
HN-57a (2″)	deposition (e-beam) on silicon	Very poor gold adhesion
HN-57b (2″)	deposition (e-beam) on silicon	Very poor gold adhesion
HN-58 (2″)	Exposure energy, deposition (e-beam)	Features: fair, Gold: poor quality, adhesion, thickness
HN-59 (2″)	Exposure energy, deposition (e-beam)	Features: fair, Gold: poor quality, adhesion, thickness
HN-60 (2″)	Exposure energy, deposition (e-beam)	Features: fair, Gold: poor quality, adhesion, thickness
HN-61 (2″)	Exposure energy, deposition (e-beam)	Features: fair, Gold: poor quality, adhesion, thickness
HN-62 (2″)	Exposure energy, deposition (“no spit”)	Features: good, Gold: poor quality, thickness
HN-63 (2″)	Exposure energy, deposition (“no spit”)	Features: good, Gold: poor quality, thickness, AFM

Table A3
Cytop Based Biosensor Wafer Summary

Tests for gold quality; roughness, thickness		
Wafer (diam)	**Particulars Tested**	**Results Summary**
HN-64 (2″)	Exposure energy, deposition (“no spit”)	Features: good, Gold: poor quality, thickness
HN-65 (2″)	Exposure energy, deposition (“no spit”)	Features: good, Gold: poor quality, thickness
HN-66 (2″)	Exposure energy, deposition (thermal)	Features: very good, Gold: poor thickness, AFM
HN-67 (2″)	Exposure energy, deposition (thermal)	Features: very good, Gold: poor thickness
HN-68 (2″)	Exposure energy, deposition (thermal)	Features: very good, Gold: poor thickness
HN-69 (2″)	Exposure energy, deposition (thermal)	Features: very good, Gold: poor thickness
HN-70 (4″)	Gold quality. No Cytop	very good features, over deposition, O.U. AFM
HN-71 (4″)	Gold quality. No Cytop	very good features, over deposition
HN-72 (2″)	Gold quality. No Cytop	very good features, over deposition, SSW AFM
HN-73 (2″)	Gold quality. No Cytop	very good features, over deposition, CU AFM
HN-74 (2″)	Gold quality. No Cytop	very good features, good thickness, CU AFM
HN-75 (2″)	Gold quality. No Cytop	very good features, good thickness, SSW AFM
HN-76 (2″)	Surface roughness: raw wafer	Sent to U.O for AFM
HN-77 (2″)	Surface roughness: post HF clean	Sent to U.O for AFM
HN-78 (2″)	Surface roughness: post plasma preen	Sent to U.O for AFM
HN-79 (4″)	Full current fabrication procedure	Very poor Bragg grating gold adhesion; discontinued
HN-80 (4″)	Full current fabrication procedure	Over etched channels; discontinued
HN-81 to HN-98: HMDS and LOR-1A application/interaction testing		
HN-81 (2″)	Post development bake	Very thin gold: incomplete LOR removal?
HN-82 (2″)	Post development bake	Very thin gold: incomplete LOR removal?
HN-83 (2″)	Cytop surface quality: post roughen	Sent to U.O for AFM
HN-84 (2″)	Cytop surface quality: no roughen	Sent to U.O for AFM
HN-85 (2″)	HMDS/LOR-1A: no HMDS	Poor LOR adhesion. Inconsistent feature dimensions. AFM
HN-86 (2″)	HMDS/LOR-1A: curing temperature	Poor LOR adhesion. Inconsistent feature dimensions
HN-87 (2″)	HMDS/LOR-1A: no HMDS	Poor LOR adhesion. Inconsistent feature dimensions. AFM
HN-88 (2″)	HMDS/LOR-1A: curing temperature	Poor LOR adhesion. Inconsistent feature dimensions
HN-89 (2″)	No lithography. Roughen only	Control sample. CU AFM
HN-90 (2″)	HMDS/LOR-1A: no HMDS	Very poor lithography; no LOR-1A adhesion
HN-91 (2″)	HMDS/LOR-1A: no mask exposure	No gold deposition. CU AFM
HN-92 (2″)	Standard current lithography	Excellent lithography. Insufficient gold. CU AFM
HN-93 (2″)	Pre and post HMDS curing, no roughening	No gold adhesion
HN-94 (2″)	Pre and post HMDS curing, no roughening	Very poor waveguide adhesion. CU AFM
HN-95 (2″)	Raw wafer surface roughness	CU AFM
HN-96 (2″)	HF cleaning surface roughness	CU AFM
HN-97 (2″)	HMDS: No oven; spin and bake	Very overdeveloped. CU AFM
HN-98 (2″)	HMDS: No oven; spin and bake	Very overdeveloped.
HN-99 (2″)	HMDS oven at 115°C	Overdeveloped. CU AFM
HN-100 (2″)	HMDS oven at 115°C	Overdeveloped.
HN-113 (4″)	Gold thickness: Au on Cr on Si	Deposition error
HN-114 (2″)	Gold thickness: Au on Cr on Si	Deposition error
HN-115 (2″)	Gold thickness: Au on Cr on Si	Deposition error

Table A4
Cytop Based Biosensor Wafer Summary

Upper cladding preparation tests and product samples

Wafer (diam)	Particulars Tested	Results Summary
HN-116 (4″)	Gold thickness: Au on Cr on Si	Rotation tooling factor 185; high deposition thickness
HN-117 (2″)	Gold thickness: Au on Cr on Si	Rotation tooling factor 185; high deposition thickness
HN-118 (2″)	Gold thickness: Au on Cr on Si	Rotation tooling factor 185; high deposition thickness
HN-119 (4″)	Gold thickness: Au on Cr on Si	Rotation tooling factor 195; low deposition thickness
HN-120 (2″)	Gold thickness: Au on Cr on Si	Rotation tooling factor 195; low deposition thickness
HN-121 (2″)	Gold thickness: Au on Cr on Si	Rotation tooling factor 195; low deposition thickness
HN-102 (4″)	Product: Bragg	Very poor Bragg grating adhesion. Discontinued
HN-103 (4″)	Product: Wei Ru mask	Excellent quality. Over channel etched. Discontinued
HN-108 (4″)	Upper clad baking: Bragg	Very poor adhesion of Bragg gratings. Discontinue
HN-109 (4″)	Upper clad baking: Wei Ru mask	Some Cytop cracking, waveguide damage. Delivered
HN-109A (4″)	Product: Wei Ru mask	Poor adhesion gold. Discontinued
HN-109B (4″)	Product: Wei Ru mask	Poor adhesion gold. Discontinued
HN-109B2 (4″)	Product: Wei Ru mask	Contaminated lower cladding. Discontinued
HN-109B3 (4″)	Product: Wei Ru mask	Contaminated lower cladding. Discontinued
HN-109C (4″)	Upper clad application and baking; Wei Ru	Significant waveguide deformation. Discontinued
HN-109D (4″)	Upper clad application and baking; Wei Ru	Significant waveguide deformation. Discontinued
HN-111 (4″)	Upper clad application and baking; Bragg	Some Cytop cracking, waveguide damage. Delivered
HN-112 (4″)	Upper clad application and baking; Bio	Cytop cracking from contamination. Delivered
HN-123 (4″)	Standard upper clad: Bragg	Poor grating adhesion; no Cr used in deposition
HN-124 (4″)	Standard upper clad: Biosensor	Upper clad Cytop cracking. and w.g damage
HN-125 (4″)	Standard upper clad: Bragg	Good C82, over etched. Delivered
HN-126 (4″)	Standard upper clad: Bragg	Poor litho, etching excellent. Delivered
HN-127 (4″)	Standard upper clad: Wei Ru	Cytop cracking, w.g. damage, good etch. Delivered
HN-128 (4″)	Standard upper clad: Wei Ru	Cytop cracking, w.g. damage, good etch. Delivered

Note: “New Biosensor” mask = “Wei Ru” mask

Table A5
Multilayer Biosensor Wafer Summary

Preparation tests and Multilayer samples		
Wafer (diam)	**Particulars Tested**	**Results Summary**
HN-101 (4”)	Test for Multilayer: Au on Cr on Cytop	Excellent Au quality, slightly underdeveloped features
HN-104 (2”)	Multilayer test preparation; Bragg	Excellent quality. Excessive gold thickness.
HN-105 (2”)	Multilayer process witness; Bragg	CU AFM
HN-106 (4”)	Multilayer test preparation; Bragg	Very good results: feature dimensions, gold quality
HN-107 (4”)	Multilayer wafer; Bragg mask	Excellent fabrication results
HN-110 (4”)	Multilayer wafer; Biosensor mask	Excellent fabrication results
HN-110A (2”)	Multilayer process witness; Bragg	CU AFM
HN-122 (4”)	Multilayer wafer; Wei Ru mask	Excellent fabrication results

Appendix B Profilometry and AFM Analysis Summary

Profilometry and AFM Analysis Summary

Table B
Surface Roughness, Gold Roughness and Gold Thickness Results From AFM and Profilometry

Wafer (diam)	Gold Thickness (nm)	Roughness (nm)				Data Source
		Substrate average	Substrate RMS	Gold average	Gold RMS	
HN-55 (2″)	36 E-beam	~ 3peak to peak (p-p)		~ 6peak to peak (p-p)		O.U AFM
HN-63 (2″) Half Cytop	~32 E-beam	Poor gold quality: roughness and winging				O.U. AFM
HN-66 (2″)	44.5 T.F.R. = 125	~10 p-p		~10 p-p		O.U. AFM
	45.5 T.F.R. = 125	1.1	1.4	1.4	1.7	SSW AFM
	~45 T.F.R. = 125					C.U profilometer
HN-70 (4″) No Cytop	61 T.F.R. = 125	~5 p-p Deposition controller fail		~8 p-p		O.U. AFM
	~75 T.F.R. = 125	1.7	2.1	1.7	2.1	C.U AFM
HN-71 (4″) No Cytop	~63 T.F.R. = 125	Deposition controller fail				C.U profilometer
HN-72 (2″) No Cytop	37 T.F.R. = 160	~10 p-p		~10 p-p		O.U. AFM
	37.6 T.F.R. = 160	0.3	0.4	1.2	1.4	SSW
HN-73 (2″) No Cytop	~38-40 T.F.R. = 160					C.U profilometer
	~40 T.F.R. = 160	0.7	1.2	1.6	2.0	C.U AFM
HN-74 (2″) No Cytop	~40nm T.F.R. = 170	0.8	1.0	1.0	1.2	C.U AFM
	~33nm					C.U profilometer
HN-75 (2″) No Cytop	35.1 T.F.R. = 170	0.3	0.4	0.9	1.2	SSW
HN-85 (2″)	42 T.F.R. = 165	0.8	1.0	2.2	2.8	C.U AFM
HN-87 (2″)	44 T.F.R.= 165	0.8	1.0	1.5	1.9	C.U AFM

Legend T.F.L.O.J = Tooling Factor Lift-Off Jig T.F.R. = Tooling factor Rotation T.T = Target Thickness

Note: Samples have a full Cytop lower cladding unless otherwise specified

Profilometry and AFM Analysis Summary

Table B
Surface Roughness, Gold Roughness and Gold Thickness Results From AFM and Profilometry

Wafer (diam)	Gold Thickness (nm)	Roughness (nm)				AFM Data Source
		Substrate average	Substrate RMS	Gold average	Gold RMS	
HN-89 (2") Half Cytop	NA	0.4	0.5	Cytop		C.U AFM
	NA	3.4	4.5	Roughened Cytop 20sec@100W		C.U AFM
HN-91 (2") Half Cytop	NA maskless exposure	1.3	1.5	NA	NA	C.U AFM
HN-92 (2") Half Cytop	21	1.5	1.8	1.3	2.0	C.U AFM
	20	Run out of gold				C.U profilometer
HN-94 (2") Half Cytop Lower Cladding	~45 (wings) T.F.R. = 170	~1.2	~1.4	~1.7	~2.1	C.U AFM
	39 T.F.R. = 170					C.U profilometer
HN-95 (2") HF only	NA	0.15	0.19	NA	NA	C.U AFM
HN-96 (2") Factory	NA	0.3	0.4	NA	NA	C.U AFM
HN-97 (2") Half Cytop Lower Cladding	~25 T.F.R.= 170	Poor profilometer profiles				C.U profilometer
	35 T.F.R. = 170	1.7	2.1	1.9	2.5	C.U AFM
HN-99 (2") Half Cytop Lower Cladding	~25 T.F.R. = 170	Poor profilometer profiles				C.U profilometer
	37 T.F.R.= 170	2.0	2.5	2.1	2.6	C.U AFM
HN-100 (2") Half Cytop	~25 T.F.R.= 170	Poor profilometer profiles				C.U profilometer
HN-102 (4")	~36 T.F.R. = 170					C.U profilometer
HN-104 (2") No Cytop	22-23 T.F.L.O.J = 170 T.T. = 200A					C.U profilometer
HN-105 (2") No Cytop Lower Cladding	37-38 T.F.R. = 170					C.U profilometer
	~400 Å T.F.R. = 170	1.0	1.3	1.8	2.2	C.U AFM
HN-106 (4") No Cytop	~35 T.F.R. = 170					C.U profilometer
HN-107 Multilayer	40-46 T.F.R. = 170	Run out of gold at 225Å. Break vacuum, load more gold and continue next day.				C.U profilometer
	43 T.F.R. = 170			4.4	7.1	O.U profilometer

Legend T.F.L.O.J = Tooling Factor Lift-Off Jig T.F.R. = Tooling factor Rotation T.T = Target Thickness

Note: Samples have a full Cytop lower cladding unless otherwise specified

Profilometry and AFM Analysis Summary

Table B
Surface Roughness, Gold Roughness and Gold Thickness Results From AFM and Profilometry

Wafer (diam)	Gold Thickness (nm)	Roughness (nm)				Data Source
		Substrate average	Substrate RMS	Gold average	Gold RMS	
HN-108 (4") Half Cytop	~375 Å T.F.R.=172.5					C.U profilometer
HN-109A (4")	~345 Å T.F.R. = 189					C.U profilometer
HN-110A (2") No Cytop Lower Cladding	~325 Å T.F.R. = 175					C.U profilometer
	~400 Å T.F.R. = 175	1.1	1.4	1.5	1.8	C.U AFM
HN-110 Multilayer	35-37 T.F.R. = 175					C.U profilometer
HN-116 (4") No Cytop	~356 Å T.F.R. = 185					C.U profilometer
HN-117 (2") No Cytop	~351 Å T.F.R. = 185					C.U profilometer
HN-118 (2") No Cytop	~357 Å T.F.R. = 185					C.U profilometer
HN-119 (4") No Cytop	~333 Å T.F.R. = 195					C.U profilometer
HN-120 (2") No Cytop	~336 Å T.F.R. = 195					C.U profilometer
HN-121 (2") No Cytop	~312 Å T.F.R. = 195					C.U profilometer
HN-111 (4")	~349 Å T.F.R. = 189					C.U profilometer
HN-122 Multilayer	~345 Å T.F.R. = 189					C.U profilometer
HN-123 (4")	~325 Å T.F.R. = 187	Note: Gold thickness profiled immediately after deposition				C.U profilometer
	~400 Å T.F.R. = 187	Note: Gold thickness profiled again after 8 days in 100°C oven				C.U profilometer
HN-124 (4")	~325 Å T.F.R. = 187	Note: Gold thickness profiled immediately after deposition				C.U profilometer
	~400 Å T.F.R. = 187	Note: Gold thickness profiled again after 8 days in 100°C oven				C.U profilometer
HN-125 (4")	335 - 370 Å T.F.R. = 187					C.U profilometer
HN-128 (4")	340 - 370 Å T.F.R. = 188					C.U profilometer

Legend T.F.L.O.J = Tooling Factor Lift-Off Jig T.F.R. = Tooling factor Rotation T.T = Target Thickness

Note: Samples have a full Cytop lower cladding unless otherwise specified

Appendix C Cytop Based Fabrication Procedure Summary

Cytop Based Biosensor Fabrication Summary

Table C1
Wafer Preparation and Lower Cytop Cladding

Day 1 Step Number	Activity	Description	Chapter Reference
1	Select and scribe wafer	Single polish side. N or P type. Annotate on backside.	2.1.1.1 & 2.1.1.2.1
2	HF dip (10% HF solution)	50 seconds. For cleaning and surface smoothing	2.1.1.2.2
3	Plasma Preen	For organic cleaning 5 min on, 5 min off, 5min on	2.1.1.2.3
4	Spin coat 5% diluted M grade Cytop	10 sec@500 rpm/20 sec@1000 rpm	2.1.2.1
5	Baking	50°C for 30 min	2.1.2.1
5a	Optical examination	At 50x magnification: look for Cytop degradation; cracking, inclusions, contamination	2.1.2.6
6	Spin coat 9% S grade Cytop	10 sec@1000/20 sec@1500 rpm	2.1.2.2
7	Baking	50°C for 30 min	2.1.2.2
7a	Optical examination	At 50x magnification: look for Cytop degradation; cracking, inclusions, contamination	2.1.2.6
8	Spin coat 9% S grade Cytop	10 sec@1000 rpm/20 sec@1500 rpm	2.1.2.2
9	Baking	50°C for 30min	2.1.2.2
9a	Optical examination	At 50x magnification: look for Cytop degradation; cracking, inclusions, contamination	2.1.2.6
10	Spin coat 9% S grade Cytop	10 sec@1000 rpm/20 sec@1500 rpm	2.1.2.2
11	Ramp hard bake for Cytop M grade adhesion to silicon, cladding Baking and flow	50°C to 200°C @ 10 °C/hour for 18+ hrs	2.1.2.2
Note: All Cytop baking performed on hot plate			

Cytop Based Biosensor Fabrication Summary

Table C2
Lower Cytop Cladding

Day 2 Step Number	Activity	Description	Chapter Reference
11a	Optical examination	At 50x magnification: look for Cytop degradation; cracking, inclusions, contamination	2.1.2.6
12	RIE Edge Bead Removal	10min@200W	2.1.2.3
13	Spin coat 5% diluted M grade Cytop	20 sec@1000 rpm	2.1.2.4
14	Baking	(30 min @ 50°C) + (50°C to 200°C @150°C/hr) + (minimum 2.5hrs @ 200 °C) or 50°C to 200°C @ 10°C/hr for 18+ hrs (overnight)	2.1.2.4
Note: All Cytop baking performed on hot plate			

Cytop Based Biosensor Fabrication Summary

Table C3
Lithography and Deposition Preparation

Day 3 Step Number	Activity	Description	Chapter Reference
14a	Optical examination	At 50x magnification: look for Cytop degradation; cracking, inclusions, contamination	2.1.2.6
15	RIE Roughen (March)	20 sec for 2" wafer, 30 sec for 4" wafer	2.1.3.1
16	HMDS application (oven)	Temperature set at 98°C	2.1.3.2
17	Spin coat LOR-1A lift off resist (LOR)	10 sec@1000 rpm/30 sec@4000 rpm	2.1.3.3
18	Baking LOR	3min @180°C	2.1.3.3
19	Spin coat S1805 photo resist (PR)	10 sec@1000 rpm/30 sec@4000 rpm	2.1.3.4
20	Baking S1805 PR	3min @115°C	2.1.3.5
21	Ultraviolet exposure with MAG6 Aligner (calibrate prior to exposure)	- LOR on Silicon: 118mJ/cm^2 (H-line - 405nm) - LOR on short lower Cytop cladding (approx 4µm): 116mJ/cm^2 H-line - Full lower Cytop cladding (approx 8µm): 114mJ/cm^2 H-line	2.1.3.5
22	Develop MF-321	60 seconds	2.1.3.6
23	Optical examination in UV filtered environment (yellow room)	At 500x magnification: look for proper lithographic development; features and undercut	2.1.3.6
24	Load in Balzers Evaporator	Immediately after development (same day) for overnight pump down	2.1.4.1
Note day 3: activities in this table must be done in a single day			

Cytop Based Biosensor Fabrication Summary

Table C4
Gold Deposition and Start Upper Cytop Cladding

Day 4 Step Number	Activity	Description	Chapter Reference
25	Gold deposition	Thermal, 0.1A/s, rotation mounting, Tooling factor of 188	2.1.4.1
26	1165 Microstrip liftoff	10 min dirty 1165 @80°C + 10 sec ultrasonic + 10 min clean 1165 @80°C + (5 sec + 5 sec) ultrasonic + 10 min IPA + 10 min DI water	2.1.4.2
27	Wafer dehydration	15 min@ 100°C	2.1.4.2
27a	Optical examination	At 50x magnification: assess Cytop (cracking, inclusions, contamination) and metallization (adhesion) quality At 1000x magnification: feature dimensions, fine feature quality	2.1.4.3
27b	Profilometer examination	Determine metal thickness at various locations on the sample	2.1.4.4
28	Upper Clad Layer 1 Spin coat 9% S grade Cytop	10 sec@500 rpm/20 sec@4000 rpm	2.1.5
29	Upper Clad Baking 1	50°C to 100°C @ 5°C/hr for +13hrs (overnight)	2.1.5
Note: Step 26 must be done immediately after step 25 on the same day.			
Note: All Cytop baking performed on hot plate			
Note: At the time of writing, limiting the upper cladding bake temperature to 85°C was appearing to be effective in preventing Cytop cracking and the associated waveguide damage.			

Cytop Based Biosensor Fabrication Summary

Table C5
Upper Cytop Cladding

Day 5 Step Number	Activity	Description	Chapter Reference
29a	Post Bake 1 Optical examination	At 50x magnification: look for Cytop degradation (and associated waveguide damage); cracking, inclusions, contamination	2.1.5
30	Upper Clad Layer 2 Spin coat 9% S grade Cytop	10 sec@1000/20 sec@4000 rpm	2.1.5
31	Upper Clad Baking 2	50°C to 100°C @ 10°C/hr for +8hrs (overnight)	2.1.5
Day 6 31a	Post Bake 2 Optical examination	At 50x magnification: look for Cytop degradation (and associated waveguide damage); cracking, inclusions, contamination	2.1.5
Day 6 – 9	Perform steps 32, 33, 33a: 7 times (layers 3 to 9) for a total of 9 spun layers in the upper cladding		2.1.5
32	Upper Clad Layer 3 to 9 Spin coat 9% S grade Cytop	10 sec@1000/20 sec@4000 rpm	2.1.5
33	Upper Clad Baking 3 to 9	(30 min @ 50°C) + (50°C to 100°C @25°C/hr) + (minimum 2hr @ 100 °C) or 50°C to 100°C @ 10°C/hr for +8hrs (overnight)	2.1.5
33a	Post Bake 3 to 9 Optical examination	At 50x magnification: look for Cytop degradation (and associated waveguide damage); cracking, inclusions, contamination	2.1.5
Note: All Cytop baking performed on hot plate			
Note: At the time of writing, limiting the upper cladding bake temperature to 85°C was appearing to be effective in preventing Cytop cracking and the associated waveguide damage.			

Cytop Based Biosensor Fabrication Summary

Table C6
Channel Etch Mask Lithography

Day 10 Step Number	Activity	Description	Chapter Reference
34	RIE Roughen (March)	20 sec for 2” wafer, 30 sec for 4” wafer	2.1.6
35	HMDS application (oven)	Temperature set at 98°C	2.1.6
36	SPR-220 application	Spin: 30@1000 rpm/10@2300 rpm	2.1.6
37	SPR-220 Photoresist baking on hot plate	30 min @ room temperature + Room temperature to 100°C + 15min @ 100°C + 100°C to room temperature	2.1.6
38	Ultraviolet exposure with MAG6 Aligner	H-line (405nm) @ 870mJ/ cm^2	2.1.6
39	SPR-220 Photoresist baking	Room temperature overnight	2.1.6

Cytop Based Biosensor Fabrication Summary

Table C7
Channel Etch Mask Baking, Development and Channel Etching

Day 11 Step Number	Activity	Description	Chapter Reference
40	SPR-220 Photoresist baking on hot plate	Room temperature to 100°C + 60 sec @ 115°C + 100°C to room temperature	2.1.6
41	MF-24A development	4:00 minutes (for H-line exposure of 870mJ/ cm^2) **Make sure fully developed!**	2.1.6
42	Channel Etching (March RIE)	**Be Careful Here! Profilometer check of waveguide height often!** For upper cladding procedure of day 4 to day 9 (~9µm) etch for no more than 30 100w-min, to yield an etch depth of approximately 9500nm.	2.1.7

Cytop Based Biosensor Fabrication Summary

Table C8
Channel Etch Mask Removal

Day 12 Step Number	Activity	Description	Chapter Reference
43	SPR-220 removal	Acetone, IPA, DI immersion: 10min each	2.1.8.1
44	Dehydrate bake	95°C for 15 min	2.1.8.1
45	Etching examination	Profilometer to determine channel depth	2.1.8.2

Cytop Based Biosensor Fabrication Summary

Table C9
Dicing Preparation

Day 12 Step Number	Activity	Description	Chapter Reference
46	HMDS application (oven)	Temperature set at 98°C	2.1.8.3
47	SPR-220 application	Spin: 30@1000 rpm/10@2300 rpm	2.1.8.3
48	SPR-220 baking	30 min @ room temperature + Room temperature to 100°C + 20min @ 100°C + 100°C to room temperature	2.1.8.3
49	Package for delivery	Put in 4" wafer puck (face down). Label, tape seal, tissue wrap and place in plastic bag.	2.1.8.3

Appendix D Multilayer Based Fabrication Procedure Summary

Multilayer Based Biosensor Fabrication Summary

Table D1
Wafer Preparation, Lithography and Deposition Preparation

Day 1 Step Number	Activity	Description	Chapter Reference
1	Select and scribe wafer	Pre-fabricated Ta_2O_5-SiO_2 multilayered stack on 4" silicon wafer. Annotate on backside.	3.1.2.1 & 3.1.1.2.1
2	Plasma Preen	For organic cleaning	3.1.1.2.3
3	HMDS application (oven)	Temperature set at 98°C	3.1.3
4	Spin coat LOR-1A lift off resist (LOR)	10@1000 rpm/30@4000 rpm	3.1.3
5	Baking LOR	3min @180°C	3.1.3
6	Spin coat S1805 photo resist (PR)	10@1000 rpm/30@4000 rpm	3.1.3
7	Baking S1805 PR	3min @115°C	3.1.3
8	Ultraviolet exposure with MAG6 Aligner (calibrate prior to exposure)	114mJ/cm^2 H-line	3.1.3
9	Develop MF-321	60 seconds	3.1.3
10	Optical examination in UV filtered environment (yellow room)	At 500x magnification: look for proper lithographic development; features and undercut	3.1.3
11	Load in Balzers Evaporator on rotation mounting plate	Immediately after development (same day) for overnight pump down	3.1.3.1
12	Descum	Technics Planar RIE for 60 seconds @ 100W	3.1.3.2
Note: Day 1 activities in this table must be done in a single day			

Multilayer Based Biosensor Fabrication Summary

Table D2
Gold Deposition and Start Upper Cytop Cladding

Day 2 Step Number	Activity	Description	Chapter Reference
13	Chrome[1] and Gold deposition	Thermal, 0.1A/s, rotation mounting, Tooling factor of 188	3.1.4.1
14	1165 Microstrip liftoff	10min dirty 1165 @80°C + 10 sec ultrasonic + 10min clean 1165 @80°C + 10 sec ultrasonic + 10min IPA + 10min DI water	3.1.4.2
14a	Optical examination	At 1000x magnification: look for proper feature dimensions	3.1.4.2
15	Spin coat 5% diluted M grade Cytop	10@500 rpm/20@1000 rpm	3.1.5
16	Cytop Baking	50°C for 30min	3.1.5
Note: Step 14 must be done immediately after step 13 on the same day.			
Note: All Cytop baking performed on hot plate			
[1] A chrome layer is always required for gold adhesion on the multilayer wafer			

Multilayer Based Biosensor Fabrication Summary

Table D3
Continuation and Completion of Cytop Cladding

Day 3 Step Number	Activity	Description	Chapter Reference
16a	Optical examination	At 50x magnification: look for Cytop degradation (and associated waveguide damage); cracking, inclusions, contamination	3.1.5
17	Spin coat 9% S grade Cytop	10 sec@1000/20 sec@1500 rpm	3.1.5
18	Cytop Baking	50°C for 30min	3.1.5
18a	Optical examination	At 50x magnification: look for Cytop degradation (and associated waveguide damage); cracking, inclusions, contamination	3.1.5
19	Spin coat 9% S grade Cytop	10 sec@1000 rpm/20 sec@1500 rpm	3.1.5
20	Cytop Baking	50°C for 30min	3.1.5
20a	Optical examination	At 50x magnification: look for Cytop degradation (and associated waveguide damage); cracking, inclusions, contamination	3.1.5
21	Spin coat 9% S grade Cytop	10 sec@1000 rpm/20 sec@1500 rpm	3.1.5
22	Cytop Baking	50°C for 30min	3.1.5
22a	Optical examination	At 50x magnification: look for Cytop degradation (and associated waveguide damage); cracking, inclusions, contamination	3.1.5
23	Spin coat 5% diluted M grade Cytop	20 sec@1000 rpm	3.1.5
24	Cytop Baking	50°C to 200°C @ 10 °C/hour for 18+ hrs	3.1.5
Note: All Cytop baking performed on hot plate			

Multilayer Based Biosensor Fabrication Summary

Table D4
Channel Etch Mask Lithography, Exposure and Curing

Day 4 Step Number	Activity	Description	Chapter Reference
24a	Optical examination	At 50x magnification: look for Cytop degradation (and associated waveguide damage); cracking, inclusions, contamination	3.1.5
25	RIE Roughen (March)	20 sec for 2” wafer, 30 sec for 4” wafer	3.1.6
26	HMDS application (oven)	Temperature set at 98°C	3.1.6
27	SPR-220 application	Spin: 30@1000 rpm/10@2300 rpm	3.1.6
28	SPR-220 Photoresist curing	30 min @ room temperature + Room temperature to 100°C + 15min @ 100°C + 100°C to room temperature	3.1.6
29	Ultraviolet exposure with MAG6 Aligner	(H-line) @ 870mJ/ cm^2	3.1.6
30	SPR-220 Photoresist curing	Room temperature overnight	3.1.6

Multilayer Based Biosensor Fabrication Summary

Table D5
Channel Etch Mask Curing and Channel Etching

Day 5 Step Number	Activity	Description	Chapter Reference
31	SPR-220 Photoresist curing	Room temperature to 100°C + 60 sec @ 115°C + 100°C to room temperature	3.1.6
32	MF-24A development	4:00 minutes (for H-line exposure of 87mJ/ cm^2) **Make sure fully developed!**	3.1.6
33	Channel Etching (March RIE)	**Don't Have to Be So Careful Here, Have an Etch Stop!** For upper cladding procedure of day 2 and day 3 (~8µm), etch for approximately 32.0 100w-min	3.1.7

Multilayer Based Biosensor Fabrication Summary

Table D6
Channel Etch Mask Removal and Dicing Preparation

Day 6 Step Number	Activity	Description	Chapter Reference
34	SPR-220 removal	Acetone, IPA, DI: 10min each	3.1.8
35	Dehydrate bake	95 °C for 15 min	3.1.8
35a	Etching examination	Profilometer to determine channel depth	3.1.8
Dicing Preparation			
36	HMDS application (oven)	Temperature set at 98°C	3.1.8
37	SPR-220 application	Spin: 30@1000 rpm/10@2300 rpm	3.1.8
38	SPR-220 curing	30 min @ room temperature + Room temperature to 100°C + 20min @ 100°C + 100°C to room temperature	3.1.8
39	Package for delivery	Put in 4" wafer puck (face down). Label, tape seal, tissue wrap and place in plastic bag.	3.1.8

Appendix E Cytop Etch Test Procedure Summary

Table E1 - Etch Sequence for 8.5µm Cytop Etch Depth

Etch Sequence for 8.5µm Cytop Etch Depth March RIE: O2 flow 220 sccm, Pressure 350 mTorr		
Etch Series	**Details**	**Location in Etch Chamber**
1 Total 100W-min = 16	2 minutes @ 200W	N
	2 minutes @ 200W	E
	2 minutes @ 200W	S
	2 minutes @ 200W	W
	Profilometer waveguide height examination	
2 Total 100W-min = 6	1.5 minutes @ 100W	N
	1.5 minutes @ 100W	E
	1.5 minutes @ 100W	S
	1.5 minutes @ 100W	W
	Profilometer waveguide height examination	
3 Total 100W-min = 3	45 seconds @ 100W	N
	45 seconds @ 100W	E
	Profilometer waveguide height examination	
	45 seconds @ 100W	S
	45 seconds @ 100W	W
	Profilometer waveguide height examination	
4 Total 100W-min = 2	60 seconds @ 50W	N
	Profilometer waveguide height examination	
	60 seconds @ 50W	E
	Profilometer waveguide height examination	
	60 seconds @ 50W	S
	Profilometer waveguide height examination	
	60 seconds @ 50W	W
	Profilometer waveguide height examination	
Total power time = 27 100W-min		

Appendix F Cytop Lower and Upper Cladding Application Procedures Summary

Table F1 - Lower Cytop Cladding Application and Bake Summary - per Chiu [28]

Lower Cytop Cladding Application Summary	
Activity	**Details**
Spin (1st layer): 5% M-Grade Cytop	10 seconds @ 500 rpm + 20 seconds @ 1000 rpm (~0.4µm)
Bake: 1st layer	(30 min @ 50°C)
Spin (2nd to 4th layers): 9% S-Grade Cytop	10 seconds @ 1000 rpm + 20 seconds @ 1500 rpm (~2.65µm)
Bake: 2nd to 4th layers	(30 min @ 50°C)
Spin (5th to 7th layers): 5% S-Grade Cytop	10 seconds @ 500 rpm + 20 seconds @ 1000 rpm (~0.76µm)
Bake: 5th to 7th layers	(30 min @ 50°C)
Final Bake	(50°C to 200°C @ 150°C/hr) + (1.5 hours @ 200°C)
Reported Thickness	10.0 µm
Baking method	hot plate

Table F2 - Lower Cytop Cladding Application and Baking Summary - per Banan [42]

Lower Cytop Cladding Application Summary	
Activity	**Details**
Spin (1st layer): 5% M-Grade Cytop	~0.4µm
Bake: 1st layer	(30 min @ 50°C)
Spin (2nd to 4th layers): 9% S-Grade Cytop	~2.6µm
Bake: 2nd to 4th layers	(30 min @ 50°C)
Spin (5th layer): 5% S-Grade Cytop	~0.8µm
Bake: 5th layer	(30 min @ 50°C)
Final Bake	(50°C to 220°C @ 150°C/hr) + (more than 12 hours @ 220°C)
Reported Thickness	Approximately 9 µm
Baking method	hot plate

Table F3 - Lower Cytop Cladding Application and Baking Summary - per Asiri [30]

Lower Cytop Cladding Application Summary	
Activity	**Details**
Spin (1st layer): 5% M-Grade Cytop	10 seconds @ 500 rpm + 20 seconds @ 1000 rpm (~0.4µm)
Bake: 1st layer	(30 min @ 50°C)
Spin (2nd to 4th layers): 9% S-Grade Cytop	10 seconds @ 500 rpm + 20 seconds @ 1000 rpm (~2.35µm)
Bake: 2nd to 4th layers	(30 min @ 50°C)
Spin (5th layer): 5% S-Grade Cytop	20 seconds @ 1000 rpm (~1.4µm)
Bake: 5th layer	(30 min @ 50°C)
Final Bake	(50°C to 200°C @ 150°C/hr) + (2.5 hours @ 200°C)
Reported Thickness	Approximately 9 µm
Baking method	hot plate

Table F4 - Lower Cytop Cladding Application and Baking Summary - per Hassan [31]

Lower Cytop Cladding Application Summary	
Activity	**Details**
Spin (1st layer): 5% M-Grade Cytop	10 seconds @ 500 rpm + 20 seconds @ 1000 rpm (~0.4µm)
Bake: 1st layer	(30 min @ 50°C)
Spin (2nd to 4th layers): 9% S-Grade Cytop	10 seconds @ 500 rpm + 20 seconds @ 1000 rpm (~2.35µm)
Bake: 2nd to 4th layers	(30 min @ 50°C)
Spin (5th layer): 5% S-Grade Cytop	20 seconds @ 1000 rpm (~1.4µm)
Bake: 5th layer	(30 min @ 50°C)
Final Bake	(50°C to 200°C @ 150°C/hr) + (2.5 hours @ 200°C)
Reported Thickness	8.8 µm
Baking method	DATAPLATE brand programmable hot plate

Table F5 - Lower Cytop Cladding Application and Baking Summary - per Northfield

Lower Cytop Cladding Application Summary	
Activity	**Details**
Spin (1st layer): 5% M-Grade Cytop	10 seconds @ 500 rpm + 20 seconds @ 1000 rpm (~0.4µm)
Bake: 1st layer	(30 min @ 50°C)
Spin (2nd to 4th layers): 9% S-Grade Cytop	10 seconds @ 500 rpm + 20 seconds @ 1000 rpm (~2.35µm)
Bake: 2nd to 4th layers	(30 min @ 50°C)
Pre edge bead removal bake	50°C to 200°C @ 10°C/hr (for more than 18 hours)
Edge bead removal	10min @ 200W in March RIE
Spin (5th layer): 5% M-Grade Cytop	20 seconds @ 1000 rpm (~1.4µm)
Bake: 5th layer	(30 min @ 50°C) + (50°C to 200°C @150°C/hr) + (2.5hrs @ 200 °C) or 50°C to 200°C @ 10°C/hr for 18+ hrs (overnight)
Reported Thickness	Post etch profilometry indicates 8µm
Baking method	DATAPLATE brand programmable hot plate

Table F6 - Upper Cytop Cladding Application and Bake Summary - per Chiu [28]

Upper Cytop Cladding Application Summary	
Activity	**Details**
Spin (all 6 layers): 9% S-Grade Cytop	10 seconds @ 1000 rpm + 20 seconds @ 4000 rpm (~1.35µm)
Bake: 1st to 6th layers	(30 min @ 50°C)
Final Bake	(30 min @ 50°C) + (50°C to 90°C @ 20°C/hr) + (2 hours @ 90°C)
Reported results	Slight deformation of contact pads and joints, no deformation of waveguides. No Cytop cracking or waveguide cracking.
Reported Thickness	6 x 1.35 µm = 8.1µm
Baking method	hot plate

Table F7 - Upper Cytop Cladding Application and Baking Summary - per Banan [42]

Upper Cytop Cladding Application Summary	
Activity	**Details**
Spin (all 6 layers): 9% S-Grade Cytop	~ 1.35 µm
Bake: 1st to 6th layers	(30 min @ 50°C) + (50°C to 90°C @ 5°C/hr) + (at least 12 hours @ 90°C)
Reported results	No observable metal deformation.
Reported Thickness	6 x 1.35 µm = 8.1µm

Table F8 - Upper Cytop Cladding Application and Baking Summary - per Asiri [30]

Upper Cytop Cladding Application Summary	
Activity	**Details**
Spin (all 7 layers): 9% S-Grade Cytop	10 seconds @ 1000 rpm + 20 seconds @ 4000 rpm
Bake: 1st to 7th layers	(30 min @ 50°C) + (50°C to 100°C @ 25°C/hr) + (4 hours @ 100°C)
Reported results	No metal deformation, no cracking
Reported Thickness	6 x 1.1 µm = 7.7µm
Baking method	hot plate

Table F9 - Upper Cytop Cladding Application and Baking Summary - per Hassan [31]

Upper Cytop Cladding Application Summary	
Activity	**Details**
Spin (all 6 layers): 9% S-Grade Cytop	10 seconds @ 1000 rpm + 20 seconds @ 4000 rpm
Bake: 1st layer	(30 min @ 50°C) + (50°C to 100°C @ 5°C/hr) + (24 hours @ 100°C)
Bake: 2nd layer	(30 min @ 50°C) + (50°C to 100°C @ 10°C/hr) + (24 hours @ 100°C)
Bake: 3rd to 6th layers	(30 min @ 50°C) + (50°C to 100°C @ 25°C/hr) + (2 hours @ 100°C)
Reported results	No metal deformation, no cracking
Reported Thickness	6 x 1.35 µm = 8.1µm
Baking method	DATAPLATE brand programmable hot plate

Table F10 - Upper Cytop Cladding Application and Baking Summary - Northfield

Upper Cytop Cladding Application Summary	
Activity	**Details**
Spin (all 9 layers): 9% S-Grade Cytop	10 seconds @ 1000 rpm + 20 seconds @ 4000 rpm
Bake: 1st layer	50°C to 100°C @ 5°C/hr (more than 13 hours)
Bake: 2nd layer	50°C to 100°C @ 10°C/hr (more than 8 hours)
Bake: 3rd to 9th layers	(30 min @ 50°C) + (50°C to 100°C @ 25°C/hr) + (2 hours @ 100°C) or (if end of day in fabrication lab do an overnight bake) 50°C to 100°C @ 10°C/hr (more than 8 hours)
Reported results	Cracking after first layer causing gold cracking. Final results: no metal deformation, only "spider web" cracking around contamination bits
Reported Thickness	9.2µm (determined by etch depth)
Baking method	DATAPLATE programmable hot plate

Table F11 - Upper Cytop Cladding Application and Baking Summary - Northfield (Test)

Upper Cytop Cladding Application Summary	
Activity	**Details**
Spin: 1st layer 5% M-grade	10 seconds @ 500 rpm + 20 seconds @ 1000 rpm
Bake: 1st layer	room temperature to 100°C @10°C/hr (+10hrs)
Spin: 2nd layer 9% S-grade	10 seconds @ 1000 rpm + 20 seconds @ 1500 rpm
Bake: 2nd layer	(30 minutes @ room temperature) + (room temperature to 50°C, hold for 30 minutes) + (50°C to 80°C, hold for 60 minutes)
Spin: 3rd layer 9% S-grade	10 seconds @ 1000 rpm + 20 seconds @ 1500 rpm
Bake: 3rd layer	(30 minutes @ room temperature) + (room temperature to 50°C, hold for 30 minutes) + (50°C to 80°C, hold for 60 minutes)
Spin: 4th layer 9% S-grade	10 seconds @ 1000 rpm + 20 seconds @ 1500 rpm
Bake: 4th layer	(30 minutes @ room temperature) + (room temperature to 50°C, hold for 30 minutes) + (50°C to 80°C, hold for 60 minutes)
Spin: 5th layer 5% M-grade	20 seconds @ 1000 rpm
Bake: 5th layer	room temperature to 100°C @10°C/hr (+10hrs)
Reported results	Final results: Significant contamination particles and associated Cytop spider web cracking. Breaks in waveguides where cracks transected.
Reported Thickness	Post etch profilometry indicates 8µm
Baking method	DATAPLATE programmable hot plate