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SUR MICROFICHENAME OF AUTHOR/NOM DE L'AUTEUR CROWDHURY FAZLUR RAHIMTITLE OF THESIS/TITRE DE LA THÈSE AN INVESTIGATION OF MOS SWITCHED
CAPACITOR FILTERSUNIVERSITY/UNIVERSITÉ CARLETON UNIVERSITYDEGREE FOR WHICH THESIS WAS PRESENTED/
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LA THÈSE A ÉTÉ
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AN INVESTIGATION OF MOS SWITCHED CAPACITOR
FILTER CIRCUITS

by

Chowdhury Fazlur Rahim, B.Sc., M. Eng.

A thesis submitted to the Faculty of Graduate Studies,
and Research in partial fulfillment of the requirements
for the degree of Doctor of Philosophy.

Faculty of Engineering
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November 1978

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Filter Circuits

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ABSTRACT

A systematic approach to the design of switched capacitor filters has been developed in this work. Its relation to active-RC filters in the analog domain and IIR filters in the digital domain has been investigated, and the relative pros and cons of the various modes of achieving switched capacitor filters studied. In particular, the bilinear transformation has been achieved by suitably combining the two basic modes of the switched capacitor element, viz. series and parallel. This was found very useful for realizing high-Q filters and equalisers. Based on the above knowledge, various transfer functions, involving poles as well as zeros, have been simulated, and the results presented. Finally, the implications of the process limitations on the realizability of switched capacitor filters in MOS LSI systems have been studied. The dominant sources of non-ideal behaviour, viz. parasitic capacitances and diode leakage, have been identified. An alternate circuit structure which may be less sensitive to parasitic capacitance and diode leakage in MOS LSI implementation has been proposed and investigated.

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LIST OF SYMBOLS

- A Ratio of switched capacitor coefficients $\frac{\alpha_2 \alpha_3}{\beta}$ (Chapter 3)
- A Effective area of the p-n junction (Section 4.1)
- A The open-loop gain of the operational amplifier (Section 4.2)
- A' The unloaded gain of the operational amplifier.
- a_i Coefficients of the digital filter
- B Sum of switched capacitor coefficients $\alpha_1 + \alpha_2 + \alpha_3$
- b_j The jth coefficient of the transfer function
- C Capacitance of the integrating capacitor
- C_D Diffusion capacitance of the p-n junction
- C_{D0} d-c diffusion capacitance of the p-n junction
- C_L Load capacitance
- C_R Capacitance of the switched capacitor elements
- C_s The effective capacitance of the capacitors C_R and C_L in series.
- $C_{s,N}$ Stray capacitance at the nth node.
- C_i Capacitance of the input switched capacitor.
- C_f Capacitance of the feedback switched capacitor.
- C_1, C_2 Capacitors in an R-C circuit.
- e_n The spectral density of the noise source in switched capacitor.
- $\langle e_{op}^2 \rangle$ The spectral density of the operational amplifier.

- $\langle e_{na}^2 \rangle$ The noise power spectral density of the operational amplifier in the MFB filter.
- $\langle e_{nb}^2 \rangle$ The rms noise power at the bandpass output of the biquad.
- f_H Upper cutoff frequency in Hz.
- f_L Lower cutoff frequency in Hz.
- f_a Lower bound for the operational amplifier noise.
- f_b Upper bound for the operational amplifier noise.
- f_p The highest frequency in the passband.
- f_q The lowest frequency in the stopband.
- f_s Sampling frequency in hertz, $f_s = 1/T$.
- f_o Resonant frequency in hertz, $f_o = \omega_o/2\pi$.
- G A constant proportional to the gain in resonance.
- $H(z)$ Transfer function in z-domain.
- $H_B(z)$ The transfer function of the biquad filter at the bandpass output.
- $H_{os}(z)$ The transfer function between the output and the positive terminal in the MFB filter.
- h The bump height (i.e., the gain at resonance).
- I_g Leakage current due to generation of carriers in the depletion region.
- I_{go} d-c leakage current in the depletion region.
- K Fraction of the output voltage fed back to the notch filter.

K_S	Dielectric constant of the semiconductor.
K_1^2	The component contributing to $1/f$ noise of the operational amplifier.
K_2^2	Thermal noise of the operational amplifier.
k	The Boltzmann constant.
k_j	Measure of the deviation of the j th switched capacitor from design value.
ℓ_j	Measure of the deviation of the j th integrating capacitor from design value.
m	Integral ratio of the sampling interval of the feedback switched capacitor to that of the input switched capacitor.
N_A	Acceptor dopant concentration, holes/cm ³ .
n	Order of the filter.
n_i	Intrinsic carrier concentration, 1.45×10^{10} cm ⁻³ for silicon.
P	Total integrated noise power up to the Nyquist.
Q_{po}	Quality of the pole.
ΔQ	Net transfer of charge.
q	Electronic charge, 1.6×10^{-19} coulombs.
Δq_D	Net charge delivered by the diffusion capacitor to the summing junction of the operational amplifier.
R	Value of resistor in ohms.
r	The effective resistance of the MOSFET switches.

r_m	Ratio of the mth diffusion capacitance to the integrating capacitor C.
S	An operator, denoting $(z-1)/(z+1)$.
S_y^α	Sensitivity of the parameter α with respect to y .
s	Complex frequency.
T	Sampling interval in seconds.
ΔT	Time interval between the ON-time of ϕ_1 and ϕ_2 .
t	Time in seconds.
δt	Time interval in seconds.
$u(t)$	Step response of the operational amplifier to a sampled input in time domain.
V_{BIAS}	Bias voltage applied to the input of the switched capacitor.
$V_i(z)$	The Z-transform of the input voltage.
$V_m(s)$	The voltage at the mth node in s-domain.
$V_m(z)$	The voltage at the mth node in z-domain.
V_n	The amplitude of the nth harmonic.
V_O	The output voltage of the operational amplifier.
$V_O(z)$	The z-transform of the output voltage.
V_{os}	The d-c offset of the operational amplifier.
V_R	Voltage across the reverse-biased p-n junction.
V_{SUB}	Potential applied to the substrate of the MOSFET switches.
V_t	Voltage $(V_{BIAS} + \phi_B - V_{SUB})$

- V_x Voltage at the negative input to the operational amplifier.
- v_i Instantaneous signal voltage applied to the input of the switched capacitor.
- $v_{i,n}$ The input voltage at the nT -th instant.
- $v_i(t)$ Input voltage at time t .
- $v_{l,n}$ Sampled voltage at the l th mode at the nT -th instant.
- $v_{o,n}$ The output voltage at the nT -th instant.
- $v_o(t)$ Output voltage at time t .
- W Depletion region width of the reverse-biased p-n junction.
- X Ratio of the capacitors, C_R/C .
- $y(n)$ Value of y at the nT -th instant.
- z An operator, denoting $z = \exp(sT)$.
- Z_o Output impedance of the operational amplifier.
- Z_{out} Output impedance of the switched capacitor integrator.
- Z_p The pole of a sampled-data system in z domain.
- Z_z The zero of a sampled-data system in z -domain.
- α The ratio of the feedback switched capacitor C_f to the integrating capacitor C (i.e., $\alpha = C_f/C$).

α_R	Switched capacitor coefficient, whose equivalent resistance value is R .
α_m	The m th switched capacitor coefficient.
α'_m	The switched capacitor coefficient corresponding to the equivalent continuous case.
β	The voltage feedback ratio for a switched capacitor feedback system.
γ	Ratio of switched capacitor coefficients α_3/α_2
ϵ_0	Permittivity of free space, 8.86×10^{-14} f/cm.
ϵ	Error in realizing the switched capacitor.
η	Amplitude of brickwall filter with cutoff at f_c and area equivalent to the transfer function of a sampled-data filter.
τ_0	Effective lifetime within a reverse biased depletion region.
ϕ_B	Built-in voltage of the metallurgical p-n junction.
ϕ_T	Total electrostatic potential from one side of the p-n junction to the other.
Ω	Real frequency in the analog domain which corresponds to ω in the sampled-data domain.
ω	Real frequency in the sampled-data domain.

ω_0 Resonant frequency in radians per second.

ω_c Corner frequency in radians per second.

$\Delta\omega$ Bandwidth in radians.

ω_{3dB} The cutoff frequency in radians.

CHAPTER ONE

INTRODUCTION

1.1. SUBJECT OF THESIS

This thesis explores a means of achieving monolithic integrated filters in a sampled analog MOS LSI circuit, which makes use of the periodic switching of capacitors to derive the desired analog function [1]. Essentially the concept involves simple manipulation of charge on a sampled basis between different nodes of the circuit. Over periods of time which are long compared to the periodic switching intervals, the transfer of charge is quasi-continuous, and equivalent to the continuous flow of current in resistors. Therefore to assist in generalizing the design approach for all kinds of analog applications, the name "switched capacitor" is proposed for the basic element, which consists of a capacitor and two analog switches. In most applications, a circuit will contain other capacitors which are considerably larger in value than those contained in the associated switched capacitors. These larger capacitors fully correspond to those in a classical RC circuit.

One purpose of this dissertation is to study, in the sampled analog domain, the general equivalence between switched capacitor networks and conventional RC networks, both passive and active. The second, and more important, objective is to create techniques for designing arbitrary analog filter functions using such switched capacitors.

1.2. SWITCHED CAPACITOR NETWORKS IN THE PERSPECTIVE OF PRESENTLY AVAILABLE TECHNOLOGY

It will be demonstrated in this dissertation that the switched capacitor approach makes possible the design of useful analog functions, in particular, frequency selective filters, in monolithic integrated form, without any parametric trimming, using MOS LSI technology. This has important implications in telecommunications, where a large number of filter circuits are required for system LSI applications. The technologies available for such filtering to the present have not fully met the requirements essential for integration in monolithic LSI, viz. production-line fabrication of completely integrated systems (having both analog and digital functions) together with their functional interconnection. Charge-coupled device (CCD) filters are a step in this direction but are not general enough for the whole range of applications, because they are non-recursive and hence not very suitable for frequency selective filters. There are also other forms of presently available filtering circuits, which will be briefly reviewed in this section as background to the thesis.

1.2.a) PASSIVE RLC CIRCUITS

Passive RLC circuits can be used for realizing frequency emphasizing networks with relative ease. However for lower frequency ranges, inductors, because of their size, weight and practical performance limitations are unattractive for miniaturization of large circuits.

1.2.b) ACTIVE RC CIRCUITS - THIN FILM "HYBRID" CIRCUITS

The active RC circuit is an improvement in this respect over the passive counterpart. Among the advantages are small size and weight, simplicity of synthesis and tuning, isolation of stages, and large available gain. There are limitations, for example, limited dynamic range in terms of voltage and current levels, inability to "float" a given realization, possibility of the circuit being unstable, and parasitic effects induced by the active element, such as dc output voltage offset, input bias currents, etc. However, in most applications the advantages outweigh the disadvantages, and thus active RC filters are popular in a wide range of engineering applications. Miniaturization of active RC circuits by the thin-film approach has permitted the construction of numerous precision circuit elements and their interconnection [2]. Thin-film circuits assume the form of "hybrid" circuits (for example, deposited RC networks with attached discrete chip transistors and diodes). For precise tuning of the filter circuits, the resistors can be fine-tuned at the post-fabrication stage. Although the process can be automated, it is costly.

1.2.c) MONOLITHIC INTEGRATED ACTIVE FILTER

Since the basic building blocks for an active filter, namely the resistors, capacitors and amplifiers are available in integrated form, active filter techniques are in principle readily compatible with monolithic integrated technology [3]. However the performance characteristics are very strong functions of the system's natural

frequencies, which are determined by resistor-capacitor (RC) products and the overall loop gain in the feedback circuit. While the loop gain can be desensitized by providing local feedback around gain stages, the absolute value of the RC time-constant can be controlled only if the absolute value of the two dissimilar circuit elements, such as a resistor and a capacitor, can be tightly controlled. Since the two elements are fabricated using different processing steps, it is difficult to achieve the latter objective. Furthermore the temperature and voltage coefficients for the resistor and capacitor are different, which limit the range of use. Such circuits are therefore not widely used.

1.2.d) TRANSVERSAL FILTERING USING CHARGE-TRANSFER DEVICES

Recently a form of MOS LSI filtering that has gained widespread attention is the sampled-data analog filter. The advent of various charge transfer devices, especially charge-coupled devices, has stimulated extensive interest in discrete-time analog signal processing [4]. Numerous innovations in the past few years have brought the technology forward and made possible a wide range of analog functions such as transversal filters, both fixed tap weight and electrically programmable, matched filtering, radar pulse compression, spectral analysis, adaptive channel equalizer, etc. While this type of filtering is a very powerful tool in certain signal processing applications, it is relatively inefficient in others. For example, a tunable narrowband bandpass filter with a 3 dB bandwidth of about 0.7% of center frequency and 40 dB sidelobes requires an 800 stage transversal filter [5]. This

requires large chip area and moderately complex peripheral circuits to run the CCD. Furthermore, the circuit is only mask programmable. This means that for spectral analysis, etc., a large number of such chips are required. Furthermore these filters have finite insertion loss; approximately 20 dB has been reported [5]. Therefore in order to have a wide dynamic range, the filter circuit must include a low-noise high gain amplifier at the output end. Until now, on-chip amplifiers with sufficiently good characteristics have not been reported.

1.2.e) RECURSIVE FILTERING USING CONVENTIONAL CHARGE-TRANSFER DEVICES

A form of filtering which is conceptually quite close to the switched capacitor filtering reported here is recursive filtering using conventional charge-transfer devices such as the bucket-brigade device (BBD), charge coupled device (CCD), etc. Essentially these devices serve the purpose of delaying the sampled signal, while the coefficients are generated by using active feedback amplifiers with very accurately controlled gain [4]. To date, such amplifiers have not been completely integrated on the chip. Moreover, the tapping techniques at the various delay elements by source-followers, etc. introduce distortion into the system [6]. They also need relatively large off-chip circuitry to support the system. Recently CCD recursive filters have also been reported [7], which tap the analog signal at intervals in the CCD delay line. Once again these filters use off-chip amplifiers. The transfer inefficiency of each delay stage affects the poles of the filter. Furthermore each sensing stage uses charge to voltage

conversion for feedback, introducing non-linearity in each conversion process. Thus these filters do not meet the requirements set forth at the beginning of this section.

Another form of recursive filtering using MOS sampled-data techniques has been reported [8]. In this work, the canonic second-order digital recursive filter has been realized by suitably combining MOS switched capacitors and on-chip operational amplifiers. The output signal voltage in these filters can be sensed directly (instead of capacitively, as in the previous case). This results in a larger signal output and the amplifier specifications are comparatively relaxed. However the sensitivity of the important filter parameters to coefficients of the recursive structure can be very high. While recursive structures are more efficient than transversal structures for frequency selective filtering, the high sensitivity of the circuit to parametric variations (i.e. coefficients) has discouraged its use in monolithic integrated circuits.

1.2.f) SWITCHED CAPACITOR FILTERS

The switched capacitor filter circuits to be described overcome many of the problems in the previous sections. They have no inherent insertion loss as in CCDs, to a first-order approximation. Consequently the design of the amplifier is considerably relaxed. The clocking schemes are relatively simple and small silicon chip area is required. By choosing an appropriate topology, it is possible to construct filters with low sensitivity. Hence circuits may be built which can give the

desired response without external trimming. Thus these circuits provide an important alternative for LSI system applications.

1.3. HISTORICAL BACKGROUND

The concept of switched capacitors is not new. The basic concept, and a suggestion that it should be applicable to monolithic integrated circuit technology, was outlined by Fried [9]. The author realized the equivalence between the sampled-data circuit and the simple RC filter, and also that it is feasible to introduce the concept in monolithic integrated circuit technology. However the concept was not further pursued because of the lack of availability of on-chip operational amplifiers in MOS LSI technology and also because of the heavy emphasis in recent years on other radically new methods of analog sampled-data filtering such as CCD transversal filters.

Considerable work has also been done on periodically operated switching networks. Sun and Frisch [10] have pointed out that the effective values of resistors can be increased by time-switching. The time-constant of the circuit is a function of both the duty cycle and the switching frequency. Thus for precise timing, both have to be accurately controlled. Another drawback is that the signal frequency range is limited by the rise and fall time of the controlling switching circuits. Fettweis [11] has given a steady-state solution to the problem of periodically operated switches, while Liou [12] has given an exact analysis using the state-space approach. Hirano and Nishimura [13] have extended the concept to active RC filters. They

have demonstrated that multiplication of resistances and multiplication of gyration conductances in an active RC network, and multiplication of transfer coefficients of controlled sources and negative impedance converters can be achieved by means of the switching technique. However the concept of switched capacitance, as discussed in this thesis, has not been evident in their work.

1.4. THESIS FORMAT

Chapter One introduces the concept of switched capacitor filtering, the state-of-the-art of other competing techniques of analog signal processing and the previous work in this field.

Chapter Two draws the equivalence between the basic switched capacitor network and a resistance, in both passive and active RC-circuits, and experimentally validates the introductory theory.

Chapter Three discusses the switched capacitor network from a more detailed analytic viewpoint. It also provides the design rules for synthesizing arbitrary filter functions using this technique.

Chapter Four discusses the effects of non-ideal behaviours of the different elements used in switched capacitor networks. It identifies the significant sources of non-ideal behaviour and suggests one possible means of improving the system response.

Chapter Five is the concluding chapter which summarizes the results drawn from this thesis and delineates further work to be done in this field.

CHAPTER TWO

SWITCHED CAPACITORS AS CIRCUIT ELEMENTS - PRELIMINARY INVESTIGATIONS AND EXPERIMENTS

2.1. INTRODUCTORY REMARKS

It has been stated in Chapter One that the basic element being studied consists of a capacitor and switches. For convenience, such a basic element will be called a "switched capacitor". In this chapter, the fundamental mathematical model of the switched capacitor filter will be analyzed and experimentally validated and the non-ideal properties following from its use will be presented.

Two different modes of transferring charge between different nodes of the circuit have been investigated. To differentiate between the two modes, the elements will be called "series switched capacitor" and "parallel switched capacitor". The series mode is discussed in Section 2.2. and the parallel mode in Section 2.3. Some aspects of the generalization of the continuous equivalence are discussed in Section 2.4.

The experiments were conducted on a test chip fabricated for this purpose. The test vehicle was fabricated at the Bell Northern Research Laboratories Limited, Ottawa, using an n-channel double polysilicon gate process. Further description of the test chip will be presented in Section 2.5. In Section 2.6., the passive first-order lowpass filter is examined. In Section 2.7. and 2.8. the transfer function of the active first-order lowpass filter, both series and parallel mode, are described. Section 2.9. discusses the response of

a synchronous multiple-clock active lowpass filter. In Section 2.10., a bandpass filter is presented, based on the theory presented for the discrete-time analog resonator.

2.2. SERIES SWITCHED CAPACITOR

The series switched capacitor is shown in Figure 2.1.(a). Initially it is assumed that both ports 1 and 2 are voltage-driven. Switches S_1 and S_2 are operated at the same periodic frequency, but conduct at different times. During the on-period of S_1 , the capacitor C_R is initialized, while during the on-period of S_2 , net charge $C_R(v_1 - v_2)$ is transferred. As this delivery occurs at every sampling interval T , this represents an average current flow of $C_R(v_1 - v_2)/T$. The network shown in Figure 2.1.(a), therefore simulates a resistor R of value

$$R = \frac{T}{C_R} \quad (2.1)$$

where T is the sampling interval

and C_R is the capacitance used in the "switched capacitance" element.

Eqn. (2.1.) indicates the possibility of simulating ratioed resistors by the switching of ratioed capacitors. Further, the resistive ratios can be varied by using different switching frequencies for different resistors.

2.3. PARALLEL SWITCHED CAPACITOR

An alternate version of the switched capacitor element is shown in Figure 2.1.(b); henceforth this element will be referred to as the

Fig. 2.1(a)

Fig. 2.1(b)

Fig. 2.1(a) Series switched capacitor

Fig. 2.1(b) Parallel switched capacitor.

parallel switched capacitor. Once again it is assumed that both the input and output ports are voltage driven. S_1 and S_2 are non-overlapping switches. During the on-period of S_1 , the capacitor C_R is pre-charged to the input voltage v_1 . During the on-period of S_2 , net charge $C_R(v_1 - v_2)$ is delivered to the output port. Reasoning similar to the series case thus leads also to eqn. 2.1. Although the end-results are the same for the elementary cases studied here, a closer look at the two elements using the sampled-data analysis (z-transform) will reveal fundamental differences. This subject will be considered in greater detail in Chapter Three.

2.4. EXTRAPOLATION TO RC-CIRCUIT AND FURTHER GENERALIZATION

The two previous sections introduce the concept of switched capacitors - series and parallel mode. It was also demonstrated that for both ports being voltage driven, the switched capacitor acts as a resistor on a global basis. For further demonstration and to indicate the generality of the concept, the simple passive RC-circuit and the corresponding series switched capacitive realization are considered, as shown in Figures 2.2.(a) and 2.2.(b) respectively. The ideal switches are replaced by MOS transistors, driven by non-overlapping two-phase clocks ϕ_1 and ϕ_2 , whose waveforms are shown in Figure 2.2.(c).

The equivalence between the two cases in Figures 2.2.(a) and 2.2.(b) may be derived by noting that in Figure 2.2.(a) the net transfer of charge between two times t_1 and t_2 in the RC-case is given by.

$$\Delta Q = \int_{t_1}^{t_2} i \, dt = \frac{v_1(t_2) - v_0(t_1)}{R} \quad (2.2)$$

Fig. 2.2(a)

Fig. 2.2(b)

Fig. 2.2(c)

Fig. 2.2(d)

Fig. 2.2(a) An R-C circuit.

Fig. 2.2(b) Its switched capacitor equivalent.

Fig. 2.2(c) Clocking schemes for the switched capacitor circuit.

Fig. 2.2(d) A more general R-C circuit.

where $v_i(t_2)$ is the input voltage at time t_2

$v_o(t_1)$ is the output voltage at time t_1

R is the value of the resistance

and $\delta t = t_2 - t_1$

Eqn. (2.2) has been derived on the assumption that the current i can be approximated by its trapezoidal approximation. This assumption requires that the initial and the final time, t_1 and t_2 respectively, be closely spaced compared to the RC-time constant.

The equivalent charge transferred in the switched capacitor circuit of Figure 2.2.(b) for clock period T is

$$\Delta Q = \{v_o(nT) - v_o[(n-1)T]\}C_L \quad (2.3)$$

where $v_o(nT)$ denotes the output voltage at the nT -th instant

$v_o[(n-1)T]$ denotes that at the $(n-1)T$ -th instant

C_L is the load capacitance

The voltage v_o may be obtained from the difference equation for the circuit as

$$v_o(nT) = v_o[(n-1)T] + \frac{C_R}{C_R + C_L} \{v_i(nT) - v_o[(n-1)T]\} \quad (2.4)$$

Combining eqns. (2.3.) and 2.4.),

$$\Delta Q = \{v_i(nT) - v_o[(n-1)T]\} \frac{C_L C_R}{C_L + C_R} \quad (2.5)$$

where nT and $(n-1)T$ correspond to t_2 and t_1 in eqn. (2.2) of the continuous case, and T corresponds to δt .

From eqns. (2.2) and (2.5), the equivalent resistor achieved by the switched capacitive network may be expressed as:

$$R = T \left(\frac{1}{C_R} + \frac{1}{C_L} \right) \quad (2.6)$$

If $C_L \gg C_R$, eqn. (2.6) reduces to eqn. (2.1). From eqn. (2.6), it follows that the effective time constant, measured in clock periods, is given by $(C_L + C_R)/C_R$, or approximately C_L/C_R in most cases.

A similar analysis for the parallel switched capacitor also leads to eqns. (2.5) and (2.6).

The above analysis is based on approximating the integral in eqn. (2.2) by the trapezoidal rule. In general this result is not valid. A more precise definition of the resistance would be a weighted average of eqns. (2.1) and (2.2).

Figure 2.2.(d) shows two nodes extracted from such a network where C_1 and C_2 represent the total capacitance to ground from the two nodes respectively, and the nodal voltages are v_1 and v_2 . The other circuit connections signify non-capacitive components, for example, resistors, amplifiers, etc.

The resistor R is now replaced by the switched capacitor equivalent (series mode). As before the unidirectional charge transfer between the two nodes is calculated, and equivalently to eqn. (2.2), the result is:

$$R = \frac{C_1 C_2 + (C_1 + C_2) C_R}{C_1 C_2 C_R} T \quad (2.7)$$

where C_1 , C_2 and C_R are the capacitances as described in Figure 2.2.(d).

A similar analysis performed for the parallel switched capacitor gives:

$$R = \frac{C_1 C_2 + (C_1 + C_2) C_R + C_R^2}{C_1 C_2 C_R} T \quad (2.8)$$

The difference between the two cases arises because, for the series switched capacitor, both capacitors C_1 and C_2 participate in the charge sharing simultaneously, while only one of them is involved at one time in the parallel switched capacitor.

It is seen that as the circuit complexity increases, the resistive equivalent equation becomes more and more complex. At this point it is necessary to contemplate whether the analogy between a switched capacitor element and a resistor is useful to carry further, especially when the exact solution is readily obtainable from the z-transform analysis. It is the contention of the author that the analogy is helpful in deriving knowledge from the continuous analog filter technology, and implementing this knowledge in switched capacitor filters.

Alternatively, the switched capacitor filter can be viewed as a sampled-data analog filter similar to recursive filters. However, it is not easy to dissociate the coefficients from the delay blocks, which appear in classical recursive formulations. Thus the approach taken in the dissertation is to consider the continuous equivalence as a

starting point in designing such filters and to explore the question as to how far we can carry the equivalence, while the sampled-data analysis is performed to determine the exact circuit behaviour.

2.5. DESCRIPTION OF THE TEST CHIP

As stated earlier, the experiments were conducted on a test chip fabricated for this purpose. The test chip contains binary-ratioed capacitors, n-channel MOS transistors acting as switches and an MOS amplifier with a feedback capacitor. The process technology was enhancement mode silicon-gate using two levels of polysilicon, so that the ratioed capacitors have polysilicon-oxide-polysilicon construction. The circuit diagram and a photomicrograph of the test chip are shown in Figures 2.3.(a) and 2.3. (b) respectively. The smallest capacitor (C_R in Figure 2.3 (a)) is of nominal value 1/2 pf. Suitable connections were provided so that both series and parallel switched capacitor modes could be simulated.

One objective of this design work was to minimize the chip area per RC-section. For that reason, the active element used was a single-ended amplifier, consisting of three cascaded inverting stages. Each inverting stage consisted of an enhancement mode driver-enhancement mode load pair [14].

The total chip dimension was 66 mils x 24 mils. As evident from the photomicrograph in Figure 2.3.(b), the major area in the test chip is taken by the integrating capacitor C. This was done to ensure the stability of the circuit.

Fig. 2.3(a)

Fig. 2.3(a) The circuit diagram of the chip.

Fig. 2.3(h) Photomicrograph of the chip.

2.6. SAMPLED-DATA ANALYSIS OF SWITCHED CAPACITOR NETWORKS-PASSIVE CASE

In the previous sections, the switched capacitor element was analyzed essentially as the replacement of resistors in the sampled-data domain. However such an analysis is valid only when the signal frequency is negligible compared to the sampling frequency. This limitation is, of course, severe. Hence, for a more accurate knowledge of the circuit behaviour the z-transform of the switched capacitor networks will be presented here.

As mentioned earlier, the switched capacitor circuits need non-overlapping two-phase clocks, ϕ_1 and ϕ_2 . During ϕ_1 , the switched capacitor element is initialized and during ϕ_2 , charge transfer between the input and output nodes occur. If the pulse-widths of ϕ_1 and ϕ_2 are such that the system reaches equilibrium condition within the ON-period of the clocks, the pulse-widths of the clocks do not affect the system response.

The difference equation which describes the circuit under the above condition is given by:

$$C_R(v_{i,n} - v_{o,n}) = C_L(v_{o,n} - v_{o,n-1}) \quad (2.9)$$

where C_R is the capacitance in the switched capacitor element

C_L is the load capacitance

$v_{i,n}$ denotes the input voltage at the nT -th instant

$v_{o,n}$ denotes the output voltage at the nT -th instant

and $v_{o,n-1}$ denotes that at $(n-1)T$ -th instant

The z-transform of eqn. (2.9) is:

$$C_R[V_i(z) - V_o(z)] = C_L V_o(z)[1 - z^{-1}] \quad (2.10)$$

where $V_i(z)$ denotes the z-transform of sampled input voltage v_i

$V_o(z)$ denotes the z-transform of sampled output voltage v_o

The transfer function of the circuit follows from eqn. (2.10) is:

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{C_R}{C_R + C_L(1 - z^{-1})} \quad (2.11)$$

Eqn. (2.11) describes the exact response of the circuit.

Figure 2.4.(a) shows the theoretical response of the circuit in

Figure 2.2.(b) for different ratios of C_R/C_L , obtained from the continuous equivalence approach [eqn. (2.6)] and the exact response [eqn. (2.11)]

It is observed that for small values of C_R/C_L the continuous equivalence approach coincides with the exact response except near the Nyquist

frequency; the reason being that the signal frequency may no longer be considered slowly varying compared to the sampling frequency - an

assumption made for deriving eqn. (2.1). It may also be noted that as

C_R becomes comparable to C_L , the transfer function deviates from the continuous equivalence for a greater range of frequency.

A similar analysis may be done for Figure 2.2.(b), after replacing the series switched capacitor with the parallel switched capacitor. The difference equation for this case is:

$$C_R(v_{i,n-1} - v_{o,n}) = C_L(v_{o,n} - v_{o,n-1}) \quad (2.12)$$

Corresponding transfer function is, therefore

Fig. 2.4(a)

Fig. 2.4(a) Theoretical response of the passive series switched capacitor circuit shown in Fig. 2.2(a).

$$H(z) = \frac{C_R z^{-1}}{C_R + C_L (1 - z^{-1})} \quad (2.13)$$

Comparing eqns. (2.11) and (2.13) reveal that there is an additional delay involved in the parallel case over the series case. As will be evident later, this introduces significant differences in the response of the recursive filter for the two modes.

The passive example was constructed using an on-chip series switched capacitor, an off-chip load capacitor and the amplifier not activated. As the switched capacitance is of very small value, necessary precautions had to be taken to avoid loading the circuit. For that purpose, an off-chip FET input operational amplifier (with input impedance of the order of $10^{12} \Omega$) was used. Furthermore to minimize the effect of stray capacitance, the connecting wires were properly shielded. The result of the experiment is shown in Figure 2.4.(b). The figure shows the frequency response for two capacitance loadings as marked. The third response was used to obtain an estimate of the stray capacitance. Including this estimated stray capacitance, the other two curves match the expected corner frequency and frequency roll-off closely with the continuous equivalence approach, except for signal frequencies which are comparable to the Nyquist limit, where a significant divergence occurs. The reason is that for such frequencies the signal amplitude varies by a large amount between sampling intervals, so that first-order interpolation is no longer valid, and the difference equation solution as in eqn. (2.9) must be employed. Alternatively this may be considered

Fig. 2.4(b)

Fig. 2.4(b) The frequency response (experimental) of the passive series switched capacitor circuit shown in Fig. 2.2(b).

as the aliasing effect, which raises the response near the Nyquist frequency. The exact z-transform solution, as in eqn. (2.11), validates the above statement.

At this point, it is necessary to contemplate the necessity to invoke the continuous equivalence approach, even though the exact solution to the problem is available. The reason is that this approach allows the designer to draw useful information from the active-RC filter technology and to implement it as a switched capacitor. However the sampled-data analysis may be necessary to derive the exact response of the system. This subject will be dealt with in further detail in Chapter Three.

2.7. ACTIVE SWITCHED CAPACITOR FILTER - SERIAL MODE

The analogy between the resistor and the switched capacitor filter naturally leads to the investigation of an active switched capacitor filter, which is analogous to the active-RC filter. The series mode is considered first as shown in Figure 2.5.(a). The active element may be either a single-ended amplifier with 180° phase shift between the input and the output, or a differential amplifier in the inverting mode as shown in Figure 2.5.(b). The clocks driving the complementary switches of the switched capacitor elements are non-overlapping but synchronous, operating at the sampling interval T . During the interval ϕ_1 , the switched capacitors C_i and C_f are initialized, while during the interval ϕ_2 , the input and output nodes deliver an amount of charge to the negative terminal of the amplifier, given by the difference equation:

Fig. 2.5(a)

Fig. 2.5(b)

Fig. 2.5(a) First-order active lowpass filter using the series switched capacitor.

Fig. 2.5(b) First-order active lowpass filter using the parallel switched capacitor.

$$C_i v_{i,n} + C_f v_{o,n} = -C[v_{o,n} - v_{o,n-1}] \quad (2.14)$$

where C_i is the capacitance of the input switched capacitor

C_f is the capacitance of the feedback switched capacitor

C is the integrating capacitor

$v_{i,n}$ denotes the sampled value of the input voltage at the

nT -th instant

$v_{o,n}$ denotes the sampled value of the output voltage at the

nT -th instant

$v_{o,n-1}$ denotes that at the $(n-1)T$ -th instant

The transfer function of the active serial switched capacitor filter follows from eqn. (2.14) as:

$$H(z) = \frac{V_o(z)}{V_i(z)} = - \frac{C_i}{C_f + C(1-z^{-1})} \quad (2.15)$$

Eqn. (2.15) represents a first-order lowpass sampled-data filter with the low-frequency gain being given by C_i/C_f , and the cutoff frequency in radians being given by,

$$\omega_{3dB} = \frac{1}{2T} \sin^{-1}[2\alpha + \alpha^2] \quad (2.16)$$

where ω_{3dB} is the cutoff frequency in radians of the first order lowpass filter

T is the sampling frequency

and α is the ratio of the feedback switched capacitor C_f

to the integrating capacitor C (i.e. $\alpha = C_f/C$)

It is interesting to note that for $\alpha \ll 1$, the cutoff frequency is identical to that derived from the continuous equivalence approach.

2.8. ACTIVE SWITCHED CAPACITOR FILTER - PARALLEL MODE

The parallel mode of the active switched capacitor filter is shown in Figure 2.5.(b). Except for the alternative mode of the switched capacitors, the circuit is identical to that in Figure 2.5.(a). During the ON-time of ϕ_1 , the switching capacitors C_i and C_f are charged to the voltages $v_{i,n-1}$ and $v_{o,n-1}$ respectively; while during the ON-time of ϕ_2 , the charges held on the switching capacitors are delivered to the input of the amplifier (negative terminal). The difference equation which describes this circuit is given by,

$$C_i v_{i,n-1} + C_f v_{o,n-1} = -C[v_{o,n} - v_{o,n-1}] \quad (2.17)$$

where C_i is the capacitance of the input parallel switched capacitor

C_f is the capacitance of the feedback parallel switched capacitor

$v_{i,n-1}$ is the input voltage at the $(n-1)T$ -th instant

$v_{o,n}$ is the output voltage at the nT -th instant

$v_{o,n-1}$ is that at $(n-1)T$ -th instant.

The transfer function for this sampled-data filter, is therefore, given by,

$$H(z) = \frac{V_o(z)}{V_i(z)} = - \frac{C_i z^{-1}}{C_f z^{-1} + C(1-z^{-1})} \quad (2.18)$$

A first-order sampled-data filter was built using the parallel switched capacitor, shown in Figure 2.5.(b). The low frequency gain of the switched capacitor filter is determined by the ratio C_1/C_f if the switched capacitors are operated at the same frequency.

Figure 2.6. shows the comparison between the theoretical and experimental results. The small difference between the two may be attributed to the inaccuracy in measuring the ratio C_R/C . The input switched capacitor is changed with values as noted, to change the DC closed loop gain but not the corner frequency.

The experiment was also performed for the first-order active lowpass filter using series switched capacitor in place of the parallel ones. Once again the theory agrees quite closely with the experiment, as in Figure 2.6.

2.9. MULTIPLE CLOCK SWITCHED FILTERS

In Section 2.2., it was mentioned that equivalent resistive values of the switched capacitors, i.e., the transfer function, may also be varied by running different switched capacitors at different sampling rates. In this section, analytical model for this case is developed.

The systems considered in this dissertation are linear and time-invariant (LTI). In order that the multiple clock switched filters be LTI systems, it is necessary that the clocks be synchronous, and be integrally related (or be a rational fraction).

Fig. 2.6 Comparison between theory and experiment for the first-order lowpass active filter. The solid line is the theoretical curve, the circle indicates the experimental, and the broken line, the continuous equivalent response. Sampling frequency = 50 kHz; $\alpha_f = C_f/C = 0.026$, $\alpha = C_f/C$, $f = 1, 2, 3, 4$ are indicated in the figure.

The system considered for investigation is shown in Figure 2.7. The switched capacitors are considered serial. The pulses driving the different switching capacitors are also shown in Figure 2.7. It is assumed that the sampling interval for the input switched capacitor is T and that for the feedback switched capacitor is mT , where m is an integral number. For ease of analysis, two hypothetical switches are incorporated, one at the input to the amplifier (negative end) operating at the sampling interval mT (same as ϕ_2'). The rest of the circuit is identical to that in Figure 2.5.

The difference equations describing this system are as follows:

$$\text{at time } (n+1)T, C_i v_{i,n+1} = -C[v'_{o,n+1} - v'_{o,n}] \quad (2.19a)$$

$$\text{" " } (n+2)T, C_i v_{i,n+2} = -C[v'_{o,n+2} - v'_{o,n+1}] \quad (2.19b)$$

$$\text{" " } (n+m-1)T, C_i v_{i,n+m-1} = -C[v'_{o,n+m-1} - v'_{o,n+m-2}] \quad (2.19c)$$

$$\text{" " } (n+m)T, C_i v_{i,n+m} + C_f v'_{o,n+m} = -C[v'_{o,n+m} - v'_{o,n+m-1}] \quad (2.19d)$$

where, C_i is the capacitance in the input switched capacitor

C_f is the capacitance in the feedback switched capacitor

C is the integrating capacitor

$v_{i,n}$ is the input voltage at time slot nT

$v'_{o,n}$ is the output voltage of the amplifier at time slot nT

The other subscripts for v_i and v'_o denote the time slots of interest.

Fig. 2.7

Fig. 2.7 First order active lowpass series switched capacitor filter using multiple clocks.

Adding up all the eqns. (2.19a) through (2.19d) gives:

$$C_i[v_{i,n+1} + v_{i,n+2} + \dots + v_{i,n+m-1} + v_{i,n+m}] + C_f v'_{o,n+m} = C[v'_{o,n+m} - v'_{o,n}] \quad (2.20)$$

Again, $v'_{o,n} = v_{o,n}$

$$v'_{o,n+m} = v_{o,n+m} \quad (2.21)$$

Therefore, from eqns. (2.20) and (2.21),

$$C_i[v_{i,n+1} + v_{i,n+2} + \dots + v_{i,n+m-1} + v_{i,n+m}] + C_f v_{o,n+m} = -C[v_{o,n+m} - v_{o,n}] \quad (2.22)$$

The z-transform of eqn. (2.22) gives

$$C_i V_i(z)[z + z^2 + \dots + z^m] + C_f V_o(z)z^m = C V_o(z)[z^m - 1] \quad (2.23)$$

Taking z^m common from both sides of eqn. (2.23), it becomes,

$$C_i V_i(z)[z^{-(m-1)} + z^{-(m-2)} + \dots + 1] = V_o(z)[C_f + C(1 - z^{-m})] \quad (2.24)$$

Simplifying (2.24),

$$C_i V_i(z) \frac{1 - z^{-m}}{1 - z^{-1}} = -V_o(z)[C_f + C(1 - z^{-m})] \quad (2.25)$$

Thus, the transfer function of the circuit shown in Figure 2.6 is:

$$H(z) = \frac{V_o(z)}{V_i(z)} = - \frac{C_i \frac{1 - z^{-m}}{1 - z^{-1}}}{C_f + C(1 - z^{-m})} \quad (2.26)$$

Eqn. (2.26) also represents a first-order lowpass filter.

If the sampling frequency is very high compared to the signal frequency ($\omega T \ll 1$), then

$$\frac{1 - z^{-m}}{1 - z^{-1}} = m \quad (2.27)$$

For this case, the low-frequency gain is being given by mC_i/C_f , and the cutoff frequency in radians being given by $f'_s C_f/C$ where f'_s is the sampling frequency of the feedback switched capacitor [$f'_s = 1/(mT)$]. It is also interesting to note that the aliasing effect occurs at the signal frequency $f'_s/2$. One further remark is that the low-frequency gain and the cutoff frequency follows more readily from the continuous equivalence approach, by replacing the switched capacitors by resistors as in eqn. (2.1).

The above theory was experimentally validated, as is shown in Figure 2.8. The figure shows the response of the system, along with the theoretical value of the response. Results agree fairly well, indicating the validity of the theory. One interesting fact to note is that aliasing occurs at half the lower sampling frequency (i.e. that of ϕ'_1 and ϕ'_2). This means that in practical cases, it is not feasible to arbitrarily lower the clock frequency without limiting the useful range of analog signal frequency.

A similar analysis may be done where the pulses driving the input and feedback switched capacitors are related as a rational fraction.

Fig. 2.8 Theoretical responses of the switched capacitor (series) filter using multiple clocks for the different switched capacitors. m is the ratio of the sampling interval for the feedback switched capacitor to that for the input switched capacitor.

Although the analysis is more involved, it leads once again to the conclusions as stated above. The analysis is presented in Appendix I. The series switched capacitor is considered above. Analysis may also be done for the parallel switched capacitor, which leads to results similar to Appendix I.

2.10. SWITCHED CAPACITOR BANDPASS FILTER

Finally the circuit to be investigated is a switched capacitor resonator, analogous to the bandpass active RC-filter. The circuits in Figures 2.5(a) and 2.5(b) contain the sampled-data versions of the basic building blocks required in designing continuous-time state-space realization of active RC-filters [15], viz. negative gain integrators and summers. Thus it naturally follows from the previous discussion to design a state-variable resonator consisting of negative gain integrators and summers.

One such circuit used for the realization of any second-order voltage transfer function is the so-called Biquad configuration [16]. This configuration has characteristically low sensitivity and remains stable with respect to changes in the passive components and the active devices [17]. It allows non-interactive variation of the resonant frequency and the selectivity by changing individual resistors.

In the previous sections, the switched capacitor filter has been used in a state variable type configuration. In such cases, the switched capacitor element may be approximated by resistors, provided the signal frequency is far lower than the sampling frequency.

Similarly, a bandpass filter was designed using the same chip in a state-variable type configuration, as shown in Figure 2.9. The transfer function realized is of the form:

$$H(s) = \frac{Gs}{s^2 + \frac{\omega_p}{Q_{po}} s + \omega_p^2} \quad (2.28)$$

where ω_p is the resonant frequency in radians per second

Q_{po} is the nominal selectivity

and GQ_{po}/ω_p is the gain at resonance.

The circuit required three of the test chips, and is shown in Figure 2.9. The block (C,f) denotes the switched capacitor whose resistive equivalent value is $1/fC$. The list of selected capacitors and frequency multiples used is shown at the bottom left of the figure.

In this filter, the gain at resonance is controlled by the ratio of the switched capacitor values only, and is independent of the value of C, provided that the signal frequency is low compared to the sampling frequency. Identical sampling frequencies f_1 and f_2 were used so that the gain was only determined by the capacitive ratio C_1/C_2 . The selectivity Q of the filter was adjusted by varying the frequency ratio f_4/f_2 , using equal values of capacitors, $C_2 = C_4$. All clocks were synchronized to a master clock of frequency f_0 (=125 KHz).

$C_1 = 4C_R$	$f_1 = f_0/8$
$C_2 = C_R$	$f_2 = f_0/8$
$C_3 = C_R$	$f_3 = f_0$
$C_4 = C_R$	$f_4 = f_0$
$C_5 = C_R$	$f_5 = 8f_0$
$C_6 = C_R$	$f_6 = 8f_0$
$C_7 = C_R$	$f_7 = f_0/4$

Fig. 2.9 A second order active bandpass switched capacitor circuit using the biquad configuration.

Fig. 2.10 The frequency response of the circuit shown in Fig. 2.9 (experimental).

The unit II in Figure 2.9. must function as an inverting amplifier of gain unity. To suppress clock feedthrough, the relatively large integrating capacitor C was used, and the frequencies for the switched capacitors in unit II were increased by a factor of eight to make the corner frequency of unit II relatively high. The frequency response of the circuit is shown in Figure 2.10. The center frequency for the bandpass filter is at approximately 500 Hz. The broken curve shows the second-order bandpass transfer function, while the solid curve is the second-order lowpass function. The measured Q of the filter is 7.07 compared to a theoretical Q of 8. The slopes of the transfer functions beyond the resonant frequency are seen to correspond closely to the theoretical (continuous equivalence) roll-off for the bandpass and lowpass functions. However the slope of the bandpass transfer function does not follow the 6 dB/octave roll-off near the low-frequency limit of the circuit because of the additional feedback resistance used for the integrating block (unit III in Figure 2.10.).

Although aliasing occurs above the lowest clock frequency in the circuit, the response has been shown for the extended frequency range, to indicate the amplitude of clock feedthrough. In the lowpass transfer function, the first feedthrough peak occurs at a frequency corresponding to f_1 and f_2 (15.625 KHz), while the next peak occurs at the frequency corresponding to f_7 (31.25 KHz).

The above analysis was done using the continuous equivalence approach. However, this is valid only if the frequency range of

interest (i.e. the resonant frequency and half-power points) is negligible compared to the sampling frequency. This is too strict a limitation. In the more general case, the z-transform approach has to be used. The topic will be discussed in detail in Chapter Three.

CHAPTER THREE

DESIGN APPROACH FOR SWITCHED CAPACITOR MOS LSI FILTERS

3.1 Introduction

The previous chapters have outlined the work (original to this thesis) which validated the concept of switched capacitor filters in MOS LSI. The aim of this chapter is to establish the methods for designing an arbitrary filter function using switched capacitor circuits and to explore the possibility of realizing these filters on MOS integrated circuits, taking into consideration the limitations of the technology.

Section 3.2 deals with the realizability of IIR filters by switched capacitors. Section 3.3 formulates the design procedure for realizing filters using the series switched capacitor mode. The design procedure is then applied in realizing an infinite-gain multiple feedback filter in section 3.4, and notch filter in section 3.5. Section 3.6 deals with realizing switched capacitor filter using the parallel mode. In section 3.7, a design procedure is laid down for realizing filter using the bilinear transformation mode of switched capacitor circuits. In section 3.8, the design procedure is applied in the case of a lowpass filter. Finally, in section 3.9, a practical demonstration of the above mentioned design procedure for constructing a variable amplitude- and phase equaliser is shown.

3.2 Realizability of IIR Filters by Switched Capacitors

The switched capacitor filter is a discrete-time analog filter. Infinite impulse response (IIR) filters can therefore be designed using switched capacitors as basic elements. One popular way of designing IIR filters is to begin with an appropriate continuous time filter and digitize the resulting design to give the sampled-data filter. This method is most useful for designing standard filters such as lowpass, bandpass, bandstop and high pass filters where a considerable body of theory on continuous time filters is available [18].

The most general form of the z-transform of IIR filters can be written as

$$H(z) = \frac{\sum_{i=0}^M b_i z^{-i}}{1 + \sum_{i=1}^N a_i z^{-i}} \quad (3.1)$$

where a_i 's and b_i 's are the coefficients of the filter. The problem of designing the sampled-data filter is one of finding the filter coefficients, viz. a_i 's and b_i 's. As stated earlier one popular approach in designing such filters is to transform an existing analog filter to an "equivalent" sampled-data filter, i.e., simple mapping procedures can be used to transform filters in one domain to filters in the other domain.

3.2a Backward Difference Formulation

In order to appreciate how switched capacitors can be used to form IIR filters, the switched capacitor integrator circuit is investigated more closely. The active RC integrator and its series switched capacitor equivalent are shown in Figures 3.1a and 3.1b respectively.

For Figure 3.1a, the transfer function is given by

$$H(s) = \frac{V_o(s)}{V_i(s)} = -\frac{1}{sRC} = -\frac{\alpha_R C}{sTC} \quad (3.2)$$

where eqn. (3.1) is used to replace the resistor by equivalent switched capacitor.

By analysis similar to that in section 2.7, the sampled-data transfer function for the circuit in Figure 3.1b is given by

$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{\alpha_R}{C(1-z^{-1})} \quad (3.3)$$

Fig. 3.1(a)

Fig. 3.1(b)

Fig. 3.1(c)

Fig. 3.1(a) An R-C integrator

Fig. 3.1(b) A series switched capacitor integrator.

Fig. 3.1(c) A parallel switched capacitor integrator.

If the transfer function $H(z)$ is identical to $H(s)$ within the Nyquist frequency, it can be seen that eqn. (3.3) is obtained from eqn. (3.2) by replacing s by,

$$s = \frac{1-z^{-1}}{T} \quad (3.5)$$

Essentially what this means is that series-switched capacitor filters can be derived from continuous time filters by using the transformation given by eqn. (3.4) providing the generality of doing so can be validated. This is the so-called backward difference transformation in "digitizing" the analog filter [19]. Some of the implications of the transformation have been tacitly introduced in Chapter Two (Section 2.6.). The properties of the transformation and their effect on the design of series switched capacitor filter circuits will be reviewed now in greater detail.

Two desirable properties of mapping from the continuous to discrete space are [20],

"1. The $j\Omega$ axis in the s -plane should be mapped to the unit circle in the z -plane,

2. Points in the left half s -plane ($\text{Re}[s] < 0$) should be mapped inside the unit circle ($|z| < 1$).

Property 1 preserves (through the uniformity of the mapping) the frequency selective properties of the continuous system, whereas property 2 ensures that stable continuous systems (filters) are mapped into stable discrete systems."

To study these two properties in the series switched capacitor circuit, which satisfies the backward difference transformation, we note that the latter is used to make the replacement,

$$\frac{dy}{dt} \rightarrow \frac{y(n) - y(n-1)}{T} \quad (3.5)$$

where, dy/dt denotes the first differential of y with respect to time, t

T denotes the sampling interval in time

$y(n)$ denotes the value of y at the nT -th instant

$y(n-1)$ denotes that at $(n-1)T$ -th instant

In terms of operators, this corresponds to,

$$s = \frac{1-z^{-1}}{T} \quad (3.4)$$

or,
$$z = \frac{1}{1-sT}$$

To examine property 1, let $s=j\Omega$. Then eqn. (3.4) may be written, after some algebraic manipulation, as [19],

$$\left\{ \operatorname{Re}[z] - \frac{1}{2} \right\}^2 + \left\{ \operatorname{Im}[z] \right\}^2 = \left(\frac{1}{2} \right)^2 \quad (3.7)$$

This represents a circle on the z -plane. The mapping is described in Figure 3.2.a. From the figure, it is evident that except for small values of ΩT , the mapping of the $j\Omega$ axis on the z -plane does not lie on the unit circle in the z -plane. Thus property 1, in general, is not satisfied.

Fig. 3.2(a)

Fig. 3.2(b)

Fig. 3.2(a) s-plane to z-plane mapping of $j\Omega$ axis for backward difference method.

Fig. 3.2(b) s-plane to z-plane mapping of $j\Omega$ axis for forward difference method.

To determine if property 2 is satisfied, let

$$sT = \alpha + j\beta \quad (3.8)$$

where α and β are real and let $\alpha < 0$. Then from eqn. (3.6), it is easy to see

$$|z| = \frac{1}{\sqrt{(1-\alpha)^2 + \beta^2}} < 1 \quad (3.9)$$

which indicates that property 2 is satisfied. This means that sampled-data filters designed using the backward difference formulation will be stable, if the analog equivalent is stable. However the frequency selective property of the filter is not maintained.

3.2.b) FORWARD DIFFERENCE FORMULATION

Similar to the analysis for the series switched capacitor, analysis may also be done for the parallel switched capacitor circuit. The circuit is shown in Figure 3.1.c. Analysis follows as in Section 2.8. The transfer function is given by,

$$H(z) = \frac{V_o(z)}{V_i(z)} = - \frac{a_R C z^{-1}}{C(1-z^{-1})} = - \frac{a_R C}{C(z-1)} \quad (3.10)$$

As before, if the transfer function $H(z)$ in (3.10) is to be identical to $H(s)$ in (3.2), the replacement involved is,

$$s = \frac{z-1}{T} \quad (3.11)$$

$$\text{or, } z = 1 + sT \quad (3.12)$$

Physically, this method uses the replacement

$$\frac{dy}{dt} \rightarrow \frac{y(n+1) - y(n)}{T} \quad (3.13)$$

where, dy/dt denotes the first differential of y with respect to time, t

T denotes the sampling interval in time

$y(n)$ denotes the value of y at the nT -th instant

$y(n+1)$ denotes that at $(n+1)T$ -th instant

Thus it is noted that both forward and backward difference techniques essentially mean the mapping of the differential, i.e. replacing a first-order differential by a backward or forward difference equation.

Once again to test property 1 for this transformation, let $s = j\Omega$. Eqn. (3.12) shows

$$z = 1 + j\Omega T \quad (3.14)$$

This mapping is described in Figure 3.2.b. Once again it is observed that except for small values of ΩT , the image of the $j\Omega$ -axis in the s -plane does not correspond to the unit circle in the z -plane, i.e. property 1 is not satisfied.

To test property 2, let $sT = \alpha + j\beta$, $\alpha < 0$. Then,

$$z = \sqrt{(1+\alpha)^2 + \beta^2} \quad (3.15)$$

From eqn. (3.14) follows the fact that

$$|z| > 1 \quad (3.16)$$

when $\beta^2 > 1 - (1+\alpha)^2$ (3.17)

i.e. property 2 is not satisfied when the inequality (3.16) occurs. Thus even if the analog filter is a stable filter, the corresponding digital filter, using the forward difference formulation, is not necessarily stable.

From the study of the two design methods, it is evident that the series switched capacitor circuit is more advantageous than the parallel version, as the stability of the former is always ensured. Furthermore both the design methods suffer from inability to maintain the frequency selective properties. However, it is possible to improve upon the frequency properties by certain approximation techniques. This will be discussed in design method I in Section 3.3.

3.2.c) BILINEAR TRANSFORMATION

The bilinear transformation is a more ideal mapping than the others mentioned earlier. Therefore, efforts were made to inquire if the bilinear transformation could be implemented using switched capacitor networks. To investigate this, vector diagrams for the two types of integrators, series and parallel, were studied. The real frequency domain behaviour is obtained by replacing $s=j\omega$ in eqn. (3.2) for the active RC integrator and by $z=e^{j\omega T}$ in eqns. (3.3) and (3.10) as follows:

$$H(j\omega) = - \frac{\alpha_R}{j\omega T} \quad (3.18)$$

$$H(e^{j\omega T}) = - \frac{-\alpha_R}{1-e^{-j\omega T}} \quad (3.19)$$

for the series switched capacitor integrator, and

$$H(e^{j\omega T}) = - \frac{\alpha_R}{e^{j\omega T} - 1} \quad (3.20)$$

for the parallel switched capacitor integrator.

The vector diagrams describing the sampled-data integrators, given by eqns. (3.19) and (3.20) are depicted in Figures 3.3.a and 3.3.b respectively. The ideal response, as given by eqn. (3.18) is shown in both figures. It is observed that while at any particular value of ωT , the phase angle of the vector $-\alpha_R/(1-e^{-j\omega T})$ is more than $\pi/2$, that for $-\alpha_R/(e^{j\omega T}-1)$ is less than $\pi/2$. It is intuitively obvious that if the parallel and series switched capacitors can be suitably combined, it may be able to restore the phase shift to the ideal value, i.e. $\pi/2$. One possible combination to obtain that is shown in Figure 3.4.a. A closer look at the circuit indicates that the two sets of switches may be integrated in one, as shown in Figure 3.4.b.

The sampled-data transfer function of the circuit shown in Figure 3.4 is (for both cases):

$$H(z) = - \alpha_R \frac{1+z^{-1}}{1-z^{-1}} \quad (3.21)$$

Fig. 3.3(a)

Fig. 3.3(b)

Fig. 3.3(a) Vector diagram to illustrate the response of series switched capacitor integrator.

Fig. 3.3(b) Vector diagram to illustrate the response of parallel switched capacitor integrator.

The continuous equivalent analog integrator gives (by eqn. [2.1]):

$$H(s) = 2a_R/sT \quad (3.22)$$

From eqns. (3.21) and (3.22), it is observed that the new integrator circuit in Figure 3.4. may be obtained from its analog equivalent integrator by replacing s by:

$$s = \frac{2}{T} \cdot \frac{1-z^{-1}}{1+z^{-1}} \quad (3.23)$$

It is immediately realized that this new circuit utilizes the bilinear transformation to obtain the sampled-data integrator from the analog circuit. An alternate circuit has recently been reported [45].

The bilinear transformation is a simple conformal mapping from the s -plane to the z -plane, defined by

$$s = \frac{2}{T} \cdot \frac{1-z^{-1}}{1+z^{-1}} \quad (3.24)$$

or,
$$z = \frac{\frac{2}{T} + s}{\frac{2}{T} - s} \quad (3.25)$$

From (3.25), replacing $s=j\Omega$ gives, $|z|=1$, i.e. property 1 is preserved. Figure 3.5.a describes the mapping from the s -plane to the z -plane.

Fig. 3.4(a)

Fig. 3.4(b)

Fig. 3.4(a) Proposed switched capacitor integrator using the bilinear transformation.

Fig. 3.4(b) Improved version of the integrator in Fig. 3.4(a).

To test property 2, once again, let $sT = \alpha + j\beta$, $\alpha < 0$; then, from eqn. (3.25),

$$|z| = \left[\frac{(2+\alpha)^2 + \beta^2}{(2-\alpha)^2 + \beta^2} \right]^{1/2} \quad (3.26)$$

i.e. $|z| < 1$ for $\alpha < 0$, which means that property 2 is satisfied too. Thus, the bilinear transformation seems ideal for designing such filters. However there are disadvantages, the major one being the "frequency warping" property of the bilinear transformation. This property is evident from eqn. (3.25). Thus when $\Omega=0$, $z=1$; when $\Omega=\infty$, $z=-1$; between these limits the angle of z varies from 0 to π ; i.e. the entire real frequency (Ω) axis is in the s -plane and is mapped between $z=+1$ and $z=-1$ (i.e. between the zero and the Nyquist frequency). This indicates a highly non-linear relationship between analog frequency Ω and digital frequency, ω . Mathematically this is expressed as,

$$\Omega \rightarrow \frac{2}{T} \tan \frac{\omega T}{2} \quad (3.27)$$

The relationship between the analog frequency and the digital frequency is described in Figure 3.5.b. The bilinear transformation cannot be used to realize a filter characteristic having discontinuities. However the filter characteristics may be approximated by a piece-wise constant function and then be realized.

Fig. 3.5(a)

Fig. 3.5(b)

Fig. 3.5(a) s-plane to z-plane transformation for bilinear transformation.

Fig. 3.5(b) Relation between analog frequency Ω and its transformed sampled-data frequency ω .

3.3. DESIGN METHOD FOR SERIES SWITCHED CAPACITOR FILTERS

In Section 3.2. it was indicated that the bilinear transformation switched capacitor circuit is suitable for synthesizing any transfer function. However there will be situations where the use of bilinear transformation elements may not be suitable, because of larger chip area needed to realize two switched capacitors instead of one; larger required resolution of the halved capacitors, which also means larger chip area; and required precise balance of the parallel and series switched capacitors. In such cases, singular switched capacitor elements (like series or parallel) become important. Hence a design method will be presented for the series (and parallel) switched capacitor filters, taking into consideration the limitations of such circuits viz. to be able to realize high Q filters with (1) as low spread of capacitor values as possible, and also (2) as low sensitivity to variations of different parameters as possible. The earlier factor is important for optimizing the area of the chip, and the latter factor is to ensure the reproducibility of the filter, in spite of the parametric variations of capacitors and operational amplifiers.

Before proceeding with the design approach, it seems necessary to present the context for this design approach. Methods (a) and (b), described in Section 3.2., which involved the replacement of differentials by finite differences, have the advantage that the z -transform of the sampled-data filter can be trivially derived from the Laplace Transform (transfer function) of the analog filter by an algebraic substitution. From the circuit point of view, it means that the design formulas maintain the form of the equivalent continuous active filter equations

and that the topology of the continuous filter is also preserved. However such realizations suffer from the fact that except for small values of the signal frequency relative to the sampling frequency, the frequency selective properties of the equivalent continuous system cannot be preserved.

Therefore synthesizing such filters based on continuous equivalence poses a problem. It is possible to utilize computer-aided design methods for synthesizing such filters [43,44]. This method utilizes the computer to compute the coefficients from the data of a given transfer function to be realized. It involves the solution of a set of linear or non-linear equations. However, even for obtaining coefficients of a second order transfer function, partial derivatives of an error function with seven variables have to be solved. An insight into the sensitivity of the poles, resonant frequency and Q of the filter may not be obtained in this approach.

Hence an alternative design method, which is simpler to compute, and which also provides an insight into the behaviour of the circuit for parametric variation becomes necessary. The design method presented here is one such alternative.

It has been indicated by a previous author [21] that the sensitivity of the circuit increases as the centre frequency of a frequency selective network becomes comparable to the sampling frequency. Furthermore, for good noise performance, the sampling frequency should be as high as possible. Thus, for a design requirement that the sampling frequency is large compared to the resonant frequency.

(as, for example, $\omega T \leq 1$), the following method is quite satisfactory to predict the filter coefficients. This method is based on the fact that if the series or parallel switched capacitor circuit is employed, using the continuous equivalence approach while transforming from the s-domain to the z-domain, the poles are caused to shift away from their required values. For example, if eqn. (2.1) is used to design a high Q filter using the series switched capacitor elements, it will have a degraded Q factor. This is evident from Figure 3.6. For a high Q filter, the poles in the z-domain should be very near to the unity circle. However, the backward difference transformation is such that the transformed poles from the s-plane to the z-plane are shifted away from the unity circle (Figure 3.6.b). The poles will however remain inside the unity circle. Hence such a filter will be stable, but will have a degraded Q factor. So the aim is to restore the frequency properties of its continuous analog by modifying the poles, as shown in Figure 3.6.b. If some correction factors may be incorporated into the design equations to account for the shift in poles, the frequency selectivity property of the circuit may be restored.

In order to evaluate the required correction terms, the backward difference formulation equation is re-examined again as follows:

$$s \rightarrow \frac{1-z^{-1}}{T} \quad (3.4)$$

For real frequencies, this means $j\omega T$ is mapped to $(1 - \cos \omega T + j \sin \omega T)$

By series expansion, the above equation may be written as,

$$j\omega T \rightarrow j\omega T \left[1 - \frac{(\omega T)^2}{3!} + \frac{(\omega T)^4}{5!} - \dots - j \left\{ \frac{\omega T}{2!} - \frac{(\omega T)^3}{4!} + \dots \right\} \right] \quad (3.28)$$

Fig. 3.6(a) Poles for high Q filter in s -plane.

Fig. 3.6(b) Figure illustrating the shift in poles by using the backward difference transformation and also modifying the poles to restore the frequency characteristics.

The quantity in parenthesis shows the perturbation on the real frequency that is encountered by the sampling action. Therefore for any frequency selective circuit, if the above perturbation may be evaluated at or near the frequency of interest, then it may be corrected for. Thus the frequency selectivity property may be restored.

i.e. assuming that ω_0 is the frequency of interest and the transfer function, $H(e^{j\omega T})$, of the given circuit is known, $H(e^{j\omega_0 T})$ may be simplified by eqn. (3.28). As for example if $\omega_0 T \ll 1$, the quantity in parenthesis becomes approximately equal to unity. In that case, the continuous equivalence expression would have been completely valid. However, as $\omega_0 T$ becomes larger, more and more correction terms have to be incorporated. If only second-order correction is sufficient, then eqn. (3.28) becomes

$$j\omega_0 T = j\omega_0 T \left[1 - \frac{(\omega_0 T)^2}{3!} - j \frac{\omega_0 T}{2!} \right] \quad (3.29)$$

Thus, using eqn. (3.29), $H(e^{j\omega_0 T})$ may be written in the same form as the continuous equivalence. By comparing the two equations, it is possible to formulate the important filter equations, incorporating the effect of sampling on the switched capacitor filter. The algorithm for the design method may then be laid down as follows:

- 1) From the filter specifications and for the topology chosen, the type of analog filter and its order are determined.

2) From the topology chosen, the transfer function in the z -domain, $H(z)$ may be derived by substituting for s according to eqn. (3.4). Using $z=e^{j\omega T}$, and determining the frequency at which the best fit of the switched capacitor filter to the desired transfer function is required, a simplified transfer function may be written in a form similar to $H(j\omega)$ rather than $H(e^{j\omega T})$. Then the equations for the filter characteristics can be derived by comparing with the continuous equivalent transfer function. The derived equations would indicate the perturbations on the s -domain equations because of the sampling action.

3) If the filter characteristics are specified, then the above-mentioned equations may be used to obtain the filter coefficients. Alternatively these equations can also be used to derive the filter coefficients, given the resistances and capacitances, obtained from an already existing continuous filter design method. This will be explained through two examples in the next section.

To summarize the above algorithm the design approach presented here uses first-order correction terms of approximating the differential equation of the continuous analog filter by the backward difference equation for series switched capacitor elements. Then, the design equations are made to fit the required transfer function at the resonant frequency of the circuit, or near it (e.g. the 3 dB points). It is understood that this is only a first-order approximation to the desired transfer function. Nevertheless it will be observed in the next section that for the case where the sampling frequency is large

compared to the resonant frequency (as for example, $\omega T \leq 1$), the method is quite satisfactory to predict the filter coefficients. Furthermore, it also predicts the sensitivity of the filter characteristics to the sampling frequency. Thus it provides an insight into the behaviour of the filter under practical circumstances.

As the sampling frequency becomes larger, more correction terms will be necessary. The modifications on the design equations become more cumbersome. In the general case, the closed form solution will have to be used. In such cases, the above design method becomes inapplicable.

To illustrate the method, a switched capacitor biquad resonator as shown in Figure 3.7. is investigated. The transfer function is given by,

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{\alpha_1(1-z^{-1})}{(1-z^{-1})^2 + \alpha_2(1-z^{-1}) + \alpha_3 \alpha_4} \quad (3.30)$$

where the α 's are the coefficients of the various switched capacitor elements, as illustrated in Figure 3.7.

The method of obtaining this transfer function is by substitution from the continuous equivalent expression by using eqns. (2.1) and (3.4) (i.e. backward difference formulation for series switched capacitor case). As in eqns. (3.29), for $\omega T \ll 1$, $(1-z^{-1})$ may then be simplified as,

$$(1-z^{-1}) \Big|_{z=e^{j\omega T}} \approx j\omega T \left[1 - \frac{(\omega T)^2}{3!} - j \frac{\omega T}{2!} \right] \quad (3.31)$$

Replacing (3.31) in eqn. (3.30) and after some manipulation eqn. (3.30) may be reformulated as,

Fig. 3.7

Fig. 3.7 A switched capacitor (series) biquad resonator.

$$H(z) \Big|_{z=e^{j\omega T}} = \frac{-j\omega \frac{\alpha_1}{T} \left[\left\{ 1 - \frac{(\omega T)^2}{6} \right\} - j \frac{1}{2} (\omega T) \right]}{\left[1 - \frac{\alpha_2}{2} \right] \left[-\omega^2 + j\omega \frac{\alpha_2}{T} \left\{ 1 + (\omega T)^2 \left(\frac{1}{\alpha_2} - \frac{1}{6} \right) \right\} \left(1 - \frac{\alpha_2}{2} \right) + \frac{\alpha_3 \alpha_4}{1 - \frac{\alpha_2}{2}} \right]} \quad (3.32)$$

Note the analogy of this expression to the continuous active equivalent one. Recalling that the aim is to approximate the function to the continuous equivalent equation near the resonant frequency, eqn. (3.32) is rewritten as,

$$H(e^{j\omega T}) \Big|_{\omega \rightarrow \omega_0} = \frac{-j\omega \frac{\alpha_1}{T} \left[\left\{ 1 - (\omega_0 T)^2 \right\} - j \frac{1}{2} (\omega_0 T) \right] / \left[1 - \frac{\alpha_2}{2} \right]}{-\omega^2 + j\omega \frac{\alpha_2}{T} \left[1 + (\omega_0 T)^2 \left(\frac{1}{\alpha_2} - \frac{1}{6} \right) \left(1 - \frac{1}{\alpha_2} \right) + \frac{\alpha_3 \alpha_4}{T^2} \left(1 - \frac{\alpha_2}{2} \right) \right]} \quad (3.33)$$

Note that eqn. (3.33) is a linear second-order transfer function, similar to the continuous equivalent circuit. The important filter characteristics can therefore be identified by comparing eqn. (3.33) with its linear counterpart (eqn. 3.34). This is illustrated in Table I. To observe the equivalence between this equation and that of the continuous equivalent circuit, the various switched capacitors $\alpha_1 C$, $\alpha_2 C$, $\alpha_3 C$ and $\alpha_4 C$ are replaced by their resistive equivalents as defined by eqn. (2.1). The transfer function of the simulated system is given by,

$$H(j\omega) = \frac{-j\omega \frac{\alpha_1}{T}}{-\omega^2 + j\omega \frac{\alpha_2}{T} + \frac{\alpha_3 \alpha_4}{T^2}} \quad (3.34)$$

where α_1 , α_2 , α_3 and α_4 are coefficients which give the desired response for the continuous case; i.e. $H(j\omega_0)$ is identical to $H(e^{j\omega_0 T})$. The filter characteristics for the approximate expression (3.33) and eqn. (3.34) are compared in Table I. The closed form solution is also presented for comparison. Note the apparent similarity between the continuous expression and the modified expression, which incorporates the first-order effect of the sampling frequency on the transfer function. Also note the simplicity of the expression as compared to the closed form solution.

Based on the equations in Table I, various circuit parameters have been derived for two bandpass filters, a low Q case (center frequency of 500 Hz, Q of 5, gain of 1 and the sampling frequency 32 KHz), and a high Q case (Q of 50, gain of 5 at resonant frequency other parameters being same). For the latter case, negative values of α_2 may be obtained by taking the local feedback α_2 from output v_o in Figure 3.7. Computer simulations, comparing the results in the three cases, are illustrated in Figures 3.8.(a) and 3.8.(b). It is evident that the approximate solution fits closely with the theory.

Considering the fact that the results correspond closely for the exact and approximate solutions, sensitivity analysis* may be done based on the approximate expressions of this work which are more straightforward than those from the exact solution; (for comparison the continuous equivalence case is shown).

* The sensitivity in the above analysis has been defined for a quantity H to a variation in a parameter x in the usual manner as:

$$S_x^H = \frac{\delta H}{\delta x} \cdot \frac{x}{H}$$

TABLE 1

<u>Filter Parameters</u>	<u>Closed Form Equations</u>	<u>Continuous Equivalent Expressions</u>	<u>Modified Expression Obtained from Design Method.</u>
Center frequency, ω_0 radians per second	$f_s \cos^{-1} \frac{1 + \frac{\alpha_2}{2}}{[1 + \alpha_2 + \alpha_3 \alpha_4 \beta]^{1/2}}$	$f_s \frac{\sqrt{\alpha_3 \alpha_4}}{\alpha_2}$	$f_s \frac{\sqrt{\alpha_3 \alpha_4}}{\sqrt{1 - \alpha_2/2}}$
Quality of the poles, Q	$\cos^{-1} \frac{1 + \frac{\alpha_2}{2}}{[1 + \alpha_2 + \alpha_3 \alpha_4 \beta]^{1/2}}$ $\log_e \left[\frac{1}{1 + \alpha_2 + \alpha_3 \alpha_4 \beta} \right]^{1/2}$	$\frac{\sqrt{\alpha_3 \alpha_4}}{\alpha_2}$	$\frac{\sqrt{\alpha_3 \alpha_4}}{\alpha_2} \frac{\sqrt{1 - \alpha_2/2}}{(1 + (\omega_0 T)^2 (1/\alpha_2 - 1/6))}$
Gain at resonance, G	$H(e^{j\omega_0 T})$	$\frac{\alpha_1}{\alpha_2}$	$\frac{\alpha_1}{\alpha_2} \frac{[1 - (\omega_0 T)^2/24]}{[1 + (\omega_0 T)^2 (1/\alpha_2 - 1/6)]}$

3.8(a) Comparison of frequency responses for the respective design approaches and low Q case.

Fig. 3.8(b) Comparison of frequency responses for the respective design approaches: high Q case. The negative value of α_2 is obtained by taking the local feedback (α_2) from output.

2

Switched Capacitor Case

$$S_{\alpha_1}^{\omega_0} = 0$$

$$S_{\alpha_2}^{\omega_0} = \frac{1}{2} \frac{\alpha_2}{2^{-\alpha_2}}$$

$$S_{\alpha_3}^{\omega_0} = S_{\alpha_4}^{\omega_0} = \frac{1}{2}$$

Continuous Equivalence Case

$$S_{\alpha_1}^{\omega_0} = 0 \quad (3.35a)$$

$$S_{\alpha_2}^{\omega_0} = 0 \quad (3.35b)$$

$$S_{\alpha_3}^{\omega_0} = S_{\alpha_4}^{\omega_0} = \frac{1}{2} \quad (3.35c)$$

and, for $\alpha_2 \ll 1$, the following relations may be derived for $\Delta\omega$ and Q

Switched Capacitor Case

$$S_{\alpha_1}^{\Delta\omega} = 0$$

$$S_{\alpha_2}^{\Delta\omega} = \frac{1 + \alpha_3 \alpha_4 / 2}{1 + \alpha_3 \alpha_4 / \alpha_2}$$

$$\approx \frac{1 + (\omega_0^T)^2 / 2}{1 + (\omega_0^T)^2 / \alpha_2}$$

$$S_{\alpha_3}^{\Delta\omega} = S_{\alpha_4}^{\Delta\omega} = \frac{\alpha_3 \alpha_4}{\alpha_2 + \alpha_3 \alpha_4}$$

$$\approx \frac{(\omega_0^T)^2}{\alpha_2 + (\omega_0^T)^2}$$

Continuous Equivalence Case

$$S_{\alpha_1}^{\Delta\omega} = 0 \quad (3.36a)$$

$$S_{\alpha_2}^{\Delta\omega} = 1 \quad (3.36b)$$

$$S_{\alpha_3}^{\Delta\omega} = S_{\alpha_4}^{\Delta\omega} = 0 \quad (3.36c)$$

Switched Capacitor Case

$$S_{\alpha_2}^Q = - \frac{\alpha_2}{\sqrt{\alpha_3 \alpha_4}} Q$$

$$= - \frac{\alpha_2}{\omega_0 T} Q$$

$$S_{\alpha_3}^Q = S_{\alpha_4}^Q = \frac{1}{2} [\alpha_2 - \alpha_3 \alpha_4]$$

$$= \frac{1}{2} [\alpha_2 - (\omega_0 T)^2]$$

Continuous Equivalence Case

$$S_{\alpha_2}^Q = -1 \quad (3.37a)$$

$$S_{\alpha_3}^Q = S_{\alpha_4}^Q = \frac{1}{2} \quad (3.37b)$$

These results are essentially the continuous active equivalent sensitivity equations with correction factors due to the sampling action.

These equations have interesting implications. It is observed that the sensitivity of the resonant frequency, ω_0 , to the various coefficients approaches that of its continuous counterpart. However, that of the bandwidth, or of the Q of the filter is strongly influenced by the sampling frequency. This is implied by the presence of the factor $(\omega_0 T)$ in the equation. Furthermore, for high Q filters, α_2 is negative. Hence the sensitivity of the bandwidth and also that of the Q of the filter is higher than unity; as for example, for the high Q bandpass filter in Figure 4.7.(b), $S_{\alpha_2}^Q$ is approximately 3.9. It may be higher as α_2 approaches $\omega_0 T$. It is also noted that unlike its continuous counterpart, the sensitivity of Q to α_2 is proportional to Q for the series switched capacitor configuration.

Apart from the sensitivity to the various coefficients mentioned earlier, the sensitivity of the center frequency, ω_0 , and the Q of the

filter to the clock frequency ($f_s = 1/T$, T being the sampling interval) must also be considered:

$$\text{i.e. } S_{f_s}^{\omega_0} = 1, \text{ (as expected)} \quad (3.38a)$$

$$\text{and } S_{f_s}^Q = Q \cdot \frac{(\omega_0 T)^2 - \alpha_2}{\omega_0 T}, \quad \alpha_2 \ll 1 \quad (3.33b)$$

Thus the sensitivity of Q to f_s is proportional to Q . Hence the achievable Q with the circuit will be dependant on the acceptable range of variation of the clock frequency. The factor becomes even greater for negative values of α_2 , required for achieving high Q filters. The sensitivity may, in that case, be increased by the factor $|1 - \alpha_2/(\omega_0 T)^2|$. This sets a practical limit to the achievable Q , using this configuration.

In order to validate the concepts presented in this section, the circuit of Figure 3.7. was breadboarded using 741 op amps and CMOS 4066 transmission gates. The capacitors used were polystyrene capacitors of 2% tolerance; fine trimming of the capacitances was done using trimmer capacitors for the smaller capacitors. As may be observed from the coefficients of the realized filter, the total spread of capacitors is quite large. In order to realize the smaller value of capacitors, considerable care was taken to minimize stray capacitances.

Fig. 3.9(a) Theoretical vs. experimental results for the high Q biquad resonator. The coefficients are shown in the inset.

The design values of the various coefficients shown in the inset of Figure 3.9.(a) were finally realized using trimmer capacitors. The experimental results are presented in Figures 3.9.(a) and 3.9.(b). Figure 3.9.(a) demonstrates the frequency response from 0 Hz to 2 kHz. The sampling frequency used was 32 kHz and the resonant frequency was approximately 500 Hz. The 3 dB bandwidth was measured as approximately 10 Hz, (i.e. $Q=50$), and the center frequency gain was approximately 5 (=14 dB). The transfer function near the pass band of the filter is shown in Figure 3.9.(b). Computer simulation was done for the circuit, using the coefficients shown in Figure 3.8.(b). The results agreed within ± 1 dB over the whole frequency range. The maximum deviation was noted near the resonant frequency. It will be shown in the next chapter that this difference may be attributed to the stray capacitance and diode leakages from the switched capacitors etc.

The experiment demonstrates the validity of the concept. It may be noted that the negative value of α_2 means positive feedback for the system. Essentially positive feedback raises the Q of the filter to the desired value. However, such feedback configuration always suffers from higher sensitivity, and this characteristic was also noticed in the experiment. It was observed that for the Q of the filter approaching 100, the circuit Q became extremely sensitive to small parameter variations and change of clock frequency. This means that the above design method is only suitable for realizing medium- Q filters. Furthermore, the resonant frequency should be small compared to the sampling frequency.

Fig. 3.9(b) Experimental response in the passband for the filter mentioned in Fig. 3.9(a). The scale is shown relative to the response at the resonant frequency, where the gain was found to be 1.5 dB lower than the expected value.

Some concluding remarks about the limitations of this design method seem necessary. First, this design method is based on a precise charge transfer cycle, viz. during one phase of the cycle, ALL summing and integrating nodes will interact to redistribute the charge throughout the circuit, whereas during the other phase, the switched capacitors will be initialized. Only with this operation will the backward difference transformation be valid in general for all passive and active RC circuits; this is explained in Appendix II.

The above design method is best applicable for a second-order system and for $\omega T \ll 1$. The simplicity of the method breaks down when the individual system considered is of order higher than two, or when the frequency region of interest becomes comparable to sampling frequency, i.e. ωT becomes comparable to one. It is well-known that from sensitivity considerations, second-order filter sections are cascaded to obtain higher order filters. The design method is adequate to handle this case. This justifies the presentation of the above-mentioned design method for synthesizing second-order switched capacitor filters with $\omega T \ll 1$.

3.4. SWITCHED CAPACITOR REALIZATION OF INFINITE GAIN MULTIPLE FEEDBACK (MFB) FILTER

The design method presented in the last section is not only applicable for realizing high Q filters, but is equally applicable for approximating any transfer function characteristic. In this section, a 0.1 dB fourth-order Chebychev lowpass filter will be synthesized by this design approach. The circuit used is the multiple

feedback (MFB) active RC filter [22]. The topology of the switched capacitor realization of the MFB circuit is shown in Figure 3.10. The circuit requires only two integrating capacitors, three switched capacitor elements and only one operational amplifier. Good stability characteristics and low output impedance [22] make it attractive for realization in switched capacitor circuits.

In Figure 3.10., replacing the switched capacitors by resistors, the continuous equivalent circuit may be obtained. The transfer function for this case may be obtained as:

$$H(s) = \frac{\alpha_1 \alpha_3 / BT^2}{s^2 + (\alpha_1 \alpha_2 + \alpha_3) s / T + \alpha_2 \alpha_3 / BT^2} \quad (3.39)$$

By using eqn. (3.4) for the series switched capacitor case in eqn. (3.39) the transfer function is obtained as:

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{\alpha_1 \alpha_3 / B}{(1-z^{-1})^2 + [\alpha_1 + \alpha_2 + \alpha_3] (1-z^{-1}) + \alpha_2 \alpha_3 / B} \quad (3.40)$$

The above equation may also be derived from the following difference equations: at node 1, when ϕ_1 is ON, the charge conservation principle is used. Thus at the n -th instant, at node 1,

$$\begin{aligned} &\alpha_1 C(v_{i,n} - v_{1,n}) + \alpha_2 C(v_{o,n} - v_{1,n}) \\ &+ \alpha_3 C(v_{2,n} - v_{1,n}) = C(v_{1,n} - v_{1,n-1}) \end{aligned} \quad (3.41)$$

Fig. 3.10 Infinite gain multiple feedback (MFB) series switched capacitor filter.

and at node 2,

$$\alpha_3 C v_{1,n} = -C_2 (v_{0,n} - v_{0,n-1}) \quad (3.42)$$

As an exercise this filter was designed with parameters suitable for prefiltering and reconstructing purposes at audio bandwidths.

The design specifications chosen are shown in Figure 3.11.(a). It is observed from Figure 3.11.(a), using the continuous equivalence (referred as case III hereafter), that the transfer function matches well over most of the frequency range, except near the cutoff frequency. Thus, the following exercise will employ first-order curve fitting at the cutoff frequency, or near it (as for example, the resonant frequency of each of the second-order MFB filter sections), thus achieving overall matching over the complete frequency range.

The design method proceeds as in the series switched capacitor resonator. Using eqn. (3.31) in (3.39), after lengthy but simple manipulation, eqn. (3.39) becomes,

$$H(e^{j\omega T}) \approx \frac{GA/T^2}{-\omega^2 + j\omega\{B(1-(\omega T)^2/6) + (\omega T)^2\}/T + A/T^2} \quad (3.43)$$

$$\text{where } A = \alpha_2 \alpha_3 / \beta \quad (3.44a)$$

$$B = \alpha_1 + \alpha_2 + \alpha_3 \quad (3.44b)$$

$$\text{and } G = \alpha_1 / \alpha_2 \quad (3.44c)$$

As the first case (denoted as Case I hereafter), the best fit near the cutoff frequency, ω_c , is desired.

Fig. 3.11(a) Frequency response of the infinite-gain MFB filter.

In such a case, eqn. (3.43) becomes,

$$H(e^{j\omega T}) \Big|_{\omega=\omega_c} = - \frac{GA/T^2}{-\omega^2 + j\omega\{B(1-(\omega_c T)^2/6) + (\omega_c T)^2\}/T + A/T^2} \quad (3.45)$$

From eqn. (3.39), the transfer function for the continuous case is written as follows:

$$H(j\omega) = - \frac{G'A'/T^2}{-\omega^2 + j\omega \cdot B' + A'/T^2} \quad (3.46)$$

where, $A' = \alpha_2' \alpha_3' / \beta$

$$B' = \alpha_1' + \alpha_2' + \alpha_3' \quad (3.47)$$

$$G' = \alpha_1' / \alpha_2'$$

α_1' , α_2' , α_3' and α_4' denote the continuous equivalence values derived by using eqn. (2.1) on resistance values.

Comparing eqns. (3.44) and (3.47), it is observed that only scaling the coefficients in the design equations is sufficient to meet the design requirements as follows:

$$1) \frac{\alpha_2 \alpha_3}{\beta^2} = \frac{\alpha_2' \alpha_3'}{\beta'^2} \quad (3.48)$$

$$2) \alpha_1 + \alpha_2 + \alpha_3 = \alpha_1' + \alpha_2' + \alpha_3' - (\omega_c T)^2 \quad (3.49)$$

$$3) \frac{\alpha_1}{\alpha_2} = \frac{\alpha_1'}{\alpha_2'} = \gamma_1 \quad (3.50)$$

If an additional constraint is added that

$$\frac{\alpha_3}{\alpha_2} = \frac{\alpha_3'}{\alpha_2'} = \gamma_2 \quad (3.51)$$

$$\text{then } \beta = \beta' (\alpha_2/\alpha_2')^2 \quad (3.52)$$

$$\text{and } \alpha_2 = \alpha_2' - (\omega_c T)^2 / (1 + \gamma_1 + \gamma_2) \quad (3.53)$$

The other parameters, viz, α_1 and α_3 follow from (3.50) and (3.51). It is observed that the coefficients α_1 , α_2 and α_3 are changed by the ratio α_2/α_2' , while β is changed by the factor $(\alpha_2/\alpha_2')^2$. From eqn. (3.53), we observe that this is due to the sampling action, to a first-order approximation.

To obtain the filter coefficients (in this case, the values of α_1 , α_2 , α_3 and β), the following procedure is followed:

1) From the filter specifications, and for the topology mentioned (in this case, MFB filter), the type of analog filter and its order are chosen. From conventional active RC filter equations, it has been derived that two stages of second-order 0.1 dB Chebychev MFB filters satisfy the required filter characteristics.

2) From any standard handbook on active RC filters, the values of the resistances and capacitances are chosen [23]. By using the continuous equivalence as given by eqn. (2.1), the values of the various switched capacitors are derived. In this case, α_1' , α_2' , α_3' and β are calculated.

3) The α'_n 's are used with equations (3.48) to (3.53) to obtain the desired coefficients, α 's. Note that the equations decouple in this case also.

Based on the above design procedure with cutoff frequency, f_c , as 4 KHz the filter parameters are derived for the frequency specification in Figure 3.11.(a) (inset):

Case I: Sampling frequency = 256 kHz

Stage 1

$$\alpha_1 = .0156$$

$$\alpha_2 = .0156$$

$$\alpha_3 = .0108$$

$$\beta = .0163$$

Stage 2

$$\alpha_1 = .0371$$

$$\alpha_2 = .0371$$

$$\alpha_3 = .0412$$

$$\beta = .2766$$

To evaluate the accuracy of the fit between desired and actual values, the passband of the filter is shown on an expanded scale in Figure 3.11.(b). It may be observed that the best fit occurs at the cutoff frequency. Although it was designed for 0.1 dB ripple in the passband, the maximum ripple was observed to be approximately 0.3 dB in the passband. The stopband attenuation agreed well with the

Fig. 3.11(b) Frequency response in the passband of the infinite-gain MFB filter

continuous case. It may be noted that at the passband edge deviation from ideal is less than .05 dB.

Alternatively, instead of matching at the cutoff frequency of the overall filter, it is possible to match the desired response at the resonant frequency of each section. Eqn. (3.3) then becomes,

$$|H(e^{j\omega T})| = - \frac{GA/T^2}{\omega^2 + j\omega\{B(1-(\omega_0 T)^2/6) + (\omega_0 T)^2\}/T + A/T^2} \quad (3.54)$$

where G , A and B are as defined in eqns. (3.44).

It may be noted that ω_0 equals $(\alpha_2'\alpha_3')^{1/2}/\beta'$. Using the above equation, the maximum ripple was improved to 0.2 dB. The stop-band attenuation did not change significantly. The coefficients in this case are as follows:

Case II: Sampling frequency = 256 kHz

Stage 1

$$\alpha_1 = .0145$$

$$\alpha_2 = .0145$$

$$\alpha_3 = .0100$$

$$\beta = .0113$$

Stage 2

$$\alpha_1 = .0383$$

$$\alpha_2 = .0383$$

$$\alpha_3 = .0425$$

$$\beta = .2720$$

This is also computed in Figure 3.11.(b). A better fit between the theory and design values over the entire passband is readily evident. The fit at the cutoff frequency is the best. However, the ripple height is increased to .2 dB. This indicates that a trade-off is

involved between realizing the cutoff frequency to its closest approximation, and realizing the maximum passband ripple. The fact that the maximum ripple in the passband is increased is not a serious disadvantage. By starting with a smaller passband ripple filter, any constraint on the maximum allowable ripple may be achieved.

It is interesting to compare these values with those available from the continuous equivalence; viz.

Case III: Sampling frequency = 256 kHz

Stage 1

$$\alpha_1' = .0192$$

$$\alpha_2' = .0192$$

$$\alpha_3' = .0133$$

$$\beta = .02$$

Stage 2

$$\alpha_1' = .0402$$

$$\alpha_2' = .0402$$

$$\alpha_3' = .0446$$

$$\beta = .3$$

Comparing the two sets of values, it is observed that the effect of the sampling action is to reduce the coefficient values. Alternatively, if the continuous equivalent values are retained, it is evident from eqns. (3.48), (3.49) and (3.50) that only the Q of the filter is affected. Hence for low-Q cases, it may be advantageous to choose the continuous equivalence values (the latter set) for economizing the chip area. So far as the lowpass filter is concerned, this only lowers the cutoff frequency. Hence to restore the cutoff frequency, it may be necessary to design the circuit assuming a slightly larger cutoff frequency, for meeting the requirements of the transfer characteristics.

It is possible to find the approximate sensitivity of the filter response from parameter variations. From eqn. (3.43), it is noted that

$$\omega_0 \approx \frac{\sqrt{A}}{T} \quad (3.55)$$

$$\text{bandwidth } \Delta\omega \approx \left\{ B \left(1 - \frac{(\omega_c T)^2}{6} \right) + (\omega_c T)^2 \right\} / T \quad (3.56a)$$

$$\text{and } Q = \frac{\omega_0}{\Delta\omega} \quad (3.56b)$$

where A and B are as defined in eqns. (3.44).

It may be pointed out that the design method was derived for high Q filters. For low Q filters, as in this case, replacing ωT in eqn. (3.43) near the resonant frequency ω_c by $\omega_c T$ is incorrect. However to assess the sensitivity of the circuit from simpler formula, the replacement has been done, i.e. eqn. (3.56) is only qualitatively correct, and can only give a rough idea of the true sensitivity. Based on the above equations, the following derivations are obtained:

$$S_{\alpha_1}^{\omega_0} = 0 \quad (3.57a)$$

$$S_{\alpha_2}^{\omega_0} = S_{\alpha_3}^{\omega_0} = \frac{1}{2} \quad (3.57b)$$

$$S_C^{\omega_0} = S_B^{\omega_0} = \frac{1}{2} \quad (3.57c)$$

i.e. the sensitivity of the resonant frequency (approximately 3 dB cutoff frequency) is almost equal to that of its active RC counterpart.

Using the approximate eqns. (3.56) for bandwidth, the following derivations are obtained:

$$S_{\alpha_1}^{\Delta\omega} = \alpha_1 \cdot \frac{1 - \frac{A}{B}}{B \left\{ 1 - \frac{A}{B} \right\} + A}$$

$$\approx \frac{\alpha_1}{\alpha_1 + \alpha_2 + \alpha_3 + \alpha_2 \alpha_3 / B}, \text{ if } A \ll 1 \quad (3.58)$$

$$S_{\alpha_2}^{\Delta\omega} = \frac{\alpha_2 \left\{ 1 - \frac{A}{B} \right\} + A \left\{ 1 - \frac{B}{A} \right\}}{B \left\{ 1 - \frac{A}{B} \right\} + A}$$

$$\approx \frac{\alpha_2}{\alpha_1 + \alpha_2 + \alpha_3 + \alpha_2 \alpha_3 / B}, \text{ if } A \ll 1 \quad (3.59)$$

Similarly,

$$S_{\alpha_3}^{\Delta\omega} = \frac{\alpha_3}{\alpha_1 + \alpha_2 + \alpha_3 + \alpha_2 \alpha_3 / B}, \text{ if } A \ll 1 \quad (3.60)$$

and also,

$$S_C^{\Delta\omega} = \frac{A(1 - \frac{B}{A}) + B(1 - \frac{A}{B})}{A + B(1 - \frac{A}{B})} \approx 1 \text{ if } A, B \ll 1 \quad (3.61)$$

and

$$S_B^{\Delta\omega} = \frac{A(1 - \frac{B}{6})}{A(1 - \frac{B}{6}) + B} = \frac{A}{A + B} \quad \text{if } A, B \ll 1 \quad (3.62)$$

where A and B are as defined in eqns. (3.44).

It is observed that the sensitivity of the bandwidth to parameter variations is less than 1, which is quite satisfactory.

The infinite gain multiple feedback series switched capacitor filter was simulated on a breadboard using the coefficients derived in this section (Case III). The output from the first stage and the cascaded two stages are shown in Figure 3.12.(a). The 6 dB/octave roll-off of the first stage and the 12 dB/octave roll-off of the overall filter are evident from the figure. The passband gain is 0 dB and the peak passband ripple was approximately 0.2 dB. The 3 dB cutoff frequency found to be approximately 4.5 kHz. The maximum harmonic distortion in the passband was measured as -48 dB at approximately 2400 Hz for an input voltage of 1.5 V peak-to-peak. The reason for this is evident, looking at the output of the first stage. The first stage has a gain of approximately 2. Hence the output of the first stage is approximately 3 volts peak-to-peak. The major contribution of the harmonic distortion is therefore from the first stage. Finally, it may also be observed that because of the low output impedance and the high input impedance of each stage, no loading problems arise. Hence the design becomes more straightforward.

Fig. 3.12(a) Experimental results of the frequency response of the MFB filter.

Fig. 3.12(b) Experimental response in the passband for cases II and III (continuous equivalence). Comparison with the desired response, shown by solid lines, illustrate the fact that case II gives a better fit with the experiment

The passband characteristics for Cases II and III were also experimentally checked. The results of this experiment are shown in Figure 3.12.(b). The discrepancy between the theory and experiment arose due to the combined effect of coefficient inaccuracy, parasitic capacitance and diode leakage from the switched capacitors etc. For Cases I and II, slight overshoot near the cutoff frequency is observed. This is due to inaccuracy in realizing the coefficients. Because of the fact that a higher resolution may be obtained in realizing capacitors in an integrated chip, this problem would not arise there. Again the fact that the gain near the cutoff frequency is higher for Cases I and II means that the dynamic range of the filter has to be reduced if the same amount of harmonic distortion is to be tolerated. Experimentally, it was observed that the reduction in the dynamic range is approximately 6 dB for the maximum harmonic distortion of -48 dB.

The measurements on harmonic distortion and noise spectral density will be presented in the next chapter.

3.5. NOTCH FILTER (60 Hz REJECTION)

Finally, the series switched capacitor will be employed to obtain a transmission zero. Although the design approach is the same as in the previous cases, it was deemed unnecessary to obtain correction terms due to the sampling action because the circuit of interest realizes a transmission zero at a frequency very low compared to the sampling frequency.

The purpose of this exercise is also to explore the possibility of an all-passive switched capacitor network in achieving the notch filter, and to demonstrate the feasibility of an integrated notch filter. The twin-T network [24] is used to produce the necessary zero on the frequency axis. The series switched capacitor version of the twin-T network is shown in Fig. 3.13. Once again, this mode is chosen over the parallel mode from stability considerations.

For the continuous equivalent case, the transfer function for a symmetrical twin-T network may be written as

$$H(s) = \frac{1 + (sCR)^2}{1 + 4(1-K)sCR + (sCR)^2} \quad (3.63)$$

For a symmetrical network, following the results of the active RC twin-T circuit, the following constraints were chosen:

$$C_1 = C_2 = C_3/2 = C \quad (3.64a)$$

$$C_{R1} = C_{R2} = C_{R3}/2 = C_R \quad (3.64b)$$

Fig. 3.13 Switched capacitor (series) realization of twin-tee notch filter.

Thus the design eqns. are now limited to finding the appropriate ratio of C_R/C . Using eqns. (3.4) in (3.63), the transfer function of the sampled data filter was derived:

$$\begin{aligned}
 H(z) &= \frac{1 + \left[\frac{C}{C_R} (1-z^{-1}) \right]^2}{1 + 4(1-K) \frac{C}{C_R} (1-z^{-1}) + \left(\frac{C}{C_R} \right)^2 (1-z^{-1})^2} \\
 &= \frac{\left(\frac{C_R}{C} \right)^2 + (1-z^{-1})^2}{\left(\frac{C_R}{C} \right)^2 + 4(1-K) \frac{C_R}{C} (1-z^{-1}) + (1-z^{-1})^2}
 \end{aligned} \tag{3.65}$$

It is also possible to derive the same results from the set of difference equations. The z-transform analysis of the network follows from the following difference equations:

at node 1,

$$\begin{aligned}
 C_{R1} (v_{i,n} - v_{1,n}) + C_{R2} (v_{0,n} - v_{1,n}) \\
 = C_3 [v_{1,n} - v_{1,n-1} - K(v_{0,n} - v_{0,n-1})]
 \end{aligned} \tag{3.66}$$

at node 2,

$$C_{R_3} (v_{2,n} - K v_{0,n}) = C_1 [(v_{1,n} - v_{1,n-1}) - (v_{2,n} - v_{2,n-1})] \\ + C_2 [(v_{0,n} - v_{0,n-1}) - (v_{2,n} - v_{2,n-1})] \quad (3.67)$$

at node 3,

$$C_{R_2} (v_{1,n} - v_{0,n}) = C_2 [(v_{0,n} - v_{0,n-1}) - (v_{2,n} - v_{2,n-1})] \quad (3.68)$$

Taking the z-transform of the above equations,

$$V_1(z) = \frac{C_{R_1} V_i(z) + C_{R_2} V_0(z) + C_3 K (1-z^{-1}) V_0(z)}{C_{R_1} + C_{R_2} + C_3 (1-z^{-1})} \quad (3.69)$$

$$V_2(z) = \frac{[C_1 V_i(z) + C_2 V_0(z)] (1-z^{-1}) + K C_{R_3} V_0(z)}{(C_1 + C_2) (1-z^{-1}) + C_{R_3}} \quad (3.70)$$

and

$$V_0(z) = \frac{C_{R2} V_1(z) + C_2(1-z^{-1})V_2(z)}{C_{R2} + C_2(1-z^{-1})} \quad (3.71)$$

By combining these three equations and using the constraints of symmetrical twin-T network, eqn. (3.65) may be verified. The procedure is however much more complicated than the identification $s \leftrightarrow (1-z^{-1})/T$ in $H(s)$ that we have demonstrated.

Null frequency, ω_0 , is obtained by equating the numerator of eqn. (3.65) to zero, after replacing $z = e^{j\omega T}$.

$$\text{i.e.} \quad \left(\frac{C_R}{C}\right)^2 + (1 - e^{-j\omega_0 T})^2 = 0 \quad (3.72)$$

which gives

$$\omega_0 = \frac{1}{T} \log_e \left(1 \mp j \frac{C_R}{C}\right) \quad (3.73)$$

Again the logarithmic term may be expanded binomially and if $C_R/C \ll 1$, it can also be simplified

$$f_0 = j \frac{1}{2\pi T} \log_e \left(1 \mp j \frac{C_R}{C}\right) \quad (3.74)$$

$$= j \frac{1}{2\pi T} \left[\mp j \frac{C_R}{C} \pm \frac{1}{2} \left(j \frac{C_R}{C}\right)^2 \mp \frac{1}{3} \left(j \frac{C_R}{C}\right)^3 \dots \right]$$

$$= \mp \frac{1}{2\pi T} \frac{C_R}{C} \text{ if } \frac{C_R}{C} \ll 1 \quad (3.75)$$

This equation suggests that for $C_R \ll C$, (i.e. the sampling frequency is much higher than the null frequency), the continuous active equivalence is valid. This agrees with the property 1 of the backward difference formulation, which the series switched capacitor obeys.

To determine the sensitivity of the null frequency to the ratio C_R/C , let

$$\frac{C_R}{C} = X \quad (3.76)$$

Using eqn. (3.76), eqn. (3.73) is reformulated as

$$f_0 = \frac{jf_s}{2\pi} \log_e (1-jX) \quad (3.77)$$

where

f_0 = notch frequency in hertz

f_s = sampling frequency in reps./sec. (= $1/T$, T being the sampling interval in seconds).

Differentiating eqn. (3.77) with respect to X gives,

$$\frac{\partial \omega_0}{\partial X} = \frac{f_s}{1-jX} \quad (3.78)$$

Defining the sensitivity of the null frequency, ω_0 , to the parameter X as

$$S_X^{\omega_0} = \frac{\partial \omega_0}{\partial X} \cdot \frac{X}{\omega_0} \quad (3.79)$$

From eqns. (3.77), (3.78) and (3.79), the required sensitivity is obtained as:

$$S_X^{\omega_0} = \frac{-jX}{1-jX} \cdot \frac{1}{\log_e (1-jX)} \quad (3.80)$$

Once again using the binomial expansion, and if $X \ll 1$,

$$S_X^{\omega_0} = \frac{1}{1-jX} \approx 1 \quad (3.81)$$

i.e. the sensitivity is low if $C_R/C \ll 1$. This means that for uniform variation of switched capacitors compared to integrating capacitors, the sensitivity of the null frequency is low if the ratio C_R/C is small.

The sensitivity of the null frequency ω_0 to the various individual capacitors C_{R1} , C_{R2} , C_{R3} , C_1 , C_2 , C_3 have also been derived. The analysis is simple but lengthy. Hence, only the results are presented here.

Let

$$C_{R1} = k_1 C_R \quad C_{R2} = k_2 C_R \quad C_{R3} = k_3 (2C_R)$$

(3.82)

$$C_1 = \ell_1 C \quad C_2 = \ell_2 C \quad C_3 = \ell_3 (2C)$$

Thus $k_1, k_2, k_3, \ell_1, \ell_2$ and ℓ_3 are measures of deviation of the capacitances from their design values. For this case, the equation for null frequency becomes

$$\omega_0 = j f_s \log_e \left[1 + j \sqrt{\frac{B k_1 k_2}{A \ell_1 \ell_2}} \cdot \frac{C_R}{C} \right] \quad (3.83)$$

where

$$A = (k_1 + k_2) C_R + \ell_3 (2C) (1 - e^{-j\omega_0 T}) \quad (3.84)$$

$$B = (\ell_1 + \ell_2) C (1 - e^{-j\omega_0 T}) + k_3 (2C_R) \quad (3.85)$$

This equation is transcendental in nature, and may be solved numerically. However, noting that $\omega_0 T \ll 1$, for $C_R/C \ll 1$, eqns. (3.84) and (3.85) may be simplified as

$$A = (k_1 + k_2) C_R + \ell_3 (2C) \omega_0 T \quad (3.86)$$

$$B = (\ell_1 + \ell_2) C (\omega_0 T) + k_3 (2C_R) \quad (3.87)$$

Based on this approximation, the sensitivity of the null frequency ω_0 to k_1 , k_2 , k_3 , l_1 , l_2 and l_3 are derived:

$$S_{k_1}^{\omega_0} = -\frac{1}{2} \frac{\sqrt{\frac{k_1 k_2}{l_1 l_2}} \frac{C_R}{C}}{1 - j \sqrt{\frac{k_1 k_2}{l_1 l_2}} \frac{C_R}{C}} \log_e \left[\frac{1}{1 - j \sqrt{\frac{k_1 k_2}{l_1 l_2}} \frac{C_R}{C}} \right] \quad (3.88)$$

$$S_{k_2}^{\omega_0} = S_{k_1}^{\omega_0} \quad (3.89)$$

$$S_{l_1}^{\omega_0} = \frac{1}{2} \frac{\sqrt{\frac{k_1 k_2}{l_1 l_2}} \frac{C_R}{C}}{1 - j \sqrt{\frac{k_1 k_2}{l_1 l_2}} \frac{C_R}{C}} \log_e \left[\frac{1}{1 - j \sqrt{\frac{k_1 k_2}{l_1 l_2}} \frac{C_R}{C}} \right] \quad (3.90)$$

$$S_{l_2}^{\omega_0} = S_{l_1}^{\omega_0} \quad (3.91)$$

$$S_{k_3}^{\omega_0} = 0, \text{ to a first-order approximation} \quad (3.92)$$

and

$$S_{l_3}^{\omega_0} = 0, \text{ to a first-order approximation} \quad (3.93)$$

The values of the sensitivities in eqns. (3.88) through (3.93) are approximately 1/2 for $C_R/C \ll 1$, k_1 , k_2 , k_3 , ℓ_1 , ℓ_2 , $\ell_3 \rightarrow 1$. Thus, once again it is demonstrated that if the frequency region of interest is much smaller than the sampling frequency, the switched capacitor circuit behaves identical to its continuous analog.

It is noted that there are "floating" nodes in the circuit. Stray capacitances from the nodes 1, 2 and 3 in Fig. 3.12 will affect the circuit performance thus:

Let C_{s1} , C_{s2} and C_{s3} be the stray capacitances from the nodes 1, 2 and 3 respectively. Under this circumstance, the transfer function of the circuit becomes

$$H(z) = \frac{\beta' k_1 k_2 C_R^2 + \alpha' \ell_1 \ell_2 C^2 (1-z^{-1})^2}{\alpha' \beta' \gamma' - \beta' k_2^2 C_R^2 - \beta' K k_2 \ell_3 C C_R (1-z^{-1}) - \alpha' \ell_2^2 C^2 (1-z^{-1})^2 - \alpha' K k_3 \ell_2 C C_R (1-z^{-1})} \quad (3.94)$$

where

$$\begin{aligned} \alpha' &= (k_1 + k_2) C_R + \ell_3' (2C) \\ \ell_3' &= \ell_3 + C_{s1}/2C \\ \beta' &= (\ell_1' + \ell_2) C (1-z^{-1}) + k_3 (2C_R) \end{aligned} \quad (3.95)$$

$$\ell_1' = \ell_1 + C_{s2}/C$$

$$\gamma' = k_2 C_R + \ell_2' C(1-z^{-1})$$

$$\ell_2' = \ell_2 + C_{s3}/C$$

$k_1, k_2, k_3, \ell_1, \ell_2$ and ℓ_3 being defined in eqn. (3.82).

Thus in this case, the null frequency, ω_0 , of the circuit is given by

$$\omega_0 = jf_s \log_e \left[1 \mp j \sqrt{\frac{\beta' k_1 k_2}{\alpha' \ell_1 \ell_2}} \frac{C_R}{C} \right] \quad (3.96)$$

As C_{s1} and C_{s2} effect α' and β' , eqn. (3.96) indicates that it also effects the null frequency ω_0 . From eqn. (3.95), it is noted that if C_{s1} and C_{s2} are much smaller than C , their effect is negligible. This is one reason to make C as large as possible as the chip area would permit. C_{s3} influences γ' which appears in the denominator of eqn. (3.94). Thus it effects the quality of the null frequency only.

Based on the above analysis, the proposed design of the notch filter incorporates the following features:

(1) $C_R/C \ll 1$, from sensitivity considerations. This is compatible with the choice of the sampling frequency high compared

to the null frequency, i.e. let $f_s = 32$ KHz, $f_{\text{null}} = 60$ Hz, yielding $C_R/C = 1.178 \times 10^{-2}$.

(2) The series mode for the switched capacitors has been chosen from stability considerations. As $\omega_{\text{null}}T = .0118 \ll 1$, the effect of sampling need not be considered.

(3) Complementary clocks may be used to drive the switches.

Computer simulation of the notch filter for various values of K is shown in Fig. 3.14.

The circuit of Fig. 3.13 was implemented on a breadboard. As in the high-Q bandpass cases, the range of capacitances is large. Hence once again the stray capacitances introduce problems for realizing the smaller capacitors. Furthermore, the null frequency is derived by a balanced twin-T network. Hence the capacitors were chosen to be accurate within $\pm 0.5\%$ of the design values. By proper placement of the capacitors, the stray capacitances were minimized as far as possible. It may also be noted that the node 3 of Fig. 3.13 is a high impedance point. For the circuit concerned, the input impedance of 741 op amp (≈ 10 k Ω) was found too low and hence unsatisfactory for use in this particular circuit. Instead an FET-input op amp was used, with an input impedance of 10^{12} ohms. The low input current of the op amp prevents loading of the circuit.

The results for three different values of feedback are demonstrated in the Fig. 3.14. The null frequency is approximately

Fig. 3.14(a) Theoretical vs. experimental response of the twin-tee notch filter for various values of the feedback factor

Fig. 3.14(b) Experimental response of a twin-tee notch filter for various values of the feedback factor (or gain).

60 Hz. Unlike its continuous counterpart, it is observed that the notch depth is finite. This is because of the fact that the zero of the filter does not occur on a real frequency but has a finite imaginary value (i.e. $z_p = \sigma_p \pm j\omega_p$, $\sigma_p \neq 0$). By raising the sampling frequency, and equivalently lowering the coefficients, it is possible to increase the notch depth. However, this means even larger spread of capacitor values. The circuit becomes practically unrealizable. Hence the sampling frequency was retained at 32 kHz. As predicted by the theory, it is observed that for larger values of feedback, the Q of the notch may be increased, with a consequent decrease in the notch depth. As the feedback involved is positive, feedback larger than 0.99 makes the filter susceptible to oscillation. Hence, in practical cases, it is recommended that feedback larger than 0.9 may not be used. For zero feedback the notch depth is approximately 45 dB and it decreases to approximately 40 dB for a positive feedback value of 0.9.

3.6 Design Considerations for Parallel Switched Capacitor Mode

In section 3.3, a design method was presented for the series switched capacitor mode. The design method was demonstrated in the case of the series switched capacitor biquad high Q band-pass filter and later extended in the case of the MFB filter and notch filter. The design method is also applicable for the parallel switched capacitor mode except the range of circuit

applicability is not so wide. The transformation that is to be used is the forward difference equation (3.12). As in section 3.3, it is possible to derive the simplification of the eqn. (3.12) as follows:

$$\begin{aligned}
 z - 1 &= e^{j\omega T} - 1 \\
 &= j\omega T \left[1 - \frac{(\omega T)^2}{3!} + \dots + j \left\{ \frac{\omega T}{2!} - \frac{(\omega T)^3}{4!} + \dots \right\} \right] \\
 &\approx j\omega T \left[1 - \frac{(\omega T)^2}{3!} + j \frac{\omega T}{2!} \right], \quad \omega T \ll 1
 \end{aligned} \tag{3.97}$$

Like eqn. (3.29), the above equation also denotes the perturbation on real frequency by the quantity in parenthesis, which occurs due to the sampling action.

Based on eqn. (3.97), the earlier stated design method will be demonstrated in the case of a parallel switched capacitor bandpass filter. From the continuous equivalent expression and eqn. (3.10), the transfer function for the circuit of Fig. 3.15 may be written as

$$H(z) = - \frac{\alpha_1 (z-1)}{(z-1)^2 + \alpha_2 (z-1) + \alpha_3 \alpha_4} \tag{3.98}$$

Using eqn. (3.97) and after some reorganization, eqn. (3.98) becomes

Fig. 3.15 A switched capacitor (parallel) biquad resonator.

$$H(e^{j\omega T}) = - \frac{j\omega T \alpha_1 [1 - (\omega T)^2/6 + j\omega T/2]}{-(\omega T)^2 [1 + \alpha_2/2] + j\omega T [\alpha_2 (1 - (\omega T)^2/6) - (\omega T)^2] + \alpha_3 \alpha_4} \quad (3.99)$$

Recognizing the fact that it is desired to obtain the best fit at or near the resonant frequency, eqn. (3.99) is rewritten as

$$H(e^{j\omega T})|_{\omega=\omega_0} = - \frac{j\omega(\alpha_1/T) [1 - (\omega_0 T)^2/6 + j(\omega_0 T)/2] / (1 + \alpha_2/2)}{-\omega^2 + j\omega(\alpha_2/T) [1 - (\omega_0 T)^2 (1/6 + 1/\alpha_2)] / (1 + \alpha_2/2) + (\alpha_3 \alpha_4 / T^2) / (1 + \alpha_2/2)} \quad (3.100)$$

Once again, comparing the parallel switched capacitor case with its continuous equivalence, the following derivations may be made

	<u>Switched Capacitor Case</u>	<u>Continuous Equivalence</u>
Resonant frequency in radians, ω_0	$\frac{\sqrt{\alpha_3 \alpha_4}}{T} \cdot \frac{1}{\sqrt{1 + \alpha_2/2}}$	$\frac{\sqrt{\alpha_3 \alpha_4}}{T}$
Bandwidth in radians, $\Delta\omega$	$\frac{\alpha_2}{T} \cdot \frac{1 - (\omega_0 T)^2 (1/6 + 1/\alpha_2)}{1 + \alpha_2/2}$	$\frac{\alpha_2}{T}$
Q	$\frac{\sqrt{\alpha_3 \alpha_4}}{\alpha_2} \cdot \frac{\sqrt{1 + \alpha_2/2}}{1 - (\omega_0 T)^2 (1/6 + 1/\alpha_2)}$	$\frac{\sqrt{\alpha_3 \alpha_4}}{\alpha_2}$

	<u>Switched Capacitor Case</u>	<u>Continuous Equivalence</u>
Gain at resonant frequency, $G(\omega_0)$	$\frac{\alpha_1}{\alpha_2} \cdot \frac{1 - (\omega_0 T)^2/24}{1 - (\omega_0 T)^2(1/6 + 1/\alpha_2)}$	$\frac{\alpha_1}{\alpha_2}$

The effect of sampling on the parallel switched capacitor filter can be observed by comparing the two sets of equations. It is observed that the results are similar to those of the series switched capacitor case except for the sign of α_2 . Thus the sensitivity analysis of the series switched capacitor filter of Section 3.3 is still valid after changing the sign of α_2 . The implications of the sensitivity analysis are also equally valid. Based on the design equations, computer simulations were done for a high Q bandpass filter; the results of which are presented in Fig. 3.16. The validity of the approximations are clearly evident from the example.

Finally, the limitations of the design method have to be specified. The correspondence between the sampled-data analysis and its continuous equivalence is only valid for the case where all summing and integrating nodes interact during one phase of the clock and initialize during the other phase from voltage sources. Thus if the parallel switched capacitor is used to charge share between two floating nodes, the above condition is

Fig. 3.16 Theoretical response of the parallel switched capacitor circuit shown in Fig. 3.15.

not satisfied. For such cases, the difference equation has to be formulated from the topology and the forward difference equation cannot be used to obtain the transfer function in the z-domain. Whereas for the series case, the condition may be satisfied in general circuits, the parallel switched capacitor satisfies the condition only for the case where at least one end is voltage-driven for each switched capacitor element as in the biquad. As for example, for the notch filter, these conditions are not satisfied. Hence the transformations cannot be applied. The above statements have been validated by an example cited in Appendix II.

3.7 Design Approach for the Bilinear Transformation Case

In the previous sections, it was demonstrated that for frequency selective circuits e.g. bandpass and bandstop filters, the series or parallel switched capacitor, using mapping of differentials, circuits are not very efficient. What is required is the conformal mapping of the s-plane to the z-plane. The bilinear transformation, illustrated in section 3.2, achieves this. A method to realize the bilinear transformation analog to an active RC-integrator was also demonstrated in section 3.2. The design of state-variable type switched capacitor filters using such transformation, therefore, follow naturally.

The design method will now be presented. The state variable type of filter has already been introduced in sections

Fig. 3.17(a)

Fig. 3.17(b)

Fig. 3.17(a) Block diagram of a state-variable type second-order system.

Fig. 3.17(b) Bilinear transform realization of the system described in Fig. 3.17(a).

2.10 and 3.3. That was the so-called Biquad circuit. The continuous Biquad circuit is illustrated by using state-variable blocks in Fig. 3.17(a). By replacing each block by an integrator using bilinear transformation, the switched capacitor circuit realization is obtained, as shown in Fig. 3.17(b). The unity gain inverting amplifier can be realized using the series switched capacitor circuits. For simplicity, it is only referred to by the block, -1 . From continuous equivalence equations, the transfer functions at the bandpass and lowpass output are obtained as

$$H_B(s) = - \frac{\alpha_1 s}{s^2 + \alpha_2 s + \alpha_3 \alpha_4} \quad (3.101)$$

and

$$H_L(s) = \frac{\alpha_1 \alpha_4}{s^2 + \alpha_2 s + \alpha_3 \alpha_4} \quad (3.102)$$

By replacing s by the transform in eqn. (3.24), the transfer function for the bandpass function is obtained as

$$H_B(z) = - \frac{\alpha_1 \left(\frac{1 - z^{-1}}{1 + z^{-1}} \right)}{\left(\frac{1 - z^{-1}}{1 + z^{-1}} \right)^2 + \alpha_2 \left(\frac{1 - z^{-1}}{1 + z^{-1}} \right) + \alpha_3 \alpha_4} \quad (3.103)$$

and that of the second order lowpass filter is

$$H_L(z) = \frac{\alpha_1 \alpha_4}{\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right)^2 + \alpha_2 \left(\frac{1 - z^{-1}}{1 + z^{-1}}\right) + \alpha_3 \alpha_4} \quad (3.104)$$

It is possible to obtain the above relations from the difference equations. The results may be verified by writing the difference equations.

Closed form solutions for the center frequency, f_0 , in Hz and the quality Q , of the resonant circuit are respectively given by [42]:

$$f_0 = \frac{1}{2\pi T} \cos^{-1} \left[\frac{1 - \alpha_3 \alpha_4}{[(1 + \alpha_3 \alpha_4)^2 - \alpha_2^2]^{1/2}} \right] \quad (3.105)$$

and

$$Q = \frac{\cos^{-1} \left[\frac{1 - \alpha_3 \alpha_4}{[(1 + \alpha_3 \alpha_4)^2 - \alpha_2^2]^{1/2}} \right]}{\log_e \left[\frac{1 - \alpha_2 + \alpha_3 \alpha_4}{1 + \alpha_2 + \alpha_3 \alpha_4} \right]} \quad (3.106)$$

Although the above design equations are cumbersome, the design procedure is much simpler:

let f_o and Q be given;

then the lower and upper cutoff frequencies, f_L and f_H are obtained as follows:

$$f_H, f_L = [f_o^2 + (f_o/2Q)^2]^{1/2} \pm f_o/2Q \quad (3.107)$$

Note that frequency warping modifies these expressions from the continuous equivalent. The corresponding frequencies, in the continuous domain are given by

$$\Omega_o T = 2 \tan(2\pi f_o T/2) \quad (3.108a)$$

$$\Omega_H T = 2 \tan(2\pi f_H T/2) \quad (3.108b)$$

$$\Omega_L T = 2 \tan(2\pi f_L T/2) \quad (3.108c)$$

and

$$\Delta\Omega = \Omega_H - \Omega_L \quad (3.109)$$

where Ω_o , Ω_H and Ω_L are the continuous domain equivalent frequencies to f_o , f_H and f_L respectively and $\Delta\Omega$ is the corresponding bandwidth.

The continuous-domain first-order bandpass filter equation is given by

$$H(s) = \frac{G(\Delta\Omega)s}{s^2 + (\Delta\Omega)s + \Omega_0^2} \quad (3.110)$$

By using eqn. (3.24), the corresponding bilinear transformation equation is obtained:

$$H(z) = \frac{G(\Delta\Omega) \frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}}}{\left(\frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}}\right)^2 + (\Delta\Omega) \left(\frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}}\right) + \Omega_0^2} \quad (3.111)$$

The structure of the bandpass circuit proposed is essentially the same as in Fig. 3.17(b), with the output being taken at v_B . The response is, therefore, given by eqn. (3.103). Comparing eqns. (3.103) and (3.111), the following relations are obtained:

$$\alpha_3 = \alpha_4 = \frac{\Omega_0 T}{2} \quad (3.112a)$$

$$\alpha_2 = (\Delta\Omega) \frac{T}{2} \quad (3.112b)$$

$$\alpha_1 = G \frac{(\Delta\Omega)T}{2} \quad (3.112c)$$

From eqns. (3.112), it is observed that the center frequency ω_0 , (its frequency warped value being Ω_0) is dependent

SAMPLING FREQ = 32KHZ $\alpha_1 = 3.01E-2$
 RESONANT FREQ = 1500HZ $\alpha_2 = 3.01E-2$
 Q = 50 $\alpha_3 = .1483$
 GAIN = 1 $\alpha_4 = .1483$

Fig. 3.18 Frequency response of the bilinear transformation switched capacitor circuit of Fig. 3.17(b).
 The upper curve stands for the bandpass output, v_B , and the lower curve for the lowpass
 output, v_L . Experimental results are shown for the bandpass output.

only on α_3 and α_4 . Similarly, the bandwidth $\Delta\Omega$ and the gain G of the filter may be individually controlled by varying the parameters α_2 and α_1 respectively. This means that the three characteristics of the bandpass filter may be non-interactively controlled, showing the feasibility of building a programmable bandpass filter using switched capacitor networks.

The bilinear transform switched capacitor version of the biquad filter was simulated in the laboratory. The circuit diagram of the filter is shown in Fig. 3.17(b). The coefficients for a medium Q ($Q \approx 50$) bandpass filter are shown in Figure 3.18. Once again, the spread of capacitance values is large. Hence, care has to be taken to realize the small capacitors. The problem becomes even more complicated by the fact that the "series" and "parallel" switched capacitors of each bilinear element should be identical (to within $\pm 1\%$). This necessitates greater care of the circuit layout. By taking proper precautions in the layout, the circuit was built. The realized transfer function is shown in Fig. 3.18.

The sampling frequency used was 32 kHz. The resonant frequency of the filter was approximately 1475 Hz and the realized Q was approximately 40. The frequency response at the output of both the bandpass and lowpass circuit are shown in Fig. 3.18. As the horizontal scale is linear rather than logarithmic, the 6 dB/octave and 12 dB/octave roll of the two

transfer functions are not clearly evident from the figure. Measurements by wave analyzer (HP 3490A) validate the point.

The maximum harmonic distortion of the filter was approximately 55 dB throughout the passband. This is for a peak-to-peak output signal of 3 volts. The low harmonic distortion may be attributed to the fact that all the switched capacitor elements are terminated by voltage sources at both ends. The effect of the diode leakage from the switched capacitor elements for voltage constrained nodes are lower than those for floating output points. A quantitative description of the above statement will be presented in the next chapter.

3.8 Design of Sharp Cutoff Lowpass Biquad Switched Capacitor Using Bilinear Transformations

It was demonstrated in section 3.7 that lowpass filters may be realized by switched capacitor networks using the bilinear transformation. A systematic approach for using such networks to realize specific filter functions will now be demonstrated. Once again, efforts will be made to relate the filter coefficients to the component values in the analog equivalent circuit. To illustrate this, note that the continuous second-order lowpass filter equation is:

$$H(s) = \frac{Gb_0}{s^2 + b_1s + b_0} \quad (3.113)$$

where b_0 , b_1 and G are the filter coefficients.

By using eqn. (3.24), the corresponding lowpass filter in bilinear transformation form is obtained:

$$H(z) = \frac{Gb_0}{\left(\frac{2}{T} \frac{1-z^{-1}}{1+z^{-1}}\right)^2 + b_1 \frac{2}{T} \frac{1-z^{-1}}{1+z^{-1}} + b_0} \quad (3.114)$$

Re-organizing (3.114) and denormalizing the frequency

$$H(z) = \frac{Gb_0 \frac{T^2}{2} \Omega_c^2}{\left(\frac{1-z^{-1}}{1+z^{-1}}\right)^2 + b_1 \frac{T}{2} \frac{1-z^{-1}}{1+z^{-1}} \Omega_c + b_0 \left(\frac{T}{2}\right)^2 \Omega_c^2} \quad (3.115)$$

where Ω_c is the equivalent frequency of the passband edge, ω_c .

Comparing eqns. (3.103) and (3.115), the following relations are obtained:

$$\alpha_2 = b_1 \frac{\Omega_c T}{2} = b_1 \tan\left(\frac{\omega_c T}{2}\right) \quad (3.116a)$$

$$\alpha_3 = \alpha_4 = \sqrt{b_0} \frac{\Omega_c T}{2} = \sqrt{b_0} \tan\left(\frac{\omega_c T}{2}\right) \quad (3.116b)$$

$$\alpha_1 = G\alpha_3 \quad (3.116c)$$

Once the type and order of the filter are established, it is possible to obtain the parameters b_0 , b_1 and G from standard handbooks on active RC filters [26]. However, the cutoff frequency Ω_c in the s -plane is different from ω_c in the z -plane because of "frequency warping" during bilinear transformation, as discussed in section 3.2. This will be explained in the example.

The filter characteristics for the sharp-cutoff lowpass filter is shown in Fig. 3.19. From the figure, the following data are obtained:

$$f_p = 2400 \text{ Hz} \quad (3.117a)$$

$$f_q = 4800 \text{ Hz} \quad (3.117b)$$

where f_p and f_q denote the highest frequency in the passband and the lowest frequency in the attenuation band in hertz respectively. From Fig. 3.19, the specifications on the sampled-data filter are seen to be as follows:

$$20 \log_{10} |H(j2\pi f_p)| \geq -0.5 \quad (3.118a)$$

and

$$20 \log_{10} |H(j2\pi f_q)| \leq -22 \quad (3.118b)$$

Signal frequency in Hz: Passband Region

Signal frequency in Hz: Stopband Region

3.19 Required frequency characteristics of the sharp cutoff lowpass filter.

The corresponding frequencies in the equivalent analog domain are obtained by using eqn. (3.27) in (3.118). Thus, eqn. (3.118) becomes

$$20 \log_{10} |H(j2 \tan \frac{2\pi f_p/f_s}{2} s)| \geq -0.5 \quad (3.119a)$$

and

$$20 \log_{10} |H(j2 \tan \frac{2\pi f_q/f_s}{2} s)| \leq -22 \quad (3.119b)$$

The aim of this exercise is to realize the specification mentioned above using the minimum number of stages. As the Chebychev filter is characterized by a sharper transition than the other types, this type was chosen. The order of the filter is obtained by using the following equation [27]:

$$n = \frac{\log_{10}(g + g^2 - 1)}{\log_{10}(\Omega_r + \Omega_r^2 - 1)} \quad (3.120a)$$

where

n denotes the order of the filter

Ω_r denotes the ratio of Ω_q/Ω_p

Ω_p denotes the analog equivalent frequency of ω_p and

is given by $\Omega_p T = 2 \tan (2\pi f_p / 2f_s)$

and

Ω_q denotes the analog equivalent frequency of ω_p

and is given by $\Omega_q T = 2 \tan (2\pi f_q / 2f_s)$

and

$$g = \frac{A^2 - 1}{\epsilon} \quad (3.120b)$$

where

A denotes the parameter related to the stopband loss

(as in this example, 22dB)

ϵ denotes the parameter related to the passband

ripple (as in this example, 0.5dB)

From eqns. (3.120) and using the data in eqns. (3.119), it was established that a fourth-order 0.5 dB Chebychev lowpass filter would satisfy the filter requirements. From sensitivity considerations, two stages of second-order filters are used.

Once this is established, it is a simple matter to obtain the continuous filter coefficient data from the handbooks as mentioned above, and use eqns. (3.116) to obtain the sampled-data filter coefficients.

Thus, for the sharp cutoff lowpass filter, the filter coefficients are calculated:

Stage 1

$$\alpha_1 = 0.181$$

$$\alpha_2 = 0.257$$

$$\alpha_3 = 0.181$$

$$\alpha_4 = 0.181$$

Stage 2

$$\alpha_1 = 0.314$$

$$\alpha_2 = 0.106$$

$$\alpha_3 = 0.314$$

$$\alpha_4 = 0.314$$

The circuit used to realize each stage of the lowpass filter is the same as in Fig. 3.17(b). The transfer function is compared with the desired response in Fig. 3.20. It is readily observed that the circuit realizes the required frequency specification over the entire frequency range, up to the Nyquist limit. This exercise shows that the bilinear transformation element is suitable for realizing the required transfer function with relative ease, compared to the series or parallel mode. The stability of the circuit is also guaranteed provided its

Fig. 3.20 Theoretical response of the lowpass filter using the bilinear transformation element.

analog equivalent is stable too. However, it requires proper balancing of the switched capacitor elements and also more area. Thus, a trade-off is involved in choosing the switched capacitor mode for realizing a filter function.

3.9 A Variable Amplitude and Phase Equaliser Using Switched Capacitor Elements

The possibility of using switched capacitor circuits in designing programmable filters has been indicated previously [1, 21, 25]. In Section 3.7, it was indicated that the bilinear transform realization of the biquad circuit is suitable for obtaining programmable filter. In this section the concept has been utilized for designing switched capacitor programmable variable equalisers (for both amplitude and phase equalisation).

The use of equalisers in communication circuits are varied. The design of any analog cable system is closely related with the equalisation of the end-to-end transmission response. Signals applied at the system input at specific transmission levels must be delivered at the system output at specified levels. It is desired that while traversing the system, all of the signals must experience a specific constant amount of loss or gain independent of the transmitted frequency. The provision of the desired flat transmission response requires the correction or equalisation, of whatever

deviations from nominal may exist in the response of many elements making up the system [28]. Thus, equalisers are used along the length of the system and at the terminals to hold transmission deviations from the ideal condition within acceptable bounds. Amplitude equalisers are used to compensate for the attenuation of the signals in the facility at both the low and high frequency ends [29]. Also, in the reproduction of signals from records, an amplitude equaliser is required to boost the output voltage at frequencies below the crossover frequency [29]. Delay distortion, however, is not a problem in these applications since the human ear is relatively insensitive to phase distortion in the voice signals. Private line data transmission operating in the voice frequency band, on the other hand, requires careful delay equalisation in addition to the equalisation of the amplitude [29]. The above examples justify the importance of investigating the use of switched capacitor circuits to design equalisers.

Equalisers, using passive and active elements, have been demonstrated earlier by previous authors [29, 30, 31]. Fleischer [30] has demonstrated an adjustable equaliser for use in data communication using variable resistors. However, the variable resistors were realized using thin-film resistors and rhodium plated contacts. By selectively shorting various combinations of thin film resistors, the characteristics of the

equaliser were varied. The process is cumbersome and costly. Moreover, these variable resistors add extra load to the op amp, lower the gain of op amp and enhance the noise and offset voltages. The design by Brglez [31] requires lesser active and passive elements. However, it requires simultaneous variations of two resistors to change the Q of the circuit. A more recent paper by Bhattacharya et. al [29] using the simulation of an inductor by active elements has been reported. However, this also lacks the orthogonal property of tuning the equaliser. Besides, the variations of capacitor elements is $9Q^2$ if the resistors are of equal value. Furthermore, none of these filters can be implemented in monolithic integrated form because of the classical problem of realizing an RC-time constant accurately in integrated circuits.

The design of an equaliser using switched capacitor elements provides an alternative to the above active RC equalisers. Using the biquad configuration, the orthogonal property of tuning is maintained. The resonant frequency, Q of the filter and bump height (i.e. gain at resonant frequency) can be independently controlled by gating different combinations of binary-ratioed switched capacitor arrays.

The design of the equaliser requires the realization of the following transfer function:

$$H(s) = \frac{s^2 + h(\Delta\Omega)s + \Omega_0^2}{s^2 + (\Delta\Omega)s + \Omega_0^2} \quad (3.121)$$

where Ω_0 is the resonant frequency; $(\Delta\Omega)$ denotes the bandwidth of the filter and h denotes the bump height or the gain at the resonant frequency. The difference between this design and the previous one is that the circuit realized here has transmission zeros as well as poles in the same circuit.

The system diagram of the equaliser is shown in Fig.

3.21. It is actually a switched capacitor realization of the circuit proposed by Fleischer [30]. It can be observed that the op amps I and II realize the second-order bandpass function. Op amp III utilizes the feedforward approach to obtain the transmission zero. An important point to note is that like the previous cases, this method also requires the two phase operation where in one phase, all charge transfer takes place and during the other phase, the circuit is initialized, i.e. only under such circumstances, the equivalence between resistors and switched capacitor elements are valid. The circuit of Fig. 3.21 meets the above requirement. Hence, the realization of transmission zero and poles do not produce any additional circuit problem. It can also be observed in Fig. 3.21 that each unit is an inverting summer-integrator. Hence, a modular unit, such as shown in Fig. 3.22, was used. Each set of

Fig. 3.21 System diagram of the equaliser using the biquad approach.

Fig. 3.22 Proposed modular unit for the programmable switched capacitor filter.

filter coefficients can be realized by binary-ratioed capacitor banks. Each of these switched capacitor banks are used in the bilinear transformation switched capacitor mode [32]. This modular unit can also be used for realizing the unity-gain inverting amplifier and the summing amplifier. In such cases, the effects of feedback capacitance across the op amps in the inverting amplifier and summer have to be considered.

a. DESIGN METHOD

Initially, the unity gain inverter and the summer will be considered ideal. The z-transform of the transfer function of the bilinear transform switched capacitor circuit may then be written as:

$$H(s) = - \frac{\alpha_5}{\alpha_7} \frac{s^2 + h\alpha_2 s + \alpha_3\alpha_4}{s^2 + \alpha_2 s + \alpha_3\alpha_4} \quad (3.122)$$

where, $\hat{S}$ is an operator defined as

$$\hat{S} = \frac{2}{T} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \quad (3.123)$$

and h is given by the following equation

$$h = 1 \pm \frac{\alpha_1}{\alpha_2} \cdot \frac{\alpha_6}{\alpha_5} \quad (3.24)$$

S may be recognized as the bilinear transform operator for mapping from the s-plane (continuous frequency) to the z-plane (sampled data domain). From the knowledge of s-plane equations and using eqn. (3.123), the following relations may be derived:

$$\text{resonant frequency, } \Omega_0 = 2f_s \sqrt{\alpha_3 \alpha_4} \quad (3.125)$$

$$\text{quality of the pole, } Q'_p = \frac{\sqrt{\alpha_3 \alpha_4}}{\alpha_2} \quad (3.126)$$

and

$$\text{bump height, } h = 1 \pm \frac{\alpha_1}{\alpha_2} \cdot \frac{\alpha_6}{\alpha_5} \quad (3.127)$$

where the bump height denotes the gain at resonant frequency.

The relation between these equations and the actual realization in the sampled-data domain is obtained by the relation [33]:

$$\Omega = \frac{2}{T} \tan \frac{\omega T}{2} \quad (3.128)$$

where ω is the signal frequency in the sampled-data domain, and Ω is the corresponding analog frequency.

The design procedure goes as follows:

$$\omega_L, \omega_H = \omega_0 \left[\sqrt{1 + \left(\frac{1}{2Q_p} \right)^2} \pm \frac{1}{2Q_p} \right] \quad (3.129)$$

where

ω_0 = resonant frequency in radians per second

ω_L = lower 3 dB frequency

and

ω_H = upper 3 dB frequency

Q_p is the desired quality of the pole.

Hence, the corresponding frequencies in the continuous s-domain are given by

$$\Omega_0 = \frac{2}{T} \tan \frac{\omega_0 T}{2} \quad (3.130)$$

$$\Omega_L = \frac{2}{T} \tan \frac{\omega_L T}{2} \quad (3.131)$$

and

$$\Omega_H = \frac{2}{T} \tan \frac{\omega_H T}{2} \quad (3.132)$$

Hence,

$$Q_p = \frac{\Omega_0}{\Omega_H - \Omega_L} \quad (3.133)$$

Therefore, from eqns. (3.122) and (3.125) through (3.133),

the following relations are obtained:

$$\alpha_3 = \alpha_4 = \tan \frac{\omega_0 T}{2} \quad (3.134)$$

$$\alpha_2 = \frac{\alpha_3}{Q_p} \quad (3.135)$$

Using $\alpha_5 = \alpha_6 = \alpha_7$, the bump height will once again be controlled by α_1 only:

$$\alpha_1 = \alpha_2 (1 - h) \quad (3.136)$$

It may be observed from eqn. (3.125) that the resonant frequency is determined by the product of α_3 and α_4 . Therefore, by choosing various coefficients for α_3 and α_4 , it is possible to tune the resonant circuit over a wider range of frequencies. This provides an advantage in designing the equalisers. A computer program was developed to predict the filter coefficients to obtain the nearest approximation to the desired transfer function.

b. EXPERIMENTAL RESULTS

Based on the scheme presented in the above section, experiments were performed for amplitude and phase equalisations

as required in practical circuits. The circuit diagram is shown in Fig. 3.21. The need and requirements for amplitude and phase equalisations are prescribed in the literature [34], which justify the importance of this experiment. Results will be presented in separate sections for the amplitude and phase equalisers.

c. AMPLITUDE EQUALISATION

As a design example, a practical circuit for amplitude equalisation in private line data telecommunication circuits will now be demonstrated. Bhattacharya [29] has reported the following transfer functions to give the gain bumps required in a private line data communication system as one example of equalisers. For amplitude equalisation, they were used as the required characteristics of the filters [29]:

$$300 \text{ Hz bump: } Q_p = 1.3 \quad h = -1.585$$

$$3000 \text{ Hz bump: } Q_p = 4.9 \quad h = -1.679$$

An important consideration in realizing the above transfer functions is the bit-accuracy of the filters. Computer simulations predicted that a minimum of 5-bit accuracy was sufficient to meet the filter requirements over the frequency range of interest. Hence, 5-bit coefficients were

chosen to realize the various filters.

A sampling frequency of 32 kHz was chosen for the main filter banks. Identical coefficients were used in the summer-integrator units (i.e. $\alpha_5 = \alpha_6 = \alpha_7 = .25$). Apart from the reasons presented earlier, these figures were found practical for integrating on a chip from the point of view of silicon area, clock feedthrough, etc.

The 300 Hz bump filter was realized using the bilinear transformation switched capacitor configuration. The same filter function may also be derived using the parallel switched capacitor circuit too. Although it is generally possible to design the equaliser using either mode, it was observed that the latter suffered an additional phase shift (the amount varying with frequency) over the frequency range of interest, thereby deteriorating the equaliser performance. In Fig. 3.23(a), the amplitude response of the 300 Hz bump filter realized using the coefficients is shown. ~~Very~~ good fit between desired and achieved response throughout the frequency range of interest is evident. For clarity, the discrepancy with the continuous active RC filter realization is also shown in Fig. 3.23(b). It is observed that the total discrepancy is less than 0.5 dB over the entire frequency range considered. It is also observed that the maximum error occurs near the resonant frequency. If more accuracy is required,

Fig. 3.23(a) Frequency response of the 300 Hz amplitude equaliser using the circuit of Fig. 3.21. The coefficients used are shown in the inset.

Fig. 3.23(b) Effect of quantization (5-bit accuracy) on the response of the amplitude equaliser I.

then the number of bits in realizing the switched capacitor coefficients has to be increased.

The circuit of Fig. 3.21 using the coefficients shown in Fig. 3.23(a) was simulated in the laboratory using 741 op amps, and CMOS 4066 transmission gates. Discrete capacitors were used to simulate the switched capacitor values. Exact values of these units were arrived at using trimmer capacitors. The experimental results are shown by dotted circles in Fig. 3.23(a). The results agree well with the expected values. The harmonic distortion of the output signal was less than 55 dB over the complete frequency range (0 - 6 kHz) for a 3V peak to peak signal using 10 volts supply for the op amp and the transmission gates.

The 3000 Hz bump filter was realized using the same switched capacitor configuration. As in the previous case, Fig. 3.24 shows the simulated curve for the coefficients shown in the figure itself. These coefficients were arrived at using the design equations (3.134), (3.135) and (3.136). An interesting thing to note is that the transfer function is more accurate than the previous case (Fig. 3.23). This is because of the improved bit quantization accuracy near the resonant frequency. The figure also shows the results of the breadboard simulation, based on the experimental setup described earlier. The agreement between the predicted and actual values over the entire range is evident.

Fig. 3.24(a) Frequency response of the 3000 Hz amplitude equaliser using the circuit in Fig. 3.21. Coefficients for this case are shown in the inset.

Fig. 3.24(b) Effect of quantization on the realized transfer function for the case in Fig. 3.24(a).

The overall result of using the above mentioned amplitude equalisers in cascade with the system to be equalised with is shown in Fig. 3.25. The dotted curve shows the line attenuation. The overall response after equalisation is also shown in the figure. It is readily observed that the equalised output meets the required characteristics. This demonstrates the usefulness of the approach in obtaining amplitude equalisation in practical circuits.

d. PHASE EQUALISER

The importance of phase equaliser for delay equalisations had been indicated earlier. The implementation of such equaliser for a practical requirement will now be demonstrated. Specifications for such equalisers are also available in the literature [34]. The phase equaliser requires an all-pass filter, where the amplitude remains constant over the frequency range of interest, but the phase response varies over the range. The same circuit of Fig. 3.21 may also be used for delay equalisation by replacing h by -1 in eqn. (3.136).

Once again using eqns (3.134), (3.135) and (3.136), the filter coefficients may be obtained. The phase equalisers were also designed on the filter specifications given by Bhattacharya [29], viz.

Fig. 3.25 Figure showing the attenuation to be equalised in one example, and subsequent correction by the amplitude equalisers.

1) resonant frequency, $f_0 = 1600$ Hz

$$Q_p = 1$$

$$h = -1$$

and

2) resonant frequency, $f_0 = 2200$ Hz

$$Q_p = 2$$

$$h = -1$$

The conformal mapping property of the bilinear transform configuration makes ideal for realizing phase equalisers. Figs. 3.26 and 3.27 show the theoretical results as compared to the desired transfer function. It is observed that the two curves match satisfactorily for the frequency range of interest. However, the discrepancy between the two curves is greater, when the signal frequency becomes comparable to the Nyquist frequency. This does not pose any significant problem, because the group delay (which is the function of interest in this case) matches well over the whole range. This is shown in Fig. 3.28. Note that the two curves match well over the whole range of frequencies.

The results in Figs. 3.26 and 3.27 indicate that it is possible to reproduce any desired phase response by using switched capacitor equalisers. The overall results of using the

Fig. 3.26(a) Phase plot of the phase equaliser using the circuit of Fig. 3.21 and the coefficients in the inset.

Fig. 3.26(b) Effect of 5-bit quantization on the realized transfer function for the coefficients in Fig. 3.26(a).

Fig. 3.27(b)

Fig. 3.27(a) Phase plot of the phase equaliser using the circuit of Fig. 3.21 and the coefficients in the inset.

Fig. 3.27(b) Effect of 5-bit quantization on the realized transfer function for the coefficients in Fig. 3.27(a).

Fig. 3.28 Figure illustrating the group delay obtained by the two phase-equalisers as compared to the desired group delays.

two cascaded phase equalisers in this example is demonstrated in Fig. 3.29. The facility characteristics and the overall equalised output are shown in the figure. It is observed that the group delay of the system has been approximately compensated by the two equalisers.

The experiment demonstrates the potential use of switched capacitors in synthesizing prescribed phase response. The fact that the circuit may be fabricated on integrated chips, using the modular approach mentioned earlier, makes it more appropriate for use.

e. DISCUSSION

A circuit has been presented which can serve the purpose of amplitude equalisation for voice transmission and phase equalisation for data transmission. The circuit is inherently stable and the transfer function can be controlled by switching-on and -off an array of capacitors. The practicability of the structure over those presented earlier is immediately evident. The proposed structure is capable of being integrated on IC chips with the available technology. The modular structure makes it ideal for easy reproducibility. The present scheme has the orthogonal tuning property of Fleischer's circuit. However, when the frequency range of interest becomes comparable to the sampling frequency, the frequency warping property of

Fig. 3.29 Figure illustrating a typical system to be equalised and the system after equalisation.

the bilinear transformation circuit has to be considered. The easy tunability of the filter makes it useful for use in communication systems.

Because the filter is a sampled-data filter, it requires an anti-aliasing filter. However, the inherent sample-and-hold action at the input lifts any stringent requirements from the anti-aliasing filter at the input. A simple RC filter with a cutoff frequency at the Nyquist frequency was found to be satisfactory. Because of the sample-and-hold action at the output, no post-filtering is required.

CHAPTER FOUR

PRACTICAL CONSIDERATIONS IN THE DESIGN OF SWITCHED CAPACITOR FILTERS

4.1 Introduction

The design work presented in the previous chapter considered the capacitors, switches and the operational amplifier to be ideal. In actual fact, these elements, when used in MOS LSI technology, are non-ideal. Their shortcomings will be studied in this chapter.

The capacitors realized in MOS technology are usually characterized by a non-linear diffusion-to-substrate capacitance. The switches are realized with MOS transistors. They have finite ON resistance and also have diffusion-to-substrate capacitance. Because of the reverse-biased p-n diode at the diffusions, they also have leakage current. The operational amplifier has finite gain and bandwidth, input offset voltage, limited slew rate and limited phase margin. All these problems combine to produce an output which deviates from the ideal. To study all these effects simultaneously is difficult. Therefore, each one of the problems will be individually studied for each filter, and the significant sources of non-ideal behaviour will be identified. If possible, means of reducing the effects will also be provided.

Section 4.2 deals with the non-ideal properties of the switched capacitor element. Section 4.3 deals with those of the switched capacitor integrator and its subsequent extension to the switched capacitor bilinear transform filter circuit. Section 4.4 deals with the effect of the non-ideal characteristics on the MFB filter. Section 4.5 considers the same effects on the notch filter. Section 4.6 deals with an experiment to validate the major sources of non-ideal behaviour, and indicate a method of improvement.

4.2 Non-Ideal Properties of the Switched Capacitor

It was mentioned earlier that the switched capacitor circuits are realized by using MOS transistors as switches. Some secondary effects are introduced into the network because of this which will be discussed in this section. Although the discussion is general, the analysis will be presented for n-channel MOS transistors.

a. NON-LINEAR p-n JUNCTION CAPACITANCE

The MOS realization of a series switched capacitor filter (integrator) is shown in Fig. 4.1(a). The source and drain diffusions for the two switches are indicated in the figure. It is easy to observe that the source diffusion of the ϕ_1 switch and the drain diffusion of the ϕ_2 switch have junction capacitances, which are effectively acting as

Fig. 4.1(a)

Fig. 4.1(b)

Fig. 4.1(a) A series switched capacitor integrator indicating the diffusions of the MOS FET switches.

Fig. 4.1(b) The equivalent circuit of Fig. 4.1(a) indicating the junction capacitances.

parallel switched capacitances, as depicted in Fig. 4.1(b). The junction capacitance is voltage-dependent. Therefore, in addition to changing the effective value of the resistor, it introduces distortion to the system. This effect will be discussed later.

Let the junction capacitances of the source of the ϕ_1 switch and the drain of the ϕ_2 switch be lumped together as C_D , as shown in Fig. 4.1(b). Assuming shallow junction for the above-mentioned diffusions, so that they may be considered as one-sided step junction, then the junction width W of the reverse-biased diffusions are given by [35],

$$W = \sqrt{\frac{2K_s \epsilon_0}{qN_A} \phi_T} \quad (4.1)$$

where,

W = depletion-region width of the reverse-biased
p-n junction

K_s = dielectric constant of semiconductor

ϵ_0 = permittivity of free space, 8.86×10^{-14} f/cm

q = electronic charge, 1.6×10^{-19} coulombs

N_A = acceptor dopant concentration, holes/cm³

ϕ_T = total electrostatic potential from one side of
the p-n junction to the other

The junction capacitance is given by

$$C_D = \frac{K_S \epsilon_0 A}{W} = \sqrt{\frac{q N_A K_S \epsilon_0}{2(V_R + \phi_B)}} A \quad (4.2)$$

where

$$V_R = V_{BIAS} + v_i - V_{SUB}$$

ϕ_B = built-in voltage of the metallurgical p-n junction

V_{BIAS} = bias voltage applied to the input of the switched
capacitor

v_i = signal voltage applied to the input of the switched
capacitor

V_{SUB} = potential applied to the substrate of the MOSFET
switches

A = effective area of the p-n junction

Eqn. (4.2) may be rewritten as

$$C_D = C_{D0} \left[1 + \frac{v_i}{V_{BIAS} + \phi_B - V_{SUB}} \right]^{-1/2} \quad (4.3)$$

where C_{D0} is the value of the junction capacitance C_D in the absence of signal voltage. C_{D0} is given by

$$C_{D0} = \sqrt{\frac{qN_A K_s \epsilon_0}{2(V_{BIAS} + \phi_B - V_{SUB})}} A \quad (4.4)$$

For small signal analysis, C_D may be simplified as

$$C_D \approx C_{D0} \left[1 - \frac{1}{2} \frac{v_i}{V_{BIAS} + \phi_B - V_{SUB}} \right] \quad (4.5)$$

provided that

$$v_i \ll V_{BIAS} + \phi_B - V_{SUB} \quad (4.6)$$

The effect of the junction capacitance on the system behaviour may be viewed from two different points of view. Firstly, the junction capacitance has an average value, C_{D0} , which can be, to a first-order approximation, considered constant. The difference equation for this case may be written as

$$C_R(v_{i,n} - v_{o,n}) + C_{D0}(v_{i,n-1} - v_{o,n}) = -C_L(v_{o,n} - v_{o,n-1}) \quad (4.7)$$

The transfer function, $H(z)$, is given by

$$H(z) = \frac{V_o(z)}{V_i(z)} = - \frac{C_R + C_{DO}z^{-1}}{C_R + C_{DO} + C_L(1-z^{-1})} \quad (4.8)$$

If the signal frequency is negligible compared to the sampling frequency, the time-constant of this first-order sampled-data filter is given by $T(C_L/[C_R+C_{DO}])$, where T is the sampling interval of the ϕ_1 and ϕ_2 clocks. Thus, to a first-order approximation, the effect of this junction capacitance C_D , is to lower the nominal resistive value of the switched capacitor by the ratio $C_{DO}/(C_R+C_{DO})$. Analysis similar to that of the series case for the parallel switched capacitor also leads to the same conclusion.

Secondly, the junction capacitor, being voltage-dependent, introduces harmonic distortion in the integrator. To analyze this, the amount of charge delivered by the junction capacitor C_D to the summing junction is calculated as follows. Let the input voltage be v_i . Then the charge delivered by the junction capacitance to the negative input of the op amp is given by:

$$\Delta q_d = \int_0^{v_i} C_D dv \quad (4.9)$$

$$= \int_0^{v_i} \frac{C_{DO}}{\sqrt{1 + \frac{v}{V_t}}} dv \quad (4.10)$$

which is obtained by combining eqns. (4.9) and (4.3). In eqn. (4.6), V_t is given by

$$V_t = V_{BIAS} + \phi_B - V_{SUB} \quad (4.11)$$

From eqn. (4.10), after some simple mathematical manipulation, the following relation is obtained:

$$\Delta q_d = C_{DO} v_i - \frac{1}{4} C_{DO} \frac{v_i^2}{V_t} \quad (4.12)$$

In order to simplify the analysis, the continuous equivalence approach is invoked, i.e., the switched capacitors are replaced by the resistive equivalence as given by eqn (2.1).

In this case, equating the input charge and feedback charge (via the integrating capacitor), the following relation may be written:

$$\frac{1}{T} \left[v_i C_R + v_i C_{DO} - \frac{1}{4} C_{DO} \frac{v_i^2}{V_t} \right] = - C \frac{dv_o}{dt} \quad (4.13)$$

Letting v_i be a sinusoidal input, $V_i \sin \omega t$, the various harmonic contents may be identified:

$$\text{i.e.} \quad v_i = V_i \sin \omega t \quad (4.14)$$

where V_i is the input voltage, and ω is the frequency of the input voltage

$$\text{and let } v_o = V_1 \sin \omega t + V_2 \sin 2\omega t \quad (4.15)$$

Thus equating the various harmonics:

$$V_1 = - \frac{C_R + C_{DO}}{j\omega C T} V_i \quad (4.16)$$

$$V_2 = \frac{C_{DO} V_i^2}{16\omega C T V_t} \quad (4.17)$$

Eqn. (4.17) gives a measure of the second harmonic distortion arising due to the non-linear junction capacitance. Eqn. (4.17) indicates that the second harmonic is proportional to the ratio C_{DO}/C , and also V_i/V_t . This means that the harmonic distortion can be reduced by making C_{DO} as small as possible, compared to C .

b. INCOMPLETE TRANSFER OF CHARGE

The switches have finite ON resistance. Hence, the maximum switching rate of the switched capacitor networks will

be determined by the need to ensure that relatively complete charge transfer has occurred during the finite pulse-widths of the clocks. This sets a limit on the maximum size of C_R , relative to the size of the switches, and limits the precision (i.e., amplitude and frequency distortion) which deteriorates with increase in sampling frequency.

The effect of the finite pulse-width of the ϕ_2 clock for the series switched capacitor may be derived as follows: the non-ideal behaviour of the series switched capacitor circuit, depicted in Fig. 4.2(a), is shown in Fig. 4.2(b). Assuming that the ϕ_1 pulse is sufficiently wide to discharge the switched capacitor C_R completely, then

$$v_2(o) = v_o(o) \quad (4.18)$$

where $v_o(o)$ and $v_2(o)$ denote the initial voltages held on the nodes 1 and 2 in Fig. 4.2(b) respectively. When the ϕ_2 switch closes, the voltage $v_2(t)$ at any later time, t , is given by

$$v_2(t) = v_i(o) [1 - e^{-\Delta T/rC_s}] + v_o(o) e^{-\Delta T/rC_s} \quad (4.19)$$

where

$v_i(o)$ denotes the initial voltage on the input node when the ϕ_2 switch closes

Fig. 4.2(a)

Fig. 4.2(b)

Fig. 4.2(a) A series switched capacitor circuit.

Fig. 4.2(b) The equivalent circuit during the ON-time of ϕ_2 , assuming finite-ON resistance of the switch.

$v_o(0)$ denotes the initial voltage on the output node
when the ϕ_2 switch closes

r is the effective resistance of the MOSFET switch
(assumed constant)

C_s is the effective capacitance of the capacitors

C_R and C_L in series, i.e., $C_s = C_R C_L / (C_R + C_L)$

If the pulse-width of the ϕ_1 pulse is ΔT , then by using
eqn. (4.19), the following relation is obtained:

$$v_2(\Delta T) = \frac{C_R}{C_R + C_L} \left[1 - e^{-\Delta T / r C_s} \right] v_i(0) + \left[1 - \frac{C_R}{C_R + C_L} \left\{ 1 - e^{-\Delta T / r C_s} \right\} \right] v_o(0) \quad (4.20)$$

Eqn. (4.20) may be rewritten as a difference equation
as follows:

$$v_{o,n} = v_{o,n-1} + \frac{C_R}{C_R + C_L} \left\{ 1 - e^{-\Delta T / r C_s} \right\} \left[v_{i,n} - v_{o,n} \right] \quad (4.21)$$

Comparing eqn. (4.21) with (2.4), it is observed that
the effect of the finite resistance of the ϕ_2 switch is to
increase the time constant by the proportion $1/(1 - e^{-\Delta T / r C_s})$.

This also means an effective increase of the resistive value of the switched capacitor by the same proportion. For instance, if ΔT is four times the time constant rC_s , resistive value of the series capacitor increases by 1.86%.

If the ϕ_1 switch is also considered non-ideal, the transfer function will deviate further away from eqn. (2.4). The initial condition for this case is given by

$$v_2(0) = v_0(0) \left[1 - e^{-\Delta T/rC_R} \right] \quad (4.22)$$

Eqn. (4.22) indicates the partial discharge of the switched capacitor C_R . By mathematical manipulation as in the previous case, the following difference equation is obtained:

$$v_{0,n} = v_{0,n-1} + \frac{C_R}{C_R+C} \left\{ 1 - e^{-\Delta T/rC_s} \right\} \left[v_{i,n} - v_{0,n} \right] - \frac{C_R}{C_R+C} e^{-\Delta T/rC_R} v_{0,n-1} \quad (4.23)$$

The last term may be considered to introduce distortion of the signal, i.e., the response deviates from the simple first-order difference equation with a continuous equivalence.

Analysis similar to that above may also be done for the parallel switched capacitor, also leading to the same conclusion.

c. CLOCK FEEDTHROUGH NOISE

The gate-to-diffusion capacitance introduces further non-ideal behaviour of the switches. This capacitance, being lumped together with the fringing, channel charging and discharging capacitance is "feedthrough capacitance" C_f . The effect of this capacitance is to introduce offset error into the system.

The analysis follows from Fig. 4.3. Assuming that the output node is holding the correct voltage v_0 , when ϕ_1 is off, and working through the output voltage over one complete sampling interval, it is easy to see that the feedthrough introduces offset error equal to $-(C_f/C')V_{\phi_2}$, where C' is the effective value of the capacitors C_R and C in series, and V_{ϕ_2} is the height of the ϕ_2 pulse. If $C_R \ll C$, then the offset error becomes equal to $-(C_f/C_R)V_{\phi_2}$. The same result is also obtained by starting from the assumption that the output is valid when ϕ_2 is off and going through one complete sampling interval.

The value of the offset error can be minimized by making C_R significantly larger than C_f , but this limits the maximum switching frequency, as discussed in the previous section. Thus, in practice, compromise between the two must be reached to get optimum result.

3

Fig. 4.3

Fig. 4.4

Fig. 4.3 Switched capacitor circuit illustration of clock feedthrough capacitances.

Fig. 4.4 Parallel switched capacitor circuit indicating leakage current.

d. LEAKAGE CURRENT

Another factor that may effect the behaviour of the switched capacitor is the leakage current of the p-n junction. The leakage current is primarily the generation current in the depletion region in silicon. Whereas the series switched capacitor delivers the charge instantaneously to the output node, the parallel switched capacitor has an inherent delay before it is delivered to the output node. During the interval between the time the signal is being sampled and the time it is delivered, the leakage current can degrade the information content as is evident from Fig. 4.4.

The sources of dark current include the band-to-band transition of electrons, diffusion of minority carriers from the bulk, generation within the depletion region by recombination-generation centers in silicon and the surface generation current. The most significant source of them being the generation in the depletion region given by [36],

$$I_g = \frac{1}{2} q \frac{n_i}{\tau_0} WA \quad (4.24)$$

where

q = electronic charge, 1.6×10^{-19} coulomb

n_i = intrinsic carrier concentration, $1.45 \times 10^{10} \text{ cm}^{-3}$
for Si

τ_0 = effective lifetime within a reverse-biased depletion region

W = depletion region width of the p-n junctions

A = the cross-sectional area of the metallurgical junction

Again, by combining eqn. (4.24) with (4.3),

$$I_g = I_{g_0} \left[1 + \frac{V_i}{V_t} \right]^{1/2} \quad (4.25)$$

where

$$I_{g_0} = \frac{1}{2} q \frac{n_i}{\tau_0} \sqrt{\frac{2K_s \epsilon_0 V_t}{qN_A}} \quad (4.26)$$

and

$$V_t = V_{BIAS} + \phi_B - V_{SUB} \quad (4.27)$$

K_s = dielectric constant of semiconductor

ϵ_0 = permittivity of free space

N_A = acceptor dopant concentration holes/cm³

V_{BIAS} = bias voltage applied to the input of the switched capacitor

ϕ_B = built-in voltage of the metallurgical junction

V_{SUB} = potential applied to the substrate of the MOSFET switches

v_i = signal voltage applied to the input of the switched capacitor

Let the interval between the ϕ_1 and ϕ_2 switches be δT , and let the charge stored on C_R during the ϕ_1 pulse be given by v_i . Then the charge lost due to the leakage current in time δT is given by

$$I_g dt = -C_R dv \quad (4.28)$$

or,

$$I_{g0} \sqrt{1 + \frac{v}{V_t}} dt = -C_R dv \quad (4.29)$$

which is obtained by combining eqns. (4.28) and (4.25). Eqn. (4.29) may be reorganized and integrated as follows:

$$I_{g0} \int_0^{\delta T} dt = -C_R \int_{v_i}^{v_f} \frac{dv}{\sqrt{1 + \frac{v}{V_t}}} \quad (4.30)$$

Solving (4.30), the following relation is obtained,

viz.

$$I_{g_0} \delta T = -C_R 2V_t \left[\sqrt{1 + \frac{V_f}{V_t}} - \sqrt{1 + \frac{V_i}{V_t}} \right] \quad (4.31)$$

Reorganizing eqn. (4.31),

$$V_f = V_i - \frac{I_{g_0} \delta T}{C_R} \sqrt{1 + \frac{V_i}{V_t}} + \left[\frac{I_{g_0} \delta T}{2C_R} \right]^2 \frac{1}{V_t} \quad (4.32)$$

Assuming small leakage, the third term in eqn. (4.32) may be neglected.

$$\text{Assuming } v_i = V_i \sin \omega t \quad (4.33)$$

and

$$\begin{aligned} V_f = & V_0 + V_{11} \sin \omega t + V_{21} \sin 2\omega t + V_{31} \sin 3\omega t + \dots \\ & + V_{12} \cos \omega t + V_{22} \cos 2\omega t + V_{32} \cos 3\omega t + \dots \end{aligned} \quad (4.34)$$

Combining eqns. (4.32) and (4.33) gives

$$V_0 \approx - \frac{I_{g_0} \delta T}{C_R} \quad (4.35)$$

$$\begin{aligned} V_{11} &= V_i - \frac{I_{g_0} \delta T}{2C_R} \cdot \frac{V_i}{V_t} \\ &\approx V_i \left(1 - \frac{I_{g_0} \delta T}{2C_R V_t} \right) \end{aligned} \quad (4.36)$$

$$V_{12} = 0$$

(4.37)

$$V_{21} = 0$$

(4.38)

$$V_{22} \approx \frac{1}{16} \frac{V_i^2}{V_t}$$

(4.39)

and so on.

Thus, eqns. (4.35) through (4.39) indicate that the effect of the leakage current is to introduce offset error and harmonic distortion. It is assumed in this analysis that the leakage current acts as a harmonic generator which is fed to a network that is linear. Thus, the harmonics are only acted upon by the transfer function of the circuit.

e. CLOCK FEEDTHROUGH, OFFSET ERROR AND NOISE

Fig. 4.5b shows the output of the circuit of Fig. 4.5a with no input signal, demonstrating the offset error effects mentioned in the previous section. This experiment was performed on the initial test chip shown in Fig. 2.3(a). There are three separate traces shown. The input switched capacitor circuit is shut off, so the amplifier is in self-biasing mode, with the output voltage acquiring enough offset to feedback through the feedback switched capacitor, a current equal to

Fig. 4.5(a)

Fig. 4.5 (b)

Fig. 4.5(a) Figure illustrating the experimental setup for studying the effect of leakage on switched capacitor circuit.

Fig. 4.5(b) Picture demonstrating the effect of leakage at low sampling (50 Hz) for the circuit shown in Fig. 4.5(a). Horizontal scale: 5 msec/cm. Vertical scale: .01 volt/cm.

the net leakage current onto the summing junction. The clock frequency was lowered to 50 repetitions per second to make the effects visible. The top trace in Fig. 4.5b is for a substrate bias of -5 volts. The vertical discontinuity is happening at the instant (ϕ_1 on), when the leakage controlling charge is delivered back to the summing junction. As leakage thereafter is accumulated, it is integrated in the feedback capacitor and a ramp is generated at the output. The average output offset developed here is 2.5 millivolts. The middle trace of Fig. 4.5b is as in the top trace except with the substrate bias increased from -5 volts to -7 volts. This is the point of onset of high diffusion leakage, which increases the average output offset to 11 millivolts.

The bottom trace of Fig. 4.5b is with substrate bias at -5V again, but with ϕ_2 of the input switched capacitor of Fig. 4.5b also operating. The summing junction is now picking up the leakage onto the input switched capacitor C_1 , which is appearing as a step when ϕ_2 is turned on, i.e. halfway up the ramp. There is additionally leakage from the feedback switched capacitor, C_f , which is part of the vertical discontinuity at the end of the ramp - a positive step cancelled by the larger negative feedback charge caused by the output offset.

Also seen in Fig. 4.5b is the clock feedthrough from overlap capacitance of the transistor switches. At this low

clock frequency, the on-time of the clocks is relatively short, so the feedthrough (at the ramp discontinuities) is just visible. The feedthrough amplitude here is 6 millivolts. Its theoretical amplitude is given by the clock pulse height times the ratio of feedthrough capacitance to feedback capacitance. It is evident that active switched capacitive filters must be operated with a feedback capacitor, to prevent the amplifier from being open loop to capacitive feedthrough from the switches.

The basic switched capacitor element of Fig. 2.1 consists of two MOS transistor switches, which are sources of noise for the element. In order to evaluate the effect of the "noisy" switched capacitor element, the total integrated noise of the circuit in Fig. 2.1(b) is investigated.

Fig. 4.6(a) illustrates the two noise sources S_1 and S_2 by e_{n_1} and e_{n_2} respectively. R_{s_1} and R_{s_2} denote the respective ON resistances of the two switches. For multiple sources of noise in a linear system, the sources may be considered individually and then superposition may be applied. Thus, considering e_{n_1} and e_{n_2} separately, and assuming R_{s_1} and R_{s_2} to be negligible, the effect of the sample-and-hold action of the switched capacitor element on the power spectral density is given as:

$$\langle e_{n_1}'^2 \rangle = \langle e_{n_2}'^2 \rangle = \frac{kT}{C_R} \cdot \frac{1}{f_s/2} \quad (4.40)$$

where

e_{n_1}' denotes the spectral density of the noise source
 e_{n_1} after the effect of sampling has been
 considered

e_{n_2}' denotes that of the noise source, e_{n_2}

k denotes the Boltzman constant

T the absolute temperature in degrees Kelvin

C_R is the switched element capacitance

and

f_s is the sampling frequency

In each case, the transfer function of the passive
 integrator is the same:

$$H(z) = \frac{C_R/(C_R + C)}{1 + (C/(C_R + C))z^{-1}} \quad (4.41)$$

Thus, the mean-squared noise power of the switched capacitor integrator (Fig. 4.6a) is given by:

$$\langle e_{n_0}^2 \rangle = |H(z)|^2 \langle e_{n_1}^2 \rangle + |H(z)|^2 \langle e_{n_2}^2 \rangle \quad (4.42)$$

Hence, the total noise power integrated up to the Nyquist frequency is given by

$$P = [\langle e_{n_1}^2 \rangle + \langle e_{n_2}^2 \rangle] \int_0^\pi \frac{\beta d(\omega T)}{1 + (1-\beta) e^{-j\omega T}} \quad (4.43)$$

where

$$\beta = C_R / (C_R + C) \quad (4.44)$$

By algebraic manipulation, it is possible to show that the total integrated noise power reduces to

$$P = 2KT/C \quad (4.45)$$

The implication of this exercise is that the switched capacitor configuration maintains the same level of noise as its continuous counterpart.

Fig. 4.6b shows a spectrum analyzer photograph for the passive single pole filter with a 38 pf load, the sampling frequency being 100 KHz. The top trace is the frequency

Fig. 4.6(a)

Fig. 4.6(b)

Fig. 4.6(a) Equivalent circuit of the switched capacitor element illustrating the noise sources and the effective ON-resistance of the switches S_1 and S_2 .

Fig. 4.6(b) Frequency spectrum of the lowpass filter (Fig. 4.6(a)) Top trace shows the noise spectral density (amplified by 70 dB) at the output terminal of the device.
Horizontal scale: 0.5 KHz/div.
Vertical scale: 10 dB/div.

response up to 50 KHz. The bottom trace shows the noise spectrum (with a previous low noise preamplifier gain of 70 dB). The spectrum at 100 Hz bandwidth averages - 130 dB. The RMS random noise from 10 Hz to 10 KHz was measured to be 7 microvolts.

The noise output of the active filter circuit of Fig. 4.5a was also measured at a clock rate of 100 KHz for unity gain configuration. The rms noise from 10 Hz to 10 KHz was 60 microvolts with a 1/f spectrum, after circuit precautions were taken to reduce the common mode noise from power supply and ground. This suggests that as far as switched capacitor circuits are concerned, independent of the operational amplifier, it is possible to attain signal-to-noise ratio of over 100 dB for audio filtering, assuming 1 volt dynamic range.

4.3 Non-Ideal Aspects of the Bilinear Transform Switched Capacitor Filter

Both the lowpass filter and the programmable equaliser are realized using the bilinear transform switched capacitor elements. Hence, the sources of non-linearity and noise in such systems will be studied. Both of these filters were realized using the biquadratic approach. Therefore, the analysis of these filters boils down to analyzing that of a switched capacitor integrator as in Fig. 3.4(b). Each individual source of non-ideal behaviour will be identified

and the analysis done considering that as the only source of such behaviour. Finally by comparing all of them, the major sources of non-linearity and signal-to-noise ratio will be investigated.

a. THE NON-IDEAL NATURE OF THE OPERATIONAL AMPLIFIER

As in other filters, the integrator of Fig. 3.4(b) is affected by the finite gain and unity gain bandwidth product of the op amp. Assuming the op amp as a wide-band amplifier, the effect of finite-gain of the operational amplifier may be analyzed as follows (re. Fig. 4.7(a)):

$$\begin{aligned}
 H(z) &= - \frac{\alpha_R (1 + z^{-1})}{(1 + \frac{1}{A}) (1 - z^{-1}) + \frac{2\alpha_R}{A}} \\
 &= - \frac{\alpha_R (1 + z^{-1})}{(1 - z^{-1})} \cdot \left[\frac{1}{1 + \frac{1}{A} + \frac{2\alpha_R}{A} \cdot \frac{1}{1 - z^{-1}}} \right] \quad (4.46)
 \end{aligned}$$

The quantity in the parenthesis shows the proportional deviation from the ideal behaviour. This factor indicates that the integrator time constant is effected by approximately the factor $(1 + \frac{1}{A})$. Even for a d-c gain of 1000, this is only

Fig. 4.7(a)

Fig. 4.7(b)

Fig. 4.7(a) A switched capacitor integrator circuit - with a finite op amp gain.

Fig. 4.7(b) Circuit diagram to study the effect of finite gain of the op amps on the response of the biquad switched capacitor circuit.

0.1% and does not pose any serious problem. However, the remaining factors in the parenthesis denotes an additional phase shift to the integrator. While realizing high Q filters, this phase shift may degrade the performance of the filter.

Based on eqn. (4.46), the transfer function of the second-order biquad bilinear transform switched capacitor filter may be derived: (Ref. Fig. 4.7(b))

$$H(z) = \frac{\alpha_1 \beta_1 \left(\frac{1+z^{-1}}{1-z^{-1}} \right)}{1 + \alpha_2 \beta_2 \left(\frac{1+z^{-1}}{1-z^{-1}} \right) + \alpha_3 \alpha_4 \beta_3 \cdot \left(\frac{1+z^{-1}}{1-z^{-1}} \right)^2} \quad (4.47)$$

where

$$\beta_1 = [1 + 1/A_1 + 2\alpha_1/(A_1(1-z^{-1}))]^{-1} \quad (4.48)$$

$$\beta_2 = [1 + 1/A_1 + 2\alpha_2/(A_1(1-z^{-1}))]^{-1} \quad (4.49)$$

and

$$\beta_3 = [1 + 1/A_1 + 1/A_2 + 2(\alpha_3/A_1 + \alpha_4/A_2)/(1-z^{-1})]^{-1} \quad (4.50)$$

Eqn. (4.47) is a fourth-order transfer function. It is difficult to find a general solution for the resonant frequency and Q of the filter. In the above equation, A_1 denotes the gain of the op amp I and A_2 that of the op amp II (Fig. 4.7(b)).

If $\alpha_3, \alpha_4 \ll 1$, then the resonant frequency is diminished by the ratio $1/(1 + 1/A_1 + 1/A_2)^{1/2}$. The Q of the filter is approximately affected by the ratio A_2/A_1 , if $A_1, A_2 \gg 1$, and $\alpha_2 \ll 1$. For high Q filters, the effect of the phase shift due to the factors $2\alpha_2/(A_1(1-z^{-1}))$, $2\alpha_3/(A_1(1-z^{-1}))$ and $2\alpha_4/(A_2(1-z^{-1}))$ have to be considered. For the high-Q filter discussed in section 3.7, the effect of finite op amp gain on the filter response (amplitude and phase response) is shown in Fig. 4.8. The effect on the filter characteristics is also shown in the inset. It is observed that an op amp gain of 2000 or higher is sufficient for high Q filters. For lower Q, lesser op amp gain may be tolerated. It may be noted that on-chip MOS amplifiers with gain to this order have already been reported.

The gain bandwidth product of the operational amplifier gives a measure of the corner frequency, ω_c , of the op amp. If the sampling frequency ω_s (in radians), becomes comparable to ω_c , then the op amp cannot reach steady-state value within the pulse-width of the switched capacitors. This may be evaluated by assuming the op amp as a first-order lowpass filter, with an open loop low frequency gain of A and the corner frequency given by ω_c , ($\omega_c = \omega_u/A$, where ω_u is the unity gain bandwidth). In such case, the step response of the operational amplifier is given by:

Fig. 4.8(a)

Fig. 4.8(b)

Fig. 4.8(a) Amplitude response of the biquad filter using the bilinear mode switched capacitor elements for finite gain of the op amps, as indicated in the figure.

Fig. 4.8(b) Phase response of the above mentioned circuit.

$$u(t) = \frac{A}{j\omega_c} [1 - e^{-j\omega_c t}] \quad (4.51)$$

where

A denotes the low frequency gain of the op amp

ω_c denotes the corner frequency in radians

For a pulse width τ of the sampling clocks, the final value to a unit step input is

$$u(\tau) = \frac{A}{j\omega_c} [1 - e^{-j\omega_c \tau}] \quad (4.52)$$

Thus, the effect of the finite bandwidth is to reduce the step response by a factor $(1 - e^{-j\omega_c \tau})/j\omega_c \tau$. Equivalently, this may be considered as a reduction of the open loop gain of the op amp by the same factor. The additional phasor introduced thus may cause further deterioration of the phase angle. For example, an omp with a gain of 1000 and unity gain bandwidth of 2 MHz, the reduction is 0.1% with a phase angle of 5° , for a pulse width of 15 μ s (corresponding to sampling frequency of 32 kHz).

When the switched capacitor filters are cascaded, the equivalent input and output impedance of the adjacent stages of filters have to be considered. The equivalent input

impedance of the switched capacitor integrator is approximately given by $T/2\alpha_R C$, where T is the sampling interval and $\alpha_R C$ is switched capacitor value. The output impedance of the integrator in the continuous case is given by

$$z_{out}(s) \approx \frac{z_o(s)}{1 + A'(s)B(s)} \quad (4.53)$$

where

$z_o(s)$ = output impedance of the op amp

$A'(s)$ = unloaded amplifier gain at the complex frequency s

$B(s)$ = voltage feedback ratio at the same frequency.

The output impedance of the switched capacitor integrator is however different for the complementary clocks, ϕ_1 and ϕ_2 (Ref. Fig. 4.7). When ϕ_1 is ON (i.e., ϕ_2 OFF), the voltage feedback ratio, $\beta_1(s)$, given by V_x/V_o , is effected by the stray capacitance, C_s at the virtual ground node:

$$\beta_1(s) = \frac{V_x}{V_o} = \frac{C}{C + C_s} \quad (4.54)$$

This is because, for this situation, the virtual ground node is isolated from the input node. In this case $\beta_1(s)$ is approximately unity assuming the stray capacitance, C_s , is negligible compared to C . For a large open loop gain, the output impedance approximately equals $z_o(s)/A'(s)$.

Alternatively when ϕ_2 is ON (i.e., ϕ_1 OFF), the feedback ratio, $\beta_2(s)$ is given by

$$\beta_2(s) = \frac{V_x}{V_o} = \frac{C}{C + 2\alpha_R C} = \frac{1}{1 + 2\alpha_R} \quad (4.55)$$

For a large open loop gain, the output impedance $z_{out}(s)$, is approximately $z_o(s)/A'(s)\beta_2(s)$. Even for $\alpha_R = .25$, $\beta_2(s)$ equals $2/3$. That means the closed loop output impedance is higher than the previous case by 50%. For a large open loop gain, $A'(s)$, the closed loop output impedance is very small anyway. Hence, this increase in closed loop output impedance is negligible.

The discussion of the output impedance may be summarized as follows:

$$\phi_1 \text{ ON, } \phi_2 \text{ OFF: } \beta_1(s) = C/(C + C_s); z_{out}(s) = z_o(s)/A'(s)\beta_1(s) \quad (4.56a)$$

$$\phi_1 \text{ OFF, } \phi_2 \text{ ON: } \beta_2(s) = C/(C + 2\alpha_R C); z_{out}(s) = z_o(s)/A'(s)\beta_2(s) \quad (4.56b)$$

where

$\beta(s)$ denotes the voltage feedback ratio

C_s denotes the stray capacitance

C denotes the integrating capacitor

$\alpha_R C$ denotes the switched capacitance

$A'(s)$ denotes the open-loop gain (no load)

To summarize the above results, for an operational amplifier with an open loop gain of 1000 or higher, the effect of its non-ideal behaviour, even for a Q of 100, was found to be small. The unity-gain bandwidth product of 2 MHz or higher was also found satisfactory. The major effect of the op amp was the enhancement of noise, especially the $1/f$ noise.

So far as the switched capacitor circuits are concerned, lower coefficient values or identically higher sampling frequency are preferable for good signal-to-noise ratio. The integrated noise over the passband in this case is also small.

b. EFFECT OF OFFSET VOLTAGE ON A LOSSY INTEGRATOR

Although the offset voltage does not directly effect the transfer function, it causes the zero-input response to be non-zero. For large offset, the harmonic distortion would increase, as the op amp saturates earlier. Hence, the dynamic range is reduced. The effect of offset voltage is studied in the case of lossy integrator. The model for studying this effect is shown in Fig. 4.9. The transfer function is given by

$$H(z) = 1 + \frac{\alpha_1/\alpha_2}{1 + \frac{1}{\alpha_2} \cdot \frac{1-z^{-1}}{1+z^{-1}}} \quad (4.57)$$

For a d-c offset, V_{os} , the output of the integrator also has a d-c offset given by

$$V_{o,offset} = V_{os} \cdot H(z) \Big|_{z=e^{j\omega T}, \omega=0} = \left(1 + \frac{\alpha_1}{\alpha_2}\right) V_{os} \quad (4.58)$$

For a high gain system, the offset voltage is increased by the factor α_1/α_2 . This would require the offset correction mechanism. For low gain, this can be usually neglected.

By simple extension of the arithmetic to a second order state-variable system (Fig. 4.7(b)), the d-c offset of

Fig. 4.9 Figure illustrating the model to study the effect of offset voltage on a lossy integrator.

the system may be derived:

$$V_{\text{offset, bandpass}} = V_{\text{offset, lowpass}} = V_{\text{os2}} \quad (4.59)$$

It is observed that the offset of the integrating op amp II of Fig. 4.7(b) is only manifested at the output. This is because the bandpass section offers a high impedance to the offset of the op amp I itself. The integrating section, on the other hand, passes the low frequency signal. It is, therefore, displayed at the output. Because of feedback, the same output also appears at the output of the bandpass section.

c. EFFECT OF JUNCTION LEAKAGE

In section 2.12(d), it was observed that the effect of junction leakage was to attenuate the signal, and also to introduce distortion into the system. So far as its effect on the transfer function is concerned, the leakage may be modelled by a linear resistor between the diffusion and substrate. For a lossy integrator, the model is shown in Fig. 4.10(a). The transfer function then becomes

$$H(z) = - \frac{\alpha_1(1 + \beta_1 z^{-1})}{1 + z^{-1} + \alpha_2(1 + \beta_2 z^{-1})} \quad (4.60)$$

Fig. 4.10(a)

Fig. 4.10(b)

Fig. 4.10(a) Figure illustrating the model for studying the effect of p-n junction leakage on a lossy integrator.

Fig. 4.10(b) Figure incorporating the gain parameter to model the effect of leakage.

where

$$\beta_1 = (1 - \frac{T}{\alpha_1 C} \cdot \frac{1}{R_1}), \quad \beta_2 = (1 - \frac{T}{\alpha_2 C} \cdot \frac{1}{R_3}) \quad (4.61)$$

The reduction in the values of the parallel capacitors will have two effects. Because of the reduction of the coefficient of the input parallel switched capacitor, the low frequency gain would be lower than the design values. For the reduction of the feedback parallel switched capacitor, the cutoff frequency would be higher than the design value. The effect may be modelled as in Fig. 4.10(b) by incorporating a multiplier in the parallel branch. It is interesting to note that the reduction in the coefficients is proportional to the ratio of the switched capacitor equivalent resistor to the "leakage resistor" (i.e., the first-order equivalent of leakage current).

Using this model, the transfer function for the biquad filter is obtained as

$$H_B(z) = - \frac{\alpha_1 \cdot \frac{1+\beta_1 z^{-1}}{1-z^{-1}}}{1 + \alpha_2 \frac{(1+\beta_2 z^{-1})}{(1-z^{-1})} + \alpha_3 \alpha_4 \cdot \frac{(1+\beta_3 z^{-1})(1+\beta_4 z^{-1})}{(1-z^{-1})^2}} \quad (4.62)$$

For high Q filters, it is observed that the equivalent switched capacitor resistance for α_1 and α_2 may become comparable to the leakage resistances. Thus, the effect of leakage current on the Q of the filter and the gain at resonant frequency is more than that on the resonant frequency itself. This was also observed in the experiment in section 3.9. In order to evaluate the extent of this effect, a computer simulation of the "leaky" biquad circuit was performed, the results of which are presented in Fig. 4.12. From Fig. 4.12, it is observed that as the parameter T/RC (where T is the sampling frequency, C is the integrating capacitor and R is the leakage resistance) becomes comparable to the smallest coefficient of the filter, the effect on the filter characteristics is considerable. This is because leakage reduces drastically charge held on the smaller capacitors. It is observed that the smallest coefficient should be at least a decade larger than the parameter T/RC to obtain the desired filter characteristics.

One way to compensate for the effect is to scale the capacitors sufficiently high that the effect of leakage current is reduced. Alternatively, the bilinear transform switched capacitor element may be made slightly assymetrical; i.e., the parallel switched capacitor element may be designed to have a value larger than the series switched capacitor element by the ratio β .

Fig. 4.11(a) Amplitude response of the biquad resonator for various values of the leakage parameter, ρ .
Fig. 4.11(b) Phase response of the above mentioned circuit.

Fig. 4.12 Experimental demonstration of the effect of leakage on the biquad bilinear wide filter. The input to the filter is shown at the top. The response at the bandpass and lowpass outputs are shown. Note that the response at resonance is approximately 2 dB lower than the expected value (0 dB).

The leakage current also introduces harmonic distortion because of the non-linear leakage current. Its effect may be considered in the same manner as in section 4.2(d). Since no further insight may be obtained by the analysis and the analytical solution is quite involved, this was not done. However, an estimate of this may be obtained from the analysis of section 4.2(d).

The effect of leakage current on the response of the high Q bandpass filter was observed to be dominant. The response at the resonant frequency was observed to be approximately 2 dB lower than the designed values. The other parameters, however, remained unaffected. This is illustrated in Fig. 4.12.

d. EFFECT OF MISMATCHED CAPACITORS

The capacitors realized in MOS technology can be slightly different from the design values. Although, by making the design values sufficiently large, the deviations can be made minimal, their effects have to be considered. Let the deviations from the ideal of the switched capacitor coefficients be given by (Ref. Fig. 4.13(a)):

$$\alpha_{R_1}' = \alpha_R (1 + \epsilon_1) \quad (4.63a)$$

$$\alpha_{R_2}' = \alpha_R (1 + \epsilon_2) \quad (4.63b)$$

Fig. 4.13(a)

Fig. 4.13(b)

Fig. 4.13(a) Figure illustrating the effect of stray capacitance on a switched capacitor integrator.

Fig. 4.13(b) Pole zero diagram of the integrator in the z-plane.

where

α_R is the designed coefficient

ϵ_1 is the error in realizing the series switched capacitor

ϵ_2 is the error in realizing the parallel switched capacitor

In this case, the transfer function of the integrator becomes

$$H(z) = -\alpha_R \cdot \frac{z+1}{z-1} \left[1 + \frac{\epsilon_1 z + \epsilon_2}{z+1} \right] \quad (4.64a)$$

$$= -\alpha_R \frac{z+1}{z-1} + \frac{\epsilon_1 z}{z-1} + \frac{\epsilon_2}{z-1} \quad (4.64b)$$

Equation (4.64a) shows the deviation of the transfer function from the ideal. Both the magnitude and phase of the integrator deviates from the ideal by the factor $(\epsilon_1 e^{j\omega T} + \epsilon_2)/(e^{j\omega T} + 1)$, where T is the sampling interval and ω is the signal frequency.

Alternatively, the integrator may be considered as the superposition of the three integrators:

- 1) the ideal bilinear switched capacitor
coefficient α_R
- 2) the series switched capacitor
coefficient $\epsilon_1 \alpha_R$
- 3) the parallel switched capacitor
coefficient $\epsilon_2 \alpha_R$

This is illustrated by the eqn. (4.64b). The effect of these non-idealities may be better illustrated from the pole-zero diagram in Fig. 4.13(b). For the ideal integrator, the pole z_p , and zero, z_z of the integrators in z-domain are:

$$z_p = 1 \quad (4.65a)$$

$$z_z = -1 \quad (4.65b)$$

In this non-ideal case, they are

$$z_p = 1 \quad (4.66a)$$

$$z_z = -\frac{1+\epsilon_2}{1+\epsilon_1} \quad (4.66b)$$

As the transfer function at any signal frequency is the ratio of two vectors from the zero and pole to the signal frequency, it is observed that for small clock frequency, the

magnitude is negligibly effected. But the effect on the phase angle is more appreciable. For a high Q filter, this may introduce errors in the result. Near the Nyquist frequency, both the magnitude and phase angle are appreciably effected. But if the transfer function is sufficiently attenuated, then the effect is negligible.

To estimate the effect of stray capacitance and mismatched capacitances, Monte Carlo simulation of a high Q filter using the bilinear transformation was done, for various ranges of allowable capacitance variations. The result is shown in Table II. It is observed that for resonant frequency nearer to the Nyquist frequency and for the same tolerance, the deviation from the expected value increases, which is intuitively obvious, i.e., for such cases, tighter control on the process parameters is needed for the same performance of the filter.

e. EFFECT OF DIFFUSED JUNCTION CAPACITANCE

Capacitors realized in MOS technology [46] are characterized by a stray capacitance, viz. the diffusion capacitance from the floating nodes of the switched capacitors to ground. For polysilicon-oxide-polysilicon capacitors, these diffusion capacitances have negligible values; on the other hand, metal-oxide-diffusion or polysilicon-oxide-diffusion capacitors would

TABLE II

Tolerance in capacitors	2%	5%	2%	5%	2%	5%
Designed center frequency, Hz (clock frequency being 20KHz)	1000	1000	2500	2500	5000	5000
Designed bandwidth, Hz (Q = 100 nominal)	10	10	25	25	50	50
Expected center frequency, Hz (for an ensemble of 100)	999.6	998.5	2498	2498	5001.3	4998
Standard deviation of the center frequency, Hz	1.2	2.0	1.6	8.0	2.6	8.9
Expected bandwidth, Hz	9.9	10.1	24.0	24.1	50.7	54.0
Standard deviation of the bandwidth, Hz	0.2	0.5	1.0	2.6	4.2	9.0

Sampling frequency for this set of data: 20KHz

have values which may be comparable to the gate-to-silicon (linear) capacitors. This is especially so if the diffusion dopant concentration is small.

The effect of the junction capacitance of the MOS switches S1 and S2 is two fold (Ref. Fig. 4.14):

- 1) it increases the effective values of the parallel switched capacitor by the d-c value of the junction capacitance, C_{D2} , and
- 2) it introduces non-linearity into the system because of the voltage-dependence of the capacitor, C_{D2} .

The first factor has already been considered by the effect of stray capacitance on the integrator. The second factors will now be discussed. It may be noted that the other junction capacitors are not considered because C_{D1} , C_{D3} and C_{D4} are all voltage constrained (Ref. Fig. 4.14). Hence, they do not affect the filter behaviour. On the other hand, C_{D2} is acting on a floating node; hence, it is most dominant. Assuming the open-loop gain of the op amp as very large, the following difference equation may be written:

Fig. 4.14

Fig. 4.14 Figure illustrating the non-linear diffusion capacitances present at the different nodes of the bilinear-switched capacitor integrator.

$$\alpha_R C [v_{i,n} + v_{i,n-1}] + \int_{v_{i,n-1}}^0 C_{D2} v dv = - C [v_{o,n} - v_{o,n-1}] \quad (4.67)$$

Using eqn. (4.5), and integrating eqn. (4.67), the following relation may be derived:

$$\alpha_R C [v_{i,n} + v_{i,n-1}] + 2C_{D0} V_t \left[1 - \left(1 - \frac{v_{i,n-1}}{V_t} \right)^{1/2} \right] = - C [v_{o,n} - v_{o,n-1}] \quad (4.68)$$

If $v_{i,n-1} \ll V_t$, the eqn. (4.68) may be simplified to:

$$\alpha_R C [v_{i,n} + v_{i,n-1}] + C_{D0} v_{i,n-1} + \frac{1}{4} C_{D0} \frac{v_{i,n-1}^2}{V_t} \approx - C [v_{o,n} - v_{o,n-1}] \quad (4.69)$$

It is observed that the above equation is a non-linear difference equation. Hence, the z-transform method cannot be used. Instead, a computer-aided method was used to evaluate the time-domain response to a sinusoidal input. By using the DFT algorithm, the harmonic content of the output was evaluated. The result is illustrated in Fig. 4.15.

Fig. 4.15 Figure illustrating the harmonic distortion present in the switched capacitor lossy integrator (Fig. 4.14). The feedback switched capacitor coefficients were chosen identical to the input coefficients.

The analysis may be extended to the second-order section. It does not provide any additional insight into the behaviour of the filter. Hence, the analysis was not performed.

f. SIGNAL-TO-NOISE RATIO

To evaluate the signal-to-noise ratio of a lossy integrator, the sources of noise are identified in Fig. 4.16(a). The switched capacitor noise for each individual element was shown in section 4.2 as similar to that in the continuous resistor.

$$\text{i.e. } \langle e_n^2 \rangle = 4kTR = 4kT (1/f_s \alpha_R C) \quad (4.70)$$

where

k = Boltzmann constant

T = temperature in Kelvin, $^{\circ}\text{K}$

f_s = sampling frequency

$\alpha_R C$ = value of the switched capacitor

The total noise, $\langle e_{no}^2 \rangle$, is computed as (Ref. Fig. 4.16(a))

Fig. 4.16(a)

Fig. 4.16(b)

Fig. 4.16(a) Figure showing the noise sources in the switched capacitor elements.

Fig. 4.16(b) Figure showing the noise source in the op amp.

$$e_{no}^2 = \int_0^{f_s/2} [|H_1(z)|^2 \langle e_{n1}^2 \rangle + |H_2(z)|^2 \langle e_{n2}^2 \rangle] df \quad (4.71)$$

where

$$H_1(z) = - \frac{\alpha_1/\alpha_2}{1 + \frac{1}{\alpha_2} \cdot \frac{1-z^{-1}}{1+z^{-1}}} \quad (4.72)$$

and

$$H_2(z) = \frac{1}{1 + \frac{1}{\alpha_2} \cdot \frac{1-z^{-1}}{1+z^{-1}}} \quad (4.73)$$

Assuming the transfer function may be approximated by a brickwall filter up to n times the cutoff frequency f_c of the lossy integrator, where n is a constant of proportionality, then the following equations may be derived:

$$\int_0^{f_s/2} |H_1(z)|^2 \langle e_{n1}^2 \rangle df = \frac{\alpha_1}{\alpha_2} n f_c \langle e_{n1}^2 \rangle \quad (4.74)$$

where

$$f_c = 2f_s \tan^{-1} \alpha_2 \quad (4.75)$$

Similarly the second component may also be computed.

The total noise from the switched capacitors may then be

written as

$$\langle e_{no}^2 \rangle = \frac{\alpha_1}{\alpha_2} n f_c \langle e_{n1}^2 \rangle + n f_c \langle e_{n2}^2 \rangle \quad (4.76)$$

where f_c is given by eqn. (4.75). Again, by analysis similar to that in section 4.2(e), it may be shown that the total integrated noise power from each switched capacitor element equals kT/C .

Furthermore, the noise power spectral density of the operational amplifier is given by

$$\langle e_{op}^2 \rangle = \frac{K_1^2}{f} + K_2^2 \quad (4.77)$$

where

K_1^2 denotes the component contributing to $1/f$ noise

K_2^2 denotes the thermal noise of the op amp

The contribution from the op amp is obtained from Fig. 4.16(b). This component of output noise is given by

$$\langle e_{o,op}^2 \rangle = \int_0^{f_s/2} \langle e_{op}^2 \rangle |H_{op}(z)|^2 df \quad (4.78)$$

Fig. 4.17

Fig. 4.17 Figure illustrating the op amp noise sources of the biquad filter using the bilinear transformation elements.

where

$$H_{op}(z) = \frac{(\alpha_1 + \alpha_2)/\alpha_2 + \frac{1}{\alpha_2} \cdot \frac{1-z^{-1}}{1+z^{-1}}}{1 + \frac{1}{\alpha_2} \cdot \frac{1-z^{-1}}{1+z^{-1}}} \quad (4.79)$$

Once again approximating the first-order function by a brickwall filter of amplitude n and cutoff at f_c , then

$$\langle e_{o,op}^2 \rangle = (1 + \frac{\alpha_1}{\alpha_2}) [K_1^2 \log_e \frac{f_b}{f_a} + n f_c K_2^2] \quad (4.80)$$

where f_a and f_b are the lower and upper bounds for the $1/f$ noise.

Hence, the total noise power of the integrator is the rms summation of the two components. In the present state of the MOS op amp design, the $1/f$ noise from the op amp is the dominant component [37]. Hence, the noise power spectral density of the switched capacitor integrator becomes

$$\langle e_{o,op}^2 \rangle = (1 + \frac{\alpha_1}{\alpha_2}) K_1^2 \log_e \frac{f_b}{f_a} \quad (4.81)$$

For the high Q biquad bandpass filter case, the analysis involves eight switched capacitors and three

op amps. However, from the discussion of the integrator above, it may be inferred that the noise from the op amp is the most dominant noise. Then, from Fig. 4.17, the output of the high Q biquad filter at the bandpass output can be found using the transfer functions between the noise sources and the bandpass output, i.e.,

$$\begin{aligned} \langle e_{nB}^2 \rangle = & \left[1 - \frac{(\alpha_1 + \alpha_3)S + \alpha_3\alpha_4}{S^2 + \alpha_2S + \alpha_3\alpha_4} \right] \langle e_{n1}^2 \rangle + \\ & \left[\frac{\alpha_3S + \alpha_3\alpha_4}{S^2 + \alpha_2S + \alpha_3\alpha_4} \right] \langle e_{n2}^2 \rangle \end{aligned} \quad (4.82a)$$

where

$$S = \frac{1-z^{-1}}{1+z^{-1}} \quad (4.82b)$$

and the coefficients are as indicated in Fig. 4.17. e_{n1} and e_{n2} denote the noise sources of the op amps I and II respectively and are as defined in eqn. (4.77). The noise power spectral density has three components as seen from eqn. (4.82a). The first component is the direct feed through of e_{n1} to the output. The second component is the filtered output of noise from the first op amp and the third component is that from the second op amp. Thus,

$$\begin{aligned}
 \langle e_{nB}^2 \rangle &= \langle e_{n1}^2 \rangle + \int_0^{f_s/2} \langle e_{n1}^2 \rangle |H_1(z)|^2 df \\
 &\quad + \int_0^{f_s/2} \langle e_{n2}^2 \rangle |H_2(z)|^2 df
 \end{aligned} \tag{4.83}$$

where

$\langle e_{nB}^2 \rangle$ denotes the rms noise power at the bandpass output

and

f_s denotes the sampling frequency

$$H_1(z) = \frac{(\alpha_1 + \alpha_3)S + \alpha_3\alpha_4}{S^2 + \alpha_2S + \alpha_3\alpha_4} \tag{4.84}$$

and

$$H_2(z) = \frac{\alpha_3S + \alpha_3\alpha_4}{S^2 + \alpha_2S + \alpha_3\alpha_4} \tag{4.85}$$

For a high-Q bandpass filter, eqn. (4.83) may be approximately obtained by assuming the filter as cutting off at the 3 dB points. In such a case, eqn. (4.83) becomes

$$\begin{aligned}
e_{nB}^2 = e_{n1}^2 + e_{n1}^2 \left[\left(\frac{\alpha_1 + \alpha_3}{\alpha_2} \right)^2 + \left(\frac{\alpha_3 \alpha_4}{\alpha_2} \right)^2 \right] K_{1,1}^2 \log_e \frac{f_b}{f_a} \\
+ e_{n2}^2 \left[\left(\frac{\alpha_3}{\alpha_2} \right)^2 + \left(\frac{\alpha_3 \alpha_4}{\alpha_2} \right)^2 \right] K_{1,2}^2 \log_c \frac{f_b}{f_a} \quad (4.86)
\end{aligned}$$

assuming $1/f$ noise in the amplifier dominates, and where

$K_{1,n}$ denotes the K_1 component of noise of the n .th
op amp K_1 is defined in eqn. (4.72)

Equation (4.86) indicates that larger values of α_1 , α_3 and α_4 and smaller values of α_2 increase the noise content than smaller values. In effect, this means that as the resonant frequency becomes comparable to the Nyquist frequency, or as the Q of the filter is increased, or as the gain at resonant frequency is increased, the noise spectral density also increases. Correspondingly the signal-to-noise ratio is decreased. Hence, it is preferable to use smaller coefficients (i.e., higher sampling frequency) if higher signal-to-noise ratio is desired.

The noise spectral density for the bilinear transform bandpass filter was also measured. The results are presented in Fig. 4.18. It is observed that the spectral density of the

Fig. 4.18 Figure showing the transfer function and the noise spectral density of the bilinear transform biquad filter (X-Y recorder output; spectrum analyzer bandwidth = 30Hz).

Fig. 4.19 Figure showing the frequency spectrum of the bilinear transform biquad filter in the passband. The frequency spectrum of the input frequency is also shown for the sake of comparison.

noise is maximum at the resonant frequency. The integrated noise of the bandpass filter was measured at 30 μv . The harmonic distortion of the filter in the passband was also evaluated. The frequency spectrum for an input frequency of 1500 Hz is shown in Fig. 4.19. For a peak-to-peak signal voltage of 3 volts, the harmonic distortion was measured to be -55 dB. The corresponding signal-to-noise ratio is computed as 90 dB from the random noise measurement.

4.4 The Infinite-Gain Multiple Feedback Lowpass (MFB) Filter

The systems analysis of the MFB filter was presented in section 3.4. However, the circuit implementation requires more careful consideration of the various non-ideal behaviours of the capacitors, the op amp and the switches. The effects of the factors will be studied individually in the following subsections where the result differs from those in the biquad filter case.

a. DIFFUSED JUNCTION CAPACITANCE OF THE CAPACITORS

In the presence of non-linear junction capacitances, the circuit looks like that in Fig. 4.20. The non-linear capacitors are shown as $\gamma_1 C$, $\gamma_2 C$, ... $\gamma_7 C$. The junction capacitors include those of the capacitors as well as those of the MOS switches. Of these, the ones that are voltage

Fig. 4.20 Figure illustrating the presence of various non-linear junction capacitances present in the MOS LSI realization of infinite-gain multiple feedback filter.

constrained do not pose any problem, viz. $\gamma_1 C$ and $\gamma_7 C$. However, the fact that the other nodes are "floating" means that the corresponding junction capacitances take part in charge sharing, thereby affecting the transfer function of the circuit. A comprehensive analysis of the whole circuit taking all the capacitances at one time is difficult, and do not provide any further insight into the circuit behaviour. So each junction capacitance will be considered individually. As the integrating capacitor C is very large compared to $\gamma_2 C$, $\gamma_4 C$ and $\gamma_6 C$, the effects of these capacitances are similar to that described in section 4.2(a); $\gamma_3 C$ is very small compared to C , and therefore, may be ignored. The effect of $\gamma_5 C$ to the total harmonic distortion of the system is dependent on the open-loop gain of the amplifier. For an ideal infinite-gain amplifier, the circuit should present no additional problem. But in reality, the finite gain of the amplifier may introduce non-linearity into the system, because of the fact that the "virtual ground" (at the negative terminal of the op amp) is not a "true" ground. The effect of the junction capacitance to a finite-gain amplifier input may be analyzed from Fig. 4.20.

Defining the junction capacitance $\gamma_5 C$ as in eqn. (4.3), eqn. (3.42) may be rewritten as

$$q_n = \alpha_3 C (v_{1,n} - \frac{v_{o,n}}{A}) = -C_2 (1 - \frac{1}{A}) (v_{o,n} - v_{o,n-1}) + \frac{C_{D0}}{A} [v_{o,n} - v_{o,n-1}] - 2C_{D0} V_t \frac{1}{8} \frac{(v_{o,n}^2 - v_{o,n-1}^2)}{(AV_t)^2} \quad (4.87)$$

where

C_{D0} = d-c value of the junction capacitance of $\gamma_5 C$

A = open loop gain of the op amp

V_t is defined by eqn. (4.11)

From eqn. (4.87), it is evident that for large values of A , the effect of C_{D0} is negligible. This is intuitively obvious because in such cases, v_B will be extremely small. Hence, the departure of v_B from virtual ground will also be small. Even for an open loop gain of 1000, C_{D0} is reduced by the same factor. Hence, the effect of $\gamma_5 C$ becomes significantly reduced.

The harmonic distortion of the MFB filter (continuous equivalence) was measured over the passband. For a 3 volts peak-to-peak signal, the maximum harmonic distortion was measured at approximately 4 kHz as -54 dB.

b. NON-IDEAL CHARACTERISTICS OF THE OPERATIONAL AMPLIFIER

In the analysis of infinite gain MFB filter of section 3.4, the operational amplifier was considered of infinite gain and bandwidth. But in practice, both gain and bandwidth of the amplifier are finite. Its effect will now be considered in the perspective of the available op amp. It is a well known fact that at low frequencies the response of an integrator (the operational amplifier with feedback capacitor C_2 is an integrator) departs from the ideal due to finite gain of the amplifier, A ; at high frequencies, the departure is due to the finite amplifier bandwidth [38].

First the effect of finite gain of the amplifier, A , will be investigated. By analysis similar to that in section 3.4, the transfer function may be evaluated:

$$H(z) = - \frac{\frac{C_{R1} C_{R3}}{C_1 C_2}}{(1-z^{-1})^2 + ((C_{R1} + C_{R2} + C_{R3})/C_1)(1-z^{-1}) + \frac{C_{R2} C_{R3}}{C_1 C_2}} \quad (4.88)$$

where

$$C'_{R2} = C_{R2} \left(1 + \frac{1}{A} \frac{C_{R3}}{C_{R2}} \right) \quad (4.89)$$

and

$$C'_2 = C_2 \left(1 - \frac{1}{A}\right)$$

(4.90)

Thus, the effect of feedback is to reduce the value of C_2 and increase that of C_{R_2} . Considering the open-circuit gain of the op amp as 1000, the effective value of C_2 is reduced by 0.1% and C_{R_2} is increased by .07%. The overall effect of it is to reduce the resonant frequency (approximately 3 dB point of the lowpass circuit) by 0.2%. The effect is minimal and may, therefore, be neglected. The finite bandwidth of the op amp affects the high-frequency signals, and as in our case, the gain-bandwidth product is 5 MHz or higher, and the sampling frequency is low (256 kHz) compared to it, the effect on the transfer function is limited. However, if the filter were used for sampling frequencies of, say 2 MHz or higher, it can be shown by qualitative arguments, that the transfer function would be affected. In fact, if the system cannot settle down to the sampled-data value within the pulse-width, the transfer function would be dependent on pulse-width.

The input offset voltage, V_{os} , of the operational amplifier will affect the dynamic range of the op amp. The effect of V_{os} on the output may be studied by considering a voltage source V_{os} at the positive terminal of the op amp and grounding the input terminal.

The transfer function between the output terminal and the positive terminal of the op amp is, for the series switched capacitor case,

$$H_{os}(z) = \frac{C_{R3} (C_{R1} + C_{R2} + C_1 (1-z^{-1}))}{C_{R2} C_{R3} + (C_{R1} + C_{R2} + C_{R3}) C_2 (1-z^{-1}) + C_1 C_2 (1-z^{-1})^2} \quad (4.91)$$

Thus, the effect of V_{os} at the output is

$$V_o, V_{os} = \frac{C_{R3} (C_{R1} + C_{R2})}{C_{R2} C_{R3}} V_{os} \quad (4.92)$$

It is observed that the designed circuit virtually doubles the offset voltage. For on-chip cancellation of the offset voltage, V_{os} , chopper stabilization may be used. However, for this case, this was not deemed necessary.

To study the effect of slew rate limitation, it may be observed that the lowpass filter output goes through the maximum time rate of change at the corner frequency of the filter. At the corner frequency, the filter output can be assumed quasi-continuous. Thus, the maximum rate of change of the output voltage is $A\omega_c/2$, where A is the amplitude of the sinewave and ω_c is the corner frequency in radians. Thus,

the signal change between sampling intervals is $\Delta\omega_c/2f_s$, where f_s is the sampling rate. As for example, assuming 10 volts dynamic range, $f_c = 4000$ Hz and $f_s = 256$ kHz, the signal change expected at the output is 0.25V between sampling intervals. Assuming the pulse-width as $1 \mu s$, the slew rate required from the operational amplifier is $.25V/\mu s$. The operational amplifier used has a much higher slew rate and is considered satisfactory for the circuit. The operational amplifiers realized in MOS LSI technology have also met the required specifications [37].

c. SIGNAL-TO-NOISE RATIO OF THE MULTIPLE FEEDBACK FILTER

All the significant sources of noise, viz. e_{n1} , e_{n2} , e_{n3} , due to switched capacitors $\alpha_1 C$, $\alpha_2 C$ and $\alpha_3 C$ respectively and also that due to the op amp, e_{nA} , are shown in Fig. 4.21. The overall effect of them is obtained by superposition. Thus, the total noise power e_{no}^2 , of the system is given by

$$e_{no}^2 = \frac{1}{\Delta^2} \left\{ (\alpha_1 \alpha_3)^2 \langle e_{n1}^2 \rangle + (\alpha_2 \alpha_3)^2 \langle e_{n2}^2 \rangle + \alpha_3 (\alpha_1 + \alpha_2 + (1 - z^{-1}))^2 [\langle e_{n3}^2 \rangle + \langle e_{nA}^2 \rangle] \right\} \quad (4.93)$$

Fig. 4.21

Fig. 4.21 Figure illustrating the noise sources present in the switched capacitor MFB filter.

Fig. 4.22 X-Y recorder output of the MFB filter for cases II and III, showing the transfer function and the noise for the two cases.

where

$$\Delta = \alpha_2 \alpha_3 + (\alpha_1 + \alpha_2 + \alpha_3) \beta (1 - z^{-1}) + \beta (1 - z^{-1})^2 \quad (4.94)$$

The noise spectra of the MFB filter (Case II and Case III of section 4.5) were studied experimentally. This is shown in Fig. 4.22. It is observed that Case II which corresponds to higher Q than Case III has higher noise content at resonance. It is also seen that the maximum noise spectral density is near the cutoff frequency. This is because the first stage of the filter has a fairly high Q . The integrated noise over a bandwidth of 1000 Hz (center frequency of 4.3 kHz) was measured as 21 μ v. This means that the signal-to-noise ratio for Case II and Case III are 93.5 dB and 86 dB respectively; both of the above cases correspond to a total harmonic distortion of 54 dB.

4.5 Notch Filter

The notch filter is essentially a passive filter. The op amp at the output acts only as a buffer. It could be replaced by simply a source follower. However, the addition of the op amp provides some flexibility in the design. As for example, by feeding back a fraction of the output, the Q of the notch may be controlled. The non-ideal behaviour of the filter will now be discussed.

$$C_1 = C_2 = \frac{C_2}{2} = C_{128}$$

C = Contact diffusion capacitance

$$C_4 = C_5 = \frac{C_6}{2} = C_N$$

CD_9 = Switch

CD_n = Diffusion to substrate capacitance of the n-th capacitor.

Fig. 4.23 Figure illustrating the various diffusion capacitances present in the MOS LSI realization of the twin-tee notch filter.

a. THE DIFFUSED-JUNCTION CAPACITANCES

As in the MFB, the non-linear diffusion-to-substrate capacitances of the capacitors and the switches complicate the behaviour of the filter. The circuit, considering the junction capacitances, is shown in Fig. 4.23. If the system can be considered linear, the constant part of the junction capacitances, C_{D0} , will affect the transfer function. Once again, if the effect of all the capacitances are considered together which interact with each other at each sampling interval, the analysis becomes complicated. Therefore, by considering numerical values for each of the capacitances, a computer simulation was done. The results indicate that the notch frequency changes by less than 1% taking care of all the capacitances.

The effect of nonlinearity of the junction capacitance is involved and does not provide much insight into the filter behaviour. Hence, the analysis will only be considered partially, i.e., the dominant source of nonlinearity will be identified and its effect will be studied.

From the actual circuit built, the dominant junction capacitance is seen to appear at the positive input of the op amp. Hence, the circuit to be analyzed is as shown in Fig. 4.24.

Fig. 4.24 Figure illustrating the dominant non-linear capacitance in a notch filter.

Therefore, eqns. (3.66) and (3.67) remain valid.
Equation (3.68) is rewritten considering the non-linear
load capacitance C_{D0} as:

$$C_{R2} [v_{1,n} - v_{3,n}] + C_2 [(v_{2,n} - v_{2,n-1}) - (v_{3,n} - v_{3,n-1})] \\ \approx C_{D0} \cdot 2V_t \left[\sqrt{1 + \frac{v_{3,n}}{V_t}} - \sqrt{1 + \frac{v_{3,n-1}}{V_t}} \right] \quad (4.95)$$

where

C_{R2} is the switched capacitance shown in Fig. 4.24

C_2 is the integrating capacitance shown in Fig. 4.24

C_{D0} is the d-c value of the non-linear diffusion
capacitance at node 3

$v_{l,n}$ denotes the sampled voltage at the l -th node at the
 n -th instant.

The detailed derivation is given in Appendix III. Using eqns.
(3.66), (3.67) and (4.95), $v_{3,n}$ may be derived over one complete
cycle of a sinusoid. Discrete Fourier Transform of the sampled
wave shape may be used to derive its harmonic content. The

detailed analysis is also presented in Appendix III. Based on the analysis, the results are presented in Fig. 4.25. The results indicate that the harmonic distortion increases with lower substrate voltage, lower bias voltage and also higher signal voltage. It also increases with higher signal frequency, the reason being that the diffusion capacitor has higher signal swing between two sampling intervals. On the other hand, it decreases for higher sampling frequency for the same reason.

b. NON-IDEAL NATURE OF THE OP AMP

The op amp is used as a unity gain buffer amplifier. All the characteristics of the continuous counterpart will be affecting the circuit. As for example, for a finite gain op amp, the op amp output is attenuated by a factor of approximately $1/(1+1/A(s))$, where $A(s)$ is the open-loop gain of the op amp at the signal frequency. Because of the reduced feedback involved from the output, this would also affect the Q of the notch. However, even for an open loop gain of 1000, this reduction is less than 0.1% and hence, becomes of negligible importance. The noise analysis of the notch filter proceeds in the same manner as the MFB filter. As the device is passive except for the buffer amplifier, it is expected that the total noise power will be low.

Fig. 4.25 Figure illustrating the harmonic content of the notch filter for various values of gain (K).

4.6 Comments

In this chapter, the effect of non-ideal characteristics of the elements used in switched capacitor circuits were identified. Analysis for these non-ideal behaviours have also been presented. Certain inferences may be made in a general sense:

The two major sources of non-ideal behaviours in such filters are stray capacitance and diode leakage from the switched capacitance. The stray capacitance affects the transfer characteristics; the effect being more pronounced in high Q filters. In integrated circuits, such stray capacitance effects may be minimized by taking proper precautions [39].

Diode leakage also effects the filter performance, mainly in the passband of the filters. It also introduces harmonic distortion, thus reducing the dynamic range of the filters. There is no way to eliminate these problems. However, they may be reduced by making the switched capacitors as large as may be possible for a given area on the integrated circuit.

4.7 An Alternative Solution for Compensating the Dominant Non-Ideal Behaviours

In section 4.6, two major sources contributing to errors in realizing a designed filter were identified, viz. stray capacitance and leakage current from the diffusions.

Both these factors require that the smallest switched capacitor value be large enough that the above mentioned sources become negligible. However, for high Q filters, it was noticed that the range of capacitance was very high. That means the chip area becomes excessively large for such cases, i.e. trade-off between the Q of the filter and the chip area is involved, the reason being that chip area is inversely related to the smallest realizable coefficient. However, if the coefficient may be realized by an alternate means, the switched capacitors may be made arbitrarily large. This is evident from Fig. 4.26(b), where the alternative means of realizing the coefficients is to use a four-quadrant multiplier. The switched capacitors may now be increased to the value of the integrating capacitor, C . If the coefficients are positive, a two-quadrant multiplier is sufficient. However, in general both coefficients may have to be realized in a recursive filter. Hence, a four quadrant multiplier was considered a better choice.

The proposed scheme can also be extended to realize the second-order biquad filter. The system diagram of the filter is shown in Fig. 4.26(c). More about this circuit will be discussed later.

There are a number of advantages of using this scheme. Firstly, the fact that the switched capacitor values are identical to the integrating capacitor value means that the

Fig. 4.26(a)

Fig. 4.26(b)

Fig. 4.26(c)

Fig. 4.26(a) Figure illustrating the presence of parasitic capacitance and leakage current in a switched capacitor circuit.

Fig. 4.26(b) The circuit of Fig. 4.26(a) with the switched capacitor component being removed from the circuit.

Fig. 4.26(c) The switched capacitor biquad circuit with the coefficients disassociated from the switched capacitor elements.

range of capacitors is minimized to unity. Secondly, in Fig. 4.26(a), it has been shown earlier that the switched capacitor $\alpha_1 C$ has to be large compared to the stray capacitance, C_s , and diode leakage factor, T/R . If α_1 is a small value in order to realize accurately the switched capacitor coefficient $\alpha_1 C$, the chip area increases to a large value. But in Fig. 4.26(b), it is only necessary that the integrating capacitor value, C , be large compared to the stray capacitance, C_s , and diode leakage factor, T/R . Thus, the corresponding chip area is smaller than the earlier case. Thirdly, by similar reasoning, the capacitor value, C , may be chosen large enough compared to the diffusion capacitance. Therefore, harmonic distortion may also be minimized.

As mentioned earlier, the proposed scheme depends on accurate low noise realization of the coefficients by a two- or four-quadrant multiplier.

The four-quadrant multiplier is useful for realizing negative coefficients. This may be useful for some filters; as for example, in the biquad, by realizing $-\alpha_4$ instead of α_4 , one inverting amplifier may be avoided. Previous authors [40, 41] have discussed the implementation of such multipliers in MOS LSI chips. With small modifications, either of the two schemes may be used to implement the analog multiplier.

It should be mentioned that to realize smaller coefficients, higher bit accuracy of the multiplier is needed. This means larger chip area would be required. Hence, practical implementation in a chip would require some sort of multiplexing such that one analog multiplier of sufficiently large resolution can be used to implement each coefficient of the filter. This was considered beyond the scope of the present research work. Hence, only the circuit of Fig. 4.26(c) was investigated experimentally. The analytical results of this circuit are identical to those in section 3.7. Hence, the experimental results on the circuit would be presented now.

To validate the concept, the circuit of Fig. 4.26(c) was implemented on the breadboard, using multiplying digital-to-analog converters (MDAC's) for the analog multipliers. A commercially available 10 bit CMOS MDAC (AD7520JD by Analog Devices) was used for this purpose. The capacitors were chosen of equal value (1500 pF) for all the capacitors. The op amps used were 741's and the transmission gates were CMOS 4066 types. The circuit to be experimentally demonstrated is the high-Q bandpass filter of section 3.7. The design specifications were chosen identical to the previous one. The results are demonstrated in Fig. 4.27. The resonant frequency and Q of the filter were experimentally derived as 1485 Hz and 49.5

Fig. 4.27 X-Y recorder output of the circuit in Fig. 4.26(c). The small overshoot at the resonant frequency is due to the inaccuracy in realizing the coefficient, α_1 .

respectively. It is observed that unlike the previous one, the resonant frequency gain suffered no unpredictable insertion loss. This confirms the assertion made in section 4.7 that the major sources of error are diode leakage and stray capacitances. In Fig. 4.28, the spectrum of the passband of the filter is shown. It is observed that the harmonic distortion of the filter for a 3 volts peak-to-peak signal is less than 70 dB as opposed to 58 dB in the previous case. This also validates the inference made earlier in this section.

In Fig. 4.29, the noise spectral density of the filter is shown. Curiously this filter has a large noise content, the reason being that the smaller coefficients are associated with a large attenuation and thus a reduction of signal to noise ratio.

This experiment validates the point that special precautions have to be taken to minimize stray capacitance and diode leakage while realizing high Q bandpass filters. It also demonstrates the use of a four-quadrant multiplier to build a general purpose filter, whose characteristics can be altered by only changing the coefficients (i.e., bit patterns of the MDAC).

Fig. 4.28 Harmonic distortion in the passband of the circuit in Fig. 4.26(c). Note that the second and the third harmonics are appreciably smaller than those in Fig. 4.19, signifying that the harmonic distortion is associated with the realization of the smaller coefficients in the earlier case (Fig. 3.15(b)).

Fig. 4.29 Figure illustrating the transfer function and the noise spectrum of the circuit in Fig. 4.26(b).

CHAPTER FIVE

CONCLUSIONS

5.1 Summary of the Work

In Chapter one, it was mentioned that the aim of this thesis is to study the feasibility of the switched capacitor circuit in realizing monolithic integrated filters. These filters should meet the required specifications without parametric trimming. In the last few chapters, it has been established that the switched capacitor filter can meet the above-mentioned requirement. Furthermore, it is compatible with MOS LSI technology, and is suitable for use in system LSI applications. It was also demonstrated in this thesis that it is possible to use the knowledge of active RC filters in designing switched capacitor filters.

In Chapter two, preliminary investigations of the switched capacitor element were done. An initial test chip, which consisted of switched capacitor elements, an integrating capacitor and a single ended amplifier was used for this purpose. The switched capacitor element has properties similar to that of a resistor. However, the fact that the former operates in the sampled-data domain makes it unique in its behaviours. Qualitative correspondence between the resistor and the switched capacitor element was established. Thus, a

state-variable type second-order filter, having both lowpass and bandpass output, was constructed. In this chapter, two basic types of switched capacitor element, viz. series and parallel, were put forward. Basically they perform the same; however, some subtle differences remain. This was studied in Chapter three.

In Chapter three, the two modes of switched capacitor elements were studied. It was revealed that under certain circumstances, the series and parallel switched capacitor element realize the backward and forward difference equation. Thus, it is possible to use the large body of knowledge available in active RC filters to design sampled-data filters using switched capacitors. Lowpass, bandpass and bandstop filters have been successfully constructed using the above transformations. However, realizing high-Q filters using the above mentioned modes proved to be difficult. This was solved by suitably combining the two modes. Consequently, the bilinear transform switched capacitor element was obtained. This element was found to be specially suitable for designing high Q filters. Finally, it was also demonstrated that this new element is useful for designing the biquad equaliser. It was shown that the equaliser can be used for both amplitude- and phase-equalisation. Besides, by choosing different combinations of switched capacitors, it is possible to realize

a variable equaliser. Thus, a programmable equaliser has been successfully demonstrated in this work. Furthermore, the fact that it is completely integratable on a chip makes it all the more attractive.

Finally, in Chapter four, the problems of fabricating switched capacitor filters in MOS LSI technology have been studied. The switched capacitor filter consists of capacitors, switches (made of MOS transistors) and operational amplifier; all of them deviate from the ideal properties. The effects of these non-ideal characteristics were studied in this chapter. Computer simulations and experiments have validated that the diode leakage and stray capacitance effects are the two major factors affecting the frequency characteristics. One way of solving this problem has been discussed towards the end of the chapter.

5.2 Concluding Remarks

The present work has successfully demonstrated the suitability of realizing switched capacitor filters in MOS LSI technology. It has also put forward a systematic approach to the design of switched capacitor filters. The related theories regarding such design have been satisfactorily backed up by computer simulations; and have also been demonstrated by experiments. The author believes that using this approach, the knowledge of active-RC filter circuits

can be translated to switched capacitor circuits with relative ease. The approach is simple and easy to comprehend. Furthermore, the effect of sampling action on the sensitivity of the switched capacitor filters become readily evident from the equations obtained by this approach. Thus, fruitful information regarding the design of switched capacitor filters may be obtained from this approach.

Finally, the effects of various non-ideal characteristics, encountered in MOS LSI circuits, on the behaviour of switched capacitor filters have been studied. Specifically, it has been shown that diode leakage and parasitic capacitance associated with p-n junctions are the major sources of limitations on the circuit behaviour. The above-mentioned sources affect both the frequency response in the passband and the harmonic distortion of the filters. An alternative circuit has been proposed which can minimize these effects. This circuit is realizable in MOS LSI technology. It is believed that by suitable implementation, this circuit can overcome the above mentioned effects in MOS LSI switched capacitor filters.

5.3 Further Work to be done on Switched Capacitor Filters

This work has shown that it is possible to design a

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universal active filter in monolithic form, using the switched capacitor element. However, the design of such a filter has its own problems. It has been shown that the three modes of the switched capacitor element have advantages over one other, as well as disadvantages.

Thus, an intelligent choice of the modes has to be made while designing such universal active filter. Again, the recent papers on switched capacitor filters [2], [25] have shown that the operational amplifier takes a considerable area in such filters. Thus, where a high order of filter circuit is required, it would be interesting to study the effect of time multiplexing the operational amplifier over a number of integrating capacitors. Again, it has been demonstrated in this dissertation and other works [37] that the noise of the operational amplifier is a dominant factor in limiting the signal-to-noise ratio of the filter.

Therefore, designing low-noise operational amplifier is another area, where considerable work has to be done.

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APPENDIX I

MULTIPLE CLOCK (RATIONAL FRACTIONALLY RELATED) FIRST ORDER
LOWPASS SWITCHED CAPACITOR FILTER

The circuit is shown in Fig. I.1. The switched capacitors from the input side and that from the feedback side are operated at different sampling intervals T_1 and T_2 . In order that the system be linear and time-invariant, the two clocks must be related as a rational fraction; thus, let

$$\frac{T_1}{T_2} = \frac{p}{q} \quad (I.1)$$

where p and q are integers.

A hypothetical switch is added at the input to the amplifier, which is running at sampling interval T , the highest common factor between T_1 and T_2 , i.e.,

$$\frac{T_1}{p} = \frac{T_2}{q} = T \quad (I.2)$$

In other words, that is

$$T_1 = pT$$

and

Fig. I.1 First order lowpass parallel switched capacitor filter using multiple clocks (rational fractionally related). The sampling intervals T_1 and T_2 are shown below. The complementary switches in each switched capacitor are driven by non-overlapping clocks.

$$T_2 = qT \quad (I.3)$$

Another hypothetical switch is added at the output of Fig. I.1, whose sampling interval is the lowest common multiple of T_1 and T_2 , i.e., the output is valid only at the selected time slot pqT .

The strategy to follow to solve this problem is the same as in section 2.9. For the linear time-invariant (LTI) system, the sampling cycle repeats after pqT time. Hence, the amount of charge delivered to the negative end of the amplifier between the nT -th instant and $(n + pq)T$ -th instant is considered. Thus, the charge impulse from the input end between time nT and $(n + pq)T$ is:

$$q_I = C_i [v_{s,n} + v_{s,n+p} + \dots + v_{s,n+(q-1)p}] \quad (I.4)$$

and similarly, that through the feedback switched capacitor in the same time interval is

$$q_o = C_f [v'_{o,n} + v'_{o,n+q} + \dots + v'_{o,n+(p-1)q}] \quad (I.5)$$

Thus, the total charge input to the amplifier between nT -th and $(n+pq)T$ -th are given by

$$q_t = q_I + q_0 \quad (I.6)$$

Again, the response v'_0 is related to q_t by the following relation:

$$C[v'_{0,n+pq} - v'_{0,n}] = -q_t \quad (I.7)$$

Combining eqns. (I.4) through (I.7), gives

$$\begin{aligned} & C_i[v_{s,n} + v_{s,n+p} + \dots + v_{s,n+(q-1)p}] \\ & + C_f[v'_{0,n} + v'_{0,n+q} + \dots + v'_{0,n+(p-1)q}] \\ & = -C[v'_{0,n+pq} - v'_{0,n}] \end{aligned} \quad (I.8)$$

Taking the z-transform of both sides of eqn. (I.8)

gives

$$\begin{aligned} & C_i[1 + z^p + \dots + z^{(q-1)p}] v_s(z) \\ & + C_f[1 + z^q + \dots + z^{(p-1)q}] v'_0(z) = -C[z^{pq} - 1] v'_0(z) \end{aligned} \quad (I.9)$$

Eqn. (I.9) may be simplified as

$$C_i \frac{z^{pq-1}}{z^{p-1}} V_s(z) + C_f \frac{z^{pq-1}}{z^{q-1}} V'_o(z) = -C[z^{pq-1}] V'_o(z) \quad (I.10)$$

or

$$\frac{V'_o(z)}{V_s(z)} = - \frac{C_i \frac{z^{pq-1}}{z^{p-1}}}{C_f \frac{z^{pq-1}}{z^{q-1}} + C(z^{pq-1})} \quad (I.11)$$

Note that this expression is general in the sense that by assuming the feedback sampling interval, a multiple of the input sampling interval (i.e., $p = 1$), eqn. (2.26) is obtained. Again, if the two sampling intervals are identical (i.e., $p = q = 1$), then eqn. (2.18) is obtained.

APPENDIX II

VALIDATION OF THE USE OF BACKWARD AND FORWARD DIFFERENCE FORMULATION FOR SERIES AND PARALLEL SWITCHED CAPACITOR ELEMENTS

A general series switched capacitor circuit is shown in Fig. II.1. e_1 , e_2 and e_3 are voltage sources; ϕ_1 and ϕ_2 are non-overlapping two-phase clocks. During ϕ_1 , each switched capacitor element is initialized, while during ϕ_2 , the various nodes of the circuit reach their new equilibrium values for the n -th time slot. The difference equations may be written for this time slot:

$$\begin{aligned} \text{Node 1: } C_{R_1}(e_{1,n} - v_{1,n}) + C_{R_2}(v_{2,n} - v_{1,n}) + C_{R_3}(v_{2,n} - v_{1,n}) \\ + C_3(v_{2,n} - v_{1,n} - (v_{2,n-1} - v_{1,n-1})) = C_1(v_{2,n} - v_{1,n-1}) \end{aligned} \quad (\text{II.1})$$

$$\begin{aligned} \text{Node 2: } C_{R_4}(e_{3,n} - v_{2,n}) + C_3(v_{1,n} - v_{2,n} - (v_{1,n-1} - v_{2,n-1})) \\ = C_2(v_{2,n} - v_{2,n-1}) \end{aligned} \quad (\text{II.2})$$

Fig. II.1

Fig. II.2

Fig. II.1 Figure showing a series switched capacitor realization of an arbitrary R-C circuit.

Fig. II.2 Figure showing the above-mentioned circuit with parallel switched capacitor elements.

Taking z-transforms of the above equations give:

$$C_{R_1}(E_1(z) - V_1(z)) + C_{R_2}(E_2(z) - V_1(z)) + C_{R_3}(V_2(z) - V_1(z)) \\ + C_3(V_2(z) - V_1(z))(1 - z^{-1}) = C_1V_1(z)(1 - z^{-1}) \quad (II.3)$$

$$C_{R_1}(E_1(z) - V_2(z)) + C_3(V_1(z) - V_2(z))(1 - z^{-1}) \\ = C_2V_2(z)(1 - z^{-1}) \quad (II.4)$$

If the switched capacitor elements are replaced by the equivalent resistances using eqn. (2.1), then the following equations may be written in the s-domain:

$$\frac{C_{R_1}}{T}(E_1(s) - V_1(s)) + \frac{C_{R_2}}{T}(E_2(s) - V_1(s)) + \frac{C_{R_3}}{T}(V_2(s) - V_1(s)) \\ + sC_3(V_2(s) - V_1(s)) = sC_1V_1(s) \quad (II.5)$$

$$\frac{C_{R_4}}{T}(E_3(s) - V_2(s)) + sC_3(V_1(s) - V_2(s)) = sC_2V_2(s) \quad (II.6)$$

Comparing eqns. II.3 and II.5, and also II.4 and II.6, it is evident that equations in the z-domain may be written from those in the s-domain by using the following replacement:

$$s \leftrightarrow \frac{(1-z^{-1})}{T} \quad (II.7)$$

This is the equation for the backward difference formulation. This example demonstrates that if all nodes interact to reach equilibrium during one phase of the Clock for each sampling interval, the backward difference formulation may be used to obtain the transfer function from any active RC circuit to its switched capacitor analog. Note that if the clocks are interchanged for only one switched capacitor at a time, eqn. (II.7) does not remain valid. This is because it violates the condition required for the use of the above transformation for series switched capacitor filter; the condition was mentioned earlier in the paragraph.

A general parallel switched capacitor circuit, analogous to the series switched capacitor case, is shown in Fig. II.2. It is immediately recognized that the charge transfers to all the integrating nodes (nodes 1 and 2 in this example) do not take place at the same instant. In section III.2, this was considered a precondition for using the forward difference formulation in the parallel switched

capacitor case. Thus, it is observed that the forward difference formulation can not be used to obtain the transfer function for the above-mentioned sampled-data filter (Fig. II.2) from its continuous equivalence where two or more floating nodes interact with each other.

APPENDIX III

HARMONIC DISTORTION ANALYSIS OF THE NOTCH FILTER

It was stated in section 4.5 that the single most dominant source of non-linearity is the diffusion capacitance at the input to the op amp, C_D , as shown in Fig. 4.24. Harmonic distortion of this system, considering this as the only non-linearity present in the system was done. This is illustrated in this section.

The difference equations describing this system were stated in section 4.5:

$$C_{R_1}(v_{1,n} - v_{1,n-1}) + C_{R_2}(v_{3,n} - v_{1,n}) =$$

$$C_3[(v_{1,n} - v_{1,n-1}) - K(v_{3,n} - v_{3,n-1})] \quad (3.66)$$

$$C_1[(v_{1,n} - v_{1,n-1}) - (v_{2,n} - v_{2,n-1})] +$$

$$C_2[(v_{3,n} - v_{3,n-1}) - (v_{2,n} - v_{2,n-1})] =$$

$$C_{R_3}(v_{2,n} - v_{2,n-1}) \quad (3.67)$$

4 4

OF / DE

and

$$C_{R_2}(v_{1,n} - v_{3,n}) + C_2 [(v_{2,n} - v_{2,n-1}) - (v_{3,n} - v_{3,n-1})]$$

$$= C_{D0} \cdot 2V_t \left[\sqrt{1 + \frac{v_{3,n}}{V_t}} - \sqrt{1 + \frac{v_{3,n-1}}{V_t}} \right]$$

where

V_t is given by eqn. (4.11)

Reorganizing the above equations,

$$(C_{R_1} + C_{R_2} + C_3)v_{1,n} - (C_{R_2} + KC_3)v_{3,n} = C_{R_1}v_{1,n} + C_3v_{1,n-1} - KC_3v_{3,n-1} \quad (\text{III.1})$$

$$(C_1 + C_2 + C_{R_3})v_{2,n} - (KC_{R_3} + C_2)v_{3,n} = C_1v_{1,n} - C_1v_{1,n-1} + C_1v_{2,n-1}$$

$$- C_2v_{3,n-1} + C_2v_{2,n-1} \quad (\text{III.2})$$

and

$$-C_{R_2}v_{1,n} - C_2v_{2,n} + (C_{R_2} + C_2)v_{3,n} = -C_2v_{2,n-1} + C_2v_{3,n-1}$$

$$-2C_{D0}V_t \left[\sqrt{1 + \frac{v_{3,n}}{V_t}} - \sqrt{1 + \frac{v_{3,n-1}}{V_t}} \right] \quad (\text{III.3})$$

This may be written in matrix form as follows:

$$\begin{bmatrix} C_{R_1} + C_{R_2} + C_3 & 0 & -(C_{R_2} + KC_3) \\ 0 & C_1 + C_2 + C_{R_3} & -(C_2 + KC_{R_3}) \\ -C_{R_2} & -C_2 & C_2 + C_{R_2} \end{bmatrix} \begin{bmatrix} v_{1,n} \\ v_{2,n} \\ v_{3,n} \end{bmatrix} =$$

$$\begin{bmatrix} C_{R_1} & 0 & C_3 & 0 & -KC_3 & 0 \\ C_1 & -C_1 & 0 & C_1 + C_2 & -C_2 & 0 \\ 0 & 0 & 0 & -C_2 & C_2 & -2C_{D0}V_t \end{bmatrix} \begin{bmatrix} v_{i,n} \\ v_{i,n-1} \\ v_{1,n-1} \\ v_{2,n-1} \\ v_{3,n-1} \end{bmatrix}$$

$$\sqrt{1 + \frac{v_{3,n}}{V_t}} - \sqrt{1 + \frac{v_{3,n-1}}{V_t}}$$

Eqn. (III.4) is a non-linear matrix equation. However, by mathematical manipulation, the unknown vector $X_n = [v_{1,n}, v_{2,n}, v_{3,n}]^T$ is expressed in terms of the known vector $Y_n = [v_{1,n}, v_{2,n-1}, v_{3,n-1}]^T$ and Z_n which corresponds to the only non-linear function in eqn. III.4. Thus,

$$AX_n = [B; D] \begin{bmatrix} Y_n \\ Z_n \end{bmatrix} \quad (\text{III.5})$$

where

A denotes the square matrix in the left-hand side of eqn. (III.4)

B denotes the partitioned matrix in the right-hand side of eqn. (III.4)

D denotes the vector, $[0, 0, -2C_{D0}v_t]^T$

and

$$Z_n = \sqrt{1 + \frac{v_{3,n}}{v_t}} - \sqrt{1 + \frac{v_{3,n-1}}{v_t}} \quad (\text{III.6})$$

Eqn. (III.5) may be solved as follows:

$$X_n = A^{-1}BY_n + A^{-1}DZ_n \quad (\text{III.7})$$

Noting that Z_n is a non-linear function of the unknown parameter $v_{3,n}$, it is necessary to solve eqn. (III.7) iteratively.

until sufficient convergence is achieved. Once the set of v_3 corresponding to a known sinusoidal input is obtained, discrete fourier transform (DFT) on the above-mentioned set may be performed to obtain the harmonic content of the notch filter at various frequencies. The result of the simulation is displayed in Fig. III.1. The figure shows that the harmonic distortion increases with higher signal voltage for a specific sampling frequency and substrate voltage. Simulation has also indicated that the harmonic distortion increases for lower sampling frequency and lower substrate voltage for any given signal frequency. These results have been justified from physical considerations in section 4.5.

END

0	3	H	0	9	H	8	2

FIN