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NOVEL TECHNOLOGICAL AND MODELLING APPROACHES
FOR VLSI DEVICE STRUCTURES

by

© Abdalla Aly Naem

A thesis submitted to the Faculty of Graduate
Studies and Research in partial
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for the degree of

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ABSTRACT

The requirement for very large scale integration of MOSFETs poses challenge in both device technology and modelling. A novel 3-D MOSFET structure that will allow vertical integration of ICs is proposed. This approach will allow the fabrication of stacked devices with aspect ratio (W/L) equivalent to that of a planar device, utilizing only half the active surface area required by planar techniques. The basis of the technological and modelling requirements of such a device is established.

A novel laser processing technique is described, in which a silicon nitride anti-reflection coating is used to achieve selective recrystallization and preferential etching of small designated areas. The technique also allows simultaneous laser activation of the source/drain implants and recrystallization of the gate polysilicon, so that high quality devices can be achieved with shallow junctions.

Subsequently, the compatibility of laser processing with IC technology is examined and verified. The electrical and physical effects of laser recrystallization of polysilicon gates on underlying gate oxide, the most process sensitive device element, is critically investigated. The characteristics of laser processed contacts, shallow junctions, and small geometry MOSFETs are also studied. It is concluded that laser techniques have a strong potential for application to VLSI devices with excellent performance, and without any deleterious effects, as long as it is carried out at a laser power level within the useful laser "processing window".

As a prerequisite for modelling 3-D MOSFETs, which will tend to take the form of narrow devices with multichannels stacked one on top of another, a novel dc model for narrow channel devices is derived and

experimentally verified, under different operating conditions. The model is applicable to both narrow/long or wide/long MOSFETs and is characterized by: 2-D evaluation of device charges, "effective gate voltage", linear variation of the surface potential at the width sides of the channel, and an "effective channel width". The sensitivity of the device performance and the effective channel width to substrate bias, a critical mechanism in narrow channel devices, is well modelled. The model can be a valuable tool, with appropriate modifications, in characterizing and understanding the proposed 3-D MOSFETs. The critical design implications and the modelling considerations relevant to the analysis of the upper device of the proposed 3-D MOSFET structure are also identified.

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LIST OF ABBREVIATIONS

AR	Anti-Reflective
CAD	Computer-Aided-Design
CPU	Central Processing Unit
FA	Furnace Annealing
GCA	Gradual Channel Approximation
HiPOx	High-Pressure Oxide
IC	Integrated Circuit
LA	Laser Annealing
LOCOS	Local Oxidation Of Silicon
LPCVD	Low-Pressure Chemical Vapour Deposition
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NCEs	Narrow Channel Effects
NCDs	Narrow Channel Devices
Poly	Polysilicon
PSG	Phosphosilicate Glass
SCDs	Short Channel Devices
SCEs	Short Channel Effects
Si	Silicon
SLA	Selective Laser Annealing
SMOS.	Stacked MOS
SOI	Silicon On Insulator
SOS	Silicon On Sapphire
VLSI	Very Large Scale Integration
1-D	One Dimensional
2-D	Two Dimensional
3-D	Three Dimensional

LIST OF SYMBOLS

A	Effective Channel Width Fitting Parameter
C_0	Gate Capacitance Per Unit Area
D	Diffusion Coefficient
E_n	Electrical Field in x Direction
g_m	Transconductance
g_d	Drain Conductance
I_{DS}	Drain Current
k	Boltzmann's Constant
L	Channel Length
L_D	Diffusion Length
L_g	Gate Length
N_A	Impurity Design of a Uniformly Doped p-Type Substrate
n_1	Refractive Index of Air
n_2	Refractive Index of Dielectric Film
n_3	Refractive Index of Silicon
P	Incident Laser Power
q	Electron Charge
Q_m	Absolute Value of Mobile Charge Density
Q_D	Absolute Value of Depletion Charge Density
Q_{ss}	Fixed Oxide-Interface Charge Density
Q_G	Charge Density on the Gate
R	Reflectivity of Laser Beam
R_c	Contact Resistance

LIST OF SYMBOLS (CONT'D)

T	Temperature
T_o	Wafer Back Surface Temperature
V_{DS}	Externally Applied Drain to Source Potential
V_{FB}	Flatband Voltage
V_{gs}	Gate Potential w.r.t. Flatband
V_{GS}	Externally Applied Gate to Source Bias
V_G	Externally Applied Gate Bias w.r.t. Substrate
V_o	Voltage Drop Across the Gate Oxide
V_{BS}	Applied Substrate Bias
V_T	Threshold Voltage
w	Laser Beam Radius
W	Nominal Channel Width
W'	Effective Channel Width
W_g	Nominal Gate Width
x_D	Depletion Layer Width
x_F	Field Oxide Thickness
x_i	Gate Oxide Thickness
x_J	Junction Depth
x_o	Oxide Thickness
β	A Correction Factor for Laser Scanning Speed
ϵ	Permittivity of Free Space
ϵ_o	Dielectric Constant of Oxide
ϵ_{ox}	Permittivity of Gate Oxide
ϵ_{si}	Permittivity of Silicon
λ	Fringing Factor
μ_n	Surface Electron Mobility
μ_o	Low Field Surface Electron Mobility

LIST OF SYMBOLS (CONT'D)

ϕ_F	Fermi Potential
ϕ_{MS}	Metal Semiconductor Work Function Difference
ϕ_{fn}	Quasi Fermi Potential of Electrons
ϕ_{fp}	Quasi Fermi Potential of Holes
ψ_s	Surface Potential
δ	Fitting Parameter for the Non-uniform Depletion Layer Width
χ	Fitting Parameter for the Uniform Depletion Layer Width

CHAPTER 1

INTRODUCTION

The packing density of MOS integrated circuits has increased dramatically in recent years due to the advances in lithographic and design techniques. Accordingly, Metal Oxide Silicon Field Effect Transistors (MOSFETs) are continuously decreasing in size to meet the requirements for Very Large Scale Integrated (VLSI) circuits of high packing density and fast switching speed. Usually this is done by reducing device channel length and/or width [1.1-1.3]. A device scaling approach [1.4] has been proposed whereby the lateral and vertical dimensions and bias voltages are scaled down in proportion, while the substrate doping is scaled up by the same ratio. However, there are physical and technological limitations to that approach [1.5, 1.6]. Most important are: short and/or narrow channel effects, polysilicon gate edge nonuniformity, gate resistivity, the formation and annealing of shallow junctions, the properties of metal/semiconductor contacts to shallow junctions, and oxide/silicon interfaces. The direct scaling approach does not apply to these effects and properties.

When the device channel is made short and/or narrow the gate edge nonuniformity and undercut becomes comparable to the actual dimensions [1.7]. This results in poor reproducibility and controllability of the threshold voltage, which is the most important electrical device parameter. Also, the shallow junctions required by the scaling approach lead to high gate resistivity, since the junction formation and a polysilicon gate are, conventionally, doped simultaneously in one doping step [1.7]. This problem stems from the requirement that, in forming shallow

junctions, extensive doping must be avoided. But, to achieve low gate resistivity, extensive doping is required. Such contradictory requirements must be fulfilled simultaneously if the scaling rules are to be applied.

A way around the above difficulties is to introduce novel device structures that allow VLSI integration, without having to apply the scaling rules. This is possible through vertical integration i.e., any IC technology that would yield more than one plane of active devices, and should be capable of formation of low gate resistivity and shallow junctions simultaneously. Such an approach entails new technological and modelling techniques. Basic to a successful technology is the capability of achieving accurate patterning of polysilicon gates with minimum undercut. Laser annealing (LA) is an emerging technology which offers great promise to achieve these contradictory requirements and to be most useful in the context of vertical integration. It is particularly attractive in light of the fact that the current technological advances are focused towards lower processing temperature techniques to allow the fabrication of multilayer MOS devices with shallow junctions.

In addition, the need for a good low temperature oxide has become essential for small size devices that include multilayers of gate oxides, e.g. 3-D stacked devices [1.8, 1.9] for which the upper gate oxides must be grown in the presence of junctions formed in the starting substrate. High temperature oxidation, however, causes degradation of the electrical characteristics of such a device structure. Most serious is the severe redistribution of dopants previously implanted in underlying layers. Since High Pressure low temperature Oxide (HiPOx) [1.10] is an advantageous means to overcome this problem, the potentiality of using HiPOx as a gate dielectric for these devices needs to be examined. Furthermore,

the application of LA in device fabrication must not introduce any laser-induced damage into the underlying gate oxides or Si/SiO₂ interfaces, since LA of the polysilicon films must take place in the presence of underlying gate oxides.

Most critical is that laser processing must be compatible with IC technology when applied to a complete device system. Therefore the impact of this process technique on a device performance as a whole, while preferably positive, must at least not be negative, for the viability of this process as a candidate for VLSI processing techniques. The contact, shallow junction, key device parameters, and the overall device performances must not be degraded by laser processing, particularly when this process is applied to VLSI devices ($\sim 1 \mu\text{m}^2$ size). These concerns are particularly strong for devices fabricated in the starting substrate, since they are inevitably subjected to laser beams in the case of vertically integrated 3-D devices. In most cases, these devices are of good quality to start with. Moreover, they are the most sensitive to new process techniques in structures having devices stacked one on top of another. A detailed investigation of this problem is crucial for successful implementation of vertically integrated IC technology.

The mechanisms behind the nonscaling properties of Short Channel Effects (SCEs) are well known [1.11], but the Narrow Channel Effects (NCEs) and their nonscaling behavior are not well understood yet. Consequently, the departure of the behavior of Narrow Channel Devices (NCDs) from the conventional theory and direct scaling must be studied, if a better understanding of their performance is to be gained. Such a study is essential as a guiding principle in proposing a model that is capable of predicting their characteristics, while it is sufficiently simple for

use in circuit design. In addition, modelling of conventional NCDs serves as a means for understanding and characterizing the performance of NCDs of multichannels (e.g., 3-D devices), where the basic NCD physical mechanisms do exist. In view of the different physical nature of the "upper devices" in stacked device structure, compared with the device utilizing the starting substrate, the modelling considerations for these devices need to be examined and compared with those for the substrate device.

1.1 Thesis Objectives

In view of the preceding discussion, the main objectives of this thesis are the following:

- (i) Introduction of suitable vertically integrated MOSFET device structures (stacked 3-D devices) more amenable to integration, which allow reduction of device size and hence higher packing density, and definition of the process required to fabricate these devices. Since realizing such devices will require evolution of novel technological and modelling approaches, attention will be focused on the details of the key processing and modelling techniques that are basic to them.
- (ii) Examination of new technological approaches, suitable for the fabrication of 3-D devices, that enable precise definition of polysilicon gates (or resistors) with minimum undercut and low resistivity. Such techniques should also allow the formation of shallow junctions, a requirement essential for VLSI devices. The

laser processing technique is a potential approach to achieve these requirements simultaneously, because the heat generated by the laser is localized, while the whole substrate can be kept at ambient temperature. Such a low temperature technique is particularly important in the fabrication of 3-D structures.

- (iii) Study of the effects of cw laser processing on the properties of gate oxide (standard and HfPO_x), the most critical device element. This is to verify whether or not laser recrystallization of the polysilicon gates, inevitable for 3-D devices, causes any deleterious effects on underlying oxide or the Si/SiO_2 interfaces.
- (iv) Investigation of the impact of laser processing on the overall performance of small size (single layer) devices, fabricated in the starting substrate. These devices are most sensitive to any new processing technique, and their behavior is a critical indicator of the quality of the technique adapted in realizing them.
- (v) Formulation of a model for NCDs, which is economically feasible, in terms of computation expenses and computer memory area, and mathematically sufficiently simple for implementation in circuit design. Modelling of these devices can be in particular a useful means for understanding and characterizing the performance of novel multichannel narrow devices (e.g. 3-D devices), which are basically narrow devices but with several layers to make up the required width (only two layer devices will be considered in this thesis).

- (vi) Investigation of the overall modelling considerations of the stacked device structure.

1.2 Outline of the Thesis

This thesis is organized into eight chapters.

In Chapter 1, the objectives of the research program and the outline of the thesis are stated.

In Chapter 2, a novel vertically integrated 3-D MOS transistor structure is proposed. The success of these devices depends on novel technological approaches, introduced in subsequent chapters, which are basic to them. Such devices lead to area saving without having to apply the scaling rules, with further savings resulting from subsequent scaling. Moreover, the proposed technology for these devices allows easy formation of shallow junctions.

In Chapter 3, a novel process is described, by which the polysilicon films can be recrystallized and patterned accurately with minimum undercut. This technique is based on Selective Laser Annealing (SLA) and preferential etching of designated polysilicon islands (gates). Compared with standard processes, undercut has been reduced by a factor of two and edge nonuniformity reduced by a factor of 5, without pitting of the polysilicon (a problem usually encountered in laser annealing of large polysilicon areas). The principle of the technique and sample preparation are discussed. Results on selective laser recrystallization of polysilicon films (at different laser powers and speeds) and their etching characteristics are presented and analyzed. Potential applications of the technique in VLSI devices in general, and 3-D devices in particular, are also discussed.

In Chapter 4, investigation of the effects of laser recrystallization of polysilicon gates on the electrical properties of underlying gate oxide (standard and HfPO_x) has been carried out. This study is necessary for determining a useful laser "processing window" that is to be used in the fabrication of SOI devices, in general, and multilayer (3-D) devices, in particular. In this chapter, the preparation of the samples, test structures used and characterization techniques are described and the results of that study are presented and discussed.

In Chapter 5, the compatibility of laser processing with IC technology is examined in detail when applied to an integrated device system and the overall device performance of laser processed devices is evaluated and related to the processing techniques used. MOSFET structures of VLSI size are used in this study, so that any possible undesirable electrical effects are manifested in the behavior of such devices.

In Chapter 6, as a prerequisite for modelling 3-D MOSFETs, the mechanisms associated with conventional NCDs are discussed. A novel closed form model for narrow channel MOSFETs, which accounts for the NCEs, is introduced. Expressions based on 2-D evaluation of the gate, depletion, and inversion charges are derived as the basis for models for the threshold voltage and drain current voltage characteristics. These models have been verified experimentally, for a wide range of device dimensions and bias conditions, with good matching between simulation and actual device data.

In Chapter 7 the design and modelling considerations essential to the "upper device" in the proposed stacked transistors are investigated

The application of the narrow channel model to these devices is also discussed.

In Chapter 8 conclusions, original research contributions and recommendations for future research are set out.

CHAPTER 2

A PROPOSAL FOR A NOVEL 3-D MOS TRANSISTOR

2.1 Introduction

Increased integration density for VLSI is essentially achieved through scaling down device dimensions [2.1]. However, there are a number of limitations imposed on that approach by device technology and physics [2.2-2.4]. Recently a new approach has emerged to put more devices on a constant chip area by stacking them one on top of another [2.5-2.7]. Many advantages of this approach, including denser circuitry, simplified processing, higher speed, reduced power consumption and freedom from CMOS latchup have stimulated intensive research on 3-D integration. However, this approach has not yet been applied to discrete MOS transistors.

The first stacked CMOS inverter, sharing a common gate for both the n- and p-channel transistors, was reported by Gibbons et al. [2.5]. The p-channel transistor was made in the bulk silicon while the n-channel transistor was made in a laser recrystallized polysilicon film on top. A similar stacked CMOS inverter, based on top-down rather than bottom-up technology, was then proposed by Goeloe et al. [2.6]. Both inverters suffer from low n-channel mobility and high parasitic capacitance, since the source and drain of the top transistor (n-channel) are entirely present on the gate. However, the most serious disadvantage is the incompatibility with existing technologies.

A stacked CMOS inverter (shown in Figure 2.1) has been demonstrated by Colinge et al. [2.7], in which the top and bottom devices have a

common drain; that is, the top polysilicon is in contact with the bulk silicon in the drain region. This contact can not be used to induce the substrate silicon crystal orientation in the upper polysilicon layer (lateral seeding) during laser recrystallization of the top polysilicon film. Since, if the seeding was performed and extended far enough from the contact hole to reach the upper transistor channel region, the upper channel would have been contaminated with n-type species from the junction previously formed in the substrate, and thereby rendering the device useless.

A common disadvantage in the three stacked CMOS inverters mentioned above is that the top gate oxide was grown on unannealed polysilicon, resulting in low quality top gate oxide [2.8], and poor contact between the top and bottom junctions which have opposite doping. The most recent stacked structure has been introduced by Gibbons et al. [2.9], in which each surface of a laser recrystallized SOI polysilicon (first polysilicon level) layer acts as a separate active channel region with its own gate (one in the bulk silicon, one in a second polysilicon level); a top view and cross sections of this device are shown in Figure 2.2. In this arrangement, the current flow in the two channels is in perpendicular directions, hence the name "cross-MOS" or XMOS. This is a somewhat backward step from the structure proposed by Colinge et al. [2.7], because it has serious technological and physical limitations. There is no contact between the polysilicon film and the bulk silicon, thus, the seeding technique required to achieve high quality recrystallized film can not be applied, resulting in low quality devices as can be concluded from the device performance [2.9].

Figure 2.1 A cross sectional view of the stacked CMOS inverter in
Ref. [2.7]

Figure 2.2 XMOS (cross-MOS) device structure.

The main objectives of this chapter are to introduce a novel stacked MOS (SMOS) transistor structure more amenable to integration complexity without having to apply the scaling rules, with further area saving resulting from subsequent scaling, and to define the process required to fabricate these devices. Furthermore, the proposed SMOS structure should be free from the limitations that all the existing structures suffer from. A description of the SMOS devices and their process sequence is given in the subsequent sections.

2.2 Description of the Proposed Transistor

The new device structure is a discrete MOSFET, in which the width of a standard MOS transistor is effectively divided into two (or more) regions that are stacked one on top of another, to save active device area. A two layer device structure, with a single common gate, is used as a particular example in this thesis. In principle, the stacking could continue to a third and higher levels using the same technique that is used in realizing the second layer of devices. A plan view and a cross section of the proposed device are illustrated in Figures 2.3 and 2.4, respectively, where a two layer structure is presented as a particular example. The gate of the SMOS transistor is narrow but several layers in the vertical direction make up the required width. Such a device structure is of special interest when its gate is made short as well as narrow, since the overall device performance is then expected to be improved, as a result of narrowing the channel. This is because the short channel and narrow channel effects counteract one another [2.10], resulting in improved overall device performance.

Figure 2.3 A Plan view of the proposed SMOS transistor.

I, II, III, IV, V, refer to field, poly-I, seeding windows, Poly-II and contact levels respectively.

Figure 2.4 A cross-section of the proposed SMOS transistor (along A A' in Figure 2.3).

As can be seen in Figures 2.3 and 2.4, the top source and drain polysilicon regions (heavily doped and laser annealed) are extended to the bonding pads, replacing aluminum interconnects. This eliminates the requirement for source/drain contact windows. This freedom from contact windows has three advantages: (1) it eliminates the metal/semiconductor interface problems associated with small size contact windows, particularly if the junctions are made shallow; (2) it further reduces the chip area occupied by the active device region; (3) it provides design flexibility and eliminates uncertainties and errors associated with the photolithographic steps. Elimination of the source/drain contact windows in this way can also be applied to the existing stacked CMOS inverters.

The technology required to make the proposed SMOS transistor is compatible with existing technologies and involves only the application of laser processing in recrystallizing the top polysilicon film and the common gate polysilicon as additional processes. Seven masks are required to make this device, as described in the next section.

2.3 Device Fabrication Sequence

The choice of the technological parameters is, at this point immaterial. In a real application, however, it would be dictated by the quality of the devices and by the specific device application. The main fabrication steps required to realize the proposed SMOS device structure, whose cross section is shown in Figure 2.4, are the following:

- (1) Field implant, field oxide growth, device well, threshold adjust and first gate oxide are carried out with conventional LOCOS technology, using mask level I (steps a & b in Figure 2.5).

Figure 2.5 The SMOS transistor's main fabrication steps.

Figure 2.5 (Cont'd).
The SMOS transistor's main fabrication steps.

- (ii) The common gate polysilicon (Poly-I) is deposited, followed by deposition and patterning of a nitride layer, using mask level II, (step c in Figure 2.5).
- (iii) Poly-I is then recrystallized, with the nitride on, into large grains, and patterned by preferential etching employing a novel Selective Laser Annealing (SLA) technique [2.11] described in the next chapter. The nitride layer acts as an anti-reflective cap during laser processing.
- (iv) The nitride cap is etched off and Poly-I is heavily implanted (step d in Figure 2.5).
- (v) The upper gate-oxide is thermally grown, being formed on large grained smooth polysilicon (step e in Figure 2.5).
- (vi) An opening is made through the gate oxide down to the bulk silicon to provide buried contact holes to allow contacting between sources/drains of the top and bottom layers, and to serve as seeding windows. This is performed using mask level III (step f in Figure 2.5).
- (vii) A top P-type polysilicon film (Poly-II) and an anti-reflective nitride cap are deposited, followed by patterning of the nitride cap, using mask level IV, (step g in Figure 2.5).
- (viii) A second laser processing step is carried out to recrystallize Poly-II in the source, drain and gate regions, and to form a

single crystal silicon film. Under these conditions, the top gate region will be several degrees hotter than the source and drain areas and will cool and recrystallize after the source and drain regions which act as seeds. Without seeding the polysilicon film is recrystallized into large grains as a result of LA; with seeding the situation is much better, the film can be formed into a single crystal.

- (ix) Pattern Poly-II selectively, utilizing a preferential etching technique, described in Chapter 3.
- (x) Remove the nitride layer and use a photoresist (P.R.) as an implantation mask over the gate area using mask level II and then perform the top device source and drain implantation conventionally (step h in Figure 2.5). This implantation step should also allow the impurities to reach the bulk silicon, so that the bottom device source and drain junctions are formed in the same step. However, alignment of this mask is a critical step (not self-aligned) and care must be exercised. This implantation step will also result in junction profiles similar to those in lightly doped (L_{DD}) structures as shown in Figure 2.4.
- (xi) After removing the photoresist, a standard phosphosilicate glass (PSG) layer is then deposited and contact windows to the gate, top substrate (Poly-II) and source/drain interconnects are conventionally opened using mask V. The substrate contact can be included or omitted as desired (see discussion of Chapter 7). Such a contact can be made on the top of Poly. II, as shown in Figure 2.4, or at the width edge.
- (xii) Standard aluminum and pyrox deposition and patterning of bonding pads are carried out conventionally using mask levels VI and VII respectively, to complete the device fabrication sequence.

Laser recrystallization of Poly-I (common gate) not only reduces its resistivity by half but also results in a smooth surface [2.11], and thereby a high quality top gate oxide. This quality oxide should eliminate possible bridging between the gate and the top active polysilicon substrate, and improve the top gate oxide breakdown voltage and leakage current, thereby resulting in a high quality top device and a good field.

Laser recrystallization of the Poly-II film must take place to form the upper substrate into a single crystal, through laser induced lateral seeding from the lower substrate [2.12]. So, the seeding takes place from the bottom silicon substrate to the polysilicon film through two openings connecting the two layers at the source/drain regions. When the laser beam passes over this opening, it causes the melt pool to extend down through the polysilicon film and into the bulk silicon. As the beam is passed over the seed opening, the first region to cool and resolidify is the single crystal substrate. The recrystallization front now moves up from the substrate and follows the trailing edge of the melt pool across the surface of the oxide, resulting in a continuous film of single crystal silicon. High quality devices can now be fabricated in the top active substrate (Poly-II).

Since well ordered recrystallization can only proceed for a limited lateral distance ($\sim 50 \mu\text{m}$) from the seed window [2.13], placement of the seeding window near the active top device channel is, therefore, crucial. The buried contacts, mask level III in Figure 2.3, are well suited for that.

An attractive feature, unique to the present structure, is that the junctions of both the top and bottom devices are formed, after all the high temperature steps are performed, using one implantation step. As a result, shallow junctions in the bulk silicon can easily be achieved, without having to worry about contact problems. According to other 3-D fabrication sequences [2.5-2.7], the bottom device is completed before Poly-II is deposited and recrystallized. Laser recrystallization of Poly-II involves a deep melt through the seeding window and down into the heavily doped junctions of the bottom device, in order to achieve the desired seeding effect. Using a typical laser scanning speed (50 cm/s) and beam size (50 μm), the melt dwell time in the junction area is $t = 100 \mu\text{s}$, giving a diffusion length $L = 2 (Dt)^{1/2} = 4.4 \mu\text{m}$ (where the diffusion constant D is $5.1 \times 10^{-4} \text{ cm}^2/\text{s}$). This will cause a significant redistribution of the implants in the bulk silicon. Moreover, recrystallization of Poly-II, under such conditions, will contaminate the upper device channel with the impurities diffusing from the junctions in the bulk, causing a significant threshold voltage shift to a large value as to render the upper device useless. Therefore, forming all the junctions after recrystallization of Poly-II, which is possible by the present fabrication scheme, not only simplifies the process and results in shallow junctions, but also offer an easy solution to this problem.

The same laser annealing of Poly-II also reduces the resistivity of the polysilicon interconnects (replacing metal) and eliminates problems at the polysilicon/bulk silicon interface. Therefore, good contacts can be achieved at the common drain and source interfaces, so that the incorporation of shallow junctions becomes feasible.

The process described above is applicable also to SOI devices and vertically integrated CMOS inverters, with three modifications in the case of the CMOS process. First, the CMOS top and bottom devices can only have common drains; the source regions must be isolated. Secondly, the devices must have opposite type of carriers; thirdly, the formation of the top and bottom device junctions will require two implantation steps and thereby an additional implantation mask.

The advantages of the proposed MOSFET structure can be summarized as follows:

- a. Significant saving in chip area, depending on the number of the stacked layers.
- b. Self-aligned source/drain contact windows for both the top and bottom layers, eliminating alignment and registration errors associated with this step.
- c. Technology required is compatible with standard NMOS technologies, except for laser processing.
- d. Easy formation of shallow junctions, without contact problems, since the doping of the junctions, for the top and bottom devices, is carried out (in one step) after all the high temperature steps are completed.
- e. Possibility of improvement in device performance if the device active channel area is made short as well as narrow, because of the beneficial interaction between narrow channel and short channel effects.

- f. Expected improvement in switching speed due to reduction in the parasitic capacitances associated with the source/drain junctions.

Of course in making the proposed device, research will be needed in the areas of materials processing and 3-D modelling. In the processing area in particular, low temperature processes are the key, for oxidation, dopant activation, and most of all, for polysilicon film recrystallization.

A major consideration that must be taken into account with laser recrystallization of 3-D structures is that the laser beam is incident on regions with widely varying thermal properties. Therefore, laser power levels that may melt one region of a structure may be insufficient to melt another region where melting is required, while raising the temperature of a third region to a destructively high value. This problem is dealt with in the next chapter, where a novel selective laser recrystallization technique has been developed.

The most critical technological steps required for making these devices, and their influence on the MOS properties of the structure and on the overall MOSFET performance (particularly those made in the bulk silicon) are investigated and presented in Chapters 3, 4 and 5. Specific topics treated are achieving laser recrystallization of selected polysilicon areas, preferential etching with minimum undercut, and the effects of laser processing on underlying gate oxides and overall device behavior. The actual realization and characterization of the proposed SMOS transistors are, however, long term objectives and beyond the scope of this thesis.

2.4 Conclusions

A novel vertically integrated Stacked MOS transistor structure suitable for VLSI application is proposed. Such a device structure will enable the fabrication of MOS transistors, with W/L equivalent to that of a planar device, using only half the active chip area, without having to apply the scaling principles, with further area saving resulting from subsequent scaling. In this way the limitations imposed by scaling on device technology and performance are avoided. Other advantages of this approach include, elimination of source/drain contact windows, an increase in packing density, improved device performance, easy incorporation of shallow junctions and higher speed. The technology required for the fabrication of this device is compatible with existing IC technologies, except for laser processing. The process required for realizing these devices has been defined and it is also applicable, with some modifications, to vertically integrated SOI and CMOS devices.

CHAPTER 3

A NOVEL LASER ANNEALING TECHNIQUE FOR DEVICE PROCESSING

3.1 Introduction

The realization of VLSI vertically (3-D) integrated devices, introduced in the previous chapter, is contingent upon improvement in existing process techniques, and on the introduction of novel process technologies. In particular, a novel polysilicon film recrystallization technique that is capable of fabricating small geometry devices, and a low temperature dopant activation process are required. Laser Annealing (LA) is a technology which has the potential to impact both of these areas.

Small geometry devices suffer from the nonscaling nature of the edge bias tolerance, linewidth uncertainty and undercut, if the device channel is made short and/or narrow. These problems result in poor controllability of the threshold voltage [3.1], the most important electrical device parameter, and poor yield as well, due to nonuniformity of the polysilicon gate. Therefore, accurate definition of the polysilicon gate is extremely important if a tight control on device parameters is to be retained.

As well, shallow junctions required by the scaling rules result in high gate resistivity, since the junctions and the polysilicon gate are doped simultaneously in one diffusion step [3.2]. This problem stems from the requirement that extensive impurity diffusion must be avoided in forming shallow junctions, and therefore insufficient dopant is introduced to the polysilicon gate to reduce its resistance as required

by high speed devices. Such contradictory requirements must be fulfilled simultaneously if the scaling rules are to be applied, or if any shrinking of dimensions occurs, scaled or not.

The objective of this chapter is to develop a novel polysilicon film recrystallization technology that achieves accurate definition of polysilicon gates with minimum undercut, without causing deleterious effects to other chip areas where recrystallization is undesirable. Such a technology must be capable also of the formation of shallow junctions and must achieve low gate resistivity simultaneously, as required for VLSI 3-D devices.

In the next section, a technique capable of achieving these requirements is introduced; it is based on selective laser recrystallization of polysilicon MOS gates.

3.2 Selective Laser Recrystallization For Device Processing

The application of the proposed laser recrystallization technique is aimed both at device structures that are presently limited by conventional processing techniques [3.3-3.5], and at stacked structures [3.6-3.8]. The technique is particularly useful in the fabrication of the 3-D MOSFETs introduced in Chapter 2. Device structures relevant to such applications are usually complex. During the processing of such structures, the laser beam is incident on areas with widely varying optical and thermal properties. This means laser irradiation of the integrated circuit structure, at any step of the fabrication sequence, may result in laser irradiation of areas where damage can easily be introduced if high laser energy densities are used. The attainable temperature is therefore

strongly dependent upon the sample structure; in particular, conditions that will melt one region of a structure may not melt another region where melting is desirable, while raising the temperature of a third region to a destructively high value. Therefore, laser processing must accomplish the desired material transformation in the regions of interest without causing deleterious effects on other regions also inevitably exposed.

Here a technique is introduced for achieving Selective Laser Annealing (SLA) of devices, so that only designated regions of polysilicon are melted and recrystallized. Results on the effects of SLA on the grain morphology, etching characteristics, sheet resistivity and uniformity of polysilicon gates are presented and analyzed. A laser processing model [3.9] has been used to aid in the understanding of the physical process involved and predict optimum LA conditions.

3.2.1 Approach

There is little independent control over the thermal properties of a particular device structure, but through the use of a dielectric Anti-Reflection (AR) coating, the laser power absorbed can be spatially controlled [3.10,3.11]. In this section, the optimum thickness and refractive index of an AR coating suitable for SLA applications are defined.

Figure 3.1 illustrates the propagation of a laser beam of wavelength λ through a dielectric film (e.g., SiO_2 or Si_3N_4) of thickness d , deposited on a SOI polysilicon film. In this figure, n_1 , n_2 and $\hat{n}_3$ are the refractive indices of the air, the dielectric film and the polysilicon, respectively, while $\hat{n}_3 (= n_3 + ik_3)$ is complex because of the non-zero optical absorption of polysilicon.

Figure 3.1 Reflection (R) and transmission (T) of a laser beam from air (index of refraction n_1) through a dielectric film (n_2) into a polysilicon layer ($\hat{n}_3$).

The reflectivity of the laser energy from the dielectric film, at normal incidence as a function of the film thickness, can be calculated by the following equation [3.12]:

$$R = \left| \frac{r_{12} + \hat{r}_{23} \exp(4\pi i n_2 d / \lambda)}{1 + r_{12} \hat{r}_{23} \exp(4\pi i n_2 d / \lambda)} \right|^2, \quad (3.1)$$

where:

$$r_{12} = \frac{n_1 - n_2}{n_1 + n_2}, \quad \hat{r}_{23} = \frac{n_2 - \hat{n}_3}{n_2 + \hat{n}_3}.$$

This analysis shows that the reflected laser energy exhibits a periodic change as a function of the dielectric film thickness. The minimum reflectivity occurs at thicknesses given by the relation:

$$d = \frac{\lambda}{4n_2} \left\{ 2m + 1 + \pi^{-1} \tan^{-1} \left(\frac{2n_2 k_3}{n_2 - |\hat{n}_3|^2} \right) \right\}, \quad (3.2)$$

where m is an integer. Then, using equation 3.1, the ideal AR film of zero reflectivity would be obtained when:

$$n_2^2 = n_1 n_3 + \frac{n_1 k_3^2}{n_3 - n_1}.$$

Then with n_1 (air) = 1, $\hat{n}_3$ (Si) = $4.2 + 1.3i$ [3.13], n_2 (AR) should be 2.18.. This condition can be best satisfied using Si_3N_4 ($n_2 \sim 2.00$) rather than SiO_2 ($n_2 = 1.45$). For an Ar ion laser ($\lambda \sim 0.5 \mu\text{m}$), the thickness of the AR Si_3N_4 layer that allows maximum absorption of laser energy is calculated from equation 3.2 to be 560 Å.

More detailed results of calculations for the reflectivity of Ar laser light from solid and liquid Si, as a function of the Si_3N_4 thicknesses dielectric coatings, are shown in Figure 3.2. These results indicate that for melting the silicon, the selected thickness of the Si_3N_4 AR film should be ~ 530 Å; i.e., intermediate between the optimum values for solid and liquid Si. In practice, we use a Si_3N_4 thickness of 600 ± 50 Å to improve the uniformity and the quality of the film as an etch mask. Then, from the absorptivity ($1-R$) the power required to reach the melt threshold, when the temperature T reaches melting (T_M), and the recrystallization threshold when silicon melts to a significant depth (i.e., the reflectivity reaches that of molten Si) may be deduced.

If the absorbed power is normalized to $P = 1$ at the melt threshold for AR coated material, then $P = 1.7$ is required to reach the melt threshold in uncoated areas while only $P = 1.3$ is needed to reach the crystallization threshold under the AR coating. In fact, the uncoated material does not achieve a deep melt until $P = 3$. Therefore, we can selectively crystallize those areas of a silicon film covered by a patterned Si_3N_4 AR cap. Also, Si_3N_4 is compatible with Si processing in terms of its deposition, pattern definition, and etching selectivity with respect to polysilicon.

Figure 3.2 Optical reflectivity from several surfaces for light from an argon laser in the multiline mode. The material is crystalline silicon with a coating of Si_3N_4 . The optimum AR coating thickness is 560 Å on solid Si and 500 Å on molten Si.

3.2.2 Experimental Details

Based on the preceding analysis, test samples were structured as shown schematically in Figure 3.3, where a 500 Å layer of SiO₂ was thermally grown in dry O₂ at 1000°C on a <100> Si wafer. This procedure was followed by a low pressure chemical vapour deposition (LPCVD) of a 0.5 µm layer of undoped polysilicon at 650°C and a 600 Å film of Si₃N₄ at 800°C. The nitride film was then patterned by plasma etching into rectangular islands with dimensions varying from 2 µm x 100 µm up to 5 mm x 5 mm; the test pattern used is shown in Figure 3.4. The LA was carried out in a Coherent System 5000 laser annealer by the raster scanning of a focussed argon laser beam across the sample surface. With the use of a heated vacuum chuck, the substrate was maintained at a temperature of 500°C. Then, the 50 µm laser spot was scanned with 80 % overlap at an incident power of 3.5 to 5.0 W at a speed of 50 cm/s, and with an incident power of 8.5 to 12.5 W at 400 cm/s.

After laser processing, the batch was divided into four groups for analysis. The Si₃N₄ was removed from the first group so that the polysilicon could be Secco etched [3.14] to delineate its grain structure; subsequently the grains were observed in the SEM. In the second group the polysilicon was wet etched (with the nitride on) to study edge profiles, etching characteristics and undercut. A solution of CH₃COOH:HNO₃:HF was used, since it preferentially removes polysilicon over Si₃N₄ with a ratio of several hundred to one.

A similar procedure was carried out for the third group, except that dry etching in a plasma of CF₄ + 5% O₂ was used. In this case, a photoresist etch mask was required, since the plasma etched both poly-

Figure 3.3 The sample structure.

Figure 3.4 Test pattern used.

silicon and Si_3N_4 ; both groups, were then studied in the SEM. The Si_3N_4 was removed from the fourth group by etching in HF prior to performing a POCl_3 deposition for 45 min at 900°C , followed by drive-in at 1000°C for 30 min; and then sheet resistivity was measured. A subsequent laser activation step, in the solid phase, was carried out at a speed of 50 cm/s with a laser power of 5 W (below the melt threshold), followed by a repetition of the sheet resistivity measurements.

3.2.3 Results

In Figure 3.5, the effect of laser power on the grain size of polysilicon films during SLA is illustrated. Using a scanning speed of 50 cm/s, not much difference in grain size could be observed between coated and uncoated films up to a laser power of 4 W (Figure 3.5a). In this figure, the central islands were coated with the Si_3N_4 AR cap during LA, while the surrounding regions were not. Samples laser processed at 4.5 W showed partial crystallization of AR coated islands (Figure 3.5b), indicating that this laser power is just above the crystallization threshold. At a laser power of 5 W, a deep melt occurred and the coated polysilicon islands recrystallized into large elongated grains (Figure 3.5c). The uniformity of the transition region, between the large and small grain areas, appeared better along the edge parallel to the laser scan direction. The average grain size of the laser recrystallized polysilicon film was found to be limited by the island borders which affect the temperature distribution during recrystallization from the melt. Grains as large as $5\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ were observed in $5\text{ mm} \times 5\text{ mm}$

Figure 3.5 SEM micrographs of LA samples after Si_3N_4 removal and decoration of the grain boundaries with a secco etch (Scale = 2 KX). The LA was carried out at 50 cm/s with a laser power of (a) 4, (b) 4.5 and (c) 5 W.

Si_3N_4 coated areas. However, as illustrated by Figure 3.6a, these large grains exhibit protrusions or pits similar to those reported by Kamins [3.15] and Palkuti et al. [3.16]. No such defects were observed in LA polysilicon films coated with patterned small Si_3N_4 islands of $<20 \mu\text{m} \times 100 \mu\text{m}$ in size, as demonstrated in Figure 3.6b. Unlike large AR coated islands, the absence of defects in small recrystallized islands is ascribed to interfacial stress relief at the edges of the AR coating, resulting in a smooth recrystallized polysilicon film, as shown in Figure 3.6b.

No significant difference was detected in grain morphology between samples annealed at a scanning speed of 50 cm/s and those annealed at 400 cm/s, except for slightly sharper edge definition (Figure 3.7). However, the crystallization threshold at 400 cm/s was $\sim 8.5 \text{ W}$ compared to $\sim 4.25 \text{ W}$ for the case of 50 cm/s. The major changes in grain morphology, due to SLA, have a significant effect on the etch rate of polysilicon. In Figure 3.8 we show the etch rate of the AR coated and uncoated polysilicon films, subjected to identical laser annealing conditions ($v = 50 \text{ cm/s}$), as a function of laser power. In either case, for wet etching, there is a fall in the etch rate from an initial value for unannealed polysilicon followed by an increase in the etch rate with increasing laser power, and ultimately a decline in the etch rate at the highest level of incident power. These results indicate that the maximum etch rate ratio between uncoated and coated laser annealed polysilicon films is 2:1, and occurs at a laser power of 4 W. Etch rates in the plasma were measured only for unannealed and fully recrystallized uncoated polysilicon films, giving a ratio of 11:1. This ratio likely held true for selectively annealed, coated material, since no change in the

Figure 3.6 SEM micrographs of two AR coated areas annealed under the same conditions (Scale = 5 KX). Pitting of the polysilicon

(a) is not present in (b).

(a) is part of a 5 mm x 5 mm region (essentially a blanket AR coating).

(b) is defined into small (20 μ m x 100 μ m) islands.

Figure 3.7 SEM micrograph similar to Figure 3.5, except that laser recrystallization was carried out at 400 cm/s. with an incident power of 10 W (Scale = 5 KX).

Figure 3.8 Etching rates for AR coated and uncoated polysilicon laser annealed under the same conditions.

edge profile of plasma-etched islands was observed until the laser power exceeded the crystallization threshold.

SEM micrographs of etched samples (with the Si_3N_4 coating still on) before and after SLA are shown in Figures 3.9 through 3.12. As can be inferred from these figures, undercut is reduced by a factor of more than two after SLA. Even more striking is the improvement in edge uniformity; since for wet etching the edge uniformity is improved from $\pm 0.25 \mu\text{m}$ to $\pm 0.05 \mu\text{m}$, while for dry etching the change is from $\pm 0.1 \mu\text{m}$ to $\pm 0.03 \mu\text{m}$. Such improvement in edge profiles is highly desirable for VLSI polysilicon gates. Because the wet etching process is self-aligning, all edges look the same. However, there is a noticeable difference between the left and right edge of Figure 3.12 because of misalignment between the nitride and photoresist.

Due to the expansion of silicon on melting ($\sim 10\%$) and contraction on cooling, there tends to be a flow of material in the direction of the advancing melt front at low speeds (Figure 3.13a). However, this phenomenon is observed only when a very long polysilicon stripe is laser annealed at low speed, since the material transported accumulates at the end of the stripe resulting in an increase in the film thickness.

Annealing at high speeds (400 cm/s) produces similar etching results, with one major improvement: because the melt dwell time is greatly reduced so that little mass transport occurs, and the island thickness remains uniform (Figure 3.13b).

Doping of polysilicon with phosphorus resulted in a sheet resistivity of $82 \pm 5 \Omega/\square$ for unannealed areas, and somewhat lower resistivities ($30\text{--}45 \Omega/\square$) for regions that had been previously recrystallized as presented in Figure 3.14. In this figure, the open symbols represent regions left uncoated during laser processing, while the filled symbols

(a)

(b)

Figure 3.9 Two polysilicon islands after wet etching with the Si_3N_4 cap still present, overhanging the undercut region. Both in this figure and in Figure 3.10 the samples were deliberately over-etched to emphasize the edge nonuniformities (Scale = 19.5 KX).

(a) was not annealed.

(b) was SLA.

Figure 3.9c) A polysilicon island (3 μm wide) is shown after wet etching with the Si_3N_4 cap still present, overhanging the undercut region (Scale = 18.7 KX). The corresponding non-annealed pattern was completely etched off.

Figure 3.10 Etch profile of SLA islands (top view) as in Figure 3.9.

Figure 3.11 Same as in Figure 3.9, but plasma etched (Scale = 15 KX).

(a) was not annealed.

(b) SLA at 5.25 W.

(a)

(b)

Figure 3.12 Top view of SLA islands shown in Figure 3.11. The left-hand edge is not well defined because of misalignment between the photoresist and the island (Scale = 15 KX).

(a)

(b)

Figure 3.13 Mass transport occurs during SLA at speeds of

(a) 50 cm/s (@ 4.5 W) and

(b) 400 cm/s, (@ 9 W).

Figure 3.14 Sheet resistivity of 0.5 μm phosphorus doped polysilicon as a function of the laser power applied during the LA step ($v = 50 \text{ cm/s}$). Results are shown before ($\circ, \bullet$) and after ($\square, \blacksquare$) the laser activation step.

indicate samples which had an AR coating. After a solid phase-laser activation step, sheet resistivity was reduced to $10.2 \pm 0.2 \Omega/\square$ as a maximum variation from wafer to wafer, and from one laser melting condition to another; within one wafer, the variations were $\pm 0.1 \Omega/\square$.

3.3 Analysis

The experimental results, described in the previous section, indicate that melting or recrystallization of AR coated SOI polysilicon islands occurs at a certain threshold laser power which is dependent on the laser scanning speed and the thickness of the underlying gate oxide. Under the same laser annealing conditions, uncoated polysilicon areas anneal slightly without melting, and with only a minor change in grain morphology. The difference in properties, between AR coated and uncoated LA polysilicon, are understood through the use of Calder's [3.9] LA model as a means to predict melting and recrystallization thresholds and depth of melting.

The results illustrated in Figure 3.15 are obtained using this model. As can be observed in this figure, as laser power increases, the sample is heated until the melting temperature is reached (the melt threshold). Then, over a broad range of incident power, any increase in laser power is balanced by an increase in reflectivity as the layer of molten (metallic) Si becomes thicker. Finally, at the recrystallization threshold, the reflectivity reaches the value for bulk molten silicon, and any further rise in laser power produces a rapid increase in the melt depth, and consequent large grain growth. Clearly there is a broad window in laser power (from 4 to 9.5 W at 50 cm/s in this example) within which

Figure 3.15 Melt depth and surface temperature, using the structure shown in Figure 3.3 and the model in Ref. [3.9], with and without the Si_3N_4 AR coating at 50 cm/s.

AR coated polysilicon can be melted throughout its depth, and recrystallized into large grains before the recrystallization threshold is even reached in surrounding uncoated areas. In fact, this is the major advantage of this technique.

Since the etch rate is proportional to the surface to volume ratio of the grains, an increase in grain size will reduce etch rates because fewer grain boundaries exist to enhance the effective surface area. This hypothesis is confirmed since the progression from unannealed to LA polysilicon corresponds to increasing grain size and decreasing etch rate. In fact, it has been found that fully melted and recrystallized blanket areas of polysilicon etch over 10 times more slowly than completely unannealed regions (Figure 3.8), while differences between neighbouring LA regions (coated and uncoated) are less. The lack of grain boundaries also removes most paths for rapid etching into the island edges, so that uniformity is greatly improved. Although the grain structure is visually more uniform along the edge parallel to the laser scan direction (Figure 3.5), it changes less abruptly than at the leading edge of the island, which meets the beam head-on, and is not pre heated while the beam is still over the uncoated area. Therefore, the change in etching characteristics will be more abrupt in the latter case and, as is observed, the undercut is further reduced as a result.

The absence of pitting of the polysilicon means that careful treatment of the Si_3N_4 or non-standard deposition processes are not required as in the case of blanket Si_3N_4 caps [3.16]. Since these defects are known to arise from interfacial stresses [3.16], the absence of pitting under patterned Si_3N_4 can be attributed to stress relief at the island edges. Etch rates are affected not only by the distribu-

tion of grain boundaries, but also by other defects present in the material. The creation and/or absence of defects (in the presence or absence of the Si_3N_4 cap) below the melt or recrystallization thresholds may account for the complex behaviour of the wet etch rate as a function of laser power (Figure 3.8). This phenomenon is more clearly demonstrated in Figure 3.16, where Figures 3.8 and 3.15 have been combined to plot etch rate against surface temperature. There is definitely more than one sequence of defect creation and annealing. Detailed microscopic studies are necessary to confirm this hypothesis, especially since the phenomenon apparently does not occur for plasma etching.

From the resistivity measurements, we can differentiate between the effects of crystal size and degree of activation. There is a reduction in resistivity by a factor of two when the phosphorus is diffused into large grain polysilicon, as compared to fine grained (unannealed) polysilicon, although the reproducibility is not good. Since the diffusion length during drive-in is only 650 Å, there will be a high concentration of phosphorus near the surface of the large grains, with a consequent reduction of electrical activity. The subsequent activation has a much greater effect (4 times reduction in resistivity) and results in a high degree of sample-to-sample uniformity.

From all these results, it can be appreciated that the structure shown in Figure 3.3, in conjunction with SLA and preferential etching, can be used to produce well-defined small-geometry gates, and interconnects with low electrical resistivity for VLSI devices. Reduced undercut and much improved edge uniformity will allow smaller structures to be patterned reproducibly. When this process is followed by diffusion of the polysilicon while the source/drain regions are protected, high con-

Figure 3.16 The wet etching results of Figure 3.8 replotted against surface temperature as calculated from the model [3.9]. The inset shows the data from the transition region as a function of melt depth.

ductivity, small-geometry gates and interconnects can be obtained. The same techniques can also be applied to polysilicon used as a common gate and an active substrate in stacked devices [3.7,3.8], so that a film region can be melted and recrystallized without affecting neighbouring structures. The technique is particularly useful in fabricating the 3-D MOSFET, introduced in Chapter 2.

Another potential application of the SLA technique is for the simultaneous activation of the source/drain implants, and recrystallization of the gate of a conventional MOS transistor. Annealing of implant damage is an important area of LA research since, if the silicon is held to a temperature below the melting point during LA, then high quality recrystallization of implanted regions with 100 percent activation can be obtained with negligible dopant redistribution [3.17]. Therefore, very shallow junctions can be fabricated with no lateral diffusion [3.18]. Unfortunately, these requirements for source/drain implant annealing are not compatible with recrystallization of gate polysilicon where melting is desirable; therefore the two processes cannot be optimized simultaneously [3.19]. In the SLA process presented, a Si_3N_4 AR coating is introduced over the gate region, but not the source or drain regions of an MOS transistor; the gate can then be melted and recrystallized into low-resistivity material with large grains while annealing the source and drain implant damage, but without melting and subsequent dopant diffusion. For example, under the conditions shown in Figure 3.15, a laser power of 4.5 W would be appropriate. The present approach can also be applied to future "wafer scale integration", to connect or disconnect redundant modules.

In summary, the laser processing technique presented in this chapter is characterized by the following:

- (1) Achieving recrystallization in selective polysilicon areas, by applying an AR coating of optimum thickness.
- (2) Preferential etching between LA and unannealed polysilicon areas.
- (3) Uniform edge profile with minimum undercut.
- (4) Significant increase in grain size and reduction in sheet resistance of LA polysilicon with a high degree of sample-to-sample uniformity.
- (5) The pitting problem, usually encountered in annealing continuous polysilicon films with a Si_3N_4 cap, is eliminated when the Si_3N_4 is confined into small areas.
- (6) The use of 600 Å of Si_3N_4 to achieve SLA is compatible with Si processing technology.
- (7) Activation of source/drain implants and recrystallization of gates where melting is required can be achieved simultaneously in conventional device structures.

With these advantages in mind, this technique will be useful in the fabrication of 3-D MOSFETs (SMOS).

However, in order to establish this novel technology, the electrical and physical effects of laser recrystallization of the gate polysilicon on underlying gate oxide, the most critical device element, must also be investigated, since the LA must take place in the presence of the underlying oxide. This is to verify whether or not laser recrystallization of the gate polysilicon causes any deleterious effect on the oxide itself, or on the Si/SiO₂ interface. Such a study is presented in the next chapter.

3.4 Conclusions

A novel laser technique has been described, in which a Si₃N₄ anti-reflection coating is used to achieve selective recrystallization, and preferential etching in neighbouring polysilicon islands. This technique is primarily aimed at 3-D devices. Compared with standard etching, the undercut has been reduced by more than a factor of two, and the edge nonuniformity has been significantly improved, without pitting of the polysilicon, so that precise and reproducible small-geometry gates can be fabricated. Sheet resistivity is reduced by 8 times from unannealed material, and achieves a uniformity of $\pm 2\%$, but only after a second (solid phase) laser activation step. In addition, simultaneous laser annealing of the source/drain ion implantation damage and laser recrystallization of the gate in an MOS transistor is now possible, so that high quality devices can be obtained with shallow junctions.

CHAPTER 4

EFFECTS OF LASER RECRYSTALLIZATION OF POLYSILICON GATES

ON UNDERLYING OXIDES

4.1 Introduction

Laser processing applications in novel (e.g., multilayer 3-D MOS devices) or conventional device structures must accomplish the desired material alterations in regions of interest without causing deleterious effects on underlying layers. Therefore, laser recrystallization of polysilicon films on insulators (SOI), as in SMOS or SOI devices [4.1], must not result in degradation of the underlying gate oxides or Si/SiO₂ interface. In conventional devices, the gate polysilicon is very heavily doped, therefore the polysilicon/SiO₂ interface is never depleted. In 3-D devices, the active region of the top device is placed in the LA top polysilicon film itself; therefore the film is doped only moderately so that it becomes the conduction channel of stacked devices. Then, there is the possibility that depletion and inversion layers can be formed by degradation of the insulator or the active polysilicon substrate/insulator interface. It is clear then that the underlying insulator and the quality of the interface play an important role in the performance of these devices.

In addition, the requirement for a device quality low temperature oxide has become essential for small geometry VLSI devices [4.2], and devices that include more than one layer of gate oxide, e.g., stacked devices [4.1, 4.3-4.7], for which the upper gate might be grown in the presence of junctions formed in the starting substrate. High temperature oxidation causes severe redistribution of dopants previously implanted in

underlying layers. The use of High Pressure Oxide (HiPOx) [4.8] for the upper gate oxide is an advantageous means of overcoming this problem because it can reduce the oxidation time and temperature, compared to atmospheric thermal oxidation [4.9], so that the junction movement is greatly reduced. It has also been reported that oxidation induced defects are suppressed [4.10] and stresses in the larger wafer can be reduced as a result of high pressure oxidation. Thus, it has become necessary to examine the potential of HiPOx as a gate dielectric for these devices.

Therefore, a research study was conceived to investigate the electrical properties of conventional thermal and HiPOx oxides underlying Laser Annealed (LA) polysilicon films, using the electrical properties of non-annealed samples as a reference. In this study, a range of oxide thicknesses in single layer MOS capacitors, formed from atmospheric oxide or HiPOx with n^+ polysilicon electrodes on n-type substrates, will be used to simulate the fabrication process of single and stacked MOS devices. This chapter describes the LA effects of polysilicon gates on one atmosphere and high pressure oxides in single layer devices, and discusses the applicability of this study to double layer structures (interlayer oxides).

Most previous research on LA of conventional thermal oxides on silicon has been carried out with pulsed lasers [4.11,4.12]. In these studies, there was no polysilicon layer over the oxide, and LA was applied until visual damage became apparent. It was found that such damage occurs when silicon beneath an oxide is melted; since SiO_2 is not wetted by molten silicon there is a loss of adhesion and even buckling of the SiO_2 film [4.13]. However, laser irradiation of a polysilicon film on SiO_2 should melt only the uppermost layer, and

therefore protects the underlying oxide. Furthermore, for selective laser annealing [4.14], the LA conditions are optimized such that laser processing achieves the desired material changes in selected regions, without causing undesirable material changes elsewhere.

The present study involved mainly the fabrication and analysis of two batches (SP36 and SP8), and was conceived to achieve the following objectives:

- (i) Verify if LA can be used advantageously to melt polysilicon on insulator (SOI) films, without damaging either the SiO_2/Si interface or the underlying SiO_2 layer itself, for conventional thermal oxide and HfPO_x .
- (ii) Determine an optimum LA "process window" to achieve good-quality recrystallized polysilicon films on insulator, for application in 3-D devices, with device quality MOS properties.
- (iii) Examine the suitability of HfPO_x for application to low temperature processing in general and 3-D technologies, in particular.

The experimental details, results and discussions are presented in the next sections.

4.2 Experimental Details

4.2.1 Sample Preparation

All structures used in this investigation were fabricated on n-type <100> silicon wafers with a resistivity of 3-7 $\Omega\text{-cm}$. The wafers were cleaned for 15 min at 70 to 85°C in deionized (DI) water:30%

$\text{NH}_4\text{OH}:30\% \text{H}_2\text{O}_2 = 5:1:1$, followed by 15 min at 70 to 85°C with DI water: 38% $\text{HCl}:30\% \text{H}_2\text{O}_2 = 6:1:1$. The wafers were then oxidized at 1 atm, and etched back in DI water: $\text{HF} = 10:1$ to hydrophobia. A range of thicknesses of atmospheric and high pressure thermal oxides was then grown using standard oxide-growth conditions. Oxide thickness and oxidation conditions are shown in Table 4.1. Oxide growth was followed by in situ annealing in pure nitrogen (for 20 and 30 min for atmospheric and HiPOx , respectively) at the same temperature and pressure.

A low pressure chemical vapour deposition (LPCVD) of 0.37 μm undoped polysilicon film on all wafers was then carried out at 625°C, followed by POCl_3 doping of the polysilicon and etching of the Phosphosilicate Glass (PSG). The polysilicon was then recrystallized using a scanning cw argon laser annealing system. During LA, the substrate temperature was held at 500°C for 30 min, then laser annealing conditions were optimized to achieve melting in the polysilicon layer and to determine a useful laser "processing window". The raster scans were stepped with an increment of 10 μm , giving an overlap of 80%, for a beam diameter of 50 μm scanned at a speed of 50 (or @ 400) cm/s. After LA, the samples received conventional cleaning. The polysilicon was patterned by plasma etching to form an array of capacitors, having structures as shown in Figure 4.1, with areas ranging from 25×10^{-4} to $2.25 \times 10^{-2} \text{ cm}^2$. The polysilicon served as the gate electrodes; no metal electrodes were used. Sintering at 450°C in H_2 for 35 min was carried out, and the back oxide was then etched off to allow gold deposition on the back surface, to provide good back contact.

Table 4.1: The range of oxide thicknesses and the oxidation conditions for the oxides used in the present study.

Pressure	Oxide Thickness ($\text{\AA}$)	Oxidation Conditions	Annealing Conditions
1 atm	1100	1050°C 97% O_2 + 3% HCl	1050°C in N_2 for 20 min
	900	1000°C 97% O_2 + 3% HCl	1000°C in N_2 for 20 min
	550	1000°C 97% O_2 + 3% HCl	1000°C in N_2 for 20 min
	240	900°C 50% O_2 + 47% Ar +3% HCl	* *
10 atm	1100	920°C 100% O_2	920°C in N_2 for 30 min
	900	920°C 100% O_2	920°C in N_2 for 30 min
	550	920°C 100% O_2	920°C in N_2 for 30 min.
	300	800°C 100% O_2	1000°C in N_2 for 30 min

* pre-oxidation etch: 900°C in 0.5% O_2 + 99% Ar + 0.5% HCl for 10 min.

* post-oxidation etch: 1050°C in 0.5% O_2 + 98.5% Ar + 1% HCl for 20 min.

Figure 4.1 Single layer MOS capacitor with n⁺ polysilicon electrode.

The batch SP8 was processed in the same way as batch SP36, except that only a 500 Å gate oxide was investigated, and the POCl_3 doping was performed after the LA was carried out. Also, after patterning the polysilicon, all the wafers had an additional Furnace Anneal (FA) at 900°C in N_2 ambient for 30 min, to simulate 3-D device processing [4.1] and remove effects that might result from LA.

4.2.2 Electrical Characterization Techniques

The electrical characteristics studied were breakdown field strength, leakage current, high-frequency (1 MHz) C-V characteristics, flatband and threshold voltages and minority carrier generation lifetime for laser processed and conventional samples. A computer controlled measurement system was used to provide statistical information. The breakdown field and leakage current were measured by ramping the voltage at a rate of 0.8 V/s. The leakage current was measured with a picoammeter connected in series with the sample, to monitor the current up to a maximum applied voltage of 50 V. The breakdown voltage was identified when the current through the oxide reached $50 \mu\text{A}/\text{cm}^2$ or more. The measuring polarity was selected to accumulate the semiconductor surface, so that the entire applied voltage appeared across the oxide. Effective interface charge density (Q_{ss}), oxide thickness, flatband (V_{FB}) and threshold (V_T) voltages were deduced from the C-V characteristics. The minority carrier generation lifetime was measured by the application of a voltage pulse (at 1 MHz), and monitoring the capacitance of the MOS structure as a function of time (C-t curve). Generation lifetime was determined from the straight segment slope of a Zerbst plot, which is

extracted from the transient response of the C-t curve [4.15]. After the electrical characterization was completed, the polysilicon grain boundaries were delineated with a Secco etch [4.16], for SEM observation of the crystallite morphology. The LA polysilicon was then etched off to observe in the SEM any Si residue or possible oxide damage introduced by LA. Cross sections of the LA structures were also examined to determine the oxide integrity.

4.3 Results and Analysis

Laser annealing of the n^+ polysilicon capacitor electrodes resulted in melting and recrystallization of the polycrystalline material, and thus formation of grains as large as $4\text{ }\mu\text{m} \times 20\text{ }\mu\text{m}$, compared to a grain size of about $1000\text{ }\text{\AA}$ for the unannealed samples. To examine changes in the recrystallized polysilicon surface morphology, SEM micrographs of laser annealed and unannealed, Secco etched samples are exhibited in Figure 4.2; the most striking feature is the surface smoothness of the LA sample. Further SEM analysis revealed no damage to the oxide or Si residue on the oxide surface as a result of LA, as demonstrated in Figure 4.3, where an SEM micrograph of the oxide surface, after removal of the recrystallized polysilicon, is shown. However, in the case of thin oxides ($\sim 300\text{ }\text{\AA}$), melting in the starting substrate was observed, as demonstrated by the SEM micrograph in Figure 4.4. In this particular case, the laser power level used in processing the polysilicon exceeded that required for a complete recrystallization of the polysilicon film. It is worth mentioning that the melting tracks in the substrate were apart from one another by $\sim 10\text{ }\mu\text{m}$, which was the step

(a)

(b)

Figure 4.2 SEM micrographs of unannealed (a) and 7.35 W LA (b) n^+ polysilicon capacitor electrode. The grain boundaries were delineated with a Secco etch in both cases.

Figure 4.3 SEM micrograph of oxide (1090 Å & 1 atm) surface after etch removal of laser recrystallized polysilicon (@ 7.35 W).

Figure 4.4 SEM micrograph of the starting substrate surface of an annealed (7.7 W) capacitor, after etch removal of the recrystallized polysilicon film and the underlying gate oxide (313 Å), showing melting in the bulk silicon.

size used in laser processing the polysilicon, and just above the melt threshold as will be discussed later. Melting of the starting substrate must be avoided because molten silicon does not wet SiO_2 and it results in loss of adhesion with the overlying oxide and even buckling, and thereby degraded electrical properties.

Histograms of breakdown field strengths, for laser processed and conventional capacitors fabricated in atmospheric pressure, are displayed in Figure 4.5. The breakdown field strength was defined to be the voltage of the low field breakdown, and not the final destructive breakdown. The low field breakdown voltage is of prime interest from the device application point of view, since it may render the device useless. The determination of the breakdown field strength was based on the oxide thickness as obtained from C-V measurements. As presented in Figure 4.5, for atmospheric oxide (543 Å), there is no significant change in the average breakdown field strength ($\sim 8 \text{ MV/cm}$) or in the distribution as a result of LA. The yield was 94% for non-annealed samples, and 92% for samples annealed at 7 W and 50 cm/s. The defective samples were identified as those for which the current through the oxide reached at least $50 \mu\text{A/cm}^2$ at $0.6 E_{\text{max}}$ of a good sample.

However, for samples subjected to laser powers higher than that required to achieve deep melting of the polysilicon film, i.e., when the substrate damage threshold was reached, there was a significant drop in the yield. At this point, the yield dropped to 77% for samples annealed at 17.5 W (400 cm/s) as compared to 94% for a standard sample, and further reduced to 73% for samples annealed at 7.75 W (50 cm/s). These results are consistent with those demonstrated in Figure 4.6, where a recently developed model [4.17] was used to predict a useful laser "processing window" (the hatched area) for applications in 3-D devices,

Figure 4.5 The breakdown field-strength distribution for 1 atm oxide (543 Å) with and without laser annealing.

Figure 4.6 The experimental laser powers used (●) and the predictions of the model (solid lines), which is described in Ref. [4.17], of different laser processing regimes. The hatched area is the useful laser "processing window".

which provides a basis for comparing the process window determined by the model with that determined experimentally. The thresholds for shallow melt, recrystallization, melt to oxide (i.e., throughout the polysilicon) and substrate damage are also shown in the same figure, for a wide range of oxide thicknesses.

As can be concluded from Figure 4.6, the laser power values that resulted in no detrimental effects on the oxide properties are in good agreement with the predictions of the model, i.e., located in the hatched area. Therefore, the power must be kept below the threshold for substrate damage. In this power range, the breakdown field strength and the yield are comparable or even slightly superior to those of conventionally processed oxides. The general trend for the breakdown field-strength dependence on the oxide thickness for LA or non-annealed samples is consistent with that observed by Harari [4.10]. The breakdown field was increased for decreasing oxide thickness, increasing from < 8 MV/cm for oxides thicker than 1000 Å to > 9 MV/cm for oxides thinner than 250 Å.

The I-V characteristics revealed no significant difference between laser processed and conventional samples (for oxide thicknesses > 250 Å), as demonstrated by Figure 4.7. The I-V characteristics in both cases show no peculiar behavior, and are consistent with the Fowler-Nordheim tunnelling emission process. At field strengths of > 8 MV/cm, a sharp increase in the leakage current was observed for most samples, which is attributed to a combination of Fowler-Nordheim tunneling emission and Schottky emission, the latter mechanism being the dominant effect.

Figure 4.7 Typical I-V characteristics for 1 atm oxide (543 Å) with and without laser annealing.

On the other hand, for thin oxides ($\sim 240 \text{ \AA}$) the LA samples exhibited a significant increase in the leakage current. This degradation is demonstrative of laser associated effects, which can be considered as a direct consequence of the use of laser power beyond the useful range as can be seen in Figure 4.6. Moreover, the width of the laser process window becomes smaller for thin oxides which makes laser applications in such cases more critical.

Breakdown field strength and I-V characteristics for HfPO_x were also not affected by laser recrystallization, as demonstrated by Figure 4.8. For these samples, the breakdown field strength was $\sim 8 \text{ MV/cm}$, which is comparable to that of atmospheric oxides, and in some cases increased by LA to $\sim 8.55 \text{ MV/cm}$. However, for thin oxides ($\sim 300 \text{ \AA}$), the yield was inferior to that of atmospheric oxide and dropped from 75% to 53% as a result of LA. This significant drop in the yield can be ascribed to the use of a laser power level beyond the threshold for damage, as can be seen in Figure 4.6. Consistent with this result is the melting of the starting substrate silicon, shown in the SEM micrograph of Figure 4.4, resulting in degradation of the MOS properties of these oxides. On the other hand, the optimum growing conditions for thin HfPO_x oxides still require further research to optimize the process, to give high yield and satisfactory electrical properties. No general trend for the breakdown field strength dependence on the HfPO_x oxide thickness could be determined. The breakdown field strengths, and the leakage current (determined @ 7.5 MV/cm) for 1 atm and HfPO_x oxides are summarized in Tables 4.2 and 4.3, respectively, for LA and unannealed

Figure 4.8 The breakdown field-strength distribution for HfPO_x (576 Å) with and without laser processing.

2

Table 4.2: Summary of the results of the leakage current (I_L), breakdown field strength (E_{BD}), and yield for laser annealed and unannealed atmospheric oxides.

Oxide Thickness ($\text{\AA}$)	Laser Power (W)	Laser Speed (cm/s)	I_L (namp)	E_{BD} (MV/cm)	Yield %
232	0	-	4.5	9.05	91
246	8.0	50	35	8.4	95
520	7.75	50	40	8.24	73
543	0	-	130	8.0	94
543	7.0	50	80	8.05	92
548	17.5	400	120	7.75	77
870	0	-	80	8.15	99
875	7.5	50	80	8.05	89
1100	0	-	90	7.85	97
1090	7.35	50	80	7.85	100

Table 4.3: Same as in Table 4.2 but for LA and unannealed high-pressure oxides (HfPO_x).

Oxide	Laser	Laser	I_L	E_{BD}	Yield
Thickness ($\text{\AA}$)	Power (W)	Speed (cm/s)	(namp)	(MV/cm)	%
310	0	-	7	8.65	73
313	7.7	50	9	8.20	53
596	0	-	90	8.00	94
576	7.0	50	93	8.05	95
570	6.5	50	80	8.14	95
549	16.5	400	30	8.55	87
945	0	-	94	8.10	99
919	7.5	50	92	8.20	90
1080	0	-	70	8.15	100
1060	7.5	50	50	-	-

samples. The results for HiPOx with and without LA are acceptable from the device application point of view, except for thin oxides. In most cases, the leakage current in HiPOx samples was smaller than that in atmospheric oxides. These good results are likely due to the higher density of HiPOx [4.18], and the reduction of oxidation stacking faults at high pressures [4.9]. The improvement in refresh time, in MOS dynamic RAMs, for high-pressure oxidation as compared to atmospheric oxidation [4.9] has been attributed to the reduction in leakage current as a result of a reduction in the oxidation induced stacking faults and higher density of HiPOx .

The effective fixed oxide-interface charge density Q_{ss} and the work-function difference (ϕ_{MS}) between the n^+ gate polysilicon and the substrate were extracted from the values of V_{FB} as follows:

$$Q_{ss} = \frac{\epsilon \cdot \epsilon_0}{X_o} (V_{FB} - \phi_{MS}) \quad (4.1)$$

where X_o is the oxide thickness as determined from the C-V measurements. ϵ is the permittivity of free space and ϵ_0 is the dielectric constant of oxide. The ϕ_{MS} was determined by plotting the values of V_{FB} versus oxide thickness. The extrapolation of V_{FB} to zero-oxide thickness was taken as the value of ϕ_{MS} . The values of Q_{ss}/q , V_{FB} and V_T as obtained from the C-V analysis of laser processed and conventional capacitors, made from atmospheric and HiPOx oxides, are summarized in Tables 4.4 and 4.5 respectively. The LA and post-LA thermal annealing conditions are also given in these tables.

Table 4.4: Summary of the parameters obtained from the C-V analysis for laser annealed and unannealed atmospheric oxides.

Oxide Thickness (Å)	Laser Power (W)	Post-LA FA Temp. (°C)	Laser Speed (cm/s)	V_{FB} (V)	V_T (V)	Q_{ss}/q ($10^{10} \cdot \text{cm}^{-2}$)
232	0	-	-	-0.20	-0.93	2
246	8.0	-	50	-0.30	-1.04	3
517	0	900	-	-0.24	-1.01	3
535	4.75	900	50	-0.24	-1.01	3
546	6.0	900	50	-0.24	-1.04	3
543	0	-	-	-0.29	-1.09	5
543	7.0	-	50	-0.52	-1.27	10
548	17.5	-	400	-0.44	-1.24	7
543	7.0	1100	50	-0.30	-1.07	5
520	7.75	-	50	-0.47	-1.38	9
870	0	-	-	-0.35	-1.32	4
875	7.5	-	50	-0.45	-1.41	5
1110	0	-	-	-0.29	-1.33	2
1090	7.35	-	50	-0.47	-1.52	4

Table 4.5: Same as in Table 4.4 but for High-Pressure Oxides (HiPOx).

Oxide Thickness (Å)	Laser Power (W)	Post-LA FA Temp. (°C)	Laser Speed (cm/s)	V_{FB} (V)	V_T (V)	Q_{ss}/q (10^{10} cm^{-2})
310	0	-	-	-0.30	-1.06	4
313	7.7	-	50	-0.40	-1.14	5
516	0	900	-	-0.31	-1.09	3
514	4.75	900	50	-0.32	-1.09	3
596	0	-	-	-0.33	-1.12	3
576	7.0	-	50	-0.44	-1.21	4
570	6.5	-	50	-0.44	-1.20	4
549	16.5	-	400	-0.40	-1.21	3
945	0	-	-	-0.61	-1.60	8
919	7.5	-	50	-0.49	-1.45	4
1080	0	-	-	-0.43	-1.44	4
1060	7.5	-	50	-0.47	-1.49	3

Typical high-frequency C-V characteristics of 1 atm oxide (543 Å) with and without LA are presented in Figure 4.9. The LA samples showed no abnormality in the C-V curves, although a shift to more negative flatband ($\Delta V_{FB} = -0.23$ V) and threshold ($\Delta V_T = -0.18$ V) voltages was, however, observed for these samples. Also, the C-V characteristics revealed slightly higher than normal values of the average effective oxide-interface fixed charge density ($Q_{ss}/q \approx 6.10^{10} \text{ cm}^{-2}$) as can be seen in Table 4.4. These observations are evidence of laser associated damage effects or improper handling or contamination of the wafers during laser processing. It appears that the shift in the C-V parameters have no detrimental effect on the I-V characteristics or breakdown voltages. However, an additional furnace anneal at 1100°C in N₂ ambient for 20 min resulted in shifting the C-V curve back to the same shape as that of non-laser processed samples as displayed in Figure 4.9. The V_{FB} , V_T and Q_{ss}/q values were then the same as those of control samples, and in some cases were even superior.

At this point, a question comes to mind as to whether or not these results are reproducible after post-LA thermal anneal at lower temperature. Indeed, similar electrical behavior was also observed for samples LA at different laser powers, and followed by a furnace anneal at 900°C in N₂ for 30 min as illustrated by Figure 4.10 and Table 4.4. This suggests that the effects due to LA, within the useful power range which caused the shift in the C-V characteristics, are metastable and can be removed by thermal annealing subsequent to laser irradiation. Such a thermal annealing step has also been found to be beneficial in reducing the sheet resistivity of the recrystallized film, as a result of suppression of stresses in the film from $9 \times 10^9 \text{ dyne/cm}^2$ just after

Figure 4.9 High-frequency C-V characteristics for atmospheric oxides (543 Å) without and with LA (before and after Furnace Annealing, FA).

Figure 4.10 Typical high-frequency C-V characteristics for atmospheric oxides, with and without LA. In all cases an additional thermal anneal at 900°C in N_2 ambient for 30 min was carried out.

laser melting to 5×10^9 dyne/cm² after successive furnace annealing [4.19]. How much further the temperature can be lowered while the thermal anneal remains effective is still, however, an open question.

Characterization of HfPO_x also revealed a shift in the C-V curves, typified by those shown in Figure 4.11, as a result of LA. This shift can also be removed by a thermal anneal at 900°C in N_2 for 30 min, as can be depicted by Figure 4.12 in which the C-V curve of a LA sample coincides with that of a control non-laser annealed sample as a result of the thermal anneal, demonstrative of a complete recovery of the laser associated effects. A summary of these results is given in Table 4.5. The properties of HfPO_x , with or without LA, are comparable to those of atmospheric oxides, and are acceptable from device applications point of view. Thus, HfPO_x is recommended as a gate dielectric in MOS devices in general, and for 3-D devices in particular, since the low growth temperature of HfPO_x is an attractive feature for processing such devices.

The previous results were confirmed by characterizing the Minority Carrier Generation Lifetime (MCGL) in the bulk silicon, since the MCGL is extremely structure sensitive; i.e., it is sensitive to the process used in preparation of the device. All the samples characterized by this technique received an additional furnace anneal at 900°C in N_2 ambient for 30 min. The results indicated no significant difference between the lifetimes of laser processed and control samples, as can be concluded from Figures 4.13 and 4.14. The Zerbst plots of LA and control samples (Figures 4.12b and 4.13b) exhibit a considerable linear region with constant slope, indicative of bulk dominated generation of minority carriers. This implies that the minority carrier generation is proportional to the width of the depletion-charge region. Such a conclusion is

Figure 4.11 High-frequency C-V characteristics for High-Pressure Oxides (HiPOx), with and without LA.

Figure 4.12 Same as in Figure 4.10 but for High-Pressure Oxides (HiPOx).

C-t & ZERBST Plot

HP 4061A

Sample = Test

 $V_{ds} = -4.0V$ $T = 296.0K$ $Area = 8.25E-03cm^2$ $C_o = 533.10pF$ $T_{goff} = 3.74E-05sec$ $V_{dd1} = -6.0V$ $N_{sub} = 2.0E+15/cm^3$ $X_o = 500\text{\AA}$ $C_{fin} = 86.90pF$

Figure 4.13 Computer output of the minority carrier generation lifetime measurement showing the C-t (a) and Zerbst (b) plots. Also shown is the generation current as a function of the depletion-layer depth (c). These results are for conventional non-laser annealed oxide (500 Å).

C-t & ZERBST Plot

HP 4061A

Sample = SP-8-6A-8-Annealed

 $V_{ds} = -2.0V$ $V_{dd} = -6.0V$ $T = 296.0K$ $N_{sub} = 2.0E+15/cm^3$ $Area = 8.25E-03cm^2$ $X_o = 500\text{\AA}$ $C_o = 520.50pF$ $C_{fin} = 79.00pF$ $T_{gff} = 4.54E-05sec$

Figure 4.14 Same as in Figure 4.13 but for laser processed conventional oxide (500 Å).

consistent with the results of Figures 4.13c and 4.14c, which exhibit a linear relationship between the generation current, and the depletion-layer width for LA and control samples, respectively. Thus, the contribution of the surface, and thereby the surface states density, to the generation of the minority carrier was negligible as compared to that of the bulk of the depletion charge region. The MCGL was $\sim 37 \mu\text{s}$ and $45 \mu\text{s}$ for control and LA samples, respectively. These results imply that the laser process did not result in the formation of defects, which act as generation-recombination centers for carriers, in the bulk silicon nor did it degrade the Si/SiO₂ interface. Such a conclusion is consistent with the results presented earlier. A similar conclusion is valid for HiPOx.

4.4 Top Gate Oxide

The stacked (3-D) devices, introduced in Chapter 2, require at least two gate oxide levels, as shown in Figure 4.15. Since the upper gate oxide might be grown in the presence of junctions, formed in the starting substrate, it should be a device quality low temperature oxide. High temperature atmospheric oxide is not suitable because it results in severe redistribution of previously implanted dopants in bulk Si. The HiPOx, which is a low temperature gate-worthy insulator as demonstrated in the preceding section, is most useful in this respect because it can reduce the oxidation time and temperature considerably, compared to conventional one atm thermal oxidation, so that dopant redistribution is greatly reduced.

Figure 4.15 Double layer (3-D) capacitor with a common n⁺ polysilicon electrode, representative of CMOS transistors.

In 3-D devices, which require two layers of polysilicon, the upper thermal oxide of the first polysilicon level serves as a gate oxide for the top device. The quality of such oxide is, therefore, crucial for good device performance. As-deposited polysilicon films suffer from crystals with random crystallographic orientations resulting in surface irregularities, mainly asperities and protuberance. When this material is thermally oxidized, the result is an extremely rough oxide surface due to the differences in oxidation rates of the various crystal orientations, resulting in localized field enhancement and, therefore, lower oxide breakdown field strengths and higher gate leakage current [4.20,4.21]. However, laser processing of the first polysilicon layer (common gate) melts the film so that it regrows into large smooth grains, as presented in Section 4.3, resulting in high quality oxides. This observation suggests that laser recrystallizing the first polysilicon layer will result in a drastic improvement of the properties of the upper gate oxide, a significant reduction of the leakage current and increase in the breakdown field-strength. This is indeed consistent with the results reported by Yaron et al. [4.22], who reported three orders of magnitude reduction in the leakage current in oxides grown from laser recrystallized polysilicon, relative to that in oxides of as-deposited polysilicon, as illustrated by Figure 4.16.

The application of LA to 3-D devices requires laser recrystallization of the second (top) polysilicon layer, which acts as an active substrate for the top device. Here, a question arises about the effect of laser processing this layer on underlying gate oxides. The results presented in Section 4.3, for single layer capacitors which are more critical than double layer structures from the laser processing point of

Figure 4.16 The top gate-oxide leakage current as a function of the applied voltage for laser annealed (continuous line) and unannealed (broken line) polysilicon films Ref. [4.22].

view, provide an answer to this question. The results strongly suggest that LA will not degrade the underlying oxide quality or the Si/SiO₂ interface in single layer structures or in double layer structures, since laser processing of the top polysilicon layers is usually easier. In addition, the top SiO₂/LA polysilicon interface, which plays a major role in a 3-D device performance because it forms the conducting channel region of the top device, is significantly improved by laser processing. The effective interface charge density (Q_{ss}) and flatband voltage (V_{FB}) for laser processed (60 kW/cm²), p-type (4.5×10^{14} cm⁻²), polysilicon-oxide (5000 Å) were found to be 5.0×10^{10} cm⁻² and -1.5 V, respectively [4.20]. These values are much superior to those of nonlaser processed structure and are acceptable for all device applications.

4.5 Conclusions

The application of a CW laser to processing of gate polysilicon does not introduce non-recoverable effects to the properties of the underlying gate oxides and/or the Si/SiO₂ interface, at laser power levels below the threshold for substrate melting. There was no significant change in the breakdown field strength or in the I-V characteristics of the oxide as a result of laser processing. However, a slight shift to more negative values of the C-V parameters was observed, demonstrative of laser associated electrical damage, but was eliminated with a subsequent thermal anneal at 1100 or 900°C in N₂ ambient. Characterization of the minority carrier generation lifetime revealed no degradation in the quality of the starting silicon substrate. This result, coupled with those

mentioned above, indicates that no formation of thermally stable defects was caused by laser process in the silicon substrate. The SEM analysis revealed no damage to the oxide or Si residue on the oxide surface, caused by laser processing. Grains as large as $4 \times 20 \mu\text{m}^2$ were observed in the laser recrystallized polysilicon. The results obtained for high pressure oxides imply that their quality is comparable to that of conventional oxides, and they can be used as a gate insulator in MOS structures.

CHAPTER 5
COMPATIBILITY OF CW LASER ANNEALING WITH VLSI TECHNOLOGY
IN MAKING SMALL-GEOMETRY DEVICES

5.1 Introduction

The 3-D MOSFET structures, introduced in Chapter 2, entail the application of laser processing, which is basic to them. The feasibility of this processing technique is contingent upon whether its impact on the device electrical performance as a whole is positive or at least not be negative. The characteristics of contacts, shallow junctions, and the device as an integrated system must not be degraded by LA, especially the devices fabricated in the bulk silicon. Laser Annealing (LA) is particularly interesting because annealing of implantation damage takes place in the solid phase within times of less than 1 ms, so that dopant redistribution is essentially eliminated both vertically and laterally [5.1]. This feature is attractive for the fabrication of VLSI devices, but there have been few published results on this application. Reported work has been for MOSFETs with large-geometry [5.2-5.4]; cw laser annealed devices of small size have not previously been reported.

This chapter describes the fabrication, characterization and analysis of small geometry NMOS transistors, with the objective of investigating the impact of laser processing on the device performance, relating device performance to the materials and device processing techniques, and studying device size limitations. The devices were fabricated in a standard 5 μm process with three variations: (1) the source and drain (S/D) areas were implanted with arsenic and subsequently laser annealed;

(ii) phosphosilicate glass (PSG) densification was the only high temperature step after LA; (iii) wafer stepping was used for improved lithography. Details of the fabrication procedure are described in Section 5.2, whereas device characterization and analysis are discussed in Section 5.3.

5.2 Device Fabrication

The devices were fabricated in 6-10 Ω -cm $\langle 100 \rangle$ p-type silicon substrates. Following conventional LOCOS field oxidation and threshold adjust implantation, a 1067 Å gate oxide was grown in dry O_2 . Polysilicon (0.35 μ m) was deposited by LPCVD, heavily doped by phosphorus diffusion, and patterned by plasma etching to define the S/D regions. The gate length was varied from 1.3 to 50 μ m, and the gate width from 1 to 50 μ m. Arsenic ions were implanted through the gate oxide at 180 keV with a dose of 10^{16} ions/cm², and LA was carried out with a Coherent System 5000 argon ion laser annealer. The laser conveyed 3 W of power in a 50 μ m diameter beam, moving in a raster pattern at 50 cm/s with 10 μ m steps between successive scans, while the back of the wafer was maintained at $500 \pm 2^\circ\text{C}$. Following laser activation of the S/D implants, the gate oxide was removed from these regions, and PSG was deposited and densified at 1000°C for 15 min in a N_2 ambient. Contact windows were then opened and Al-1%Si metallization was carried out with sintering at 450°C for 30 min in H_2 ; a cross section of the device structure is shown in Figure 5.1. The key thermal cycle resulting from the laser annealing step was analyzed using conventional theory [5.5,5.6,5.7], but with the surface reflectivity adjusted to 20%, the

Figure 5.1 A schematic cross section of the device structure.

value for a 1067 Å SiO₂ cap over silicon irradiated by an argon laser ($\lambda = 0.5 \mu\text{m}$). The maximum temperature at the semiconductor surface, for a very high optical absorption, high SiO₂ thermal conductivity, and a gaussian beam of radius w is given by,

$$T = T_0 \{1 + \exp[\beta P(1-R)/2\pi^{1/2} wB]\},$$

where T_0 is the back surface temperature, P is the total incident power, and the silicon thermal conductivity is assumed to be $K = B/T$, where $B = 345 \text{ W/cm}$. The parameter β is a correction for the scanning speed v [5.6], and equals 0.74 for $v = 50 \text{ cm/s}$. The dependence of the surface temperature on laser power is calculated and presented in Figure 5.2. At $P = 3 \text{ W}$, the thermal cycle for silicon is given approximately by $T = 1210^\circ\text{C}$ for a time $t = 2w/v = 100 \mu\text{s}$.

5.3 Device Characterization and Analysis

5.3.1 Physical Characterization

The junction depth (x_j) was measured after the completion of all processing steps by a bevel and etch technique, and found to be 3000 Å, while the initial junction depth before any heat treatment was calculated (using SUPREM-III) to be 2500 Å. The two important thermal cycles are the LA and the PSG densification. The diffusion length for the LA thermal cycle (1210°C for 100 μs) is then only $L_{D\text{max}} = 2(Dt)^{1/2} = 3 \text{ Å}$ (the diffusivity is $D = 2 \times 10^{-12} \text{ cm}^2/\text{s}$ [5.8]); therefore, LA does

Figure 5.2 Dependence of the maximum surface temperature on the incident laser power according to the models of Ref. [5.5 - 5.7]. Results are shown for $1067\text{ }\text{\AA}$ of SiO_2 on Si (—) and for the polysilicon over the field oxide (---).

not contribute to the increased x_j . On the other hand, the PSG densification step at 1000°C for 15 min gives a final calculated junction depth of 2900 Å, without allowing for damage-enhanced diffusion or other effects. As a result, this thermal step effectively accounts for the observed 400 Å increase in the junction depth.

Measurement of channel length was done optically (Figure 5.3), and the lateral diffusion $\Delta L = L_g - L$, where L_g is the gate physical length and L is the actual channel length between metallurgical S/D junctions, was found to be beyond the resolution of the microscope (0.1 μm). Consequently, the smallest physical channel length equals the gate length (1.3 μm). The value of L determined from the electrical measurements was in good agreement with this result. Presented in Figure 5.3 are optical micrographs of polysilicon gates (Figure 5.3a) and the junction boundaries delineated by preferential etching, after the gate polysilicon was lifted off (Figure 5.3b). To estimate x_j and ΔL in an equivalent furnace process, some of the LA samples that had the metal film removed, were given a conventional heat treatment (1000°C in N_2 for 44 min); then, x_j and ΔL were found to be 4100 Å and 0.3 μm respectively, compared with a calculated junction depth of 4300 Å. The effective change in channel width, ΔW , determined electrically by plotting the transconductance (g_m) measured in the linear region (i.e., $V_{DS} \ll V_{GS} - V_T$) versus the nominal gate width. The g_m can be expressed as follows:

$$g_m = \frac{W}{L} \mu_n C_o V_{DS} = \frac{\mu_n C_o V_{DS}}{L} (W_g - \Delta W),$$

Figure 5.3 Optical micrographs showing the polysilicon gate length (a), and the actual channel-length after polysilicon removal (b), made visible by preferential etching.

where $W = W_g - \Delta W$; ΔW denotes the deviation of the physical channel width (W) from the nominal gate width (W_g). The g_m was determined from the measurement of I_{DS} - V_{GS} characteristics. Only the maximum values of g_m were considered to ensure that second order effects are absent, i.e., V_{GS} sufficiently above V_T for g_m to become a maximum, but with V_{GS} still low enough for gate field effects to be negligible. From a least squares fit of the data (Figure 5.4), the interception of the straight line at the abscissa gives $\Delta W = 0.06 \pm 0.18 \text{ } \mu\text{m}$ which we subsequently take to be zero, i.e., $W = W_g$. Then, the smallest device was of approximately $1 \text{ } \mu\text{m}$ square channel size; i.e., $L \times W = 1.3 \times 1 \text{ } \mu\text{m}^2$.

5.3.2 Electrical Evaluation

Electrical evaluation was carried out by means of characterizing sheet resistivity, junction and contact characteristics and transistor performance. Within the S/D regions, the sheet resistivity was $34 \text{ } \Omega/$; if a uniform mobility and 100% activation is assumed, we derive a value of $20 \text{ cm}^2/\text{V.s}$ for the mobility, consistent with recent measurements at high concentrations [5.9]. The low sheet resistivity in the polysilicon regions ($25 \text{ } \Omega/\square$) is a consequence of the melting and recrystallization of the polysilicon films into large ($\sim 1 \text{ } \mu\text{m}$) grain material during the laser processing. The field oxide acts as a thermal insulator, so that the maximum temperature here is higher than in the S/D region; the calculated temperature is shown in Figure 5.2.

Junction diodes fabricated in the same manner as the S/D regions, exhibited a forward-biased characteristic which can be described by the general expression:

Figure 5.4 Transconductance (g_m) versus nominal channel-width (W_g).

$$I = I_0 [\exp (q V_F / mkT) - 1],$$

using an ideality factor $m = 1.17$ for $0.25 < V_F < 0.6$ V (Figure 5.5), indicating that the current is dominated by diffusion not by generation-recombination mechanisms and thus there are few generation-recombination centres. One may conclude that no significant electrical damage was introduced into the junction as a result of laser processing; SEM observations also revealed no surface alteration or cracking. The reverse-biased characteristics indicated a breakdown voltage of $V_{BD} \approx 30$ V, smaller than the value of 60 V predicted by theory [5.10] for a cylindrical junction; an assumption usually applied for furnace annealed devices. The reduced value of V_{BD} for LA diodes can be attributed to a high concentration gradient at the junctions and a low radius of curvature.

The I-V contact characteristics for both the S/D contacts and the gate polysilicon contacts were highly linear, as demonstrated by Figure 5.6, indicating no detrimental effect on the semiconductor surface introduced by LA. The contact resistance (R_c), measured by the 4-terminal Kelvin technique [5.11] in an $8 \times 8 \mu m^2$ area, was 1.5Ω for the S/D areas and 0.5Ω for the polysilicon. This remarkably small value for R_c on polysilicon is attributed to a high surface dopant concentration, in conjunction with the smooth surface of the large grain recrystallized polysilicon, resembling single crystal Si rather than fine grain polysilicon. The morphology of the silicon underlying the contact was examined by SEM after removal of the Al film, and no defects or etch pits were observed. In addition, the melting and recrystallization of polysilicon into large grains resulted in a small number of Si precipitates at the Al/Si interface like the ones depicted in Figure 5.7a.

Figure 5.5 I-V characteristics of LA n^+p junction diodes. The forward biased ideality factor is 1.17 for $0.25 \text{ V} < V_F < 0.6 \text{ V}$, while the reverse breakdown voltage is approximately 30 V.

$R_c(\text{Si}) = 1.5 \Omega$

$R_c(\text{poly}) = 0.5 \Omega$

Figure 5.6 Current-Voltage Characteristics of Laser Annealed Si and Polysilicon Contacts.

This smooth surface contrasts with non-recrystallized polysilicon films, which are known to suffer from large number of Si precipitates (Figure 5.7b) as a consequence of the high diffusion rate of Si in Al, resulting in reduced active contact area and thus high values of R_C . The precipitates are due to Si dissolution in the Al during sintering and precipitates at the contact interface upon cooling. If the polysilicon is recrystallized into large grains, as in the present case, the amount of dissolved Si is smaller, due to a reduction in grain boundary areas and thus less Si precipitation.

5.3.3 Transistor Evaluation

In Figure 5.8, the drain current-voltage ($I_{DS}-V_{DS}$) characteristics are presented for LA NMOS transistors with $W \times L = 50 \times 2.3 \mu m^2$. The device exhibited good $I_{DS}-V_{DS}$ characteristics, no evidence of anomalous behavior or strong short-channel effects over a wide range of V_{DS} , as evidenced by Figure 5.8. No punch through or avalanche multiplication currents below $V_{DS} = 12$ V; V_T was found to be 0.418 V.

The low-field electron effective surface mobility (μ_{no}) for this device was extracted from the $I_{DS}-V_{GS}$ characteristics, in the triode mode of operation (i.e. $V_{DS} < V_{GS} - V_T$), using the relationship:

$$\mu_{no} = \frac{X_o \cdot L \cdot I_{DS}}{\epsilon_{ox} \cdot W \cdot F},$$

Figure 5.7 SEM micrographs of Al-1%Si/polysilicon contact areas with (a) and without LA (b). The metal has been chemically removed.

Figure 5.8 I_{DS} vs V_{DS} characteristics for a LA MOSFET of channel dimensions $W \times L = 50 \times 2.3 \mu m^2$.

$$\text{where } F = \left\{ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right\},$$

ϵ_{ox} is the oxide permittivity, and V_{DS} and V_{GS} are the applied drain and gate voltages (w.r.t. the source), respectively. Small values of V_{GS} and V_{DS} were used to avoid high electric field effects in the channel region. From the applied gate and drain voltages, the measured values of L , W , I_{DS} , V_T and the gate

oxide thickness (X_o), the obtained value of μ_n was $834 \text{ cm}^2 \cdot (\text{V} \cdot \text{s})^{-1}$. This value of μ_n is comparable to values obtained for conventional furnace-annealed devices [5.12], indicating no undesirable effects on the semiconductor surface as a result of laser irradiation. On the contrary, it resulted in shallow junctions and lead to improvements in device performance such as good contact performance, a reduction of short-channel effects and negligible gatesource (or drain) overlap capacitance.

The device with $W \times L = 50 \times 1.3 \text{ } \mu\text{m}^2$ (Figure 5.9a) exhibited deteriorated performance due to high field effects; punch-through is visible at $V_{DS} \approx 1.5 \text{ V}$ and avalanche multiplication currents become significant at $V_{DS} \approx 12 \text{ V}$. On the other hand, the characteristics of the small-size device with $W \times L = 1 \times 1.3 \text{ } \mu\text{m}^2$ (Figure 5.9b) resemble those of large geometry transistors, with a well-defined saturation region over a wide range of V_{DS} . No punch-through is observed for $V_{DS} < 13 \text{ V}$, while avalanche breakdown only occurs for $V_{DS} \approx 14 \text{ V}$. We have also observed a strong dependence of I_{DS} on the substrate-bias (V_{BS}) for short/narrow devices, but little dependence in

(a) $W \times L = 50 \times 1.3 \mu\text{m}^2$.

(b) $W \times L = 1 \times 1.3 \mu\text{m}^2$.

Figure 5.9 I_{DS} vs V_{DS} characteristics for LA MOSFETs with short/wide (a) and short/narrow (b) channels.

the case of short/wide devices, as depicted in Figure 10. Furthermore, I_{DS} for the short/ wide devices is less dependent on V_{GS} than for the short/narrow devices in both sub-threshold and above threshold modes of operation as illustrated by the same figure. Also, I_{DS} of the first device is larger than that of the second device by more than the channel widths scaling ratio (50). The gate voltage swing, ΔV_{GS} , required to reduce the sub-threshold drain current by one decade for the two devices was 0.16 and 0.14 V/decade respectively. The explanation for these results is that, in the case of the short/wide device, I_{DS} is dominated by punch-through current which is weakly dependent on V_{BS} and V_{GS} , while in the second case I_{DS} is mainly due to surface channel current which is strongly influenced by V_{BS} and V_{GS} .

The V_T , extracted by extrapolating I_{DS} vs V_{GS} (@ $V_{DS} = 50$ mV) to zero I_{DS} , was 0.295 V for a device with $W/L = 50/1.3$; however, it was 0.61 ± 0.013 V for a device with $W/L = 1/1.3$ over 32 samples on a single wafer; a histogram showing the V_T distribution for this device is presented in Figure 5-11.

This excellent reproducibility of V_T from one device to another is attributed to the reduction of lateral diffusion in the S/D areas, and to the uniformity of junction edge profiles. The poor uniformity of V_T in furnace annealed devices, particularly those with short channels, is well known [5.13]. A more sensitive annealing quality indicator is the stability of the device's most important electrical parameters, V_T . The stability of V_T of the smallest device ($W \times L = 1 \times 1.3 \mu m^2$) was determined by monitoring the change in V_T (ΔV_T) after bias-temperature stress. A ΔV_T of less than 4% was

(a) $W \times L = 50 \times 1.3\text{ }\mu\text{m}^2$.

(b) $W \times L = 1 \times 1.3\text{ }\mu\text{m}^2$.

Figure 5.10 I_{DS} vs V_{GS} characteristics for a short/wide (a) and short/narrow (b) MOSFETs.

Figure 5.11 Threshold voltage distribution for narrow/short MOSFETs with $W \times L = 1 \times 1.3 \mu\text{m}^2$.

observed, when the gate oxide was stressed by applying 10 V to the gate of the transistor (at 230°C) with the source and drain terminals kept at ground potential for 1 hour. These results imply that laser processing did not degrade the MOS properties of the gate or the electrical performance of the MOSFETs. .

The improved dc characteristics of the short/narrow devices, as compared to the short/wide devices, are due to the beneficial interaction between the narrow- and short-channel effects when combined in one structure. These effects tend to counteract one another resulting in suppressed small-size channel effects, as a consequence of the net electric field distribution in the channel of a short/narrow structure, thereby resulting in a performance that resembles that of long/wide devices. This mechanism can be exploited in reducing the physical limits imposed by geometric effects on device performance in novel short/wide planar or nonplanar (3-D) MOSFET structures like those proposed in Chapter 2 if they are made simultaneously short and narrow.

The results presented in Chapters 4 and 5 verify the compatibility of CW laser processing with IC technology in making VLSI device structures. Such a conclusion is extremely important in the case of 3-D MOSFETs, since laser processing is inevitable for these devices and must not degrade the properties of the underlying gate oxides, the Si/SiO₂ interface or the performance of the device made in the starting substrate.

5.4 Conclusions

Cw laser processing is compatible with standard IC technology and, in fact, results in high-quality VLSI devices with shallow junctions. Small ($W \times L = 1 \times 1.3 \mu\text{m}^2$) devices exhibit particularly good dc characteristics with $V_T = 0.61 \pm 0.013 \text{ V}$, V_T stability within 4% after bias-temperature stress, and high punch-through and avalanche breakdown voltages. This excellent performance arises from the negligible lateral spread of impurities under the gate, from the source and drain areas, as a consequence of short-time laser annealing. It is also attributed to the counteracting short- and narrow-channel effects of electric field distribution.

It is concluded that no detrimental electrical effects or laser damage to the underlying substrate or the MOS structure were found in the properties of small-geometry MOSFETs.

CHAPTER 6

MODELLING OF NARROW-CHANNEL MOSFETs

There is a need to look at modelling and understanding the performance of the vertically integrated 3-D MOSFETs [6.1-6.2], introduced in chapter 2, which are essentially NCDs but with several layers to make up the required width (only two layers are considered in this thesis). However, very scanty work that includes the nonscaling feature of the drain current of conventional NCDs has appeared in the literature. Therefore, the modelling problem of classical (single layer) NCDs is addressed in this chapter, so that an understanding of the mechanisms behind their non-scaling performance can be gained. Addressing this problem is inevitable before the question of modelling 3-D narrow devices can be dealt with. Moreover, the resulting model should be applicable to the 3-D devices, with appropriate modifications. In the next section, the mechanisms that control the performance of narrow devices and are responsible for the invalidity of the conventional theory in these devices are discussed. The mechanisms that are relevant to the modelling of 3-D devices are discussed in the next chapter.

6.1 Introduction

MOS transistors have been scaled down to near micron dimensions to achieve high packing density, and speed, but small size effects resulting from this scaling are an additional source of device para-

meter variation. Such parameter variation can have severe impact on worst case circuit design rules, and therefore must be predictable. Short Channel Devices (SCDs) have been studied by several researchers [6.3-6.7]; modelling of Short Channel Effects (SCEs) is fairly mature, and therefore they are not emphasized in this study.

Narrow Channel Devices (NCDs) are currently receiving intensive study because of their importance in the production of high density MOS-VLSI circuits. It has been found that the channel width has a significant effect on device behavior [6.8, 6.9]. As the device width is made narrow, the classical MOSFET theory fails to predict accurately the behavior of these devices. This is simply because that theory is based on the Gradual Channel Approximation (GCA) [6.10], by which the device behavior is described by a one-dimensional Poisson's equation. Due to the neglect of the 2-D fields associated with the true charge distribution, the classical model fails when the channel becomes narrow. For a NCD, the electric field gradient along the width direction is no longer negligible compared to the gradient normal to the semiconductor surface, particularly at the device width edges. Therefore, the NCD problem is essentially 2-D.

The depletion layer edges under the thin and thick oxides overlap resulting in a reduced depletion layer depth under the remaining part of the thin oxide region, as can be seen in Figure 6.1. As the

Figure 6.1 Schematic device cross section for discussion of narrow-channel effects (NCEs). W is the channel width of a wide device and W_x is the width of a scaled down device.

gate bias is increased, the depletion charge under the thin oxide spreads out both vertically and laterally. However, the thin depletion layer under the thick field oxide hinders the spreading of the thin oxide depletion region at both thin thick oxide transition regions, and thus the depletion charge profiles become curved rather than being ideally square as is conventionally assumed. It follows that under small gate bias conditions the semiconductor surface near the thin thick interface, is weakly inverted, due to the behavior of the depletion layer in this region; hence the effective channel width may very well be narrower than the physical gate width, depending on the bias condition, threshold adjust and field implants, and bird's beak effect.

To bring this region into strong inversion the gate bias has to be increased, causing further lateral extension of the depletion layer charge beyond the gate width edges, an effect increased by the fringing of the electric field beyond the thin oxide region. Strong field-fringing effects, due to high gate bias, could cause semiconductor surface inversion, in which case the effective channel width exceeds the gate width, but is not inverted uniformly. Under such a condition, the drain current is expected to be higher than that predicted by scaling theory [6.11], even though the threshold voltage of a NCD is relatively higher.

In summary, the device behavior is basically controlled by the behavior of the charges in the semiconductor, as a result of the applied bias conditions. Therefore, there are two basic mechanisms that need to be studied in NCDs: the increase in threshold voltage due to the two dimensional spread of the channel depletion region beyond the nominal device width, and the increase in channel current due to exten-

sion of the channel beyond the width of the gate. So far, very little work has been done on modelling Narrow Channel Effects (NCEs); furthermore, reported approaches involve complex numerical analysis [6.12,6.13], and consequently require lengthy computing time and substantial computer memory area, and hence are economically unfeasible. Although such numerical analysis gives some insight into device mechanisms, it is not useful for device modelling in computer aided design, or for analysis which requires that device models be expressed in the simplest possible mathematical forms. Also, previous work has been focused only on modelling the threshold voltage and little attempt has been made yet to understand and model the drain current-voltage characteristics.

From the preceding discussion, it is concluded that formulation of a model for NCDs, in a simple form suitable for design purposes, is an urgent problem. Therefore, the task at hand is to develop a model for analyzing NCDs which is capable of predicting their performance reasonably accurately, over a wide range of operation, but which is still computationally and mathematically sufficiently simple for use in circuit design and circuit level simulation. This modelling problem is more complicated than that of the SCDs. The complexity stems from the fact that the depletion charge region, along the width direction, has three free boundaries, two at the device edges and the third at the depletion charge/neutral substrate boundary. These boundaries are bias dependent. The effective channel width is consequently voltage dependent.

Several 2-D numerical solutions have been reported by research groups using either finite element [6.12] or finite difference techniques [6.13]. An exact solution of this problem would require solution of the 2-D Poisson's equation, which is difficult not only because of the nonlinearity of the equation but also because of the free boundaries mentioned above.

To obtain a solution useful for CAD applications in the present work, an approximate analytical model based on simplifying assumptions is developed to avoid 2-D or 3-D analysis. This approach is applied to the derivation of analytical expressions for threshold voltage and drain current-voltage ($I_{DS} - V_{DS}$) characteristics which are simple enough for CAD.

6.2 The Proposed Model

In this section, the basic assumptions on which the new model is based are discussed, followed by derivations of expressions for the depletion, gate and inversion charges, threshold voltage and output ($I_{DS} - V_{DS}$) characteristics. Experimental verification of the threshold voltage and drain $I_{DS} - V_{DS}$ models is presented in Section 6.3. The classical theory [6.14] is also used as a reference to compare with the present model.

6.2.1 Depletion Charge Profile

Due to the NCEs, the depletion layer profile, at the thin-thick oxide interface, is curved rather than the ideal square assumed for wide/long device. The point at which the depletion charge starts to deviate from uniformity can not be specified. Either for small bias conditions where the uniform region of the depletion charge is smaller than the actual gate width, or for large bias conditions where the uniform charge region extends beyond the gate width. In order to reduce the complexity of the problem, there is assumed to be a uniform region of depletion charge, and hence of inversion charge, of width AW . The width of this "effectively uniform" region is related to the physical gate width W by the parameter A , which is assumed to be given by an empirical expression, $A = 1 - \chi/W$, where χ is a fixed distance representing the extension (or reduction) of the uniform depletion charge region relative to the nominal situation. Introducing this parameter helps not only to represent modulation of the depletion charge uniform region, but also to account for etch bias at the thin-thick oxide interface at the width edges, while W can be considered as the mask gate width. Therefore it is not necessary to know the actual

physical gate width on the wafer. The parameter A (or χ) is to be determined by matching the experimental results with the predictions of the present theory, and could be more or less than unity, depending on the bias conditions, device structural parameters and technological errors.

Having defined the uniform region, we may further assume that the depletion charge in the fringing regions is nonuniform and within a width δ , an empirical parameter that is also to be determined by matching the theory with actual device data. Figure 6.2 illustrates this representation of the device, assuming symmetry w.r.t. the center line of the width. Also, indicated is the nature of the depletion layer charge distribution implied in the model. The model developed below is based upon an approximate analytic representation of the gate electric field and surface potential, and thus gate charge and depletion charge densities, within the fringing region defined by δ .

6.2.2 Effective Gate Voltage

As shown in Figure 6.2, the polysilicon gate overlaps the thick oxide sides of the field, and the transition from the thin to the thick oxide is tapered for both the polysilicon and the oxide, rather than abrupt, as in the existing MOSFET models. This representation of the thin-thick oxide transition region is more realistic than being abrupt. To account for the field-fringing effects in the region beyond the thin oxide boundary, for narrow devices where this region becomes comparable to the gate width, an "effective" applied gate voltage*

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* All analysis throughout this chapter is carried out for an n-channel device.

Figure 6.2 A half cross section along the width of a simplified device geometry showing the actual and assumed depletion-layer profiles.

is defined. The effective gate voltage $V_{gs}(z)$ (first, the case of $V_{BS} = 0$ is considered) is such that if applied to a gate situated at a constant oxide thickness from the semiconductor, and considered to set up normal field lines, it would induce a charge density distribution approximating that in the actual device. The induced charge is basically controlled by the difference between the gate voltage and the surface potential distributions in these regions. Figure 6.3 qualitatively illustrates the distribution of these quantities for ($V_{BS} = 0$) at the width sides, while Figure 6.7 gives more detailed calculations. In actual device operation, the applied drain voltage also causes departure of the gate field from a normal configuration. This effect will however be neglected and a long channel analysis conditions will be assumed to apply. The effective gate voltage is a function of the space coordinate z . A function which satisfies the requirements that $V_{gs}(z) = 0$ at $z = AW/2 + \delta$ and $V_{gs}(z) = V_{gs}$ at $z < AW/2$, and gives an approximate distribution of the effective gate voltage between these two boundaries is assumed. This function depends upon the tapered oxide shape (assumed linear), which determines the distribution of the effective voltage in the fringing region. For a given field oxide, as δ shrinks the voltage gradient becomes steeper and steeper until, as δ approaches zero, it changes abruptly from its nominal value to zero, resembling a wide device. A form suitable for mathematical manipulation is:

$$V_{gs}(z) = V_{gs} \sin(\theta) \quad (6.1)$$

where:

Figure 6.3 The effective gate voltage and surface potential distributions at the device width sides ($V_{BS} = 0$).

$V_{gs}(z)$ = the effective gate voltage at any point along the z-direction,

V_{gs} = the applied gate-to-source voltage,

$$\begin{aligned} 0 &= \tan^{-1} \left\{ \frac{X_F - X(z)}{z - AW/2} \right\}; \\ &= \tan^{-1} \left\{ b(1/z' - 1) \right\}, \end{aligned} \quad (6.2)$$

and
$$X(z) = X_1 + \frac{(X_F - X_1)(z - AW/2)}{\delta} = X_1 + X_{F1} \cdot z',$$

where:

X_F = the thick-oxide thickness,

$z' = \frac{z - AW/2}{\delta}$ (the normalized lateral distance),

$$b = \frac{X_F - X_1}{\delta},$$

$X(z)$ = the oxide thickness at any point along the z-direction,

and X_1 = the thin oxide (gate oxide) thickness.

Expression (6.2) was chosen such that the gate fringing field at the end of the edge region (i.e., at $z' = 1$) drops off to zero, while it becomes equal to its 1-D value in the uniform region at $z' < 0$; and it gives an approximate field distribution between the two boundaries (i.e., for $0 < z' < 1$). The expression is controlled by the device geometrical and processing parameters through the normalized lateral distance z' and the parameter b . The effective gate voltage and normal field distributions in the fringing region, as obtained using the previous expression, will be presented shortly, along with the surface potential distribution, so that the validity of the expression can be examined. Substituting from (6.2) into (6.1), we obtain

$$V_{gs}(z) = V_{gs} \sin \left\{ \tan^{-1} \left(b(1/z' - 1) \right) \right\}$$

or

$$V_{gs}(z) = \frac{V_{gs}}{\left[1 + \left(\frac{1}{b(1/z' - 1)} \right)^2 \right]^{1/2}} = \lambda(z) V_{gs} ; \quad (6.3)$$

where the fringing factor $\lambda(z)$ can be written as:

$$\lambda(z) = \frac{1}{\left(1 + \left(\frac{1}{b(1/z' - 1)} \right)^2 \right)^{1/2}} . \quad (6.4)$$

At $z = AW/2$, i.e., right at the edge of uniform region ($z' = 0$), $\lambda = 1$ and hence $V_{gs}(z) = V_{gs}$. At $z = AW/2 + \delta$; $z' = 1$, i.e., at the end of the fringing region, we get:

$$V_{gs}(z) = \frac{V_{gs}}{\sqrt{1 + \infty}} = 0$$

The variation of the fringing factor, equation (6.4), between these two boundaries (i.e., $0 < z' < 1$) is illustrated in Figure 6.4. The effective gate voltage lateral distribution (w.r.t. the flatband condition) beyond the nominal width is also shown in the same figure for various values of δ , illustrating the dependence of $V_{gs}(z)$ on the fringing factor $\lambda(z)$ and on δ . The induced gate charge is mainly controlled by the difference between this voltage and the surface potential; the latter is calculated as a function of the normalized distance z' in Section 6.2.4. The consideration of an effective gate potential, beyond the uniform depletion charge region, represents the most important narrow channel effect, the fringing of the gate field, while still allowing a simple comparison with the standard model. A similar approach can be used in the general case with applied substrate bias, and is treated in Section 6.2.5.

6.2.3 The Energy Band Diagram Along the Device Width

As previously mentioned, the device width sides are conventionally assumed to have negligible effects on device characteristics. This is a valid assumption for a long/wide device. However, for a NCD, these regions have a considerable effect on its operation, and must be taken into account, as has been discussed in the preceding sections.

Figure 6.4 The fringing factor (λ) and effective gate voltage (V_{gs}) distribution as a function of the normalized lateral distance (z'). $V_{BS} = 0$, $X_1 = 400\text{\AA}$, $X_F = 7000\text{\AA}$ and $A = 1$.

Moreover, these regions play a significant role in modifying the classical energy band diagram configuration, and the charge associated with the surface potential.

The proposed model takes into consideration the modification of the energy band structure in the thin-thick oxide transition regions, which could be comparable to the gate width in very narrow devices. The energy band diagram, at flatband condition, is shown in Figure 6.5a. With a gate bias sufficient for strong inversion, it is represented conventionally as in Figure 6.5b, assuming that no drain or substrate bias is applied and the energy bands in the extrinsic device region are assumed to be at flatband condition. Considering the device width edges, as is essential for NCD modelling, the actual band diagram becomes as illustrated in Figure 6.6a. The band structure varies from the inverted semiconductor surface under the thin oxide to the uninverted surface under the thick oxide, at both device width sides.

As shown in Figure 6.6a, the difference between E_i and E_{FP} varies at both device sides while it is constant and equal to $q\phi_F$ in the uniform central region. Correspondingly, the surface band bending ($\psi_s^0(z)$) deviates from the strong inversion classical value $2\phi_F$ at both width sides (at the source end of the channel). For simplicity, a piecewise linear energy band diagram will be assumed, as can be seen from Figure 6.6b. For this configuration, the widths of the uniform and nonuniform regions are the same as those of the depletion charge region, i.e., $AW/2$ and δ respectively.

Therefore surface potential $\psi_s^0(z)$ (w.r.t. the flatband condition) at $y=0$ (source boundary) at any location z along the channel width, with no applied drain-to-source or substrate-to-source bias, is given by:

Figure 6.5 The classical energy band diagram along the device-width (P-substrate) in two cases with $V_{BS} = 0$, $V_{DS} = 0$, (a) $V_{GS} = 0$ and (b) V_{GS} applied.

(a)

(b)

Figure 6.6 The energy band diagram with $V_{BS} = 0$, $V_{DS} = 0$, $V_{GS} > 0$ and strong inversion assumed, showing its deformation at the width ends of the channel due to NCEs

(a) Actual

(b) Model

$$\psi_s^0(z) = \begin{cases} 2\phi_F + 2\left(\frac{z+AW/2}{\delta}\right) \cdot \phi_F, & \text{for } -(AW/2+\delta) < z < -AW/2 \\ 2\phi_F, & \text{for } -AW/2 < z < AW/2 \\ 2\phi_F - 2\left(\frac{z-AW/2}{\delta}\right) \cdot \phi_F, & \text{for } AW/2 < z < AW/2 + \delta. \end{cases} \quad (6.5)$$

This expression implies that the strong inversion condition in the uniform region of the channel is reached when the surface potential in this region is equal to $2\phi_F$, an assumption utilized by the classical theory, and the flatband condition applies for $(AW/2+\delta) < z < -(AW/2+\delta)$.

The $\psi_s^0(z)$ was assumed to be independent of the applied gate voltage and equal to its value at the onset of inversion in the uniform region of the channel. But, at the width edges, it decreases by $-2\phi_F \cdot \left(\frac{z-AW/2}{\delta}\right)$. For an n-channel MOSFET with applied substrate bias, the surface potential at any point z along the channel width (with respect to the intrinsic Fermi level) is taken to be:

$$\psi_s(o,y,z) = \psi_s^0(z) + \phi_n(o,y) - [1 \pm (z \pm AW/2)/\delta] V_{BS}, \quad (6.6)$$

where $\phi_n(o,y)$ equals zero at the source end of the channel, and V_{DS} at the drain. The minus sign applies when z is positive, while the positive sign applies when z is negative.

Expression (6.6) implies that the effect of V_{BS} on ψ_s drops off from its nominal value (at the edge of the uniform region) to zero at the end of the active device region (i.e., at $z' = 1$). On the other hand, the influence of $\phi_n(o,y)$ on ψ_s beyond this region is disregarded, since it is negligible when averaged across the channel length.

The total band bending with applied drain and substrate biases can now be defined along the width regions:

$$\psi_s(o, y, z) = \begin{cases} 2\phi_F + 2\left(\frac{z+AW/2}{\delta}\right) \cdot \phi_F + \phi_n(o, y) - (1+(z+AW/2)/\delta)V_{BS}, \\ \text{for: } -AW/2 > z > -(AW/2 + \delta) \\ \\ = 2\phi_F + \phi_n(o, y) - V_{BS}, \\ \text{for: } -AW/2 < z < AW/2 \\ \\ 2\phi_F - 2\left(\frac{z-AW/2}{\delta}\right) \cdot \phi_F + \phi_n(o, y) - (1-(z-AW/2)/\delta)V_{BS}; \\ \text{for: } AW/2 < z < AW/2 + \delta. \end{cases} \quad (6.7)$$

The accuracy of the assumption of linear variation of the surface potential at the channel width sides is investigated in the next section and verified by comparing the overall model results with experimental data, as will be demonstrated at the end of this chapter.

6.2.4 Discussion of the Assumptions

In the foregoing analysis, three assumptions have been made in order to develop the model, and are summarized as follows:

- (1) The width of the uniform region of the depletion layer is given by AW , where W is the nominal gate width and A is an empirical parameter dependent on W , χ being a constant value. The lateral extension of the depletion charge beyond the uniform region is given by δ .

(ii) The effects of the width edges on the surface potential are taken into account and assumed to be piecewise linear, i.e., ψ_s decreases by $2\phi_F - V_{BS}$ at the end of the edge region relative to its 1-D value in the uniform region.

(iii) The effective gate voltage beyond the gate oxide boundary, which is due to both the gate fringing field effects and gate polysilicon overlapping on the field oxide, is taken into account using a simple function capable of satisfying the physical requirements of that region and suitable for mathematical manipulation, this function is:

$$V_{gs}(z) = \frac{V_{gs}}{[1 + (\frac{1}{b(1/z - 1)})^2]^{1/2}} .$$

The validity of the assumptions, summarized above, is compared against results obtained from numerical techniques; namely, the lateral variation of the surface potential, depletion charge profile and normal interface electric field at the device edges. The distribution of the effective gate voltage (w.r.t. flatband condition) in the fringing region can be obtained using the fringing function (equation 6.4) as displayed in Figure 6.7. Illustrated in the same figure is the lateral variation of the surface potential (@ $V_{gs} = 3.5$ V), predicted using the piecewise linear assumption introduced earlier. The device geometry and parameters used are identical to those used in 2-D analysis [6.18], so that a direct comparison between the two cases can be made in order

to judge the accuracy of our assumptions. The surface potential distributions are in good agreement, depending on the value chosen for δ . The difference between the effective gate voltage $V_{gs}(z)$ and the approximate surface potential, which is responsible for inducing charges in the semiconductor, is much larger than the difference between the approximate and actual surface potentials. This difference arises from the neglect, by the present model, of the surface potential associated with the field oxide beyond the active device region (the flatband condition is assumed in this region). Such a small difference can be neglected without resulting in significant error in the calculation of the depletion charge layer. This is demonstrated in Figure 6.8, where the depletion charge profile as a function of the lateral position z is calculated, according to the linear distribution of the surface potential at the channel sides, and compared against the 2-D calculations of Chao-Ren et al. [6.18]. The depletion charge thicknesses, for several channel widths, vary in a manner similar to those obtained by Chao-Ren, except that the depletion charge according to the present model drops off to zero at $z' = 1$, i.e., at the boundary of the active device region. Also, illustrated in the same figure is the expected parallel shift of the depletion layer profile as the device width changes, while the profile remains unchanged. The only change is the width of the uniform region at the gate center. At high applied substrate bias (e.g., $V_{BS} = -11$ V) the model predicts a depletion charge depth which is about 11% larger (at the channel center) than that obtained by the 2-D analysis of Nobel et al. [6.5], although the total charge appears to be the same. This result is indicated by

Figure 6.7 The fringing factor (λ), effective gate voltage (V_{gs}) and surface potential (ψ_s) distributions as a function of the normalized lateral distance (z'). $V_{BS} = 0$, $X_1 = 400\text{\AA}$, $X_F = 7000\text{\AA}$ and $\Lambda = 1$.

Figure 6.8 Depletion charge profile as a function of lateral distance from the device center, for several device widths, $V_{BS} = 0$.

Figure 6.9, where the lateral depletion charge profile is shown. At such a large value of V_{BS} , the 2-D field distribution in the depletion region influences the middle part of the channel resulting in a depletion layer depth smaller than its 1-D value.

The validity of the fringing function can be further examined by comparing the computed fringing field with that obtained from 2-D simulation [6.5]. At the channel center (i.e., in the uniform region), the normal electric field (E_n) in the semiconductor at threshold is classically given by:

$$E_n = \frac{\epsilon_{ox}}{\chi_o \epsilon_{si}} (V_{gs} - 2\phi_f).$$

In the fringing region, V_{gs} is modified by the position dependent fringing factor $\lambda(z)$ so that an approximate effective gate voltage beyond the nominal channel width boundary can be obtained. Also, in the same region the surface potential is assumed to drop linearly from its 1-D value at the edge of the uniform region to zero at the end of the fringing region. Based on these approximations, the resulting distribution of the normal electric field at the semiconductor surface is compared in Figure 6.10 with that obtained from 2-D numerical computations [6.5]. Beyond the device uniform region, where the normal field deviates from its corresponding 1-D value in the uniform region, the lateral variation of the field is mainly determined by the choice of the parameters δ and χ and can approximate reasonably to that obtained from the 2-D computation.

Figure 6.9 Lateral depletion charge profile according to the present model and the 2-D simulation in Ref. [6.5], for $W = 2\text{ }\mu\text{m}$ ($2\text{ }\Omega\text{cm}$).

Based on the foregoing discussion, the assumptions are applicable to the analysis of narrow devices so long as the 1-D feature of the surface potential, and thus the depletion charge layer, is maintained at the width centre. However, when the 2-D effects begin to influence the middle part of the channel width the 1-D property of this region start to be distorted, and therefore the approximations stated in the previous section are not expected to apply. At this point, the fringing field penetrates significantly into the middle part of the device width, causing a reduction of the depletion charge thickness and surface potential in this region. The critical device width at which this effect takes place can be estimated by determining the device width at which the model fails to apply. As will be demonstrated at the end of this chapter (for the devices whose technological parameters are summarized in Table 6.2), the critical width appears to be smaller than $1\text{ }\mu\text{m}$, since the previous assumptions are quite adequate to predict the characteristics of devices as narrow as $1\text{ }\mu\text{m}$. On the other hand, the critical width is a complicated function of device structural and geometrical parameters, bias conditions and design rules, therefore it is expected to be strongly technology dependent.

In the next subsections, expressions for the induced device charges and the dc characteristics are derived. Initially the condition $V_{DS} = 0$ is assumed and the device charges are derived on the basis of the above assumptions, after which analysis of current flow, for $V_{DS} \neq 0$, is undertaken. In the latter, the analysis is in terms of the average gate, depletion and inversion charges across the device width, these being treated in the same manner as for the classical 1-D transistor.

Figure 6.10 Normal field distribution across a narrow device width ($w = 1 \mu\text{m}$) as predicted by the present model and by 2-D simulation [6.5]. The device is at threshold ($V_{\text{BS}} = -1 \text{ V}$).

6.2.5 Gate Charge

Having introduced the assumptions and their influence on the band energy diagram, surface band bending and the applied gate bias along the device width, the average gate charge per unit area can be expressed in the following form:

$$Q_G(y) = 2C_O \cdot M \int_0^{(AW/2+\delta)} V_O(y,z) dz, \quad (6.8)$$

where $V_O(y,z)$ is the voltage drop across the gate oxide, C_O is the oxide capacitance per unit area and $M = 1/(AW + 2\delta)$.

In the central region $-AW/2 < z < AW/2$, at strong inversion, with the intrinsic Fermi level as a reference, $V_O(y,z)$ is given by:

$$V_O(y)^v = [(V_{GS} - V_{FB}) - V_{BS}] - \psi_s(y), \quad (6.9)$$

where $\psi_s^v(y)$ is the total band bending at the semiconductor surface w.r.t. the neutral substrate, and is given by:

$$\psi_s(y) = \psi_s^0(y) + \phi_n(y) - V_{BS}.$$

Substitution for $\psi_s(y)$ in (6.9) yields:

$$V_O(y) = V_{gs} - \psi_s^0(y) - \phi_n(y) = V_{gs} - 2\phi_F - \phi_n(y), \quad (6.10)$$

where V_{gs} is the gate-to-source applied voltage (w.r.t. the flatband condition) and $\phi_n(y)$ is the channel potential w.r.t. the source boundary at the channel location of y and its values at the channel end points are given by:

$$\phi_n(y) = \begin{cases} 0 & \text{at } y = 0 \\ V_{DS} & \text{at } y = L. \end{cases}$$

Similarly, $V_o(y,z)$ in the fringing region can be written as:

$$V_o(y,z) = V_G(z) - \psi_s(y,z)$$

where $V_G(z)$ is the effective gate voltage (w.r.t. substrate) and $\psi_s(o,y,z)$ is the surface potential, defined in equation (6.6). The variation of $V_G(z)$ and $\psi_s(o,y,z)$ across the device width is illustrated in Figure 6.11. Then from equation (6.6), with $V_G(z) = V_{gs}(z) - V_{BS}(z)$, we get $V_o(y,z)$ is the same as for the case of $V_{BS} = 0$ as follows:

$$V_o(y,z) = V_{gs}(z) - \psi_s^o(z) - \phi_n(y)$$

$$= V_{gs}(z) - \left(2\phi_F - 2\phi_F \frac{(z - AW/2)}{\delta} \right) - \phi_n(y),$$

for

$$AW/2 < z < AW/2 + \delta.$$

Substituting for $V_{gs}(z)$ from equation (6.3), we obtain:

$$V_o(y, z) = \frac{V_{gs}}{\left[1 + \left[\frac{1}{b(1/z' - 1)}\right]^2\right]^{\frac{1}{2}}} - \left(2\phi_F - 2\phi_F \frac{(z - AW/2)}{\delta}\right) - \phi_n(y) . \quad (6.11)$$

Substituting from equations (6.10) and (6.11) in equation (6.8), we obtain:

$$Q_G(y) = 2C_o \cdot M \int_0^{AW/2} (V_{gs} - 2\phi_F - \phi_n(y)) dz \\ + \int_{AW/2}^{AW/2+\delta} \frac{V_{gs} dz}{\left[1 + \left[\frac{1}{b(1/z' - 1)}\right]^2\right]^{\frac{1}{2}}} \\ + \int_{AW/2}^{AW/2+\delta} \left\{ -[2\phi_F - 2\frac{(z - AW/2)}{\delta} \cdot \phi_F] - \phi_n(y) \right\} dz .$$

Thus,

$$Q_G(y, z) = 2C_o \cdot M [I_1 + I_2 + I_3], \quad (6.12)$$

where:

$$I_1 = \int_0^{AW/2} [V_{gs} - 2\phi_F - \phi_n(y)] dz = [V_{gs} - 2\phi_F - \phi_n(y)] AW/2 .$$

Figure 6.11 The lateral variation of $V_G(z)$ (a) and $\psi_s(0,y,z)$ (b) across the device width ($\phi_n(y) = 0$).

Performing the second integration as shown in Appendix A (equation 2A), yields:

$$I_2 = \frac{a \cdot V_{gs}}{A'} \left\{ \sqrt{\zeta} - 1 + \xi \left[\ln \left(\frac{(A')^{\frac{1}{2}} - 1}{(A'\zeta)^{\frac{1}{2}} + A' - 1} \right) \right] \right\}.$$

Also

$$I_3 = \int_{AW/2}^{AW/2+\delta} \left[- \left(2\phi_F - 2 \left(\frac{z-AW/2}{\delta} \right) \cdot \phi_F \right) - \phi_n(y) \right] dz,$$

$$= \delta [-\phi_F - \phi_n(y)].$$

Substituting for I_1 , I_2 and I_3 in equation (6.12), we obtain:

$$Q_G(y) = C_o \cdot M \cdot \left[(V_{gs} - 2\phi_F - \phi_n(y)) (AW) + \frac{2a \cdot V_{gs}}{A'} x \right. \\ \left. \left\{ \sqrt{\zeta} - 1 + \xi \left[\ln \left(\frac{(A')^{\frac{1}{2}} - 1}{(A'\zeta)^{\frac{1}{2}} + A' - 1} \right) \right] \right\} + 2\delta (-\phi_F - \phi_n(y)) \right], \quad (6.13)$$

where

$$a = X_F - X_1,$$

$$\xi = \frac{1}{\sqrt{\left(\frac{X_{F1}}{\delta} \right)^2 + 1}},$$

$$\zeta = (X_{F1}/\delta)^2 ,$$

$$A' = \left(\frac{X_{F1}}{\delta}\right)^2 + 1 ,$$

and $C_o = \epsilon_{ox}/X_1.$

6.2.6 Depletion Charge

The average depletion charge per unit area created by the potential at the silicon surface can be expressed as:

$$Q_D(y) = -M \int_{\text{width}} \int_0^{\psi_s} C_D(z) d\psi_s dz ,$$

where ψ_s is the previously defined surface potential and C_D is the depletion layer capacitance per unit area. Using the previously assumed linearized energy band diagram to define ψ_s and integrating over the width yields

$$\begin{aligned} Q_D(y) = -2 \cdot M \left\{ \int_0^{AW/2} \int_0^{\psi_s} \frac{\epsilon_s}{x_D} d\psi_s dz \right. \\ \left. + \int_{AW/2}^{AW/2+\delta} \int_0^{\psi_s} \frac{\epsilon_s}{x_D} d\psi_s dz \right\} = (I_4 + I_5) , \end{aligned} \quad (6.14)$$

where x_D is the depletion charge depth under the channel.

Performing the integrations I_4 and I_5 , assuming a uniform substrate doping, as shown in Appendix B (equations 1B and 2B), the value of the depletion charge per unit area can be expressed as:

$$Q_D(y) = -K' \cdot M \{ AW[2\phi_F + \phi_n(y) - V_{BS}]^{\frac{1}{2}} + \alpha [[2\phi_F + \phi_n(y) - V_{BS}]^{\frac{3}{2}} - [\phi_n(y)]^{\frac{3}{2}}] \} , \quad (6.15)$$

where:

$$\alpha = 4\delta/3(2\phi_F - V_{BS}),$$

$$M = 1/(AW + 2\delta) \text{ and}$$

$$K' = (2\epsilon_s q N_A)^{\frac{1}{2}} .$$

In obtaining this expression, the additional depletion charge associated with the field regions at the device width sides has been considered. So that, a geometry, technology, and substrate bias dependent expression has been achieved. The depletion charges associated with the source/drain junctions are neglected in this expression, since the device under consideration is long and can be modelled by long channel analysis.

Two terms can be identified in equation 6.15: the first term is the standard long/wide device expression, while the second term represents the additional depletion charge in the field region, created by the fringing field. For a wide device $\alpha.M$ becomes very small and the expression is reduced to the standard form.

6.2.7 Inversion Charge

The overall charge neutrality condition requires that the summation of the gate, depletion and inversion charges be equal to zero, i.e.,

$$Q_G(y) + Q_D(y) + Q_m(y) = 0. \quad (6.16)$$

The Q's are in units of charge per unit area. From equation (6.16), an expression for the inversion charge can be easily obtained:

$$Q_m(y) = -Q_G(y) - Q_D(y).$$

Substituting for $Q_G(y)$ and $Q_D(y)$, from equations (6.13) and (6.15), the resulting mobile charge per unit area becomes:

$$\begin{aligned} Q_m(y) = & -C_o \cdot M \left[(V_{gs} - 2\phi_F - \phi_n(y)) (AW) + \frac{2a \cdot V_{gs}}{A'} [(\zeta)^{\frac{1}{2}} - 1 \right. \\ & + \xi \left\{ \ln \left(\frac{(A')^{\frac{1}{2}} - 1}{(A' \cdot \zeta)^{\frac{1}{2}} + A' - 1} \right) \right\} + 2\delta (-\phi_F - \phi_n(y)) \\ & - \frac{K'}{C_o} \left\{ (AW) \left[(2\phi_F + \phi_n(y) - V_{BS})^{\frac{1}{2}} + \alpha (2\phi_F + \phi_n(y) - V_{BS})^{3/2} \right. \right. \\ & \left. \left. - (\phi_n(y))^{3/2} \right] \right\} \right]. \quad (6.17) \end{aligned}$$

For a conventional wide device, this expression is reduced to:

$$Q_m(y) = -C_o \left\{ (V_{gs} - 2\phi_F - \phi_n(y)) - \frac{K'}{C_o} (2\phi_F + \phi_n(y) - V_{BS})^{\frac{1}{2}} \right\},$$

which is the standard inversion charge expression.

6.2.8 Threshold Voltage Model

In NCDs, the effects associated with the distribution of the depletion and inversion charges cause a threshold voltage increase, since the edge region requires a higher applied gate voltage to begin conduction than in the middle region under the gate. Since the threshold voltage is the most important electrical MOSFET parameter, it has been almost the only consideration in modelling narrow devices so far. In this section, an analytical model for the threshold voltage as a function of the gate width is developed. Following the classical theory, the threshold voltage is defined as the value of the gate voltage for which the average inversion charge across the width is equal to zero, at the source end of the channel [i.e., $\phi_n(y) = 0$]. Thus, setting $Q_m(y)$ to zero in equation (6.17) yields

$$V_{gs} \left[AW + \frac{2a}{A'} \left\{ (\zeta)^{\frac{1}{2}} - 1 + \epsilon \left[\ln \left(\frac{(A')^{\frac{1}{2}} - 1}{(A'\zeta)^{\frac{1}{2}} + A' - 1} \right) \right] \right\} \right] \\ = 2\phi_F(AW + \delta) + \frac{K'}{C_o} [AW (2\phi_F - V_{BS})^{\frac{1}{2}} + \alpha (2\phi_F - V_{BS})^{3/2}],$$

where $V_{gs} = V_{GS} - V_{FB}$, and V_{GS} is the applied gate-to-source voltage.

Setting $V_{GS} = V_T$ and rearranging the expression, we obtain:

$$V_T = V_{FB} + \frac{1}{S} \left\{ 2\phi_F (AW + \delta) + \frac{K'}{C_o} [AW (2\phi_F - V_{BS})^{\frac{1}{2}} \right. \\ \left. + \alpha (2\phi_F - V_{BS})^{3/2}] \right\}, \quad (6.18)$$

where:

$$S = AW + \frac{2a}{A'} \left[(\zeta)^{\frac{1}{2}} - 1 + \xi \left[\ln \left(\frac{(A')^{\frac{1}{2}} - 1}{(A' \cdot \zeta)^{\frac{1}{2}} + A' - 1} \right) \right] \right]. \quad (6.19)$$

The expression given by (6.18) is valid for both n- and p-channel devices and is geometry, technology and substrate-bias dependent. For standard long/wide devices, the factor S approaches AW, while δ/S and α/S approach zero, reducing equation (6.18) to the classical theory, given by:

$$V_T = V_{FB} + 2\phi_F + \frac{K}{C_o} (2\phi_F - V_{BS})^{\frac{1}{2}}. \quad (6.20)$$

However, for NCDs, the factor S is small and becomes larger as the device is made wider. In the expression for V_T , (6.18), the narrow channel effects on the depletion charge are also taken into account, resulting in an expression that predicts the correct trend of the NCDs threshold voltage, as will be demonstrated later. This expression also considers a linear variation of the surface potential in the edge regions.

The parameters A, which is width dependent and may be larger or smaller than unity by χ/W (where χ is a constant value) and δ are expected to be strongly technology dependent and used to account for the NCEs and to compensate for errors introduced by the assumptions made. The values of these parameters can be determined by matching the

actual device data with the simulation results and are fixed for a certain technology. To demonstrate the validity of equation (6.18), it is compared against published theoretical and experimental threshold voltage data, for a wide range of channel widths and applied substrate bias, in Section 6.3. Derivation of the drain current expression is carried out in the subsequent section.

6.2.9 Drain Current-Voltage Characteristics Model

The drain current in n-channel MOSFETs is attributed to a flow of electrons along the channel length parallel to the semiconductor surface. Assuming current flow to be predominantly by drift, flowing in a thin channel "sheet", the potential difference across any differential element dy within the surface inversion layer is given by:

$$d\phi_n(y) = I_{DS} \cdot dR = - \frac{I_{DS} dy}{Q_m(y,z) \mu_n(y) W'(y)},$$

where dR is the differential resistance of an element of the channel, $W'(y)$ is the "effective" channel width, which may be different from the depletion layer width and is dependent upon the applied terminal voltages and therefore varies along the channel. At small gate bias, only the middle part of the channel is inverted, but at large gate biases the inversion region will spread beyond the nominal device width. Therefore, $W'(y)$ is expected to be gate bias dependent. This mechanism has, alternatively, been modelled by introducing an effective applied gate voltage ($V_{gs}(z)$), as discussed in Section 6.2.2. Also, the

applied drain voltage (V_{DS}) modulates the normal field set up by the gate voltage, a mechanism that results in a reduction of the effective channel width at the width edges adjacent to the drain end of the channel and thereby tends to reduce I_{DS} in the triode region. Such a mechanism can be modelled by assuming a drain bias dependent effective channel width, as will be discussed later. Also, V_{DS} results in an additional depletion charge created at the width edges at the drain side of the channel. This effect has been accounted for in the derivation of the depletion charge expression as can be concluded by examining equation (6.15). In narrow devices the effective channel width is sensitive to the process parameters, design rules and is most sensitive to substrate bias (V_{BS}); this mechanism will be dealt with later. At this point, a 1-D average effective channel-width W' is assumed, shortly the physical basis of determining a function that describes the dependence of W' on the device biasing conditions will be explained and later an expression for W' will be obtained by matching simulation results with device characteristics. Introducing W' in this way makes the following analysis effectively 1-D.

Applying these assumptions, the drain current can be expressed

as

$$I_{DS} \cdot L \cdot \frac{1}{L} \int_0^L \frac{1}{\mu_n(y)} dy = -W' \int_{\phi_n(0)=V_s}^{\phi_n(L)=V_{DS}} Q_m(y) d\phi_n(y), \quad (6.21)$$

where

$$\frac{1}{L} \int_0^L \frac{1}{\mu_n(y)} dy = \frac{1}{(\mu_n)_{av}} = \frac{1}{\mu_n},$$

and μ_n is the average electron surface mobility. Incorporating μ_n in equation (6.21) yields:

$$I_{DS} = - \frac{\mu_n W'}{L} \int_{\phi_n(0)=V_S}^{\phi_n(L)=V_{DS}} Q_m(y) d\phi_n(y). \quad (6.22)$$

In this integration, it is assumed that $d\phi_n/dy$ is constant in the x -direction, i.e., there is no current perpendicular to the semiconductor surface. From the analysis presented in Section 6.2.7, the integrand Q_m is given by equation (6.17).

Substitution for Q_m and integration of the current continuity equation from source ($y=0$) to drain ($y=L$), equation (6.22), results in an expression for the drain current, which is valid only in the triode region, as follows:

$$\begin{aligned} I_{DS} = K_3 \int_{\phi_n(0)=0}^{\phi_n(L)=V_{DS}} \{ & (V_{GS} - V_{FB} - 2\phi_F - \phi_n(y)) AW + A_4 S_6 \\ & + A_5 (-\phi_F - \phi_n(y)) \\ & - K [AW (2\phi_F + \phi_n(y) - V_{BS})^{\frac{1}{2}} \\ & + \alpha [(2\phi_F + \phi_n(y) - V_{BS})^{\frac{3}{2}} \\ & - (\phi_n(y))^{\frac{3}{2}}] \} d\phi_n(y), \end{aligned} \quad (6.23)$$

This expression is based on the consideration of an effective gate voltage in the fringing region and consequently a lateral position dependent gate charge. The depletion charge corresponds to a change in the surface potential by V_{DS} along the channel length; and by $(2\phi_F - V_{BS})$ in the width edge regions, relative to its 1-D value in the uniform region of the width. Furthermore, incorporated in the expression is an average effective channel width (W') which is independent of the space coordinate y . Also, the electron surface mobility is assumed, at this point, field independent but the dependence of mobility on the normal component of the field will be considered later. Evaluation of the integration in equation (6.23) from the source to the drain leads to the following expression for the drain current:

$$\begin{aligned}
 I_{DS} = K_3 \{ & [(V_{GS} - V_{FB}) AW - \phi_F (2AW + A_5) + A_4 S_6 \\
 & - (AW + A_5) \frac{V_{DS}}{2}] V_{DS} - K \left\{ \frac{2AW}{3} [(2\phi_F + V_{DS} - V_{BS})^{3/2} \right. \\
 & - (2\phi_F - V_{BS})^{3/2}] + \frac{2\alpha}{5} [(2\phi_F + V_{DS} - V_{BS})^{5/2} \\
 & \left. - (2\phi_F - V_{BS})^{5/2} - (V_{DS})^{5/2}] \right\} \}. \quad (6.24)
 \end{aligned}$$

where:

$$A_4 = \frac{2a \cdot V_{gs}}{A'},$$

$$S_6 = \zeta^{\frac{1}{2}} - 1 + \xi \left[\ln \left(\frac{(A')^{\frac{1}{2}} - 1}{(A'\zeta)^{\frac{1}{2}} + A' - 1} \right) \right],$$

$$A_5 = 2\delta,$$

$$\alpha = 4\delta/3(2\phi_F - V_{BS})$$

$$a = X_{F1} - X_F - X_1,$$

$$A' = [(X_{F1}/\delta)^2 + 1],$$

$$K_3 = \frac{\mu_n C_{ox} W'M}{L},$$

$$K = (2\epsilon_S q N_A)^{\frac{1}{2}} / C_{ox},$$

$$C_{ox} = \epsilon_{ox} / X_1.$$

The first term in the previous equation is the standard surface potential expression, but modified to account for the effect of the device width edges, as discussed in Section 6.2.3. The second term

exists in most of the existing models. The third term arises as a consequence of the NCEs on I_{DS} , which were accounted for in the expression for the bulk depletion charge. For wide channel devices, expression (6.24) necessarily approaches that of the standard theory. The NCEs become negligible contributions to the drain current, and the factors $A_5 \cdot M$, $A_4 \cdot M$ and $\alpha \cdot M$ approach zero, resulting in the classical long/wide device drain current expression:

$$I_{DS} = K_4 \left\{ (V_{GS} - V_{FB} - 2\phi_F - V_{DS}/2) V_{DS} - \frac{2K}{3} [(2\phi_F + V_{DS} - V_{BS})^{3/2} - (2\phi_F - V_{BS})^{3/2}] \right\} \quad (6.25)$$

where:

$$K_4 = \frac{\mu_n C_{ox} W'}{L}$$

The effective channel width W' is expected to be strongly dependent on device geometry, processing parameters and biasing conditions. In the case of wide devices, W' must necessarily approach the nominal width W , since the narrow effects become insignificant. In narrow devices, the drain field (in the drain section of the channel) modulates the normal field induced by the gate, resulting in weak inversion of the semiconductor surface at the device edges and thereby reduces W' . As a result W' tapers off along the channel, being wider at the source than at the drain. Such a mechanism is particularly strong in narrow/short

devices. With applied substrate voltage, the degree of inversion at the width edges is further reduced making the narrow width effect more prominent; at high substrate voltage this mechanism penetrates into the uniform central region of the channel, as demonstrated by the 2-D analysis of Nobel [6.5], resulting in a significant shrinkage of W' . However, the gate field fringing effects tends to widen W' as a consequence of spreading the inversion layer beyond the nominal width, an effect that increases with increasing V_{GS} due to the increasing fringing field. The dependence of W' on the structural and processing parameters can be represented in an expression for W' through the parameters A and δ .

An expression for W' that combines all the mechanisms mentioned above can now be introduced by the following empirical function.

$$W' = \frac{AW + F_1(\delta, W)}{1 + F_2(V_{GS}, V_{BS}, V_{DS}, W)} \quad (6.26)$$

The function F_1 is expected to represent the deviation of W' from AW , without substrate bias applied, at low values of V_{DS} , while F_2 represents the effect of V_{BS} , V_{GS} and V_{DS} on W' . These functions must necessarily approach zero when expression (6.26) is applied to a wide device, resulting in an effective width equivalent to the nominal width (W).

The functional dependence of W' on the bias conditions and the parameters A and δ will be determined in Section 6.3.2 by matching theory with experimental device data. A strong dependence of W' on V_{BS} is expected due to strong body effects in narrow devices; these effects will be discussed in more detail in Section 6.3.2.

Now, the electron field dependent surface mobility (μ_n) can be incorporated in the drain current expressions (6.24) and (6.25), to account for the mobility degradation caused by the field normal to the semiconductor surface. Under large drain voltage conditions the potential along the channel $\phi_n(y)$ will vary significantly leading to a significant modulation of the normal surface field. This mechanism can be represented by using an average mobility based on an average normal surface field along the channel. The average normal field (E_n) at a given drain bias can be defined as:

$$E_n = \frac{\int_0^{V_{DS}} Q_G(y) d\phi_n(y)}{\epsilon_{s1} \cdot V_{DS}}.$$

Substitution for $Q_G(y)$ (equation 6.13) yields:

$$E_n = K_5 \left[V_{gs} \cdot AW \gamma \phi_F (2AW + A_5) + A_4 S_6 - (AW + A_5) \frac{V_{DS}}{2} \right], \quad (6.27)$$

where $K_5 = C_0/\epsilon_{s1}$. Hoenesien et al. [6.15] and D. Forman-Bentchkowsky [6.16] used a similar expression in analyzing small size devices, except that the present expression accounts for the fringing fields, by considering an effective gate voltage, and the variation of the surface potential (by $2\phi_F$) across the width sides of the channel. The surface

potential decrease in these regions causes an increase in the normal field. The average field dependent mobility is assumed given by the following well known function:

$$\mu_n = \frac{\mu_{no}}{1 + \gamma E_n} \quad (6.28)$$

The coefficient γ is used to model mobility degradation, where μ_{no} is the low field mobility. Expression (6.28) is adequate, as proven later, to describe the dependence of the mobility on the normal field.

The drain current expression given by equation (6.24) is valid only below saturation, i.e. in the triode region. In this regime I_{DS} increases in response to V_{DS} until it reaches a point where I_{DS} remains constant with further increase in V_{DS} . In the foregoing analysis, it is assumed that beyond saturation the drain resistance becomes infinite, while the drain current remains constant at a value equal to that reached at the onset of saturation.

An expression for the drain voltage, at which the drain current saturates or alternatively the channel is "pinched off", may be generated by setting the first partial derivative of equation (6.24) w.r.t. V_{DS} to zero as follows:

$$\left. \frac{\partial I_{DS}}{\partial V_{DS}} \right|_{V_{DS} = V_{DSat}} = 0$$

$$\begin{aligned}
& K_3 \{ [V_{gs} \cdot S - \phi_F (2AW + A_5) - (AW + A_5) V_{Dsat}] \\
& - KAW (2\phi_F + V_{Dsat} - V_{BS})^{\frac{1}{2}} \\
& - K\alpha [(2\phi_F + V_{Dsat} - V_{BS})^{3/2} \\
& - (V_{Dsat})^{3/2}] \} = 0 .
\end{aligned} \tag{6.29}$$

After mathematical manipulation, equation (6.29) becomes:

$$M_1 x^5 + M_2 x^4 + M_3 x^3 + M_4 x^2 + M_5 x + M_6 = 0 , \tag{6.30}$$

where x , M_1 , M_2 , M_3 , M_4 , M_5 and M_6 are defined as follows:

$$x = V_{Dsat} + 2\phi_F - V_{BS} ,$$

$$M_1 = 4 \left(\frac{AW + A_5}{\alpha K} \right)^2 ,$$

$$M_2 = - \left[8 \frac{(AW + A_5)}{(\alpha K)^2} G_1 + 12 \left(\frac{AW + A_5}{\alpha K} \right)^2 (2\phi_F + V_{BS}) \right] - C_1^2 ,$$

$$M_3 = \frac{4 G_1^2}{(\alpha K)^2} + 24 \frac{(AW + A_5) (2\phi_F + V_{BS}) G_1}{(\alpha K)^2} + 12 \left(\frac{AW + A_5}{\alpha K} \right)^2 x$$

$$(2\phi_F + V_{BS})^2 - 2 C_1 C_2 ,$$

$$M_4 = \frac{-12 (2\phi_F + V_{BS})}{\alpha K} \left[\frac{G_1^2}{\alpha K} + 2 \left(\frac{AW + A_5}{\alpha K} \right) G_1 (2\phi_F + V_{BS}) + \frac{1}{3\alpha K} \right. \\ \left. (AW + A_5)^2 (2\phi_F + V_{BS})^2 \right] - 2C_1 C_3 - C_2^2 ,$$

$$M_5 = 12 \left(\frac{2\phi_F + V_{BS}}{\alpha K} \right)^2 G_1 \left[G_1 + \frac{2}{3} (AW + A_5)(2\phi_F + V_{BS}) \right] - 2 C_2 C_3 ,$$

$$M_6 = -4 \frac{(2\phi_F + V_{BS})^3 G_1^2}{(\alpha K)^2} - C_3^2 ,$$

$$G_1 = V_{gs} \cdot S - (AW + A_5) V_{BS} + \phi_F A_5 ,$$

$$S = (AW + \frac{2a}{A_1} S_6) ,$$

$$C_1 = \frac{2AW}{\alpha} + 3 (2\phi_F + V_{BS}) - \left(\frac{AW + A_5}{\alpha K} \right)^2 ,$$

$$C_2 = \left(\frac{AW}{\alpha} \right)^2 - 3 (2\phi_F + V_{BS})^2 + 2 \left(\frac{AW + A_5}{\alpha K} \right) \left(\frac{G_1}{\alpha K} \right) \quad \text{and}$$

$$C_3 = (2\phi_F + V_{BS})^3 - \left(\frac{G_1}{\alpha K} \right)^2 .$$

To obtain an expression for x and hence for V_{Dsat} , equation (6.30) must be solved explicitly for x . An analytical solution to a fifth degree polynomial is not generally possible [6.17]. However, an efficient numerical solution can be obtained using the bisection method [6.17] in about ten iterations. In the worst case the error in the value of V_{Dsat} will not exceed 0.1%, which is acceptable in all

practical applications of MOSFETs. Equation (6.30) can be reduced to a 4th degree polynomial by Taylor series expansion of the third term in Equation (6.29), and consideration of the significant terms only. This is a good approximation because the parameter α is small and is particularly reasonable if the gate oxide thickness or the substrate doping is small (e.g., $X_o < 500 \text{ \AA}$ & $N_A < 2 \times 10^{15} \text{ cm}^{-3}$). The simplified equation can be written as follows:

$$\begin{aligned}
 & A_1^2 y^4 + 2 A_1 B y^3 + [2 A_1 C - B^2 - (2KAWZ_2)^2] y^2 \\
 & + [2 BC - (2KAWZ_2)^2 \cdot (2\phi_F - V_{BS})] y + C^2 - (2KAWZ_2)^2 \\
 & 2\phi_F V_{BS} = 0 \quad (6.31)
 \end{aligned}$$

where:

$$y = V_{DS} - V_{BS},$$

$$A_1 = (AW + A_5)^2,$$

$$\begin{aligned}
 B = & [-2 (V_{gs} \cdot S - \phi_F \cdot (2AW + A_5) - (AW + A_5) V_{BS}) (AW + A_5) \\
 & - (KAW)^2 - (\frac{3}{2} K \alpha (2\phi_F - V_{BS}))^2]
 \end{aligned}$$

$$\begin{aligned}
 C = & [(V_{gs} \cdot S - \phi_F \cdot (2AW + A_5) - (AW + A_5) V_{BS})^2 - 2 (KAW)^2 \\
 & \phi_F - \frac{3}{2} K \alpha (2\phi_F - V_{BS})^2 V_{BS},
 \end{aligned}$$

$$Z_2 = \frac{3}{2} K \alpha (2\phi_F - V_{BS}),$$

and A_5 , S , K , V_{gs} and α are as defined earlier.

6.3 Results and Analysis

In this section, the models for the threshold voltage and the device output characteristics ($I_{DS} - V_{DS}$) are compared against actual data, for a wide range of device widths and bias conditions. The inapplicability of the standard theory to the analysis of the drain current of narrow devices is also clearly demonstrated.

6.3.1 Threshold Voltage

The results shown in Figures 6.12 through 6.17 demonstrate the dependence of the threshold voltage (V_T) on device parameters. The experimental V_T data were obtained from n-channel devices whose technological parameters are given in Table 6.1 [6.19]. The V_T was determined by linear extrapolation to the gate voltage axis from a plot of channel conductance versus gate voltage, while V_{DS} was kept constant at 100 mV, for different values of V_{BS} . Illustrated in Figure 6.12 is the dependence of V_T on channel width, where the results from the present model are compared with measurements and a theory from Ref. [6.19] for channel widths ranging from 20 to 2 μm . The threshold voltage increases as the channel width is reduced and the rate of change increases with increasing the substrate doping (N_A). Using the same values of A and δ , the model also predicts a strong dependence of V_T on N_A , as shown by the same figure. In general, in all n-channel MOSFETs V_T increases as N_A increases; however, for NCDs the gradient of V_T (as a function of channel width) increases with increasing N_A because the depth of the depletion charge layer under the channel decreases and consequently NCEs become more pronounced. The present model shows general agreement with that in Ref. [6.19]. The former model exhibits superior agreement with the experimental data in some cases; see for example, Figure 6.12 at $N_A = 1.71 \times 10^{16} \text{ cm}^{-3}$ and $W = 2 \mu\text{m}$. The para-

Figure 6.12 Threshold voltage versus channel width with the substrate doping (N_A) as a parameter ($V_{BS} = 0$).

Figure 6.13 Threshold voltage as a function of applied substrate bias

$$(V_{BS}) \cdot N_A = 1.55 \times 10^{16} \text{ cm}^{-3} \text{ and } W = 2.1 \text{ } \mu\text{m}.$$

Figure 6.14 Threshold voltage versus device width for four models.

Curve 1, Akers's model with $\alpha = 1$ [6.20], curve 2, Model in Ref. [6.19], curve 3, Merckel's model [6.21], and x refers to the present model. $N_A = 1.25 \times 10^{16} \text{ cm}^{-3}$ and $V_{BS} = 0$.

Figure 6.15 Threshold voltage versus channel width, with the gate oxide thickness as a parameter ($V_{BS} = 0$).

Figure 6.16 Threshold voltage versus channel width as a function of the parameter δ ($V_{BS} = 0$).

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Figure 6.17 Comparison between the accuracy of the present model and the 2-D analysis in Ref. [6.12]. $X_I = 500\text{\AA}$, $X_P = 0.8\text{ }\mu\text{m}$, $N_A = 2.5 \times 10^{16}\text{ cm}^{-3}$, $\delta = 1.1\text{ }\mu\text{m}$ and $A = 1$.

Table 6.1 Device parameters used in obtaining the simulation results in Figures 6.12 through 6.16, taken from Ref. [6.19].

(n-channel polysilicon gate MOSFETs)

Parameter	Value	Units
X_1	395.0	$\text{\AA}$
X_F	0.7	μm
L	20	μm
W	2 to 20	μm
N_A	$1.25 \text{ to } 1.71 \cdot 10^{16}$	cm^{-3}
A	1	-
δ	1.55	μm

meters A and δ were obtained by matching the model predictions with those obtained from experiment, so that good matching could be obtained. It was found that setting the parameter A equal to unity (i.e., $\chi = 0$) was quite adequate, i.e., simulation results were obtained by choice of δ only. All the parameters used in obtaining the simulation results of Figures 6.12 through 6.16 are given in Table 6.1, unless otherwise stated or given in the figure. The strong dependence of V_T on channel width is due to an extra depletion charge associated with device width edges and consequently weak inversion of the semiconductor surface as one moves away from the device center. Such a mechanism is more pronounced with an increase in V_{BS} which results in more additional depletion charge in both the uniform and fringing regions. To bring about strong inversion in these regions the applied gate voltage must be increased resulting in higher values of V_T . This effect is clearly demonstrated in Figure 6.13, where the proposed model shows excellent agreement with the experimental data for a wide range of substrate bias ($V_{BS} = 0$ to -4.5 V). Displayed in Figure 6.14 is a comparison among three threshold voltage models from the literature [6.19-6.21] and the present model. The latter model compares favourably with the experimental data and the model in Ref. [6.19]. However the models of Akers [6.20] and Merckel [6.21] exhibit significant deviation from the experimental data. Akers's model overestimates the values of V_T ; this is believed to be due to the consideration of a square additional depletion charge region beyond the nominal MOSFET width. Merckel's model assumes a triangular region of width equals to the depletion layer thickness in the bulk, which results in an underestimation of V_T .

The present model also predicts the correct trend of V_T for various gate oxide thicknesses, as demonstrated in Figure 6.15. The V_T shows a strong dependence on δ as illustrated by Figure 6.16; V_T increases as δ increases and approaches that of a wide device as δ decreases. Under such a condition, the contributions to V_T resulting from the surface potential variation, additional depletion charge, and fringing field at the width edges become insignificant, resulting in values for V_T similar to those of wide devices.

Buturla and Cottrell [6.12] have used a two dimensional finite element analysis technique to investigate the threshold voltage behavior for narrow/long channel devices. Figure 6.17 provides a comparison between their simulation and experimental results, and the predictions of the present V_T model using their device technological parameters and values for the parameters δ and A equal to $1.1 \mu\text{m}$ and unity, respectively. As clearly indicated by this figure, the accuracy of the present model is comparable to theirs for narrow devices, but superior in case of wide devices, with the advantage that the present model is much simpler.

6.3.2 Drain Current-Voltage Characteristics

The $I_{DS} - V_{DS}$ model developed in section 6.2.9 is intended to be applied to both narrow and wide devices. It is presented in a simple analytical closed form and based on long channel theory approximations. The model is characterized by: 2-D evaluation of the device charges, application of the charge neutrality condition in the direction normal to the semiconductor surface and the mobility dependence on the normal

field. All the expressions incorporated in this model are geometry dependent which makes them approach those of long/wide device theory.

The validity of the present drain current-voltage model is demonstrated in Figures 6.18 through 6.25 for a wide range of bias conditions. The MOSFET parameters adopted in obtaining the theoretical results are given in Table 6.2, unless otherwise stated or given in the figure. The electron surface mobility dependence on the normal field has been assumed to be given by the function $\mu_{no}/(1 + \gamma E_n)$, E_n being the average field component normal to the surface. In determining the mobility function, the model was applied to a large geometry device (Figure 6.18) and a value for μ_{no} was chosen to give a good fit at low V_{GS} , and γ was chosen to achieve a good overall match between the theory and experiment. In the simulation results demonstrated in this section, values of $1.0 \times 10^{-6} \text{ V}^{-1} \cdot \text{cm}$ and $640 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ were used for γ and μ_{no} , respectively. These values were kept constant in obtaining all the other results in this section.

In the present model the effective channel width (W') dependence on the terminal voltages and the parameters A and δ can be determined, by matching simulation results with actual device performance. Initially, the function F_1 in Expression 6.26 was determined so that the simulation results fit the actual data of wide ($50 \mu\text{m}$) and narrow ($1 \mu\text{m}$) devices, while V_{DS} was kept at a small value and V_{BS} equals zero. Having arrived at an expression for F_1 , the dependence of F_2 on the bias conditions was determined; first, at large values of V_{DS} (with $V_{BS} = 0$) then the dependence of F_2 on V_{BS} was examined, so that an overall good fit could be obtained. It has been found possible to do this with the following empirical function:

$$W' = \frac{AW + 2\delta/(W)^{1/2}}{1 + 0.75 (V_{BS}^{1.2}/(V_{GS} \cdot W^{1/2})) + 0.005 V_{DS}/W} \quad (6.32)$$

This expression holds for devices with nominal channel width ranging from 1 to 50 μm and for a wide range of operating conditions. As demonstrated by the expression (6.32), W' is more sensitive to the substrate bias than to the drain bias, indicative of strong body effects in NCDs as discussed earlier. As V_{BS} increases, W' shrinks as a result of weak inversion of the semiconductor surface at the width edges, a mechanism enhanced by an increase in V_{DS} . In obtaining the simulation results (Figures 6.18 through 6.25) a value of A equals unity has been used, with the value of δ given in Table 6.2. The validity of the expression for W' is demonstrated by Figures 6.18 through 6.25 in which the calculated results using this expression exhibit good agreement with actual drain current measurements for all practical biasing conditions.

Figures 6.18 and 6.19 demonstrate the applicability of the model to long/wide devices and provides a comparison between the classical model and the present one, with and without substrate bias. The drain characteristics for narrow devices with channel width of 2 and 1 μm , as calculated by the model, are compared with experimentally measured data in Figures 6.20 through 6.25. As can be seen in these figures, the model is capable of simulating the performance of narrow devices down to 1 μm reasonably accurately in both the linear and saturation modes of operation.

Figure 6.18 Simulated and experimental characteristics of a long/wide channel MOSFET with $L \times W = 50.3 \times 50 \mu\text{m}^2$ ($V_{BS} = 0$).

Figure 6.19 Same as in Figure 6.18, but with applied substrate bias of -2 V.

Figure 6.20 Modelled and measured $I_{DS} - V_{DS}$ characteristics of a long/narrow MOSFET with $L \times W = 50.3 \times 2 \mu\text{m}^2$ ($V_{BS} = 0$).

Figure 6.21 Same as in Figure 6.20 ($L \times W = 50.3 \times 2 \mu\text{m}^2$), but with applied substrate bias of -2 V .

Figure 6.22 Simulated and measured $I_{DS} - V_{DS}$ characteristics of a long/narrow MOSFET with $L \times W = 50.3 \times 1 \mu\text{m}^2$ ($V_{BS} = 0$).

Figure 6.23 Same as in Figure 6.22 ($L \times W = 50.3 \times 1 \mu\text{m}^2$), but with applied substrate bias of -1 V .

Figure 6.24 Same as in Figure 6.22 ($L \times W = 50.3 \times 1 \mu\text{m}^2$), but with applied substrate bias of -2 V .

Figure 6.25 Same as in Figure 6.22 ($L \times W = 50.3 \times 1\text{ }\mu\text{m}^2$), but with applied substrate bias of -5 V .

Table 6.2 Device parameters used in obtaining the simulation results in Figures 6.18 through 6.25.

(n-channel, n^+ doped polysilicon gate MOSFETs)

Parameter	Value	Units
μ_{no}	640.0	$\text{cm}^2 \cdot \text{v}^{-1} \cdot \text{s}^{-1}$
γ	$1.0 \cdot 10^{-6}$	$\text{cm} \cdot \text{v}^{-1}$
x_j	0.3	μm
x_l	1067.0	$\text{\AA}^\circ$
x_F	0.5	μm
Q_{SS}/q	$5.0 \cdot 10^{10}$	cm^{-2}
L	50.3	μm
W	1.0 to 50.0	μm
N_A	$2.3 \cdot 10^{15}$	cm^{-3}
ϕ_{MS}	0.7	v
A	1	-
δ	0.23	μm

For zero substrate bias, the classical theory underestimates the drain current of these devices (see Figure 6.22 in particular) despite relatively a higher threshold voltage for NCDs. This effect becomes significant (in the linear region) as V_{GS} increases, indicative of an increase in the effective channel width (W') as compared to the nominal width. The increase in W' is a consequence of the fringing field effects around the width edges, an effect which is partially compensated by an additional depletion charge created by high values of V_{DS} (equation 6.15). As V_{DS} increases, there is a less rapid increase in I_{DS} , and eventually I_{DS} saturates sooner than the predictions of the classical theory.

Conversely, with substrate bias applied, the classical theory over estimates I_{DS} (Figures 6.21 and 6.25). The over estimation of the current is maximum ($\sim 100\%$) at low values of V_{GS} and gradually decreases as V_{GS} increases. This can be ascribed to a significant shrinkage of W' and increase in the threshold voltage, at high values of V_{BS} (see, e.g., Figure 6.25). The substrate bias has primarily three influences on the drain current characteristics of narrow devices. First, there is a significant increase in the threshold voltage as a function of substrate bias. Second, a reduction occurs in the value of the drain current at particular bias conditions relative to no substrate bias applied (see, e.g., Figures 6.22 and 6.25). Third, there is lowering of the drain voltage at which the drain current saturates (see, e.g., Figures 6.22 and 6.25 at $V_{GS} = 7$ V). Therefore, the mechanisms associated with NCDs result in gross inadequacy of the classical theory, which is based on linear scaling of the device width, and therefore, is not applicable to the analysis of these devices.

It can be concluded that the present model is in good agreement with experimental data both in the linear and saturation regions. The main advantage of the model is its inherent simplicity. The fitting parameters are determined by matching the theory with actual device data; this procedure is required only once for a particular technology. A technique like this in device modelling is more efficient than using 2-D or 3-D numerical analysis. A 3-D analysis of a device, using the finite element technique [6.12], over a range of device sizes and operating conditions, takes approximately 20 CPU hours on an IBM System/370 Model 168 and results only in about 800 values of current as a function of bias and device size.

Although the parameters A and δ can be expressed in terms of device technological parameters and terminal voltages, it is advantageous to leave them as they are; this allows for compensation for any error in the device parameters introduced during the fabrication process, e.g., knowing the actual physical channel width, which is difficult to determine accurately, is not necessary in using the present model.

In the next chapter the mechanisms that control the operation of the upper device of the SMOS structure, introduced in Chapter 2, are identified and their implementation in the present narrow channel model is also discussed.

6.4 Conclusions

A new model for NCDs has been derived and experimentally verified for devices with widths varied from 50 down to 1 μm and different operating conditions, with good agreement between model and experiment. The model is in a simple analytical form and suitable for application

in CAD. A good feature of the model is that it is geometry dependent, and thus converges to the classical theory, under all bias levels, when applied to a wide device. It also provides a basis for studying non-planar narrow devices, e.g., 3-D stacked MOS (SMOS) transistors which are essentially narrow devices, but stacked one on top of another. The modelling considerations relevant to these devices are investigated in the following chapter.

CHAPTER 7

MODELLING CONSIDERATIONS IN 3-D MOSFETs

The 3-D SMOS devices described in Chapter 2 consist of an n-channel enhancement (bulk) device fabricated on the basic p-substrate together with an enhancement mode device built in an upper recrystallized polysilicon active substrate with the same type of carriers as the bulk device; the two devices share a common gate, source and drain. Cross-sectional views of the SMOS structure, along the device width and length, are illustrated in Figure 7.1. The bulk device is a conventional one to which the narrow channel model developed in the foregoing chapter and the available short channel model [7.1] apply. However, the upper device is somewhat different in structure, being similar to a SOI device, and the basis for modelling it needs to be investigated. In this chapter, the performance, design and modelling considerations relevant to this device are discussed. The electrical characteristics of SOI devices are discussed briefly, and compared with those of conventional devices, in the subsequent section.

7.1 Electrical Characteristics of SOI Devices

MOSFETs fabricated in SOI single crystal silicon islands, using CW laser recrystallization have been reported [7.2,7.3] to have electrical behavior comparable to that of bulk devices. Typical drain current characteristics of those devices are demonstrated in Figure 7.2. These devices had a substrate doping of $6 \times 10^{15} \text{ cm}^{-3}$, substrate thickness of $0.5 \text{ }\mu\text{m}$ and gate oxide thickness of $0.1 \text{ }\mu\text{m}$ [7.2]. The mobility as measured on large geometry transistors, to avoid errors caused by reduction of

Figure 7.1 Cross-sectional views of the SMOS transistor, introduced in Chapter 2, along the device width (a) and length (b) (i.e., along BB' and AA' in Figure 2.3).

Scale is: 100 μA per vertical division, 1 V per horizontal division and 0.5 V per step ($V_{\text{GS}} = 0-5 \text{ V}$).

Figure 7.2 Drain current-voltage characteristics of n-channel/SOI devices.

(a) $W \times L = 8 \times 8 \mu\text{m}^2$, Ref. [7.2].

(b) $W \times L = 25 \times 5 \mu\text{m}^2$, Ref. [7.3].

channel length due to lateral diffusion from source/drain areas, was as high as $650 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$. The threshold voltage was 0.3 V, as compared to 0.38 V for bulk devices (calculated assuming $\phi_{\text{MS}} = -0.85 \text{ V}$ and $Q_{\text{ss}} = 10^{11} \text{ cm}^{-2}$). The yield obtained was 90%, indicating that high quality SOI devices can be achieved by laser technology with good yield. These results are consistent with those published recently by Kawamura et al. [7.4]. They reported a propagation delay time, as obtained from a seven stage ring oscillator with $2 \text{ }\mu\text{m}$ channel lengths, of 430 pS per stage at a supply voltage of 5 V. The small delay time can be ascribed to high mobility and the reduced parasitic capacitance of the SOI structure. The yield was greater than 95%, distributed uniformly over the entire laser recrystallized polysilicon area.

Although the devices whose characteristics are shown in Figure 7.2 had floating substrates (no substrate contacts), their characteristics showed no kink in the drain current in the saturation region. The absence of the kink is an indicative of no high drain field effects under those biasing conditions ($V_{\text{DS}} < 10 \text{ V}$). This speculation is consistent with the absence of avalanche multiplication currents, as can be noted in the same figure. However, at a drain voltage high enough to cause impact ionization the kink does appear in the drain current-voltage characteristics of (nonscaled) SOI devices [7.5] giving a rise to the substrate potential. Consequently, the threshold voltage decreases by the known body effect.

For the SMOS structure as described in Chapter 2, if there is no substrate contact in the upper device, the 'kink' effect for a floating substrate would be present for a sufficiently large V_{DS} value; also substrate bias would not be applied to the upper device, so that the two

devices of the complete structure would be dissimilar in this respect. These problems are overcome by making contact to the substrate of the upper device, as indicated in Figure 7.1a, enabling the substrate of the two devices to be connected together. Furthermore, the overall device structure is likely to be scaled in proportion and operating from 5 V supplies. Under such conditions, there will be no kink in their current characteristics and no appreciable carrier multiplication, even with a floating substrate. Such a contact to the upper device substrate is assumed in the following discussion.

7.2 Modelling Considerations in the 'Upper' SMOS Device

The upper device in the SMOS structure, is basically an SOI transistor, but with nonfloating substrate. Assuming no applied substrate bias and a uniform doping level of $2 \times 10^{16} \text{ cm}^{-3}$, the depletion layer thickness (x_D), where $x_D = (4 \epsilon_{si} \phi_F / q N_A)^{1/2}$, is $\sim 0.21 \text{ } \mu\text{m}$ at the onset of surface inversion (at the source end of the channel). In order to ensure partial depletion of the active substrate region, for devices operating from 5 V power supply, the thickness of the substrate should be $> 0.6 \text{ } \mu\text{m}$. Under such conditions, the substrate is partially depleted across the entire width of the channel, x_D equals $0.21 \text{ } \mu\text{m}$ and $.6 \text{ } \mu\text{m}$ at the source and drain sides, respectively, this situation is illustrated by Figure 7.3. With substrate bias applied, the depletion layer thickness (at the source) widens and becomes $\sim 0.6 \text{ } \mu\text{m}$ (at $V_{BS} = -5 \text{ V}$), while it increases to $\sim 0.9 \text{ } \mu\text{m}$ at the drain side. Consequently, for devices operating from 5 V supplies (assuming substrate thickness of $0.9 \text{ } \mu\text{m}$), the

Figure 7.3 SOI structure of an n-channel MOSFET, similar to that inherent in the SMOS devices but upside down. The depletion region and the device terminals are also shown.

depletion charge behavior in response to applied bias is essentially similar to that in bulk devices.

The device operation mechanism is, therefore, fundamentally similar to that of bulk devices. The majority carriers in, for example, an n-channel transistor, are supplied from n^+ regions (source/drain). The degree of surface inversion is controlled by the gate field. Assuming an optimized fabrication process is used, so that the device active substrate is single crystal silicon (which is achievable by the lateral seeding technique discussed in Chapter 2), it should be possible (as demonstrated in the previous section) to obtain devices fabricated in the upper layer with electrical characteristics comparable to those of bulk silicon devices. Consequently, carrier mobilities and doping levels equivalent to those of bulk devices can be assumed obtainable, and have in fact been reported [7.6], as discussed earlier. Therefore, the mobility can be modelled in a manner similar to that used for conventional devices. Other simplifying assumptions commonly used in modelling conventional devices, such as a long-channel (GCA), negligible diffusion current and conventional notion of threshold voltage, are applicable to the analysis of the devices under investigation.

The upper device suffers from narrow channel effects similar in nature to those existing in devices built in the bulk silicon. The upper device substrate is patterned by removing the polysilicon between devices, i.e., it is an "island". Accordingly, a parasitic transistor action occurs along the sidewall of the silicon island (at the width ends of the channel), as a result of the gate field fringing in these regions. This parasitic effect is similar to that found in Silicon-On-Sapphire (SOS) technology [7.7]. Shown in Figure 7.4 are the field fringing lines

Figure 7.4 A half cross section along the width of the "upper" device inherent in the proposed SMOS structure. Also shown are the depletion layers associated with the conventional surface and sidewall channels (at the source end).

at the sidewall edge and the depletion charges associated with the conventional and sidewall channels regions. As demonstrated by this figure, the fringing fields induce an additional depletion charge on the edge surface and under high gate bias conditions surface inversion at the edges can occur. This situation, to a large extent, is similar to that in the conventional substrate device where the depletion and inversion charges extend (or shrink), depending on the biasing conditions, beyond the nominal device width. So, the concept of "effective gate voltage" along the device width, introduced in Chapter 6, is still applicable to the device under analysis.

In wide (i.e., large aspect ratio) devices the sidewall channel effects can be neglected, since the thickness of the sidewalls is small compared to the nominal channel width, but in NCDs the sidewalls can be a significant contribution to the total channel area. Such an effect can not be neglected in analyzing devices with narrow channels. The sidewall channels may result in a significant increase in the drain current, depending on the gate bias applied. This speculation is, in fact, consistent with reported experimental results [7.8]. As can be noted from Figure 7.5, the drain current of these devices does not follow linear scaling of the nominal channel width. The current is higher than that predicted by direct scaling, using the current of a wide device (e.g., 8 μm) as a reference. For example, when the device width is scaled down from 8 μm to 2 μm (at $V_{GS} = -5\text{ V}$) the drain current of the scaled down device is only ~2.3 times smaller than that of the wide device and not 4 times as predicted by linear scaling. This increase in I_{DS} is believed to be due to the contribution of the sidewall channels to the drain current, i.e., the "effective" channel width is larger than the nominal

Figure 7.5 Drain current of SOI P-MOSFETs versus device width (W), data are taken from Ref. [7.8].

width as a result of surface inversion in the sidewall regions. The amount of increase in I_{DS} (relative to I_{DS} predicted by linear scaling) decreases as V_{GS} decreases (see, e.g., Figure 7.5 @ $V_{GS} = -3$ and $V_{GS} = -5$ V). Therefore, the concept of the "effective channel width" used in analyzing conventional narrow devices applies as well to the upper device of the SMOS structure.

As illustrated by Figure 7.4, the total device depletion charge can be represented by two components; the uniform depletion charge region associated with the conventional surface channel and a nonuniform region associated with the parasitic sidewall channel which is induced by the gate fringing field. The nominal uniform depletion charge region is restricted to the physical dimensions of the device active substrate and extends across the entire nominal device width, since the gate is wider than the substrate polysilicon island. Unlike conventional narrow devices, the nominal width of the uniform depletion charge region is not modulated by the gate fringing fields. The sidewall channel may have a portion with a depletion region having a thickness equal to that of the conventional channel, depending on the bias condition. As a result, the total uniform region may extend to the sidewalls (as shown in Figure 7.4). Therefore, the parameter "A" used to represent the modulation of the uniform depletion charge region is still applicable to the present case, but with a slightly different meaning. The parameter A is expected to be always greater than unity and its function takes the form $A = 1 + \chi/W$, where χ represents the width of the uniform depletion region in the sidewalls and it is always a positive value regardless of the technology used or the device biasing conditions. In bulk devices χ can be a positive or negative quantity, depending on the operating condition.

But, the width of the nonuniform region associated with the side-wall channels may be assumed given by " δ " in a manner similar to that used in modelling the depletion charge in bulk devices. Therefore, the basic formulation of the depletion charge model for the lower (bulk) devices is applicable to the upper device. The parameters needed in the model can be obtained by comparing the model predictions with actual device characteristics.

The 1-D behavior of the depletion layer associated with the nominal device width results in threshold voltage which is not expected to exhibit significant dependence on the device width, since V_T is primarily determined by the gate voltage required to induce a uniform strong surface inversion across the nominal width. Experimental results for V_T as a function of channel width are very scanty. According to one published source [7.8], there appears in fact to be negligible V_T dependence on channel width of SOI devices. Therefore, in this particular case it appears that the 1-D classical V_T model is adequate for modelling V_T of the upper device. Further experimental evidence is, however, necessary before one can come to firm conclusions about the dependence of V_T on the channel width of the upper device. In bulk devices the depletion charge layer is nonuniform beyond the central 1-D region defined by " AW ", due to the influence of the transition region between the thin gate-oxide and the thick field-oxide, resulting in high V_T values for narrow devices relative to that of wide devices. The possibility of a mismatch in V_T behavior between the upper and lower devices exists and it will in this event be necessary to minimize such a mismatch by proper choice of the device technological parameters.

Figure 7.6 Short-channel effects in SOI devices.

(a) Drain current of p-MOSFETs versus channel length (L),
 $N_A = 6.1 \times 10^{16} \text{ cm}^{-3}$.

(b) Threshold voltage of n-MOSFETs versus channel length
(L), $N_A = 6 \times 10^{16} \text{ cm}^{-3}$.

Like bulk devices, the behavior of SOI^P MOSFETs exhibits SCEs. As depicted in Figure 7.6a, the drain current increases sharply as the channel length decreases [7.8]. This increase in the channel current, beyond the scaling ratio of the channel length, can be ascribed to the channel shortening, punch-through current and carrier multiplication effects in the saturation region. The threshold voltage as a function of the channel length behaves in a similar manner to standard devices. As the channel length is reduced, the space charge associated with the source/drain junctions begins to enhance the surface band bending which, in turn, results in a lower threshold. Displayed in Figure 7.6b is the influence of the channel length of SOI devices on the threshold voltage as determined experimentally [7.9]. Standard deviations of 50 mV, across the wafer, and less than 90 mV, from wafer to wafer, were obtained. These values are typical of short channels and are acceptable from the device application point of view. The breakdown mechanism in SOI devices is the same as that in single crystal devices; it is strongly dependent on the channel length.

As a result, the SCEs in SOI devices do not result in anomalous characteristics of these devices and therefore can be modelled in a similar fashion to those in bulk devices. In fact, the junction geometry in the former device is, however, different and is particularly simple (1-dimensional), relative to that of the latter devices. The short channel V_T model for such devices is in the literature [7.10]; it appears to be applicable so long as the active substrate layer is not depleted throughout at the source side of the channel. Due to different junction

geometries in the upper and lower devices, there is a possibility of different V_T shifts as a result of SCEs; but such a difference can be minimized by careful choice of device parameters.

In summary, the narrow and short channel effects in the upper device, discussed above, are controlled by the same physical mechanisms as those in the lower bulk devices. The width edges are particularly simple, since there is no field implant or bird's beak effects. The NCD model developed for the lower device is also applicable to the upper device, as discussed earlier. The basic concepts of the model are still valid for the latter device. Application of the model to those devices will, of course, require suitable choice of the fitting parameters incorporated in the model. Such parameters are believed to be different from those used in analyzing the lower devices, due to possible differences in the technological parameters. The overall SMOS device characteristics are simply those of the upper and the lower devices combined together, since they are connected in parallel. So, the SMOS transistor is expected to have a current gain factor twice as much as that of the lower device (in the best case); but it is more practical from the circuit design point of view to allow for a slightly lower carrier mobility for the upper device, relative to that of the lower device. An average mobility of $775 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{S}^{-1}$ for the combined structure would result in a gain factor of 1.72 times that of the lower device. This value assumes mobilities for the upper and lower devices of 650 and $900 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{S}^{-1}$, respectively, which represent typical cases. With an upper substrate thickness of $\sim 0.9 \text{ } \mu\text{m}$, the overall device behavior in response to applied substrate bias should be similar to that of conventional devices. The possibility of mismatching V_T between the upper and bulk devices as a

result of NCEs or SCEs can be minimized by optimizing the device structural and electrical properties.

7.3 Conclusions

The characteristics of SOI devices, similar to the upper device in the SMOS structure, fabricated by laser recrystallization have been discussed and compared with those of bulk devices. The narrow and short channel effects in the upper device are governed by the same physical mechanisms as those in the bulk device. The V_T of the upper device does exhibit significant dependence on the nominal channel width, therefore it can be modelled by the 1-D theory. The concepts of the effective gate voltage and effective channel width and the depletion charge model used in analyzing the bulk devices, are applicable to the upper device. Therefore, the model developed for the lower devices appears to be useful in modelling the drain current-voltage characteristics of upper devices, with appropriate choice of the fitting parameters. The combined SMOS devices are likely to have overall characteristics that look like those of the bulk devices, but with higher current gain factor for a given active device area on the chip (2 in the best case).

CHAPTER 8

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE RESEARCH

8.1 Conclusions

The device structure innovations required for very large scale integration pose challenges in both technology and modelling. Novel methodologies relevant to both aspects have been presented.

A new 3-D vertically integrated MOSFET (SMOS) structure suitable for high integration density of ICs has been introduced. Such a device structure will allow the realization of stacked devices with aspect ratios (W/L) equivalent to that of conventional bulk devices, utilizing only half of the active surface area required by planar devices. Further area savings can be gained from subsequent scaling. Other advantages inherent in this new structure include: (i) easy formation of shallow junctions without contact problems; (ii) the technology required for realizing these devices is compatible with existing technologies; (iii) source/drain contacts are self-aligned; (iv) an improvement in overall device performance is expected, if the active channel area is made simultaneously narrow and short. The technological and modelling requirements that are basic to these devices have been identified and established, resulting in the evolution of novel processing and modelling methodologies. The vertical integration process, as defined in Chapter 2, is also applicable to SOI and 3-D CMOS devices, with little modification, and provides almost unlimited scope for imaginative device structures and novel circuit architecture.

A new laser processing technique, selective laser annealing (SLA), that allows selective recrystallization of designated polysilicon areas

has been established. The principle of the technique is based on the use of an anti-reflection coating. Low laser power levels can be used to recrystallize the coated regions, while the power is still insufficient to introduce material transformation in uncoated regions. This technique allows preferential etching between laser treated and untreated regions resulting in accurate patterning of polysilicon gates with minimum undercut. Simultaneous laser activation of junction implants and recrystallization of the gate polysilicon has become possible with SLA so that high-quality devices with shallow junctions can be achieved. Furthermore, the technique can be applied to future "wafer scale integration" to connect or disconnect redundant modules.

Subsequently, a detailed investigation of the effects of laser processing on the electrical and physical properties of underlying gate oxides, the most critical device element, has been carried out. Laser processed single layer capacitors with n^+ polysilicon electrodes have been evaluated by characterization of the breakdown field strength, leakage current, high frequency C-V characteristics, and minority carrier generation lifetime and SEM analysis. Moreover, the characteristics of laser processed Al-1%Si (or polysilicon) contacts, shallow junctions, and the overall performance of small-geometry MOSFETs have been thoroughly examined. A significant conclusion is that laser technology does not have any non-recoverable effect on the properties of underlying gate oxide, the Si/SiO₂ interface or output device characteristics, if it is carried out at laser power level within the useful laser "processing window".

The proposed 3-D devices, being stacked one on top of another, will tend to be limited by the same physical mechanisms as conventional

planar narrow devices. Consequently, the nonscaling properties of NCDs have been investigated and novel threshold voltage and drain current-voltage characteristics models for these devices have been introduced. The validity of the models extends to both wide and narrow devices (with long channels in both cases). The modelling approach is based on a 2-D evaluation of device charges, an effective gate voltage, linear variation of the surface potential at the width ends of the channel, an "effective" channel width and two fitting parameters (A and δ). The determination of the effective width function is based on experimentally measured characteristics and thus the device geometry need not be precisely known, which is a very desirable feature. All the resulting expressions in the model are geometry dependent and therefore approach those of wide/long device theory, when applied to wide devices. The sensitivity of the threshold voltage and the device output characteristics to substrate bias, a critical mechanism in NCDs is well modelled. Comparison between the prediction of the model and actual device data, under different operating conditions, clearly demonstrates the capability of the model in analyzing narrow devices. Furthermore, the model exhibits excellent agreement with experimental results, significantly superior to published models.

The upper device in the SMOS structure can have characteristics comparable to those built in the starting substrate. The assumptions commonly used in analyzing bulk devices are applicable to the modelling of the upper devices. The modelling considerations relevant to these devices have been identified. Most important is the sidewall channel effect which results in induced inversion and depletion charges and, therefore, a transistor action at the device width edges. The applicability of the model, developed in Chapter 6, to the modelling of this situation and the overall SMOS structure has been discussed.

8.2 Original Research Contributions

The main original contributions of the present thesis can be summarized as follows:

1. The proposed vertically integrated MOS structure and its fabrication scheme which hold promise for increasing packing density without applying the scaling concept, are first reported in this thesis [8.1-8.2].
2. The selective laser recrystallization technique, and its applications in IC technology, and the differential etching between LA and nonannealed polysilicon areas have not been reported in the literature or used in the fabrication of MOS devices [8.3].
3. An extensive investigation of the effects of laser processing of polysilicon gates on the electrical and physical properties of underlying gates oxides (conventional and HfPO_x) [8.4-8.5], contacts, shallow junctions and the overall MOSFET characteristics are first carried out in this thesis [8.4-8.5].
4. CW laser processed one micron size transistors, with high quality, have first been reported in the present thesis [8.6].

5. The model that considers the nonscaling feature of the $I_{DS}-V_{DS}$ characteristics of NCDs, while valid for both narrow and wide devices, has not appeared in the literature so far.
6. The modelling considerations relevant to the analysis of the upper device in the SMOS structure have been identified.

8.3 Recommendations For Future Research

The evolution of vertically integrated technology, i.e., more than one active device layer in the vertical direction, opens a new era of research. It will lead to a wide range imaginative device structures and circuit architectures. In addition to the technological and modelling aspects dealt with in Chapters 2 through 7, the following suggestions for future work would give more insight into the physical nature of the proposed SMOS structure and assist in the realization of such devices.

8.3.1 3-D Technology

Characterization of double layer capacitor structures, which are inherent in SMOS devices, is certainly one of the research areas that should receive extensive attention in the future. Even though the results presented in Chapter 4 are likely to hold for stacked capacitors, a laser "processing window" for the upper active substrate needs to be defined in a similar fashion to that determined for the common gate polysilicon layer. Generally speaking, laser processing of the upper layer is usually easier than that of the bottom one, and should not lead to detrimental electrical or physical effects on that layer. But, the

optimum laser parameters that result in SiO_2/Si interface characteristics comparable to those of the bulk device need to be determined. Extensive electrical and physical analysis, similar to that used in Chapter 4, would lead to the determination of such processing parameters.

Another aspect that requires further investigation is the interface contact resistance between different metallization schemes and laser recrystallized polysilicon, using the test structure utilized in studying the contact characteristics described in Chapter 5. Such a study should be carried out for a range of laser processing parameters so that a correlation between the laser power and contact resistance could be obtained and used as a guide in designing 3-D structures.

8.3.2 Application of the Model to SMOS Structures

The NCD model presented in Chapter 6, with appropriate modifications based on the modelling considerations that are basic to 3-D structures discussed in the preceding chapter, can be extended to the analysis of the SMOS MOSFETs. This, however, will certainly require more study; the dissimilarities between the upper and lower devices, discussed in Chapter 7, must be represented in modelling the SMOS devices. The resulting model should be capable of predicting the combined characteristics of the overall structure in such a way that it gives some insight to the device operating physical mechanisms. This, of course, will require the fabrication of SMOS devices to generate experimental data against which the predictions of the new model can be compared.

8.3.3 Modelling of Small-Size MOSFETs

The simplicity of the NCD model presented in Chapter 6 enables an easy derivation of the small signal equivalent circuit parameters, namely, g_m , g_d , C_{gs} , C_{gd} and C_{gb} ; such parameters are useful in circuit design. Attempts should be made to obtain the expression for the effective channel width analytically, rather than empirically as given by the present formulation of the model. A natural extension of the present modelling problem is the analysis of small size (short/narrow) MOSFETs. The small size effects, which are significantly different from those of short or narrow devices when considered individually, are still not well understood. The narrow and short channel effects, when combined in one structure, result in threshold, punch-through and avalanche breakdown characteristics which are different from those of short or narrow devices, but similar to those of large geometry devices as demonstrated in Chapter 3. The 3-D analysis techniques [8.7] gives valuable insight into the 3-D distribution of the electric field in small structures, but are prohibitive for use in CAD in terms of complexity, computation time, and computer memory required. The model presented in Chapter 6, in conjunction with available SCEs models [8.7], can be applied to small geometry (short/narrow) devices; such a modelling approach may be more practical for design purposes, due to its inherent simplicity and economical advantages, than 3-D numerical analysis techniques [8.8].

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APPENDIX A

The integrated I_2 given by equation (6.12) in the text is carried out as follows:

$$I_2 = \frac{V_{gs} dz}{\left[1 + \frac{1}{b(1/z' - 1)}\right]^2}^{1/2}$$

$$= \int_{AW/2}^{AW/2+\delta} \frac{V_{gs} dz}{1 + \left(\frac{z-AW/2}{X_{F1} - \frac{X_{F1}(z-AW/2)}{\delta}}\right)^2}$$

Let:

$$Z = z - AW/2$$

$$a = X_{F1}$$

and $b = X_{F1}/\delta$.

Therefore, we get

$$I_2 = V_{gs} \int \frac{dz}{1 + \left(\frac{Z}{a-bZ}\right)^2} = V_{gs} \int \frac{dz}{1 + \left[\frac{1}{-b} \left(\frac{-bZ+a-a}{a-bZ}\right)\right]^2}$$

$$= V_{gs} \int \frac{dz}{1 + \left[\frac{1}{-b} \left(1 - \frac{a}{a-bZ}\right)\right]^2}$$

This gives:

$$I_2 = V_{gs} \int \frac{a dt}{(1+t^2)^{1/2} (tb+1)^2}, \quad (1A)$$

where:

$$t = \frac{1}{-b} \left(1 - \frac{a}{a-bZ}\right).$$

Therefore:

$$\frac{tb+1}{b} = \frac{a}{b(a-bZ)},$$

or

$$\frac{b}{tb+1} = \frac{b(a-bz)}{a}$$

Thus:

$$dz = \frac{a}{(bt+1)^2} dt$$

Let:

$$tb+1 = \frac{1}{x},$$

or

$$dt = \frac{-1}{bx^2} dx$$

Also,

$$t = \frac{1}{b} \left(\frac{1}{x} - 1 \right) = \frac{1}{bx} - \frac{1}{b},$$

or

$$t^2 = \frac{1}{b^2 x^2} - \frac{2}{b^2 x} + \frac{1}{b^2}$$

Substituting for t^2 and dt in equation (1A), we get:

$$\begin{aligned} I_2 &= a \cdot v_{gs} \int \frac{\left(\frac{-1}{bx^2} \right) dx}{\left[\sqrt{1 + \frac{1}{b^2 x^2} - \frac{2}{b^2 x} + \frac{1}{b^2}} \right] \left(\frac{1}{x^2} \right)} \\ &= -a \cdot v_{gs} \int \frac{x dx}{\sqrt{(b^2 + 1)x^2 - 2x + 1}} \end{aligned}$$

Let:

$$A' = b^2 + 1,$$

$$A' = b^2 + 1 = \left(\frac{x_{F1}}{\delta}\right)^2 + 1,$$

$$B = -2 \quad \text{and}$$

$$C = 1.$$

This gives:

$$I_2 = -a \cdot V_{gs} \int \frac{x \, dx}{\sqrt{A'x^2 + Bx + C}}.$$

Using integration tables, we get:

$$I_2 = -a \cdot V_{gs} \left[\int_0^{\delta} \frac{\sqrt{\frac{A'x^2 + Bx + C}{A'}}}{A'} - \frac{B}{2A'} \left[\frac{1}{\sqrt{A'}} \ln(2 \sqrt{A'}) \right. \right. \\ \left. \left. + \sqrt{A'x^2 + Bx + C} + 2A'x + B \right) \right] \right],$$

where:

$$\frac{1}{x} = bt + 1 = -1 + \frac{a}{(a - bz)} + 1$$

$$= \frac{a}{(a - bz)}.$$

or

$$X = \frac{a - bZ}{a} = (1 - Z/\delta), \text{ where } \delta = a/b.$$

Substituting for X in I_2 , we obtain:

$$I_2 = a \cdot v_{gs} \int_0^\delta \sqrt{\frac{A'(1 - Z/\delta)^2 + B(1 - Z/\delta) + C}{A'}} dZ$$

$$= \frac{B}{2A'} \left[\frac{1}{(A')^{\frac{1}{2}}} \ln \left(2(A')^{\frac{1}{2}} (A'(1 - Z/\delta)^2 + B(1 - Z/\delta) + C)^{\frac{1}{2}} + 2A'(1 - Z/\delta) + B \right) \right]$$

$$I_2 = -a \cdot v_{gs} \left\{ \frac{\sqrt{C}}{A'} - \frac{B}{2A'} \left[\frac{1}{\sqrt{A'}} \ln(2(A'C)^{\frac{1}{2}} + B) \right] - \frac{\sqrt{A'+B+C}}{A'} + \frac{B}{2A'} \left[\frac{1}{(A')^{\frac{1}{2}}} \ln(2\sqrt{A'(A'+B+C)} + 2A' + B) \right] \right\}.$$

For convenience let:

$$\zeta = A' + B + C,$$

$$\xi = \left(\frac{B}{2\sqrt{A'}} \right),$$

This gives:

$$I_2 = \frac{a \cdot v_{gs}}{A'} \left\{ \zeta^{\frac{1}{2}} - \sqrt{C} + \xi \left[\ln \left(\frac{2\sqrt{A'C} + B}{2(A'\zeta)^{\frac{1}{2}} + 2A' + B} \right) \right] \right\}.$$

Substituting for B and C in the previous equation yields:

$$I_2 = \frac{a \cdot V_{gs}}{A'} \left\{ \sqrt{\zeta} - 1 + \xi \left[\ln \left(\frac{(A')^{\frac{1}{2}} - 1}{(A'\zeta)^{\frac{1}{2}} + A' - 1} \right) \right] \right\} . \quad (2A)$$

APPENDIX B

The first integral in equation (6.10) in the text is performed as follows:

$$I_4 = \frac{-2}{AW+2\delta} \int_0^{AW/2} \int_0^{\psi_s} \frac{\epsilon_s}{(2\epsilon_s/q N_A)^{1/2} (\psi_s(y,z))^{1/2}} d\psi_s dz .$$

where the integration limits are from zero potential at the depletion charge boundary in the bulk, to ψ_s at the surface, where ψ_s as defined in page 136.

$$\begin{aligned} &= -2 \cdot M \int_0^{AW/2} \left(\frac{1}{2} q N_A \epsilon_s \right)^{1/2} \cdot 2 (\psi_s(y))^{1/2} dz \\ &= -2K' \cdot M \int_0^{AW/2} (\psi_s(y))^{1/2} dz = -2KM \left[z (\psi_s(y))^{1/2} \right]_0^{AW/2} . \end{aligned}$$

where:

$$K' = (2\epsilon_s q N_A)^{1/2} ,$$

$$M = 1/(AW + 2\delta) .$$

Thus,

$$\begin{aligned} I_4 &= -K' \cdot M (2\phi_F + \phi_n(y) - V_{BS})^{1/2} AW . \\ (1B) \end{aligned}$$

The second integration in equation (6.14) in the text is carried out as follows:

$$I_5 = -2M \int_{AW/2}^{AW/2+\delta} \int_0^{\psi_s} \frac{\epsilon_s}{(2\epsilon_s/q N_A)^{1/2} (\psi_s(y,z))^{1/2}} d\psi_s dz$$

$$= -2M \int_{AW/2}^{AW/2+\delta} \left(\frac{1}{2} q N_A \epsilon_s \right)^{1/2} [2(\psi_s(y,z))^{1/2}] dz$$

$$= -2K \cdot M \int_{AW/2}^{AW/2+\delta} (\psi_s^0(z) + \phi_n(y) - v_{BS}(z))^{1/2} dz$$

$$\text{where } K = (2qN_A \epsilon_s)^{1/2}$$

$$= -2K \cdot M \int_{AW/2}^{AW/2+\delta} \{ (2\phi_F - v_{BS})(1 - (z - AW/2)/\delta) + \phi_n(y) \}^{1/2} dz$$

$$= -2K \cdot M \left[\{ (2\phi_F - v_{BS})(1 - (z - AW/2)/\delta) \right.$$

$$\left. + \phi_n(y) \}^{3/2} \frac{2/3}{(2\phi_F - v_{BS})/\delta} \right]_{AW/2}^{AW/2+\delta}$$

$$= -2K \cdot M \left[(\phi_n(y))^{3/2} - (2\phi_F + \phi_n(y) - v_{BS})^{3/2} \right] \left(\frac{-2/3 \delta}{2\phi_F - v_{BS}} \right)$$

$$= +2K \cdot M \left[(2\phi_F + \phi_n(y) - v_{BS})^{3/2} - (\phi_n(y))^{3/2} \right] \left(\frac{2/3 \delta}{2\phi_F - v_{BS}} \right)$$

This gives:

$$I_5 = \frac{-4\delta K \cdot M}{3(2\phi_F - v_{BS})} [(2\phi_F + \phi_n(y) - v_{BS})^{3/2} - (\phi_n(y))^{3/2}] \quad (2B)$$

END

2 9 H 1 0 H 8 5

FIN