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A Comprehensive Design Method
for
Dual Gate MOSFET Mixers

by

Adrian John Bergsma, B.Eng.

A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfillment of
the requirements for the degree of
Master of Engineering

Ottawa Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada
May 1998

The undersigned hereby recommend to
the faculty of Graduate Studies and Research
acceptance of the thesis

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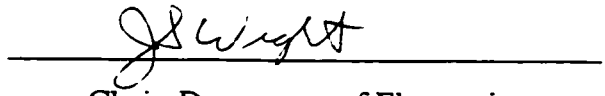

Chair, Department of Electronics

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Carleton University

May 1998

Abstract

A comprehensive design method for a dual gate MOSFET mixer is proposed providing a simple, practical, methodical approach to predict the gain and input compression point of a DGFET mixer with each step in the process being easily implemented by either simulation or lab bench techniques. It also provides an accurate, understandable procedure for identifying and verifying the appropriate bias conditions and the minimum LO power level required.

Using a discrete packaged device, a dual gate mixer core structure is fully characterized for conversion gain and input compression point. A single-balanced dual gate MOSFET mixer circuit is constructed and measured with an RF input frequency of 857 MHz, LO frequency of 694 MHz, and an IF output frequency of 163 MHz.

The final mixer exhibits 5.4 dB conversion gain and an input compression point of -9 dBm. When the external matching networks are accounted for, the mixer core structure exhibits 11.9 dB of conversion gain and an input compression point of 3 dBm.

The information in this thesis comes in part from the research program of Dr. Barry Syrett. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis, including tables, graphs, and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Syrett and his associates for education and research purposes only, including publication in the open literature with appropriate credits to Adrian John (A.J.) Bergsma. Matters of intellectual property may be pursued with Carleton University and Dr. Syrett where and when appropriate.

Acknowledgments

I would like to take the opportunity to thank Professor Barry Syrett for his assistance in the completion of this thesis and the degree program. The constructive discussions, the attention to detail, the expectation of excellence, and the willingness to help in all areas of the program were greatly appreciated.

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I would like to thank my parents, Jerry and Dianne Bergsma, for all of the help, support, and understanding over the years, without which I would have never been able to make the vision a reality. Thank you very much.

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List of Abbreviations and Acronyms

ADC	Analog to digital converter
AGC	Automatic gain control
BJT	Bipolar junction transistor
CAD	Computer aided design
CDMA	Code division multiple access
DAC	Digital to analog converter
DC	Direct current
DGFET	Dual gate field effect transistor
DRC	Design rule check (a design verification tool)
EMI	Electromagnetic interference
FET	Field effect transistor
GaAs	Gallium arsenide
HB	Harmonic balance analysis method
IC	Integrated circuit
IF	Intermediate frequency
IP3	Third order intercept point
LNA	Low noise amplifier
LO	Local oscillator
LS-SS	Large signal - small signal analysis method

LVS	Layout versus schematic (a design verification tool)
MOSFET	Metal oxide semiconductor field effect transistor
P1dB	One dB compression point
PA	Power amplifier
PLL	Phase locked loop
RF	Radio frequency
RFIC	Radio frequency integrated circuit
TDMA	Time division multiple access
VCO	Voltage controlled oscillator

$gm2$	the nonlinear function that represents the pseudo-transconductance of the dual gate device from gate 2 to drain.
$\Delta gm2$	the nonlinear function that represents the sensitivity of the $gm2$ function to the input signal. It is related to the conversion transconductance.
g_c	the conversion transconductance from RF input voltage to IF output current.

Chapter 1: Introduction

1.1 Introduction

The consumer demand for low cost, high quality, mobile communications services has resulted in continued growth for the telecommunications industry[1.1]. In order to maximize the efficient use of available spectrum as well as provide improved services, digital transmission techniques such as TDMA and CDMA have become the dominant communication standards. The use of digital communication methods has provided the means for a convergence in the methods of treating already digital computer traffic and the now digitized voice traffic.

While most of the active components dealing with the high frequency signal transmission and reception functions are done with either bipolar or MESFET technologies, most digital processing is done with the significantly less expensive, low power MOS technology. Significant cost savings could result if the radio system, from transmission and reception to data processing, could be completely integrated on one chip in one technology. Although this is economically attractive, there are serious technological hurdles to overcome before this can become a commonplace reality [1.2 to 1.8].

Although the complete integration of the radio system on one chip may not currently be feasible, there is also a growing economic benefit of a general cost reduction in terms of the discrete parts used to create the radio system. The use of MOS devices for the high frequency analog sections of radio systems and the economies of scale made possible by the use of the lower cost MOS technologies, already used for mass production of

digital circuits, may provide significant system level cost reductions without a reduction in quality or reliability.

To address the concerns and questions about the high frequency capabilities of the MOS technologies, significant research is continuing into the high frequency characteristics of MOS technologies to determine whether they are suitable for high frequency applications in the transmission and reception sections of modern communication systems [1.9 to 1.15]. Along with new radio system architectures and methods, research is continuing into integrated circuit structures and topologies for amplifiers, filters, dividers, oscillators and mixers. It is the aim of this thesis to add to this growing body of knowledge.

1.2 Thesis Outline

This thesis is organized into seven chapters. The first chapter provides a general introduction to the current technological and economic situation which provided the impetus for the development of the design procedure described in the thesis as well as an outline and the thesis contributions to the topic.

Chapter two reviews the system considerations such as architecture and specifications followed by a discussion of the technological challenges specific to the use of MOSFETs in high frequency analog applications. A review of some of the basic radio frequency integrated circuit (RFIC) mixer circuit topologies provides a background for the circuit topologies currently available to the RFIC designer.

Chapter three explains the dual gate FET structure followed by a discussion of some of the modeling concerns for single as well as dual gate MOSFETs. The 'cascode approximation' and its usefulness in the context of design and modeling is explained.

Chapter four is concerned with describing the design methodologies currently available for dual gate mixers. A brief introduction to the harmonic balance and large signal/small signal analysis techniques is followed by summaries of some key design approaches currently available in the literature. Following this review, the proposed design method is described using a brief theoretical introduction, the mathematical equations used in the method, and then a concise summary to clarify the simplicity of the method.

Chapter five deals with the detailed practical application of the design method. Each step of the method is described in detail along with the practical aspects of implementing each step. It is structured to closely follow an expected design procedure and includes all of the required DC and RF data from one characterization example including the determination of bias conditions as well as the calculation of conversion transconductance and input compression point.

Chapter six further explores the characterized circuit and provides the extra information needed by the designer for intelligent optimization of the final design. The discussion and results showing the effects of RF bias and LO power levels on the mixer circuit are invaluable tools and illustrate the flexibility available to the designer as well as the accuracy of the design method over various bias and power conditions. Using the results of this exploration, a final mixer is designed with the results being tabulated and a brief comparison being made to other similar dual gate structures.

Chapter seven provides the conclusions that can be drawn from this thesis and gives some areas that can be explored for future work.

1.3 Thesis Contributions

This thesis seeks to expand the knowledge base for the use of MOS technologies in high frequency communication circuits by providing a practical, systematic, theoretically sound method to accurately design a dual gate MOSFET mixer. Applications include, but are not restricted to, the high frequency or intermediate frequency portions of wireless systems, cable TV systems, and computer modems.

Although the dual gate field effect transistor (DGFET) has been in use for a number of years, its operation is significantly more complex than a single gate transistor with its true behaviour being difficult to model effectively. This has left the designer with insufficient details concerning the operation of the device to properly design circuits with the device. This results in empirical designs with often disappointing characteristics, or the avoidance of designing with the device at all.

The method proposed in this thesis provides a solution for this situation by providing a design method that employs a simple, practical, methodical approach to calculate the gain and input compression point of a DGFET mixer with each step in the process being easily implemented by either simulation or lab bench techniques. It provides an accurate, understandable procedure for identifying and verifying the appropriate bias conditions and also provides the means to define the minimum LO power level required. The technique is aimed at producing a well engineered design, not a rigorous numerical solution.

Chapter 2: System Considerations

Mixers are used in radio communication systems to translate signals from one frequency to another so that information signals can be more effectively processed. Proper mixer design can be critical to the success of a communication system as the characteristics of the mixer can often be the limiting factor in a communication system[2.1]. This discussion will concentrate on the implementation of mixers in a radio frequency integrated chip (RFIC) environment.

2.1 System and Specification Overview

2.1.1 System Architecture

A representation of a generic modern receiver architecture is shown in Figure 2.1. The receiver consists of an input, for example an antenna or cable system, an RF filter for selecting the radio frequency (RF) band desired, a low noise amplifier (LNA), another RF filter, a mixer (MIX2) driven by the local oscillator (LO2), a filter at the intermediate frequency (IF2), another mixer (MIX1) driven by the first LO (LO1), followed by a low pass filter (IF1) and an analog to digital converter (ADC). This system translates the information in the RF signal to a lower frequency where it can be more effectively digitized for further processing.

The transmitter is similar in architecture to the receiver, but with a reversed signal path. It converts the digitized information into an analog signal and translates the information signal, with appropriate filtering, to a higher frequency where it can be more

easily transmitted by an antenna or cable system, using a power amplifier (PA) to obtain the transmit power required.

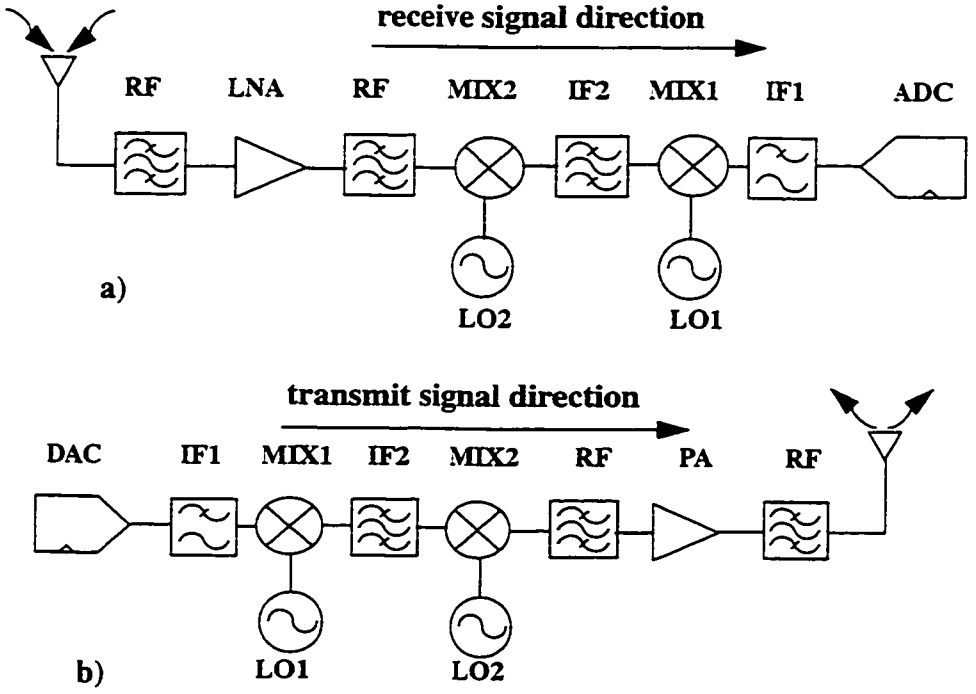

Figure 2.1 a) Typical receiver architecture
b) Typical transmitter architecture

2.1.2 Mixer Specifications

Mixers generally make use of the trigonometric identity shown in Equation 2.1. The multiplication of two frequencies together creates frequency components at the sum and difference frequencies, only one of which is usually desired. Normally, the equation that describes the operation of the circuit is much more complex than a simple cosine multiplication, resulting in many extra frequency components. Filtering of the output not

only selects the desired sideband, but is helpful in reducing extraneous frequency components at the output.

$$\cos(2\pi f_1 t) \times \cos(2\pi f_2 t) = \frac{1}{2}\left(\cos(2\pi(f_1 + f_2)t) + \cos(2\pi(f_1 - f_2)t)\right) \tag{2.1}$$

A perfect mixer performs this frequency translation with no modification or distortion of the information in the signal, no signal strength loss, no dependence upon the amplitude of the LO waveform, and no addition of noise. Ideally, the only output would be the frequency desired, with no components of the local oscillator frequency, the original signal frequency, or any other undesired frequencies. Real mixers differ on how well they approach this ideal, resulting in specifications for linearity, noise figure, signal handling capabilities, LO compression, and port isolation. A brief review of these specifications will help illustrate the challenges involved.

Signal handling capabilities are often discussed in terms of the one dB compression point, or P1dB. As the input signal power increases, the circuit can no longer process the signal correctly without distortion. One result of this is a reduction in gain. The P1dB value identifies the input power at which the circuit gain is one dB lower than the expected gain. In a receiver, a high P1dB point allows a circuit to withstand multiple input signals without distortion, providing a measure of immunity from blocking signals, desensitization, and signal power fluctuations. In a transmitter, a high P1dB point allows for increased signal to noise ratios and more efficient use of the circuit.

The third-order intercept point, or IP3, is a measure of the linearity of the system. Third-order distortion results from nonlinearities in the circuit that cause the multipli-

cation of the desired input signal with adjacent channel signals, creating distortion products that are close in frequency to the original desired signal. Due to this proximity in frequency, third-order products cannot be filtered out and, once created, remain in the system causing distortion and errors. In a receiver, a high IP3 may allow the relaxation of filtering requirements as well as provide a measure of protection against large adjacent signals causing distortion in the radio.

Noise figure is a measure of how much noise the circuit adds to the signal as it passes through the circuit, or alternatively, the change in the signal to noise ratio through the circuit. Each circuit topology has different noise characteristics depending upon inherent device and technology capabilities as well as circuit structure. Mixer noise contributions can be a significant portion of the system noise floor. In a receiver, this places a lower limit on the minimum receivable signal power. In a transmitter, the noise floor can be transmitted as sidebands, creating interference for adjacent channels. Minimum noise figure is beneficial in reducing these effects.

The LO compression characteristic is a measure of the immunity of the mixer gain to variations in the amplitude of the LO waveform. This is commonly described by the ratio of change in mixer gain to the change in LO power, with the ideal case being a ratio of zero. At low LO power levels, mixers can exhibit 1 dB of gain variation for 1 dB change of LO power, resulting in a high sensitivity to the LO power level. As the LO waveform may arrive at the mixer input through a series of amplifiers and filters, each with its own temperature and process variation, a mixer that is highly dependent upon the LO input waveform becomes susceptible to large temperature and process variation which could lead to specification failures due to a cascading effect at the system level.

Port isolation is a measure of frequency component suppression between ports. Mixer circuit topologies are described as unbalanced or single-balanced, double-balanced, or fully balanced. Balanced circuits use the relative phase of the signals to provide suppression of the input signals and enhancement of the output signal at the output port of the circuit. Some circuit topologies provide inherent isolation between the LO and RF ports, although many do not. The degree of port isolation possible with any given technology or circuit topology is often dependent upon parasitic effects such as capacitive coupling and device mismatch. Port isolation is very important at the system design level as it impacts directly on the amount of filtering required before and after the mixer. For example, in some systems, a significant LO frequency component at the output of the mixer is unacceptable as it causes compression and distortion in the following amplifier or spurious frequency generation or transmission elsewhere in the system. Increased filtering may not be an acceptable solution as filtering can cause increased signal loss, distortion through filter gain ripple and phase delays, and increased manufacturing costs. As such, port isolation can be a determining factor in the choice of circuit topology.

Once the specifications for linearity, noise figure, signal handling capabilities, LO compression, and port isolation are decided, the circuit designer must choose how to approach the design by investigating process technologies, circuit topologies, and design tools or methods that will provide a cost effective solution.

2.2 Technology Issues

2.2.1 The One Chip Radio Challenge

The increasing consumer demand for high quality mobile communication capabilities provides a compelling economic impetus to investigate innovative technological solutions to reduce the cost of providing communication services. Consumer interest is increasingly concentrated on mobility, low cost, and speed and reliability of transmission. In order to address these concerns, system designers have reduced supply voltage levels to reduce the size, weight, and cost of mobile units, have used digital transmission techniques such as TDMA and CDMA to improve the signal transmission reliability and quality, and have improved digital signal processing capabilities in order to be able to provide enhanced consumer services.

A significant source of electromagnetic interference (EMI) is the transfer of signals between integrated circuits. The need to use external filtering and multiple integrated circuits to complete a given system function increases the opportunities for spurious frequency generation and reception. In addition, the need to use multiple technologies such as MOSFETs for the digital portion and a bipolar or GaAsFET technology for the radio or analog portion of the radio system results in an increased component count leading to increased costs due to area usage, packaging, manufacturing costs, RF shielding requirements, and power distribution difficulties.

One possible solution is to use a single technology to implement the entire radio system. This 'one IC solution' employs the digital MOSFET transistor in an analog

RF application so that the signal doesn't need to leave the IC except for reception and transmission.

Although this seems to be the ideal solution, severe technological challenges are preventing the full implementation of the concept. For example, the MOS device has not yet been fully characterized for RF usage, CAD models are not of sufficient accuracy to be used for product quality RF MOS circuits, on-chip filtering capabilities are severely lacking, and crosstalk between digital and analog circuitry on the same substrate and in the same package is significant and is poorly modeled. Although improved transistor and process characterization can ameliorate the first two concerns, the filtering and circuit isolation problems are inherent limitations with current technology capabilities. These effects are manifested as noise injected into oscillators, excess frequencies generated in mixers, parasitic oscillations, low Q filters, increased noise floor, and reduction of overall system sensitivity.

A second compelling economic argument for the investigation into MOSFET technologies is process technology cost. The use of less expensive standard MOS technologies to implement RF analog functions will reduce the cost of individual components in the radio system. This becomes very important for mass produced consumer electronic products as any small reduction in cost can result in major cost savings for the producer.

Regardless of the current technology limitations, the overwhelming economic benefits involved with the single IC solution requires that design methods and practices be generated and tested to provide the ground work for a possible implementation of the concept in the future. Even if the investigations reveal that a single IC solution is not feasible, the economies of scale available with MOS technologies is sufficient to warrant increased

investigation into its RF capabilities. One way to approach this is to investigate RF MOSFET circuit topologies and capabilities in order to create a background of knowledge and experience in the field.

2.2.2 MOSFET Process Technology Background

For many years, MOS technologies have dominated low frequency digital applications. However, with increased demand for faster computing capabilities, MOS technologies were modified and improved to operate faster in the digital environment. With further device enhancements and improved CAD support, MOS devices proved to be highly suitable for the high speed digital processing of analog signals. As this trend of process improvement continues, research into the capabilities of MOS transistors for analog and digital operations at higher frequencies is continuing. Promising results are being shown for filters, ADCs, DACs, dividers, multipliers, counters, PLLs, VCOs, mixers and LNAs [2.2 to 2.16]. Significantly, research has produced exciting results at 1 to 2 GHz for analog operations such as low noise amplifiers, oscillators, and mixers. The frequency of operation for these circuits is expected to increase as device geometries go below the half- and quarter micron level.

As MOS technologies improve, technical challenges are being exposed. Modeling issues not encountered in digital applications such as short channel effects, noise performance, and linearity are becoming obstacles to further exploitation of the high frequency capabilities of the technology[2.17, 2.18]. As transistors are reduced in size to enable higher frequency operation, process variations play a larger role in the reliability of designs and devices deviate significantly from the traditional long gate drain current to

gate voltage square law relationship[2.19]. Greater understanding of the device nonlinearities, 1/f noise, channel noise, short channel effects, doping gradients, gate resistance, parasitic capacitances, and power requirements is needed so as to avoid underestimating or overestimating the capabilities of the process technologies. More accurate process characterization must include RF criteria such as transconductance, noise, port impedances and process variations so that CAD tools can be improved to enhance the accuracy of high frequency analog simulations. As simulation capabilities improve, the margin for error that a designer needs to include in production designs can be reduced, allowing for more aggressive use of the process capabilities, thus avoiding overly conservative design approaches. An improved understanding of MOS technologies will also reveal limitations of the FET device, providing valuable design information to the circuit and system designer. With this knowledge, the design engineer can reduce design cycle time by concentrating on circuit topologies and approaches that will be successful while avoiding fruitless design strategies. Also, the system designer can adjust system level specifications to take full advantage of the capabilities of the technology.

As this research continues, circuit designers need immediate intermediate solutions. A toolkit of design techniques and practices must be developed that can be used to design high frequency MOS circuits with some degree of confidence. Conservative approaches such as using standard low frequency designs modified for higher frequency operation and the transfer of BJT circuit topologies into MOS are good beginnings. High frequency design techniques common with GaAs MESFET or even bipolar technologies are also beneficial, often proving to be directly applicable to new MOS designs. However,

for full technology exploitation, new design methods must be developed specifically for MOS technologies.

MOS technology, with more research and improved design techniques, may prove to be a useful process technology for the high frequency applications in modern communication systems. Although not currently at the maturation level required, it is possible that MOS technologies, fully exploited, may compete technically and economically with bipolar devices for low GHz analog applications.

2.3 RFIC Mixer Circuit Topologies

A wide variety of circuits have been used to make mixers. The two main techniques used are the multiplication of the signal with a square wave and the exploitation of device nonlinearities. This discussion will concentrate on the current state of the art in bipolar and FET technologies in a radio frequency integrated circuit environment.

2.3.1 BJT Base and FET Gate Mixers

Conceptually, one of the simplest methods to create a mixer is to use the inherent nonlinearities of a transistor biased as an amplifier. This can be done in almost any technology and is generally based upon creating an amplifier and then modulating the amplifier characteristics at the frequency of the LO. The superposition of two signals onto a device in such as way as to excite the device nonlinearities will produce many extraneous frequency components, only one of which is the desired mixing frequency. Usually, the LO and RF input signals are applied to the base or gate of the transistor after appropriate impedance matching with the IF output signal being extracted from the collector or drain

of the transistor after appropriate matching and filtering. Practically, however, it is often difficult to balance all of the design criteria to produce a successful design in the RFIC environment. Usually, adequate linearity and gain are a design trade-off as any technique used to linearize the device reduces the conversion transconductance. In the simple configurations, there is little port isolation and the separation of RF, LO, and IF signals is difficult, often making this technique unsuitable for integration due to the filtering required. A representative circuit, without biasing, is shown in Figure 2.2

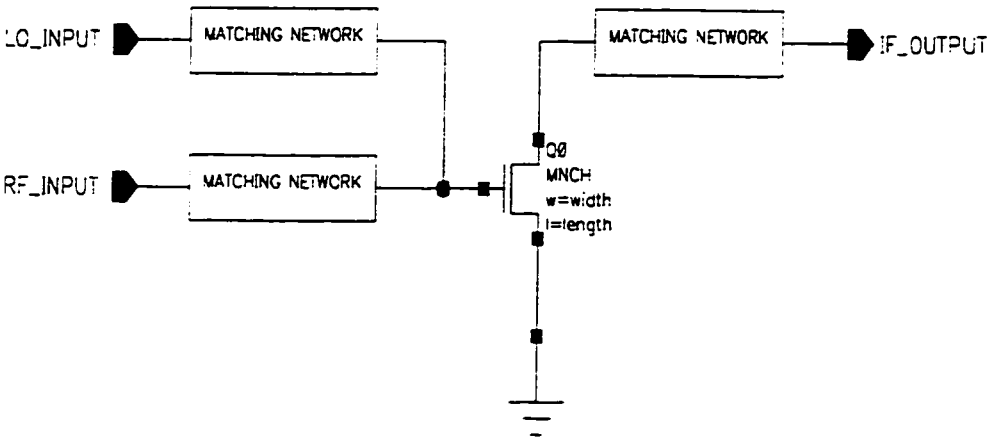

Figure 2.2 MOS gate mixer structure

2.3.2 Tree or Gilbert Cell Mixers

One of the better integrated mixers is the very common tree mixer, also referred to as the Gilbert cell [2.20]. This circuit is well suited for the RFIC environment and relies upon the co-integration of transistors for its success. It can be singly or fully balanced, and provides inherent port to port isolation which is primarily dependent upon device matching. It can have high linearity and low noise figure with the correct design techniques, usually involving design trade-offs to achieve respectable values. It uses a quad of transistors to switch the gain of an RF amplifier from positive to negative at the frequency of the LO, effectively producing a multiplication between the two signals. This mixer structure can be implemented in almost any transistor technology with varying results. The basic topology is not well suited for reduced power supplies as all devices must be in the active region and a current source is often necessary for biasing. In addition, the operation of the MOS version of this circuit is not optimal as the switching and distortion characteristics of the MOSFET are different from those of the BJT [2.21]. In addition, the parasitic capacitance of the switching devices causes some undesired effects that may impact the high frequency capabilities of the topology. A representative circuit, without biasing, is shown in Figure 2.3.

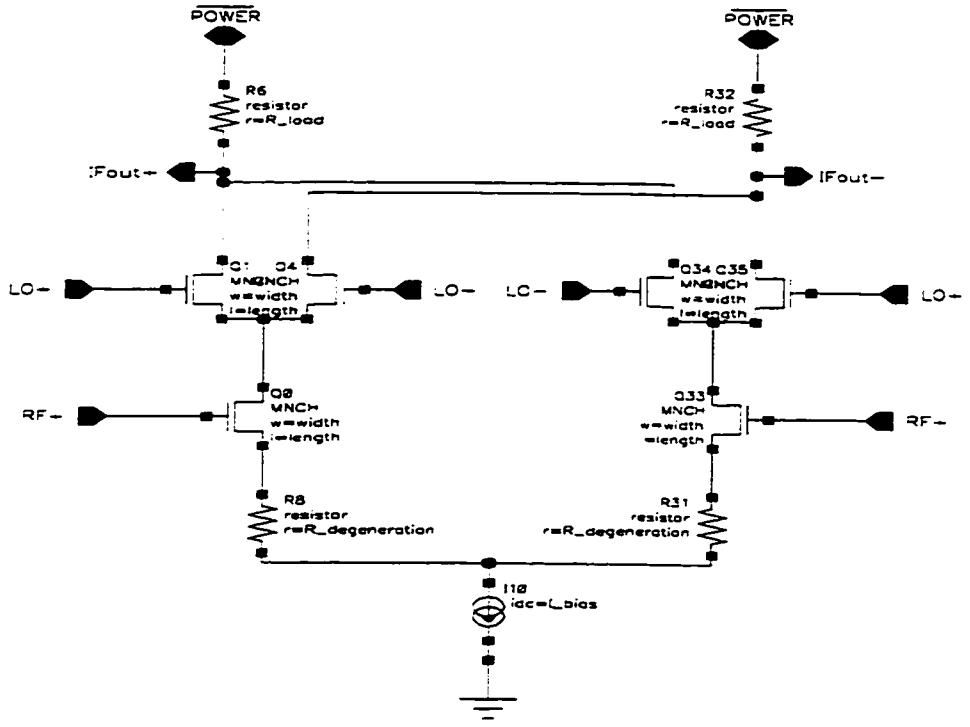

Figure 2.3 MOS tree mixer structure

2.3.3 FET Drain Mixers

In the linear, or ohmic, region of operation, the FET transistor channel operates as a nonlinear voltage controlled impedance, using the gate-source voltage, V_{gs}, and the drain-source voltage, V_{ds}, to control the impedance between the drain and the source. As the device current is then dependent upon two voltages, this nonlinearity allows the use of the device as a mixer by varying the two voltages at different frequencies. One result of this characteristic is the drain mixer, shown in Figure 2.4, in which the RF signal is applied

to the gate and the LO signal is applied to the drain. The resulting IF signal is extracted from the drain with appropriate filtering. This method suffers from similar implementation difficulties as the FET gate and BJT base mixers, and also exhibits significant conversion loss. The usefulness of this mixer is mainly due to the very linear conversion characteristics possible.

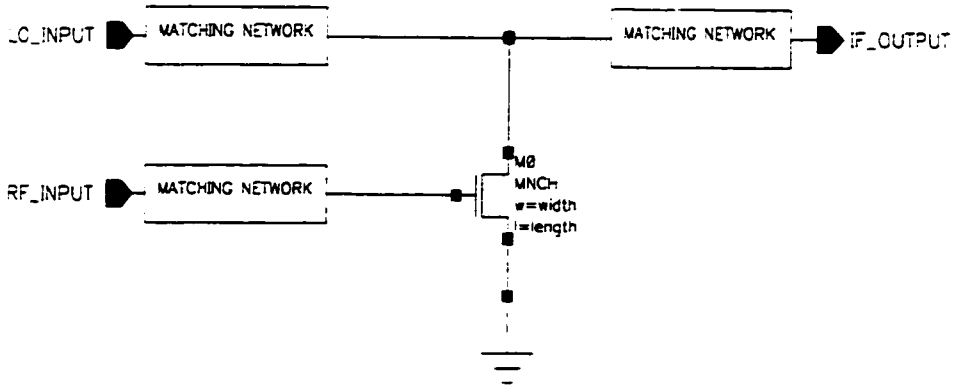

Figure 2.4 MOS drain mixer structure

2.3.4 FET Ring Mixers

The FET channel impedance characteristics also allow the device to be used as a switch, allowing signals to pass through the device when the channel impedance is low, rejecting signal passage when the impedance is high. This can be used to control the transmission of a signal by a gate control voltage, effectively resulting in the multiplication of the signal with the control voltage. If connected in a ring topology as shown in Figure 2.5, similar in structure and operation to a diode ring mixer, the input RF signal is commutated

to produce the IF signal. This structure can be highly linear but also suffers from similar design constraints as the diode ring mixer such as high LO power requirements, difficulty in port matching, poor port isolation, requirement of baluns at all ports, and conversion loss.

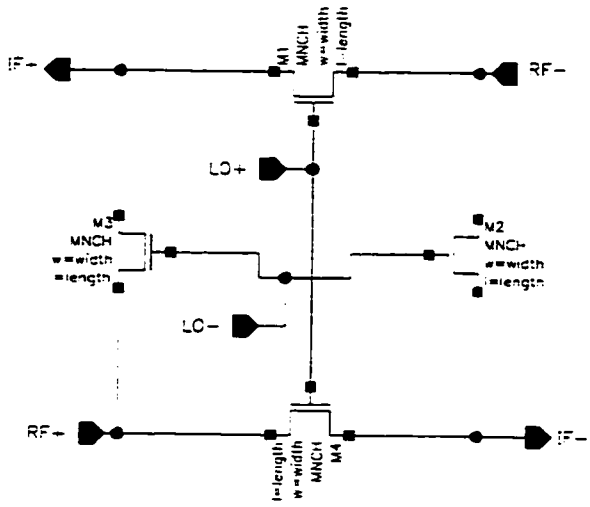

Figure 2.5 MOS ring mixer structure

2.3.5 FET Dual Gate Mixers

The FET device normally employs one gate to control the channel characteristics. Another form, the dual gate FET or DGFET, uses two gates to accomplish this function providing enhanced functionality and versatility. Depending upon the bias conditions, the DGFET can be used as an amplifier, a mixer, a modulator, or automatic gain control circuit (AGC) among many other uses[2.22 to 2.24]. As a mixer, the LO signal is normally

applied to the second, or top, gate, with the RF signal being applied to the first, or lower, gate. This not only provides the best linearity and mixing characteristics, but also allows the use of standard port matching techniques for the RF signal and helps improve the IF to RF port isolation [2.25]. The resulting IF can be recovered at the drain of the composite device after appropriate filtering. In an RFIC environment, suitable balancing structures can obviate or relieve the need for stringent filtering, similar to the tree mixer topologies. The ports of the DGFET are inherently isolated as the LO and RF signals are applied on separate ports and the feedback capacitance between the output and either input is small. In addition, the topology shows great promise for use with reduced power supplies as not all of the devices are biased in the saturation region and there is no inherent need for a current source bias method. Representative circuits, without bias details, are shown in Figure 2.6.

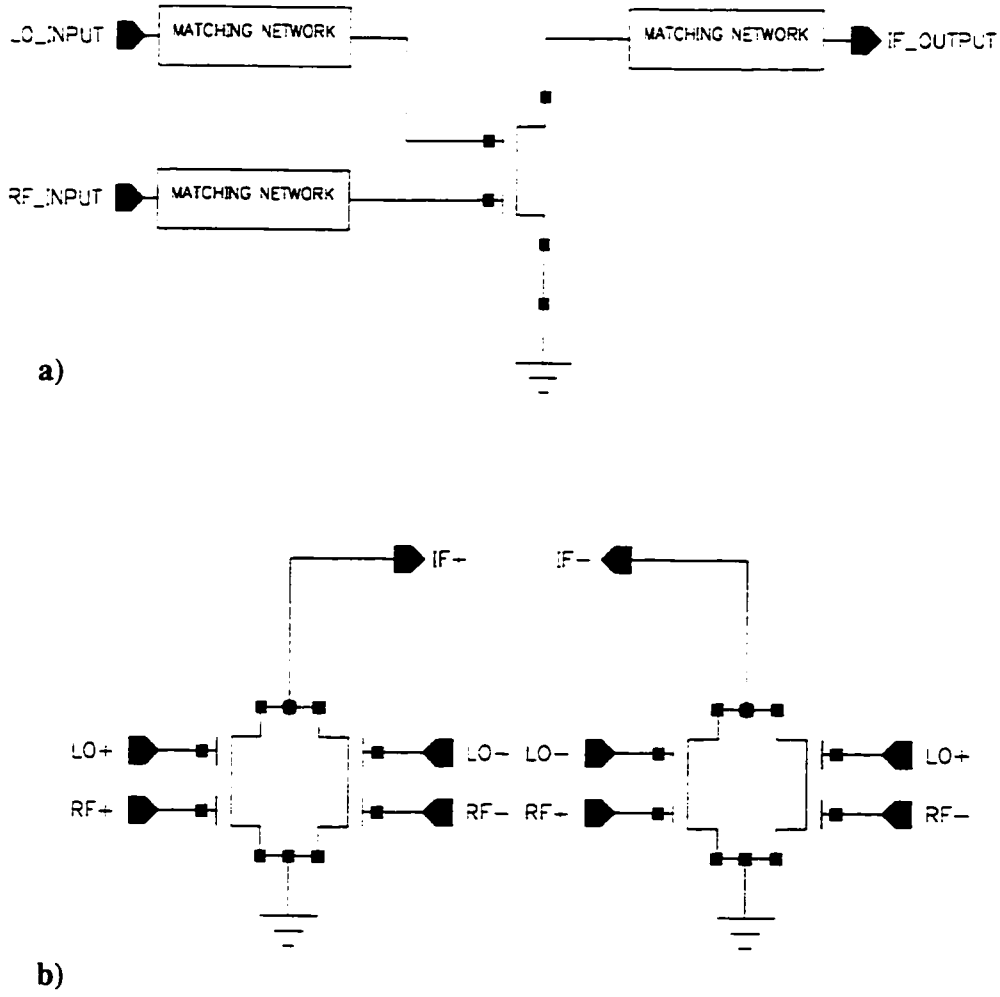

Figure 2.6 a) Unbalanced dual gate mixer structure

b) Balanced dual gate mixer structure

2.4 Summary

In order to take advantage of the economic benefits of producing a single IC radio system design or the use of lower cost technologies, research into MOSFET technologies for RF analog applications in the front end of radio systems can be expected to continue.

The design of high performance mixers in an RFIC environment is already a challenge in any technology, but as system complexity increases, the care and innovation required in the design of components such as mixers also increases. The tree or Gilbert cell mixer has been used extensively and is often the first topology used when implementing a MOS version of a high frequency mixer since the design methodology as well as the circuit operation are well understood. In addition, the drain and gate mixer topologies are also well understood, but they are not well suited for RFIC environments due to the low port isolation and filtering requirements. The FET ring topology is often the mixer of choice for high linearity systems but suffers from conversion loss as well as poor port isolation.

The dual gate mixer is the remaining viable option for RFIC mixer design due to inherent port isolation, capability of gain, and low supply voltage capabilities. However, the operation of the device is not well understood and no comprehensive design methods have been reported for use in the RFIC environment. In order to provide another mixer topology option to the RFIC designer and allow greater exploitation of the capabilities of MOS processes for high frequency analog operations, a method to accurately and system-

atically design a dual gate mixer was developed for use in an RFIC or discrete component environment.

Chapter 3: The Dual Gate FET

3.1 The Dual Gate Structure

In order to better understand the dual gate structure, Figure 3.1 shows a representative single gate structure consisting of a source, a drain, a gate, and a substrate or bulk connection. The source and drain are n+ diffusion regions with ohmic contacts for connection to other circuitry. The gate consists of a polysilicon material over a thin silicon dioxide layer located over the channel region, the area between the source and drain directly under the gate. The low impedance p+ substrate is used as a reference plane, usually ground, and also serves as the 'back gate' of the channel region. This structure can be shown to have the simplified small signal model shown in Figure 3.1.

The dual gate structure, shown in Figure 3.2, can be seen as an extension of this single gate device. Two gates between the source and drain effectively create two series connected devices with an internal node, labelled D1/S2 in the figure, that simultaneously serves as the drain for one device and the source for the other. A linear small signal model for this device can be formed by the series combination of two single gate small signal models. A generic physical representation and a simplified small signal model are shown in Figure 3.2.

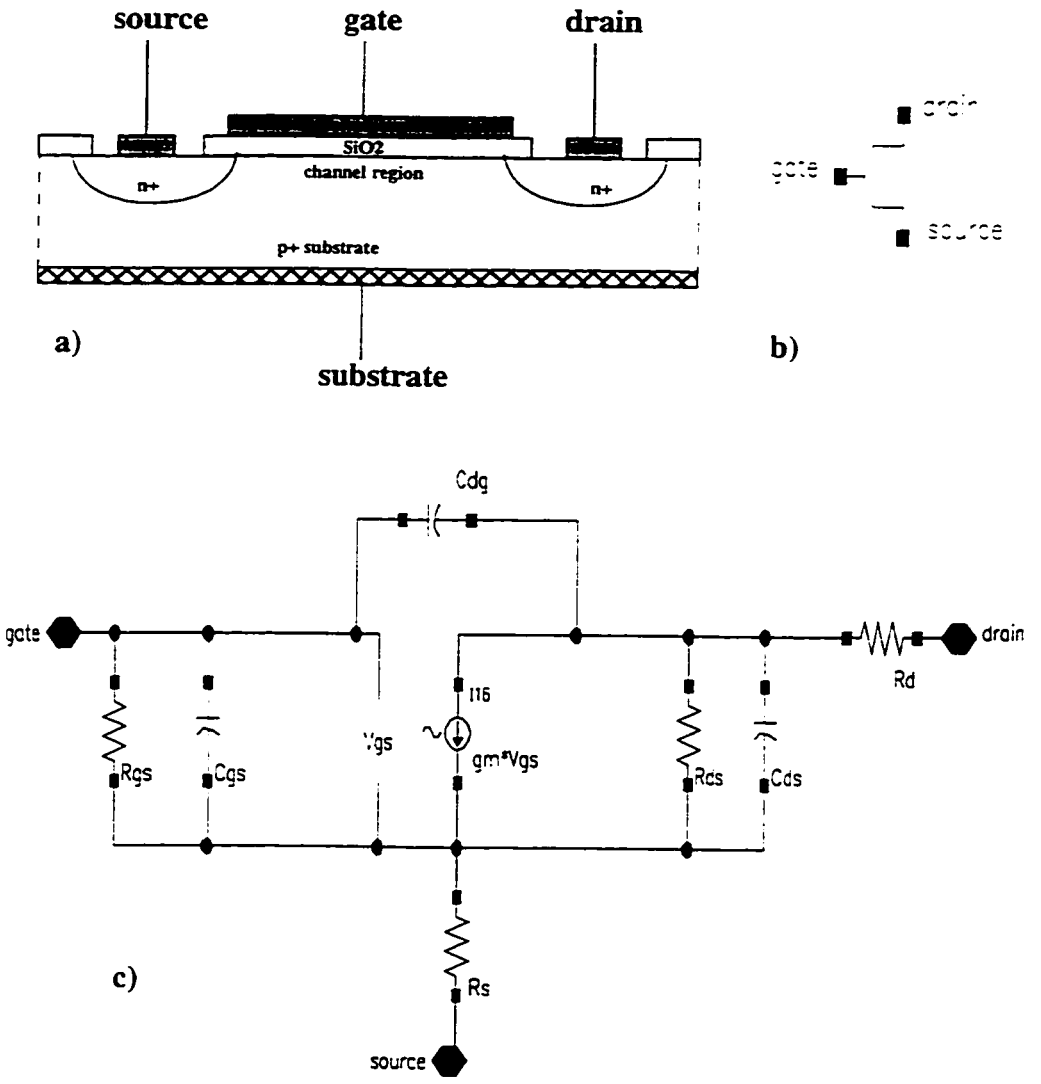

Figure 3.1 a) Generic MOS single gate physical representation
b) Generic MOS single gate schematic symbol
c) Simplified MOS single gate small signal model

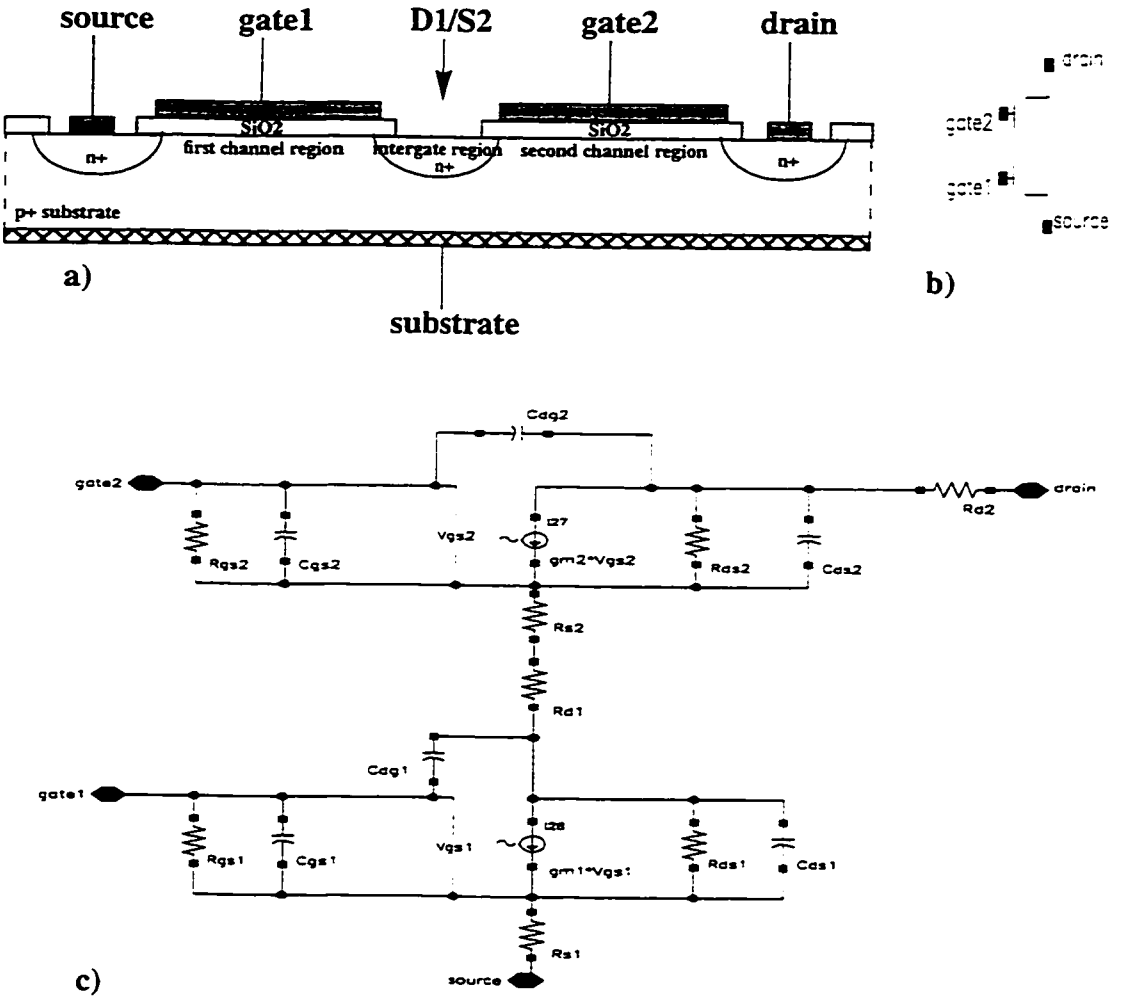

Figure 3.2 a) Generic MOS dual gate physical representation
b) Generic MOS dual gate schematic symbol
c) Simplified MOS dual gate small signal model

The use of these small signal models in a mixing application context is somewhat limited due to the highly nonlinear nature of the circuit and to the fact that the excitation of nonlinearities in each device is bias dependent. However, with proper care, linear

models can be used to qualitatively investigate the effects of such characteristics as gate capacitance, port isolation, output impedance, and substrate effects.

3.2 Modeling Concerns

3.2.1 The Single Gate MOSFET

The current state of the art high frequency models for single gate MOSFETs implemented in CAD simulators do not accurately account for non-ideal device characteristics. Some models do not even calculate the transconductance, output conductance, or the drain current through the transition region between the linear and saturation regions of operation accurately. The current model implementations for such effects as 1/f noise, channel noise, short channel effects, doping gradients, gate resistance, and parasitic capacitances are often insufficient for accurate design and are not generally trusted for production level high frequency analog designs. Tsividis [3.1 to 3.3] provides a valuable overview of various modeling deficiencies in MOSFET models.

This lack of accurate device models can be traced to the history of the MOSFET and its primary reason for existence, namely low frequency digital applications. If the device is being used as a digital circuit component, essentially being either on or off, with a small transition time between states, then the effects of noise, channel impedance, nonlinearities, and gate resistance are not important. As such, there was little incentive to improve the models as the important regions for digital applications were quite sufficiently modeled. As the demand for high speed digital applications increased, the device speed

was increased by scaling the device size, allowing the non-ideal portions of the characteristic to remain hidden in the large signal operation of the digital application.

Only recently has the economic incentive been sufficient to warrant additional research into the full modeling of the MOSFET device, including all effects, in all regions. High quality analog MOSFET models are emerging such as the Nortel MISNAN model [3.4] and new research is continuing[3.5]. With these efforts, more accurate simulation tools are being created in order to enhance the capabilities of the RF MOS designer to create high performance RF MOS analog circuitry.

3.2.2 The Dual Gate MOSFET

Although the dual gate device can be viewed as a series connection of two single gate MOSFET transistors, there are a number of issues specific to the dual gate device that require it to be defined as more than just a 'simple' series connection. Each device of the composite transistor suffers from all of the modeling deficiencies that currently affect single gate devices. In addition, the interconnection of the two devices creates a region of interaction that proves to be difficult to model[3.6,3.7].

In Figure 3.2a, an intergate region is defined as the area between the two channel regions which consists mostly of an n+ doped diffusion. As the RFIC designer often has complete control over the layout of the transistors used, the size of this region depends heavily on the way the transistor is laid out and how the surrounding gates are connected to other circuitry. In addition, the process may not control the doping in this region very closely due to the self aligning properties of many MOS fabrication techniques. As a result, wide variances on the parasitic resistances and capacitances in this region are possi-

ble. Depending on the circumstances, these parasitics may or may not be the dominant impediment to improved simulation accuracy.

Due to the topology, each device experiences a different substrate to source voltage which, among other effects, causes the threshold voltage of each device to be different. This effect must be modeled correctly or device characteristics can be grossly distorted in simulation. In addition, the drain current through a device is dependent upon the gate to source voltage, v_{gs}, as well as the drain to source voltage, v_{ds}. In this topology, the v_{gs} for the top device and the v_{ds} for the bottom device are dependent upon the unknown intergate region voltage and must be solved for numerically by iteration. Although this is not impossible to do, it increases the complexity of the device calculations required and impacts the speed capabilities of the simulation.

As a result of the poor modeling of the conductances in the individual FETs, there is some question as to the effectiveness of the simulation of the interaction of the two devices in the intergate region. Assuming that the RF effects of power transfer depend upon the calculated nodal impedances of the circuit, incorrect conductances at the internal node may cause major errors in simulation. This effect may also depend upon the bias conditions due to the discontinuities in some models between the linear and saturation regions of operation. If the lower device is biased at an inappropriate manner for the simulator, the simulator may produce anomalous circuit responses and the designer may be misled as to the operation of the circuit.

If the DGFET is operated as a small signal amplifier, these modeling effects may be easily avoided by employing appropriate biasing techniques. In a DGFET mixer however, the large signal operation sweeps the operating points of the mixer through the

regions in which the model is deficient. The designer, by using conservative design techniques and relying more upon the currents and voltages that are simulated, and not the derived quantities such as the conductances, can use simulations to provide a means of estimating circuit behaviour.

3.2.3 The Cascode Approximation

Although the current MOS models do not inspire much confidence, circuits need to be designed and research must continue. The RF MOS designer can take some positive steps to minimize the detrimental effects of the simulator models currently available.

In the context of dual gate MOSFETs, the designer can minimize the use of special devices, instead relying upon devices more similar in size and shape to the devices that have been characterized for the model. The main result of this is the 'cascode approximation' [3.8 to 3.10] to the dual gate in which all simulations and the physical layouts are done using two separate devices in an explicit series connection of two devices. This allows the use of schematically driven simulation engines without modifications such as special model parameter files, symbols, or model files. In addition, this allows the unmodified use of current layout capabilities such as device extraction, layout vs. schematic (LVS), design rule checking (DRC), as well as parasitic extraction.

In terms of the physical layout, the use of distinct devices to approximate the dual gate may help in a number of ways including ease of layout, improved signal routing, as well as enhanced design reliability. The use of separate devices allows increased care in the layout of each device including substrate contacts, thermal gradients, and number and

location of gates and source and drain contacts. The designer can also increase the separation of the gate circuitry in order to improve port isolation characteristics or to ease the routing of signal or decoupling lines.

The rapid integration of dual gate simulations into the work place can be greatly facilitated by relying upon the simulation environment capabilities currently available. If no user specific files are created, designers can immediately make use of simulator or model upgrades allowing for the highest degree of accuracy and confidence in the design. For these reasons, among others, it is suggested that a suitable design approach to dual gate circuits can be made using the cascode approximation.

3.3 Summary

Although the structure of the dual gate device has been shown to be similar in physical construction to the well known single gate device, several effects require that the DGFET be modeled slightly differently than the single gate device. The effects of substrate bias and the intergate region interactions need to be better controlled and more accurately modeled for amplifier or mixer applications.

While the use of the dual gate device for analog applications is currently hampered by the lack of adequate high frequency modeling capabilities, this difficulty is seen to be common to RF MOS devices in general. As the implementation of better high frequency models continues, several suggestions, primarily the use of the cascode approximation, were provided for the RFIC designer to help ameliorate this situation. This provides an interim solution and facilitates the rapid integration of modeling and simulation improvements to the design environment.

Chapter 4: Design Methodologies

This chapter explains the criteria used in defining a useful engineering design method and explores some of the state of the art design methodologies for dual gate mixers including a short discussion on numerical solution techniques. A theoretical background as well as a concise summary is provided for the proposed method and some of the pertinent features of the method are discussed.

4.1 Design Methodology Requirements

An RF design engineer relies upon design methodologies and techniques that have been understood, tried, and confirmed to work. If a design method is inaccurate, cumbersome, or time consuming, it is unlikely to be widely accepted. A good design method helps the engineer design high quality, reliable circuits in the shortest possible amount of time. In order to accomplish this, a good design method should have certain basic qualities. The method should be as simple and accurate as necessary, should provide insight into the operation of the circuit, and be suitable for as wide a variety of situations or circuits as possible. It should not be excessively reliant on computer models and should require a minimum of effort to characterize devices for use in the method.

An engineering design method should only be as simple or as rigorous as necessary. If a method is too simple, inaccuracies result and insufficient information is given to the designer for informed optimization. If the method is too complicated, it may require too much time to implement. If a method involves too many detailed steps, or if the final solution is obscured with excessively detailed mathematical equations, the method may

prove to be unwieldy to the designer and be prone to errors or inaccuracies. The price of excessive accuracy may be increased simulation or lab time for a sometimes questionable amount of overall design improvement.

The method should explain or clarify the operation of the circuit to a sufficient degree of detail. This allows the engineer to make informed circuit modifications for intelligent design optimizations. Unknown side effects from uninformed design modification can result in specification failure. Without the required information, the designer must often resort to implementing excessively conservative designs, not realizing the full capabilities of the design.

A useful design methodology is one that can be applied, perhaps with minor modifications, to a wide variety of circuits. Most designers use a 'toolkit' of a limited number of design techniques that have been thoroughly tested and in which they have some degree of confidence. An isolated technique that is difficult to learn and apply does not become part of such a toolkit.

A common problem with RFIC designs is the lack of accurate CAD models for the devices used in the design. Although most device simulation models can predict the current and voltage levels in the devices to a sufficient degree of accuracy, some of the derived quantities such as transconductance or conductance, are very poorly modeled [4.1]. A higher degree of confidence is often given to a design method that does not rely upon these derived quantities. As the designer may have to characterize the devices in the lab before the design can continue, a method that requires a minimum amount of device characterization can significantly reduce design cycle time.

A successful design method should, therefore, be of sufficient rigor and accuracy, should provide information for optimization, have minimal reliance upon CAD tools, and be as flexible as possible.

4.2 Current State of the Art

A brief description of the numerical methods used in CAD design tools is provided in order to better understand the theoretical background of some of the mixer design methodologies that are reviewed, followed by brief summaries of some key mixer design approaches to provide a more comprehensive view of the challenges involved in the design procedures.

Following the theoretical background required to explain the proposed design method, the proposed dual gate mixer design procedure for gain and input compression point is outlined and summarized.

4.2.1 Harmonic Balance and Large Signal - Small Signal Techniques

The harmonic balance (HB) and large signal-small signal (LS-SS) circuit analysis techniques are used to provide numerical solutions to nonlinear circuits for CAD applications. For a more in depth treatise on these topics, refer to Maas[4.2].

The harmonic balance technique can be viewed as a partitioning of the circuit into linear and nonlinear sections. The nonlinear partition, containing the active devices, is described with equations for the equivalent circuit components and is usually solved using time domain techniques. The linear partition contains the rest of the circuit including, for example, bias and matching circuitry, and is often solved in the frequency domain. The in-

put signals are applied to the circuit and the resulting currents and voltages are calculated in each partition. Conceptually, when the currents and voltages at the interface of the linear and nonlinear partitions match, or are balanced, at all frequencies harmonically related to the input signals, thus 'harmonically balanced', the steady state can be considered achieved, resulting in a numerical solution for the circuit transfer function.

The large signal - small signal (LS-SS) technique is also referred to as conversion matrix analysis and is applicable for nonlinear circuits that have two signal inputs, one being very large compared to the other, and the other being small enough so as to create negligible harmonics in the circuit. This is a situation commonly found in mixer circuits where the LO is large compared to the RF signal and the excess harmonic content caused by the RF signal is small. Initially, the steady state of the complete circuit is found with only the large signal applied, often using HB techniques. Using the steady state results, functions for the nonlinear equivalent circuit components are generated. The nonlinear equivalent circuit model is then converted into a quasi-linear, small signal equivalent circuit, using the derived steady state functions instead of the linear equations for the quasi-linear components. Using linear analysis techniques, equations can then be formulated which provide a numerical solution for the transfer function for the circuit. The application of two signals of different frequencies to a nonlinear circuit will result in the multiplication of the two signals together producing many conversion frequency components. This is represented by the use of matrices instead of scalar values in the linear analysis equations, thus the term 'conversion matrix' analysis.

4.2.2 Dual Gate FET Mixer Design Methodologies

Various design methods have been explored for dual gate FET mixers, usually aimed at producing accurate CAD models for design applications and often relying upon variations on the HB or LS-SS numerical analysis methods. Accurate modeling, however, does not always provide the means or method for high performance designs. A few key approaches will be mentioned here as background information for the method proposed in this thesis.

4.2.2.1 Dual Gate MOSFET Method: Kleinman

Kleinman's [4.3] method relies upon the understanding that the current and thus the transconductance of the complete dual gate device is a function of both gate biases. Employing a simple equation relating the DC transconductance from each gate to the output as a function of the other gate voltage, the IF frequency components can be isolated and the conversion transconductance, g_c, can be calculated. This can be seen as a simplification of an analysis based upon a two dimensional Taylor series [4.2]. Kleinman approximates the rather complicated transfer function by ignoring the nonlinearities at each gate and using the linear region of the DC transconductance of each gate to the output.

This method is not difficult to apply but provides no insight into the proper selection of bias points for either the RF or LO ports. As a result, little information is available on how to adjust the bias or LO power conditions to optimize the circuit design. It is, however, aimed at providing a practical design approach for the circuit designer to esti-

mate the conversion gain of the mixer using circuit parameters that are directly available to the designer and are easily measurable.

The concept of treating the dual gate device as a 'multiple entity', where each gate has a separate but codependent function in relation to the output current, is very useful and allows for the characterization of any dual gate device, without having to try and isolate each device separately. The section of the paper concerning gain controlled amplifiers is informative and provides an intuitively appealing description of the operation of the dual gate device. A key portion of this method was the treatment of the transconductance due to the second gate voltage as a separate entity, and not just as a method to modify the transconductance from gate 1 to the output.

4.2.2.2 Dual Gate MESFET Method: Tsironis, Meierer, Stahlman

These authors [4.4,4.5] explain a detailed method for the numerical modeling of a DG MESFET device and its use in the design of a mixer. The analysis that is provided is also applicable to MOSFET technologies and provides significant insight into the details of the operation of DG MOSFET devices and, in particular, mixers.

The method of visualizing the usually unavailable drain to source voltage of the bottom device with the aid of a DC nomogram is particularly useful and provides some critical information for the designer. The resulting information concerning the effect of the second gate voltage on the internal operation of the circuit is very revealing. The identification of regions of operation and the descriptions of some of the characteristics of each region is instructive for the selection of bias regions as well as LO signal levels. The investigations into the effects of the external matching circuitry are also very useful and provide

the designer with a considerable wealth of knowledge to draw upon while considering how to interface properly with the mixer. The detailed approach, along with the realistic assumptions and approximations used, provides solid background knowledge for a clearer understanding of the operation of dual gate mixers and permits more informed decision making in the design process.

This method can be considered a type of HB and LS-SS analysis. The individual FET equivalent circuit components are identified and functions are generated for each component. The effects of the LO waveform are assumed and are implicit in the functions that are generated. The treatment of the LO effects on the internal components as a steady state condition and then investigating the RF effects on the overall circuit are key techniques to the success of the method.

Although a design implementation of the method is described, the effort appears to have been aimed more at modeling a specific mixer and confirming the model than providing a general design method. The approach is somewhat complicated, is 'tedious' in its applications [4.5], and requires significant lab work to characterize each device. It must be acknowledged that this work was undertaken in 1983 and significant advances in CAD tools and device modeling, in part due to this work, have occurred since then, possibly reducing the 'tedious' nature of the technique.

4.2.2.3 Microwave Mixer Methods: Maas

Maas has published several definitive works [4.6 to 4.8] on nonlinear microwave circuits including the operation of FET mixers, usually focussing on numerical mod-

eling methods and providing significant theoretical detail for the modeling methodologies involved.

The analysis of FET mixers has been identified as a subset of a more general nonlinear analysis approach. Using LS-SS and HB analysis techniques, the operation of MESFET single gate mixers and the methods used to model them are discussed in detail. The extension of these techniques to dual gate devices and a general description of the operation of dual gate devices is also included. While general design guidelines are provided, an in-depth design method for the DGFET is not provided nor suggested.

These numerical methods, meant to provide accurate CAD models, provide improved tools for the designer but are not always directly applicable to the actual design of such mixers. Although the results for a DGFET mixer are provided in final equation form and allow for identification of general trends, they are not directly useful for proper selection of bias points, power levels, nor for a detailed understanding of individual circuits.

The description of the HB and LS-SS approaches found in this work [4.7] is a major portion of the theoretical underpinnings of the method described in this thesis.

4.2.3 Drain Mixer Methodologies

Drain mixer design methods are useful to investigate because it is possible to view the DGFET mixer as a variation of the drain mixer. Considering the bottom device as the mixing element, the top device can be seen to be the means of applying the LO to the drain as well as being a common gate amplifier stage for the extraction of the IF signal. As

the mixing action in both types of mixers occurs in a similar manner, drain mixer topologies can be instructional in DGFET mixer designs as well.

4.2.3.1 MESFET Drain Mixer Method: Begemann, Jacob

This numerical method [4.9] is also a type of HB and LS-SS analysis. It uses an equivalent circuit for the FET in the linear operation region, identifies the effect of the LO waveform on each component, and creates functions for all of the individual components. Linear analysis techniques are used to create the required matrix equations to calculate the mixer characteristics.

The separation of the frequency components using ideal filters, similar to Pucel's treatment with gate mixers [4.10], is insightful and allows the designer to view the circuit in a variety of ways, depending on which frequency component is being investigated.

An interesting conclusion drawn in this paper is that the drain to source channel resistance, R_{ds}, is not a major contributing factor to the overall conversion gain, while the dominating factor is the device transconductance itself.

Although the paper concentrates on the theoretical analysis of the mixing processes in a drain mixer, the mixing process itself is very similar to that of the DGFET in one region of its operation, providing a deeper understanding of the DGFET mixing action. However, little insight into the proper selection of RF or LO bias points or LO power level requirements is provided.

4.2.3.2 MESFET Drain Mixer Method: Cayrou, Gayral, Graffeuil...

This analysis [4.11], also just for drain mixers, is very similar to the one by Begemann and Jacob but differs slightly in the mathematical approach. The separation of the effects of the transconductance and the channel conductance provides a means to calculate the effect of each separately. This provides a means of simplification of the final result and helps identify the main contributions to the mixing process. The authors used the HB technique to confirm the theory by simulation.

This work also supports Begemann and Jacob's conclusion that the contribution of the channel conductance, G_{ds}, to the mixing process is minimal, while the time varying transconductance of the device is the dominant factor.

Although it is indicated that this method can be used to identify the proper selection of LO power, the paper does not provide much information on the criteria used for the selection of, or the effects of, the bias of the LO or the RF ports.

4.3 Proposed Design Method

4.3.1 Features of Proposed Design Method

The method proposed in this thesis attempts to address the inadequacies of the current state of the art design methods while drawing on the strengths and advantages that each method possesses.

This method relies upon identifying the practical aspects of the HB and LS-SS numerical analysis methods and applying them correctly to achieve the desired result. Most methods that have been discussed use HB and LS-SS to get numerical results. How-

ever, the design methods themselves do not make direct use of these techniques. The novel aspect of this design method is the implicit practical application of these numerical method concepts to produce the circuit transfer function in a form useful to the engineer for design purposes. Often, the approach of the design of DGFET mixers is based upon finding the effect of the LO on the RF waveform. The proposed method, however, explores and exploits the effect of the RF waveform upon the circuit steady state induced by the LO. It is this shift in perspective that clarifies the method and gives it general applicability.

The proposed method employs a simple, methodical approach to calculate the gain and input compression point of a DGFET mixer with each step in the process being easily implemented by either simulation or lab bench techniques. It provides an accurate, understandable procedure for identifying and verifying the appropriate bias conditions and also provides the means to define the minimum LO power level required. The technique is aimed at producing a well engineered design, not a rigorous numerical solution.

In the methods that have been discussed, little information is provided on why or how the steady state of the system was chosen or obtained. The proposed method clearly illustrates the criteria for the selection of the LO power and bias as well as the RF bias point. The important parts of the steady state are then defined by measurable circuit parameters and used in sufficient, but not excessive, detail.

The proposed method requires a minimum of device characterization, using easily measured or simulated DC drain current and gate voltage data. Other required RF data, such as the port impedances, are easily measured using standard lab or simulation techniques.

The method proposed in this thesis provides a useful engineering design method for nonlinear circuits, in particular dual gate FETs, with a general reduction in method complexity, a reduction in application difficulty, an increase in confidence, and includes a solid, widely accepted, theoretical background.

4.3.2 Theoretical Background

4.3.2.1 Introduction

The main purpose of the derivation is to provide a short, simplified, theoretical background sufficient enough for the designer to understand the reasons for each step in the method and is specifically aimed at the particular application of the dual gate FET mixer. It is also sufficiently general to be applicable to other types of circuits with minor modifications. More detailed equations can be found in Appendix A. For more detailed information on the topic, an excellent description of these techniques can be found in the works of Maas[4.7].

4.3.2.2 Equations for Gain Calculation

If a single large input signal is applied to a nonlinear circuit, the resulting steady state of the system can be described in the following general way:

$$output(\text{largeSignal}) = (someTransferFunction) \cdot (\text{largeSignal}) \tag{4.1}$$

If a much smaller signal is then imposed on the system in addition to the large signal, we can describe the system as:

$$output(\text{largeSignal,smallSignal}) = (someModifedTransferFunction) \cdot (\text{largeSignal}) \quad (4.2)$$

The small signal's contribution to the output, implicit in the modified transfer function, can be isolated by subtracting out the steady state condition:

$$output(\text{smallSignal}) = output(\text{largeSignal,smallSignal}) - output(\text{largeSignal}) \quad (4.3)$$

In this case, the desired output is the drain current, I_{ds}, of a cascoded connection of two MOSFETs when the top gate is driven by a large LO voltage, V_{lo}, and the bottom gate is driven by a much smaller RF voltage, V_{rf}. In the following derivation, the notation of V_{lo} and V_{rf} includes the amplitude and frequency of the respective signals. The system at steady state, with no RF input signal applied, can then be described using:

$$I_{ds}(V_{lo}) = gm2(V_{lo}) \cdot V_{lo} \quad (4.4)$$

where V_{lo} is the large signal applied to the circuit, $I_{ds}(V_{lo})$ is the output current as a function of the large signal [4.12], and $gm2(V_{lo})$ is the the pseudo-transconductance from the second gate to the drain equal to the output drain current, $I_{ds}(V_{lo})$, divided by V_{lo}.

With the addition of the small RF signal, the system can be described using the following equation:

$$I_{ds}(V_{lo}, V_{rf}) = (gm2(V_{lo}) + (\Delta gm2(V_{rf}, V_{lo}) \cdot V_{rf})) \cdot V_{lo} \quad (4.5)$$

where the term $\Delta gm2(V_{rf}, V_{lo})$ indicates the function that describes the 'delta', or shift, away from the steady state caused by V_{rf}, the RF input signal.

In order to isolate the effects of the small RF signal, the original steady state is subtracted in the following manner:

$$I_{ds}(V_{rf}) = I_{ds}(V_{lo}, V_{rf}) - I_{ds}(V_{lo}) \tag{4.6}$$

which reduces to:

$$I_{ds}(V_{rf}) = \Delta gm2(V_{rf}, V_{lo}) \cdot V_{rf} \cdot V_{lo} \tag{4.7}$$

where $I_{ds}(V_{rf})$ is the change in the steady state output current caused by the RF signal.

Looking further at Equation 4.4, the nonlinear transfer function for the steady state system can be seen to be composed of many components at harmonics of the LO frequency and can be expanded as:

$$gm2(V_{lo}) = \sum_{n=0}^{\infty} gm2(V_{lo})\big|_{nf_{lo}} \tag{4.8}$$

Similarly, the application of the RF signal will cause shifts around the steady state resulting in:

$$gm2(V_{lo}) + (\Delta gm2(V_{rf}, V_{lo}) \cdot V_{rf}) = \sum_{n=0}^{\infty} [gm2(V_{lo})\big|_{nf_{lo}} + [\Delta gm2(V_{rf}, V_{lo}) \cdot V_{rf}]\big|_{nf_{lo}}] \tag{4.9}$$

The resulting output signal contains many frequency components related to the LO and RF input signals. The desired output component of the resulting waveform is caused by the multiplication of the fundamentals of the RF and LO signals only. After dis-

carding frequency components other than the sum and difference frequencies, the system can be described as:

$$I_{ds}(f_{rf-lo}, f_{rf+lo}) = (\Delta gm2|_{f_{lo}}) \cdot V_{rf} \cdot V_{lo} \tag{4.10}$$

where $I_{ds}(f_{rf-lo}, f_{rf+lo})$ indicates the output current at the sum and difference frequencies only and $\Delta gm2|_{f_{lo}}$ is the LO frequency component of the $\Delta gm2(V_{rf}, V_{lo})$ function. This can be viewed as a standard double sideband result of which only one sideband is desired. Using the results of Equation 2.1 to get the magnitude of one sideband at the frequency f_{if}, and assuming that both sidebands have equal conversion gains and minimal losses to the output, we can describe the system as:

$$I_{ds}(f_{if}) = \frac{\Delta gm2|_{f_{lo}} \cdot V_{rf} \cdot V_{lo}}{2} \tag{4.11}$$

or:

$$I_{ds}(f_{if}) = g_c \cdot V_{rf} \tag{4.12}$$

where g_c, the conversion transconductance, is described as:

$$g_c = \frac{\Delta gm2|_{f_{lo}} \cdot V_{lo}}{2} \tag{4.13}$$

Using this result, we can calculate the magnitude of the potential output voltage of the circuit using the following relationship:

$$\left|V_{out}\right|_{f_{if}} = g_c \cdot |V_{rf}| \cdot \left|Z_{out}\right|_{f_{if}} \tag{4.14}$$

where:

$\left|V_{out}\right|_{f_{if}}$ = magnitude of the voltage out at the desired IF frequency,

g_c = input to output frequency conversion transconductance,

$|V_{rf}|$ = magnitude of the RF input voltage,

$\left|Z_{out}\right|_{f_{if}}$ = magnitude of the output impedance at the IF frequency.

4.3.2.3 Method for Calculation of Input Compression Point

The input compression point can be calculated from the calculated conversion transconductance, g_c, and selected load impedance. As the method may be difficult to visualize without graphs of the characteristic g_c function, a brief description of the technique will be provided here, with more detail and graphs provided in Chapter 5 of the thesis.

Each RF bias point generates a corresponding value of g_c for a specified LO bias and power level. By using a significantly larger RF signal, the mixer is essentially being swept through a range of operating conditions, each one with a specific conversion transconductance. It is the average of all of the traversed operating conditions that provides the estimate for the input compression point.

Using the RF bias point as a start point, the RF signal can be viewed as excursions above and below the bias point. The effect of a large RF signal can be approximated by taking the average of the calculated g_c values over a range of RF bias values above and below the bias point. The input compression point is found when the average value is 0.89, or 1dB, below the value at the bias point. Alternatively, the expected gain can be calculat-

ed using the expected load impedance, and the gains over the same range averaged. In a similar fashion, the P1dB is located when the average gain calculated is 1 dB below the bias point gain.

4.3.3 Concise Summary of Method

The proposed design method can be summarized in the following steps. Each step, using the appropriate techniques, is compatible with both a simulation and a lab bench environment. The summary closely follows the order of the equations as developed above. The actual details of each step are further described in the application of the method in Chapter 5 of the thesis.

1. Choose a device based upon gain, frequency, and power specifications.

2. Measure the DC drain current, I_{ds}, to create a family of curves designated $I_{ds}(V_{g1}, V_{g2})$.

3. Calculate $gm2(V_{g1}, V_{g2}) = \frac{I_{ds}(V_{g1}, V_{g2})}{V_{g2}}$, plot as $(x, y) = (V_{g2}, gm2(V_{g1}, V_{g2}))$.

4. Calculate $\Delta gm2(V_{g1}, V_{g2})$ over the range of RF bias points using Equation 4.15 and plot as $(x, y) = (V_{g2}, \Delta gm2(V_{g1}, V_{g2}))$

$$\Delta gm2(V_{g1}, V_{g2}) = \frac{(gm2(V_{g1}, V_{g2}))|_{positiveexcursion} - (gm2(V_{g1}, V_{g2}))|_{negativeexcursion}}{2} \quad (4.15)$$

5. From the plot of $\Delta gm2(V_{g1}, V_{g2})$, locate the V_{g2} values that correspond to:

- the maximum $\Delta gm2(V_{g1}, V_{g2})$ point, to get $V_{g2}(max)$
- the 'zero point', to get $V_{g2}(min)$
- the mid point between these two, to get $V_{g2}(bias)$.
- the V_{g1} corresponding to the curve with the maximum $\Delta gm2(V_{g1}, V_{g2})$ value.

6. Measure the port impedances at the initial bias points found in step 5.

7. Create a 50 ohm impedance at each port at the corresponding frequency:

   - gate 1: RF
   - gate 2, drain: LO

8. Set the LO power based upon step 5.

9. Vary the V_{g1} DC bias. Monitor and record the output level at the LO frequency.

10. Calculate the current at the LO frequency to create $I_{ds}(f_{lo})$.

11. Calculate $(\Delta gm2|_{f_{lo}} \cdot V_{lo}) = \frac{I_{ds}(f_{lo})}{V_{g1}}$

12. Calculate $g_c = \frac{(\Delta gm2|_{f_{lo}} \cdot V_{lo})}{2}$, and plot as $(x, y) = (V_{g1}, g_c)$

13. Verify and adjust the V_{g1} bias point if required

14. Verify the g_c calculation by:

   - Adjusting the load at the IF frequency
   - Calculating the expected output level
   - Recording the IF output power, comparing this to the calculated value

15. Once g_c is confirmed, the design can continue by:

   - Using an impedance transformation on the LO port to reduce the required LO power,
   - Choosing appropriate RF input and IF load impedances for the required gain and input compression specifications.

4.4 Summary

The current state of the art design methods for dual gate mixers have been discussed and shown to be lacking in general applicability and ability to provide sufficient information for design optimization. The use of numerical techniques for the modeling of

specific devices and mixers has provided the ground work for the current design method as it uses these numerical methods in a practical manner suitable for a lab bench or simulation environment.

The design method as it is described fulfils the requirements of a useful design procedure as it has a solid theoretical foundation, is as rigorous or detailed as the designer chooses it to be, does not require excessive device characterization, is flexible in its implementation, and provides the means for intelligent optimization of the circuitry.

Chapter 5: Application of the Method

This chapter deals with the practical application of the proposed design method. Although the method is directly applicable to both a simulation or lab bench environment, the following discussion concentrates on the application of the method in a lab bench environment.

5.1 A Characterization Example

This description of the application of the design method is structured to closely follow the method summary. Following some discussion on each step, the results of the step in a design example are provided.

5.1.1 Determination of Bias Conditions

5.1.1.1 Device Selection

One of the more important criteria in choosing or designing a potential device is the inherent available gate 1 transconductance of the dual gate device as if it would be used as an amplifier. The device chosen should have a transconductance, g_m, of at least four to five times more than the expected conversion transconductance required for the mixer [5.1, 5.2]. This can be verified by either checking the device data sheet or measuring or simulating DC g_m values.

The device chosen is the Philips BF901 Dual Gate MOSFET [5.3], a discrete enhancement mode device intended for LNA applications to 1 GHz. It has a DC g_m of 28 mS, a low noise figure, and has no extra gate circuitry such as is found with the BF904.

Although a Spice model parameter file of this device is available, it was found to be unacceptable for design purposes due to discrepancies between the simulated and measured DC currents and port impedances. As a result, no simulated results are available.

5.1.1.2 DC Characteristics

Initially, curves of I_{ds} as a function of V_{ds} for stepped V_{gs} can be created for each separate device in the DG FET. This is easily done in a simulator, but can be difficult to perform on the lab bench. It does, however, allow the visualization of the regions of operation for both devices and allows for an initial estimate of the range of operation for the mixer. Although the use of Tsironis' DC nomogram [5.4] is insightful at this stage, it is not necessary for, and is not directly used in, the design method.

Alternatively, the total device drain current can be viewed as a function of both the gate voltages, as in Kleinman's [5.5] approach. This can be implemented by plotting the output current as a function of the gate voltages creating two separate families of curves. The more important one for this method is the current as a function of V_{g2} with stepped values of V_{g1}, shown in Figure 5.1. For clarity, the data points corresponding to the V_{g2} bias points are only shown for representative curves.

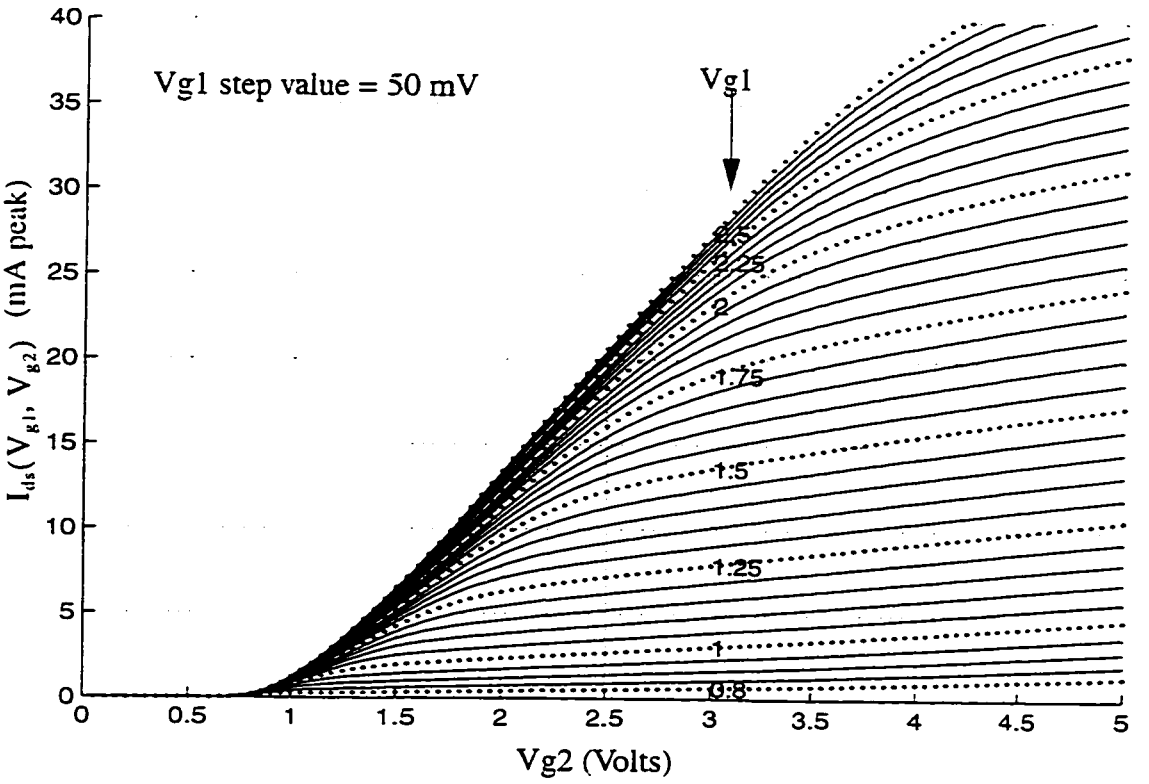

Figure 5.1 Graph of measured DC drain current as a function of V_{g2} for stepped values of V_{g1}

5.1.1.3 The gm2 Function

The pseudo-transconductance of the composite device referred to the second gate, designated as $gm2(V_{g1}, V_{g2})$, is calculated by dividing the output current by the second gate voltage. It is important to realize that this operation is a division, not a derivative, and is actually a modified form of the normal transconductance. The function is created by measuring or simulating the drain current for swept gate 2 voltages at stepped values of gate 1 voltage and then dividing each data point by the corresponding V_{g2} voltage.

The graph of the $gm2(V_{g1}, V_{g2})$ family of curves, plotted in Figure 5.2, shows that, at a given gate 1 bias point, the pseudo-transconductance of the composite device relative to the second gate first peaks and then decreases as the second gate voltage increases. This is due to the bottom RF device moving from the linear into the saturation region, effectively increasing the source degeneration of the top single gate device. The graph also shows that $gm2(V_{g1}, V_{g2})$ is effectively zero at low values of second gate voltage. This is caused by the upper device turning off as its gate voltage goes below its own threshold voltage. However, the most important information on this graph is not the function itself, but the amount of change between each line. This change represents the amount of change of the $gm2(V_{g1}, V_{g2})$ function caused by the RF level, or the $\Delta gm2(V_{g1}, V_{g2})$ as described earlier.

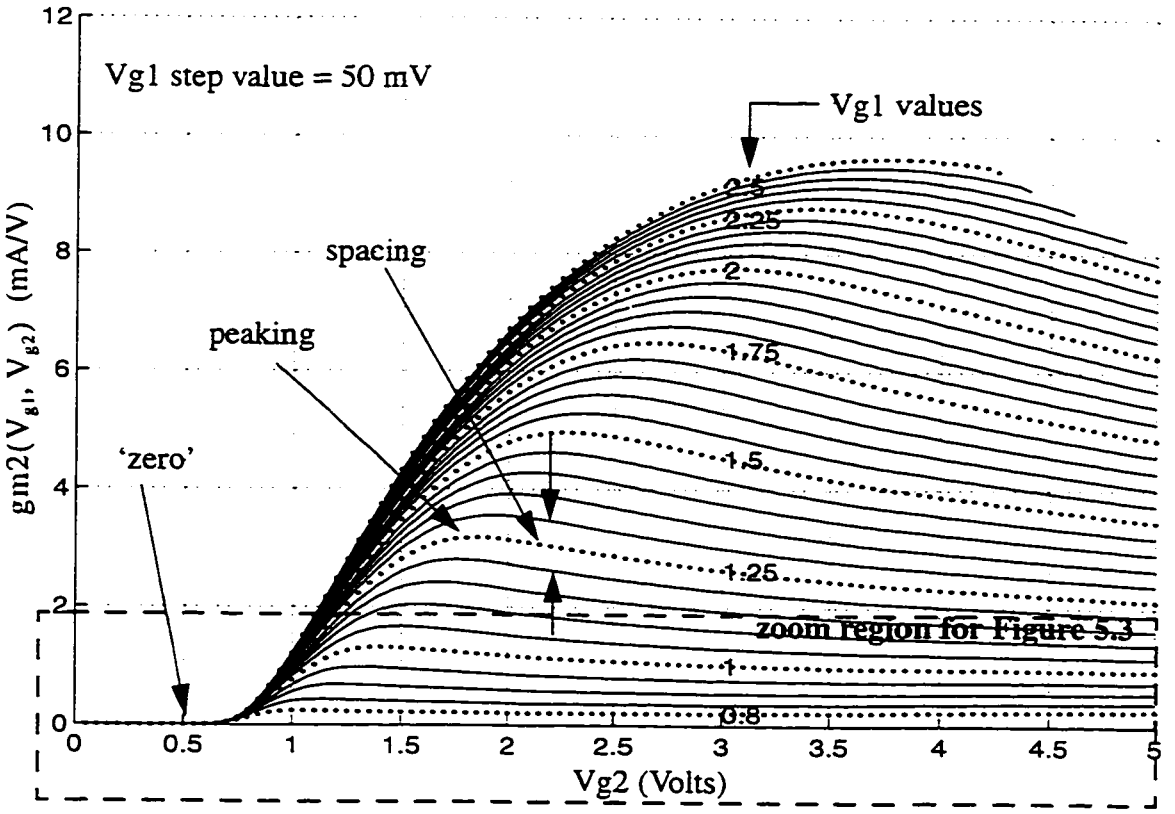

Figure 5.2 Graph of calculated gm2 as a function of V_{g2} with stepped V_{g1}

The change in $gm2(V_{g1}, V_{g2})$ due to the RF signal can be isolated by 'normalizing' the response around a given RF or gate 1 bias point. This is accomplished by assuming that the given gate 1 bias point is the 'steady state' of the system and excursions above or below this bias point are perturbations from the steady state caused by the RF signal. By subtracting out the gate 1 bias point curve from curves above and below it, a set of new curves is generated representing the $\Delta gm2(V_{g1}, V_{g2})$ function.

Using the gate 1 RF bias point of 1 volt as a representative example [see close up in Figure 5.3], the curves created by the normalization process are shown in Figure 5.4. The positive excursion of the waveform is represented by the 1.05 Vdc curve with the 1 Vdc curve subtracted from it. The negative excursion curve is represented by the 0.95 Vdc curve having the 1 Vdc curve subtracted from it. This emulates an RF waveform, biased at 1Vdc, with a peak amplitude of 50mV. These curves represent the amount of change the RF waveform would cause to the steady state of the circuit around a given V_{g1} bias point for a range of V_{g2} values

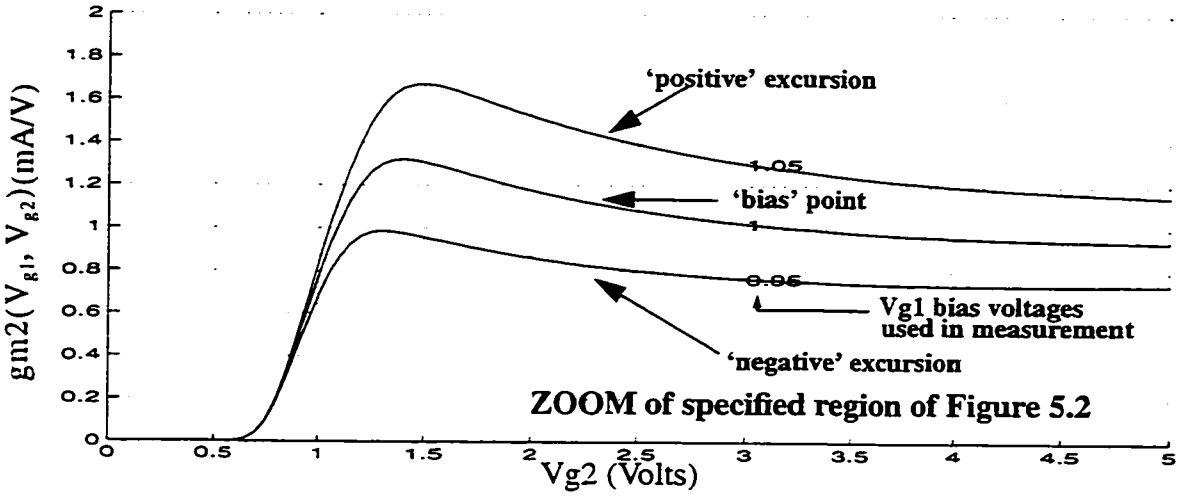

Figure 5.3 Close up graph of gm2 as a function of V_{g2} for representative RF bias condition showing excursions from the bias point

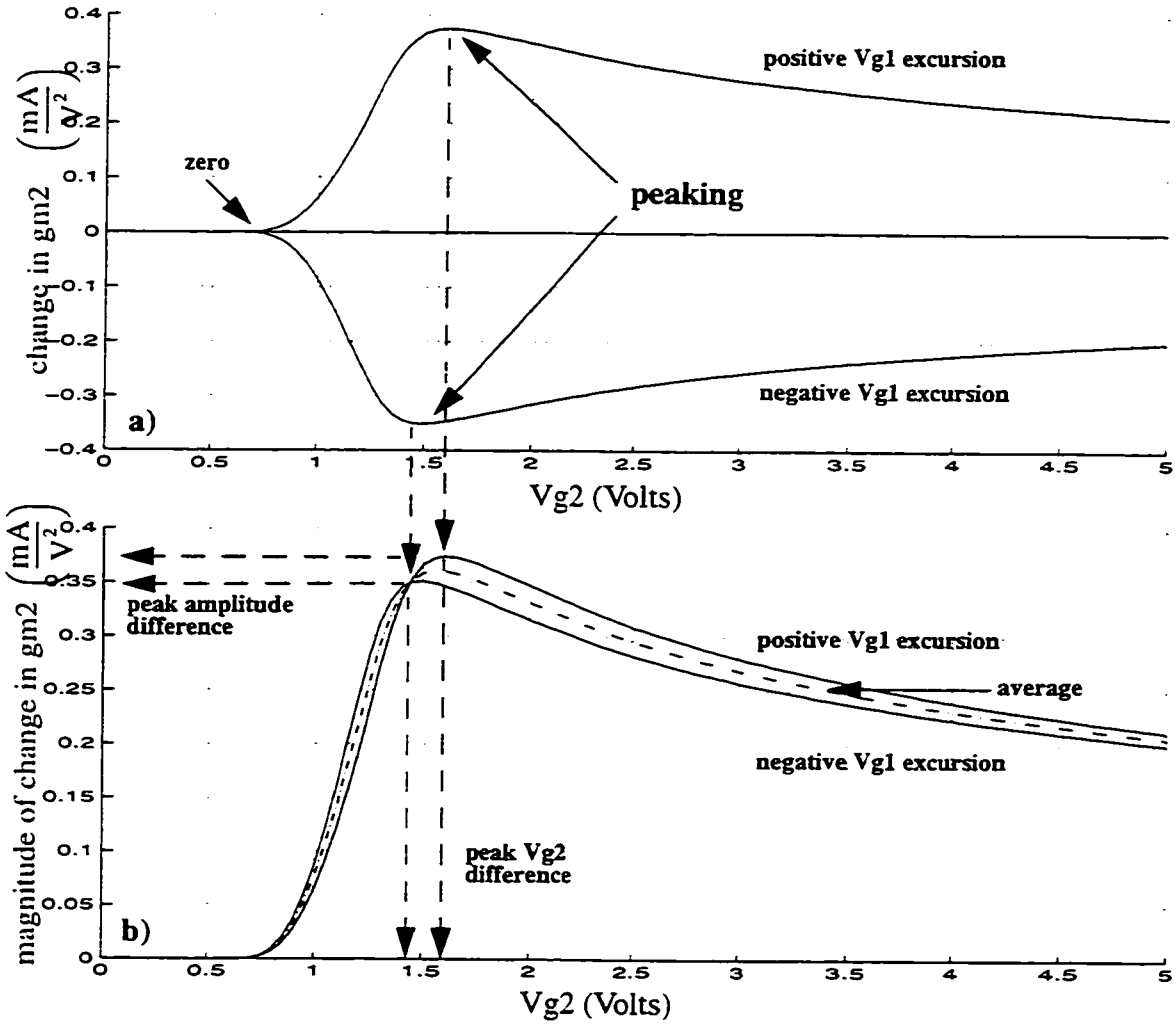

Figure 5.4 a) Graph of change in gm2 caused by a shift in RF bias normalized to the bias point as a function of V_{g2}

b) Graph of magnitude of change in gm2 as a function of V_{g2} to clarify differences between positive and negative RF excursions

5.1.1.4 The Δgm2 Function

The graph of the normalized $gm2(V_{g1}, V_{g2})$ function, in Figure 5.4a, is very important because it shows very clearly the change in $gm2(V_{g1}, V_{g2})$ caused by a shift in the RF level away from the 'steady state' bias point. As V_{g2} increases, the change in

$gm2(V_{g1}, V_{g2})$ rises from zero, peaks, and then decreases slightly. It also clearly shows that the change in the $gm2(V_{g1}, V_{g2})$ function is different for positive and negative excursions of the RF waveform and that the peaking phenomenon occurs for different values of gate 2 voltage. This is seen more clearly by plotting the magnitude of the change in $gm2(V_{g1}, V_{g2})$ as in Figure 5.4b. As real signals are considered symmetrical, the average change around the bias point is used to account for the non-symmetry of the device response resulting in the function designated $\Delta gm2(V_{g1}, V_{g2})$.

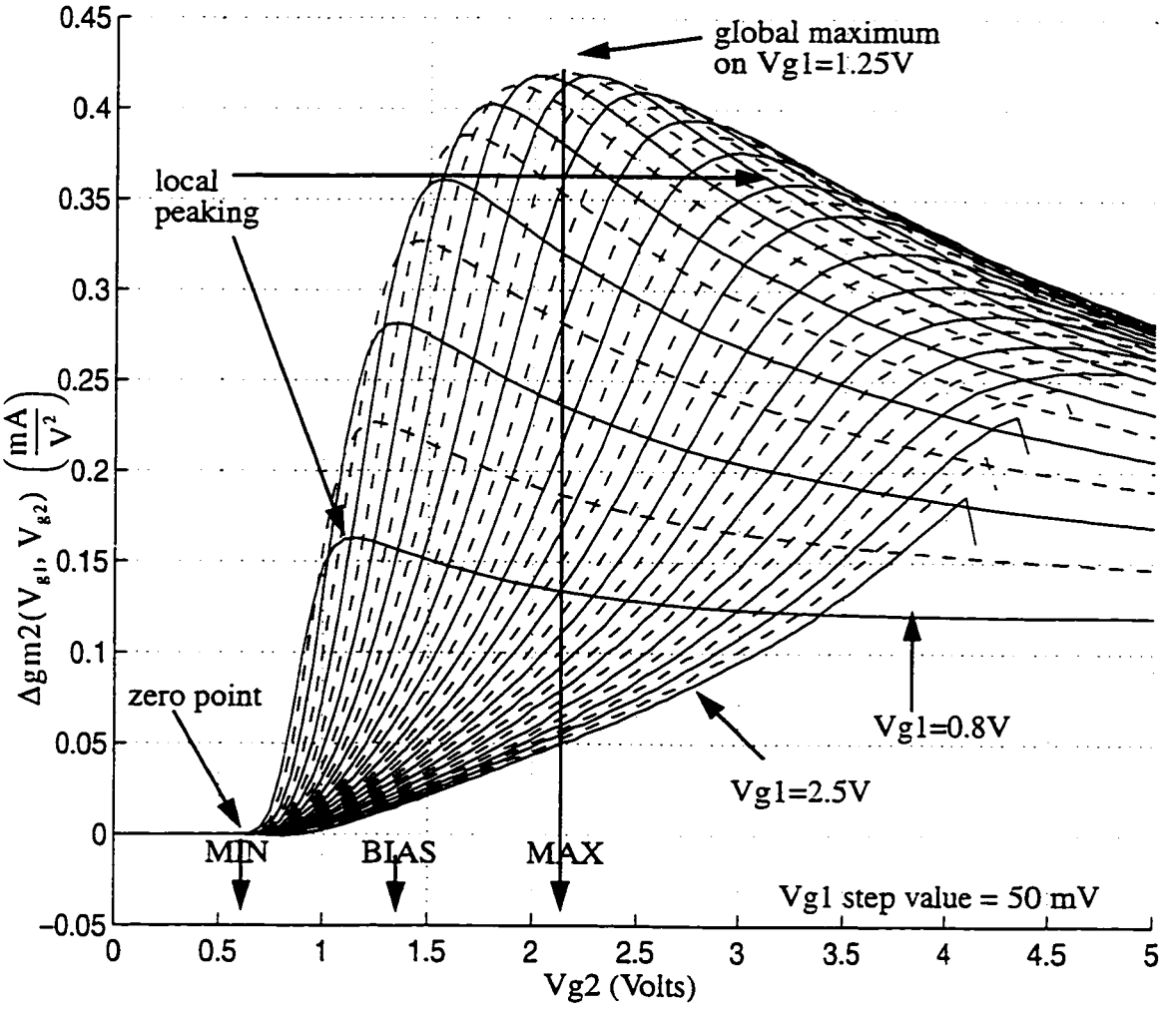

Figure 5.5 Graph of $\Delta gm2$, the average change in gm2, as a function of V_{g2} for stepped values of V_{g1} showing details for bias selection

Figure 5.5, the graph of the $\Delta gm2(V_{g1}, V_{g2})$ function over the entire range of V_{g1} and V_{g2} bias voltages, is the most important graph in this method. It shows that not only does the $\Delta gm2(V_{g1}, V_{g2})$ function rise, peak, and fall for each RF bias point, but that a global maximum exists as well. This global maximum represents the maximum change in $gm2(V_{g1}, V_{g2})$ that is possible for this device. It is this point that is critical for the proper application of the design method.

5.1.1.5 Bias Selection

It is from this graph of the $\Delta gm2(V_{g1}, V_{g2})$ function, Figure 5.5, that the initial bias points and power levels of the LO and RF are chosen. The global maximum of the $\Delta gm2(V_{g1}, V_{g2})$ function locates the maximum V_{g2} voltage that is required for the mixer. The point where the $\Delta gm2(V_{g1}, V_{g2})$ function goes to zero is the minimum V_{g2} voltage that is required for the mixer. The optimum LO bias point is then midway between these two points. This effectively defines the LO bias and, along with the gate 2 impedance, the minimum required power level. The initial RF bias point is chosen from the curve that contains the $\Delta gm2(V_{g1}, V_{g2})$ function global maximum.

Using Figure 5.5 as a reference, the initial RF bias point was chosen as 1.25 Vdc, the LO bias voltage was chosen as 1.4 Vdc and the peak LO voltage swing was chosen as 800 mVpk corresponding to an LO input power level of 8 dBm into a 50 ohm LO port impedance.

5.1.2 Determination of RF Characteristics

5.1.2.1 Steady State Condition and $\Delta gm2|_{f_{lo}}$ function

Once the initial DC bias conditions and minimum LO power level of the circuit are known, the mixer steady state is needed. As $gm2(V_{g1}, V_{g2})$ is a nonlinear function of the LO, the output current will be composed of a number of LO harmonics. As developed in the background theory, only the LO frequency component is required to calculate the conversion gain. In addition, it is realized that the $gm2(V_{g1}, V_{g2})$ function itself is not an important quantity to know, only the change in the $gm2(V_{g1}, V_{g2})$ function caused by the RF signal, the $\Delta gm2(V_{g1}, V_{g2})$ function, is needed. This single frequency component can be isolated by measuring the change in the output current at the LO frequency as the RF bias point is varied.

Physically, the steady state of the mixer can be created by first biasing the circuit as previously described and measuring the port impedances. In order to permit rapid and accurate measurement of all of the required voltages and currents at high frequencies, a 50 ohm impedance is used as a standard port impedance to reduce difficulties in interfacing with measurement equipment. For this design, the RF frequency selected is 850 MHz, the LO frequency is 700 MHz, and the IF frequency is 150 MHz as discussed in section 6.2.1. Gate 1 should be measured at the RF frequency, gate 2 at the LO frequency, and the drain at both the LO and the IF frequencies. Using this information, the gate input impedances should be forced to 50 ohms by selectively resonating out the capacitances and placing shunt 50 ohm resistors. The drain should be parallel resonated at the LO frequency and

the 50 ohm load created by capacitively coupling to the measuring equipment. Ensure that the bias technique used for the drain does not allow the top gate device to enter the linear region of operation.

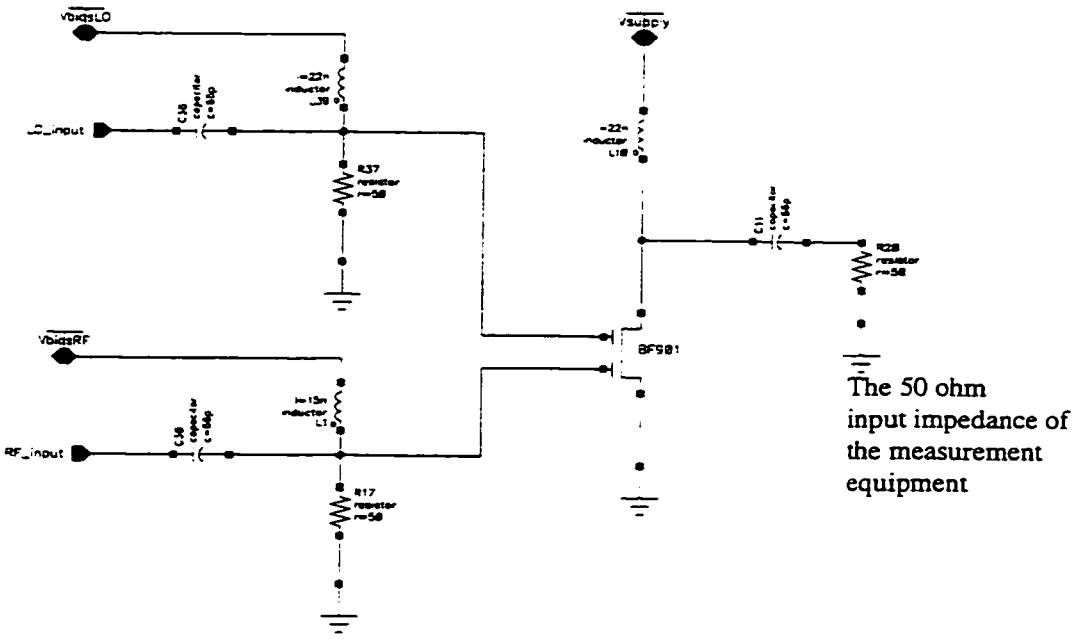

Figure 5.6 Schematic of circuit used for characterization with 50 ohm port impedances

The LO power should be set so as to ensure that the voltage on the gate of the device is the same as calculated from the $\Delta gm2(V_{g1}, V_{g2})$ graph. With the LO power of 8 dBm applied, step the gate 1 voltage through a range of values that encompasses the RF bias point found from the $\Delta gm2(V_{g1}, V_{g2})$ graph while measuring and recording the output power at the LO frequency. Verify that the output voltage did not force the top device of the dual gate into the linear region.

5.1.2.2 Conversion Transconductance

The LO current in the 50 ohm load was calculated and the results were graphed in Figure 5.7, showing the LO output current as a function of the applied RF bias point. In order to get a clearer picture of the transfer function characteristics, the curve generated can be divided by the RF bias point to generate the function $((\Delta gm2|_{f_{lo}}) \cdot V_{lo})$. Recalling Equation 4.13 from chapter 4, the conversion transconductance, g_c, is the $((\Delta gm2|_{f_{lo}}) \cdot V_{lo})$ function divided by 2. At this stage of the characterization process, the output current and the $((\Delta gm2|_{f_{lo}}) \cdot V_{lo})$ function implicitly include the amplitude, frequency, and bias point of the LO waveform. As such, these functions are only valid at this particular set of LO bias condition, frequency, and power level.

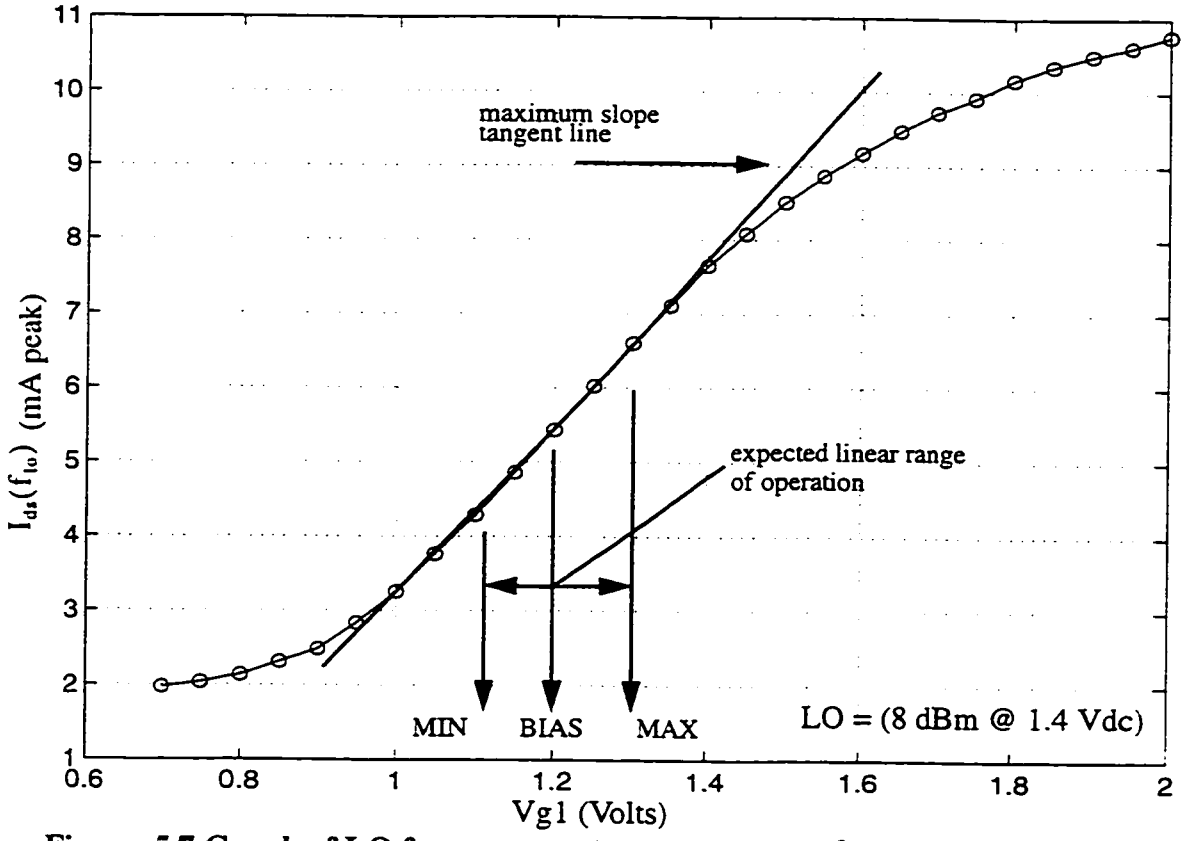

Figure 5.7 Graph of LO frequency output current as a function of V_{g1}

Figure 5.7 shows the effect of the RF bias point, or equivalently, the RF signal, on the LO output current. It is apparent that the region that is the most linear also has the highest slope. The range of the linear region is an indication of the size of the RF signal that can be accommodated before distortion or gain compression occurs and is a conservative estimate for the expected compression point.

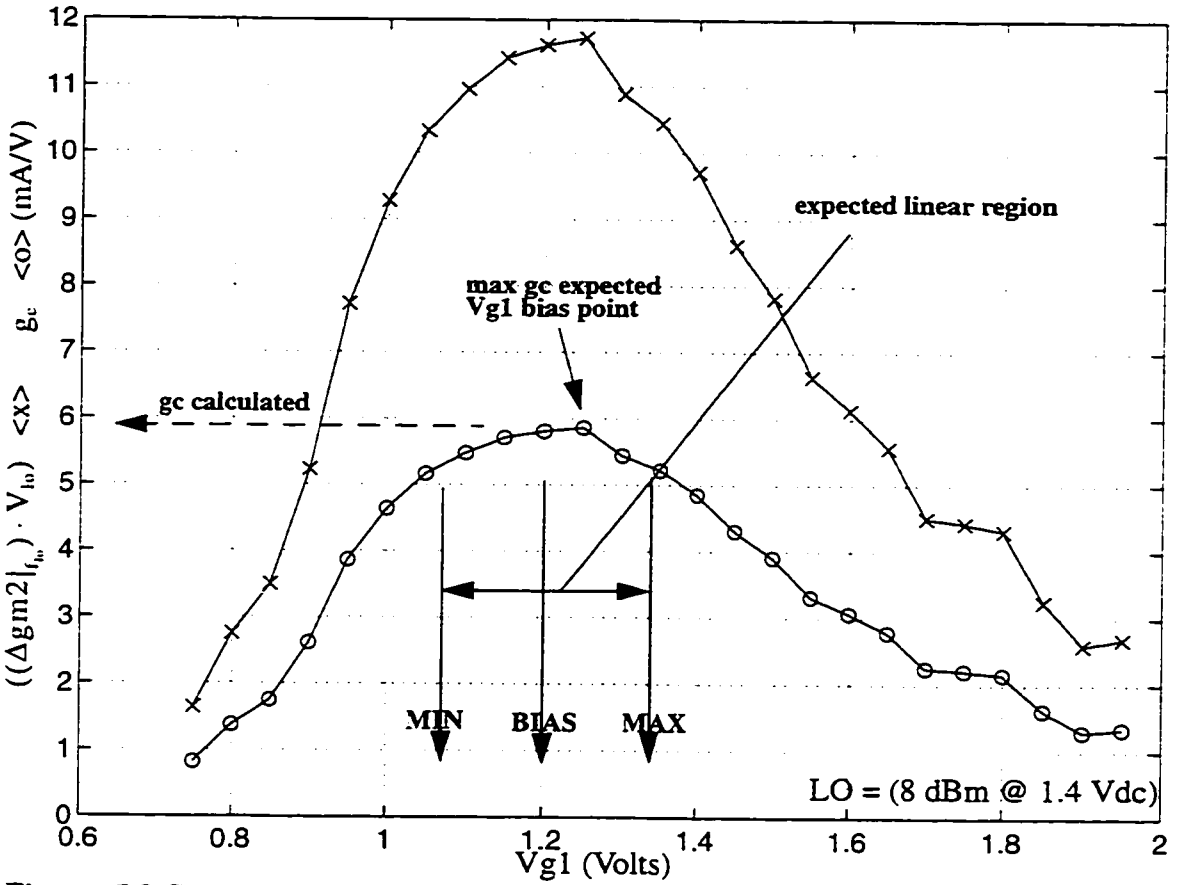

Figure 5.8 Graph of calculated conversion transconductance and $\left(\left(\Delta gm2|_{f_{lo}}\right) \cdot V_{lo}\right)$ as a function of RF bias (V_{g1})

It can be seen from Figure 5.8, the graph of $((\Delta gm2|_{f_{lo}}) \cdot V_{lo})$ and the conversion transconductance, g_c, as a function of the RF bias point, that the g_c function peaks and remains almost constant for a range of RF bias points. This corresponds to the region

of operation with the highest gain and the highest linearity for this given LO bias and power level. This is the optimum bias range for the RF and some slight adjustment in the RF bias point may be desirable depending on the compression point and linearity specifications.

The conversion transconductance thus calculated should be confirmed before usage. This is easily accomplished by shifting the output resonating network to the IF frequency, applying a small RF signal (-20 dBm) to ensure linear operation, and measuring the resulting output power at the IF frequency. From this information, the expected conversion gain can be calculated. The expected and measured conversion gains are plotted in Figure 5.9. From this graph, it can be seen that the calculation of the expected conversion gain accurately predicts the measured results indicating that the conversion transconductance characterization is accurate. This is discussed further in Chapter 6 following testing over a more extensive set of bias conditions.

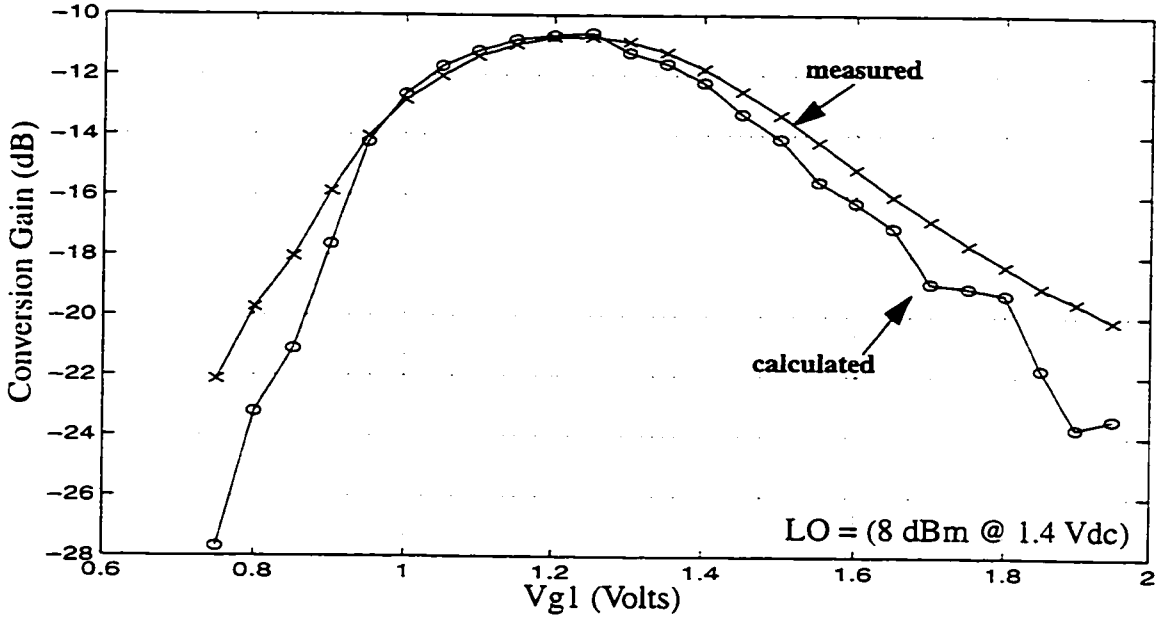

Figure 5.9 Graph of calculated and measured conversion gain as a function of RF bias voltage (V_{g1}) with 50 ohm load

5.1.2.3 Verification of LO Bias Selection

In order to verify the selection of the LO bias point, it is necessary to investigate the effects of the conversion transconductance or gain in relation to the LO bias voltage. Using an LO power level of 8 dBm and the RF bias point of 1.25 Vdc as found in the DC characterization [Figure 5.5] and confirmed with the RF characterization [Figure 5.9], the gain of the circuit into a 50 ohm load was measured while stepping the LO bias voltage through a range of values encompassing the expected LO bias of 1.4 Vdc. The results of this measurement are plotted in Figure 5.10 and show that, at this power level and RF bias condition, an LO bias point of 1.4 Vdc provides close to the maximum gain possible, indicating a suitable bias selection.

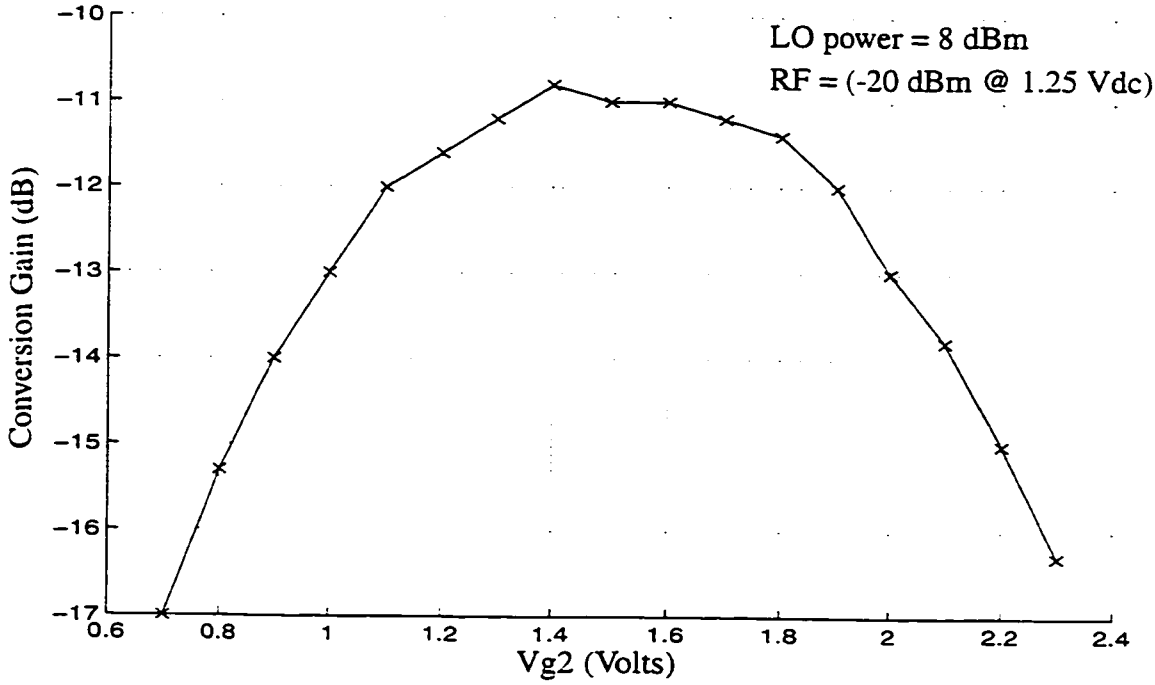

Figure 5.10 Graph of measured conversion gain as a function of LO bias with 50 ohm load

Figure 5.10 also shows that there is a range of LO bias values, between 1.4 and 1.6 Vdc in this case, where the gain of the circuit is almost constant with respect to the LO bias condition. This is discussed further in Chapter 6 following testing over a more extensive set of bias and LO power level conditions.

5.1.2.4 Input Compression Point

Recall that the RF characterization bias points are used to represent an equivalent RF voltage on the gate of the transistor. By averaging the calculated gain values in a range around the given bias point, average values of gain for a given 'RF signal' amplitude can be made. For example, if the RF characterization points are 50mV apart, and the best bias point chosen was 1.25 volts, the gain for a 50 mV peak RF signal amplitude can be estimated by averaging the 3 gain values for 1.2V, 1.25V, and 1.3V. If this calculation is done for successively larger 'RF signal' amplitudes, the input compression point can be estimated from the RF characterization range, or the 'RF signal amplitude', when the average gain falls one dB from the expected value at the original bias point.

In order to see the gain compression characteristics more clearly, the average gain values can be normalized to the original bias point gain where linear operation is expected, resulting in a curve that shows the deviation or compression from the expected small signal gain. The results of this calculation are shown in Figure 5.11 along with the measured data for comparison and verification using a circle to clarify the 1 dB compression point. From this graph, it can be seen that the calculated compression characteristic accurately predicts the measured data indicating that the design method provides a means

to predict the input compression point. This is discussed further in Chapter 6 following testing over a more extensive set of bias conditions.

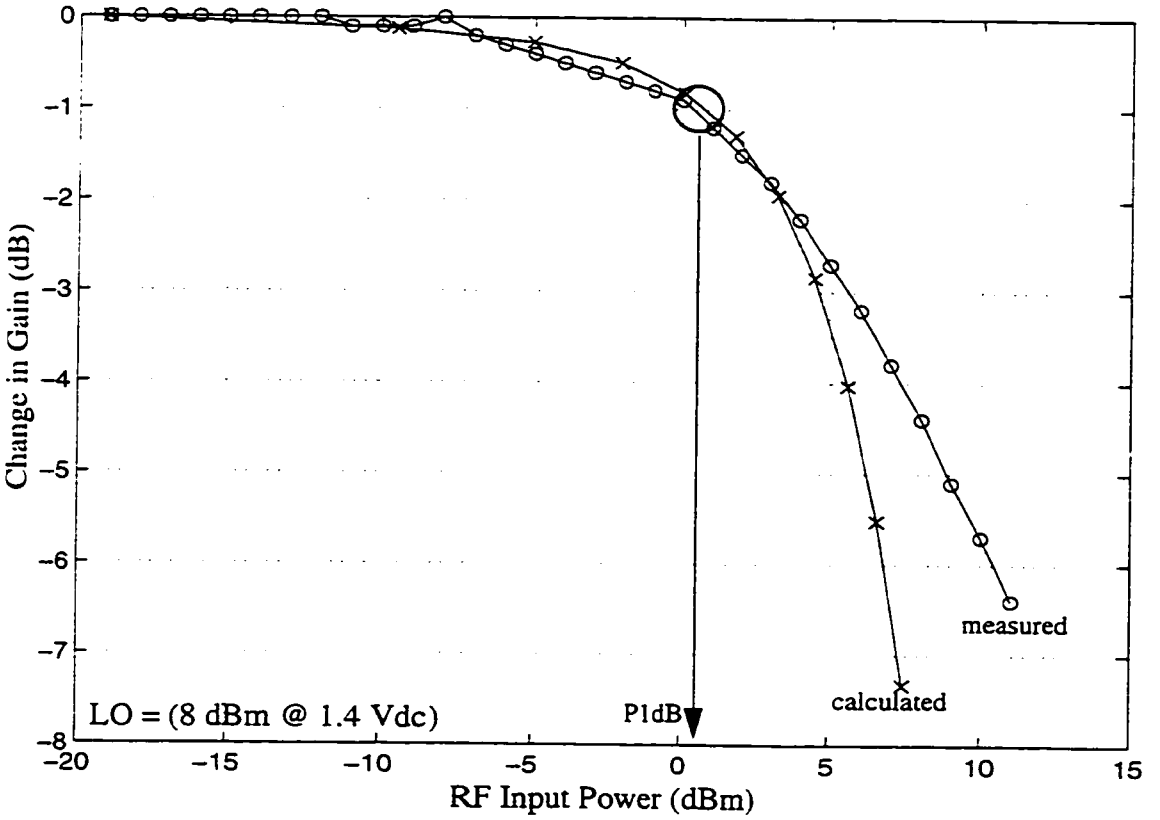

Figure 5.11 Graph of calculated and measured conversion gain compression as a function of RF input power with 50 ohm load

5.2 Summary

The method has characterized the mixer using the voltages imposed on the gates and the output drain current. Using the DC current characterization to identify the desired bias points and the RF characterization to calculate the conversion transconductance and the input compression point, the mixer core has been fully characterized. As long as the gate voltage values used in the final design are maintained, the mixer core char-

acterization will remain valid. Further optimization of the circuit such as noise matching or setting of the port impedances, will depend upon the design requirements and environment. If the device is designed as an RFIC, matching of some of the impedances may be difficult. If the design is with discrete components, the ports may be appropriately matched so as to provide impedance transformations at the inputs and outputs. A combination of RFIC and discrete techniques will prove to useful for most designs.

Chapter 6: Design Optimization and Results

The method has produced a well characterized mixer core that can be used directly for a complete design. However, before the design is completed, more information may be needed by the designer to allow for intelligent optimization of the final circuitry.

After the characteristics of the mixer core are investigated, a complete mixer circuit is designed and implemented. The final characteristics of the mixer are reported along with summaries of the characteristics of some comparative circuits.

6.1 Generalization of the Design Method

The method, as it has been implemented in the last chapter, has provided one specific bias condition and LO power level to define the operating conditions of the mixer. Although this places the mixer in a desirable operating condition, there is no inherent restriction in the method to choose these conditions. Indeed, the method is sufficiently general to allow an almost arbitrary choice of bias conditions and LO power level and still provide an accurate characterization of the mixer's capabilities. An investigation into the effects of other operating conditions will show the flexibility available to the designer as well as illustrate the generality and the accuracy of the method in other operating conditions.

6.1.1 Effect of RF Bias and LO Power on Mixer Characteristics

6.1.1.1 Gain Characteristics

With the mixer port impedances set to 50 ohms as in Figure 5.6, the effects of RF bias and LO power levels can be isolated more easily. The original LO bias point of 1.4 Vdc is used as it provides for the most rapid movement through the transition region between maximum and minimum $\Delta gm2$ and an RF input power level of -20 dBm is used to ensure linear operation. The mixer characterization was repeated by setting the LO input power level and recording the LO frequency output power while stepping through a range of Vgate1 bias voltages, effectively repeating steps 8 to 12 of the design method.

Figure 6.1 shows the calculated conversion transconductances for the LO powers used and shows that increased LO power results in increased conversion transconductance and that the optimum RF bias point increases slightly as the LO power increases.

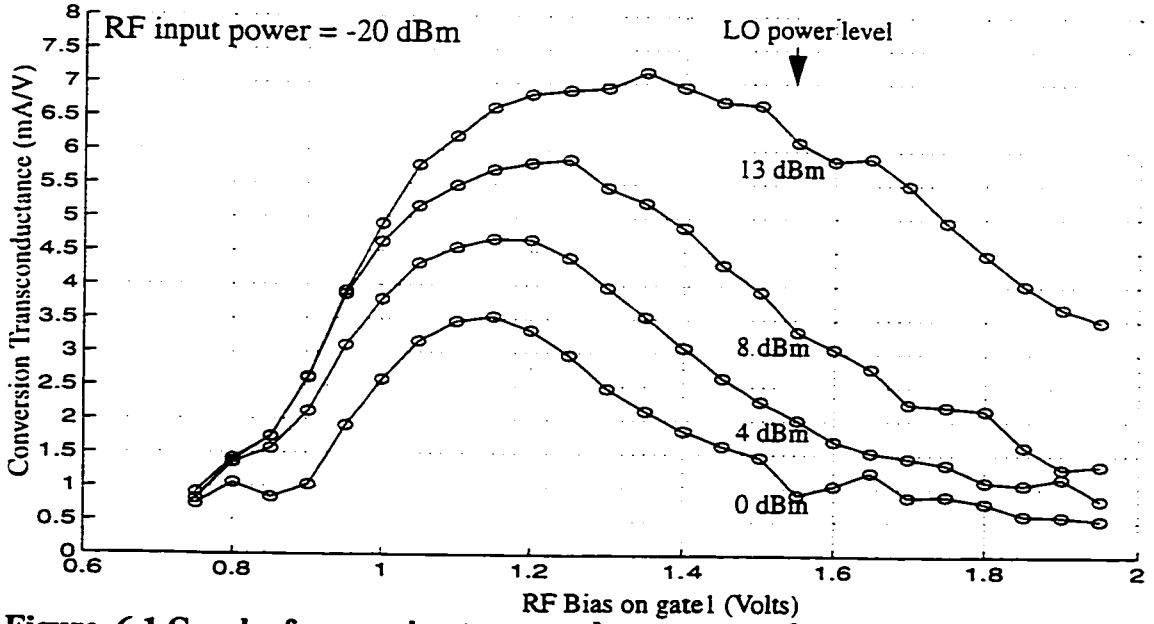

Figure 6.1 Graph of conversion transconductance as a function of RF bias for various LO power levels

Using the calculated g_c, the expected conversion gain with a 50 ohm load can be calculated and compared to the measured gain, the results of which are shown in Figure 6.2. This graph shows that the characterization technique is valid and accurate in predicting the gain for all of the LO power levels especially in the high gain region of each curve which is the expected region of operation.

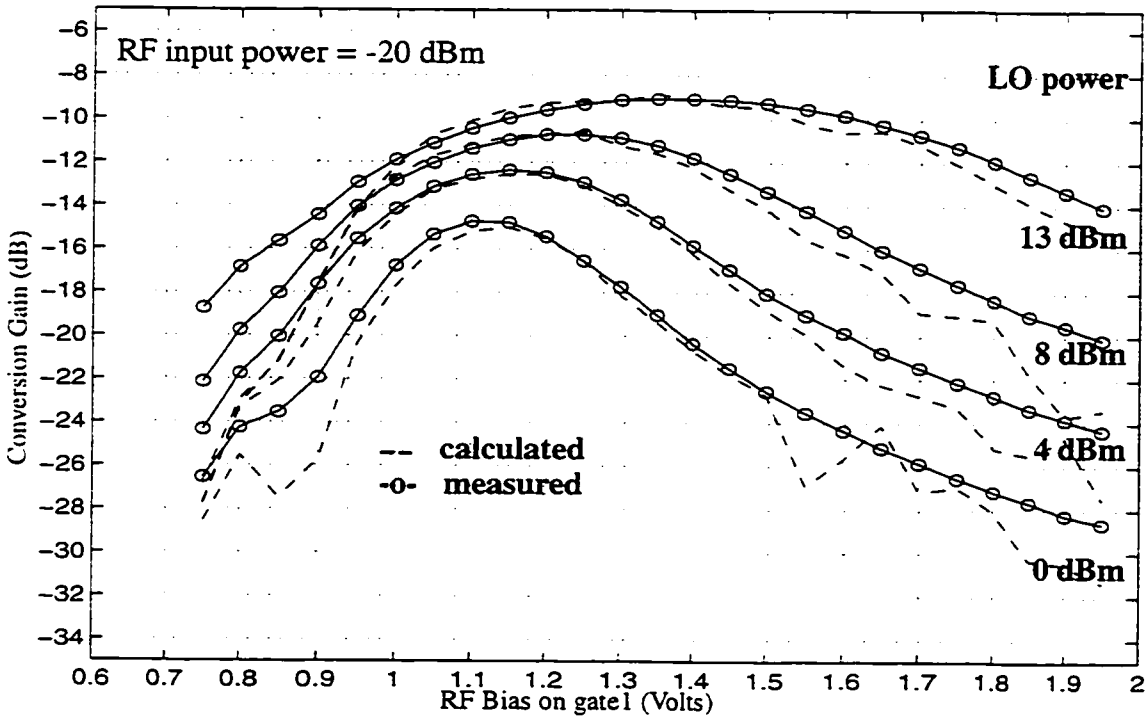

Figure 6.2 Graph of calculated and measured conversion gain as a function of RF bias for various LO power levels

In order to see the gain estimation error more clearly, the difference between the calculated and measured values are plotted in Figure 6.3. Here it can be seen that the method provides very accurate results in the expected region of operation with the loss of accuracy out of the region of operation attributable to measurement errors due to the small

LO power variations present in these regions during the characterization. More precise measurement will reduce the error in this region.

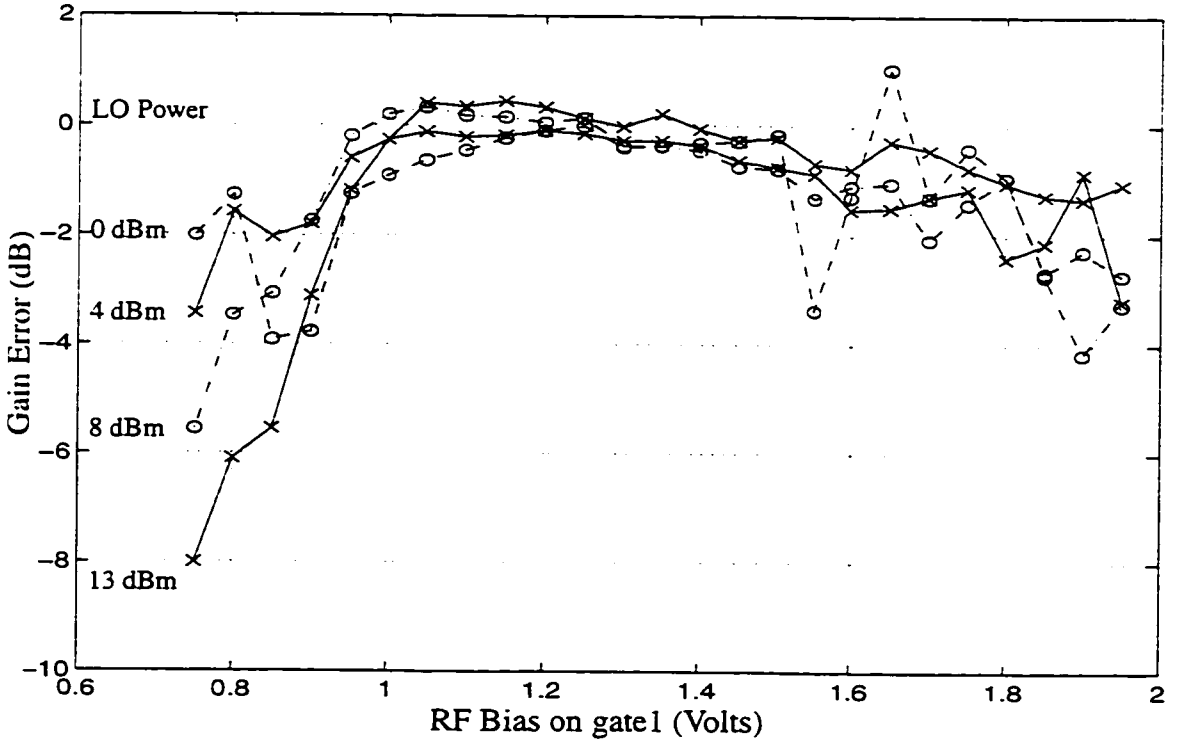

Figure 6.3 Graph of conversion gain error as a function of RF bias for various LO power levels

6.1.1.2 Input Compression Point

In order to confirm the input compression point prediction over all LO powers, the gain compression was measured and compared to the estimated gain compression curves with the results plotted in Figure 6.4. The RF bias points were chosen as the points of maximum gain and are the bias points of the expected regions of operation. The input compression points at the higher LO power levels are identified with a circle for clarity.

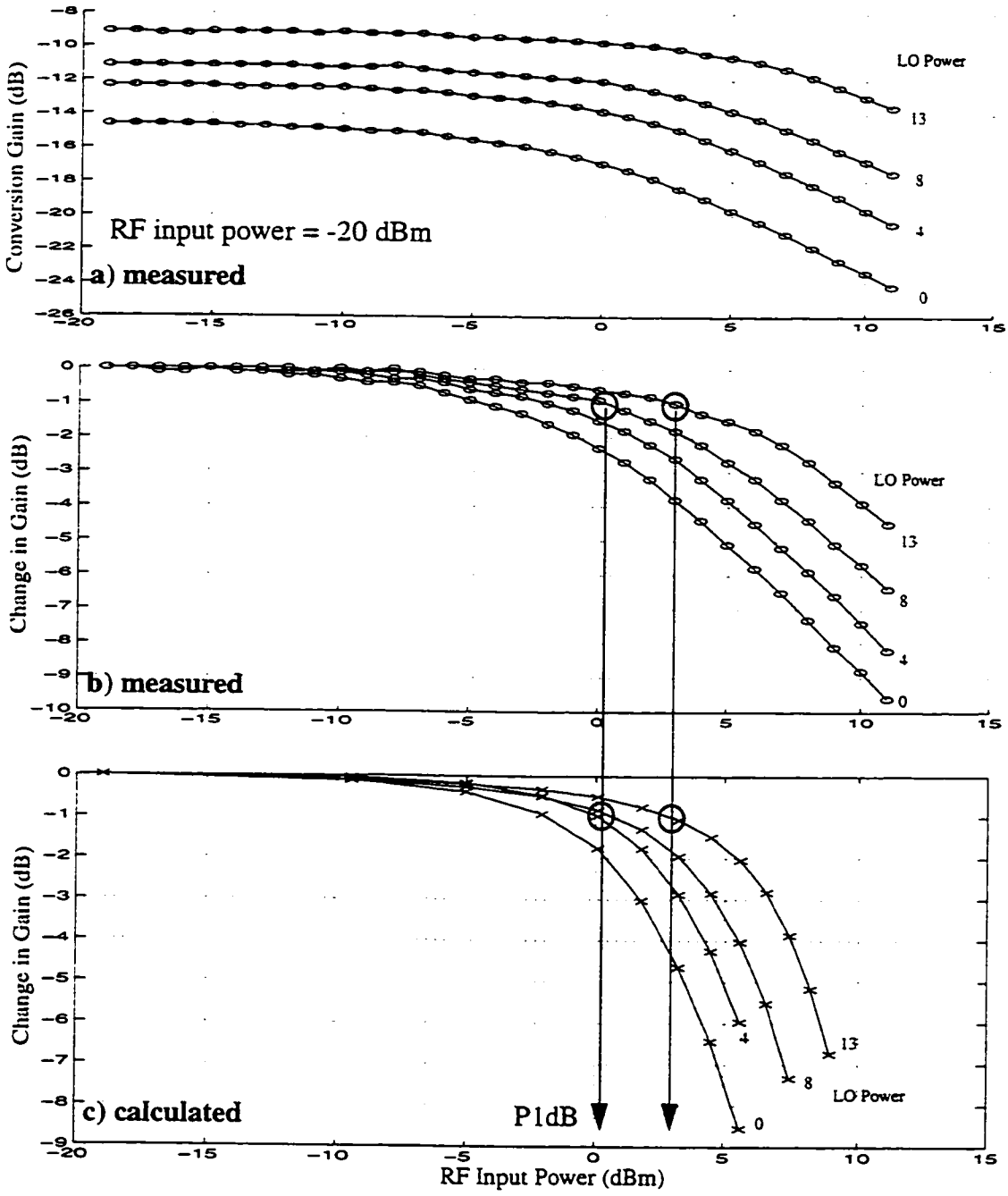

Figure 6.4 a) Graph of measured conversion gain as a function of RF input power for various LO power levels

b) Graph of measured gain compression as a function of RF input power for various LO power levels

c) Graph of calculated gain compression as a function of RF input power for various LO power levels

From the graphs, it can be seen that the design method accurately predicts the input compression point for the larger LO power levels. Discrepancies at the lower LO power values can be attributed to the same measurement accuracy in the characterization as was identified in calculating the gain. Although the compression point estimation is dependent upon the initial gain estimation accuracy, the method still estimates the input compression point within 3 dB.

6.1.1.3 Third Order Intercept Point

In order to investigate the effects of RF bias and LO power on the third-order intercept, the output third-order intercept point, or IP3o, was measured. As the gain also changes significantly over these conditions, the IP3o was referred to the input to create the input IP3, or IP3i, so as to provide a means of comparing the results. In addition, the RF points were chosen so as to be symmetrically located around the expected region of operation, the maximum gc or gain characteristic region, for each LO power condition. This provides insight into the trade-offs between gain and linearity in terms of the RF bias conditions relative to the peak in the gain characteristic at a given LO bias and power level. The results were plotted in Figure 6.5 and show that the IP3i increases significantly as the RF bias voltage increases. This is consistent with expectations as the mixing device, the lower transistor, exhibits more linear characteristics as the gate 1 voltage increases. Vendelin et al. [6.1] provide an interesting insight into the effect of bias on IP3 characteristics.

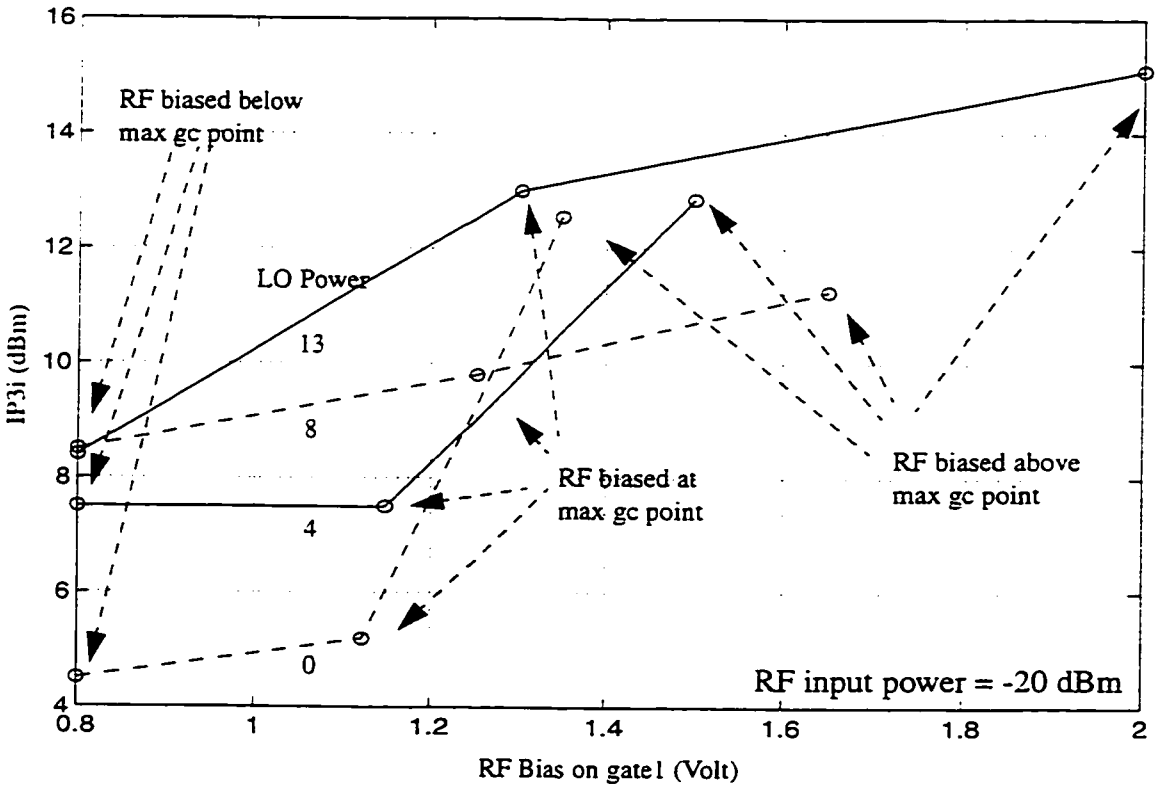

Figure 6.5 Graph of input third-order intercept characteristics as a function of RF bias for various LO power levels

6.1.1.4 LO Compression

To investigate the effect of LO power levels on the conversion gain, LO compression curves were generated using the maximum gain locations as the RF bias points and an RF input power of -20 dBm to ensure linear operation. The results of this experiment are shown in Figure 6.6. It is beneficial to operate the mixer in a region of the curve that has minimum and constant slope, corresponding to a minimum conversion gain sensitivity to the LO amplitude. The 8dBm LO power level identified in the design method for the RF bias point of 1.25 Vdc provides a region of operation exhibiting an almost constant

slope for a +/- 3dB LO power variation indicating a suitable minimum LO power level. It can also be seen that increased LO power provides improved LO compression at all RF bias conditions. At the lower range of LO powers, for example between -10 dBm and 5 dBm, it can be seen that the lower RF bias points require less LO power for a given conversion gain. This provides information for the designer for the choice of LO drive level. One drawback of using this range of LO powers is the increased sensitivity of the conversion gain to the amplitude of the LO waveform. These curves also show that the mixer exhibits very gradual LO compression and does not have a sharply defined region where the mixer gain is not affected by the LO amplitude. It can be shown, however [Figure 6.9], that higher LO powers do lead to a full LO compression characteristic.

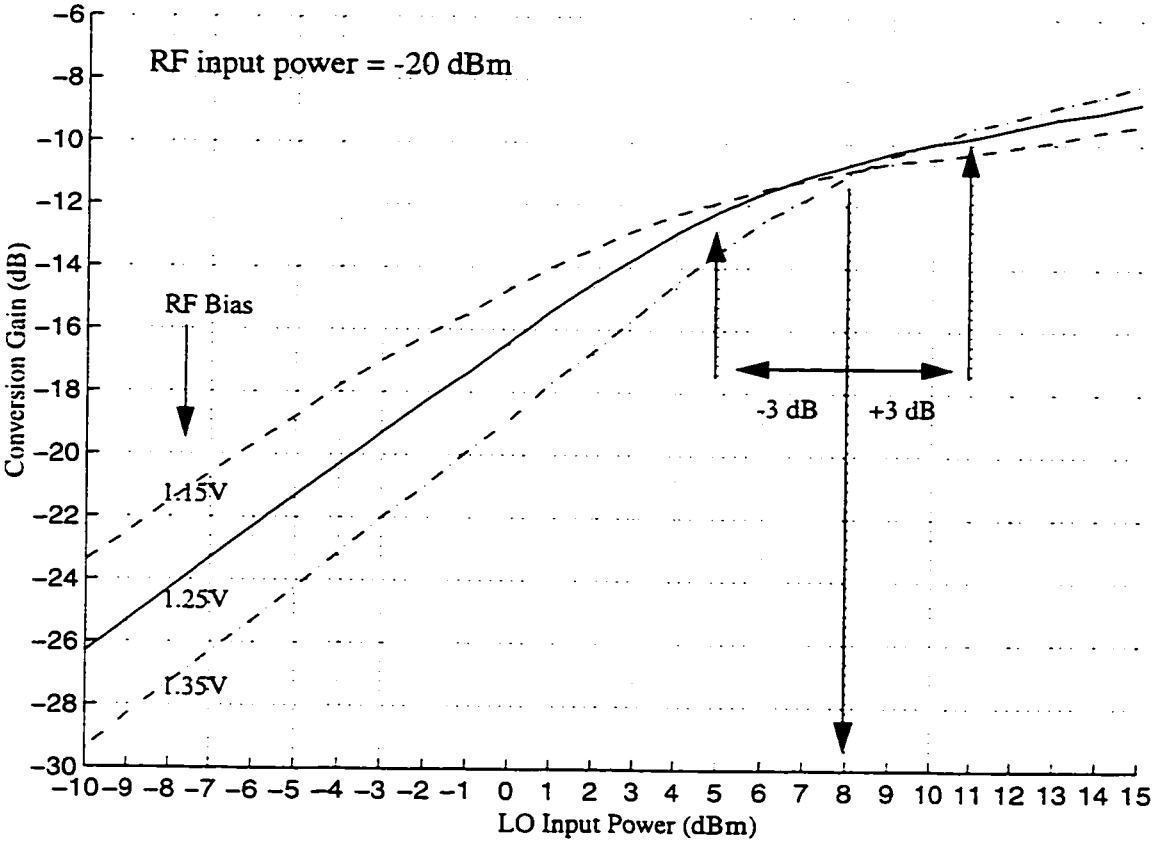

Figure 6.6 Graph of conversion gain as a function of LO drive level for various RF bias conditions

6.1.2 Effect of LO Bias and LO Power on Conversion Gain

As the mixer characteristics are a function of the RF bias, the LO power, and the LO bias, it is convenient to set one as a constant in order to isolate the effect of the LO bias voltage. As the optimum RF bias voltage for the LO power level of 8dBm has already been determined to be 1.25 Vdc [Figure 5.9, Figure 6.2], this value will be set as a constant in the following measurements so as to better observe the effects of LO bias and power level on the conversion gain of the mixer.

It is also informative to investigate the effect of the LO power level at the various LO bias conditions to verify the optimum power level for a given LO bias condition. To investigate this effect, the LO power levels of 0, 4, 8, and 13 dBm are chosen for continuity with the power conditions used in the RF characterization.

Using the circuit of Figure 5.6, with the RF port biased to 1.25 Vdc, the LO power level and LO bias were varied to investigate the sensitivity of the mixer conversion gain characteristics to the LO bias at various power levels. The results are plotted in Figure 6.7 and show that the LO bias and LO power level do have a significant effect on the conversion gain. It can be seen that at low LO power levels, the conversion gain is highly sensitive to the LO bias exhibiting a sharp peaking of the gain at an optimum point of 1.5 Vdc. As the LO power increases, this sensitivity is reduced, providing a larger range of LO bias points where the conversion gain is approximately constant. At the LO power of 13 dBm, the conversion gain is almost flat, indicating a low sensitivity to the LO bias point.

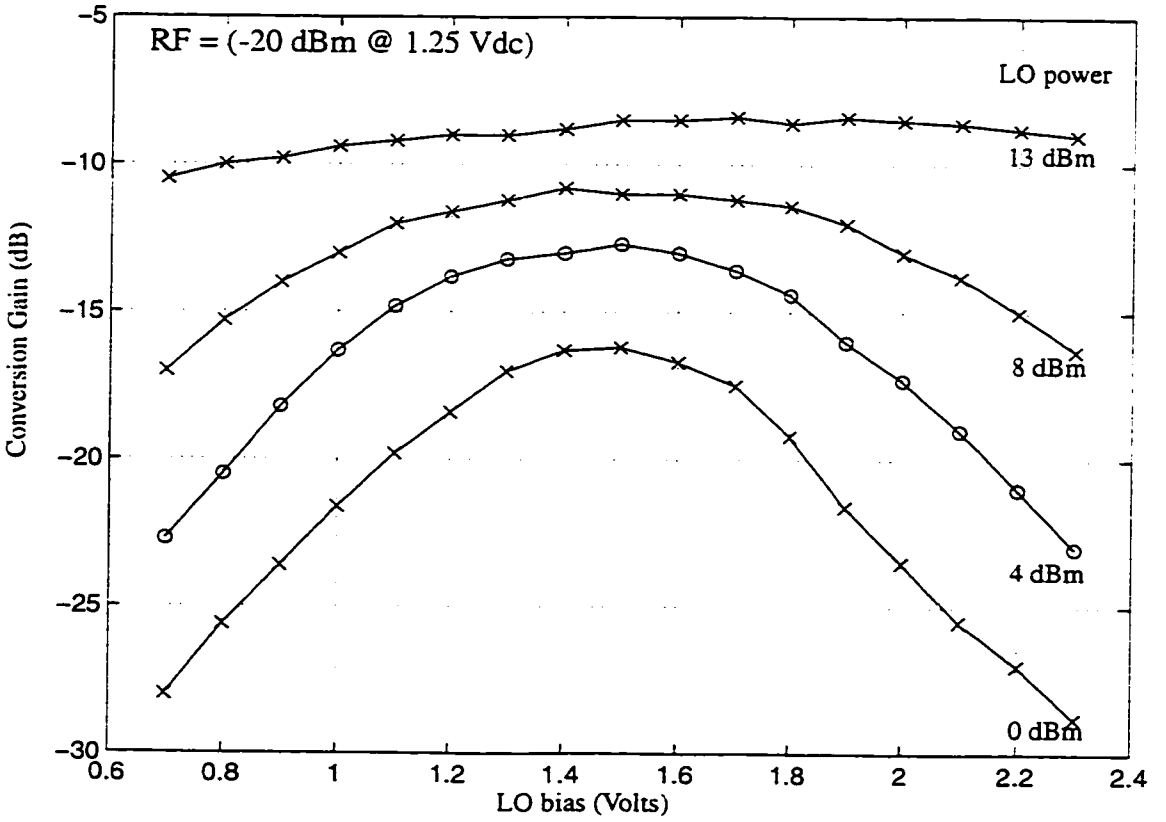

Figure 6.7 Graph of conversion gain as a function of LO bias for various LO power levels

6.1.3 Summary of Effect of Bias Conditions on Mixer Performance

The results from sections 6.1.1 and 6.1.2 concerning the effects of RF bias, LO bias, and LO power level provide valuable information to the designer. Although the results indicate that the mixer characteristics can be highly sensitive to the bias conditions in some cases, there are operating regions where these sensitivities are reduced. The use of the proposed design method ensures the selection of one such optimum point using the minimum LO power level required to achieve this. An increase in LO power improves upon this initial bias condition selection.

Although the proposed method provides a desirable bias condition, there is no inherent requirement to choose this selection as the design method can be used in any bias condition to identify the characteristics of the mixer. As a result, the designer has great flexibility in the choice of bias and power levels with the ability to accurately predict the ramifications of the design choices, allowing intelligent optimization of the design for a given application.

6.2 Design Completion

6.2.1 Design Criteria

The following general criteria are used as guidelines for the final design:

1. Moderate conversion gain is desired,
2. High linearity is desired,
3. Lowest possible noise figure is desired,
4. Lowest possible power usage is desired,
5. 1 GHz frequency range of operation.

Although the design method does not directly address the noise figure criterion, high conversion efficiency will help maximize the signal to noise ratio in the circuit and should lead to a lower noise figure [6.2]. Usage of this method places the design in a maximum conversion transconductance region as well as a high linearity region. With the additional information provided by the extensions of the method concerning the IP3,

trade-offs can be made involving the bias conditions or port matching to obtain a desired linearity level.

As the port matching techniques involved in the mixer design are standard RF techniques, the design will concentrate on proving the capabilities of the mixer core itself. It is assumed that the designer will chose appropriate RF and LO input matching networks and IF load impedance as the design requires. In order to continue measurements and to prove that the method is applicable for a complete mixer design, representative narrow-band matching networks to 50 ohms were designed to interface with the test equipment.

The RF input frequency was chosen as 850 MHz so as to be similar to typical cellular phone operating frequencies in order to show the applicability of the method for high frequency circuits.The IF frequency was chosen as 150 MHz based upon a typical down conversion receiver topology [Figure 2.1a] with the first IF between 100 to 200 MHz. A low side LO configuration was chosen resulting in an LO frequency of 700 MHz.

6.2.2 Port Impedance Selection

6.2.2.1 The LO Input Port

As was previously seen, the second gate needs a significantly large voltage to fully compress the mixer relative to the LO. Using the measured port impedance, a matching network at 700 MHz can be designed that will provide significant voltage gain, reducing the input LO power required. The voltage gain in this matching network must be accounted for by re-characterizing the mixer using the new circuit. Alternatively, if the voltage gain of the match network is known, a characterization done with the 50 ohm port

impedance may be used. After design and measurement of the matching network, the input LO frequency was adjusted to 694 MHz to exploit a region with improved matching characteristics.

6.2.2.2 The RF Input Port

The input match on the RF port serves a number of purposes including power transfer, noise matching, and gain selection resulting in a number of conflicting requirements that need to be accommodated for each specific design. To maintain generality in the proof of the design method, the RF port was narrowband matched to 50 ohms at 850 MHz to aid in the interfacing with test equipment. After design and measurement of the matching network, the input RF frequency was adjusted slightly to 857 MHz to exploit a region with improved matching characteristics.

As the input impedance of the MOS transistor is highly capacitive and has a small real part, impedance matching is challenging. In matching the transistor to 50 ohms, a voltage gain was produced in the matching network which impacts the final gain, the input compression point as well as the third-order intercept point, and needs to be included in any further calculations.

6.2.2.3 The IF Output Port

In order to show what gain is possible with just the mixer core, the load impedance was chosen without regard to the input matching network or its associated voltage gain. In this way, the mixer gain from gate 1 input to the drain output can be isolated as a measure of the capabilities of the mixer core.

An arbitrary design specification of 10 dB of conversion gain was used requiring a load impedance of 585 ohms. A tunable matching network was implemented that transformed the 50 ohm input impedance of the spectrum analyzer being used to 610 ohms at 163 MHz. This enables the circuit to achieve high gain and allows for easier measurement of the circuit characteristics. This matching network produces a voltage loss which needs to be included in all further calculations. This will also impact the gain measured and the third-order intercept point.

6.3 The Complete Mixer

6.3.1 The Mixer Circuit

The circuit of the completed mixer used in the measurements can be seen in Figure 6.8. Physically, it consists of the discrete dual gate BF901 device placed on a PCB with the addition of discrete components to implement the matching networks. Port matching was accomplished using standard RF techniques and was aided by using surface mount components and keeping the circuitry area as small as possible. DC biasing was achieved through the use of 10 Kohm resistors placed so as to minimize their effect on the circuitry. Some of the trace parasitic inductance was incorporated into the matching networks, resulting in slightly lower component values than originally calculated.

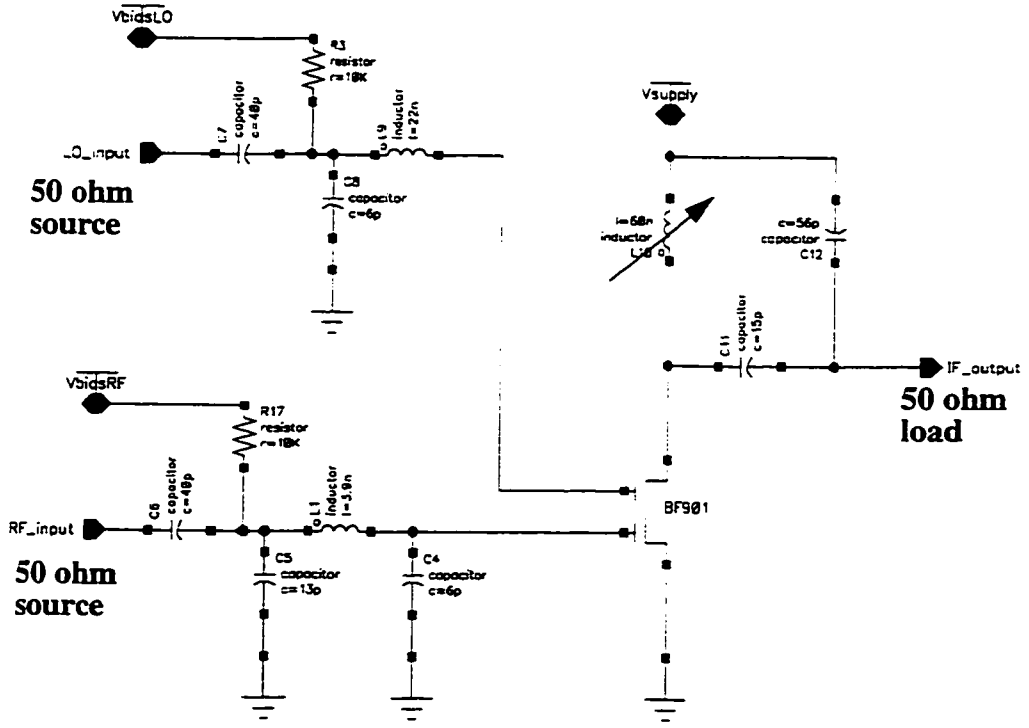

Figure 6.8 Schematic of final mixer circuit used for measurements

6.3.2 LO Power Selection

In order to confirm the optimum LO drive for the complete circuit, a new LO compression curve, shown in Figure 6.9, was generated for the mixer using the reactively matched port. It can be seen that, for this specific bias condition, there are 3 distinctive regions of compression, each with a separate slope. In region 1, the conversion gain/LO power slope is approximately 1 dB/dB, region 2 has slope of approximately 0.2 dB/dB, and the fully compressed region 3 has slope of 0 dB/dB. For LO powers larger than the re-

gion 3 values, the mixer experiences a decrease in gain corresponding to the mixer being overdriven by the LO.

An LO input power of 0 dBm was chosen for this case due to its location in region 2 of the graph, providing a reasonable LO compression characteristic and LO gate voltages which are in the range of values expected in an RFIC environment. In addition, the use of a narrowband LO matching network provides a voltage gain of approximately 13 dB. This produces an effective voltage on the second gate corresponding to the 13 dBm characterization curve generated using the 50 ohm port circuit [Figure 5.6] allowing the use of the 50 ohm characterization curves already generated in the design method.

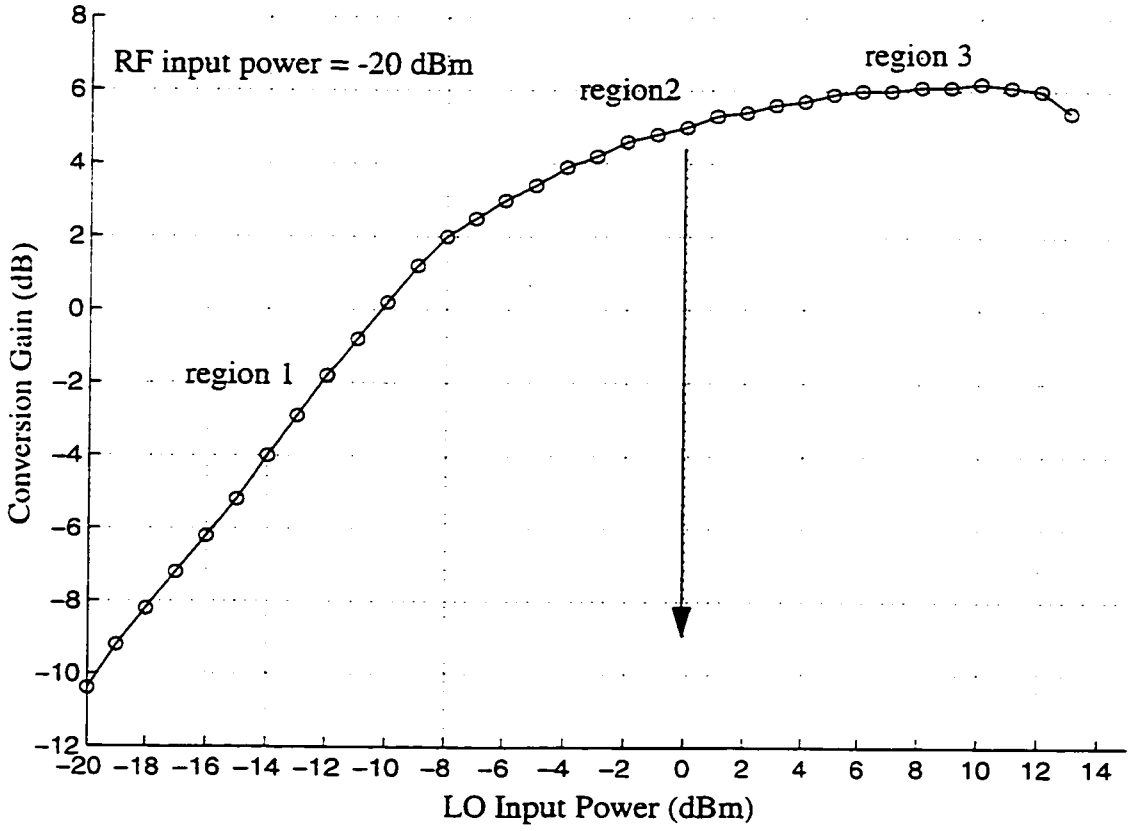

Figure 6.9 Graph of measured conversion gain as a function of LO drive level for the final mixer

6.3.3 Final Mixer Conversion Gain Characteristics

The conversion gain of the final mixer was measured over the RF bias range and compared to the estimate of the gain calculated using the 50 ohm characterization values for the 13 dBm LO power level. The expected gain value has been adjusted to account for the input and output matching network contributions to the gain.The results are plotted in Figure 6.10 and show that the calculated gain estimate using the 50 ohm characterization curves provides an accurate prediction of the final gain of the mixer.

From Figure 6.10, it can be seen that the final mixer gain peaks at the RF bias point of 1.35 Vdc due to the increase in the applied LO power level on the second gate, consistent with the characteristics found in Figure 6.2. To maximize the conversion gain as well as the linearity of the final mixer, the RF bias point for the expected region of operation is adjusted to 1.35 Vdc.

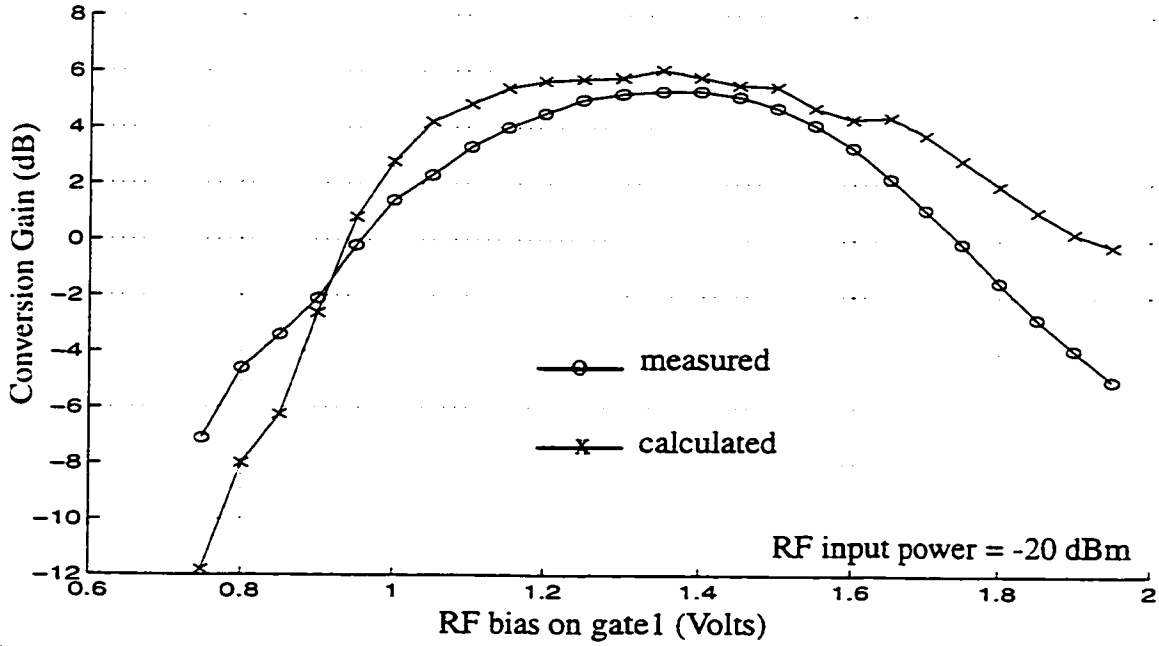

Figure 6.10 Graph of calculated and measured conversion gain as a function of RF bias for the final mixer

In order to better see the conversion gain estimation error, the gain error was calculated and plotted in Figure 6.11. This shows that the conversion gain estimation is accurate within 0.5 dB in the expected region of operation with the error increasing as the RF bias point is shifted away from the expected bias point of 1.35 Vdc.

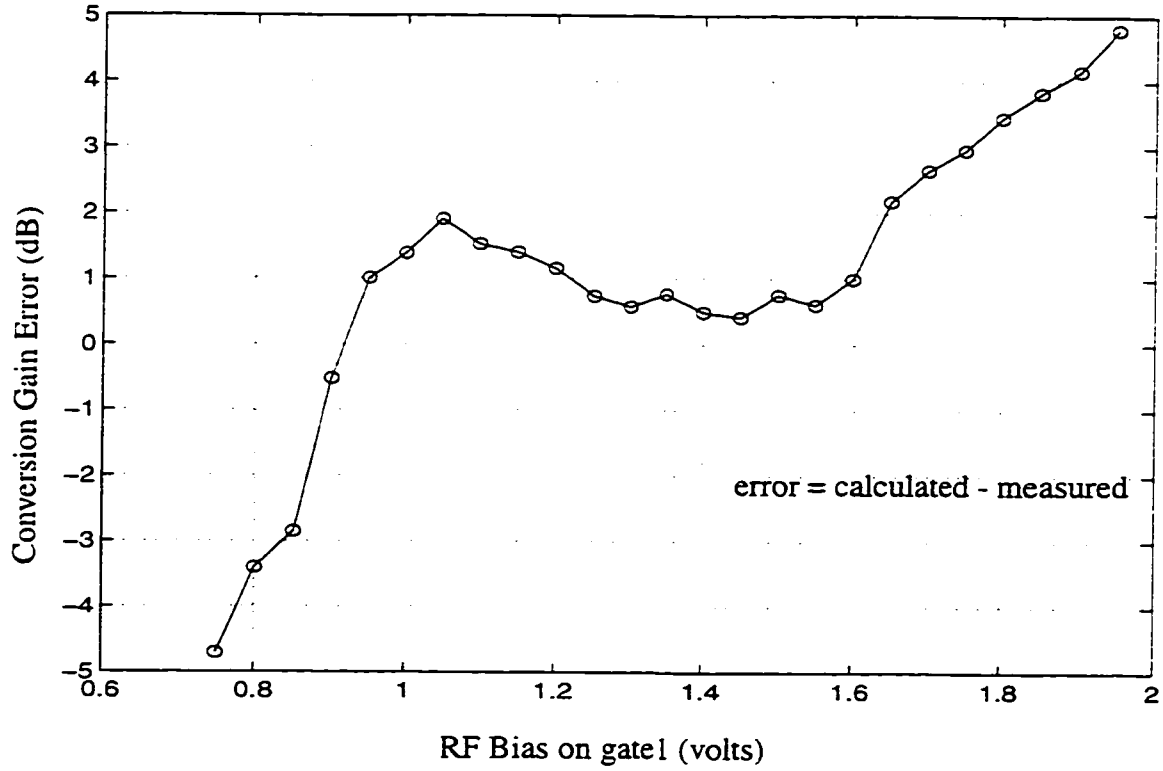

Figure 6.11 Graph of conversion gain error as a function of RF bias for the final mixer

Errors in the final gain estimation can be attributed to inaccuracies in the original 50 ohm characterization with additional inaccuracies in accounting for the external matching networks on the gate1 input and drain output. In addition, the use of the 50 ohm characterization curves is dependent upon the accurate accounting for the voltage gain in the LO matching network.

The errors away from the expected region of operation are also dependent upon the device port impedances which are a function of the bias levels. As the matching networks are narrowband, the bias position will change the impedance transformation seen at

the input of the mixer, directly affecting the gain calculation. If the gain estimation away from the expected bias point is needed, this discrepancy could be reduced by the inclusion of the real bias dependent port impedance in the gain estimation calculation.

6.4 Complete Mixer Results and Comparisons

The final mixer gain, input compression, and linearity characteristics were measured using the selected RF bias of 1.35 Vdc and LO bias and power of 1.4 Vdc and 0 dBm. The results are presented in Table 6.1 along with some other comparable dual gate circuits that have been reported in the literature or are commercially available.

For the designed mixer, the values in the first column correspond to the complete mixer as it was implemented in the thesis, including external matching circuitry. The values in the second column correspond to the mixer core structure only, excluding the effects of the input matching circuit and including the high drain load impedance to better indicate the capabilities of the mixer core. The third column summarizes a fully integrated, fully balanced MOS topology, reported by Sullivan et al. [6.2] with the results found by experiment. Column four summarizes a GaAsFET implementation of a fully balanced MESFET structure reported by Kanazawa et al. [6.3] for use in the 10 GHz range. Column five summarizes the characteristics of a commercially available MESFET dual gate mixer from Hewlett Packard [6.4] which includes an on-chip LO buffer amplifier.

Although it is difficult to directly compare these circuits, some general trends can be identified. Of the single ended topologies, the MOS mixer designed with the proposed method compares favourably with the commercially available GaAs mixer. The HP mixer uses an on chip LO buffer to reduce the LO drive required and does not include the

effects of input or output matching. This results in a similar structure to the mixer designed in this thesis and reflects what could be expected in an RFIC design environment.

Table 6.1: Table of designed mixer characteristics including comparisons with other dual gate mixers

Criteria	Designed Mixer	Designed Mixer	Sullivan et al. [6.2]	Kanazawa et al. [6.3]	HP IAM-91563 [6.4]	Units
Gain	5.4	11.9	0	6 to 8	11	dB
P1dB	-9	3	-10		-6.7	dBm
IP3i	0	13	0		0, -6	dBm
NF			13		8.5	dB
LO power	0	13 (effective)	6	10	-5	dBm
IF output frequency	163	163	250	100	250	MHz
RF signal frequency	.857	.857	1.9	.2 to.8	.9	GHz
DC current	3.5 (5V)	3.5 (5V)	8.8 (3V)	10 to 30	9 (3V)	mA (Vsupply)
Notes	Single ended topology MOS	Values adjusted to drain of the mixer	Fully balanced topology MOS	Fully balanced topology GaAs	Single ended topology GaAs	

The two fully balanced structures are useful in that they indicate what is possible with these structures as the design in this thesis can be readily extended to the fully balanced structure. If translated to a fully balanced structure, a four times increase of supply current, improved LO and RF rejection, improved signal handling capabilities, as well as increased conversion gain could be expected.

Although the power usage specification is difficult to compare due to the wide variations possible in the device dimensions and bias conditions, the proposed mixer compares favourably with all of the other structures. The power usage in the designed mixer could be reduced by a reduction in the power supply voltage, as long as the characterization included any effect this may have on the mixer structure. As the RFIC designer often has control over the size of devices used in the circuit, power usage for a given gain and linearity level can be designed for by judicious choice of device dimensions and bias conditions.

6.5 Summary

The generalization of the design method has provided a means to characterize the operation of the mixer in all ranges of operation. The accurate estimation of the gain and input compression characteristics has allowed the circuit designer some freedom to use the bias conditions and the matching networks to intelligently adjust the circuit parameters for gain and linearity in the final design.

With the selection of an appropriate transformation network on the LO port, a decrease in the required amount of applied LO power can be achieved. The selection of an appropriate output load impedance and input matching network allows the gain and linearity levels to be adjusted by the designer. The use of the IP3 characteristic by trading off gain and power usage for increased linearity allows a degree of freedom for the designer in the meeting of design specifications.

The mixer is shown to compare favourably with commercially available GaAs parts as well as other reported MOS and GaAs circuits of this type. The increased knowl-

edge provided by the design method presented in the thesis has allowed for intelligent design optimization as well as more effective comparison between dual gate mixer circuits and other mixer circuit topologies.

Chapter 7: Conclusions and Recommendations

This chapter summarizes the thesis and provides some conclusions and indicates some areas of the research that could be further studied to increase the knowledge in this field of study.

7.1 Thesis Summary

The dual gate mixer design method proposed in this thesis provides a simple, practical, methodical approach to calculate the gain and input compression point of a DG-FET mixer and can be easily implemented by either simulation or lab bench techniques. It relieves some of the reliance upon CAD tools and provides a means for the verification of CAD models and results by using easily measured DC and RF characteristics to fully characterize the mixer core. It provides an accurate, understandable procedure for identifying and verifying the appropriate bias conditions and also provides the means to define the minimum LO power level required.

7.2 Conclusions

The design method has been shown to be a subset of a generally accepted approach to the modeling and characterization of nonlinear circuits and thus to have a solid theoretical background. This allows the generalization of the design technique to other similar circuits with appropriate modifications to the method.

The design method places the mixer in a region of operation that provides maximum conversion transconductance and linearity for a given LO bias and power level. Al-

though this initial determination is done using DC characteristics, the use of the RF characterization procedure effectively includes the non-idealities involved in the high frequency operation of the circuit, providing enhanced accuracy at the expected frequencies of operation. The investigation into the RF characteristics also provides the designer with the information required to make intelligent design decisions to enable the consideration of a variety of design criteria to optimize the design of the final circuit.

The exploration into the various regions of operation has shown the flexibility of the method as well as the dual gate device. The general applicability of the method regardless of the bias conditions permits the almost arbitrary selection of bias conditions, providing a significant measure of flexibility to the designer.

The method concentrates on the characterization of the mixer core, from device gates to device drain. The use of standard, accepted RF methods to interface with the mixer core shows that the mixer is characterized in a manner consistent with currently accepted practises which adds validity and general applicability to the method. In addition, there is no loss in characterization accuracy if the proper care is taken with the interfacing circuits. This gate to drain characterization method also results in a method that is highly suited to the RFIC design environment where passive matching circuits are often not available.

The use of voltages and currents to define the characterization of the mixer core shows that the method is suitable for an IC design environment where the use of voltages and currents in the definition of signal levels is more common than the concept of power transfer as in the discrete RF design environment [7.1]. The use of voltages and cur-

rents allows the rapid visualization of the operation ranges of the device and permits selection of suitable bias and signal levels early in the design procedure.

The use of this design method has shown that the dual gate circuit topology can be a suitable alternative to the tree mixer structure and, with the comprehensive design method described in this thesis, may reveal some new circuit topologies previously unavailable to the RFIC designer.

7.3 Future Work

7.3.1 Noise Figure

The design method does not currently address the estimation or calculation of the mixer noise figure. Future work in this area would improve the usefulness of this design procedure greatly by removing the one significant specification that can not currently be characterized before construction. The effects of device size, current usage, bias condition, as well as matching circuitry should be investigated to provide the designer with as much information as possible.

7.3.2 Optimization of Device Dimensions

The results from this design method and that of Maas [7.2] and Tsironis [7.3] can be combined to gain further insight into the operation of the dual gate device. The use of Maas' numerical approach may provide the means for increased accuracy in the design and the use of Tsironis' DC nomogram can provide increased information concerning the internal operation of the device. The combination of the two techniques may provide in-

creased knowledge concerning the internal impedances that the mixer exhibits. This may provide increased information into the optimum sizing of transistors in the dual gate so as to maximize the conversion transconductance and linearity while minimizing the noise figure.

Appendix A: Theoretical Background Equations

This discussion presents a more detailed mathematical explanation for the theoretical background for the design method.After a brief presentation of the Taylor series approach, the design method is explained including the approximations made [references A.1 to A.5].

A.1 The Taylor Series

A memoryless, monotonic, nonlinear function of one variable, when the variable does not get too large, can be described in the following general way:

$$f(x) = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + \ldots \tag{A.1}$$

If the original function $f(x)$ has a small variation Δx included with the original variable x, such that $x \equiv x + \Delta x$, the Taylor series for the function can be written as:

$$f(x + \Delta x) = f(x) + \Delta x \cdot \dot{f}(x) + \frac{(\Delta x)^2}{2!}\ddot{f}(x) + \frac{(\Delta x)^3}{3!}\dddot{f}(x) + \ldots \tag{A.2}$$

It is possible to isolate the effects of the small variation Δx by subtracting out the original function resulting in:

$$f(\Delta x) = f(x + \Delta x) - f(x) \tag{A.3}$$

or, after expanding and then simplifying:

$$f(\Delta x) = \Delta x \dot{f}(x) + \frac{(\Delta x)^2}{2!}\ddot{f}(x) + \frac{(\Delta x)^3}{3!}\dddot{f}(x) + \ldots \quad \text{(A.4)}$$

If Δx is very small, higher orders of Δx will be very small and can be considered negligible. The effect of the small variation Δx on the function can then be approximated by:

$$f(\Delta x) \cong \Delta x \cdot \dot{f}(x) \quad \text{(A.5)}$$

which is the small variation Δx multiplied by the derivative of the original function with respect to the first variable x.

A.2 The Design Method Approach

A more explicit means of explaining the method will be used to show the practical application of the numerical concepts in the method. Some equations are repeated for clarity and continuity. In the following discussion, it is useful to use the following shorthand notation for the signals under consideration.

$$V_{lo} = E_{lo}\cos(\omega_{lo}t) \quad \text{(A.6)}$$

$$V_{rf} = E_{rf}\cos(\omega_{rf}t) \quad \text{(A.7)}$$

$$V_{if} = E_{if}\cos(\omega_{if}t) = E_{if}\cos(\omega_{(rf \pm lo)}t) \quad \text{(A.8)}$$

A memoryless, monotonic, nonlinear function of one variable can be described in the following way:

$$f(x) = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + \ldots \tag{A.9}$$

In this case, the output drain current, I_{ds}, caused by the LO waveform is needed.

$$x = V_{lo} \tag{A.10}$$

$$I_{ds}(V_{lo}) = a_0 + a_1 V_{lo} + a_2 V_{lo}^2 + a_3 V_{lo}^3 + \ldots \tag{A.11}$$

This function is defined as the steady state of the circuit and describes the non-reactive nonlinearities in the circuit caused by the LO and includes the LO frequency and amplitude information.

The addition of a small variation in the steady state function is described by:

$$f(x + \Delta x) = a_0 + a_1(x + \Delta x) + a_2(x + \Delta x)^2 + a_3(x + \Delta x)^3 + \ldots \tag{A.12}$$

In this case, a very small RF signal, V_{rf}, is added to the original circuit, so the output current caused by both the LO and RF waveforms can be described as:

$$x = V_{lo} + V_{rf} \tag{A.13}$$

$$I_{ds}(V_{lo} + V_{rf}) = a_0 + a_1(V_{lo} + V_{rf}) + a_2(V_{lo} + V_{rf})^2 + a_3(V_{lo} + V_{rf})^3 + \ldots \tag{A.14}$$

In order to isolate the effects of the small variation, the original function is subtracted from the composite function to get the output current caused by the RF signal alone resulting in:

$$f(\Delta x) = f(x + \Delta x) - f(x) \tag{A.15}$$

In this case,

$$I_{ds}(V_{rf}) = I_{ds}(V_{lo} + V_{rf}) - I_{ds}(Vlo) \tag{A.16}$$

or, after expanding and simplifying:

$$I_{ds}(V_{rf}) = a_1(V_{rf}) + a_2((V_{lo} + V_{rf})^2 - V_{lo}^2) + a_3((V_{lo} + V_{rf})^3 - V_{lo}^3) + \ldots \tag{A.17}$$

Recall that it was assumed that the RF signal creates negligible harmonics in the circuit. This is equivalent to ignoring the higher orders of the V_{rf} components in this function. Once simplified, the result, the output current caused by the RF waveform, is:

$$I_{ds}(V_{rf}) = V_{rf}(a_1 + 2a_2V_{lo} + 3a_3V_{lo}^2 + \ldots) \tag{A.18}$$

Recall the original steady state equation:

$$I_{ds}(V_{lo}) = a_0 + a_1V_{lo} + a_2{V_{lo}}^2 + a_3{V_{lo}}^3 + \ldots + a_n{V_{lo}}^n \tag{A.19}$$

and notice that:

$$\dot{I}_{ds}(V_{lo}) = \frac{d}{dV_{lo}}(I_{ds}) = a_1 + 2a_2V_{lo} + 3a_3V_{lo}^2 + \ldots \tag{A.20}$$

Using Equation A.20 in A.18 results in the simplification:

$$f(\Delta x) \cong \Delta x \cdot \dot{f}(x) \tag{A.21}$$

or, in this case:

$$I_{ds}(V_{rf}) \cong V_{rf}\dot{I}_{ds}(V_{lo}) \tag{A.22}$$

This result, the output current caused by the RF signal, can be seen as the RF input signal multiplied by the first derivative of the output drain current.

Another way to look at this result is to combine Equations A.16 and A.22 [A.3], resulting in:

$$I_{ds}(V_{rf}) = I_{ds}(V_{lo} + V_{rf}) - I_{ds}(Vlo) \cong V_{rf}\dot{I}_{ds}(V_{lo}) \tag{A.23}$$

The sensitivity of a function to a given variable is often described by the use of the derivative of the function with respect to the variable which, by definition, is:

$$\frac{df}{dx} = \lim_{\Delta x \to 0} \frac{(f(x + \Delta x) - f(x))}{\Delta x} \tag{A.24}$$

This identity is the basis for the estimation of the sensitivity of the steady state function to the RF input signal. Using this identity explicitly, the RF waveform is approximated by the DC bias points, separated by a small 'delta x'. The output current, at the LO frequency, is measured at these discrete steps to approximate the first derivative of the function $I_{ds}(V_{lo})$. This can also be seen by rearranging Equation A.23 to get:

$$\dot{I}_{ds}(V_{lo}) = \lim_{V_{rf} \to 0} \frac{(I_{ds}(V_{lo} + V_{rf}) - I_{ds}(V_{lo}))}{V_{rf}} \tag{A.25}$$

Although this result applies to all of the components of the original $I_{ds}(V_{lo})$ function, only the LO frequency component generates the frequencies that we desire. This

simplification allows the measurement of only the LO frequency component to calculate the conversion transconductance of the mixer. Thus, the numerator describes the change in the output current at the LO frequency caused by the small change in the RF signal and the denominator describes the small change in the RF signal. Initially, during the characterization, this small change is approximated by the DC bias level difference. The results are then used to extrapolate between values and make the estimate for a real RF input signal. It can be seen then that an increased number of points during the characterization will enhance the accuracy of the characterization.

References

List of Abbreviations

IEEE	Institute of Electrical and Electronic Engineers
MTT	IEEE Transactions on Microwave Theory and Techniques
MTT-S	MTT Symposium Digest
JSSC	Journal of Solid State Circuits
CICC	Custom Integrated Circuit Conference
ISSCC	IEEE International Solid State Circuits Conference
UCLA	University of California, Los Angeles
UCB	University of California, Berkeley

Chapter One

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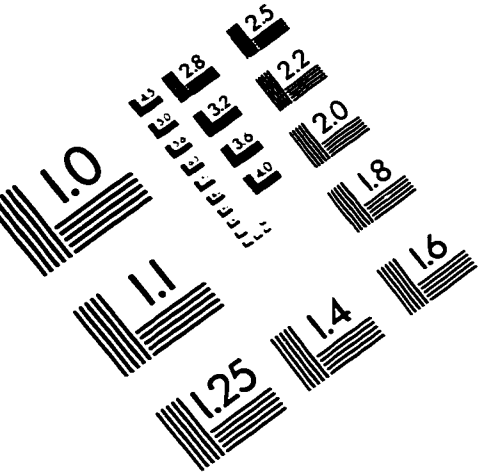

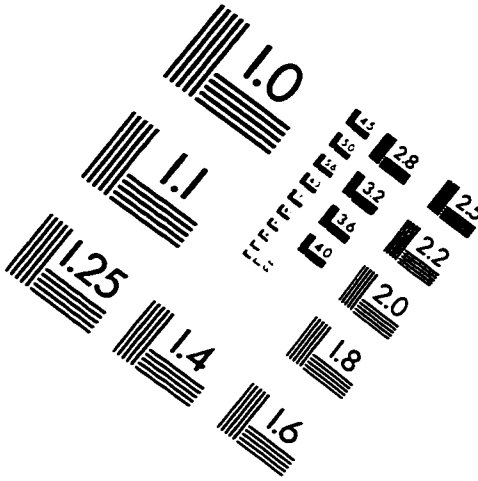

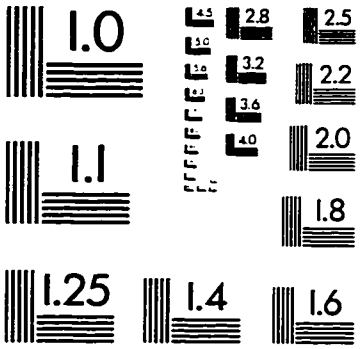

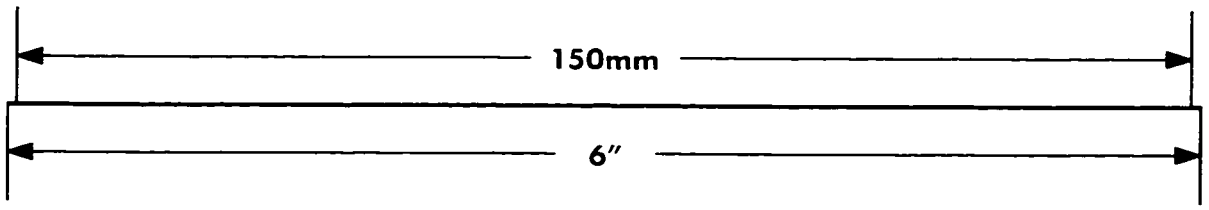

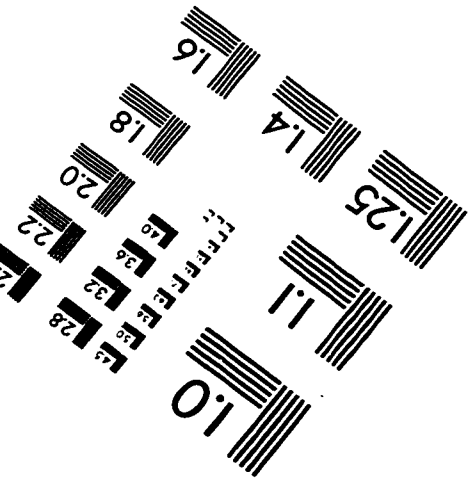

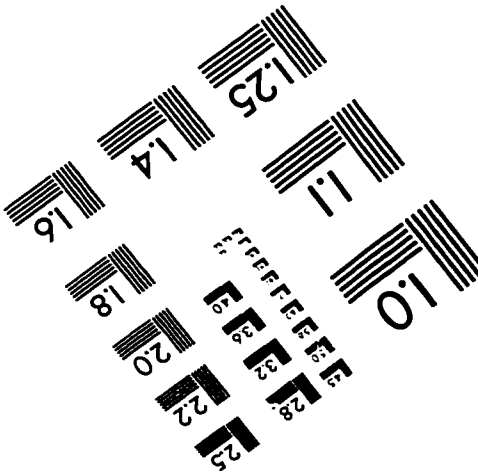

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