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Sigma-Delta Modulation for FM Mobile Radio

by

Norman M. Filiol, B. Eng., M. Eng.

A Ph.D. thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements
for the degree of
Doctor of Philosophy

Ottawa-Carleton Institute for Electrical Engineering,
Department of Electronics,
Carleton University,
Ottawa, Ontario, Canada

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in partial fulfillment of the requirements
for the degree of Doctor of Philosophy

Chair, Department of Electronics

Thesis Supervisor

External Examiner

Carleton University,
January 12, 1999

Abstract

This thesis presents VLSI architectures for frequency synthesizers and frequency and phase modulators and demodulators, realized using $\Sigma\Delta$ modulation techniques.

These building blocks use VLSI in order to achieve small size and low power dissipation. Over-sampling and noise shaping techniques are used to achieve robust architectures and to convert analog signals to the digital domain in order to take advantage of low cost digital-signal-processing techniques.

A high resolution fractional-N RF frequency synthesizer is presented which is controlled by a fourth-order digital $\Sigma\Delta$ modulator. The high resolution allows the synthesizer to be digitally modulated directly at RF. A simplified digital filter which makes use of $\Sigma\Delta$ quantized tap coefficients is included which provides built in GMSK pulse shaping for data transmission. Quantization of the tap coefficients to single bit values not only simplifies the filter architecture but the fourth-order modulator as well.

The synthesizer makes use of custom VLSI with only a simple off chip loop filter and VCO. The synthesizer operates from a single three volt supply and the two chips consume a total of 32 mW. Phase noise levels are less than -90 dBc/Hz over a 19.6 MHz tuning range.

A receive path $\Sigma\Delta$ frequency-to-digital converter which makes use of only switched capacitor and digital circuit techniques is presented. The novel architecture used reduces the amount of out of band quantization noise for low deviation FM signals when compared to previous architectures and complements the GMSK transmitter described above. A hardware version of the frequency-to-digital converter has been designed in a 0.8 μm BiCMOS process to operate at an IF frequency of 112.5 MHz.

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List of Terms and Symbols

A/D or ADC	Analog-to-Digital Converter or conversion
AIWN	Additive Independent White Noise
AM	Amplitude Modulation
β	Modulation index
BER	Bit-Error Rate
B_f	Roll-off Factor
BPF	Bandpass Filter
Bt	Ratio of 3-dB bandwidth of Gaussian pulse shaping filter to symbol rate
BW	Bandwidth
CDMA	Code-Division Multiple Access
CML	Emitter Coupled Logic without emitter followers
CMRR	Common Mode Rejection Ratio
DAC	Digital-to-Analog Converter or Conversion
DDS	Direct Digital Frequency Synthesis
DLL	Delay Locked Loop
DMD	Dual-Modulus Divider
DPA	Digital Phase Accumulator
DPC	Digital-to-Phase converter or conversion
DS	Direct Sequence Spread Spectrum
DSP	Digital Signal Processing
ECL	Emitter Coupled Logic
fm	Modulating Frequency
Δf	Maximum frequency deviation of an FM signal
FDC	Frequency-to-Digital Converter
FFH	Fast Frequency Hopping
FFT	Fast-Fourier Transform
FH	Frequency-Hopping
FIR	Finite Impulse Response
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
Fref	Reference Frequency
Fs	Sampling Frequency
f_t	Unity current gain-bandwidth product for a bipolar transistor
gm	Transconductance
GMSK	Gaussian Minimum Shift Keying
H_{CL}	Closed-Loop transfer function
HDL	Hardware Definition Language
H_{OL}	Open-Loop transfer function

IC	Integrated Circuit
IF	Intermediate Frequency
I and Q	In phase and Quadrature
ISI	Inter-Symbol Interference
ISM	Instrumentation Scientific and Medical Band
J_n	Bessel Function
K_f	FM proportionality constant
K_{PD}	Phase Detector gain
K_q	Quantizer Gain
K_{VCO}	Voltage Controlled Oscillator Gain
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Lowpass Filter
LSB	Least Significant Bit
MASH	Multi-Stage Noise Shaping
MFE	Modulator Front-end
MMD	Multi-Modulus Divider
MUX	Multiplexer
op-amp	Operational Amplifier
OSR	Oversampling Ratio
PA	Power Amplifier
PCB	Printed Circuit Board
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
PN	Pseudo-Random Number
RF	Radio Frequency
rms	Root-Mean Square
ROM	Read Only Memory
RSSI	Received Signal Strength Indicator
SAW	Surface Acoustic Wave filter
SFH	Slow Frequency Hopping
SNR	Signal-to-Noise Ratio
SSB	Single Sideband
TDD	Time Division Duplexing
TH	Time Hopping
TQFP	Quad Flatpack
T_s	Symbol Period
TTL	Transistor Transistor Logic
UGBW	Unity-Gain Bandwidth
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration
ω_n	Natural Frequency
XNOR	Exclusive NOR
ζ	Damping Factor

Chapter 1 Introduction

1.1 Introduction

The topic of this thesis is VLSI architectures for frequency synthesizers and frequency and phase modulators and demodulators, realized using $\Sigma\Delta$ modulation techniques.

Circuits for use in wireless radio applications must have low power consumption and be well suited for VLSI implementation. In a transceiver, some form of frequency synthesizer is generally required in order to generate the local oscillator (LO) and carrier, and a modulator is used to superimpose data on to this carrier. A particular form of modulation that this thesis is focussed on is constant envelope modulation (i.e., phase or frequency modulation), such as Gaussian Minimum Shift Keying (GMSK).

Several wireless radio standards employ GMSK digital data modulation. The usual approach used in a GMSK transmitter is to generate the I and Q (In-phase and Quadrature) channels containing the baseband modulation, using a digital finite impulse response (FIR) filter and direct digital synthesis (using a digital-phase accumulator (DPA) and sine/cosine lookup tables), combine these using a summer, and up convert the resulting signal to RF using a local oscillator and various mixers and filters, as shown in Figure 1-1 [RiCo94]. The components that are typically included in VLSI implementations of this architecture are shown in the shaded regions. The voltage controlled oscillators required for the I and Q mixing operation and the upconversion stage are often external components in order to achieve acceptable noise performance. Power amplifiers that generate high output power are difficult to integrate due to power handling and thermal considerations.

Figure 1-1: Typical GSM Transmitter

The approach shown in Figure 1-1 is expensive, and the highly selective filters required to attenuate harmonics of the modulated signal are not easily integrated due to the high quality factors required. As well, the approach is capable of modulating amplitude as well as phase, a capability which is not necessary for constant envelope modulation. Recently, a move towards offset phase-locked loop techniques (as a transmit synthesizer) has been occurring [BeRa98]. Such techniques are capable of constant envelope modulation. This architecture eliminates the highly selective filters that are needed in the upconversion chain of Figure 1-1, and the power amplifier can be driven directly by the VCO, whose out of band noise characteristics can be of high quality. This eliminates the need for the upconversion mixer, used in the approach of Figure 1-1, which can contribute significant phase noise to the transmitter output. However, the offset PLL technique still requires separate I and Q channels, summers, mixers, and external filters. An example of an offset transmit PLL, similar to the one presented in [BeRa98], is shown in Figure 1-2. The components that are implemented in VLSI form are shown in the shaded regions.

Figure 1-2: Offset PLL Based GMSK Transmitter

The approach taken in this thesis, which is also capable of constant envelope modulation, is $\Sigma\Delta$ controlled fractional-N frequency synthesis. These types of synthesizers have high frequency resolution and fast settling times. The GMSK data filter can be included as part of the synthesizer and simplified by using $\Sigma\Delta$ quantized tap coefficients, as demonstrated in [RCK93]. The need for separate I and Q channels, mixers, summers, and external filters is eliminated. The result is direct manipulation of the instantaneous frequency of the carrier, using mostly digital circuits. While $\Sigma\Delta$ controlled synthesizers have been in use for several years [RCK93],[MiCo90], few VLSI implementations seem to exist [PTS97], and none of these include a GMSK data filter which makes use of $\Sigma\Delta$ quantized tap coefficients.

Moving now to the receiver side, some form of demodulator is needed to recover the data. It is desirable to convert the incoming signal to the digital domain as closely to the RF front end (antenna, LNA, etc.,) as possible, in order to decrease the number of downconversion stages that are required and take advantage of powerful digital signal processing techniques. Recently, band-pass $\Sigma\Delta$ modulators have been considered for IF analog-to-digital conversion, as such oversam-

pled data converters are highly linear and can operate at high frequencies [SSJB96],[JSS97],[OWo97],[BaSn98]. However, such architectures can be complex, and the circuits used consume high power at high IF frequencies (See Table 4.1). While several digital modulation schemes employ some degree of amplitude modulation, there are still many constant amplitude angle-modulation schemes in use, such as, GMSK and analog FM. The approach used in this thesis for demodulation of such signals is divider based $\Sigma\Delta$ frequency-to-digital (FDC) conversion or discrimination [BeCo94]. Even though these architectures have been in existence for some time, relatively little research has been done in this area. $\Sigma\Delta$ FDCs are highly linear and can operate at IF frequencies well into the Gigahertz frequency range with potentially low power consumption (See Table 4.1). They perform both analog-to-digital conversion and FM demodulation. $\Sigma\Delta$ FDCs do not preserve the amplitude information of the input signal and, hence, all frequency selective filtering must be performed prior to the FDC input. Due to the high cost of filters that can perform this task at high frequencies, the IF frequency is limited to less than a Gigahertz in practical applications. However, $\Sigma\Delta$ FDCs can be used in applications that require highly linear and inexpensive frequency discriminators, such as wireless phones that make use of analog FM or GMSK type data modulation. Only a few divider based $\Sigma\Delta$ FDC architectures have been examined and a wide area of research remains [BeCo94],[Bax96],[RFCP98].

The modulation and demodulation techniques described above, and used in this thesis, utilize $\Sigma\Delta$ conversion of instantaneous frequency and phase variables, an area of research that is not commonly known. It is hoped that this thesis will demonstrate the high potential in this area of research, as well as relating it more clearly to the wide base of information that is available on $\Sigma\Delta$ modulation techniques.

The architectures presented in this thesis are for general use in digital radio. However, the implementations presented are targeted at a frequency-hopping cordless phone system which operates in the lower Instrumentation Scientific and Medical Band (ISM), from 902-928 MHz. Although the system has not been built, this specification is presented in order to put these components into context.

1.2 Contributions

The contributions made in this thesis to the area of VLSI architectures for frequency synthesis and demodulation are the following:

1) A novel architecture for a receive path $\Sigma\Delta$ frequency-to-digital converter will be shown that has a reduced fullscale input range and reduced out of band quantization noise. This architecture includes a $\Sigma\Delta$ modulator in the feedback path of another $\Sigma\Delta$ modulator. An analysis of how this architecture operates is presented. The effects of modulator overload, due to the quantization error added to the loop by the digital $\Sigma\Delta$ modulator in the feedback path, are examined. How these effects were mitigated is also explained. The first known full hardware design of a $\Sigma\Delta$ FDC with a digital $\Sigma\Delta$ modulator in the feedback path is presented. This design includes a switched-capacitor integrator which makes use of a novel sampled-time phase detector. The input to this integrator is phase rather than voltage. The difference between input referred frequency error and input referred phase error in the $\Sigma\Delta$ FDC is clarified. The contribution to the input referred frequency error and phase error due to noise in the analog block is also determined.

2) Although the work presented in [RiCo94] showed the feasibility of quantizing the tap coefficients in a digital pulse shaping filter to single bit values using a software $\Sigma\Delta$ modulator, the demonstration was partly done at the software level, and such a modulator was never combined with an integrated $\Sigma\Delta$ controlled synthesizer. It will be shown, using experimental results, that through careful design and consideration, a low power transmitter can be built by combining both the $\Sigma\Delta$ controlled synthesizer and the above filter. Also, an error in the work presented in [RiCo94] has been corrected. The filter response stored in the ROM should have been that of a Gaussian pulse convolved with a square pulse. Instead, the non-convolved pulse was used.

The design makes use of custom VLSI with only a few external components required. Many trade-offs and issues have been addressed in order to ensure good performance and low power consumption. It will be shown that careful design

using ECL/CML logic can result in low power consumption at high operating frequencies. While the synthesizer used is basically a direct combination and implementation of previously described techniques, it does demonstrate the value of such a synthesizer in mobile radio applications.

A revised version of the GMSK filter described above will be presented which greatly reduces the end effects in the quantized (explained in Chapter 3) tap coefficients, thus increasing the achievable stopband attenuation by more than 30 dB.

3) A low delay multi-modulus divider architecture is presented.

4) The link between oversampled voltage data converters and oversampled phase/frequency data converters is clarified and their usefulness in the manipulation of FM signals will be demonstrated in the contexts of both a transmitter and a receiver.

1.3 Thesis Outline

The remainder of this thesis is organized as follows. Chapter 2 presents a cordless phone system which makes use of a $\Sigma\Delta$ controlled frequency synthesizer and a $\Sigma\Delta$ frequency-to-digital converter. The technical background required to understand the work presented in thesis is reviewed as well. Chapter 3 outlines the design and testing of a fractional-N frequency synthesizer which is controlled using a fourth-order digital $\Sigma\Delta$ modulator and has built in GMSK data modulation which makes use of $\Sigma\Delta$ quantized tap coefficients. Chapter 4 outlines the requirements for a receive path frequency-to-digital converter and presents a novel architecture which may meet these requirements. An analysis of the new architecture is also presented. Chapter 5 presents design and simulation results for a hardware version of the $\Sigma\Delta$ frequency-to-digital converter, presented in Chapter 4, implemented in a 0.8 μm BiCMOS process. Chapter 6 presents conclusions and recommendations for future work.

Chapter 2 Motivation and Background

2.1 Introduction

This chapter presents a frequency-hopping transceiver which makes use of a $\Sigma\Delta$ controlled fractional-N frequency synthesizer and a $\Sigma\Delta$ frequency-to-digital converter (FDC). The transceiver would be used in a cordless phone application which would operate in the lower Instrumentation Scientific and Medical (ISM) band from 902 - 928 MHz. A block diagram of the system is presented in Figure 2-1. The $\Sigma\Delta$ FDC and the $\Sigma\Delta$ controlled fractional-N frequency synthesizer are shaded. Although the system is not realized in this thesis, it is presented here in order to place where these components are used into context. It is also important to note that this system was not designed by the author, but rather is very similar to a specification for a product that was almost put into commercial use. Finally, some of the technical background required in order to understand the system is reviewed.

The specifications and operation of the system will now be described in greater detail.

2.2 System Operation and Specifications

The system shown in Figure 2-1 can be split into two paths, the receive path (top), and the transmit path (bottom).

In the receive path, the frequency-hopped signal arrives at the antenna and is passed through a bandpass filter (BPF) to the RF front end which consists of a low noise amplifier LNA, a down-conversion mixer and a surface acoustic wave (SAW) filter. These components are standard and would be implemented in either CMOS or bipolar technology depending on the specifications

(noise figure, gain, etc.). However, since the incoming signal is frequency-hopping, the local oscillator (L.O.) must be agile in order to despread the signal. This agile L.O. is shared and is also used as the transmit synthesizer and modulator through the use of time division duplexing (TDD). The IF frequency is generated at 112.5 MHz. An external SAW is used as the IF filter whose output is fed into the $\Sigma\Delta$ FDC shown in the shaded area. The demodulator consists of a limiting amplifier and receive signal strength indicator (RSSI) circuitry, followed by a $\Sigma\Delta$ phase-locked loop (PLL) that performs frequency-to-digital-conversion. This block will be explained in greater detail.

Figure 2-1: Proposed Frequency-Hopping Transceiver

The output bitstream from the $\Sigma\Delta$ modulator is fed to the baseband digital signal processing block (DSP) where decimation, filtering, and demodulation are performed.

In the transmit path the frequency control word and unshaped data bits are fed into the $\Sigma\Delta$ controlled fractional-N frequency synthesizer shown in the shaded area. The synthesizer consists of a 4th order $\Sigma\Delta$ modulator, a GMSK data filter which makes use of $\Sigma\Delta$ quantized tap coefficients, and a high speed PLL incorporating a multi-modulus divider (MMD). The synthesizer is used both as a frequency-hopped GMSK data transmitter and an agile receive path L.O. for despread-ing and downconversion of the incoming signal. Therefore, the downconversion mixer that fol-lows the synthesizer in the transmit path is necessary. During reception, the L.O. is hopped in the frequency band from 1014.5 MHz - 1040.5 MHz giving the 112.5 MHz IF. During transmission, the synthesizer is hopped in the frequency band from 1003.8 MHz - 1029.8 MHz. This requires a downconversion to 902 MHz - 928 MHz to be performed. This is accomplished using a fixed L.O at 101.8 MHz and the downconversion mixer shown. This is followed by a power amplifier (PA) and lowpass filter (LPF). Note that the downconversion performed in the transmit path could have been accomplished using a higher frequency fixed L.O. However, the original architecture had planned for a second IF of 10.7 MHz in the receive path, and therefore, by having a 10.7 MHz off-set in the synthesizer between transmit and receive mode, the fixed second IF L.O could have been shared.

The specifications for the system shown in Figure 2-1 are given in Table 3-1 along with those for some other commonly used wireless standards. Those that relate to the data modulator, synthe-sizer, and the receive path data demodulator are shaded as they pertain to the work performed in this thesis. Any specifications that could not be found or were not known at the time this table was compiled have been left blank in the table.

The biggest drawback in sharing the synthesizer between the transmit and receive paths is the wide bandwidth required in the VCO in order to cover the desired frequency bands. This means that a high tuning constant is required, increasing phase noise in the loop. Some of these problems

could be avoided through the use of a dual band VCO.

Table 2.1: System Specifications

General Specifications	CT2+	DECT	DCS-1800	Proposed
Receive Band (MHz)	944-952	1880-1900	1805-1880	902-928
Transmit Band (MHz)	944-952	1880-1900	1710-1785	902-928
Bandwidth (MHz)	4 (8)	20	150	26
Channelization	FDMA	TDMA/FDM	TDMA/FDM	Freq. Hopping
Channels per Carrier	1	12	16	1
Duplex Method	TDD	TDD	FDD	TDD
Channel Bit Rate (Kb/s)	72	1152	270.833	80
Speech Codec	ADPCM	ADPCM	RPE-LTP	ADPCM
Bit Rate Voice (Kb/s)	32	32	13	32
Modulation	GFSK	GFSK	GMSK	GMSK
Gaussian Filter BT	0.5	0.5	0.3	0.5
Synthesizer Specifications				
Channel Spacing (KHz)	100	1728	200	200
Number of Channels	40	10	750	127
Channel Frequency Accuracy	+/- 10 KHz	+/-50 KHz		+/- 2.25 KHz
Synthesizer Switching Speed	< 2000 μ s	< 450 μ s		< 175 μ s
Phase Noise (@100KHz)				-126 dBc/Hz
Transmitter Specifications				
Peak Transmit Power (mW)	10	250	250-2000	20
Average Transmit Power (mW)	5	10	30-250	8
Power Control Range	20 dB (var)	none		13 dB(2 levels)
Receiver Specifications				
Sensitivity (dBm)	-100	-83		-101.6
SNR Required (dB)	13.6	13.6		13.3
Noise Figure (dB)	11.8	16.8		8.3
Input TOI (dBm)	-19	-27.5		-16

2.2.1 Agile GMSK transmitter and Local Oscillator

The frequency synthesizer shown in Figure 2-1 is a $\Sigma\Delta$ controlled fractional-N PLL [RCK93]. The synthesizer consists of two custom ICs. One is a 0.5 μm CMOS chip which contains a fourth-order digital $\Sigma\Delta$ modulator, a GMSK data modulator which makes use of $\Sigma\Delta$ quantized tap coefficients, and a serial bus allowing for microprocessor control. The second chip is a 0.5 μm bipolar IC which contains a multi-modulus divider (MMD), a phase frequency detector (PFD) and an output charge pump. The only external components required are a simple loop filter and a voltage controlled oscillator (VCO). The synthesizer design and measurement results are presented in Chapter 3. Most of the transmit requirements for the synthesizer were met. However, due to the wide loop bandwidth required in order to allow GMSK modulation and fast settling times, the L.O. phase noise requirements were not met (i.e., -126 dBc/Hz @ 100 KHz).

2.2.2 $\Sigma\Delta$ Frequency-to-Digital Converter

The $\Sigma\Delta$ FDC shown in Figure 2-1 is a novel architecture based on the $\Sigma\Delta$ FDC presented later on in this chapter. The new architecture uses fractional- δ division techniques in order to reduce the fullscale input range and out of band quantization noise when used to detect small deviation FM signals, relative to its reference frequency, such as the GMSK data modulation proposed for the system of Figure 2-1. The output is a single bit bitstream whose average density is an accurate representation of the instantaneous frequency deviations of the IF signal. The $\Sigma\Delta$ FDC is presented and analyzed in Chapter 4. Chapter 5 presents the design of the $\Sigma\Delta$ FDC in a 0.8 μm BiCMOS process. The limiting amplifier and RSSI circuitry were not included in the design, as demonstration of functionality and feasibility of the architecture were the goal of this first implementation. Due to unforeseen circumstances, fabrication of the circuit in this section was not possible, but the design was carried forward completely up to the fabrication stage in order to establish feasibility of the architecture. Analysis of the design indicates that it would be suitable for use in the system shown in Figure 2-1.

2.3 Frequency Modulation

The $\Sigma\Delta$ controlled synthesizer shown in Figure 2-1 can only generate constant amplitude angle modulation. Therefore, a general review of FM modulation is useful.

In order to transmit data from one location to another through a wireless link, some form of carrier is required. Typically this carrier is at a fixed frequency and has the following time domain equation;

$$X(t) = A \cos(2\pi f_c t) \quad (2-1)$$

where A is the voltage amplitude of the carrier and f_c is the frequency in Hertz. Data can be added to this carrier through amplitude modulation, frequency modulation, or phase modulation and can be digital or analog in nature. In amplitude modulation, the amplitude of the carrier is varied by the data. In frequency modulation, the frequency of the carrier is varied by the data and, similarly, in phase modulation the phase of the carrier is varied by the data. In this document, standard amplitude modulation is not discussed as it is no longer common in mobile radio. Phase modulation and frequency modulation can be classified together as angle modulation.

The general representation of any angle modulated carrier in the time domain is as follows:

$$s(t) = A \cos(2\pi f_c t + \theta(t)) \quad (2-2)$$

where $\theta(t)$ is the phase of the modulating signal. For phase modulation, $\theta(t)$ is proportional to, $m(t)$, the modulating signal. For frequency modulation, $\theta(t)$ is proportional to the integral of, $m(t)$, the modulating signal. This section only deals with frequency modulation, although the concepts are very similar and related to each other through integration or differentiation.

The general equation in the time domain for a frequency modulated signal is;

$$s(t) = A \cos\left(2\pi f_c t + 2\pi \int_0^t m(\tau) d\tau\right) \quad (2-3)$$

where $m(\tau)$ is the modulating signal. The instantaneous frequency of the carrier is defined as the

derivative of the carrier phase. For the FM signal described by Equation (2-3), the instantaneous frequency is;

$$\omega(t) = 2\pi f_c + 2\pi m(t) \quad (2-4)$$

where the first term is the constant carrier frequency and the second term is the time varying frequency due to the modulating signal. It is important to realize that if one wants to determine the frequency spectrum of the modulated carrier, the instantaneous frequency does not provide this information. The instantaneous frequency only gives information about the frequency deviations of the modulating signal and not the spectrum generated by the rate of change of the modulation, in the Fourier sense. In the following paragraphs, the spectrum for a fixed carrier frequency modulated by a sinusoid will be determined and the concept of narrowband versus wideband FM will be presented.

The time domain equation for a carrier frequency modulated by a pure sinusoidal waveform is;

$$s(t) = A \cos \left[2\pi f_c t + 2\pi \int_0^t \Delta f \cos(2\pi f_m \tau) d\tau \right] \quad (2-5)$$

where f_m is the frequency of the modulating sinusoid and Δf is the maximum frequency deviation. Δf is equal to ak_f , with a being the amplitude of the modulating sinusoid and k_f being the proportionality constant with units of Hz/V. Equation (2-5) can be re-written as;

$$s(t) = A \cos \left[2\pi f_c t + \frac{\Delta f}{f_m} \sin(2\pi f_m t) \right] \quad (2-6)$$

$\Delta f/f_m$ is defined as the modulation index and will be denoted as β . Equation (2-6) can further be expanded to give;

$$s(t) = A \cos(2\pi f_c t) \cos(\beta \sin(2\pi f_m t)) - A \sin(2\pi f_c t) \sin(\beta \sin(2\pi f_m t)) \quad (2-7)$$

If $\Delta f \ll f_m$ (i.e., $\beta \ll 1$) the following approximations can be made. The cosine of a small angle is approximately one, and the sine of a small angle is approximately equal to the angle itself. Therefore, Equation (2-7) becomes;

$$s(t) = A \cos(2\pi f_c t) - A\beta \sin(2\pi f_m t) \sin(2\pi f_c t) \quad (2-8)$$

This is the equation for narrowband FM. Taking the Fourier transform of Equation (2-8) [Rod91]

we obtain the following frequency domain equation;

$$S(f) = S_1(f) + S_2(f) \quad (2-9)$$

where the first term, $S_1(f)$, is;

$$S_1(f) = \frac{A}{2}[\delta(f - f_c) + \delta(f + f_c)] \quad (2-10)$$

and the second term, $S_2(f)$, is;

$$S_2(f) = \frac{A\beta}{4}[[\delta(f - f_c + f_m) - \delta(f - f_c - f_m)] - [\delta(f + f_c + f_m) - \delta(f + f_c - f_m)]] \quad (2-11)$$

The power spectrum for the waveform in Equation (2-11) is shown in Figure 2-2.

Figure 2-2: Sinusoidal Narrowband FM

If $\Delta f \gg f_m$ (i.e., $\beta \gg 1$) the narrowband approximation used to simplify Equation (2-7) is no longer valid and the approach used in [Stre77] must be taken in order to obtain the frequency spectrum. In this case, Equation (2-6) can be written in exponential form [Stre77] as follows;

$$s(t) = \text{Re}\{Ae^{j2\pi f_c t} e^{j\beta \sin(2\pi f_m t)}\} \quad (2-12)$$

The second term can be expanded into a Fourier series given as;

$$e^{j\beta \sin(2\pi f_m t)} = \sum_{n=-\infty}^{\infty} F_n e^{jn2\pi f_m t} \quad (2-13)$$

Where the Fourier coefficients, F_n , are given by [Stre77];

$$F_n = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} e^{j\beta \sin(2\pi f_m t)} e^{-jn2\pi f_m t} dt \quad (2-14)$$

Following the derivation in [Stre77] the solution to the integral, given in Equation (2-14), is;

$$e^{j\beta \sin(2\pi f_m t)} = \sum_{n=-\infty}^{\infty} J_n(\beta) e^{jn2\pi f_m t} \quad (2-15)$$

where J_n is a class of functions known as Bessel functions of the first kind. Bessel functions appear as the solution to many problems and, thus, their values have been extensively tabulated. Figure 2-3 shows a plot of the first four Bessel functions of the first kind. The end result is that Equation (2-6) can be re-written as;

$$s(t) = A \sum_{n=-\infty}^{\infty} J_n(\beta) \cos(2\pi f_c t + 2\pi n f_m t) \quad (2-16)$$

Thus, it can be seen that a wideband FM signal is in fact composed of an infinite number of side-

Figure 2-3: Bessel Functions of the First Kind

bands of varying amplitude. However, depending on the modulation index, β , many of these sidebands are not significant and can be ignored. Figure 2-4 shows plots of the spectra for an FM modulated signal with various values of modulation index [Stre77]. The plots were obtained through MATLAB calculations.

Since any waveform can be constructed through the superposition of various sinusoidal components, the above analysis can be generalized to any modulating signal. The total bandwidth occupancy of an FM signal can be estimated using Carsons' rule [Rod91], given as;

$$BW \approx 2(\Delta f + f_m) \quad (2-17)$$

Where Δf is the maximum frequency deviation of the FM signal and f_m is the highest frequency component of the modulating signal.

2.3.1 Digital Frequency Modulation

The general time domain equation for a digitally modulated FM waveform is given by;

$$s(t) = A \cos(2\pi f_c t + \theta(t)) \quad (2-18)$$

Where f_c is the carrier frequency and $\theta(t)$ is the phase of the modulating data, given by;

$$\theta(t) = 2\pi \int_0^t g(\tau) d\tau \quad (2-19)$$

Where $g(\tau)$ is the frequency response of the modulation, given by [ATS83];

$$g(t) = h \sum_n K_n b(t - nT_s) \quad (2-20)$$

Where h is a scaling factor, K_n is the value of the n th data symbol (1 or -1), $b(t)$ is the normalized (area under pulse set to one) impulse response of the filter used to shape the baseband data, and T_s is the data symbol period.

Gaussian minimum shift keying (GMSK) is a common type of data modulation used in digital radio applications and is of interest in this thesis as it is used in several radio standards. Minimum shift keying means that the carrier phase-shift resulting from the value of a transmitted data bit is

Figure 2-4: Frequency Spectrum for Wideband Sinusoidal FM

$\pm \pi/2$ radians. This means that the scaling factor, h , as shown in Equation (2-20) is equal to $1/4$. The pulse shaping filter employed in GMSK is a Gaussian lowpass filter (i.e., has a Gaussian impulse response).

2.4 Frequency-Hopping Spread-Spectrum

Traditionally, in radio communications, data is transmitted using a fixed carrier frequency. However, if there is an impairment at the carrier frequency due to interference or other phenomena, such as multi-path fading, the data may be lost. In spread-spectrum, the transmitted data is spread over a wide band of frequencies so that statistically the impairments can be avoided, thus reducing the bit-error rate (BER) in the receiver. There are two main types of spread-spectrum transmission, direct-sequence (DS) and frequency-hopping (FH). Other forms of spread-spectrum, such as time-hopping (TH), CHIRP radar and hybrids also exist. Only frequency-hopping will be covered in this document, as it is a form of frequency modulation.

The advantages obtained through the use of spread-spectrum transmission are low probability of intercept, anti-jamming, interference suppression/avoidance, resistance to multipath fading, and the possibility of using code-division multiple access (CDMA). In CDMA every transceiver in the system is assigned a unique spreading code. Provided that the codes used by different users have sufficiently low partial cross-correlation properties, several users can transmit in the same bandwidth without significantly interfering with one another. CDMA techniques can be used in both direct-sequence and frequency-hopping type spread-spectrum systems.

In frequency-hopping spread-spectrum systems, the carrier is moved around in frequency following a pseudo-random path unrelated to the transmitted data. Instantaneously, an FH signal is narrowband and, therefore, once the carrier is despread, a standard FM receiver can be used to recover the transmitted data. The transmission advantage in FH is obtained through interference avoidance rather than energy spreading as in direct-sequence. The hopping rate is unrelated to the spreading bandwidth and entire frequency bands can be avoided while hopping (i.e., hopping frequencies need not be contiguous).

Frequency-hopping can be classified as either fast or slow frequency-hopping. This classification is unrelated to the absolute hopping rate. Instead, the classification depends on the ratio of the hopping rate to the data rate in the system. If the ratio is less than one, this is known as slow frequency-hopping (SFH) (i.e., more than one data symbol is transmitted per hop interval). If the ratio is greater than or equal to one, this is called fast frequency-hopping (FFH) and there is more than one frequency hop taken per symbol period.

In slow frequency-hopping, additional error correction coding is required in order to introduce redundancy into the transmitted data. The coding is required because, as more than one data symbol is transmitted during a single hop period, if a degradation exists at a particular hop frequency several data bits will be lost. This is known as a burst error. Slow frequency-hopping provides some frequency diversity and resistance to multi-path fading. Usually in SFH the absolute hopping rate is lower than that of an equivalent FFH system since the data rate are similar. This simplifies the synthesizer design and the synchronization requirements for the system.

In fast frequency hopping, frequency diversity is inherent, and additional error correction coding is not required but often used. This is due to the fact that the carrier is hopped more than one time per data symbol period, resulting in redundant data transmission at different frequencies. If the sizes of the hops taken are larger than the coherence bandwidth of the channel [Pro83] the data will undergo statistically independent channel effects at each frequency. In this way, frequency diversity is achieved, as long as some form of diversity combining algorithm is implemented in the receiver. The diversity gain in FFH, a figure of merit for systems which make use of diversity, is defined as the ratio of the hopping-rate to the data rate.

In frequency-hopping spread-spectrum, synchronization between the transmitter and receiver need only be performed at the hopping rate. Since the hopping rate is not related to the spreading bandwidth, synchronization requirements in a FH system are generally less stringent than those required for a direct-sequence system with an identical spreading bandwidth [Pro83].

Frequency-hopping is a specific case of FM modulation of a carrier. Frequency-hopping systems that make use of PLL based frequency synthesis suffer from spectral splatter and IF frequency error in the receiver due to incomplete despread of the hopping, caused by transient mismatch between the transmitter and receiver synthesizers. It has been shown, in a recent Masters thesis [Fil94], that spectral-splatter and IF frequency error due to transient mismatch can be greatly reduced by attenuating the high frequency content of the hopping code through the use of a digital interpolation filter. The use of such a filter results in a carrier that moves continuously and smoothly in frequency, a reduction in spectral splatter, and a lower bit-error rate in the receiver [FPRC95]. It is also believed, since the carrier is continuously moving in frequency and valid data is available to the receiver at all times, that integrating over the entire symbol period before making a symbol decision in the receiver provides inherent diversity combining, improving system performance in a multi-path fading environment.

The above is one example that shows that through careful spectral shaping of a carrier or data using digital filtering, a large number of waveforms can be generated. These waveforms can provide the carrier with similar advantages to frequency-hopping but with more versatility. Examples of such carrier modulation methods are broad-band coded FM [Ken94], and interpolated frequency-hopping [FPRC95], [RFCP98], [Fil94]. In order to generate these types of modulation an agile frequency synthesizer is required. Recent advances in frequency-synthesis and digital filtering have now made VLSI implementations of such systems feasible and economical [RCK93], [RiCo94], [Bax95], [FRC97].

2.5 Spectral Shaping of Data Through Interpolative Coding

It is well known that baseband pulse-shaping of data is required in order to control the spectral content of a transmitted signal and to reduce adjacent channel interference [MuHi81]. This pulse shaping is captured by the $b(t)$ function shown in Equation (2-20). If data is transmitted using rectangular baseband pulse shaping, the resulting spectrum will be wideband in nature, due to the phase and frequency discontinuities present.

The Fourier transform of a rectangular pulse takes the form of a sinc function ($\sin(x)/x$), whose power spectrum is shown in Figure 2-5. It can be seen that high sidelobe energy is present. This leads to inefficient bandwidth utilization due to the wide channel spacing required in order to minimize adjacent channel interference.

Figure 2-5: Frequency Spectrum for Rectangular Pulse Shaping

Continuous phase modulation smoothens the phase changes of the transmitted data through the use of pulse-shaping. This results in lower sidelobe energy, a narrower transmitted spectrum, and ultimately, a reduction in the bit-error rate (BER) of the radio receiver [Sun86].

The properties of the transmitted data spectrum depend on the type of baseband pulse employed (i.e., the impulse response of the data filter) and the duration of the pulse with respect to the data symbol period. If the duration of the pulse is equal to one period of the data symbol this is called full response signalling. If the pulse duration is longer than one data symbol period this is called partial response signalling. This document only deals with partial response signalling.

Two commonly used pulse shapes for baseband pulse shaping are the Gaussian pulse and the raised cosine pulse. Theoretically, a Gaussian pulse is infinite in duration. However, the energy in the ‘tails’ of the pulse is very close to zero and truncation results in only a small error. For the Gaussian pulse, the parameter BT is the ratio of the 3-dB bandwidth of the Gaussian lowpass filter to the data rate. The parameters for the raised cosine pulse are the roll-off factor, B_r , and the 3-dB bandwidth. The roll-off factor determines how quickly the pulse decays to zero. Figure 2-6 shows the baseband pulse shapes and the time domain equations for a Gaussian pulse and a raised cosine pulse, as well as their respective frequency spectra.

In partial response signalling, memory, and hence inter-symbol interference (ISI), is deliberately introduced into the transmitted data by ensuring that the baseband pulse duration is longer than one data symbol period. Essentially, this means that the output of the baseband pulse shaping filter depends on the value of the present data symbol being transmitted as well as the values of past and future data symbols. Figure 2-7 shows an example of this for a truncated Gaussian pulse which spans three data symbol periods.

Gaussian Pulse

$$p(t) = \frac{1}{2T} \left[Q \left(2\pi B_b \frac{t - \frac{T}{2}}{\sqrt{\ln(2)}} \right) - Q \left(2\pi B_b \frac{t + \frac{T}{2}}{\sqrt{\ln(2)}} \right) \right]$$

$$0 < B_b T < \text{infinity}$$

$$Q(t) = \int_t^{\infty} \frac{1}{\sqrt{2\pi}} e^{-\frac{\tau^2}{2}} d\tau$$

Raised Cosine Pulse

$$p_r(t) = \frac{(\cos 2\pi B_r t) \left(\frac{\sin \pi r_b t}{\pi r_b t} \right)}{1 - (4B_r t)^2}$$

Figure 2-6: Gaussian Pulse and Raised Cosine Pulse

Figure 2-7: Partial Response Signalling

Pulse-shaping techniques can be extended in order to shape the carrier frequency deviations in frequency-hopping spread-spectrum, as demonstrated in [Fil94] and [FPRC95] as well as the data modulation.

2.6 Frequency Synthesis

Frequency synthesizers for use in mobile radio applications must be well suited for VLSI implementation and have low power consumption. In addition to providing a fixed local oscillator (LO) in a receiver, a frequency synthesizer may be called on to be agile in its frequency control, for instance, in spread-spectrum applications. Synthesizers used in such applications must have fast settling times and good spurious performance. In order to generate a wide variety of FM wave-

forms, high resolution and direct modulation capability are also assets.

It has been shown that $\Sigma\Delta$ controlled fractional-N frequency synthesis is one synthesis technique that can meet all of these requirements [RCK93], [MiCo90], [PTS97]. While other phase-locked loop synthesizers can meet some of the requirements, fractional division is required in order to meet all of them. $\Sigma\Delta$ control is capable of achieving this fractional division with lower spurious content than competitors such as “digi-phase” [Gil69] and is the technique focused on in the remainder of this thesis. Unlike direct digital synthesis (DDS), no upconversion is required and the modulated signal can be synthesized directly at the RF frequency with comparable performance. The high resolution achieved allows accurate constant amplitude modulation of the carrier at RF frequencies. The interested reader can find more background information on various frequency synthesis techniques and their properties in [Raz97]. A $\Sigma\Delta$ controlled fractional-N frequency synthesizer is shown in Figure 2-8. The synthesizer operates as follows.

The desired output frequency is fed into a digital $\Sigma\Delta$ modulator as a digital word. The resulting output bitstream is used to control the dual-modulus divider in the PLL. The average value of the bitstream is the division ratio required to synthesize the desired output frequency. The noise shaping and oversampling of the modulator push the quantization noise to higher frequencies. This high frequency noise is then filtered out by the PLL.

To understand the operation of the dual-modulus divider in Figure 2-8, when controlled by a $\Sigma\Delta$ modulator, consider a phase-locked loop with a fixed divide by N in the feedback loop. We could postulate a digital-to-phase converter (DPC) which would allow a fixed amount of phase to be added or subtracted from the divider output every reference cycle, providing digital control of the output frequency. The amount of phase added or subtracted would depend on the digital input to the DPC. The output of this DPC could be seen to quantize phase in the same way that a digital-to-analog (DAC) converter quantizes voltage. The resolution achieved would depend on the number of phase quantization levels and their linearity. Building an accurate multi-bit phase quantizer is a difficult design problem which will be addressed in Chapter 4. However, single-bit phase

Figure 2-8: $\Delta\Sigma$ Fractional-N Frequency Synthesizer

quantizers are readily available in the form of dual-modulus dividers. The input to the divider can be seen as a single control bit which allows 0 or 2π radians of phase (0 or 1 period of the VCO in Figure 2-8) to be subtracted once every reference cycle from the input signal. This subtraction is followed by a fixed divide by N . This divider model is shown in Figure 2-9 (A more complete divider model is presented in Chapter 4). Using oversampling and noise shaping techniques high resolution can be achieved using this single bit phase quantizer in the same way that high resolution is obtained from single-bit voltage quantizers [CT91],[ASV96]. Thus, the large knowledge base available on the design of $\Sigma\Delta$ modulators is also applicable to the design of high resolution frequency synthesizers.

Figure 2-9: Divider Model

2.7 Oversampled Data Conversion Techniques

It is important to present some background material on oversampled data conversion techniques in order to understand the equivalent architectures presented in this thesis which operate on phase and frequency variables.

Two common data conversion techniques are analog-to-digital conversion (ADC) and digital-to-analog conversion (DAC). In an ADC an analog value (voltage, phase, frequency, etc.,) is converted into a digital value which is discrete in both amplitude and time. In a DAC digital samples are converted back into analog values.

Typically, the staircase view of data conversion, where analog values are converted to discrete digital values, as shown in Figure 2-10, is the commonest and the easiest to understand. Architectures such as successive approximation and flash ADCs [Hau91] etc., are implementations of this transfer characteristic.

The performance of any data converter is best described using the signal-to-noise ratio (SNR) of the converter. In order to relate this to the resolution of the familiar staircase type of converter, where the number of bits is clearly defined (ideally), the SNR can be converted into an equivalent number of bits [Hau91]. The following equation relates the SNR of a general ADC to the equivalent N-bit resolution of an ideal staircase converter [Hau91].

$$SNR_{MAX}(dB) = 6.02N + 1.76 \quad (2-21)$$

Here N is the equivalent number of bits and the input signal is assumed to be a sinusoid with an amplitude close to the full-scale range of the converter. For such a “busy” input signal the noise is modeled as additive independent white noise (AIWN) with a uniform frequency distribution from DC to F_s (The sampling frequency).

Figure 2-10: Transfer Function for A Staircase Type ADC

Nyquist theory states that in order for an analog signal to be uniquely represented in digital form it must be sampled at a rate which is at least two times faster than the highest frequency component of the waveform being sampled. Figure 2-11 shows the spectrum of a sampled signal. It can be seen that the sampled data is replicated around integer multiples of the sampling frequency and that the spectrum is only unique in a bandwidth equal to one half of the sampling rate. The spec-

trum shown assumes ideal sampling which implies a series of sampling impulses in the frequency domain. This results in an infinite number of replicas at integer multiples of the sampling frequencies. In reality, ideal sampling is not possible and in practice some form of sample and hold operation must be performed. This results in a sinc/x filtering of the sampled signal.

Figure 2-11: Frequency Spectrum of a Sampled Waveform

Any signals that fall between $F_s/2$ and F_s will be replicated in the baseband of the converter after sampling. Such undesired replication is known as “aliasing”. This means that an anti-aliasing filter is required at the front end of the ADC in order to eliminate frequency components which are above half the sampling rate, thus preventing them from aliasing into the desired frequency band. This filter is analog and is one of the more difficult parts of an ADC to implement. Also, high quality continuous time filters are not well suited for VLSI implementation. Similarly, an analog reconstruction filter is required at the output of a DAC converter.

The difference between the value of a quantized sample and the actual analog signal is known as the quantization error. Assuming that the quantization error is random, the energy of the quantization noise is uniformly distributed from DC to one half of the sampling rate of the system, as shown in Figure 2-11. This is a reasonable assumption to make for “busy” inputs, but is not very accurate for DC inputs since the quantization error, in fact, depends on the input value. The random condition can be imposed on the system through the use of dithering.

If the sampling rate of a system is increased for some constant input signal (i.e., the same frequency content), the total quantization noise power remains the same but is spread over a wider bandwidth, reducing its power in the desired bandwidth. The ratio of the sampling rate of a system to the required sampling rate (dictated by Nyquist) for that system is defined as the oversampling ratio. As this ratio is increased, the power of the quantization noise is decreased in the band of interest. This leads to a higher SNR for the system (for a fixed bandwidth) and, hence, a higher effective resolution for the converter, provided the proper digital arithmetic is performed on the output bitstream. The increase in SNR gained by oversampling is equal to $10\log K$, where K is the oversampling ratio. Oversampling allows the use of less expensive anti-aliasing filters and the remaining filtering can be performed in the digital domain using a decimation filter. The decimation filter performs a lowpass filtering operation, removing the out of band quantization noise, and reduces the sampling rate to the Nyquist rate by skipping $K-1$ out of K samples from the lowpass filter. An example of a crude decimator is a digital accumulator. Every K cycles of the oversampled clock, the parallel output of the accumulator is sampled and its contents are reset to zero. More information on decimation and decimation filtering can be found in [Can86],[Hog81].

The gain achieved through the use of oversampling is not very substantial when compared to the increase in power consumption required in the system due to the higher sampling frequency. However, oversampling allows the use of noise shaping which can substantially increase the resolution of the converter. Figure 2-12 shows the block diagram of a general oversampled noise shaping data converter [Hau91], where the quantizer is modeled as a gain block followed by source of additive white noise in order to simplify the analysis of the system. In this case the quantizer gain is assumed to be one.

The transfer function, from the data input to the output of the converter, shown in Figure 2-12, is found to be,

$$\frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} \quad (2-22)$$

and the transfer function from the quantization noise input to the converter output is found to be:

Figure 2-12: General Oversampled Noise Shaping Data Converter

$$\frac{Y(z)}{Q(z)} = \frac{1}{1 + H(z)} \quad (2-23)$$

It can be seen, from Equation (2-23), that through the correct selection of transfer functions the noise can be shaped in such a way as to increase the SNR of the converter in the band of interest. If the transfer function, $H(z)$, is chosen to be a discrete time integrator, and the quantizer is single-bit, the block diagram shown in Figure 2-12 becomes that of a classic first-order $\Sigma\Delta$ modulator as shown in Figure 2-13 [Hau91]. A single bit quantizer is useful in that it is highly linear and does not suffer from mismatch between quantization levels, since only two levels are available. However, defining the quantizer gain accurately is extremely difficult, making stability analysis using the linear model difficult. Statistical definitions of quantizer gain do exist [PBSA87].

Figure 2-13: First-Order $\Sigma\Delta$ Modulator

The first-order $\Sigma\Delta$ modulator shown in Figure 2-13 works as follows. The input voltage is fed into the summing block shown and the output value of the modulator is subtracted from it after being passed through a one bit DAC. The result of the subtraction is a measure of the quantization error of the previous sample, which is then integrated and passed to the quantizer which converts it to a one or a zero. Feedback in the loop works to pull the average quantization error to zero. However, the instantaneous error can be very large. If a low value is applied to the modulator input the output bits will be mostly zeros, and if a high value is entered the output bits will be mostly ones. If the input is at a value equal to one half the input range, an equal number of ones and zeros will be produced by the modulator. Therefore, the output of the modulator is a bitstream whose average value is proportional to the value applied at the input. The transfer function, from the input of the modulator to the output of the modulator, is;

$$\frac{Y(z)}{X(z)} = z^{-1} \quad (2-24)$$

The transfer function from the quantization noise input to the output is;

$$\frac{Y(z)}{Q(z)} = 1 - z^{-1} \quad (2-25)$$

Therefore, the total output of the converter is;

$$Y(z) = X(z)z^{-1} + Q(z)(1 - z^{-1}) \quad (2-26)$$

The desired signal appears at the output of the converter delayed by a single clock cycle and the quantization noise is shaped by a discrete time implementation of a first-order highpass function. This greatly reduces the quantization noise in the desired band, improving the SNR of the converter at low frequencies.

The attractive feature of the $\Sigma\Delta$ architecture shown in Figure 2-13 is that it can easily be implemented on chip and its performance has little sensitivity to circuit component tolerances.

In practice, a multi-bit quantizer can be used in a $\Sigma\Delta$ modulator, however, a one-bit quantizer is easily implemented using a simple comparator and does not suffer from the non-linearities and slope matching issues present in multi-bit quantizers. Although these non-linearities are not an

issue for the output quantizer, since they are shaped by the same transfer function as the quantization error, they are an issue in the feedback DAC where their effect is passed directly to the output, delayed by one clock cycle.

Recently, multi-bit $\Sigma\Delta$ modulators have gained attention since DSP has progressed enough to allow economical adaptive cancellation of DAC non-linearities [CST97]. Also, several DAC element “shuffling” algorithms have been developed which can “whiten” or shape the errors created by element mismatch. Eventually, the author believes that these architectures will dominate the market since multibit quantizers result in increased modulator stability and reduced levels of quantization noise.

The additive white noise model for the quantizer does not predict the presence of limit cycle tones in $\Sigma\Delta$ modulators which occur due to the dependence of the quantization error on the value of the input signal [CT91]. These tones disappear quickly with increasing modulator order, and can be reduced in lower order modulators through the use of dithering. For first order $\Sigma\Delta$ modulators the limit cycle problems are so acute that they are rarely used in practice [CT91].

The order of the modulator can be increased in order to increase the resolution of the converter. One way to do this is to increase the number of cascaded integrators in the loop. This is shown, for example, in Figure 2-14 for a second-order modulator.

For higher orders, $\Sigma\Delta$ modulators can become unstable due to excess phase shift. The stability of these systems is difficult to analyze in closed form since the single-bit quantizer present in the loop is highly non-linear. It is almost impossible to exactly determine the quantizer gain for linear modeling purposes. Usually, these systems are analyzed through step by step simulation of the time domain difference equations. An alternative to this approach is to use a MASH architecture [UHKI88].

Figure 2-14: Second-Order $\Sigma\Delta$ Modulator

A MASH architecture $\Sigma\Delta$ modulator is shown in Figure 2-15. In this case it consists of a cascade of first order $\Sigma\Delta$ modulators. It is important to note that it is possible to use various different cascades in a MASH architecture, for a example a MASH1-2 (first-order stage followed by second order stage).

The quantization error of each stage is fed forward to the next stage, whose output bitstream is a $\Sigma\Delta$ quantized estimate of the error from the previous stage. The outputs are then combined in a noise shaping block which cancels the noise from the first $n-1$ stages, producing a multi-bit output which has n th-order noise shaping given as;

$$N(z) = (1 - z^{-1})^n \quad (2-27)$$

Where n is an integer with values: $n=1, n=2, n=3...$ etc. The advantage of this modulator architecture is that it is unconditionally stable, since no n th-order feedback is present and the first-order stages have been proven to be stable [UHKI88]. The main disadvantage is that the output is n bits wide, making a multi-bit decimator necessary in data converter applications and a multi-modulus divider necessary in PLL applications.

Analog implementations of MASH architectures suffer from gain mismatches between stages which result in incomplete cancellation of the quantization noise generated in the first $n-1$ stages.

Figure 2-15: MASH Architecture $\Sigma\Delta$ Modulator

Digital implementations of MASH architectures do not suffer from these mismatches. Thus, digital MASH architectures are capable of achieving complete cancellation of the quantization noise produced in the first $n-1$ stages of the modulator. Therefore, MASH architectures are more suited for DACs, which are mostly digital, rather than ADCs which are mostly analog in design. Recently methods for compensation of mismatch in analog MASH architectures have been introduced [Cau98]. These methods make use of adaptive filtering techniques to compensate for these mismatches.

Finally, it is important to be aware that while there is no theoretical advantage to using oversampling techniques as opposed to Nyquist rate techniques, there are several practical reasons [Hau91]. For example, analog anti-aliasing filters are much more difficult to implement than digital filters. Oversampling allows the use of only a crude analog anti-aliasing filter and the rest of the filtering can be performed digitally. Also, the ability to use a single bit quantizer avoids the problems of the differential and integral non-linearities present in multi-bit quantizers.

2.8 Measuring Instantaneous Frequency

In the receiver section of the system presented in Figure 2-1 some method of extracting the frequency modulation superimposed on the IF signal is required.

Frequency discrimination is the process of extracting a modulating signal from a FM carrier in a receiver. A frequency discriminator produces an output voltage which is proportional to the instantaneous frequency deviations of a carrier and has a characteristic sensitivity, K , which has units of V/Hz. Mathematically, frequency discrimination is performed by taking the derivative of the expression which represents the modulated carrier and then extracting the required information which has been converted to amplitude deviations. The derivative of the FM modulated carrier in Equation (2-3) is;

$$\frac{ds}{dt} = A[2\pi f_c + s(t)] \sin \left(2\pi f_c t + \int_0^t s(\tau) d\tau \right) \quad (2-28)$$

The ideal transfer function of a differentiator is shown in Figure 2-16. It can be seen that the act of differentiation converts frequency deviations to amplitude deviations.

The differentiated signal can then be passed through an envelope detector in order to recover the modulating signal, as the carrier is now amplitude modulated by an amount proportional to the instantaneous frequency of the signal. One example of a discriminator is a bandpass filter. The transfer function of a bandpass filter is shown in Figure 2-17. It can be seen that, at the edges of the bandpass characteristic, the filter has amplitude variations at its output which are caused by

Figure 2-16: Transfer Function of An Ideal Differentiator

frequency variations at its input. Provided the frequency deviations are small enough for the filter to be operated on the linear portion of the roll-off curve, it can be used as a frequency discriminator. Several variations of this type of discriminator exist [Stre77].

Figure 2-17: Bandpass Filter as Frequency Discriminator

Another type of frequency discriminator is shown in Figure 2-18.

Figure 2-18: Phase-Shift Frequency Discriminator

This is known as a phase shift frequency discriminator. Effectively, this circuit approximates a differentiator. One way to achieve the desired phase shift (time shift) shown in Figure 2-18 is to use an LC tank circuit tuned to the RF/IF centre frequency.

A phase-locked loop (PLL) can also be used as an FM demodulator. In a PLL, such as that shown in Figure 2-19, the output of a voltage controlled oscillator (VCO) is phase/frequency locked to a carrier or IF frequency. Feedback around the loop works to keep the error at the output of the phase detector close to zero. In steady state, $f_{out}(t) \approx f_{in}(t)$. If the carrier or IF signal is FM modulated by a signal that falls within the loop bandwidth, then the output frequency of the VCO must be modulated as well in order to keep the phase error close to zero. This means that the control signal applied to the VCO tuning port consists of a DC term, representing the fixed carrier frequency, and a time varying component, $m(t)$, which is proportional to the original modulating signal. The FM demodulation output is shown in Figure 2-19.

More recently, $\Sigma\Delta$ modulation techniques, described in the previous section, have been applied to the task of frequency discrimination [BeCo94], [Bax95], [Gal95], [HOLT95]. The output of such a discriminator is an oversampled bitstream whose average value is proportional to the instantaneous frequency of the input. This approach allows conversion to the digital domain at high centre

Figure 2-19: PLL Based Frequency Discriminator

frequencies, reducing analog complexity, a favorable approach in modern communication systems. Such discriminators can be used as components in frequency synthesizers or as receive path frequency-to-digital converters, as in the system shown in Figure 2-1. These architectures are now described.

2.8.1 $\Sigma\Delta$ Frequency-to-Digital Conversion

Figure 2-20 shows a block diagram to illustrate the principle of operation of a first-order $\Sigma\Delta$ frequency-to-digital converter. This structure has been called a frequency discriminator in the past [BeCo94], however, it is more generally a PLL also, since unlike most frequency discriminators, it is phase coherent and the input phase can be recovered by integrating the output bitstream [RFCP98]. In this thesis it will be called a $\Sigma\Delta$ frequency-to-digital converter (FDC).

The circuit shown in Figure 2-20 operates in the following manner. The input signal is a carrier whose frequency lies between NF_{ref} and $(N+1)F_{ref}$. The output of the dual-modulus divider shown is phase compared to a fixed reference frequency, F_{ref} , using a D-type flip-flop. If the edge of the divider output leads the reference edge a one is sampled by the flip-flop. Similarly, if the reference edge is leading the divider edge, a zero is sampled by the flip-flop. The output bits of the

Figure 2-20: A First-Order $\Sigma\Delta$ FDC

flip-flop are used as feedback to control the division ratio of the divider. In order to have negative feedback, for stable operation, a one should cause the divider to divide by $N+1$ and a zero should cause the divider to divide by N . Thus, if the divider edge is leading the reference edge, the one sampled will cause the divider to divide by the higher value delaying the output on subsequent cycles. Similarly, if the divider edge is lagging the reference edge, the divider will divide by the lower value, pulling the divider edge back ahead of the reference edge on subsequent cycles. The divider output phase is the continuous time integral of the input frequency minus the sum of all of the control bits ever fed back to the divider. This leads to the divider model that was shown in Figure 2-9 which will be derived more formally in Chapter 4.

If the input signal is FM modulated by a waveform which has a frequency much lower than that of the carrier (this is almost always the case) the output bits from the flip-flop will have an average value proportional to the instantaneous frequency deviations of the carrier. If the divider is replaced by the mathematical model given in Figure 2-9, a block diagram similar to the one shown in Figure 2-13 is obtained.

Recognizing that the D Flip-Flop shown is a single-bit phase quantizer, it can be seen that the circuit shown in Figure 2-20 is a first-order $\Sigma\Delta$ modulator on instantaneous frequency. The divider can be considered as being the modulator front-end (MFE) [Ril97], that is, the circuit which allows instantaneous frequency to be the modulator input, rather than voltage. Other possible

MFEs have been proposed in the literature including one that is based on a voltage controlled oscillator [Gal94]. However, the voltage controlled oscillator results in a VLSI implementation that is more complex than the one for a digital divider.

The next chapter presents the design and testing of a $\Sigma\Delta$ controlled fractional-N frequency synthesizer which would be suitable for use in the system of Figure 2-1, after which we return to the design of a $\Sigma\Delta$ frequency-to-digital converter as discussed in this section.

Chapter 3 A Fractional-N Frequency Synthesizer with Built in GMSK Data Modulation

3.1 Introduction

This chapter presents the design of the $\Sigma\Delta$ controlled fractional-N frequency synthesizer. The contributions specifically made by the author in this area are the following;

- 1) A digital CMOS chip was designed and built which incorporates a MASH architecture fourth-order $\Sigma\Delta$ modulator and a GMSK data filter which makes use of $\Sigma\Delta$ quantized tap coefficients. This is the first time that such a modulator has been combined with such a synthesizer at the IC level.
- 2) An ISM band frequency synthesizer was designed and tested which makes use of the above modulator chip, along with a bipolar chip which incorporates a multi-modulus divider, phase/frequency detector, and output charge pump. The bipolar chip was designed and laid out by Tom Riley. This forms a complete transmit path excluding the baseband DSP and power amplifier (PA).

Before presenting the synthesizer design in detail a brief tutorial on low power ECL/CML design will be presented.

3.2 Low Power ECL/CML Logic Design

We now turn our attention to the circuitry used in the multi-modulus divider. Such circuitry must be capable of operating, at its input, at the VCO frequency. Emitter-coupled bipolar logic can operate at very high frequency and is the fastest of all the logic families. The high speed operation is due to the fact that ECL uses non-saturating logic. That is, the transistors only operate in the

active and cut-off regions. Other families of logic, such as transistor-transistor logic (TTL), saturate the bipolar devices when changing levels and, therefore, have slow rise and fall times due to charge storage in the collector base junction. Figure 3-1 shows a schematic of an ECL inverter. The differential pair is used to steer current to either half of the gate. The output logic swing is set by the value of the load resistors. The emitter followers are used to buffer the load from the collector of the current steering transistors.

Figure 3-1: ECL Inverter

In the past, ECL was less popular because of its inherently high power consumption. Unlike CMOS logic, which only consumes power while switching, ECL gates have high static power consumption. As high frequency applications become more important, the high speed of ECL logic is needed and CMOS has less advantage. This is because CMOS power consumption increases with frequency and there comes a point where CMOS circuits can actually consume more power, for the same functions, than their ECL counterparts.

As VLSI technologies have progressed it has become more and more uncertain as to whether or not the emitter followers present in ECL gates are necessary. The emitter followers were originally used for the following reasons.

- 1) The emitter followers have a low output impedance. Although they add some propagation delay to the gate, this is more than compensated for by the large decrease in the load time constant.
- 2) The emitter followers isolate the load from the gate switching time constants.
- 3) The emitter followers provide a DC level shift which helps to improve the noise immunity of the gate and also prevents the saturation of the input transistors of subsequent stages. This results in a higher V_{ce} , increasing the f_t of the device.
- 4) The emitter followers increase the power gain of the gate, allowing a larger fanout and increasing the ability to drive large off chip capacitive loads.

However, as the circuit density of ICs increases, a large amount of power is wasted on emitter followers, especially in cases where ECL gates are used to drive other identical stages and most of the processing is performed on chip. In this case, there are only a few instances in which the circuit must link with the external world and drive large capacitive loads. Forward biasing the collector base junction of the input transistors, to an extent, is no longer a serious concern since the saturation characteristics of integrated bipolar devices have improved substantially [Tre89]. CML logic is ECL logic without emitter followers. Therefore, for low voltage operation and low power consumption, CML logic should be used wherever possible.

Another factor which determines the power consumption of an ECL/CML gate is the tail current. Higher current density through the transistors reduces the transit time and hence speeds them up. By operating in a high speed process, at relatively low frequencies, the tail current can be reduced to low levels. Using a low tail current means that the load resistors must be increased in value in order to maintain signal swings. This increases the time constant formed by the collector to sub-

strate capacitance of the switching transistor and the load resistor. For low power operation, this time constant is the limiting factor for the speed of an ECL/CML gate. Therefore, careful layout techniques must be used in order to reduce interconnect capacitance. Using minimum size transistors and merged collectors will reduce the switching time constant. At the architectural level a design which minimizes the number of gates, and hence the number of tail currents, is required. It should be noted that if the load resistors become too large, thermal noise will potentially become significant and will raise the noise floor of the synthesizer.

3.3 Synthesizer Design

A block diagram of the frequency synthesizer is shown in Figure 3-2. A method has been presented whereby the tap coefficients for a GMSK pulse shaping filter can be quantized to single bit values, using a software $\Sigma\Delta$ modulator, prior to storage in a read only memory (ROM) [RiCo94] with the potential for greatly reducing the required storage space and simplifying the multiplications required to single bit operations. Such a filter is included in the synthesizer and is shown in Figure 3-2.

While the ultimate goal is to integrate the entire synthesizer onto a single BiCMOS chip, the design presented here was partitioned such that the high frequency components of the PLL are implemented in a high quality bipolar process, Nortels' NT25, and the digital sections are implemented in a high quality 0.5 μm CMOS process. This partitioning allows the best features of both technologies to be exploited while avoiding the problems that arise when mixing noisy digital circuits with sensitive analog circuits. The two custom chips were mounted on a four layer printed circuit board along with an external loop filter and a commercial VCO. This approach avoided the difficulties of integrating a VCO onto a chip along with other noisy circuits. The design of the custom CMOS chip and the custom bipolar chip is covered in subsequent sections.

The synthesizer was designed to be part of a frequency-hopping transceiver that would operate in part of the lower Instrumentation Scientific and Medical (ISM) band from 914-928 MHz, as described in Chapter 2. For testing purposes, a 20 MHz reference was used. Therefore, the chan-

Figure 3-2: Frequency Synthesizer

nel spacing was chosen to be 78.125 KHz, with a frequency settling time of less than 50 μ s. The data transmission rate is 62.5 Kb/s with GMSK pulse shaping with a BT of 0.5, giving a frequency deviation of ± 15.625 KHz. The GMSK transmitter architecture used eliminates the need for the I and Q channels, D/A converters, summers, and upconversion normally used in GMSK data transmission.

The digital data to be transmitted is input serially to the data input of the digital CMOS chip in Figure 3-2, and filtered by the GMSK data filter to be described later, to shape the transmitted frequency spectrum. The synthesizer transmit frequency is controlled via a 3-bit serial interface (the control input in Figure 3-2). This control interface reduces the number of pads required for the digital CMOS chip and allows easy microprocessor interfacing for synthesizer control.

In order to achieve low spurious content and low phase noise levels in the synthesizer, the interactions between the loop bandwidth, settling time, data-rate, reference frequency, quantization noise, and VCO phase noise were considered carefully in the design, as follows.

The settling time of a PLL can be approximated as being equal to four times the inverse of the closed loop bandwidth [Cra94]. Therefore, in order to achieve a settling time of less than 50 μ s, the loop bandwidth must be at least 80 KHz wide. Also, since the loop used in the synthesizer is being directly modulated with data, the bandwidth must be at least as wide as the modulation rate in order to avoid unwanted filtering of the transmitted data. The loop bandwidth was chosen to be 100 KHz. This is wide enough to achieve fast settling times and accommodate the transmitted data. If faster settling times were needed the PLL could be modified such that the loop bandwidth could be increased temporarily during frequency changes [Bro96].

The PLL (bipolar chip) suppresses quantization noise from the digital CMOS chip outside of its loop bandwidth. Inside the PLL loop bandwidth, the quantization noise suppression is achieved by the noise shaping properties of the digital $\Sigma\Delta$ modulator. Therefore, the modulator oversampling ratio and order both have a great influence on the noise performance of the synthesizer. Not only is the frequency reference (F_{ref} in Figure 3-2) used to lock the PLL, it serves as the clock for the $\Sigma\Delta$ modulator and the oversampled data filter. This means that the reference frequency sets the oversampling ratio of both the data filter and the $\Sigma\Delta$ modulator. It is important to note that as the reference frequency is increased the power consumption of the CMOS chip also increases. Also, phase noise generated in the phase detector is multiplied by the division ratio of the loop before appearing at the VCO output. Therefore, a higher reference leads to lower division ratios (for a given transmission band) and lower phase noise levels at the synthesizer output. The trade-off for additional bandwidth improvement is increased power consumption. Similarly, higher order modulators used to reduce in-band phase noise and increase the bandwidth of the noise shaping require more circuitry, also increasing power consumption.

Inside the loop bandwidth the dominant sources of phase noise are the reference frequency, divider, and phase detector. Outside of the loop bandwidth the dominant sources of phase noise are the filtered $\Sigma\Delta$ quantization noise, filtered divider phase noise, and unfiltered VCO phase noise. Therefore, the loop filter must be designed in such a way as to achieve low inband and out of band phase noise levels. The loop filter used in this design consists of an integrator with phase lead correction forming a second order PLL. Two additional real poles were added to the loop in order to reduce reference feedthrough and out of band quantization noise. These poles were placed such that they would not affect loop stability. The reference frequency was chosen to be 20 MHz, and the digital $\Sigma\Delta$ modulator order four.

The multi-modulus divider makes it simple to add an integer offset (a DC component of the digital control input) to the modulator output, allowing different fractional bands to be selected for data transmission. In this case the bands are 20 MHz wide. For widely spaced bands the loop filter must be modified in order to take into account the change in loop gain brought about by the change in division ratio that is required. A different VCO might be required as well. The loop presented in this thesis was designed such that it would be usable over the entire band from 914-928 MHz without any modifications.

3.4 Phase-Locked Loop Model and Theoretical Phase Noise Analysis

The theoretical phase domain model for the PLL used in the synthesizer is shown in Figure 3-3. Assuming that any digital activity within the loop occurs at a rate equal to at least 10 times the loop bandwidth [Cra94] this continuous time model can be used. This model was used for the initial design of the loop filter, however, some adjustments were made to the final design in the laboratory.

The open loop transfer function, from the phase detector input to the divider output, for the model shown in Figure 3-3 is;

$$H_{OL}(s) = \frac{K_{PD}K_{VCO}}{sN}Z(s) \quad (3-1)$$

Figure 3-3: Phase-Locked Loop Model

Where K_{PD} is the phase detector constant (A/rads), K_{VCO} is the VCO tuning constant (Mrads/V) and $Z(s)$ is the loop filter impedance. It is important to note that, for this synthesizer, since the loop filter consists of a charge pump driving a series capacitor and resistor the phase detector gain has units of amps per volt.

The closed loop transfer function, from the phase detector input to the VCO output, is;

$$H_{CL}(s) = \frac{\frac{K_{PD}K_{VCO}}{s}Z(s)}{1 + \frac{K_{PD}K_{VCO}}{Ns}Z(s)} \quad (3-2)$$

Where N is the average division ratio of the digital frequency divider. For an integrator with phase lead correction the loop filter has the following impedance;

$$Z(s) = \frac{1 + RCs}{Cs} \quad (3-3)$$

This leads to the closed loop transfer function given below.

$$H_{CL}(s) = \frac{K_{VCO}K_{PD}Rs + \frac{K_{VCO}K_{PD}}{C}}{s^2 + \frac{K_{VCO}K_{PD}Rs}{N} + \frac{K_{VCO}K_{PD}}{NC}} \quad (3-4)$$

This can be related to the following normalized transfer function for a second order control system given as;

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (3-5)$$

Where ω_n is the natural frequency of the loop and ζ is the damping factor [Bla76]. The natural frequency, ω_n , is defined as;

$$\omega_n = \sqrt{\frac{K_{VCO}K_{PD}}{CN}} \quad (3-6)$$

The damping factor is defined as;

$$\zeta = \frac{R}{2} \sqrt{\frac{K_{VCO}K_{PD}C}{N}} \quad (3-7)$$

For the synthesizer $K_{VCO} = 2\pi(13)$ Mrads/V and $K_{PD} = (400\mu A/2\pi)$. Figure 3-4 shows plots of the open loop magnitude and phase, along with the closed loop magnitude and phase, for an ω_n of $2\pi(75)$ KHz, an average N of 45.5, and a ζ of 0.7. It can be seen that, at the unity gain bandwidth of the open loop response, the phase margin is 60 degrees indicating good stability. The required values for R and C were determined from the above equations. This is an idealized analysis and there are parasitic poles present which lead to some degradation of the phase margin.

3.4.1 Noise Sources

The different phase noise sources in the loop are shown with dashed lines in Figure 3-3 and their respective power spectral densities are denoted as ϵ_i . The phase noise sources shown are the reference input, the phase detector, the VCO, the divider and the $\Sigma\Delta$ modulator.

Figure 3-4: Bode Plots of Open Loop and Closed Loop Transfer Functions

Assuming that the individual noise sources listed above are uncorrelated, the output phase noise of the synthesizer is;

$$\varepsilon_{out} = \frac{\varepsilon_{VCO}}{|1 - H_{OL}(s)|^2} + \varepsilon_{PD}|B(s)|^2 + \varepsilon_{ref}|H_{cl}(s)|^2 + \varepsilon_{DIV}|H_{cl}(s)|^2 + \varepsilon_{\Sigma\Delta}|H_{cl}(s)|^2 \quad (3-8)$$

Where $B(s)$ is the transfer function from the phase detector noise input to the VCO output. In this analysis only the $\Sigma\Delta$ quantization error and VCO noise will be considered, since the reference noise is dependent on the reference source being used and the divider phase noise and phase detector noise are more difficult to predict.

The data sheets for the Z-COMM VCO provide a phase noise plot for the VCO [ZCOMM]. Data points were taken from this plot and used to build a piece-wise linear model of the VCO phase noise in MATLAB. A plot of this phase noise function is shown in Figure 3-5.

Figure 3-5: Z-COMM VCO (Estimated Phase Noise)

The next noise source to be considered is the digital $\Sigma\Delta$ modulator ($\varepsilon_{\Sigma\Delta}$ in Figure 3-3). The analysis that follows is basically the one from [MiCo90] and is presented here for completeness. We know that the output frequency of the synthesizer shown in Figure 3-3 is equal to $f_{out}=f_{ref}N$. If we replace N with the actual output from the digital $\Sigma\Delta$ modulator we get;

$$f_{out}(z) = X(z)f_{ref} + Q(z)(1 - z^{-1})^n f_{ref} \quad (3-9)$$

Where f_{out} is the output frequency of the synthesizer, X is the desired fractional division ratio, $Q(z)$ is the quantization error introduced by the $\Sigma\Delta$ modulator, and n is the order of the noise shaping filter. The power spectral density of the quantization error, using the white noise assumption, is equal to;

$$Q(z) = \frac{1}{12f_{ref}} \quad (3-10)$$

where f_{ref} is the PLL reference frequency. Therefore, the frequency error spectral density in (Hz^2/Hz) is

$$f_{error}(z) = \left(\frac{1}{12f_{ref}}\right) f_{ref}^2 |(1 - z^{-1})^n|^2 \quad (3-11)$$

To obtain the phase error spectral density a z-domain trapezoidal integration must be performed (as phase is the integral of frequency). This operation is given by;

$$S(z) = \frac{2\pi}{(1 - z^{-1})f_{ref}} \quad (3-12)$$

Therefore, the phase error spectral density, in rads^2/Hz , is;

$$\varepsilon_{\Sigma\Delta}(z) = \frac{(2\pi)^2}{12f_{ref}} |(1 - z^{-1})|^{(2n-2)} \quad (3-13)$$

This can be converted to single-sideband phase noise in the frequency domain as;

$$L(f) = \frac{(2\pi)^2}{12f_{ref}} \left| 1 - e^{\frac{-j2\pi f}{f_{ref}}} \right|^{2n-2} \quad (3-14)$$

Giving, in decibels;

$$L(f)_{dB} = 10 \log \left[\frac{(2\pi)^2}{12f_{ref}} \left| 1 - e^{\frac{-j2\pi f}{f_{ref}}} \right|^{2n-2} \right] \quad (3-15)$$

The theoretical output VCO phase noise and the $\Sigma\Delta$ phase error levels for the synthesizer, in dBc/Hz , are plotted in Figure 3-6, for a reference frequency of 20 MHz and a $\Sigma\Delta$ modulator order equal to 4. The total output phase noise due to these two sources is also given.

Figure 3-6: Theoretical Synthesizer Output Phase Noise

3.5 Digital Modulator Chip

Figure 3-7 shows a block diagram of the CMOS digital modulator chip, which was captured in the Verilog hardware description language (HDL) and implemented in a three volt 0.5 μm CMOS process using a low power standard cell library. Preliminary testing of the design was accomplished using a Xilinx field programmable gate array (FPGA). The use of Verilog allowed the modulator design to be technology independent, facilitating the move from FPGA to standard cell CMOS.

The main sections of the digital modulator chip are the GMSK data filter, the MASH-4 $\Sigma\Delta$ modulator, and the serial interface. Each of these blocks is described in greater detail in the following sections.

Figure 3-7: Block Diagram of Digital Modulator Chip

3.5.1 GMSK Data Filter

Figure 3-7 includes a block diagram for the GMSK data filter designed using techniques from [RiCo94]. Three data symbols, past, present and future, are multiplied by the filter tap coefficients and combined to produce Gaussian pulse shaping with a BT of 0.5. It is important to note that in a traditional GMSK data filter a data bit consists of a rectangular pulse which is then filtered by a Gaussian pulse. Thus, the output is a Gaussian pulse convolved with a rectangular pulse. The implementation used here directly looks up this convolved response in a ROM, at the oversampled rate with one filter coefficient for each sample. To reduce the ROM size to one bit per sample, the samples are quantized to single bit values, prior to storage in the ROM, using a third-order software $\Sigma\Delta$ modulator. The noise transfer function of the third-order $\Sigma\Delta$ modulator is [RiCo94];

$$N(z) = \frac{z^{-3} - z^{-2}\left(\frac{1535}{512}\right) + z^{-1}\left(\frac{1535}{512}\right) - 1}{z^{-3} - z^{-2}\left(\frac{1535}{512}\right) + z^{-1}\left(\frac{1535}{512}\right)} \quad (3-16)$$

The average value of the tap coefficients is equal to the desired Gaussian pulse and the short term

changes represent the highpass filtered quantization noise which is subsequently filtered out by the PLL. In this way, high resolution is obtained from single bit tap coefficients. The multipliers, shown in Figure 3-7, are now reduced to XNOR gates followed by the summing action shown. The output of the filter is fed to the MASH-4 $\Sigma\Delta$ modulator such that the total area under the Gaussian pulse results in a carrier phase shift of one quarter cycle, or $\pi/2$ radians, giving minimum shift-keying. The oversampling ratio is 320, giving 320 single bit coefficients and a data rate of 62.5 Kb/s, ($f_{ref}/320$), for a reference frequency of 20 MHz. The total memory storage space required to store the filter tap coefficients is 960 bits, significantly lower than what would be required if a standard filtering approach were used.

The GMSK filter response is plotted in Figure 3-8. Note that Figure 3-8 shows the response of the non-convolved pulse in order to facilitate comparison to other GMSK filters. The highpass filtered quantization error of the tap coefficients can clearly be seen on the plot. The stopband frequency attenuation is 38 dB. The inband characteristics of the filter are as expected for a Gaussian low-pass filter and the out of band characteristics depend on the MASH-4 $\Sigma\Delta$ noise shaping and on how well the PLL filters out the quantization error shown in Figure 3-8. The flat portion of the characteristic from 180 KHz to 900 KHz is a result of end effects, specifically, caused by the truncation of the sigma-delta quantized tap coefficients. Since the impulse response of the filter should be approximately equal to zero at this point, its value can never be properly represented by the truncated bitstream.

Since the GMSK data filter makes use of $\Sigma\Delta$ quantized tap coefficients, the synthesizer which follows the filter can have lower frequency resolution than would normally be required. This is true because the filter output is quantized to a fixed number of levels which are oversampled. This means that values between these levels can be represented by the bitstream. In this case, these levels represent instantaneous frequency values. For instance, a “0” in the bitstream could represent a frequency of 0 Hz at the output of the synthesizer and a “1” could represent a frequency of 20 KHz. Values between these levels could be synthesized, without requiring higher resolution in the synthesizer, due to the oversampling and noise shaping nature of their quantization. For example,

Figure 3-8: GSM Data Filter Response

in the above case, a resolution of 20 KHz in the synthesizer will allow filtering which would normally require higher resolution. Therefore, the filter architecture used, in addition to reducing the ROM storage space and hardware complexity required for GSM data filtering, also reduces the complexity required in the synthesizer $\Sigma\Delta$ modulator, lowering the power consumption of the control chip. The resolution required in the synthesizer in order to accommodate the GSM data filtering was found to be eight bits or 78.125 KHz for a 20 MHz clock. The final modulator has a resolution of 12-bits giving a frequency resolution of 4.882 KHz for a 20 MHz clock frequency. If a more conventional approach were used for the data filtering, and the tap coefficients were quantized to 8-bit values, the resolution required in the synthesizer would be 305 Hz. This would require an accumulator width of 16-bits in the $\Sigma\Delta$ modulator. Through the use of $\Sigma\Delta$ quantized tap coefficients the resolution required in the $\Sigma\Delta$ modulator has been reduced by a factor of 256, significantly lowering power consumption.

An extra input is included in the modulator chip which allows the GMSK modulator to be disabled when not in use. This allows improved power budgeting in the transmitter.

3.5.2 MASH-4 Digital $\Sigma\Delta$ Modulator

It can be shown [RCK93] that a digital accumulator is equivalent to a first order $\Sigma\Delta$ modulator as in Figure 2-13, where the parallel input to the accumulator is the input to the modulator and the carry output is the $\Sigma\Delta$ modulated bitstream. The parallel output of the accumulator is a measure of the quantization noise. Based on this, the fourth-order digital $\Sigma\Delta$ modulator required for the synthesizer is formed using a MASH architecture that makes use of four digital accumulators.

Although the accumulators allow a simple implementation of the fourth-order $\Sigma\Delta$ modulator, they are still responsible for a large portion of the power consumption of the modulator chip. In order to achieve the lowest power consumption possible the number of bits in the accumulator must be minimized. The use of $\Sigma\Delta$ quantized tap coefficients, as explained in the previous section, allows this.

One way to prevent limit cycles from occurring in the modulator, due to certain non-time varying inputs, is to “plant a seed” in the accumulator each time the circuit is reset. This is done by toggling the least significant bit in the first accumulator on for one reference cycle and then turning it off. For “busy” inputs this step is not required but is included in order to ensure proper operation of the synthesizer for all inputs.

The output of the $\Sigma\Delta$ modulator is four bits wide, making it necessary to have a minimum of sixteen available modulae in the multi-modulus divider. In order to make the design more versatile the division ratios available in the divider were set to fifty-five. In this way the synthesizer can be used with different VCOs and reference frequencies. An adder is included after the $\Sigma\Delta$ modulator, allowing an integer offset to be added to the output bits, selecting different fractional bands for data transmission. A translation circuit is included to convert the output to the format required by the divider control input. This consists of a hardwired lookup table.

3.5.3 Serial Interface and Frequency Control

The desired division ratio is controlled via a 3-bit serial interface, with an 11-bit control word. A timing diagram for the interface is shown in Figure 3-9. The slow clock (SCLK) is used to clock data into the input shift register. The data is clocked in when the load enable pin (LENABLE) is pulled low. The control word consists of a 10-bit data section and a 1-bit address. If the address bit is high, the data is treated as a fractional offset. If the address bit is low, the data is treated as an integer offset. The fractional division values allowed range from 0-1 with a resolution of $1/256$. The allowed integer values range from 16-64. The synthesizer output frequency is equal to $NF_{ref} + n(F_{ref}/256)$; where N is the 10-bit integer value and n is the 10-bit fractional value.

Also included in the design is a transmit offset pin which allows an offset to be added to the output frequency by toggling a single-bit on or off. This allows for the two separate transmit and receive bands described for the target system of Chapter 2. The offset is equal to $(1712/4096)F_{ref}$.

Figure 3-9: Serial Interface Timing Diagram

3.6 Bipolar Synthesizer Chip

A block diagram of the bipolar chip designed by Tom Riley is shown in Figure 3-10. The chip consists of a multi-modulus divider and a phase/frequency detector with an output charge pump.

The divider is capable of dividing by any integer value between nine and sixty-four. CML logic is used wherever possible in the design and the tail currents were set to the lowest value possible

Figure 3-10: Block Diagram of Bipolar Chip

while maintaining functionality. Although the lower current leads to increased phase noise in the divider and hence an increase in the synthesizer noise floor, it was felt that the reduction in power consumption was worthwhile for this application. The inband noise floor achieved in the synthesizer chip was between -90 dBc/Hz and -95 dBc/Hz. A more stringent phase noise floor specification would require higher power in the bipolar chip.

3.6.1 Multi-Modulus Divider

Looking at the multi-modulus divider part of the block diagram shown in Figure 3-10 inside the dashed lines, the first section is a dual-modulus divider (DMD), which divides by three or four depending on the polarity of the control line from the A counter. When the A counter output is high, the DMD divides by three, and when the A counter output is low the DMD divides by four. The A counter is reloaded each time the M counter reaches its terminal count. The A counter then counts down to zero, meanwhile outputting a one. When the count has reached zero, the counter remains at zero until reloaded, and puts out a zero. For example, if the A counter is loaded with three, it will count down to zero, while putting out three ones to the DMD, and stay there. This will produce three 'short' DMD cycles, which are three VCO cycles long as opposed to four cycles long. If a zero is loaded then no 'short' cycles are produced. In this way, the number of 'short' cycles is controlled by the A counter.

The M counter determines the number of DMD cycles that occur before both counters reload. Therefore, between every reload there are $M+1$ DMD cycles, A of which are 'short'. The number of VCO cycles between reloads is four times the number of 'long' cycles plus three times the number of 'short' cycles. That is; $N = 4((M + 1) - A) + 3A$. This simplifies to; $N = 4(M + 1) - A$.

In this design, the M counter is four bits wide and the A counter is two bits wide. This makes the range of available division ratios nine to sixty-four.

3.6.2 Dual-Modulus Divider

The first block of the multi-modulus divider architecture shown in Figure 3-10 is a divide-by-three divide-by-four dual-modulus divider. A logic diagram of this DMD is shown in Figure 3-11. In order to accommodate the use of low voltage swings the AND gates shown in the diagram are fully differential (Use of DeMorgan's laws in fully differential ECL/CML makes it possible to implement the AND function with NOR gates).

Figure 3-11: Dual-Modulus Divider

The operation of the DMD can be explained in terms of a Johnson counter. The upper four latches are enabled alternately when the clock is high or low. Thus, an input to the leftmost latch can propagate to the second latch when the clock is high. Similarly, when the clock signal is low, the

input can propagate through the second latch. Therefore, in one cycle, the input propagates through two latches, forming a master/slave D-Flip-Flop. In two clock cycles an input will propagate through all four latches. The single inversion at the input of the AND gate will prevent the circuit from finding a fixed state to stay in. Since it takes two clock cycles for a zero or a one to propagate through the latches, the circuit divides the clock by four. The fifth latch, shown at the bottom of the diagram, forms a feedforward path which allows a one to propagate back to the input of the circuit without the usual delay. This provides a divide by three mode of operation which is controlled by the input d3. When d3 is high, the lower latch is activated, making the circuit divide by three. When d3 is low, the latch is not activated, and the default mode of divide by four is dominant.

Although Figure 3-11 shows the AND gates and latches as separate components they are actually implemented together using a latched-NOR gate as shown in Figure 3-12.

3.6.3 Digital versus Semi-Analog

Although the function of the divider is simply to count up to some numerical value and then provide an output pulse, the edge timing of the output pulse is an analog quantity. Thus, a digital function can have an analog error in the timing. If these errors are larger than other sources of error such as VCO phase noise or quantization error, then the phase noise of the overall synthesizer can be limited by noisy (i.e., random) timing errors of the divider. To minimize these errors, several strategies are employed in the divider chip and are described in the following paragraphs.

The path from the off-chip VCO to the on-chip phase/frequency detector (PFD) in Figure 3-10, is fully differential. To use fully differential latched NOR gates with a 3 V supply requires setting the DMD clock at about 1.5 V_{be} drops below the positive supply. Initially, the VCO signal is converted to a differential signal with an off chip centre tapped transformer. It is anticipated that future versions at higher frequencies will incorporate this transformer on chip [LoCo95] or the VCO itself [DCS97] on chip. The M counter uses single ended logic internally, but its output is retimed (i.e., resynchronized) by the DMD output clock with a fully differential flip-flop.

Figure 3-12: CML Latched NOR

Previous work has presented techniques for time domain isolation of the divider output signal from the reference signal and also from power supply interference generated by the MASH-4 [MiCo90]. This interference is called “digital feedthrough”. The motivation for this is to force the rising edge of the divider output to occur at a different time from the rising edge of the reference output. By having the two events occur at different times, interactions between the two signals can be reduced. An older and simpler technique, which is used here, is to introduce an offset into the loop filter integrator which in turn forces a phase offset into the locked loop. This is accomplished with the loop filter shown in Figure 3-13.

Another simple technique to obtain time domain isolation is to decode the divider output in such a way that it occurs at a time when there is minimal digital activity in the divider. As illustrated in the timing diagram of Figure 3-14, the divider loads a new value of N during its terminal count of

0. By decoding state 2 as the divider output pulse, the PFD can be triggered before the divider reloads. This allows almost an entire reference cycle for any parasitic effects from divider loading to settle before the next divider output pulse is applied to the PFD.

Figure 3-14: Divider Timing

ECL/CML logic can be thought of as a series of switched current sources pulling various resistors to some voltage below the positive supply voltage. For this reason the positive supply is taken as a local common voltage in each major functional block in the chip. By arranging the layout of the cells for each functional block around a central positive supply, voltage drops through resistors along the length of the positive supply are minimized within each functional block.

By using differential signals between functional blocks, differences between the power supply voltages of the functional blocks are converted to common mode and attenuated by the common mode rejection ratio (CMRR) of the receiving block. In contrast, CMOS complementary logic would be more susceptible to power supply noise, and would generate larger current spikes on the power supplies.

Without exhaustive testing, it is difficult to isolate which of these approaches was most critical in its effects on phase noise or linearity. It is hoped that this discussion will stimulate further research and reporting on such approaches.

3.6.4 Phase Detector and Charge Pump

The phase/frequency detector (PFD) indicated in Figure 3-10 is a standard architecture similar to the Motorola 4044 or 12040. It is built in ECL rather than CML to allow easy design of a reference voltage for single ended logic gates.

The output of the PFD is open collector as shown in Figure 3-10. The operation is as follows: Normally, neither the PU nor PD signals are active and the two current sources are shunted one to each resistor in the off-chip load. If the VCO is leading, PD will be active more often and I_{dn} will have twice as much current pulled through it while I_{up} will be pulled up by the off-chip load. If the VCO is lagging the opposite is true.

3.7 Measurement Results

In this section experimental results for the CMOS modulator chip, the bipolar chip and the complete frequency synthesizer are presented.

3.7.1 CMOS Synthesizer Modulator Chip

A photo-micrograph of the CMOS modulator chip is shown in Figure 3-15. The die size is equal to 1.95 mm x 1.95 mm and the part was packaged in a 32-pin TQFP. The gate count is approximately 2000. The circuit was tested by capturing a large number of the divider control words using an HP16500C logic analysis system and processing them in MATLAB. The frequency spectrum of this bitstream for a fixed input is shown in Figure 3-16. The fourth-order high-pass noise shaping can clearly be seen from this plot.

In order to test the GMSK data filtering, a pseudo-random (PN) code generator was used to feed random data bits into the data input of the digital modulator chip. Once again, the words from the modulator chip were captured using a logic analyzer.

Figure 3-17 shows a plot of the output bits. This plot was obtained in MATLAB using the decimation function to process the $\Sigma\Delta$ bitstream. This function reduces the sampling rate and removes

Figure 3-15: CMOS Modulator Chip

the noise shaped quantization error. The data symbols shown in the plot represent the '1s' and '0s' generated by the PN code generator and filtered by the Gaussian filter in the digital modulator chip. The horizontal axis is representative of time and the vertical axis is representative of frequency deviation. However, the scales used have no particular significance. The small "dimples" that can be seen in the data bits are due to the truncation to a 1 or -1 that occurs at the end of the impulse response when it is quantized and then truncated. Because of this truncation, the ones and minus ones cannot be averaged to zero, which is the required value.

The maximum clock frequency was found to be 50.0 MHz, allowing GMSK data rates of up to 156.25 Kb/s. The power consumption, measured with the data filter and $\Sigma\Delta$ modulator active, was found to be 14 mW with a 20 MHz clock.

Figure 3-16: Output Spectrum of Digital $\Sigma\Delta$ Modulator

3.7.2 Bipolar Synthesizer Chip

A photo-micrograph of the bipolar synthesizer chip is shown in Figure 3-18. The die size is 1.61 mm x 1.58 mm and the part was packaged in a 32-pin TQFP. As was mentioned earlier, this chip was designed and laid out by Tom Riley. The bipolar chip was tested for functionality over a wide range of division ratios. The maximum frequency for an RF input was found to be 1.2 GHz. The maximum usable reference frequency was found to be 300 MHz. The chip consumes 18.1 mW from a 3 volt supply. The main speed limitation of the divider is the fact that the transistors were not biased for maximum f_t , but rather, minimum power consumption for the desired speed of operation.

3.7.3 Synthesizer

A picture of the unpopulated printed circuit board (PCB) is shown in Figure 3-19.

Figure 3-17: GMSK Data Bits

A single-sideband (SSB) phase noise plot of the synthesizer in fractional-N operation at a frequency of 915 MHz is shown in Figure 3-20. This plot was obtained using the phase-locked loop method with the HP3048A phase noise measurement system. It can be seen, from the plot, that the only spurs present in the output spectrum are the reference frequency feedthrough at -90 dBc and a harmonic of 60 Hz power line noise at -70 dBc. The power supply harmonic could be eliminated through improved shielding or by running the synthesizer from a battery. It is important to note that the inband phase noise at the synthesizer output is the same for both integer operation and fractional operation. This means that the $\Sigma\Delta$ modulator does not affect the inband phase noise characteristics of the synthesizer. By varying the DC phase offset adjustment of the synthesizer, inband noise could be increased or decreased. It was found that the inband noise was lowest when the divider edges and reference edges were separated as widely as possible in time while maintaining lock. This setting also resulted in the largest reference feedthrough. This result is consis-

Figure 3-18: Bipolar Synthesizer Chip

tent with the theory that “digital feedthrough” does, in fact, perturb the divider edges. The phase noise of the open-loop VCO was measured separately from the synthesizer and found to be less than -110 dBc/Hz at offsets greater than 10 KHz from the carrier. This means that the inband phase noise floor of the synthesizer, at -90 to -95 dBc/Hz is due to the bipolar synthesizer chip. This is due to the low current densities that were used in the logic gates. This lowered the gm of the devices as well making high valued pull-up resistors necessary to maintain signal swings.

In Figure 3-20, the phase noise floor from 1 MHz to 9 MHz is dominated by residual $\Sigma\Delta$ quantization noise. The level of this quantization noise can be compared to the theoretical levels shown in Figure 3-6. The $\Sigma\Delta$ noise levels, from 1MHz to 9MHz, in the actual measured results are lower

Figure 3-19: Synthesizer Printed Circuit Board

then those predicted, due to various parasitic poles in the loop, which are unavoidable. The $\Sigma\Delta$ quantization noise is not truly white, but rather shows periodicity. This periodicity occurs because the $\Sigma\Delta$ modulator used is a digital state machine. In fact, because the noise from the first three $\Sigma\Delta$ stages is cancelled, the number of possible quantization noise states is determined by the number of possible states in the final accumulator. If less periodicity is desired, increasing the number of bits in the accumulator or applying a dither signal to the first accumulator would be desirable. If we assume that the input referred divider noise is white and at a level of approximately -95 dBc/Hz the theoretical phase noise can be recalculated. The results of this are presented in Figure 3-21.

Figure 3-20: SSB Phase Noise Plot for a Transmit Frequency of 915 MHz

Figure 3-21: Theoretical Phase Noise

It was found that as the frequency being synthesized approaches the fractional band edges (integer multiples of the reference frequency), to within one loop bandwidth, inband spurs appear at a level of -40 dBc. The spurs are present on both sides of the carrier at a frequency offset exactly equal to the carrier offset from the band edge. For example, if the frequency being synthesized is $F_{\text{ref}}N$ plus 78.125 KHz, the carrier will be centered at this frequency and spurs will appear on both sides of it at a frequency offset of 78.125 KHz. These spurs do not appear in the $\Sigma\Delta$ bitstream when it is captured and processed in MATLAB. The spurs arise due to non-linear effects in the synthesizer. The exact source and elimination of this non-linear effect is the subject of ongoing investigation. It is believed that the source of this problem is the coupling of digital noise from the CMOS chip into the VCO through the power supply. However, if the band edges are avoided, a spur-free range of 19.6 MHz is available for data transmission.

The approximate settling time of the synthesizer (80% of final frequency) was measured, using the HP5372A frequency and time interval analyzer, for a frequency step of 8.4 MHz and found to range from 30 μs to 60 μs . This range is due to the fact that for this size of step the synthesizer loses lock and must reacquire lock before settling. For smaller steps, the settling time is lower than 50 μs as desired.

The overall power consumption of the synthesizer was found to be 491 mW. Most of the power consumption is due to the two “drop in” amplifiers used in the synthesizer. These amplifiers are rated at 85 mA from a 5 V supply. Another 30 mW of the power consumption is due to the VCO. If the VCO were integrated on to the chip as well, the power consumption of the synthesizer could be reduced even further [DCS97]. The combined power consumption of the CMOS control chip and the bipolar synthesizer chip was 32.1 mW.

3.7.4 Modulation Analysis

Random data bits were applied to the data input of the digital modulator chip at a rate of 62.5 Kb/s, resulting in a GMSK modulated frequency spectrum centered at 915 MHz. The modulated carrier was downconverted to 1.0 MHz in order to take advantage of the narrow resolution bandwidth

of the 40 MHz HP3585A spectrum analyzer. A plot of the downconverted spectrum is shown in Figure 3-22 along with a plot of the theoretical spectrum, for GMSK with a BT of 0.5. The horizontal frequency axis is normalized by the data rate. A plot of the downconverted and unmodulated carrier is included as well. From this plot it can be seen that the theoretical and measured spectra agree closely. The level of the sidelobes for the measured spectrum is slightly higher than theory due to the limited stopband attenuation of the Gaussian filter. By comparing the spectra of the modulated and unmodulated carriers, it can be seen that the noise floor of the modulated carrier is due to the inband and out of band phase noise of the PLL and not a non-ideal effect in the GMSK filtering.

The modulated output of the synthesizer was then applied to the HP89400-8 vector modulation analyzer. The modulation analyzer demodulates the incoming data and then uses the received data bits to construct the ideal reference modulation, for comparison with the incoming signal. This process is illustrated in Figure 3-23. The vector modulation analyzer defines the instantaneous signal as a magnitude and phase and compares this with the reference signal. In this way, the error vector is obtained. This vector representation is shown in Figure 3-24. Figure 3-25 shows the reference (TRACE B) and non-ideal (TRACE A) GMSK spectrum. Figure 3-29 shows the reference (TRACE B) and non-ideal (TRACE A) constellation plots. Figure 3-27 shows the reference (right trace) and non-ideal (left trace) I and Q eye diagrams. Figure 3-26 shows the reference (TRACE B) and non-ideal (TRACE A) phase trellis. Figure 3-28 and Figure 3-30 show the magnitude error per symbol and phase error per symbol respectively. Figure 3-31 summarizes the error statistics for the modulation. Due to a measurement error the matched filter used to generate the reference modulation was set to a rectangular response resulting in an MSK rather than GMSK reference signal. This means that the measured performance is slightly degraded from its optimum value.

The spreading of the constellation in Figure 3-29 and the phase error shown in Figure 3-31 are due to the integrated phase noise of the synthesizer over the bandwidth of interest.

Figure 3-22: Transmitted Spectrum

Figure 3-23: HP89400-8 Vector Modulation Analyzer

Figure 3-24: Vector Signal Representation

Figure 3-25: Non-ideal Versus Reference Data Spectrum (BT=0.5)

Figure 3-26: Phase Trellis, Non-Ideal versus Reference

Figure 3-27: Received I and Q Eye Diagrams, Non-Ideal versus Reference

Figure 3-28: Magnitude Error Plot for GMSK Modulation

Figure 3-29: Non-ideal Versus Reference Constellation Diagram

Figure 3-30: Phase Error Plot for GMSK Data Modulation

TRACE A: Ch1 MSK1 Syms/Errs
A Marker 23.0000 sym 1.0000

EVM	= 4.0247	%rms	10.466	% pk at sym	250
Mag Err	= 142.82	m%rms	-348.76	m% pk at sym	93
Phase Err	= 3.9406	deg	-5.9892	deg pk at sym	250
Freq Err	= 18.486	Hz			
IQ Offset	= -68.06	dB			

DATA?

Figure 3-31: Summary of Modulation Measurements

3.8 Summary

It has been shown, through the design and results presented in this thesis, that by incorporating a digital $\Sigma\Delta$ modulator, a fractional-N frequency synthesizer can be designed which has good spurious performance, low phase noise, and fast settling times. The synthesizer can be controlled with high accuracy, allowing direct digital modulation with GMSK data, within the loop bandwidth.

The data filter and the $\Sigma\Delta$ modulator were greatly simplified through the quantization of the tap coefficients using a software $\Sigma\Delta$ modulator, prior to storing them in an on chip ROM. This

reduced the required multipliers to XNOR gates.

The design was partitioned into a PLL section and a digital modulator section. A bipolar process was used to implement the PLL section, incorporating a multi-modulus divider, phase/frequency detector, and charge pump, using ECL/CML logic. The bipolar chip required 18.1 mW at 3.0 V. A CMOS FPGA was used to prototype the digital modulator section, incorporating a fourth-order $\Sigma\Delta$ modulator, a GMSK data filter and serial interface. The final digital modulator was implemented in a 0.5 μm CMOS process and required 14 mW for 20 MHz operation at 3 V. The power consumption of the digital chip could be reduced significantly by moving from a standard cell approach to a full custom digital design. In order to simplify the design an external loop filter and commercial VCO were used, but in future versions the VCO could be included on chip.

3.9 Recommendations

Two main problems were encountered in the design and testing of the synthesizer. The first was the high level of phase noise generated by the bipolar chip. Although this was due to the minimization of power in the divider, a method for predicting the phase noise level in digital dividers would be invaluable in order to optimize the design process. One possible method of doing this, which will be tested in the future, is presented in Appendix A, at the end of this thesis.

The second problem encountered was that of the limited stopband attenuation of the Gaussian lowpass filter due to end effects resulting from the $\Sigma\Delta$ quantization performed on the tap coefficients. A method will be presented, in Section 3.9.1, which can increase the stopband attenuation by more than 30 dB, at the cost of an additional quantization level.

3.9.1 An Improved GMSK Filter Architecture

As shown in Figure 3-8 the maximum stopband attenuation of the digital Gaussian filter used for pulse-shaping the transmit data in the synthesizer is 38 dB. This is due to the fact that the $\Sigma\Delta$ bit-stream, created when the Gaussian pulse is quantized to ones and minus ones, is truncated. At the ends of a Gaussian pulse, its final value approaches zero. However, due to the truncation of the

bitstream, only a one or minus one is possible. One way to reduce this problem is to add an additional quantization level equal to zero. It has been found that if an additional level is added to the output quantizer of a $\Sigma\Delta$ modulator, and that level is zero, gains of greater than one bit of resolution can be achieved [PBSA87].

Figure 3-32 shows the transfer function for a GMSK filter, with the same specifications as the one used previously in the synthesizer, except that, the tap coefficients have been quantized to three levels using a software third-order $\Sigma\Delta$ modulator. One of the levels is zero. It can be seen that the stopband attenuation is 70 dB. Figure 3-33 shows the same filter with two quantization levels, for reference, as was done in the implementation already presented. The revised approach gives an increase of 30 dB in stopband attenuation with the addition of a single quantization level. This improvement, due to the reduction in end-effects, is equivalent to, approximately, a four bit increase in resolution. The additional hardware required is 960 bits of ROM and three two bit multipliers.)

Figure 3-32: Improved GMSK Filter Transfer Function

Figure 3-33: GMSK Filter Quantized to Single Bit Values

Chapter 4 A Receive Path $\Sigma\Delta$ Frequency-to-Digital Converter With Reduced Quantization Noise

4.1 Introduction

In a wireless receiver some method of recovering the transmitted data is required. For constant amplitude frequency modulation, such as analog FM, or digital frequency modulation, such as GMSK, this is done at low intermediate frequencies using analog or digital techniques. Two possible receive path architectures are shown in Figure 4-1.

Figure 4-1: Receiver Architectures

The first architecture shown is used for analog FM and usually consists of one or two downconversion stages followed by a limiting amplifier and analog discriminator. The second architecture is a low IF downconversion followed by baseband digitization of the I and Q channels in order to allow digital filtering. The approach considered in this thesis is a single downconversion stage followed by a $\Sigma\Delta$ frequency-to-digital converter (FDC). This is basically the same as the first architecture shown in Figure 4-1 with the analog discriminator replaced by a $\Sigma\Delta$ FDC. $\Sigma\Delta$ FDCs can operate at high IF frequencies and are very linear frequency discriminators due to the single-bit quantizer used. It is important to note that these architectures combine frequency discrimination and digitization into a single operation. Other architectures are possible, such as digitization at a low IF followed by a digital I and Q downconversion to baseband.

In this Chapter, a novel architecture for a second-order $\Sigma\Delta$ FDC, aimed at receive path applications, is presented. An analysis of this architecture is presented, and in Chapter 5 a hardware design is described.

The contributions made in this area of research are the following.

- 1) The filtering requirements for a receive path $\Sigma\Delta$ FDC are discussed.
- 2) Three possible architectures for a second-order receive path $\Sigma\Delta$ FDC are investigated for suitability. (Appendix B)
- 3) A sampled-time phase detector is presented which allows a switched-capacitor integrator to be implemented in a $\Sigma\Delta$ FDC. (Appendix B)
- 4) An architecture for a second-order $\Sigma\Delta$ FDC is proposed which is suitable for receive path applications. This is the first known architecture to include a $\Sigma\Delta$ modulator as part of a feedback path in a $\Sigma\Delta$ modulator [Fil97]. The architecture demonstrates reduced quantization noise when compared to previous architectures.

In the next section we look at IF analog-to-digital conversion more closely.

4.2 IF A/D Conversion

A receive path A/D converter must have the dynamic range and resolution necessary in order to meet the SNR requirements and the bit-error rate (BER) requirements of the system being realized. Conversion to the digital domain at high IF frequencies is desirable since this reduces the analog complexity of the system, and in some cases, reduces the requirements on IF filtering. In this way, some of the selectivity of the receiver can be performed digitally. Subsequent signal processing, such as matched filtering and equalization, can also be performed digitally. Two possible approaches to this problem, both of which employ oversampling and noise shaping techniques, are $\Sigma\Delta$ frequency-to-digital conversion and bandpass $\Sigma\Delta$ modulation on analog voltage. The $\Sigma\Delta$ frequency-to-digital conversion approach was introduced in Chapter 2. In bandpass $\Sigma\Delta$ modulation, $\Sigma\Delta$ conversion on voltage is performed at an IF frequency employing either switched-capacitor or continuous time filtering techniques [SSJB96],[JSS97]. In this case, the noise transfer function is a notch and the signal transfer function is bandpass. Table 4.2, shown below, compares some recent $\Sigma\Delta$ IF A/D converters with respect to the IF frequency at which they operate. It can be seen, from this table, that continuous time bandpass $\Sigma\Delta$ modulators and $\Sigma\Delta$ FDCs have the potential to operate at high IF frequencies with high resolution.

Table 4.2: $\Sigma\Delta$ IF A/D Converters

Type	IF Freq. (MHz)	Fs (MHz)	Resolution and Bandwidth (KHz)	Power (mW)	Authors
BP $\Sigma\Delta$ (Switched Cap)	20	40	75 dB, 200	72	[OWo97]
BP $\Sigma\Delta$ (Switched Cap)	40	160	47 dB, 1250	65	[BaSn98]
BP $\Sigma\Delta$ (Continuous Time)	950	3800	57 dB, 200	135	[GaSn98]
$\Sigma\Delta$ FDC (Charge Pump)	1300	10	47 dB, 200	75	[Bax96]

The dynamic range required in the data converter used in a receiver depends largely on how interfering signals are handled. These interferers are usually other users of the same system transmitting on an adjacent frequency channel. If the frequency selective filtering of the receiver is performed in the DSP block following the data converter, or a large number of signals must be

converted simultaneously, a large input dynamic range is required in order to achieve the desired linearity and sensitivity. This is the usual approach when bandpass $\Sigma\Delta$ modulators are used. However, this is not necessarily feasible at high input frequencies and wide bandwidths.

Since the $\Sigma\Delta$ FDC is also a PLL, which is essentially phase-locked to the input signal, it locks on to the highest amplitude carrier present and, therefore, frequency selective filtering must be performed prior to the converter input. This means that the resolution required in the $\Sigma\Delta$ FDC is set mostly by the SNR required from the demodulated signal in order to achieve a particular bit error rate (BER) in the receiver, given a specific modulation format. Since no filter is perfect, the effect of adjacent channel residuals on the $\Sigma\Delta$ FDC must be determined in order to properly define the specifications for the IF filter which precedes the limiting amplifier. This presents a trade-off. While $\Sigma\Delta$ FDCs can operate with input frequencies of greater than a Gigahertz, the cost and limitations of the filters required for selectivity prior to the converter limits the input frequency to well below a Gigahertz.

In the next section, the divider model which is used to illustrate the $\Sigma\Delta$ operation of the $\Sigma\Delta$ FDC is derived.

4.3 The Divider Front-End

In Chapter 2, a $\Sigma\Delta$ FDC architecture was presented which makes use of a multi-modulus or dual modulus divider as a front-end. This front-end allows $\Sigma\Delta$ modulation to be performed on instantaneous frequency variables.

In this section, the divider front-end is examined and the model which explains the $\Sigma\Delta$ operation of the FDC is derived. This model can then be used in order to develop higher order architectures for $\Sigma\Delta$ FDCs. This model assumes that the $\Sigma\Delta$ FDC has reached steady-state operation (i.e., the loop has locked with $F_{in}/N = F_{ref}$). A full mathematical analysis of the divider and the loop is beyond the scope of this thesis.

4.3.1 Divider Phase Domain Model

The model and derivation presented here is the same as the one originally presented in [Bax95]. It is derived again in this thesis because it is felt that this model is not common or easily understood. This derivation will be used in order to justify the simplified model presented in Chapter 2, which is used in subsequent analysis.

A divide by 4/5 dual-modulus divider is shown in Figure 4-2. Figure 4-3 shows the timing diagram which describes the operation of this divider.

Figure 4-2: Divide by 4/5 Dual-Modulus Divider

Figure 4-3: Timing Diagram for Divider

The first waveform shown is, F_{in} , the input to the divider which has a nominal period, T_{IN} . The time at which the j th rising edge of the input signal occurs is denoted as $t_{IN,j}$. The second waveform shown is the divider output, F_{DIV} , which has a nominal period, T_{DIV} . The time at which the k th rising edge of the divider output occurs is denoted as $t_{d,k}$. The last waveform is the control input to the divider, b_i . If b is “0” the divider divides by 4 and if b is “1” the divider divides by 5. The division ratio is $N = n + b_i$ where $n = 4$ and $b_i = \{0, 1\}$. The k th divider edge occurs at the same time as the j th edge of the input signal, that is;

$$t_{d,k} = t_{IN,j} \quad (4-1)$$

where;

$$j = \sum_{i=1}^k (n + b_i) \quad (4-2)$$

The j th divider edge is defined as;

$$t_{IN,j} = jT_{IN} + \Delta t_{IN,j} \quad (4-3)$$

Where $\Delta t_{IN,j}$ is the instantaneous deviation from the nominal period due to modulation or noise. Combining Equation (4-2) and Equation (4-3), and resampling the signals at the divided down rate, the k th divider edge is given by;

$$t_{d,k} = \sum_{i=1}^k (n + b_i)T_{IN} + \Delta t_{IN,k} \quad (4-4)$$

The phase of the j th input edge is given by:

$$\theta_{IN,j} = \frac{2\pi}{T_{IN}}(jT_{IN} - t_{IN,j}) \quad (4-5)$$

Substituting Equation (4-3) into Equation (4-5) we obtain;

$$\theta_{IN,j} = \frac{2\pi}{T_{IN}}(-\Delta t_{IN,j}) \quad (4-6)$$

The output phase of the k th divider edge is given by;

$$\theta_{d,k} = \frac{2\pi}{T_{DIV}} \left(kT_{DIV} - \sum_{i=1}^k (n + b_i)T_{IN} - \Delta t_{in,k} \right) \quad (4-7)$$

When the divider is used as part of a $\Sigma\Delta$ FDC the loop is locked and the periods of the input signal and the divider output are related to each other through the average division ratio, $\bar{N}$. This means that $T_{DIV} = \bar{N}T_{IN}$ where, $\bar{N} = \overline{(n + b)}$. The value of n is four, in this example, and the expected value of the divider control bitstream is given by;

$$\bar{b} = \sum_{i=1}^k \frac{b_i}{k} \quad (4-8)$$

If we substitute back into Equation (4-7) with $\bar{N}$ and reorganize we obtain the following equation for the divider output phase.

$$\theta_{d,k} = \frac{2\pi}{\bar{N}} \left[k\bar{N} - \sum_{i=1}^k (n + b_i) + \frac{\Delta t_{IN,k}}{T_{IN}} \right] \quad (4-9)$$

If we multiply through by 2π and recognize that the last term is equal to Equation (4-6), resampled at the divided down rate, we can manipulate Equation (4-9) to obtain the following;

$$\theta_{d,k} = \frac{\theta_{IN,k}}{\bar{N}} - \frac{2\pi}{\bar{N}} \sum_{i=1}^k [b_i - \bar{b}] \quad (4-10)$$

Equation (4-10) leads to the block diagram shown in Figure 4-4.

Figure 4-4: Divider Model

This is basically the same model that was presented in Chapter 2. If we recognize that the input phase is the integral of the input frequency, we can replace the two integrators with a single integrator after the input summing block.

4.3.2 Adjacent Channel Residuals

An important specification of a radio receiver is how well it can detect the desired channel in the presence of an adjacent channel signal of larger amplitude. For example, a possible specification might state that a receiver must achieve an SNR of 40 dB in the presence of another signal 100 KHz away with an amplitude 70 dB higher. In the case of the divider, the input signal is required to clock the divider. This means that the signal must be hard-limited prior to the divider, in order to prevent AM to PM conversion, as only the zero crossings are of interest. Therefore, the interfering signal must have very little effect on the zero crossings of the desired signal. Figure 4-5 shows two unmodulated carriers with a frequency spacing of 100 KHz. The slower signal is the desired carrier, and the faster signal represents a carrier on an adjacent channel with an amplitude ten times larger. It can be seen, when we look at the sum of the two signals, that the zero crossings are dominated by the interfering signal. This will be the signal that the $\Sigma\Delta$ FDC will lock to. Once this occurs, the lost information cannot be recovered. If amplitude information were preserved by the loop, it would still be possible to eliminate the interfering signal. This means that any undesired signals must be attenuated prior to the demodulator input, using highly selective filtering. Filters

which can significantly attenuate a signal offset by 100 KHz at high centre frequencies are expensive and cannot be implemented on chip. This means that ceramic or SAW filter technologies are needed, increasing the cost.

Figure 4-5: Desired and Interfering Signals at IF Output

4.3.3 Higher Order $\Sigma\Delta$ Frequency-to-Digital Converter Architectures

In the previous section, a formal derivation of the divider model, shown in Chapter 2, was presented. This model has shown that a frequency divider encompasses the input summing block and the first integrator in a $\Sigma\Delta$ modulator which operates on instantaneous frequency variables. This equivalence to $\Sigma\Delta$ modulators allows the FDC presented in Chapter 2 to be extended to higher orders using standard $\Sigma\Delta$ techniques. The benefits achieved through doing this are increased SNR (resolution) and reduced tonal behaviour. However, when these architectures are mapped to hardware realizations, the resulting implementations differ from those used in voltage $\Sigma\Delta$ converters. Therefore, the mapping of a second-order $\Sigma\Delta$ FDC to hardware is now presented in order to clarify these differences. This example will be similar to existing second-order architectures which have been reported at both the PCB and IC level [Bax95],[Bax96].

A block diagram of a second-order, single-loop $\Sigma\Delta$ modulator is shown in Figure 4-6 a). Figure 4-6 b) shows the hardware implementation. The input summing block and first integrator can be implemented using a multi-modulus divider. A phase detector is then used to convert the instantaneous phase at the output of the first integrator into a proportional voltage, relative to F_{ref} . The second integrator is then implemented in continuous time using a charge pump or op-amp followed by a latched comparator. The $2 - z^{-1}$ block is implemented as follows. The output of the quantizer is split into two, separate, feedback paths. The first path consists of a delay block, D-type flip-flop, followed by an inverter, implementing $-z^{-1}$. The output of the inverter is fed into the least-significant-bit (LSB) of the divider control input (b_0 in Figure 4-6 b)). The second path feeds directly to the second control bit of the divider (b_1 in Figure 4-6 b)), achieving the required gain of two.

Figure 4-6: A Second-Order $\Sigma\Delta$ FDC

If we include the phase detector shown in Figure 4-6 b) the complete linear model is the one shown in Figure 4-7. However, since the quantizer is single-bit, the phase detector gain, K , and the 2π gain in the forward loop can be ignored as they are “absorbed” by the quantizer. The two integrators feeding the second summing block can be replaced by a single integrator at the output. Realizing that F_{ref} simply sets the DC operating point of the circuit, the model used in Figure 4-6 a) is suitable as a starting point for the design.

Figure 4-7: Full Model for Second-Order $\Sigma\Delta$ FDC

This section presented the divider model which demonstrates the $\Sigma\Delta$ nature of the $\Sigma\Delta$ FDC. An example of a second-order $\Sigma\Delta$ FDC was presented as well. Section 4.4 identifies a problem inherent in the divider front-end when it is used in receive path applications.

4.4 Modifying The Divider Front-end for Use In Receive Path Applications

It has been shown that the divider front-end allows the implementation of a $\Sigma\Delta$ FDC that can perform frequency-to-digital conversion at high IF frequencies. However, the divider front-end used in the previous architectures has a serious limitation. As the divider can only divide by integer values, equivalent to subtracting 0 or 2π radians of phase from the input, the full scale range of the modulator is equal to $\pm \frac{F_{ref}}{2}$. It is well known that, for maximum signal-to-noise ratio (SNR), the input to a $\Sigma\Delta$ modulator should have an amplitude equal to approximately 80% of the fullscale

input range of that modulator. This means that the sensitivity of the $\Sigma\Delta$ FDC is poor for signals with frequency deviations much smaller than the loop reference frequency. Since the reference frequency is also the sampling clock, it is not possible to reduce the reference frequency, for a given input signal, while maintaining performance. This is similar to the integer-N divider problem encountered in PLL frequency synthesis. If the $\Sigma\Delta$ FDC architectures presented thus far were used for FM demodulation, the maximum frequency deviation of the carrier would most likely be on the order of hundreds of Kilohertz, well below the fullscale range of the FDC. In the system proposed in Chapter 2 the IF frequency is 112.5 MHz and the GMSK modulation has a maximum deviation of $\pm 20\text{KHz}$. The modulation rate is 80 Kbs. In order to achieve an oversampling ratio of 32 in the $\Sigma\Delta$ FDC a reference frequency of 5 MHz is required. Therefore, in order to build the required receive path $\Sigma\Delta$ FDC, the architectures that have been presented must be modified in order to reduce their fullscale range or improve their noise shaping.

One way to lower the fullscale input range of the $\Sigma\Delta$ FDC is through the use of a fractional- δ frequency divider. A fractional- δ dual-modulus or multi-modulus divider, unlike an integer-N dual-modulus or multi-modulus divider, can divide by either N or $N+\delta$, where δ is a fractional value. For example, with a δ of one-quarter, the fullscale range of the $\Sigma\Delta$ FDC would be reduced to $\pm \frac{F_{ref}}{4}$, significantly increasing the sensitivity to low deviation FM signals. Fractional- δ division is difficult to achieve, especially if the δ desired is small. Possible approaches to this problem are presented in the following sections.

4.4.1 Fractional- δ Frequency Division Through Phase-Error Cancellation

One method of achieving fractional- δ division is through the use of phase error cancellation. This technique is often used in fractional-N frequency synthesis in order to achieve fine frequency resolution with a high PLL reference frequency.

One possible architecture for a fractional- δ divider, which makes use of phase-error cancellation, is shown in Figure 4-8 and can be used in order to explain this technique in general. This architecture is sometimes used in fractional-N frequency synthesis and is known as “Digi-phase”[Gil69].

The circuit shown in Figure 4-8 operates as follows. The desired division ratio is fed into the digital-phase-accumulator (DPA) as an M-bit digital word. The carry output of the DPA is used to control the divider, producing a 1-bit coarse quantization of the desired division ratio. The remainder in the accumulator is a measure of the error between the carry output and the desired output. The output of the divider is phase compared to a fixed reference converting the phase difference into a proportional voltage. The error remaining in the DPA is converted to a voltage using an M-bit DAC. This error voltage is subtracted from the phase detector output.

Figure 4-8: Fractional- δ Frequency Divider

The result of this subtraction is, ideally, the voltage which would have been obtained at the output of the phase detector had fractional division taken place. This means that the input frequency must lie between $F_{ref}(N)$ and $F_{ref}(N+1)$. The output frequency, therefore, lies between F_{in}/N and $F_{in}/(N+1)$ with a step size of $F_{ref}/(2^M)$. For example, if a two bit accumulator is used and the desired division ration is $N + 1/4$, the contents of the accumulator and the value of the carry output will be as shown in Table 4.3 below.

Table 4.3: Digi-Phase Accumulator Contents

Clock Cycle	Desired Phase	Carry output	Phase error
1	$2\pi/4$	0	$-2\pi/4$
2	$4\pi/4$	0	$-4\pi/4$
3	$6\pi/4$	0	$-6\pi/4$
4	2π	2π	0
5	$2\pi/4$	0	$-2\pi/4$
.	.	.	.

If there is mismatch between the gain of the DAC, K_D , and the gain of the phase detector, K_P in Figure 4-8, the correction signal will not be perfect, resulting in undesired tones at the divider output. Also, any non-linearities in the DAC will result in undesired tones.

Two alternative phase-error cancellation approaches were investigated for suitability in a receive path $\Sigma\Delta$ FDC. The first approach was an architecture which would combine the phase detector and DAC in such a way as to reduce the gain mismatch between them. The second approach was to perform the phase error cancellation in the phase domain, prior to the phase detector shown in Figure 4-8. These two architectures are presented in Appendix B. These approaches were found to have problems associated with them and were difficult to integrate easily. The following section details the alternative approach which was chosen in this thesis.

4.5 Proposed $\Sigma\Delta$ FDC Architecture

It was decided that, in order to increase the sensitivity of the $\Sigma\Delta$ FDC to low deviation FM waveforms, fractional- δ frequency division was necessary in order to achieve a fullscale input range which is lower than the reference frequency. However, phase-error cancellation, as discussed in the previous section, was thought to be too complex in terms of VLSI implementation requirements, particularly since quality of performance was in question. Therefore, it was felt that the

approach used in the design of the frequency synthesizer presented in Chapter 3, $\Sigma\Delta$ controlled fractional-N frequency division, might also be appropriate in the $\Sigma\Delta$ FDC.

Figure 4-9 shows a block diagram of the proposed $\Sigma\Delta$ FDC architecture.

Figure 4-9: Proposed $\Sigma\Delta$ FDC Architecture

This is the same architecture as that used in the second-order $\Sigma\Delta$ FDC of Figure 4-6, except that a $\Sigma\Delta$ DAC is nested in the feedback path and the feedback transfer function, $H_2(z)$, is, as of yet, undefined. Intuitively, this loop operates in the following manner. The output of the quantizer is fed into the feedback transfer function, $H_2(z)$. The output of this block is then fed into the least-significant-bit of the input of the digital $\Sigma\Delta$ modulator shown. The output step size of the digital $\Sigma\Delta$ modulator is still 2π , allowing a standard integer-N multi-modulus divider to be used. However, the feedback component of this bitstream is a small fraction of the total range and the remaining power is the quantization noise of the digital modulator. This means that the fullscale input range of the FDC would be $\pm \frac{F_{ref}}{2} \left(\frac{1}{2^N} \right)$; where N is the number of bits at the input of the digital $\Sigma\Delta$ modulator. This architecture is attractive in that both the feedback transfer function, $H_2(z)$, and the $\Sigma\Delta$ modulator are digital. This makes them both robust and reproducible. Also, both the feedback transfer function and the fullscale range of the $\Sigma\Delta$ FDC could be changed dynamically and easily during operation.

There are two drawbacks to this architecture. One drawback is that the nested $\Sigma\Delta$ modulator adds a significant amount of quantization error to the loop. The second problem is that of modulator overload due to the addition of this noise. The fullscale input range of the loop is now $(F_{\text{ref}}/2^N)$. However, the divider can only divide by integer values (i.e., subtracting integer multiples of 2π from the input phase). This means that, instantaneously, the level of quantization noise added to the loop is much larger than the fullscale input range of the loop, therefore, causing overload. It will be shown that the sensitivity of the modulator to overload can be reduced through proper selection of the feedback transfer function $H_2(z)$. MATLAB simulations were performed to determine a possible feedback function and the performance of the resulting modulator was compared to a standard second-order $\Sigma\Delta$ modulator under identical stimulus.

4.6 MATLAB Simulation Results

MATLAB simulations were performed for the modulator shown in Figure 4-10, which is a simplified version of the architecture shown in Figure 4-9. The simplified version of the divider model was used and the $1/\sqrt{N}$ and 2π gains have been removed as they are absorbed by the single-bit quantizer. The fullscale range is 1/64 of F_{ref} . The feedback transfer function, $H_2(z)$ in Figure 4-9, is $(k_1 + k_2) - k_2 z^{-1}$. This was derived from the general double-loop architecture for a second-order lowpass $\Sigma\Delta$ modulator, where k_1 is the gain of the outer loop and k_2 is the gain of the inner loop [ASV96]. Normally, k_1 and k_2 are set equal to one and the feedback becomes $2 - z^{-1}$. In this case, k_1 was set to 1/64 and the value of k_2 was chosen through simulation. The feedback $\Sigma\Delta$ modulator was chosen to be a second-order MASH, based on the fourth-order architecture presented in Chapter 3, due to ease of implementation.

Figure 4-10: Architecture Used for MATLAB Simulations

The resulting $\Sigma\Delta$ FDC was compared to a standard second-order $\Sigma\Delta$ FDC similar to the one shown in Figure 4-6, with a fullscale input range equal to F_{ref} . The following parameters were used in the simulations.

- 1) The reference frequency, F_{ref} , was set to 5 MHz.
- 2) A Blackman window was used for windowing of the bitstream.
- 3) Sixteen averages of 16384 point FFTs were used to obtain all power spectra.
- 4) The oversampling ratio (OSR) is defined as $F_{ref}/F_{Nyquist}$
- 5) The noise bandwidth is 0 to $F_{Nyquist}/2$.
- 6) The input sinusoid (signal FM modulating the carrier) was set at a frequency of $F_{ref}/512$ or approximately 9.8 KHz.
- 7) The frequency deviation of the sinusoid was set to $\pm 31.25 KHz$, unless otherwise stated.

A set of simulations was performed on the new architecture in order to determine the value of k_2 which maximizes the SNR of the modulator for an oversampling ratio of 128. A plot of the output

SNR versus the value of k_2 is shown in Figure 4-11.

Figure 4-11: SNR versus k_2

It can be seen, from Figure 4-11, that the SNR is maximum when $k_2 = 2/8$. This value of k_2 was used for the remainder of the simulations.

Figure 4-12 shows plots of the SNR versus OSR for the new architecture and the standard architecture. For a sinusoidal input at 9.8 KHz and a peak-to-peak deviation of $\pm 31.25 \text{ KHz}$, the curves for the new architecture and the standard architecture are nearly identical. For the standard $\Sigma\Delta$ FDC with a fullscale input of $\pm 2.0 \text{ MHz}$ the SNR is much higher.

Figure 4-12: SNR versus OSR

Therefore, there appears to be no advantage obtained through the use of the new architecture over the old. However, the advantage becomes apparent when the power spectra of the two architectures are compared. Figure 4-13 shows the output power spectrum for the new architecture and the old architecture for an input frequency deviation of $\pm 31.25 \text{ KHz}$. In this case the plot is setup relative to the signal peak. Figure 4-14 shows the output referred spectra for the same two modulators, relative to the total power in the output bitstream, which is assumed be the same for both modulators. From the first plot of the power spectra for the two modulators, Figure 4-13, it can be seen that the noise spectra are almost identical up to approximately 1 MHz, after which the new architecture demonstrates much lower quantization noise levels. From the plot of the output referred power spectra relative to the total power in the bitstream, Figure 4-14, it can be seen that the new architecture has a signal gain of 36 dB. Therefore, it is clear from both of these plots that, relative to the peak signal amplitude, the new architecture has far less out of band quantization noise than the standard architecture.

Figure 4-13: Output Referred Power Spectra (Relative to Peak)

Figure 4-14: Output Referred Power Spectra

The signal-to-noise ratio over the bandwidth from DC to $F_{ref}/2$ is -3.6 dB for the new architecture and -41 dB for the standard architecture. This indicates a 36 dB reduction in quantization noise. This means that the decimation filter requirements can be reduced for the new architecture compared to the standard architecture. The plots of SNR versus OSR were re-evaluated for both modulators. The bitstreams were passed through a second-order comb decimation filter and decimated by a factor of 16. The plots of SNR versus OSR for this case is shown in Figure 4-15.

Figure 4-15: SNR versus OSR (After Decimation Filtering)

The SNR versus OSR plot for the new architecture, after decimation, is basically the same the one shown in Figure 4-12. However, the SNR versus OSR plot for the standard second-order architecture has become much worse for the same input stimulus. The SNR versus OSR plot for the standard architecture with a fullscale input of $\pm 2.0\text{MHz}$ is now only moderately better. This can be explained by looking at the output referred power spectra for both modulators, shown in Figure 4-14. Ideally, both modulators have the same inband signal-to-noise ratio (this can be seen from the spectrum and the results of Figure 4-12). Both modulators also have the same level of out of band quantization noise. However, as can be seen from Figure 4-14, the new architecture has a signal

peak that is 36 dB higher. When the bitstreams are decimated, quantization noise around multiples of the new sampling frequency is aliased down into the band of interest, reducing the SNR. The purpose of the comb decimation filter is to “notch” (filter) the noise around multiples of the new sampling frequency. The order of the decimation filter determines the depth of these notches. Since both modulators have the same level of out of band quantization noise, the amount of noise folded back into the desired band is approximately the same for both architectures. However, since the new architecture has a higher signal and inband noise level, it can tolerate more folded noise than the standard architecture, while maintaining the same SNR. Typically, a standard second-order modulator would require a 3rd order comb decimation filter [CT91]. The new architecture, however, obtains the same result with a second-order comb filter. Figure 4-16 and Figure 4-17 show time domain plots of the decimated and filtered bits from the standard architecture and the new architecture, respectively. In the standard case, shown in Figure 4-16, high levels of quantization noise are still present. In the case of the new architecture, as shown in Figure 4-17, however, the input sinewave can clearly be seen.

Figure 4-16: Modulator Output Bits (Standard architecture)

Figure 4-17: Modulator Output Bits (New Architecture)

As a final example, GMSK data modulation with a bit rate of 78.125 KHz and a Bt of 0.5 was applied to the input of both simulated modulator architectures. The resulting bitstreams were passed through a second-order comb decimation filter and decimated by 16. The output power spectra for the two modulators are shown in Figure 4-18 and Figure 4-19, respectively. It can be seen, from Figure 4-18, that the standard architecture has much more quantization noise in this bandwidth than does the new architecture. The difference between the two bitstreams can more clearly be seen by looking at the time domain eye diagrams (obtained by running 16 averages with different sets of random data bits). The eye diagrams for both architectures are shown in Figure 4-20 and Figure 4-21. For the standard case the eye diagram, shown in Figure 4-20, is not clearly visible making data recovery difficult without higher order filtering. For the new architecture, the eye diagram shown in Figure 4-21, though noisy, can clearly be seen.

Figure 4-18: Power Spectrum for GSMK (Standard Architecture) **Figure 4-19: Power Spectrum for GSMK (New Architecture)**

Figure 4-20: Decimated Bitstream for GSM (Standard) **Figure 4-21: Decimated Bitstream for GSM (New architecture)**

In this section, it has been shown that by incorporating a $\Sigma\Delta$ modulator into the feedback path of a $\Sigma\Delta$ FDC, a stable architecture can be obtained which is able to discriminate low deviation FM signals (with respect to F_{ref}) with reduced hardware requirements on the decimation filter. The fact that the inband noise, relative to the peak signal, is the same as that of the second-order modulator, inband, is easily explained as follows.

The MASH $\Sigma\Delta$ modulator in the feedback path is a source of second-order shaped quantization noise added to the input of the overall loop. The feedback modulator has an output stepsize equal to $\pm F_{ref}/2$. Since this added noise has components in the band of interest, and undergoes the same transfer function as the input signal, it cannot be removed or reduced without affecting the input signal. The reduction in out of band quantization noise is best explained using a linear model for the new architecture. This model is presented in the next section.

4.6.1 Linear Model for the Proposed $\Sigma\Delta$ FDC Architecture

In order to more fully explain the operation of the new $\Sigma\Delta$ FDC architecture, it is useful to analyze the linear model. This model will also be used to perform a quantization noise analysis for the loop. While useful, this model does not explain all aspects of loop operation. For the analysis presented, a sampling rate of 5 MHz is used.

The linear model derived from the block diagram given in Figure 4-10 is shown in Figure 4-22.

Figure 4-22: Linearized Model for The New Architecture

The quantizer gain is denoted as Kq . It is important to be aware that a single bit quantizer is a highly non-linear element whose gain changes depending on the amplitude and nature of the input signal. For the initial analysis, Kq is set to one. However, this simplification does not take into account the effects of overload and time varying quantizer gain.

Three transfer functions can be derived from the linear model shown in Figure 4-22. The first of these is the forward signal transfer function, Y/X , given below.

$$\frac{Y}{X} = \frac{Kqz^{-1}}{1 - 2z^{-1} + z^{-2}(1 + Kq(k1 + k2)) - k2Kqz^{-3}} \quad (4-11)$$

This transfer function is plotted in Figure 4-23 below.

Figure 4-23: Signal Transfer Function (Linear Model: $Kq=1$)

It can be seen, from Figure 4-23, that the signal transfer function has a low pass response with 36 dB of passband gain. The response is flat up until approximately 10 KHz, and has decreased by 6dB at 100 KHz. The filter roll-off, after this point, is 40 dB/decade. The frequency content of the input signal should not exceed 100 KHz. Past this frequency, the signal will be attenuated. The noise transfer function for the overall loop, Y/Q_1 , is;

$$\frac{Y}{Q_1} = \frac{(1 - z^{-1})^2}{1 - 2z^{-1} + z^{-2}(1 + Kq(k_1 + k_2)) - k_2 Kq z^{-3}} \quad (4-12)$$

This transfer function is plotted in Figure 4-24 along with the standard second-order noise transfer function, $(1 - z^{-1})^2$.

Figure 4-24: Noise Transfer Function, Y/Q1 (Linear Model, Kq=1)

It can be seen, from Figure 4-24, that the slope of the noise shaping is the same for both architectures, 40 dB/decade, up to approximately 100 KHz at which point the noise shaping of the new architecture begins to flatten due to the denominator. The noise transfer function of the new architecture is 36 dB above the standard one.

The transfer function for the noise introduced by the nested $\Sigma\Delta$ modulator, Y/Q_2 , is given below.

$$\frac{Y}{Q_2} = \frac{-Kqz^{-2}}{1 - 2z^{-1} + z^{-2}(1 + Kq(k_1 + k_2)) - k_2Kqz^{-3}} \quad (4-13)$$

This transfer function is plotted in Figure 4-25. It can be seen from this plot that this transfer function is basically the same as the signal transfer function. That is, the input noise undergoes a gain of 36 dB in the 100 KHz passband and the out of band noise is attenuated by the lowpass action. This means that, inband, the dominant noise source in the output spectrum of the $\Sigma\Delta$ FDC is the MASH modulator. Out of band, this noise is attenuated by the forward transfer function of the loop.

Figure 4-25: MASH Modulator Noise Transfer function, Y/Q2

The theoretical quantization noise floor for the loop can be calculated using the linear model and compared to the noise floor obtained through simulation. The unshaped quantization noise is assumed to be uniformly distributed between 0 and $F_{ref}/2$, with a spectral density given as $\frac{\Delta^2}{12F_{ref}}$, where Δ is the step size of the quantizer in the modulator [CT91]. For the case of Q_1 , the noise added by the single-bit quantizer, this step size is $F_{ref}/64$. For Q_2 , the quantization noise added by the MASH modulator, the stepsize is F_{ref} . The noise generated by the MASH is also second-order noise shaped, apart from the lowpass action of the loop. Figure 4-26 b) shows the spectral densities of Q_1 and Q_2 when they have been filtered by the transfer functions given by Equation (4-11) and Equation (4-13) respectively. The output referred spectrum of the simulated modulator is shown in Figure 4-26 a) for comparison.

Figure 4-26: Quantization Noise Spectral Density

It can be seen that the quantization noise of the MASH $\Sigma\Delta$ modulator dominates and that the linear model almost exactly predicts the spectral density of the quantization noise.

4.6.2 Modulator Overload

It is important to note that the architecture shown in Figure 4-10 and Figure 4-22 has a delay in the feedback path as well as the forward path, after the MASH $\Sigma\Delta$ modulator. While the architecture does not require this extra delay for correct operation, it is included in order to simplify the timing constraints in the hardware design presented in Chapter 5. If this delay is removed, Equation (4-12) becomes;

$$\frac{Y}{Q_1} = \frac{(1 - z^{-1})^2}{1 + [kq(k1 + k2) - 2]z^{-1} + (1 - k2kq)z^{-2}} \quad (4-14)$$

and Equation (4-13) becomes;

$$\frac{Y}{Q_2} = \frac{(-kqz^{-1})}{1 + [kq(k_1 + k_2) - 2]z^{-1} + (1 - k_2kq)z^{-2}} \quad (4-15)$$

From these two equations we see that if, $k_1=k_2=kq=1$, Equation (4-14) becomes the noise shaping transfer function for a standard second-order $\Sigma\Delta$ modulator (i.e., $(1-z^{-1})^2$) and Equation (4-15) becomes a simple delay, multiplied by the gain of the quantizer in the forward path. Intuitively, when scaling the modulator input range, it would seem that k_1 and k_2 should be kept at a 1:1 ratio (i.e., in this case, $k_1=k_2=1/64$). The standard second-order architecture was simulated again with $k_1=k_2=1/64$ and an input frequency deviation of $\pm 31.25\text{KHz}$. The SNR versus OSR plot obtained from this simulation is shown in Figure 4-27 and the output power spectrum is shown in Figure 4-28.

Figure 4-27: SNR versus OSR

Figure 4-28: Output Power Spectrum

It can be seen that the results shown in Figure 4-27 and Figure 4-28 are comparable to the results for the second-order architecture with $k_1=k_2=1$ and a fullscale input. If we simulate the new architecture again with $k_2=k_2=1/64$ we obtain the output power spectrum shown in Figure 4-29. From the power spectrum shown in Figure 4-29 it is clear that the modulator has become unstable (i.e., the noise shaping has been corrupted). This corruption in noise shaping is due to modulator overload caused by the addition of large deviation noise to the input of the loop by the MASH $\Sigma\Delta$ modulator. This is explained by considering the quantizer gain, k_q . Because the quantizer used in the loop has only two output levels, the gain k_q is undefined. In fact, the gain of the quantizer varies as the amplitude of the input signal varies. For very small input levels to the quantizer, relative to the output levels, the quantizer has a very large gain. For very large inputs to the quantizer, relative to the output levels, the quantizer gain is very small.

Figure 4-29: Output Power Spectrum (New Architecture, $k_1=k_2=1$)

This decrease in quantizer gain is called overload and at this point the quantizer can no longer accurately represent the input signal. If we plot the pole zero diagrams and transfer functions for Equation (4-14) and Equation (4-15) respectively, the effect of varying quantizer gain can be demonstrated. Note that the second-order noise shaping function of the MASH modulator is added to the numerator of Equation (4-15) for the purposes of these plots. Figure 4-30 shows the magnitude and pole-zero plots for Equation (4-14) for $k_1=k_2=1/64$ when the quantizer gain, k_q , is varied from 64 down to 2 in steps of 1. Figure 4-31 shows the same plots but for Equation (4-15). From these two plots it is clear that, when k_q is lower than approximately twenty-five, the noise shaping starts to become corrupt.

Figure 4-30: Noise Transfer Function (Q1, $k_1=k_2=1/64$) Figure 4-31: Noise Transfer Function (Q2, $k_1=k_2=1/64$)

When k_q is equal to 64 the noise shaping becomes ideal. However, the noise from the MASH modulator would dominate and the result would be very similar to a standard second-order architecture with $k_1=k_2=1$, and no advantage would be gained.

It has been shown that through the use of a mean-square criterion [ArPa87], the non-linear quantizer in a $\Sigma\Delta$ modulator can be modeled as two separate linear gains and a source of additive white noise. One of these gains is used in the model of the signal transfer function and the other is used in the model of the noise transfer function. The gain of the noise shaping function can be statistically determined, using this method, and is equal to $k_q = \frac{\text{cov}(U, Y)}{\text{cov}(U, U)}$ [ArPa87], where cov is the covariance operator, U is the input to the quantizer and Y is the output as shown in Figure 4-22. Using this equation, the quantizer gain for the standard architecture was extracted from the results of the simulation used to obtain the power spectrum shown in Figure 4-28. The value extracted was 28. From Figure 4-32 and Figure 4-33 we can see that this value of quantizer gain is high enough to maintain the noise shaping. The quantizer gain for the new architecture was determined using the simulation results used to obtain the spectrum shown in Figure 4-29. In this case the quantizer gain was found to be 1.8, which is much too low to provide adequate noise shaping. These results show that due to quantizer overload, caused by the quantization noise added to the loop input by the MASH $\Sigma\Delta$ modulator, the quantizer is not able to achieve the amount of gain required in order to provide adequate noise shaping. Figure 4-32 and Figure 4-33 show the magnitude and pole zero plots for Equation (4-14) and Figure 4-15 with $k_1=1/64$ and $k_2=2/8$.

Figure 4-32: Magnitude and Pole Zero Plots ($k_1=1/64, k_2=2/8, Q_1$)

Figure 4-33: Magnitude and Pole Zero Plots ($k_1=1/64, k_2=2/8, Q_2$)

It can be seen, from the pole zero plots shown in Figure 4-32 and Figure 4-33, that the noise shaping transfer function is unstable for $kq > 8.0$ (i.e., a pole lies outside of the unit circle). When the quantizer gain is below 8 we can see that reasonable noise shaping can be achieved. The quantizer gain was extracted from the simulation and found to be 1.77.

The results presented in this section have shown that, due to quantizer overload, it is not possible to achieve standard second-order noise shaping using the new architecture. However, proper selection of k_2 allows for a noise shaping transfer function which is less sensitive to quantizer gain and will provide noise shaping even under overload conditions.

Next, we look at the difference between phase error and frequency error in the $\Sigma\Delta$ FDC.

4.6.3 Phase Error versus Frequency Error and Non-ideal Circuit Effects

When designing a demodulator for angle modulated signals, an important consideration which must be taken into account is; “What is the smallest frequency-shift, or the smallest phase-shift that can be detected using this architecture?” If we remember that phase and frequency are related to each other through ideal differentiation or integration, this raises some interesting issues in the case of the $\Sigma\Delta$ FDC, with respect to the above question.

Consider the conceptual block diagram for the new $\Sigma\Delta$ FDC architecture shown in Figure 4-34.

Figure 4-34: Conceptual Block Diagram of New $\Sigma\Delta$ FDC Architecture

The overall loop shown in Figure 4-34 is a $\Sigma\Delta$ modulator on instantaneous frequency. However, if the output bitstream is scaled and integrated, it is phase coherent and the input phase can be measured. In fact, the phase in the $\Sigma\Delta$ FDC accumulates indefinitely and is not limited to 2π radians. This integration reduces the noise shaping to first-order differentiation with a slope of 20 dB/decade. This observation raises an important intellectual point. While the $\Sigma\Delta$ FDC is a second-order $\Sigma\Delta$ modulator on input frequency, it is only a first-order $\Sigma\Delta$ modulator on input phase. This has strong implications when finding the input referred frequency noise or phase noise of the loop, especially with respect to non-idealities in the hardware design.

Note that the first integrator shown in Figure 4-34 is ideal and occurs due to the conversion from input frequency to input phase, in the divider. The phase detector and the second integrator, however, are not ideal. These circuits are sources of non-linearities and noise. This noise and non-linearities can be referred to the input of the phase detector as an equivalent source of additive phase error, Q_{phase} , as shown in Figure 4-34. This noise can further be referenced to the input of the modulator through differentiation and multiplication by the average division ratio, $\bar{N}$. The result of this is the input referred frequency error of the loop due to circuit non-idealities. Due to the differentiation that has taken place, this error has undergone first-order noise shaping with a perfect notch at DC. In order to obtain the input referred phase error of the modulator, due to circuit non-idealities, the frequency error must be integrated, cancelling out the differentiation. Therefore, the phase error at the input of the phase detector appears directly at the input of the modulator, scaled by the average division ratio of the loop.

The input referred phase error and frequency error for the $\Sigma\Delta$ FDC architecture presented in this chapter, obtained from theory and simulation, will now be presented.

4.6.4 Input Referred Frequency Error and Phase Error

In this section, the input referred frequency error and phase error of the $\Sigma\Delta$ FDC, due to quantization noise will be determined.

Ignoring circuit non-idealities, the output of the $\Sigma\Delta$ FDC takes the following form;

$$Y(z) = F_{in}(z)H_{sig}(z) + H_{noise}(z)Q1 + H_{sig}(z)(1 - z^{-1})^2 Q2 \quad (4-16)$$

where $F_{in}(z)$ is the instantaneous frequency of the IF input, $H_{sig}(z)$ is the forward transfer function of the modulator (Equation (4-11)), $H_{noise}(z)$ is the noise transfer function for the output comparator (Equation (4-12)), $Q1$ is the quantization noise of the comparator, and $Q2$ is the quantization error of the digital MASH-2 $\Sigma\Delta$ modulator. The noise components of Equation (4-16) are;

$$Q_{out}(z) = H_{noise}(z)Q1 + H_{sig}(z)(1 - z^{-1})^2 Q2 \quad (4-17)$$

From the simulation results of this chapter, it is known that the noise added by the MASH-2 $\Sigma\Delta$ modulator dominates and, therefore, the output frequency error of the modulator is given by;

$$Q_{out}(z) = H_{sig}(z)(1 - z^{-1})^2 Q2 \quad (4-18)$$

Using the additive white noise assumption for the MASH-2 $\Sigma\Delta$ quantization error, the spectral density of $Q2$, in Hz^2/Hz , is;

$$Q2 = \frac{(\Delta)^2}{12F_{ref}} = \frac{F_{ref}}{12} \quad (4-19)$$

The output spectral density of the quantization noise, in Hz^2/Hz , for the $\Sigma\Delta$ FDC is then given by;

$$Q_{out}(z) = \left| (1 - z^{-1})^2 H_{sig}(z) \right|^2 \frac{F_{ref}}{12} \quad (4-20)$$

Referring this to the input of the $\Sigma\Delta$ FDC we obtain;

$$Q_{in}(z) = \left| (1 - z^{-1})^2 \right|^2 \frac{F_{ref}}{12} \quad (4-21)$$

An important point must now be made about input referred frequency error and phase error versus the output referred frequency error and phase error. In all of the plots that follow, the input referred frequency error has units of dB/Hz relative to 1 Hz. The input referred phase error has units of dBc/Hz, the IF input frequency being the carrier. When the frequency error or phase error is referred to the output of the $\Sigma\Delta$ FDC using the transfer function, $H_{sig}(z)$, these units no longer hold. The 36 dB gain in the transfer function, $H_{sig}(z)$, (see Equation (4-12)) is a gain relative to the total power in the output bits of the $\Sigma\Delta$ FDC. That is, the power spectrum of the signal and the

inband noise now take up a larger fraction of the total power in the output bits, assuming that the input referred power spectrum has the same total power. However, the fullscale frequency range of the modulator represented by these bits, and the instantaneous phase shift represented by a one in the bitstream, have decreased by 36 dB relative to the loop reference frequency at lower frequencies. If the output noise spectral densities were recalculated taking this into account there would be no gain. Therefore, any calculations that involve absolute frequency shifts or phase shifts use the input referred noise spectral densities. The gain is an effective gain and is used only as a conceptual tool.

The spectral density of the input referred frequency error, in dB/Hz, relative to 1 Hz, is plotted in Figure 4-35. The spectral density of the output referred frequency error is also plotted.

Figure 4-35: Input and Output Referred Frequency Error Due to Quantization Error

As confirmation of the previous discussion, it can be seen from Figure 4-35 that the output referred frequency error is 36 dB higher, inband, than the input referred frequency error. However, the fullscale range has also been shifted by 36 dB, keeping the SNR constant. It can also be seen from Figure 4-35 that the out of band frequency error has been attenuated by the forward action of the loop. A calculation based on the power spectral density shows that the smallest theoretical rms frequency shift that can be detected over a 100 KHz bandwidth is approximately 2 KHz. Since the fullscale range of the $\Sigma\Delta$ FDC is $F_s/64 = 78.125$ KHz, the maximum SNR over the 100 KHz bandwidth would be 32 dB.

The theoretical input or output referred phase error for the $\Sigma\Delta$ FDC can be determined from Equation (4-20) and Equation (4-21), by performing the following integration.

$$H(z) = \frac{2\pi}{F_{ref}(1 - z^{-1})} \quad (4-22)$$

The spectral density of the output referred phase error is given by;

$$\mathcal{Q}P_{out}(z) = \frac{(2\pi)^2}{12F_{ref}} |H_{sig}(z)(1 - z^{-1})|^2 \quad (4-23)$$

The spectral density of the input referred phase error, in rads^2/Hz , is given by;

$$\mathcal{Q}P_{in}(z) = \frac{(2\pi)^2}{12F_{ref}} |(1 - z^{-1})|^2 \quad (4-24)$$

The spectral densities of the input and output referred phase error, in dBc/Hz (relative to the IF input centre frequency), are plotted in Figure 4-36.

Figure 4-36: Input and Output Referred Phase Error Due to Quantization Error

It can be seen from Figure 4-36 that, similar to frequency error, the output referred phase error is 36 dB higher than the input referred phase error, in band. However, the input signal also undergoes a gain of 36 dB, keeping the SNR constant. The output referred phase error is attenuated at frequencies above 100 KHz due to the forward action of the loop. It is important to note that the noise shaping is now first-order, i.e., the slope is 20 dB/decade as compared to the frequency error which has a slope of 40 dB/decade. A calculation shows that the smallest theoretical rms phase shift that can be detected over a 100 KHz bandwidth is 0.0263 radians or 1.5 degrees.

4.7 Summary and Proposed Architecture

In this Chapter, a novel $\Sigma\Delta$ architecture for use in a $\Sigma\Delta$ FDC has been presented. This architecture reduces the decimation filtering required in order to remove the quantization noise from the output bitstream. This architecture operates on low deviation FM signals. MATLAB simulations, combined with a linear analysis, have been used to explain the operation of this new architecture.

The advantages of this architecture, compared to other FM demodulation techniques are;

- 1) Uses a divider front-end which allows operation at high IF frequencies.
- 2) High linearity.
- 3) Uses a robust digital architecture.
- 4) Low power, fully integrated FM demodulator and A/D converter.

The main disadvantage of this architecture is that amplitude information is not preserved in the demodulation process. This means that it can only be used to demodulate constant amplitude angle modulated signals. Furthermore, this loss of amplitude information prevents any further frequency selective filtering to be performed after digitization. This means that all of the frequency selective filtering must be performed prior to the $\Sigma\Delta$ FDC, limiting the maximum IF frequency which can be used. However, this technique is still worth exploring as it could be used as a less expensive FM demodulator in analog cordless phones or as a low cost GMSK demodulator. Also, for digital modulation, matched filtering, etc., can now be performed in the digital domain [Pan96].

When compared to previous divider based $\Sigma\Delta$ FDCs [BeCo94],[Bax95],[Bax96], this architecture has the following advantages. For the cost of two digital accumulators and a small amount of combinatorial logic, the order of decimation filtering required has been reduced by one. Furthermore, there are a large number of possible transfer functions that have yet to be explored. Moving to a multi-bit quantizer could provide several advantages including higher SNRs and increased stability.

In Chapter 5 a hardware design of the architecture shown in Figure 4-9 is presented. This design is a proof of concept which is needed to confirm feasibility. Power consumption has not necessarily been minimized. For comparison, a standard second-order $\Sigma\Delta$ FDC was also designed.

Chapter 5 A 112 MHz IF Receive Path $\Sigma\Delta$ Frequency-to-Digital Converter IC

5.1 Introduction

This chapter presents the design of a $\Sigma\Delta$ frequency-to-digital converter based on the new architecture presented in Chapter 4. The circuit was designed in a 0.8 μm BiCMOS process. A standard second-order $\Sigma\Delta$ FDC has also been designed for comparison purposes. This circuit is used as a proof of concept. The differences between phase error and frequency error in the $\Sigma\Delta$ FDC with respect to non-ideal components will be clarified.

The contributions made to this area of research are the following.

- 1) One of the first known hardware designs of a $\Sigma\Delta$ FDC with a digital $\Sigma\Delta$ modulator in the feedback path is presented.
- 2) The first known hardware design of a divider front-end based $\Sigma\Delta$ FDC with a switched-capacitor integrator is presented.
- 3) The difference between input referred frequency error and input referred phase error in the $\Sigma\Delta$ FDC is clarified.
- 4) A low delay multi-modulus divider architecture is presented.

The overall $\Sigma\Delta$ FDC architecture is now described.

5.2 Overall Circuit Architecture

A block diagram of the $\Sigma\Delta$ FDC is shown in Figure 5-1. It consists of four blocks, the multi-modulus divider and acquisition loop, sampled-time phase detector and switched-capacitor integrator, feedback logic, and the clock generator. The architecture will now be described and detailed descriptions of each block are given in subsequent sections.

Figure 5-1: Receive Path $\Sigma\Delta$ FDC

The circuit shown in Figure 5-1 operates as follows. The input signal enters the acquisition loop which consists of a multi-modulus divider, lead-lag phase detector and acquisition logic. The input signal is divided down and phase compared to a fixed reference clock using the lead-lag phase detector. This phase detector has been modified such that it has a deadzone equal to the phase detection range of the sampled-time phase detector. Until the phase difference between the divided down input signal and the reference clock enters this range, the output of the lead-lag phase detector is used to control the loop. In this mode, the loop behaves as a first-order $\Sigma\Delta$ FDC. Once the output of the divider falls into the desired phase detection range, the second-order loop is activated. The divider output is then passed to the switched-capacitor block which consists of a

sampled-time phase detector, similar to the one shown in Figure B-1, and a switched-capacitor integrator. Here, the signal is converted into an equivalent charge in the sampled-time domain and integrated (This is the second integrator shown in Figure 4-10). The output of the integrator is fed to the digital logic block which consists of a quantizer, $(k_1 + k_2) - k_2z^{-1}$ block, and the second-order digital MASH $\Sigma\Delta$ modulator. The output of the MASH is fed to the divider control input. The clock generator distributes the loop reference signal and generates all the required clock signals, including the non-overlapping clocks required in the switched-capacitor block.

The acquisition loop and switched-capacitor blocks are fully differential in order to achieve maximum noise immunity. The digital block is composed of single-ended CMOS logic. Each block was tested individually for functionality and then combined. Overall simulations of the architecture were not practical due to the large relative differences in the time steps required.

The $\Sigma\Delta$ FDC design presented here is the circuit level version of the one presented in the MATLAB simulations performed in Chapter 4, and has the following specifications.

- 1) IF input frequency = 112.5 MHz.
- 2) The reference frequency is 20 MHz externally, 5 MHz internally.
- 3) Makes use of CML logic, CMOS logic, and switched-capacitor circuitry.
- 4) Full scale input frequency deviation range is $\pm 31.25 \text{ KHz}$.
- 5) Supply voltage is 3.3 V.

The power consumption of the entire $\Sigma\Delta$ FDC was determined from simulation and found to be 38 mW.

Each of the four blocks shown in Figure 5-1 are now described in detail and simulation results are presented where appropriate.

5.2.1 Acquisition Loop

The acquisition loop is implemented using fully differential, standard cell, CML logic blocks. The cells were hand placed and hand routed due to the presence of high frequency signals.

The acquisition loop consists of two blocks, the multi-modulus divider and the lead-lag phase detector with acquisition logic. A block diagram of the acquisition loop is shown in Figure 5-2. The acquisition loop consumes 30 mW from a 3 V supply. The multi-modulus divider and lead-lag phase detector are now described.

Figure 5-2: Acquisition Loop

5.2.1.1 Low Delay Multi-Modulus Divider

A block diagram of the multi-modulus divider is shown in Figure 5-3. The divider is implemented using fully differential, standard cell, CML logic.

Figure 5-3: Low Delay Multi-Modulus Divider

The first stage of the divider consists of an input buffer and a divide by 3/4 dual-modulus divider. The rest of the divider consists of a 3-bit M-Counter, a 2-bit A-counter, and a low delay circuit. The input buffer has a 50 ohm input impedance and a minimum sensitivity of $\pm 10\text{mV}$. The division ratio is equal to $4(M + 1) - 2A$. The 3-bit control input to the M-Counter is used to set the integer offset of the divider and is controlled external to the chip. The input to the M-counter has CMOS logic levels which are converted to differential CML levels on chip. The A-counter controls the dual-modulus divider and determines whether or not to divide by N , $N+1$, $N+2$, or $N+3$ on any given reference cycle. The two input bits of the A-counter are controlled by the 2-bit output of the MASH $\Sigma\Delta$ modulator or the output of the lead-lag phase detector depending on the mode of operation. The divider architecture is the same as that used in the synthesizer described in Chapter 3. The low delay block, however, is new and is now described.

It is important, for correct operation of the overall loop, that the delay through any given block be minimized. Thus, a low delay divider was implemented. A schematic of the low delay block is shown in Figure 5-4. This is a simplified schematic and does not include full circuit details.

Figure 5-4: Low Delay Circuit

In the divider, it is not necessary to change the division ratio from N , $N+1$, $N+2$ or $N+3$ until the N th input cycle has been counted. This means that, in theory, the minimum possible delay through the divider, from the control input to the output pulse, is three cycles of the input signal. In order to achieve this minimum delay in the multi-modulus divider, the output of the divider is fed into the three element delay line shown in Figure 5-4, which is clocked by the IF input signal. The 2-bit input to the A-counter is used to select a divider output pulse which can be delayed by N , $N+1$, $N+2$ or $N+3$ cycles. Both the M and A counters are reloaded at the same time. The divider actually performs the desired division on the subsequent cycle (i.e., “catches up”). The D-type flip-flop shown at the output of the 4:1 MUX is used to synchronize the output. By using this architecture, the maximum delay through the divider is equal to four periods of the IF input signal (i.e., 40 ns for a 100 MHz IF input).

The sampled-time phase detector requires the divider pulses to be four input cycles wide in order to ensure correct operation of the loop (This will be explained in Section 5.2.2.1). The divider operation is set up such that all the divide-by-three cycles of the DMD occur at the start of the reference cycle and the divide-by-four cycles occur at the end. Therefore, the desired pulse width of

four input cycles is guaranteed.

The lead-lag phase detector in the acquisition loop requires two inputs from the divider. The first is the divider output and the second is the divider output delayed by four periods of the input signal. This additional output is obtained by extending the delay-line shown in Figure 5-4 by three stages and adding a second 4:1 MUX and synchronization flip-flop.

Figure 5-5 shows simulation results for the divider when the division ratio is changed from 22 to 23. The divider consumes 9 mA from a 3 V supply.

Figure 5-5: Divider Simulation Results (HSpice)

5.2.1.2 Lead-Lag Phase Detector and Acquisition Logic

The lead-lag phase detector and associated waveforms are shown in Figure 5-6. The circuit consists of two D-type flip-flops.

Figure 5-6: Lead-Lag Phase Detector

The inputs to this circuit are the loop reference clock, the divider output, PdPlus, and the delayed divider output, PdMinus. The reference is used to clock both flip-flops. PdPlus and PdMinus are each sent to one of the two flip-flops. The cases where the reference is lagging or leading the divider output, and the deadzone, are illustrated. Table (5-1) describes the possible phase detector states and the action that is taken by the acquisition loop during each of these states. Once acquisition has occurred (State 1,0 in Table (5-1)), the output of the MASH is used to control the divider and the INIT signal is pulled high, enabling the sampled-time phase detector and the switched-capacitor integrator.

Table 5-1: Lead-Lag Phase Detector

OUTA	OUTB	Situation	Action
0	0	Reference leads	Divide by N
0	1	Reference Lags	Divide by N+1
1	0	Done acquisition	Activate loop
1	1	Undesired state	Divide by N+1

5.2.2 Switched Capacitor Block

Figure 5-7 shows a block diagram of the switched-capacitor block, which consists of a sampled-time phase detector and a switched-capacitor integrator.

Figure 5-7: Switched Capacitor Circuit

The sampled-time phase detector, shown in Figure 5-7, samples a differential charge onto the sampling capacitors, C1 and C2. This is done by integrating a current onto each capacitor over a period of time determined by the phase difference between the centre of the divider output pulse,

Div, and the reference clock edge, ref. This charge develops a differential voltage, V_{in} , across the sampling capacitors. This charge is then transferred to the integrator through the switches shown in Figure 5-7. In a standard switched capacitor circuit, this voltage would be sampled instantly onto the capacitors and then transferred to the integrator. However, the end result is the same in that the desired charge is transferred from the input to the output of the integrator over the reference period. This leads to the simplified, single-ended, model for the sampled-time phase detector and switched-capacitor integrator, shown in Figure 5-8.

Figure 5-8: Equivalent Switched-Capacitor Circuit Model

The sampled-time phase detector and switched-capacitor integrator have the following combined transfer function;

$$\frac{V_o}{\theta_i} = \frac{-C1}{C2} \left(\frac{1}{1 - z^{-1}} \right) K_{PD} \quad (5-1)$$

where $C1$ and $C2$ are the value of the capacitors in the sampled-time phase detector and switched-capacitor integrator, and K_{PD} is the phase detector gain, in V/rad, given as;

$$K_{PD} = \frac{IT_{ref}}{2\pi C1} \quad (5-2)$$

Where I is the tail current of the phase detector and T_{ref} is the period of the reference clock. The tail current in the design is nominally 12 μA and $C1$ has a value of 1pF. Therefore, the phase detector gain is 0.382 V/rad.

A timing diagram, including example waveforms is shown, in Figure 5-9, for one full reference cycle. (Acquisition has just occurred). Note that CLR and DUMP are active low signals.

Figure 5-9: Sampled Time Phase Detector and Integrator Waveforms

A cycle, as shown in Figure 5-9, begins after the falling edge of the reference clock. This is when the CLR signal is pulled low, shorting the sampling capacitors, C1 and C2, to analog ground. When the divider output pulse, Div, rises, the left branch of the phase detector is activated. During the time period between the divider rising edge and the reference rising edge, charge is integrated onto C2. This results in a voltage, ΔV_2 , being developed across C2. Then, between the reference rising edge and the falling edge of the divider output, charge is integrated onto C1. In the example of Figure 5-9, the charge integrated onto C1 is zero. The differential charge stored on C1 and C2 is then dumped onto the integrating capacitors, C3 and C4, while DUMP is held low. The output of the op-amp is fed into the digital block shown in Figure 5-1.

In order to determine the phase detection range required in the sampled-time phase detector, and the relative sizes of the capacitors in the switched-capacitor block, the internal swings of the $\Sigma\Delta$ FDC architecture must be known. Of importance is the maximum time shift, in nano-seconds, at

the output of the divider (output of first integrator) and the voltage swing at the output of the second integrator. Figure 5-10 shows a state-space plot for the new architecture, obtained from MATLAB simulations. The horizontal axis shows the maximum and minimum time shifts at the output of the first integrator, in reference cycles. The vertical axis shows the maximum and minimum swings at the output of the second integrator.

Figure 5-10: $\Sigma\Delta$ FDC State Space Diagram

We see, from the horizontal axis, that the time deviations of the divider output edge span approximately ± 1.3 cycles of the IF input signal. Inserting a safety margin, the range of the sampled-time phase detector was set to ± 2.0 cycles of the input signal or ± 36 degrees. Therefore, the divider output pulse must be four input cycles wide in order for the phase detector to work over this range. This means that the maximum voltage swing at the output of the sampled-time phase detector is $\pm 360mV$.

From the vertical axis, we see that the output of the second integrator spans the same range as the output of the first integrator. The maximum and minimum voltage swings at the output of the sec-

ond integrator will be set by the ratio of the integrating capacitors to the sampling capacitors. The ratio of the integrator capacitors to the phase detector capacitors was set to one, in order to guarantee a voltage swing of $\pm 360\text{mV}$ at the output of the second-integrator. Therefore, the integrating capacitor C2 was set to a value of 1 pF.

The switches shown at the input and output of the op-amp are used to pull the input and the output of the op-amp to known voltages until acquisition has taken place.

From simulations of the extracted circuit, the power consumption of the switched-capacitor block was found to be 4.0 mW.

5.2.2.1 Sampled-Time Phase Detector

A complete schematic of the sampled-time phase detector is shown in Figure 5-11. Device sizes and component values are given in Table (5-2) . This is the same phase detector that is presented in Appendix B. A description of the functionality of this circuit can be found there as well..

Figure 5-11: Sampled Time Phase Detector

Bipolar transistors were used as the current steering devices in the phase detector, since the operating speed required is fairly high. The phase detector gain can be adjusted by changing the tail current which is set using an “off chip” resistor and the current mirror formed by Q5, Q6 and Q7.

Table 5-2: Component Values and Device Sizes for Sampled-Time Phase Detector

Component	Size/Value
Q1-Q7	1 x
P1 & P2	10/0.8 ($\mu\text{m}/\mu\text{m}$)
C1 & C2	1 pF
R1 & R2	15 K Ω

Of particular interest in Figure 5-11 are the integrating capacitors and PMOS switches shown, as they are the most critical nodes in this circuit and are very sensitive to mismatch and noise. PMOS switches were used as they are capable of pulling up to Vdd. Both the capacitors and the switches are placed in an N-well which is pulled to Vdd. This provides some shielding from noise present in the substrate. Since one plate of the capacitors shown in Figure 5-11 is connected to Vdd, this plate should also be the bottom plate of the capacitor. In this way, the parasitic capacitance, from the bottom plate of the capacitor to the substrate, is shorted to analog ground (Vdd). This is illustrated in Figure 5-11, where it can be seen that the parasitic capacitance, C_p , has been “shorted out”.

The phase detector characteristic was calculated from SPICE simulation results and is plotted in Figure 5-12. A linear fit to this curve is plotted, as well, and is described by the function $y = -20.4017x - 18.5088$ mV. The constant offset term of -18.5088 mV is not a concern, since feedback in the $\Sigma\Delta$ FDC can compensate for fixed offsets. It can be seen, from Figure 5-12, that the phase detector characteristic is highly linear over the expected range of operation (± 1.3 cycles of IF input). The maximum linearity error is 0.044% and the rms linearity error is 0.016%. This results in a linearity of approximately 67 dB in the phase detector.

Figure 5-12: Phase Detector Characteristic

5.2.2.2 Folded Cascode BiCMOS Operational Amplifier

There are two circuit parameters which are of particular significance in switched-capacitor integrators for use in $\Sigma\Delta$ modulators. These parameters are the DC gain of the operational amplifier (op-amp) and the settling time of the integrator.

The DC gain of the op-amp determines the amount of quantization noise suppression in the base-band region of the modulator and becomes a significant factor at high oversampling ratios. Finite DC gain in the op-amp results in integrator “leak” which creates deadzones in the input-to-output characteristic of the modulator [FeCh91]. The bitstream generated by the $\Sigma\Delta$ FDC will be identical for different input DC frequencies that fall within the range of a deadzone. In order for the width of the deadzones to fall below the noise floor of the modulator, the DC gain of each integrator, H_0 , should be greater than $(2f_o T)^{\frac{5}{4}}$, where $f_o T$ is the inverse of the oversampling ratio of the modulator [CT91]. When measuring instantaneous frequency, the switched-capacitor integrator in

the $\Sigma\Delta$ FDC is the second integrator in the loop. The DC gain of the second integrator is less critical than that of the first integrator, since the total DC gain of the modulator depends on the cascaded gain of both integrators. Any noise, or non-linear effect, that is referred to the input of the second integrator is divided by the gain of the first integrator when referred to the input of the loop. This is not the case when measuring input phase, as explained in Section 4.6.3. For an over-sampling ratio of 128, the gain of the op-amp must be at least 45 dB. MATLAB simulations of the new $\Sigma\Delta$ FDC architecture, taking into account leakage in the second integrator, show that an SNR of 53 dB can be achieved when measuring instantaneous frequency, for an OSR of 128 and a DC gain of 40 dB or greater in the second integrator.

Since the output of the second integrator is only sampled at the end of each clock cycle, the only settling time requirement is that the op-amp has settled. Whether or not this settling process is linear is not relevant. The settling time of the integrator depends on the RC time constant formed by the transmission gate “on” resistance and the integrating capacitors, as well as the unity gain bandwidth (UGBW) and slew rate of the op-amp. In this case, the integrator has 50 ns of settling time available. Since the unity gain bandwidth of the op-amp should be five to ten times greater than this [GrTe86], a unity gain bandwidth of at least 100 MHz is required in the amplifier.

The transmission gates shown in Figure 5-7 were implemented using a PMOS device, with $W = 7.0 \mu\text{m}$ and $L = 0.8 \mu\text{m}$. The time constant formed by the “on” resistance of the transmission gate and the 1 pF capacitor will limit the settling time of the system. A plot of the “on” resistance of the transmission gate for different input voltages is shown in Figure 5-13. The step response of the RC circuit formed by the transmission gate and integrating capacitor can be approximated as [Baz96];

$$V_{cap} = V_{in} \left(1 - e^{-\frac{t}{RC}} \right) \quad (5-1)$$

Where V_{cap} is the voltage across the capacitor and V_{in} is the input voltage. For a $\pm 300 \text{ mV}$ input step, the time required for 0.1% settling is found to be 16.9 ns.

Figure 5-13: Transmission Gate On Resistance

A schematic of the op-amp used in the switched-capacitor integrator is shown in Figure 5-14. It consists of a folded cascode formed around a bipolar differential pair. NMOS source followers are used to shift the output common mode of the sampled-time phase detector down to the level required by the differential pair.

Figure 5-14: BiCMOS Folded Cascode Operational Amplifier

The common mode feedback circuit is formed using two triode connected PMOS devices, shown in Figure 5-14, P1 and P2. These devices behave as voltage controlled resistors [GrTe86]. If the output common mode voltage rises, the gates of P1 and P2 are also raised, in voltage, increasing their resistance, thus lowering the voltage at node x. This tends to lower the output common mode voltage. If the output common mode voltage decreases, the gates of P1 and P2 are pulled to a lower voltage and their resistance will decrease, thus, pulling node x closer to VDD, raising the output common mode voltage. The device sizes are given in Table (5-3) and the op-amp specifications are given in Table (5-4). The bipolar transistors are all "1x" devices and all resistors have a value of 6.5 K Ω , except for R1 which is double this.

Table 5-3: Device Sizes

Device	Size ($\mu\text{m}/\mu\text{m}$)
N1	300/0.8
N2	300/0.8
P1	150/0.8
P2	150/0.8
P3	300/2
P4	300/2
P5	150/3
P6	150/3
P7	39/0.8
P8	76/2
P9	76/3

Table 5-4: Op-Amp Specifications

Specification	Value
DC Gain	71 dB
Unity Gain Bandwidth (UGBW)	151 MHz (0.5 pF load)
Phase Margin	30 degrees (0.5 pF load)
Slew Rate	100 V/ μs
Differential Output Swing	3.4 V
Power Consumption	3.0 mW @ 3.3 V

It can be seen, from Table (5-4) , that the DC gain of the op-amp is sufficient and that the unity gain bandwidth of 151 MHz is approximately 8 times the required settling frequency. A plot of the ac response of the op-amp is shown in Figure 5-15 for a 0.5 pF differential capacitive load.

Figure 5-15: ac Characteristics of the Folded Cascode

From this plot, the DC gain of 71 dB can be seen as well as the 151 MHz unity gain bandwidth. The phase margin of 30 degrees may not be sufficient to guarantee stability of the op-amp. If this were found to be a case, stability could be increased by increasing the output load capacitance.

Figure 5-16 shows a plot of the settling characteristic of the op-amp for a 300 mV step in input voltage. The circuit used in this simulation is shown in Figure 5-17.

Figure 5-16: Output Settling Characteristic for a 300 mV Step in Input Voltage

Figure 5-17: Circuit Used for Settling Simulation

For 1% settling, or 40 dB of accuracy, the time required is approximately 20 ns. For 0.1% settling, or 60 dB of accuracy, the time required is approximately 40 ns. Therefore, the 54 dB accuracy required in the integrator, 0.2% settling, should be achievable within the 50 ns allocated for settling.

5.2.3 Digital Circuit Block

A block diagram of the digital logic is shown in Figure 5-18.

Figure 5-18: Digital Logic Block

The digital block shown in Figure 5-18 operates in the following manner. The outputs of the op-amp, OUTP and OUTN, are fed into the latched quantizer inputs, InP and InN, shown in the dashed box. The positive or negative output of the quantizer is selected using a 2:1 MUX and the control signal, SW, which is set externally. This signal, SW, allows the polarity of the feedback to be reversed if a wiring error has occurred in the design of the circuit. The output of the MUX is fed into the feedback block, and also to the output buffer, as it is the output bitstream of the modulator. The output of the feedback block is added to a 6-bit fractional channel offset which is set externally ($A_5 \dots A_0$). The result of this addition is fed into the digital second-order MASH $\Sigma\Delta$ modulator. The 2-bit output of the MASH is converted from CMOS logic levels to CML logic levels and fed to the input of the CML acquisition loop.

Each individual section of the digital logic will now be described in greater detail.

A circuit schematic for the comparator is shown in Figure 5-19 [BFR97]. The NMOS devices have a width of $1.4\text{ }\mu\text{m}$ and a length of $0.8\text{ }\mu\text{m}$. The PMOS devices have a width of $3.0\text{ }\mu\text{m}$ and a length of $0.8\text{ }\mu\text{m}$.

The core of this circuit consists of a pair of cross-coupled inverters formed by transistors N3 and N4 and transistors P1 and P2. In order to avoid hysteresis in the comparator (i.e., “memory”), a reset circuit controlled by the input signal, EVAL, is included. When EVAL is pulled low, transis-

tor N7 is turned off and the sources of N3 and N4 are pulled to VDD using P3 and P4, clearing the core latch. P5 and P6 pull the inputs of the output buffers (inverters formed by transistors P8,N5 and P7,N6) to VDD forcing both comparator outputs to a logic “low”. When EVAL is pulled high, the core latch is “released” and will latch to a state which depends on whether or not InN or InP are high or low with respect to each other.

At the end of an EVAL cycle (EVAL = “high”) the output of the comparator is latched using the two D-type flip-flops shown in Figure 5-19, after which the core latch of the comparator is cleared.

5.2.3.2 Feedback Logic and Channel Offset Adder

A schematic of the feedback logic and the channel offset adder is shown in Figure 5-20. The output of the feedback logic is a 6-bit number which is added to a 6-bit channel offset which is set externally by the user. The feedback function of the $\Sigma\Delta$ FDC, $(k_1 + k_2) - k_2z^{-1}$, is implemented with $k_1=1/64$ and $k_2=2/8$.

Figure 5-20: Feedback Logic

Table (5-5) is the truth table that was used to determine the required values for B5 to B0, based on the current value of quantizer output and the delayed version.

Table 5-5: Truth Table for Feedback Logic

Q_i	Q_{i-1}	Value	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0	0
0	1	-16/64	1	1	0	0	0	0
1	0	17/64	0	1	0	0	0	1
1	1	1/64	0	0	0	0	0	1

From Table (5-5) we can obtain the following logic equations, implemented in Figure 5-20.

$$B5 = \overline{Q_i}Q_{i-1}$$

$$B4 = \overline{Q_i}Q_{i-1} + Q_i\overline{Q_{i-1}}$$

$$B3 = B2 = B1 = 0$$

$$B0 = Q_i$$

The 6-bit output of the channel adder is fed to the 6-bit input of the MASH-2 $\Sigma\Delta$ modulator, which is described in the next section.

5.2.3.3 Digital MASH-2 $\Sigma\Delta$ Modulator

A block diagram of the second-order digital MASH $\Sigma\Delta$ modulator is shown in Figure 5-21. It is formed from two digital accumulators and noise shaping logic. This is a second-order version of the fourth-order digital MASH architecture $\Sigma\Delta$ modulator used in the synthesizer of Chapter 3.

Figure 5-21: MASH-2 Digital $\Sigma\Delta$ Modulator

5.3 Loop Timing and Clock generator

As mentioned in Chapter 4, the total number of delays around the $\Sigma\Delta$ FDC loop is two. For a 5 MHz clock, this means that the maximum delay allowable around the entire loop is 400 ns. Table (5-6) shows the maximum delays, derived from simulation, for different operations which must be performed in the loop. With a nominal input frequency of 112.5 MHz, an input cycle is approximately 9 ns.

Table 5-6: Delays In the Loop

Operation	Delay (ns)
Divider control input to output edge	$4T_{in} = 36$ ns
Phase detection	$8T_{in} = 72$ ns
Integrator Settling (0.1%)	40 ns

The distribution of the 400 ns delay around the loop is not critical so long as all timing requirements are met. Two delays were purposely introduced into the loop using D-type flip-flops. Each of these delays is equal to 200 ns. As long as the signal propagates from one of these flip-flops to

the next in this time interval, the timing requirements will be met. One of the delays is used to latch the output data from the MASH architecture $\Sigma\Delta$ modulator, prior to the input to the acquisition block. The second delay block is used to latch the output of the comparator that follows the switched-capacitor integrator.

Figure 5-22 shows a timing diagram for the loop including all of the control signals. This assumes that the loop is locked, with the divider output pulse falling within the operating range of sampled-time phase detector.

Figure 5-22: Loop Timing Diagram

The different control signals in the loop are;

- 1) CLK - Used as the EVAL signal in the quantizer. It is also the clock used to latch the accumulator feedback, the feedback logic delay and the D-type flip-flops at the output of the MASH. This signal has CMOS logic levels.
- 2) CLR - Is an active low signal used to clear the sampling capacitors in the sampled-time phase detector, once per reference cycle. This signal has CMOS logic levels.
- 3) DUMP - Is an active low signal used to “dump” the charge stored in the sampled-time phase detector on to the integrating capacitors of the switched-capacitor integrator. This signal has CMOS logic levels.
- 4) EYE - Is the signal whose edge is used to latch the output of the differential comparator. This signal has CMOS logic levels.
- 5) REFLG, REFLGb - This differential signal is used as the loop reference for the lead-lag phase detector in the acquisition circuit. This signal has CML levels.
- 6) REFPD, REFPDb - Is the differential loop reference signal used by the sampled-time phase detector. This signal has CML logic levels.
- 7) Init - Is the acquisition signal. When acquisition has occurred, Init is pulled to a logic “high” releasing the integrator from the “ready” state. Init has CML logic levels within the acquisition loop and is translated to CMOS logic levels in the clock generator, where it becomes INTS.

The events which occur over a complete cycle of the control signals are now explained sequentially. These events correspond to the numbers shown on the timing diagram of Figure 5-22.

- 1) On the rising edge of CLK, the output of the MASH modulator is latched and held for the divider control input one full reference cycle (i.e., 200 ns).
- 2) The CLR signal is pulled low for 50 ns, clearing the sampling capacitors in the sampled-time phase detector.
- 3) The divider output pulse is phase compared to the reference clock, REFPD and REFLG. This comparison occurs somewhere within the 80 ns region around the reference rising edge. This is the region between the dotted lines shown in Figure 5-22.
- 4) After the phase detection operation is completed, the DUMP pulse is pulled low for 50 ns transferring charge from the phase detector to the integrator.
- 5) While CLK is high, the quantizer is set to evaluation mode and a decision is made as to the output value of the quantizer ("0" or "1"), based on the op-amp output.
- 6) On the rising edge of EYE, the output from the quantizer is latched for one full cycle.
- 7) On the rising edge of CLK, the output of the MASH is latched. This gives 150 ns for the quantizer output to propagate through the feedback logic and the MASH. (i.e., the rising edge of EYE to the rising edge of CLK)

The above description of the timing diagram shows that it takes two full delays, 400 ns, for the output of the MASH to propagate around the entire loop.

A schematic of the clock generator is shown in Figure 5-23.

Figure 5-23: Clock Generator

From the timing diagram shown in Figure 5-22, we see that the minimum time between events is 50 ns. Therefore, the external clock applied to the clock generator must have a frequency of 20 MHz. This clock is divided by four using the two D-type flip-flops, shown in Figure 5-23, in order to obtain the 5 MHz clock signal, **CLK**. The inverted clock signal is used as the reference for the lead-lag phase detector and the sampled-time phase detector. Since this signal consists of CMOS logic levels, it is converted to fully differential CML levels using the buffers shown. The signals **EYE**, **CLR** and **DUMP** are derived from the divider using the combinatorial logic shown. Since **CLR** and **Dump** must not be “low” simultaneously (i.e., must be non-overlapping), the non-overlapping clock circuit shown in the dashed lines, [GrTe86], is used.

From simulation results the clock generator was found to consume 3.0 mW from the 3 V supply.

5.4 Standard Second-Order Single Loop $\Sigma\Delta$ FDC Architecture

For comparison purposes a standard second-order single loop $\Sigma\Delta$ FDC, like the one shown in Figure 5-24, was implemented. The block diagram for this architecture is the same as the one shown in Figure 5-1. The differences lie in the digital block, which no longer contains a MASH $\Sigma\Delta$ modulator and has a feedback transfer function equal to $2 - z^{-1}$.

Figure 5-24: Standard Second-Order $\Sigma\Delta$ FDC

Figure 5-25 shows a block diagram of the digital circuit.

Figure 5-25: Digital Block

In order for the standard second-order architecture to operate correctly, there can only be a single delay around the entire loop (i.e., 200 ns). Therefore, the latches that were present at the output of the MASH modulator in the new architecture, are eliminated in the second-order architecture.

A timing diagram for this loop is shown in Figure 5-26. The control signals are the same as those used in the new architecture, except that CLK is used to latch the output of the comparator and $\overline{\text{DUMP}}$ is the EVAL signal. The signal EYE is not employed in the standard architecture.

Figure 5-26: Timing Diagram

The events which occur in this loop are now listed and correspond to the numbered events shown in the timing diagram of Figure 5-26.

- 1) On the rising edge of CLK, the output of the quantizer is latched and propagates through the $2 - z^{-1}$ feedback block to the divider control inputs.
- 2) CLR is pulled low, shorting the sampling capacitors in the sampled-time phase detector to analog ground, removing any residual charge.
- 3) The divider output is phase compared to the fixed loop reference clock. This phase difference is stored as a proportional differential charge on the phase detector capacitors.
- 4) DUMP is pulled low, transferring charge from the sampled-time phase detector to the switched-capacitor integrator. Evaluation occurs in the comparator.
- 5) The rising edge of CLK arrives, latching the comparator outputs.

It can be seen, from the above description, that the total delay around the loop is 200 ns.

5.5 Mixed Signal Design and Layout Considerations

When building complex integrated circuits, such as the $\Sigma\Delta$ FDC, where noisy digital circuits and sensitive analog circuits must coexist on the same substrate, careful consideration must be taken in choosing design techniques, both at the architectural level and the physical layout level. Several techniques were used in the design of the $\Sigma\Delta$ FDC presented, in order to minimize this unwanted interaction between the digital and analog blocks.

Due to the common substrate, digital noise in the $\Sigma\Delta$ FDC can couple to the analog circuits, not only through the power supplies, but through the substrate itself. Figure 5-27 shows a CMOS inverter.

Figure 5-27: Digital Noise in a CMOS Inverter

Whenever the output of the inverter changes states, a surge of current is drawn from the power supply. This current generates a noise voltage in the power supply due to parasitic inductance. Also, some proportion of this switching current is injected into the substrate, either through the substrate connected ground shown, or through the parasitic output capacitance. Interconnect capacitance contributes to this output capacitance. The amount of current injected into the substrate depends on the switching rate of the gate, its drive capability and the voltage swing etc.,.

There are two approaches that can be used to reduce the digital noise injected into the substrate. One is through the minimization of the injected noise at the source, in this case, the digital gates. The second method is to increase the noise immunity of sensitive circuits through architecture choices or shielding [TsFu97]. Both of these approaches were used in the design and layout of the $\Sigma\Delta$ FDC.

5.5.1 Reduction of Noise

In order to reduce the amount of noise coupled into the analog switched-capacitor block, different techniques for reducing the digital noise were employed in the acquisition loop, the digital block and the clock generator.

At the circuit level, the following precautions were taken in order to reduce the amount of digital noise in both the power supplies and the substrate.

- 1) Separate VDD supplies were used for all four blocks shown in Figure 5-1. One version of the design uses on chip decoupling capacitors.
- 2) CML logic was used in the largest digital block, the acquisition loop. Because CML logic uses current steering and has small voltage swings, very little transient current is generated during level changes.
- 3) Both the CML and CMOS logic gates used have separate circuit grounds and substrate connected grounds. These two grounds should only be connected together on a low impedance ground plane, external to the chip. In this way, transient currents can only be coupled into the substrate through the output capacitance of the digital gates. If this capacitance is minimized, the noise is reduced farther.

At the layout level, the following precautions were taken in order to minimize the substrate and power supply noise generated within the digital blocks.

- 1) Minimization of power supply impedance.
 - a) All power supply connections, VDD, VSS and Vsub were made using wide metal lines in order to provide a low impedance return path for supply currents.
 - b) Separate VDD, VSS and Vsub metal rings were placed around each block in order to allow the shortest connection possible to any circuit within the block. The substrate connected ground was used as the outer ring.
 - c) Any metal lines connected to the substrate use a large number of substrate contacts in order to reduce the impedance of this connection. This connection is improved by placing PDEV below the connected metal.
 - d) Multiple VDD, VSS and Vsub bonding pads were used for each block, wherever possible.
 - e) All of the substrate connected grounds can be “star” connected to the die-pad which is fused to the eight corner leads of the chip package.

5.5.2 Increasing the Noise Immunity of Sensitive Circuits

The following steps were taken in order to increase the noise immunity of sensitive signal paths and the switched-capacitor block in the $\Sigma\Delta$ FDC.

- 1) The acquisition loop and the switched-capacitor block employ fully differential signaling providing a high immunity to common mode noise.
- 2) All bias voltages in the analog block are generated locally and referenced to the local, substrate connected, grounding point.
- 3) A metal guard strip was placed around the switched-capacitor block. This strip consists of p-type material and metal lines heavily contacted to the substrate. Both ends of this strip are connected to separate V_{sub} bonding pads. A similar guard strip was placed around the high impedance input NMOS devices of the folded cascode operational amplifier.
- 4) All capacitors and PMOS devices in the analog block were placed in N-wells with the N-well substrate pulled to a positive voltage, in this case VDD. This well forms a reverse biased PN junction with the substrate. Any noise coupled into the well from the substrate does this through the depletion capacitance, which has a plate shorted to VDD, the analog ground.
- 5) The placement of bonding pads takes into account the different signals and an effort was made to avoid unwanted coupling between adjacent pads.

A plot of the complete layout for the new $\Sigma\Delta$ FDC architecture is shown in Figure 5-28. The layout of the analog switched-capacitor block is shown in Figure 5-29.

5.6 Phase and Frequency Error in the $\Sigma\Delta$ FDC Due to Circuit Non-Idealities

Using the techniques described in Section 4.6.3 the levels of the input referred frequency error and phase error, due to circuit non-idealities, for the $\Sigma\Delta$ FDC shown in Figure 5-1 are now determined.

The second integrator in the $\Sigma\Delta$ FDC is not ideal and is a source of noise in the loop. The different noise sources in the switched-capacitor integrator, shown in Figure 5-7, can be referenced to the input of the sampled-time phase detector as an equivalent phase error, as shown in Figure 4-34. This noise can then be referenced to the input of the $\Sigma\Delta$ FDC as an equivalent frequency error or phase error.

There are two sources of noise in the switched-capacitor integrator shown in Figure 5-30 (shown again here for convenience). The first is the noise in the sampled-time phase detector and the

Figure 5-30: Switched-Capacitor Integrator

second is the internal noise of the operational amplifier. Although capacitors C1 and C2 behave as

switched capacitors with respect to the input signal, they behave differently with respect to noise. Unlike a standard switched-capacitor circuit, where the thermal noise of a transmission gate “on” resistance is sampled onto a capacitor, the noise in the sampled-time phase detector is integrated onto the sampling capacitors over a time period that varies from sample to sample. The worst case occurs at the edges of the phase detection range when the noise is integrated onto one of the two capacitors over the entire period of the divider output pulse, T_{div} . This assumes that Q1 is turned on and Q2 is turned off. The equivalent circuit, during the integration period, is shown in Figure 5-31. QM1 and QM2 are from the current source I in Figure 5-30, and Q1 and Q3 act as cascode devices.

Figure 5-31: Equivalent Circuit During Integration Period

The transfer function, from the output of the current source QM1 to the capacitor voltage, is given by;

$$\frac{V_{C1}}{I_{in}} = \frac{1 - e^{-j\omega T_{div}}}{sC_1} \quad (5-1)$$

which is the transfer function for an integrator that only integrates for T_{div} seconds, the worst case as above. In order to find the total power of the noise integrated onto the capacitor during this

time, the following integral must be solved;

$$P_n = \frac{\bar{I}_n^2}{2\pi} \int_0^{-2\pi} \left| \frac{1 - e^{-j\omega T_{div}}}{sC_1} \right|^2 d\omega \quad (5-2)$$

where $\bar{I}_n^2$ is the mean-squared noise, in amps², of the cascoded current source. The solution to the integral in Equation (5-2) is;

$$P_n = \frac{\bar{I}_n^2 T_{div}}{2(C_1)^2}, T_{div} > 0 \quad (5-3)$$

This result shows that the total noise can be decreased by decreasing the integration period or increasing the capacitor size. Since this noise is sampled onto the capacitor once per period of the loop reference clock, the noise power is completely aliased into the bandwidth from DC to Fref/2. Therefore, the spectral density of this noise is;

$$S_n = \frac{\bar{I}_n^2 T_{div}}{Fref(C_1)^2} \quad (5-4)$$

Equation (5-4) does not account for all of the noise sampled onto C_1 each reference period. There is also thermal noise sampled onto C_1 due to the “on” resistance of the PMOS transmission gate used to “dump” the charge on the integrating capacitors, C_3 and C_4 in Figure 5-30, as in a standard switched-capacitor circuit [BFR97]. The spectral density of this noise is;

$$S_C = \frac{2KT}{FrefC_1} \quad (5-5)$$

where K is Boltzmann’s constant and T is the absolute temperature in Kelvins. Therefore the total noise spectral density due to the phase detector and switched capacitor is given by;

$$S_{CT} = \frac{1}{FrefC_1} \left[\frac{\bar{I}_n^2 T_{div}}{C_1} + 2KT \right] \quad (5-6)$$

Next, the output noise of the current source, $\bar{I}_n^2$, as defined in Equation (5-2), must be determined. Since the current through the cascode devices, Q1 and Q3, is set by the current mirror formed from QM1 and QM2, they contribute a negligible amount of noise to the circuit. If no degeneration resistors (R1 and R2 in Figure 5-31) are used, the dominant source of noise in this circuit is

the collector shot noise and the thermal noise of the base resistance of the mirror devices QM1 and QM2. The total spectral density of this noise is given by;

$$\tilde{I}_n^2 = 2(qI_c + 4KT r_b) \quad (5-7)$$

where q is the charge of an electron which is equal to 1.6×10^{-19} Coulombs, I_c is the collector current of QM1 and QM2 (assumed to be identical) and r_b is the base resistance of both QM1 and QM2. If degeneration resistors are used in the current source, as shown Figure 5-31, the noise in Equation (5-7) is reduced by a factor which is approximately equal to the ratio of the base referred degeneration resistor and the small signal input resistance of the transistor r_{π} . In the circuit designed for this thesis, this ratio is approximately equal to seven. These results were confirmed through SPICE simulations. The noise of Equation (5-6) can be referred to the input of the sampled-time phase detector, through division by the phase detector gain, as an equivalent phase error, in rads^2/Hz , given by;

$$\theta_{i, CT} = \left| \frac{1}{K_{PD}} \right|^2 S_{CT} \quad (5-8)$$

where K_{PD} is the phase detector gain, in V/rad. This can be referred to the input of the $\Sigma\Delta$ FDC as an equivalent frequency error, given as;

$$\mathcal{Q}_{\text{freq}, CT} = |(1 - z^{-1})|^2 \left(\frac{\bar{N} F_{ref}}{2\pi} \right)^2 \theta_{i, CT} \quad (5-9)$$

The input referred phase error, in rads^2/Hz , due to KT/C noise and phase detector noise is;

$$\mathcal{Q}_{\text{phase}, CT} = \bar{N}^2 \theta_{i, CT} \quad (5-10)$$

If we consider the input referred noise spectral density of the op-amp, e_{op} , it has the following transfer function from the input terminal of the op-amp to the input of the sampled-time phase detector (see Figure 5-30);

$$\frac{\theta_i}{V_{n, op}} = \frac{-z^{-1}}{K_{PD}} \quad (5-11)$$

Therefore, the spectral density of the phase error at the input of the sampled-time phase detector,

due to the input referred noise of the op-amp, is given by;

$$\theta_{i, op-amp} = \left| \frac{-z^{-1}}{K_{PD}} \right|^2 e_{op} \quad (5-12)$$

To refer this error to the input of the $\Sigma\Delta$ FDC, as an equivalent frequency error, we must differentiate and multiply by the average division ratio of the divider, giving;

$$Q_{freq, op-amp} = |(1 - z^{-1})|^2 \left(\frac{\bar{N} F_{ref}}{2\pi} \right)^2 \theta_{i, op-amp} \quad (5-13)$$

The input referred phase error, in rads^2/Hz , due to op-amp noise is given by;

$$Q_{phase, op-amp} = \bar{N}^2 \theta_{i, op-amp} \quad (5-14)$$

The total, input referred, integrated noise voltage of the op-amp, including 1/f noise and thermal noise, was obtained from SPICE simulations of the extracted circuit, over a bandwidth of 1GHz, and is equal to 5.281×10^{-4} Volts. Assuming that the op-amp bandwidth is much greater than the sampling frequency, F_{ref} , and that the noise is therefore completely aliased into the region from DC to $F_{ref}/2$, due to sampling, the rectangular noise power spectral density over this range is equal to $1.1 \times 10^{-13} \text{ V}^2/\text{Hz}$.

For the circuit designed in this chapter and shown in Figure 5-30; $F_{ref} = 5.0 \text{ MHz}$, $T_{div} = 36 \text{ ns}$, $I_{in} = 11.29 \mu\text{A}$, and $C_1 = 1 \text{ pF}$. The input referred frequency error spectral densities, due to the KT/C noise of the switched capacitor, phase detector noise and op-amp noise are shown in Figure 5-32. The input referred frequency error due to quantization noise is included as a reference.

The spectral densities of the input referred phase error due to the KT/C noise of the switched capacitor, phase detector noise and op-amp noise are shown in Figure 5-33. The input referred phase error due to quantization error is included as a reference.

Figure 5-32: Input Referred Frequency Error for Different Noise Sources

Figure 5-33: Input Referred Phase Error Due to Different Noise Sources

It can be seen, from Figure 5-33, that the input referred phase error, due to KT/C noise, phase detector noise, and op-amp noise, is not noise shaped. It can be seen, from Figure 5-32 and Figure 5-33, that the input referred frequency error and phase error due to op-amp noise is higher than the input referred frequency error and phase error due to KT/C noise and phase detector noise, making it dominant.

The spectral density of the total input referred frequency error, due to all sources of noise considered, is shown in Figure 5-34. The frequency error due only to quantization error is also shown.

Figure 5-34: Total Input Referred Frequency Error

It can be seen, from Figure 5-34, that below approximately 10 KHz, the total input referred frequency error changes slope from second-order noise shaping to first-order noise shaping, due to noise in the sampled-time phase detector and switched capacitor integrator. This increases the frequency error, in band, and is dominant for high oversampling ratios. The smallest frequency shift that can be detected over a 100 KHz bandwidth is still approximately 2 KHz. This value has not changed significantly from the ideal case as the majority of the frequency error is due to quantiza-

tion error in the frequency range from 10 KHz to 100 KHz.

The spectral density of the total input referred phase error, due to quantization error and noise in the sampled-time phase detector and switched capacitor integrator, is shown in Figure 5-35. The phase error, due to quantization error only, is also included.

Figure 5-35: Total Input Referred Phase Error

It can be seen, from Figure 5-35, that below approximately 10 KHz the phase noise spectral density flattens out, due to noise in the sampled-time phase detector and switched-capacitor block. This additional noise will lower the SNR of the $\Sigma\Delta$ FDC, especially for high oversampling ratios. The smallest phase shift that can be measured over a 100 KHz bandwidth is 0.0263 radians or 1.5 degrees. Again, the majority of the phase error is due to quantization error in the frequency range from 10 KHz to 100 KHz.

Table (5-7) shows the minimum detectable phase shifts or frequency shifts over different bandwidths when only quantization error is considered. Table (5-8) shows the same data, when the noise of the switched-capacitor block is included in the calculation. The SNR for each bandwidth, in both tables, is given with respect to the fullscale frequency range of 78.125 KHz. The values presented in Table (5-7) and Table (5-8) are somewhat optimistic since the linear model was used to predict the quantization noise and the gain of the quantizer was set to one.

Table 5-7: Ideal Sensitivity of $\Sigma\Delta$ FDC

Bandwidth of interest	Smallest Detectable Frequency Shift (Hz) and SNR for Fullscale Frequency Deviation	Smallest Detectable Phase Shift (degrees)
4.0 KHz	0.65, SNR = 102 dB	1.2×10^{-2}
15.0 KHz	17.70, SNR = 73 dB	8.6×10^{-2}
30.0 KHz	100.35, SNR = 58 dB	0.25
62.5 KHz	628.95, SNR = 42 dB	0.75
270.0 KHz	24225, SNR = 10 dB	6.9

Table 5-8: Non-Ideal Sensitivity of the $\Sigma\Delta$ FDC

Bandwidth of interest	Smallest Detectable Frequency Shift (Hz) and SNR for Fullscale Frequency Deviation	Smallest Detectable Phase Shift (degrees)
4.0 KHz	1.12, SNR = 97 dB	2.58×10^{-2}
15.0 KHz	18.91, SNR = 72 dB	9.7×10^{-2}
30.0 KHz	102.10, SNR = 58 dB	0.26
62.5 KHz	631.49, SNR = 42 dB	0.75
270.0 KHz	24260, SNR = 10 dB	6.7

The $\Sigma\Delta$ FDC designed in this chapter is aimed at FM demodulation and has a fullscale input frequency deviation range of 78.125 KHz. Table (5-7) and Table (5-8) show the achievable SNRs over different bandwidths. If the values in Table (5-7) and Table (5-8) are compared, it can be seen that the input referred noise of the switched capacitor block has little effect on these values, except over narrow bandwidths. The first bandwidth, 4.0 KHz, is that used for voice communications in analog FM wireless systems such as AMPS. The SNR of 97 dB is more than adequate for such an application. The next bandwidths, 15 KHz and 30 KHz, could be used for audio band transmission, using analog FM, in wireless applications such as wireless loudspeakers. The SNRs achieved in this case are not acceptable for high quality audio which requires SNRs of greater than 90 dB. The 62.5 KHz bandwidth corresponds to the GMSK data modulation rate used in the transmit synthesizer presented in Chapter 3. The SNR of 42 dB is more than adequate for detection of this data. For GMSK data modulation with a BT=0.5, the SNR required for a bit error rate (BER) of 1×10^{-3} , with non-coherent demodulation, is approximately 12 dB [Bur97]. The last bandwidth, 270 KHz, corresponds to the GMSK data rate for GSM or DCS-1800. The SNR of 10 dB over this bandwidth makes this particular FDC unusable for this application. A higher clock rate in the $\Sigma\Delta$ FDC (a higher OSR) would of course be more suitable here.

As discussed previously, the $\Sigma\Delta$ FDC could also be used to detect phase. This is done by integrating and scaling the output bitstream of the FDC. The FDC can accumulate phase indefinitely (greater than 2π radians) and is slew rate limited to $\frac{2\pi F_{ref}}{64}$ rads/s. However, the phase error due to quantization noise is only first-order shaped and there is finite DC phase error present due to internal noise sources in the FDC. The results shown in Table (5-7) and Table (5-8) indicate that the performance of the $\Sigma\Delta$ FDC as a phase detector is not as impressive as for use as a frequency detector.

5.7 Conclusions

In this chapter, the design and layout of a receive path $\Sigma\Delta$ FDC, based on the new architecture presented in Chapter 4, was described. Due to circumstances beyond the author's control, fabrication of the circuit was not possible at this time, and therefore measurement results are not available.

However, from this design, a low delay multi-modulus divider and a unique switched-capacitor integrator, whose input is phase rather than voltage, were presented. Also, various mixed-signal design techniques, at both the circuit and layout level were described. The $\Sigma\Delta$ FDC would operate with an IF frequency of 112.5 MHz and a 5 MHz reference. The full scale input frequency deviation is 78.125 KHz. The power consumption, obtained through simulation, was found to be 38 mW.

The difference between input referred frequency error and input referred phase error, due to quantization error and analog noise sources in the switched capacitor block, was clarified. It was shown that the $\Sigma\Delta$ FDC is a second-order $\Sigma\Delta$ modulator on input frequency and a first-order $\Sigma\Delta$ modulator on input phase. The input referred frequency error, due to noise in the sampled-time phase detector and the switched-capacitor integrator, is first-order noise shaped. The input referred phase error, due to noise in the sampled-time phase detector and switched-capacitor block, is not noise shaped. Even if a higher order $\Sigma\Delta$ FDC architecture were used the input referred frequency error and the input referred phase error, due to noise in the analog block would not change, as the additional integrators would be placed after the sampled-time phase detector and first integrator. This means that, while the $\Sigma\Delta$ FDC is a good frequency detector, it makes a poor phase detector. The first-order differentiation of the noise in the analog block, when referred to the input, guarantees zero static frequency error. The flattening of the input referred phase error spectrum at low frequencies, due to noise in the analog block, results in non-zero static phase error. For both frequency detection and phase detection the input referred noise of the switched capacitor block becomes more significant with increasing OSR.

Results show that the $\Sigma\Delta$ FDC designed in this chapter could be used as an FM demodulator for voice communications or as a GMSK demodulator for channel bit rates of up to approximately 80 Kbs.

Chapter 6 Conclusions

6.1 Summary

In this thesis, two VLSI architectures for use in FM mobile radio were presented. The first was a frequency synthesizer and GMSK modulator, and the second was a receive path frequency-to-digital converter. When combined, these two circuits complement one another and are critical components in a radio transceiver, such as the frequency-hopping system presented in Chapter 2. Both of these architectures make extensive use of $\Sigma\Delta$ modulation techniques and digital circuits.

The frequency synthesizer, presented in Chapter 3, is a $\Sigma\Delta$ controlled fractional-N frequency synthesizer. This synthesizer includes a GMSK data filter which makes use of $\Sigma\Delta$ quantized tap coefficients. The design is partitioned into two integrated circuits. The first is a 0.5 μm bipolar chip which includes a multi-modulus divider, phase frequency detector, and part of the loop filter charge pump. The second is a 0.5 μm digital CMOS chip which includes a serial interface for synthesizer control, a GMSK data filter, and the fourth-order digital $\Sigma\Delta$ modulator used to control the divider. These two circuits were combined to form a transmit synthesizer which transmits GMSK data in the lower Instrumentation Scientific and Medical (ISM) band from 902-928 MHz, at a symbol rate of 62.5 Kb/s. This results in direct modulation at RF, within the loop bandwidth, without the need for the separate I and Q channels, ADCs, filters, and upconversion mixers normally required for this type of modulation. The design techniques and trade-offs that were considered in the design were described. The two chips, combined, consume 32 mW from a 3 V supply, with a 20 MHz reference clock.

The receive path frequency discriminator presented in Chapters 4 and 5 is a second-order $\Sigma\Delta$ frequency-to-digital converter. The input is instantaneous frequency, and the output is a single-bit bitstream whose average density represents the instantaneous frequency deviations of the input. The output bitstream is phase coherent and can be scaled and integrated in order to measure the phase of the input signal. It is important to note that this architecture combines analog-to-digital conversion and frequency discrimination in a single operation. Unlike previous divider based $\Sigma\Delta$ FDCs the novel architecture presented in this thesis employs a digital $\Sigma\Delta$ modulator in the feedback path, in order to reduce the fullscale input range of the FDC and reduce out of band quantization noise. This reduction in out of band quantization noise allows for the use of a simplified decimation filter in the baseband processor. An analysis of the architecture, explaining its operation, was presented. Such a $\Sigma\Delta$ FDC could be used as an inexpensive, highly linear, replacement for an analog frequency discriminator in an FM mobile radio system, or as an inexpensive GMSK data demodulator which facilitates the use of a digital matched filter for symbol recovery. The hardware design presented in Chapter 5 operates at an IF frequency of 112.5 MHz, with a fullscale input range of $\pm 31.25\text{ KHz}$. Simulation results show that an SNR of 32 dB can be achieved over a 100 KHz bandwidth, for a demodulated FM signal. The power consumption would be on the order of 38 mW. The contributions to the input referred frequency and phase error, due to noise in the analog block, were included in this analysis.

6.2 Future Work

The two VLSI architectures presented in this thesis both have immense potential for future work. Some possible areas that could be investigated are now described.

The transmit synthesizer architecture presented in Chapter 3 allows direct modulation at RF. Two main problems were encountered in the architecture. One was the inband phase noise floor of the synthesizer due to noise in the multi-modulus divider and the phase detector. The other is the limitation imposed on the modulation rate by the restriction that the modulation rate should fall within the loop bandwidth of the phase-locked loop. A method of predicting phase noise levels in the digital divider and the phase frequency detector would be valuable in the design of such a syn-

thesizer. In this way, the trade off between phase noise levels and power consumption in the divider and phase detector could be optimized. One possible method of predicting the phase noise in the divider is presented in Appendix A. Methods of increasing the loop bandwidth while maintaining stability could be explored. Beyond one or two Megahertz, methods of modulating the carrier outside of the loop bandwidth would probably be needed. Other, smaller, aspects of the synthesizer design that could be improved are the performance of the charge pump and loop filter, as well as the power consumption of the digital control chip.

While the inclusion of a digital $\Sigma\Delta$ modulator in the feedback path of the $\Sigma\Delta$ FDC does not reduce the inband noise floor of the FDC, it does open up a wide area of research. Different modulator feedback transfer functions can be explored as well as different architectures for the feedback $\Sigma\Delta$ modulator. This concept could also be applied to multi-bit voltage $\Sigma\Delta$ modulators. The main problem encountered in multi-bit $\Sigma\Delta$ modulators is that of undesired tones in the output spectrum due to mismatch in the output levels of the multi-bit feedback DAC. In this case, a digital $\Sigma\Delta$ modulator could be included as the feedback DAC, not to reduce the fullscale range, but rather to randomize the spectrum. Non receive path applications of the $\Sigma\Delta$ FDC could also be explored, such as frequency synthesis [Bax95], or any application that requires accurate measurement of instantaneous frequency.

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Appendix A Predicting Phase Noise in Digital Dividers

A.1 Predicting Phase Noise in Dividers

It has been shown in [Ega90], that the theoretical phase noise levels in a digital divider can be broken up into several different components which are dependent on the division ratio, the frequency of operation, and the input power. For the bipolar PLL design presented in this thesis, SPICE simulations could be used in order to try to predict the phase noise performance of the multi-modulus divider and phase detector described in the previous sections.

Figure A-1 shows a conceptual block diagram of the bipolar chip as far as phase noise is concerned. Since the required information is the overall phase noise contributed by each stage, all internal noise can be bunched together forming an equivalent noise at the output of each stage. The stages are the dual-modulus divider (DMD), the M-counter, and the phase-frequency detector (PFD). Each stage is assumed to be asynchronous with respect to the previous stages and, therefore, uncorrelated as far as noise is concerned.

Figure A-1: Phase Noise in the Bipolar Synthesizer Chip

Simulations can be performed using one ECL/CML gate from each stage. This is a reasonable approach to take since each stage is a synchronous circuit internally. Therefore, a single gate could be used to determine the phase noise contributed by a particular stage. Two sets of SPICE simulations must be performed. The first is an ac noise analysis of the gate with the inputs set to

the mid point of the switching characteristic (the meta-stable point). Although this is a linearized analysis, it is felt that this method will give a reasonable estimate of the total noise at the output of the gate. The result of this simulation is the frequency spectrum of the internal noise sources of the gate referred to its output. The units for this are V^2/Hz . The spectrum consists of two different regions. One region is due to the flicker noise of the transistors ($1/f$), and the other region consists of a white (thermal) noise region. The noise analysis would be run for a range of different supply voltages and operating temperatures. The second set of simulations to be performed is a transient analysis with an input signal applied to the gate. The slope of the output transitions is measured. The information from these simulations is then used to convert the results of the noise analysis into $(\text{sec})^2/\text{Hz}$. This information can be converted into rads^2/Hz using the following relationship.

$$N = \frac{(2\pi)^2(Fo)^2s^2}{\text{Hz}} = \frac{\text{rads}^2}{\text{Hz}} \quad (1-1)$$

Where Fo is the output frequency of the gate. These simulations must be performed for different amplitudes of input signal since higher amplitude signals will more closely approximate an ideal squarewave.

The phase noise information obtained from the two different sets of SPICE simulations can then be imported into MATLAB for combining and post-processing. Because the phase information is only sampled on the edges of the output signal, aliasing effects must be taken into account when considering the phase noise contribution of the bipolar chip to the PLL. This means that the noise spectrum for each stage must be folded around the output frequency before the noise from each stage can be combined. It can be assumed that higher frequency images (i.e., $2Fo$, $3Fo$ etc.,) are attenuated by the loop and, therefore, only one set of images must be folded. The resultant phase noise spectrum can then be imported into a mathematical spreadsheet where its effects on the phase noise of the synthesizer are determined.

A similar analysis of the noise in a single gate could be performed using a harmonic balance simulator such as LIBRA. This would allow a non-linear (i.e., large signal) noise analysis to be performed.

Appendix B Phase Error Cancellation Techniques for Fractional Division

B.1 Phase Error Cancellation Techniques

In this Appendix, two methods of performing fractional division using phase-error cancellation techniques are presented. While they are not used in this thesis, they are considered to be of interest and, therefore, are described here. The sampled time phase detector presented in Section B-2 is used in the $\Sigma\Delta$ FDC of Chapter 5.

B.2 A Combined Phase-Detector and DAC for Phase-Error Cancellation

As mentioned in Section 4.4.1, the main difficulty encountered in digi-phase is in matching the gains of the phase detector and the DAC shown in Figure 4-8. One possible method of doing this is to combine the phase detector and the DAC in such a way that both the phase detector gain and the DAC gain are set using a common reference. In the following architecture this reference is an integer multiple of the period of the input signal. This requires a sampled-time phase detector which is now introduced.

Figure B.1 shows a schematic of the sampled time phase detector and Figure B.2 shows the associated signal waveforms.

Figure B-1: Sampled Time Phase Detector

Figure B-2: Waveforms for Sampled Time Phase Detector

The phase detector operates as follows. When ϕ_1 is high, capacitors C1 and C2 are cleared of all stored charge by pulling them to an ac ground, in this case Vdd. The divider output d0 is set up such that it always has a pulse width equal to exactly X, where X is an integer, times the period of the input signal regardless of the division ratio N, as shown in Figure B.2. The reference frequency is a 50% duty cycle squarewave. During the time period between the rising edge of the divider output and the rising edge of the reference input, T_1 , a charge, Q_1 , equal to $T_1 I$, is integrated onto capacitor C1. When the positive edge of the reference arrives, Q3 is turned off and Q4 is turned on. This means that charge will be integrated onto capacitor C2 until the divider output becomes low. The total charge placed on C2 is equal to $T_2 I$. The total charge placed onto capacitors C1 and C2 is equal to $X T_{in} I$, proportional to X periods of the input to the divider. On ϕ_2 the output of the phase detector, taken at the collectors of Q3 and Q4, is dumped, through the switches shown, into a switched-capacitor filter (i.e., this could be the second integrator in a $\Sigma\Delta$ FDC.).

Differentially, the charge stored on C1 and C2 is proportional to the phase difference between the reference and the divider output.

The phase error will be zero when T_1 is equal to T_2 , which occurs when the reference rising edge is aligned with the centre of the divider output pulse. The usable range of this phase detector is;

$$\frac{X T_{in} 2\pi}{T_{ref}} \quad (B-1)$$

and the maximum differential charge is equal to $X I T_{in}$. Therefore, the phase detector gain, in Coulombs per radian, is equal to $(I T_{ref})/2\pi$. Due to the limited range of operation of the phase detector (phase detection range), for $\Sigma\Delta$ FDC applications, an additional acquisition loop would be required, in order to pull the input phase into the range required by the phase detector.

The phase detector shown in Figure B.1 can be modified, as shown in Figure B.3, to perform the phase-error cancellation required for fractional- δ division. On ϕ_1 the capacitors are cleared by shorting them to Vdd through the switches shown. Immediately afterwards, EN is pulled high,

turning on the $2Y$, where Y is an integer, switches shown at the collectors of Q3 and Q4. The phase detector operates in the same way as before except that now the charge is stored on two arrays of Y identical capacitors. Once again, the total charge stored on both arrays is equal to XI_{in} . Each individual capacitor now stores a charge equal to $(XI_{in})/(2Y)$. This means that a total charge proportional to X periods of the input signal has been split into $2Y$ discrete packets. By selectively choosing how many capacitors to dump into the integrator from each array, using the remainder in the DPA, the phase error can be cancelled. Differentially the charge stored on the capacitors is;

$$Q_d = I(T_1 - T_2) \quad (B-2)$$

T_1 and T_2 can be split up into a nominal value and an error component as shown below.

$$T_1 = \frac{XI_{in}}{2} + T_{error} \quad (B-3)$$

$$T_2 = \frac{XI_{in}}{2} - T_{error} \quad (B-4)$$

Therefore, $Q_d = 2IT_{error}$. T_{error} can be split up into two separate components, T_p and T_{Quant} . T_p is due to phase variations of the carrier and T_{Quant} is the error introduced by dividing by N or $N+1$ when the required division ratio was $N+\delta$. It is desired to combine Q_1 and Q_2 differentially such that T_{Quant} is cancelled. T_{Quant} is proportional to the remainder in the accumulator. The total charge is stored on two arrays of $2^M = Y$ capacitors. The differential charge is equal to;

$$Q_d = AIT_1 + BIT_2 \quad (B-5)$$

Figure B-3: Phase Detector/DAC

In Equation (B.5), A and B are variables whose values will be determined. Substituting Equation (B.3) and Equation (B.4) into Equation (B.2) and splitting T_{error} up into two components, we obtain;

$$Q_d = I((A + B)XTin + (A - B)T_{\text{Quant}} + (A - B)T_P)) \quad (\text{B-6})$$

T_{Quant} can be cancelled using multiples of Tin such that $Q_d = IT_P$. In order for this to occur, A - B must equal one. Therefore;

$$Q_d = I[XTin(2A - 1) + T_{\text{Quant}} + T_P] \quad (\text{B-7})$$

Here, A is a fractional value between 0 and 1 with a step size equal to 2^M . Referring back to the example of Table 4-3, we know that the error, T_{Quant} , is a fraction of Tin . Therefore, we can use

the remainder in the accumulator to select n out of Y capacitors, cancelling T_{Quant} . An important point to note about this circuit is that the phase detector gain and the DAC gain now match due to the normalization to the period of the input signal, which takes place in the phase detection process. The remainder in the accumulator is used to select a fraction of T_{in} in order to cancel out T_{Quant} , which is also a fraction of T_{in} . The total charge stored on the capacitor array is proportional to X periods of the input signal.

There are differential non-linearities present between the charges stored on individual capacitors in the array. Such a non-linearity results in undesired signal dependent tones in the output spectrum of the divider. The amplitudes of such tones depends on the degree of mismatch between elements. A way of reducing this problem is to randomly shuffle the delay elements such that the non-linearity becomes spread-out or averaged over the entire range of the capacitor array. The tones would, therefore, be whitened by this process, raising the noise floor of the divider output but eliminating tonal behavior. In this case, these differences are due to capacitor mismatch, and can be tightly controlled in a high quality IC process.

The architecture proposed here requires a large number of capacitors (i.e., 128 for a 5-bit DPA) consuming a large amount of chip area. However, the circuit is attractive in that the phase detector gain and the DAC gain are inherently matched, and switched-capacitor techniques can be employed for subsequent filtering.

It was found, through analysis and SPICE simulations of the phase detector and DAC circuit, that some fundamental problems exist in the architecture. Firstly, there is a common mode problem inherent in the way the outputs of the two capacitor arrays are combined differentially. The $2Y$ switches shown at the collectors of Q3 and Q4, implemented as CMOS transmission gates, each inject a “packet” of charge onto an integrating capacitor when they are turned off. If we consider the earlier phase detector, without phase error cancellation, the problem is not present.

$$Q_d = (IT_1 + Q_c) - (IT_2 + Q_c) \quad (\text{B-8})$$

Where Q_c is the injected charge, which is assumed to be the same for both capacitor arrays. This

will depend on device matching in the actual circuit. It can be seen, from the above equation, that the injected charge is cancelled differentially. However, if we now consider the phase error cancellation process, Equation (B.8) becomes;

$$Q_d = A(IT_1 - 2IT_2) + (2A - 1)Q_c \quad (\text{B-9})$$

It can be seen that the differential signal consists of a desired component and a noise component which depends on the remainder in the accumulator. A second-order effect has also been discovered. The charge injected on to the capacitor array is dependent on the input signal. These two problems were considered unacceptable by the author and no simple solution has been found to date. However, the phase detector shown in Figure B.1 is valuable and will be used in the $\Sigma\Delta$ FDC of Chapter 5. Unlike previous second-order $\Sigma\Delta$ FDC architectures, the sampled-time phase detector allows subsequent integrators to be implemented using switched-capacitor techniques rather than continuous time techniques, allowing more accurate and predictable transfer functions.

B.3 Delay-Locked Loop Based Phase Error Cancellation

The second approach investigated was phase-error cancellation in the phase domain, prior to the phase detector shown in Figure 4-8. In order to do this, it is necessary to break up a period of the input signal into N equal “packets” of phase. One method to do this is through the use of a delay-locked loop.

A delay-locked loop (DLL) [Chr96],[EASB94],[KKCK96] based fractional- δ divider is shown in Figure B.4.

Figure B-4: A DLL Based Fractional- δ Frequency Divider

The circuit, shown in Figure B.4, functions as follows. The output of the dual-modulus divider is fed into a set of N cascaded, tunable, delay elements. The output of the N th delay element is phase compared to the output of the divider which has been delayed by one period, 2π radians, of the input signal using the D-type flip-flop shown. The output of the phase detector is an error signal equal to the difference between the delay through the delay line and the delay of 2π radians introduced by the D-type flip-flop. This error signal is filtered using a charge pump and used to tune the delay elements. This negative feedback ensures that the total delay through the delay line is equal to one period of the input signal. The result is that one period of the input signal is split up into N discrete “packets” of phase, each equal to $2\pi/N$ radians. The digital-phase accumulator (DPA) has an input which is an M -bit word representing the desired division ratio (i.e., frequency). The number of bits in the accumulator is equal to M and the number of elements

required in the delay line is equal to 2^M . The output of the DPA is a digital phase ramp which controls a MUX used to address (choose) the required phase-shift from the delay line. The carry-out is used to toggle the DMD from N to $N+1$ or vice versa, in order to deal with phase roll-over. The resolution of the divider is equal to $F_{\text{ref}}/2^M$.

Although feedback forces the total delay through the delay line to be equal to one period of F_{in} , in the ideal case, there are differential non-linearities present due to mismatch between individual delay elements. Once again, random element shuffling could be used in order to reduce these effects. In this case, the shuffling would be difficult to achieve.

The delay elements shown in Figure B.4 could be implemented as “current starved inverters”. For high IF frequencies, which might be desired in the $\Sigma\Delta$ FDC (i.e., > 100 MHz), the individual delays required would become quite small, and the mismatch could become significant. This would limit the resolution possible in the divider.

While the DLL based divider is suitable for VLSI implementation, it is a complex analog feedback loop which would affect the reliability and complexity of the $\Sigma\Delta$ FDC. For this reason, this approach is not favored here.

IMAGE EVALUATION TEST TARGET (QA-3)

APPLIED IMAGE, Inc
1653 East Main Street
Rochester, NY 14609 USA
Phone: 716/482-0300
Fax: 716/288-5989

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