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A Narrowband Radio Receiver Front-End for Portable Communications Applications

by

John R. Long, B.Sc., M.Eng.

**A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfilment of the requirements for the degree of
Doctor of Philosophy**

**Department of Electronics
Carleton University
Ottawa, Ontario
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Abstract

A narrowband radio frequency receiver circuit for emerging hand-held personal communications systems is the subject of this thesis. A 1.9 GHz low-noise preamplifier (LNA) and doubly-balanced mixer that have been fabricated in a mature silicon BiCMOS process are described. A production silicon technology offers the advantages of low fabrication cost as well as the potential for a high level of circuit integration for this application. Monolithic transformers fabricated using coupled microstrip lines have been implemented to lower the operating voltage and the current consumed by both the receiver preamplifier and the mixer. Circuit models for inductors and transformers fabricated in a silicon VLSI technology have been developed and their accuracy experimentally verified as a part of this work.

Circuits incorporating monolithic transformers have been developed which take advantage of the benefits offered by narrowband circuits within a silicon technology. In addition to allowing a lower operating voltage, the transformer in the preamplifier is used as a low-loss feedback element. This has been exploited to achieve a low noise figure in the preamplifier, while maintaining the benefit of negative feedback to linearize the stage. The results of this study show that magnetic coupling in the feedback network offers a number of advantages over conventional, uncoupled preamplifier designs. Also, a monolithic transformer balun is used to efficiently couple the single-ended input signal from the LNA to a low power doubly-balanced mixer, and thereby realize a low level of harmonic distortion and a good noise figure.

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1. Introduction

This thesis explores the use of monolithic microstrip transformers and inductors on silicon, and demonstrates their application in narrowband receiver front-ends for low-power digital radio applications such as hand-held telephones.

Mobile cellular and home cordless telephones were the first examples of hand-held portable telephony in the marketplace, and these devices have spawned a marketing and R&D boom in the area of portable wireless communications [1]. Systems are evolving which will extend cordless voice and data services to consumers, both at home and in the workplace. To compete with wired telecommunications services, these wireless access systems must offer better voice quality and greater network availability than today's mobile cellular telephones, while at the same time being inexpensive, power efficient, rugged and lightweight [2,3]. Achieving these design goals will require low-power, highly integrated radio frequency (RF) designs which can be manufactured in large volumes and at a very low cost. These are the primary strengths of monolithic circuit integration, and there are strong indications that the discrete circuit solutions being offered today may be replaced by more highly integrated radios within the near future. The use of monolithic microstrip transformers on silicon will be shown in this thesis to assist in achieving the goal of a more highly integrated radio.

The key high frequency analog circuit components needed to implement a portable radio receiver have been chosen as an area for detailed study. A well-recognized standard for cordless portable communications, the Digital European Cordless Telephone (DECT) standard [4], was selected as the target specification for these circuit designs. In this thesis, a 1.9 GHz low-noise preamplifier (LNA) and doubly-balanced mixer that have been fabricated in a mature silicon BiCMOS process are described. A production silicon technology offers the advantages of low fabrication cost as well as the potential for a high level of cir-

cuit integration. Monolithic transformers fabricated as coupled microstrip lines have been implemented to lower the operating voltage and the current consumed by both the receiver preamplifier and the mixer. In addition to allowing a lower operating voltage, the transformer in the preamplifier is used as a low-loss feedback element. This has been exploited to achieve a low noise figure in the preamplifier, while maintaining the benefit of negative feedback to linearize the stage. Also, a monolithic transformer balun is used to efficiently couple the single-ended input signal from the LNA to a low-power doubly-balanced mixer, and thereby realize a low level of harmonic distortion and an improved signal-to-noise ratio when compared to the prior art in silicon technology.

Constraints imposed by cellular systems design, the radio receiver architecture, and RF circuit performance within the context of a radio receiver design will be outlined in this introductory chapter.

1.1 Cellular Radio Systems

Wireless communications systems, of which cordless telephones, pagers and mobile cellular telephones are familiar and successful examples, have grown enormously in commercial significance over the past decade. The convenience and efficiency of wireless access to communications networks has created a demand for a variety of wireless communications services, and it is expected that the systems used to deliver voice (telephony) and message (paging) services as well as wireless services to transport data between portable computers will continue to evolve rapidly over the next decade.

In a typical cellular radio system, a set of communications channels within a specified frequency band are allocated to the subscribers in a fixed geographic area or cell. These same frequency channels are available for re-use within another cell, if the physical separation between the cells is large enough to allow a channel of sufficient quality to be established. The limited band of frequencies available to the system can be shared by users over a wide geographic area by distributing the frequency allocation amongst the cells, and

then re-using these same frequencies in geographically distant cells. The concept of frequency re-use has been applied in other terrestrial and satellite communications systems, however, cellular radio systems have their own unique design and technology constraints.

The important specifications of some of the wireless telephone systems that have been standardized by various world organizations are outlined in Table 1-1. The present wireless telephony market can be characterized by two types of communications transceivers: high-power mobile cellular radios for use in vehicles, and low-power cordless radio telephones for use in people's homes [8]. In this context, "high-power" implies transmitted power on the order of 1 W or more while "low-power" refers to transmitter powers on the order of 1 to 100 mW. The digital cellular systems such as GSM, IS-54, IS-95 and JDC are designed for highly-mobile or vehicular telephony applications. Hand-held terminals are offered for the added convenience and utility that this offers to the digital cellular user, although the talk-time of a battery powered set is limited to only a few hours between recharging cycles because of the high power levels required for transmission.

All of these cellular and cordless telephones use digital modulation of the RF carrier in order to improve on the limited capacity of the older analog cellular systems. The cellular systems use sophisticated coding techniques which make more efficient use of the frequency spectrum than the low-power cordless systems. This helps to maximize the capacity of the expensive base stations required in a cellular system with a large cell size.

There are significant differences between the radio systems designed for "low-power" personal communications (often referred to as PCS) and the digital cellular systems designed for mobile communications listed in Table 1-1. A digital cellular system is designed to support users roaming over a wide geographic area in (potentially) fast moving vehicles, and therefore each cell in the network must be large, usually over three kilometres in diameter and can be as large as several tens of kilometres. A cell site in an urban area must house the transmit, receive and switching equipment in an environmentally controlled structure, and the site requires an antenna mounted on a mast high enough to cover the entire cell adequately. Thus, the cell site can be quite costly given the high cost of land

System	Digital Cellular Systems				Low-Power Systems			
	IS-54	GSM	JDC	IS-95	DECT	PHP	CT2/ CT2+	Belcore UDPC
Multiple Access	TDMA/ FDMA	TDMA/ FDMA	TDMA/ FDMA	FDMA/ CDMA-SS	TDMA/ FDMA	TDMA/ FDMA	FDMA	TDMA/ FDMA
Frequency Band								
Base Tx (MHz)	869-894	935-960	810-826	869-894	1881-1897	1895-1907	CT2: 864-868 CT2+: 930-931 and 940-941	?
Mobile Tx (MHz)	824-849	890-915	940-956	824-849				
Duplexing	FDD	FDD	FDD	FDD	TDD	TDD	TDD	FDD
Ch. Spacing (kHz)	30	200	21	1250	1728	300	100	350
Modulation	$\pi/4$ - QDPSK	GMSK	$\pi/4$ - QDPSK	BPSK/ QPSK	GMSK	$\pi/4$ - QDPSK	GMSK	$\pi/4$ - QDPSK
Portable Tx Power. Max/Avg.	600mW/ 200mW	1W/ 125mW	-	200mW	250mW/ 10mW	80mW/ 10mW	10mW/ 5mW	200mW/ 20mW
Frequency Assignment	Fixed	Dynamic	Fixed	-	Dynamic	Dynamic	Dynamic	Autono- mous
Power Control								
Handset	Yes	Yes	Yes	Yes	No	-	No	Yes
Base	Yes	Yes	Yes	Yes	No		No	No
Speech Rate (kBits/s)	8	13	8	1-8(var.)	32	32	32	32
Speech Channels/RF Channel	3	8	3	-	12	4	1	10
Channel Rate (kBits/s)	48.6	270.833	42	1,228.8 (chip rate)	1152	96	72	500

Table 1-1: Summary of the worldwide standards for wireless telephony [5,6,7].

and infrastructure in an urban environment. The digital cellular handsets have a high power output (approximately 1W) in order to communicate with a remote base station at the edge of a large cell, which, for a limited size battery in a hand-held portable transceiver, requires frequent recharging of the battery. The low-power personal radios are incompatible with these higher-power digital cellular sets because of the difference in co-channel interference levels produced. Hence, there are two types of portable radios that are evolving as separate systems in different frequency bands (e.g., DECT and GSM).

A portable handset designed for a vehicular cellular application is also expensive, not only because of the complexity of the terminals themselves, but because of the high charge per call levied to cover the cost of the system infrastructure. The number of users per cell can be large in densely populated areas, and to provide as many channels as possible in the allocated bandwidth for the service, complex speech coding and error correction techniques are used in digital cellular systems [9]. However, the voice quality of a digital cellular telephone remains inferior to the quality of the service available from the wired telecommunications network.

The "cordless telephone" is a mass-market consumer item that is different from the portable cellular telephone handset described above. Cordless telephones were originally conceived as a consumer item for use in the home, and function like a wireless replacement for the cord on a conventional telephone terminal that is connected to the wired network. The first generation cordless telephones are limited in range to just a few metres from a single base station. However, the demand for cordless telephone terminals, such as those designed for personal use in the home (over 75 million units sold in North America), outweighs the demand for vehicular cellular units (approximately 25 million subscribers in North America). Therefore it is expected that there will be a strong market demand in the future for communications products that offer the mobility and convenience of the cordless terminal at a low cost [10]. This is the motivation behind the development of low-power standards for pedestrian use, such as the British CT-2 standard for the TelePoint wireless access system listed in Table 1.1. Other low-power standards such as DECT (dig-

ital European cordless telephone), the Japanese personal handy phone (PHP [11]) and Bellcore's proposed universal digital personal communicator (UDPC), are also aimed at applications with limited or low-speed mobility for low-power digital cordless systems. These devices are designed to compete with the wired network and therefore they must provide higher quality communications (i.e., better voice quality and greater network availability) than today's vehicular cellular systems.

The low-power cordless terminal is envisioned as a small, lightweight, low-power and low-cost device that can be carried and used in and around office buildings, industrial complexes and city streets (i.e., not fully mobile, but rather pedestrian or walk-about access to the wired network). In an office environment, the system might be used to offer wireless access to a PBX, and consequently the cell size must be small to accommodate the large number of potential users within a small geographic area [12]. The size of each cell could be less than 400 metres in diameter and the relatively small and inexpensive base stations might be housed unobtrusively on utility poles or attached to urban and suburban buildings. Decreasing the path distance of the radio link by shrinking the cell size allows a lower transmit power for communication between the terminal and the base station. The average radiated power will be on the order of milliWatts (10-20 mW), which leads to a long battery life and will help to safeguard users from the unknown health effects of strong electromagnetic fields. A personal communications system (PCS) is intended to be an evolution of the cordless telephone terminal and hence the quality of service must be close to that to the wireline or conventional telephone service. In order to achieve this goal, simple but high quality speech coding algorithms (e.g., ADPCM) are used to maintain voice quality and conserve power that is consumed in processing of the digital bit stream. Thus, the PCS service will distinguish itself from the digital cellular service with voice quality (more intelligible voice, less noise and crosstalk) and/or service quality (better availability of the network than mobile cellular and a lower cost per call), and by offering a smaller, cheaper terminal.

In addition to telephony, applications such as data communications networks for

packet data, wireless interconnection of equipment in an office or manufacturing environment and private data networks are areas where wireless data communications technology could be applied [13]. A wireless office information network is desired by business and manufacturing concerns that want to avoid the high cost of reconfiguring voice and/or data networks. The instrument, scientific and medical (ISM) frequency bands at 900 MHz and 2.5 GHz have been opened for wireless data applications such as private telecommunications exchanges (PBX), local area data networks (LAN) or private fire, safety and security networks. Data rates for these applications vary from the low kBit/s range to over 2 Mbits/s for LANs, such as the proposed Hiperlan in the 5.15-5.3 GHz band. Portable equipment designed for these portable telephony and local-area data communications networks will require low-cost radio transceiver parts that can be manufactured in large volumes and which consume little power. This is a natural market for highly integrated monolithic circuits at RF.

1.2 Radio Transceivers

In a portable cordless telephone application, the information being relayed over the channel is either voice, or data which originates at baseband. The radio transceiver is used to access the portion of the frequency spectrum that has been allocated for the communications service, for example, the 1.9 GHz band for DECT cordless phones. Time and frequency division multiplexing are used to maximize the efficiency of all the low-power cordless systems that are listed in Table 1-1. Frequency multiplexing of the channels at the transmitting end of the system is achieved by modulating each baseband signal onto a radio frequency (RF) carrier. At the receiving end, each channel is shifted back to its original place in the spectrum by demodulation.

An alternative modulation scheme to the combined TDMA/FDMA systems is based on code-division multiple access (CDMA), such as the IS-95 digital cellular modulation scheme [14,15]. In a CDMA system for telephony, many calls share the time slots and transmit using the entire frequency band. As the number of users grow, the interference

level across the band grows and the bit-error rate for all users in the system increases. Theoretically, the use of CDMA rather than TDMA will allow more users to communicate within a given frequency band, although this has not yet been thoroughly proven in practice [16,17].

The electronic processing of the RF signal needed for proper reception is common to all of the modulation methods. Conceptually, the radio receiver functions as a tunable bandpass filter, centred at the radio frequency, which selects only the desired channel for demodulation. However, for both technical as well as economic reasons it is impractical to construct a tunable filter operating in the radio frequency band that has a passband matching the narrow channel bandwidth. Thus, frequency translation of the signal at the receiver is commonly used to shift the desired signal to a predetermined and fixed frequency for both filtering and amplification before demodulation.

The two transceiver architectures that are considered viable for portable telephony applications are shown in the block diagrams of Figure 1-1. It should be noted that in many systems, complex signals consisting of both in-phase (I) and quadrature (Q) components are used to convey binary information from the transmitter to the receiver. Thus, some of the functional blocks in the transceiver may be required to handle both the in-phase and quadrature components of a complex modulated signal. Signal paths which could be complex (i.e., separate I and Q) are indicated by a double line on the Figure.

The conventional superheterodyne transceiver (Figure 1-1a), uses a high quality bandpass filter centred at an intermediate frequency (IF) to select the desired communications channel. The radio frequency signal received at the RF input to the mixer is multiplied by the local oscillator (LO) signal and it is thereby translated to an intermediate frequency (IF) band. This facilitates signal processing at a lower frequency where higher quality filters and amplifiers can be economically constructed. In this down-conversion process from the RF to the IF bands, the received signal-to-noise ratio is degraded by the mixer, and consequently a low-noise preamplifier is placed ahead of the mixer in the receive chain to suppress the noise introduced by the mixer. A bandpass preselection filter, or

(a) Heterodyne (Dual-Conversion IF) Transceiver

(b) Homodyne (Direct-Conversion) Transceiver

Figure 1-1: Portable radio transceiver architectures.

image-reject filter, is required in a superheterodyne system to attenuate potential interferers in the radio spectrum that are also down-converted to the IF by the mixing process. Any filtering of the incoming RF signal must remain broad enough to allow all of the channels being used in the system to be shifted as a frequency block to the intermediate frequency. Attenuation of the interferers within the image frequency band, of between 80 and 100 dB is typically required in a digital cellular system [18]. Image-reject filters are normally placed at both the input and output of the receiver preamplifier in order to reduce the effect of the filter's insertion loss on the receiver noise figure.

After filtering and amplification at the IF, the received signal in Figure 1-1(a) is then demodulated. An intermediate frequency is also used in the transmit section, because single-sideband modulation of the transmit carrier is normally employed to maximize the number of users which can be served by the system. The IF filter in the transmit path prevents any residual of the unwanted sideband and the up-converting local oscillator signal (TxLO_1) at the up-converter output from reaching the antenna.

The direct-conversion or homodyne architecture in Figure 1-1(b) is an alternative to the heterodyne scheme. On the transmit side, the baseband signal directly modulates the RF carrier, while in the receive channel, the signal from the antenna is directly converted to baseband where all of the filtering must be done to select the desired channel. It should be noted that in the RF section of the receiver, the front-end active components, which are the low-noise preamplifier (LNA) and the down-converting mixer, are common to both the heterodyne and homodyne schemes. However, the homodyne architecture does put some additional performance constraints on the LNA and mixer. Leakage of the receive local oscillator signal (RxLO) via circuit parasitics from the mixer, through the LNA, and back to the antenna will be radiated and appear as an interferer to other receivers that are operating nearby. Therefore, the port-to-port isolation of the mixer and the reverse isolation of the LNA must be sufficiently high to minimize any such impairment upon the direct-conversion receiver performance. Also, in a homodyne system, the single-sideband demodulation must be performed by the down-converting mixer, rather than after the first

IF as shown in Figure 1-1(a) for the heterodyne receiver. The single-sideband down converter is considerably more difficult to build at the RF than at a lower IF, so the performance of the direct conversion receiver usually suffers as a result. Another source of performance impairment in direct-conversion receivers is dc offset that can arise from a number of sources within the receiver. Good isolation from spurious signals is necessary to minimize the effects of these offsets upon the baseband signal demodulation and detection circuitry.

The scope of this thesis will be limited to a study of active circuitry required to implement a low-power receiver front-end for portable cordless communications applications. Thus, only the low-noise preamplifier, down-converting mixer and image filtering requirements (i.e., as required for the heterodyne receiver) will be examined in further detail. The design of the power amplification stages in the transmitter, synthesizers and the other RF hardware associated with the transceiver are beyond the scope of this study and will not be considered further.

The preamplifier and mixer are basic circuit blocks that are common to both the homodyne and heterodyne transceiver architectures. More elaborate signal processing circuitry, such as the single-sideband demodulator needed for direct-conversion radios, can be developed from these basic amplifier and mixer circuit blocks. Also, it should be noted that a mixer design developed for the receiver could be adapted for use in the transmit path without modification, provided that the bandwidth of the mixer output were sufficient to cover the desired transmit frequency band for the radio. This is because the performance specifications for the up-converting RF mixer in the transmit portion of the transceiver are less demanding than the performance requirements for the receiver down-converting mixer.

1.3 The Radio Receiver Front-End

The signal processing functions that are performed by the front-end of a typical porta-

ble radio receiver will now be discussed in further detail. Two possible implementations of an IF-based radio receiver are illustrated in the block diagram shown in Figure 1-2. The receiver shown in part (a) of the Figure uses a bandpass filter connected between the receiver preamplifier (LNA) and the first down-converting mixer to reject spurious signals at the "image" of the desired signal band. The image band differs from the local oscillator frequency by the same amount as the desired RF signal band. Analog multiplication implied by the down-conversion process in a heterodyne receiver will translate signals from both the image and RF bands to the desired intermediate frequency. The unwanted interference from spurious signals in the image channel can be removed by a filter inserted in the RF signal path ahead of the mixer. A bandpass filter is commonly used for image-reject filtering, but a highpass or a lowpass filter could also be used depending upon whether the LO frequency lies above or below the desired RF band of frequencies.

It should be noted that interfering signal levels can be large compared to the received signal strength, and therefore the IF filter after the mixer in a heterodyne receiver is normally placed ahead of any amplification stages, as shown in Figure 1-2(a). This ensures that saturation of the IF circuits does not occur, and distortion of the received signal is thereby minimized.

An alternative to the image-reject filter design is a single-sideband demodulator or image-reject mixer design for the receiver front-end as shown in Figure 1-2(b). An image-reject filter is also shown in the Figure, and this filter provides some additional bandpass shaping of the received signal spectrum. The filter can be lower in quality than the image filtering used in the heterodyne architecture (Figure 1-2(a)). In the image-reject mixer design, demodulation with quadrature phase local oscillator signals is used to force cancellation of spurious components from the image frequency band. This approach adds additional cost and complexity to the receiver design and requires careful matching of components in order to achieve good performance. However, in a fully-monolithic implementation this added design complexity may be less of a problem than the technical difficulties involved in an on-chip realization of a high-quality filter for image rejection.

(a) Image-Reject Filter in Rx Front-End

(b) Image-Reject Mixer in Rx Front-End

The homodyne receiver, which converts the received signal directly to baseband, can be viewed as a simplification of the image-reject mixer design. The IF channel select (bandpass) filter would be replaced by a lowpass filter in a direct conversion receiver implementation and the image-reject bandpass filter is no longer required.

The attenuation required in the stopband of an image-reject filter will depend upon the IF chosen for the system. Choosing a high IF will relax the image filter requirements, however, the fractional bandwidth of the channel select filter decreases, which makes the IF filter more difficult to realize. A low-quality communications link might use a three-pole image-reject filter in the receiver front-end at an IF of approximately 100 MHz. One "pole" implies one L-C section of a bandpass filter, and excludes components required for impedance matching purposes. A 900 MHz ceramic resonator bandpass filter has an insertion loss of approximately 1 dB per pole in the passband. The link performance degrades when interference from the image band causes errors in the data bits detected by the receiver. This may even result in a complete failure of the link under certain conditions. Typically, attenuation of the image by 100 dB is considered necessary in telephony applications to ensure adequate bit-error performance and service continuity under all reasonable operating conditions. A five-pole bandpass filter will give 100 dB of attenuation in the image band if a 100 MHz IF is assumed.

The image-reject mixer depends upon close matching of the circuit components and fine control of the amplitude and phase of the signals being processed in order to achieve high attenuation of the unwanted sideband. A phase difference of less than 1 degree between quadrature signals and relative amplitude control within 0.1 dB is needed to achieve 40 dB of image rejection by the mixer. This can be achieved in discrete modulators by careful trimming of circuit components, and it is expected that a monolithic implementation could achieve comparable performance if carefully designed, since close matching of component performance is possible on-chip (i.e., within a few percent for a monolithic circuit). It should be noted that the attenuation of the image band does not depend upon the choice of IF, which is not the case for a passive image-reject filter, where

the filter Q-factor must increase when a lower IF is selected. Nevertheless, a combination of image-reject mixing and image-reject filtering is normally required to achieve the high degree of stopband rejection demanded in a communications channel.

The image-reject filter is normally partitioned around the first gain stage, with some filtering placed both ahead and following the preamplifier. Placing the filter after the LNA limits the effect that the filter's insertion loss has on the overall receiver noise figure. Also, filtering of out-of-band spurious components using a bandpass filter placed before the preamplifier is normally used to eliminate any interference which might otherwise saturate the receiver preamplifier. This is an important side benefit of bandpass filtering of the image, which must be carefully considered if other methods of image rejection are considered for the receiver. The design and specification of the filtering required for image rejection in the receiver is beyond the scope of this work and will not be considered further.

Radio architectures must be tailored to a design specification for the overall communications system. For the purposes of this research, it is useful to have a practical specification from which to define the level of performance required from the radio receiver front-end circuitry. Monolithic IC designs can then be devised which will meet or exceed these target specifications. A radio receiver design to meet the DECT specification will therefore be described in the following section.

1.4 A DECT Radio Receiver

Any discussion of the hardware required to implement a radio receiver must consider the applications context and the desired level of performance required for the design. The DECT standard (refer to Table 1-1) represents a well accepted benchmark that is expected to form the basis for the next generation of low-power cordless communications products in both Europe and North America. A low-power receiver front-end that meets or exceeds the requirements of the DECT specification is therefore proposed as the systems context for further study of the receiver implementation.

The intent of system standardization is to encourage product development by equipment manufacturers. Products built to comply with the DECT specifications will open up a market for inexpensive portable voice and data communications, and hence DECT hand-held terminals must be physically compact, lightweight, low-cost and have a long battery life. The battery size of a small, lightweight set is limited, and a long talk-time between battery recharging requires low-power circuitry within the transceiver unit. This implies that the set must be optimized for low power consumption, not simply power-controlled for low power consumption during idle periods. These are attributes that the vehicular cellular terminals can approach but cannot effectively cover with their present system designs. Today's vehicular cellular radio sets, which are power-controlled so that the consumption is reduced to the mW level during idle periods, cannot be small in size or lightweight, because the high-power electronics require heat sinks, shielding and heavy batteries. Because of these size and weight restrictions, there is a significant difference between the transmit power capabilities of mobile sets for vehicular use and personal communicators designed for use by pedestrian and stationary users, as shown previously in Table 1-1.

The size, power and cost constraints as well as the high manufacturing volume anticipated for PCS products, such as a DECT-compatible cordless telephone, can benefit from greater RF circuit integration than is used in today's hand-held digital cellular telephones. Economical and reliable semiconductor devices have been an important ingredient in the development of mass market consumer electronics products, and DECT portables will rely upon IC technology to achieve cost, size and performance targets. The sophisticated control of frequency allocation and frequency re-use in microcellular systems will require low-cost, low-power VLSI digital logic. However, integrated circuits that perform well at high frequencies will also be needed in order for the portable cordless telephone to meet its system specifications and succeed in the marketplace.

The design objective for this work is a radio receiver front-end that will meet the published specifications for a DECT portable set and consume as little power as possible. The

most important specifications for the front-end of a heterodyne receiver are image rejection and dynamic range. Image rejection is dependent upon the quality of the RF filters that are available and the intermediate frequency selected for the design. An intermediate frequency of 110 MHz has been recommended for DECT, which will require state-of-the-art passive filtering technology in the receiver front-end to achieve image rejection on the order of 80 to 100 dB. This is because the image and 1900 MHz RF signal bands are separated by only 220 MHz when a 110 MHz IF is chosen. The scope of this work will be limited to the design of the low-noise preamplifier and the down-converting mixer, and therefore the design of the image rejection filter and the selection of the IF will not be considered further. A total insertion loss of 5 dB will be assumed for the passive image-reject filters and the transmit/receive duplexer used in the receiver system design.

The spurious free dynamic range (SFDR) of the receiver is the other important performance specification which the radio front-end circuitry must satisfy, and it is common to both the heterodyne and homodyne architectures. The SFDR is defined by the difference between the overload point and the minimum discernible or acceptable signal level at the RF input. The minimum input signal level or receiver sensitivity is determined by the receiver noise figure (NF), which can be estimated from Friis' formula [19]. The upper limit of the receiver dynamic range is usually determined by the mixer's distortion and gain compression characteristics, if the preamplifier gain is sufficient to adequately suppress the mixer noise. The performance of the receiver front-end required by the DECT system [4,6] will now be outlined.

Sensitivity defines the lower end of the receiver dynamic range, and in a digital communications system it is defined by the signal-to-noise ratio at the data detector that is needed to achieve some arbitrarily specified bit-error performance. The DECT standard specifies that the minimum detectable signal power at the antenna is -86 dBm. A bit-error rate (BER) of one error in one thousand bits received (i.e., 10^{-3}) is allowed at this input power. Binary detection of the received bit stream theoretically requires at least a 12 dB signal-to-noise ratio (i.e., bit energy-to-noise ratio, or E_b/N , of 12 dB [20]) at the detector

input. An E_b/N ratio of 14 dB will be assumed in the following calculations in order to account for imperfections in the demodulator.

The receiver minimum detectable signal (MDS, in dB) is given by the following equation,

$$\text{MDS} = \text{Receiver Noise Floor} + \text{Receiver Noise Figure} + (E_b/N) \quad (1.1)$$

When proper noise shaping of the received signal is used, the receiver noise bandwidth will be equal to the bit-rate of the received data stream, which is 1.152 MBits/s for a DECT terminal. Given that the noise floor for a properly matched 50 Ohm receiver input is -174 dBm/Hz, the total noise power in the 1.15 MHz receiver bandwidth will be 60.6 dB above this level, and this results in a receiver noise floor of -113.4 dBm. The overall receiver noise figure can now be computed using equation 1.1 as

$$\text{Receiver Noise Figure} = -86 \text{ dBm} + 113.4 \text{ dBm} - 14 \text{ dB} = 13.4 \text{ dB} \quad (1.2)$$

This is the maximum possible noise figure for the DECT receiver chain in order to meet the minimum detectable signal specification. In a practical receiver some additional margin must be added to account for component variations in manufacture, temperature, etc.

The receiver noise figure (NF) is the parameter used by radio engineers to specify degradation in signal-to-noise ratio caused by all active or passive circuitry in the receiver chain, and is always expressed in dB. The noise factor, F , is the linear equivalent of the noise figure, and it is given by the following expression,

$$F = \frac{\text{Input Signal-to-Noise Ratio}}{\text{Output Signal-to-Noise Ratio}} \quad (1.3)$$

For a practical RF component which adds noise to the signal, the output signal-to-noise ratio (SNR) will be lower than the input SNR, which results in a noise factor greater than unity.

Receiver circuits must be as efficient as possible in transferring the power received at the antenna to the signal detector, and therefore optimum power transfer is usually desired between the stages in the receiver chain. The one common exception to this is the low-noise preamplifier, which may require a source impedance that is carefully chosen in order to minimize the amplifier noise figure. This choice of source impedance will generally not be the same as the impedance chosen for the optimum transfer of power.

While noise puts a limit on the lower level of the signal which can be received, an upper limit is imposed by the finite power supply voltage used for active circuits and the non-linear transfer characteristic inherent in semiconductor devices. As the input signal increases in amplitude, these limitations cause distortion, compression and saturation of the signal being processed by the receiver chain. Intermodulation distortion caused by non-linearities of the receiver components can result in spurious components being generated which fall inside the receive channel bandwidth. In such cases, the interference caused by the distortion products can be mistaken for the desired signal and disrupt the radio link.

Even-order intermodulation products are normally found at frequencies well above or below the signals which generated them and are usually of little concern. The odd-order distortion produced by a two-port RF component will give rise to distortion products which can mask or interfere with the desired signal in a typical narrowband radio channel. The third-order products are the strongest of the odd-order products that can be generated, and they can lie very close to the signals which generated them in frequency. Consequently it is difficult or impossible to remove these spurious signals by filtering. The third-order non-linearity is customarily characterized by a specification called the third-order intercept point. The third-order intermodulation distortion (P_{IM3}) generated for a given input signal power (P_{IN}) can be predicted from the third-order intercept point (P_{IP3}) using the following equation,

$$P_{IM3} = 3P_{IN} - 2P_{IP3} \quad (1.4)$$

where all powers are expressed in dBm.

The receiver intermodulation performance is measured using three sinusoidal test signals: a modulated RF signal in the desired channel and two interferers in two other DECT channels. Of the two interfering signals, one is modulated with a DECT signal and the other is a pure tone. Appropriate frequencies are chosen for the interfering signals such that one of the third-order intermodulation products will appear as a DECT modulated signal in the desired RF channel.

The signal levels for the desired signal and interferers for a DECT handset are given in the specification as -76 dBm and -46 dBm, respectively. The specification also states that the level of co-channel interference produced by the receiver must be 10 dB below the desired signal, or -86 dBm. The receiver third-order intercept can be calculated using equation 1.4, by noting that P_{IN} is the interfering signal power and P_{IM3} is the in-band or co-channel interference which is generated, so that

$$P_{IP3} = 1.5P_{IN} - 0.5P_{IM3} = 1.5(-46) - 0.5(-86) = -26dBm \quad (1.5)$$

Thus, the third-order intercept point for the receiver when referred back to the receiver input at the antenna must be greater than -26 dBm in order to meet the DECT specification.

Odd-order non-linearities will also generate signal components at the fundamental frequency, leading to a non-linear transfer characteristic for the fundamental. The loss of linearity is observed as saturation of the transfer characteristic at high input signal levels and a reduction in gain that is called gain compression. Since the amount of compression is proportional to the amplitude of the signals which are within the passband, it is possible that amplitude modulation present on an undesirable or interfering signal will cause amplitude changes (cross-modulation) in the desired output signal. Saturation of an amplifier by a large signal causes a decrease in gain for all signals being amplified, and a large out-of-band interferer can cause a reduction in the receiver sensitivity if it is not suffi-

ciently attenuated.

An example of a link budget for a receiver which meets the DECT specifications is shown in Figure 1-3. The loss in the transmit/receive switch or duplexer connected to the antenna is assumed to be 1 dB. A 5 pole image-reject filter with an attenuation of approximately 5 dB in the RF signal passband has been assumed. The image filtering is spread amongst bandpass filters placed before and after the receiver preamplifier in order to limit degradation of the overall receiver noise figure caused by attenuation before the receiver gain stages. A modest gain of 13 dB has been assumed for the low-noise preamplifier with a noise figure of 3 dB. This gain can be easily realized with a single stage of amplification drawing a small amount of current, which will limit the power consumption of the receiver front-end. A higher gain preamplifier would suppress the noise introduced by subsequent stages in the receiver, however, the input signal power which causes overloading of the mixer input decreases as the LNA gain is raised. The linearity of the receiver front-end is usually dominated by the mixer performance. A low conversion gain of 3 dB with a single-sideband (SSB) noise figure of 10 dB has been assumed for the mixer. This noise figure performance is state-of-the-art for silicon technology at 900 MHz. A 4 pole channel select IF filter has been assumed, which would most likely be implemented using a surface acoustic wave (SAW) resonator. An insertion loss of 4 dB can be achieved when the filter is properly impedance matched to both the mixer and IF gain stages. The specifications for the IF amplifier/demodulator are representative of what can be realized with current silicon technology [21,22]. The signal at the IF filter output is amplified and then demodulated to recover the binary-coded information from the GMSK signal at the IF, typically with an FM discriminator. In the process, the signal is converted back to a base-band binary format where it can be detected by a simple level comparator and then re-synchronized to the local system clock.

It can be seen from Figure 1-3 that the overall noise figure of the receiver is set by the front-end components, because high gain in the IF stages ensures the receiver SNR is not significantly affected by components placed after the first down-converting mixer (i.e.,

Figure 1-3: DECT receiver link budget.

point 'E' in the Figure).

An overall signal-to-noise ratio of approximately 18 dB at the binary detection circuit is predicted for the receiver for the DECT minimum input signal level of -86 dBm at the antenna, which is 4 dB larger than required to achieve the desired bit-error rate of 10^{-3} . This gives the design some margin which can be used to cover fluctuations in performance introduced by system operating conditions, temperature and component variations.

The third-order intercept of the receiver components is also listed in Figure 1-3. Passive components such as the duplexer and bandpass filters have a very high linearity when compared with the active components (intercept points on the order of 60 to 100 dB for a filter) and so these datapoints are not shown. The IF filter attenuates the adjacent channel interferers such that the linearity of the IF amplifier and discriminator do not have a significant impact on the receiver linearity. In this case it is the linearity of the mixer and preamplifier that dominate the receiver performance. The intercept point of the mixer referred back to the antenna input is -7 dBm, which sets the intercept point for the receiver overall. This is well above the DECT specification of -26 dBm calculated in equation 1.5 and results in an overall dynamic range for the DECT receiver shown in Figure 1-3 of 83 dB.

1.5 Summary

Research work toward the development of a DECT-compatible receiver front-end is the subject of the remaining chapters of this thesis. Chapter 2 outlines the advantages of narrowband circuits for RF receiver applications. In this discussion, narrowband design is compared to the more conventional broadband design techniques which have traditionally been used in silicon IC technology for receiver front-ends. Viable inductive component designs that can be integrated in a production silicon VLSI technology are vital to the development of narrowband monolithic ICs. In order to efficiently design and manufacture monolithic circuits, computer models must be available which predict the behaviour of the components that will be fabricated in a VLSI process. The results of analytical and

experimental research work in this area will also be included in the second chapter. Low-noise preamplifier and mixer designs are described in more detail in Chapters 3, 4 and 5. Other silicon IC designs are presented which can be compared to the results achieved through the use of narrowband circuit design techniques for these components. Experimental measurements are presented in these chapters for passive and active circuits fabricated in Northern Telecom's 0.8 μm BiCMOS process.

2. Design Considerations for Silicon RFICs

The design and implementation of RF and microwave circuits in silicon technology will be discussed in this chapter, although it should be understood that silicon integrated circuit technology has not been widely used for analog applications in the radio and microwave range of frequencies. This is primarily because transmission lines are required to implement high frequency analog circuits, and these structures perform poorly on semi-conducting substrates, such as those used to manufacture silicon ICs. Narrowband or tuned RF and microwave circuits fabricated in planar technologies make extensive use of the transmission line to realize an inductance, either as a lumped inductor or as a transformer. The limitations imposed by silicon technology upon the performance of these inductive components must therefore be accurately modeled and characterized in order to optimize on-chip resonant circuitry for the best possible performance.

The motivations for using a monolithic circuit technology rather than discrete or hybrid technologies (i.e., discrete components mounted on a common substrate material) will be examined in the first section of this chapter. The main benefit is the low cost of manufacturing a large number of circuits that have reproducible performance characteristics. This discussion will also outline the renewed interest in silicon as the technology base for a 2 GHz radio receiver front-end, rather than a more conventional MMIC technology based upon III-V semiconductor materials such as gallium-arsenide (GaAs).

The rationale behind the choice of narrowband rather than broadband design methods for low-cost cordless portable radio receivers will then be outlined. One of the objectives of this research work is to develop narrowband circuits which can operate within the limitations imposed by silicon technology. Broadband circuits are commonly seen in the textbooks and the literature which describe silicon IC design, however, narrowband circuits can offer better performance when used in an RF receiver [23,24]. Choosing a narrowband

design approach will require an on-chip inductance, which leads to a discussion of transmission line inductors and transformers, their characteristics, and circuit models for their simulation and design.

A suitable model that describes the electrical behaviour of the monolithic inductor and transformer at RF is needed for computer simulation and optimization of tuned circuits fabricated in silicon technology. Circuit simulation models for these components will be described in the latter sections of this chapter. Monolithic inductors and transformers are fabricated from microstrip transmission lines, and the conductive silicon substrate has a detrimental effect on the transmission line performance as the operating frequency increases. A sophisticated circuit model is required to accurately characterize the distributed parameter nature of the microstrip inductor over a wide frequency range. However, a simplified or compact version of this model (i.e., a model with the minimum possible number of circuit elements) is also needed for hand calculation and to facilitate optimization of more complex RF circuit structures. For efficient optimization, the compact model should be easily derived from the more accurate and complex model structure. Both complex and compact model structures will be described.

As a part of this research work, there has been a considerable effort made to develop accurate and efficient models for inductors and transformers that can be used in a commercial circuit simulator. The results of this modeling effort will be presented in the remaining sections of the chapter. The performance predicted by the model will be compared to experimental measurements of devices fabricated in Northern Telecom's BiCMOS technology.

2.1 Why Use Silicon Monolithic Technology for RF?

There has been a revival of interest in silicon technology for high frequency digital and analog circuit applications, which started late in the 1980's. There were attempts made earlier in the evolution of silicon IC technology to develop a process using semi-insulating

silicon wafers for microwave applications. However, these projects failed because the semi-insulating properties of the silicon wafer could not be maintained during high temperature processing steps. Very lossy substrates resulted from the diffusion of dopants used to form active devices, and the substrate material became unsuitable for the fabrication of low-loss transmission lines [25]. Aside from some circuit work in silicon-on-sapphire (SOS) technology for military applications during the late 1970's [26], there had been little interest in exploring silicon for high frequency analog circuit applications until the late 1980's.

Interest has been rekindled by two main developments in modern VLSI technologies: active devices which can operate in the GHz band of frequencies, and the capability of designing narrowband circuits using on-chip inductive elements. Active devices, such as bipolar transistors, can be fabricated using sub-micron photolithography with parasitics that are negligible in the low GHz frequency range [27]. This leads to a wider operating bandwidth for low-power bipolar circuits, which are often limited in performance by device parasitics. The adaptation of MOS processing techniques to bipolar devices in silicon technology has also played a role in extending the capabilities of silicon technology into the microwave region. The use of polysilicon for the base and emitter contact in bipolar devices has improved the gain-bandwidth product of these devices to beyond 20 GHz in some production processes [28].

In a monolithic technology, all active and passive components and their interconnections are formed on the same semiconducting substrate. The monolithic approach offers the following benefits when compared to a design based on the interconnection of discrete components:

- low cost
- improved reliability and reproducibility
- small size and weight
- multi-function performance on the same chip

These attributes are relevant to the portable cordless telephone, which must be kept small and lightweight for portability. Since it is primarily targeted at the mass consumer market, it must also be low cost. Small size and low cost have been key to the success of monolithic integrated circuit technologies in other applications, such as home video and audio equipment. Each integrated circuit chip is small (on the order of a few millimetres per side maximum) allowing hundreds of circuits to be processed as a batch on a 150 mm diameter wafer. The fabrication cost is related to the cost of processing a number of wafers at once, so it follows that the cost per IC is proportional to the area of the chip and the circuit yield. A properly designed circuit will yield an acceptable number of working devices, usually in the range from 70 to 90%. In low frequency applications, the cost per chip when a large number of devices are manufactured is lower than the cost of testing and packaging the completed IC. It is expected that this same trend will continue for high frequency analog parts, because the cost of testing and packaging circuits for radio frequency use is even greater than it is for low frequency ICs [29].

The most mature monolithic microwave integrated circuit (MMIC) technologies are based upon GaAs materials, however, silicon ICs have a 3:1 cost advantage over GaAs IC technologies [30]. Fabrication of a circuit in GaAs technology costs more because of the comparatively higher cost of the starting material (GaAs wafers), the smaller wafer diameter used for processing (typically 50 mm smaller in diameter) and the lower processing yields. This makes silicon more attractive for cost sensitive RF consumer products, such as the cordless telephone. Also, there is a possibility that the low and high frequency circuit functions of the receiver can be merged together into a single silicon integrated circuit, opening-up the possibility of a single-chip radio receiver. If monolithic radio frequency circuits can be developed which demonstrate the level of performance required for a portable telephone, then a single-chip realization of the radio through the combination of RF, filtering and A/D conversion circuits in a silicon technology is a distinct possibility. The prospects for a single-chip GaAs solution look much more remote. This is because of the difficulties involved in fabricating low-power logic in GaAs at the million transistor level, and also because device characteristics are difficult to reproduce (i.e.,

match) in the low-cost MESFET technologies, even for devices that are fabricated next to each other on the same substrate [31]. Insulated-gate transistors or MOSFETs are difficult to fabricate in III-V technologies [32], and these devices are required to implement the digital signal processing (DSP) hardware used at baseband in cellular radios. Large scale integration of a CMOS-like digital logic, which consumes very little stand-by power is, at present, considered impractical in a technology other than silicon.

It should also be realized that there are disadvantages to circuit integration in a silicon monolithic context. The processing steps that are associated with the fabrication of the active devices reduce the yield and thereby raise the cost for the entire circuit. This is not the case in a discrete component/hybrid circuit approach, where the interconnect, passive circuit and active device technologies are separated, and thus the yield of an active device will not affect the cost of the passive components. Also, in volume production it is virtually impossible to adjust a monolithic circuit's component value once it has been fabricated. Techniques have been developed for post-processing circuits in order to modify interconnections, however, this is impractical in a high volume manufacturing situation. Thus, design techniques must be developed which are insensitive to the manufacturing tolerances of the active components and variations in the physical dimensions of the passive devices. This is a real challenge when attempting to integrate an RF circuit design on an IC. At RF, circuit complexity can add bandlimiting parasitics and the maximum performance is often achieved by hand-tuning of the components in the completed circuit assembly. Computer-aided design techniques, which have been developed for low frequency IC design, must therefore be rigorously applied to the design of RF integrated circuits (RFICs) in order to optimize their performance and yield. This requires the development of accurate device models for the high frequency behaviour of the passive and active elements on-chip, which is the subject of the last section of this chapter.

2.2 Resonant-Tuned Circuits

High frequency amplifiers have traditionally been designed as broadband circuits

using resistors (R) and capacitors (C) as the sole passive circuit elements in silicon integrated circuit technology [33]. However, in the front-end of a radio telephone receiver, the preamplifier and mixer frequency response can be restricted to a narrow band of frequencies, because only a small portion of the frequency spectrum is used by the system. Narrow bandwidth or "narrowband" designs using resonant-tuned inductors (L) and capacitors (C) are widely used in commercial radio receivers because of the performance advantages that they offer over the broadband IC implementations. These advantages will be discussed in this section, using a simple common-emitter amplifier stage with series feedback at the emitter by way of example (see Figure 2-1). However, the following analysis could apply to any comparison of lossy (R-C) and lossless (L-C) feedback topologies in general. The issue of input and output impedance matching of the amplifier will be set aside for the purposes of the present discussion, however, this subject will be addressed in the third chapter of this thesis.

The R-C version of the common-emitter amplifier is shown in part (a) of Figure 2-1. The emitter degeneration resistor shown in the schematic diagram, R_E , feeds a voltage back to the base input which is proportional to the current flowing through the collector load. This negative feedback is used to stabilize the bias point and the small-signal voltage gain of the amplifier, and the feedback is most effective at low frequencies where the current gain of the transistor is large. If the emitter degeneration resistance is large compared to the dynamic emitter resistance, then the small-signal voltage gain becomes independent of the transistor parameters and can be expressed as a simple ratio of the collector and emitter resistances (i.e., $-R_C/R_E$) at low frequency. Also, most of the input signal in this case will appear across the emitter resistor and only a small portion of the input signal will appear across the base-emitter junction of the bipolar-junction transistor (bjt). Since most of the amplifier's non-linearity arises from the exponential relationship between the base-emitter voltage and the collector current, reducing the ac voltage drop from the base to the emitter will extend the linear range of the amplifier. Hence, the signal amplitude that can be handled at the amplifier input for a given level of distortion at the amplifier output, increases by applying more series feedback at the emitter. The linearity of this amplifier

(a) R-C Amplifier

(b) L-C Amplifier

Figure 2-1: Broadband (R-C) and narrowband (L-C) common-emitter amplifiers.

can therefore be improved by either increasing the emitter bias current, I_{EE} , or by increasing the emitter degeneration resistance, R_E .

The noise figure of this simple amplifier depends upon the performance of the active device as well as the other sources of dissipation that generate noise in the circuit (e.g., the bias resistors). The base resistance of the bipolar transistor appears at the amplifier input, and the thermal noise that this generates is one of the two dominant noise sources of this bjt amplifier configuration [34]. The thermal noise of the emitter resistance appears in the same loop as the input source and so its effect on the signal-to-noise ratio at the output is not suppressed by the amplifier gain. The noise power contributed by the collector load resistor is usually small, since it appears at the output of a stage which has an appreciable power gain.

The other significant noise source is the shot noise produced by the flow of current through the p-n junctions. When the shot noise is partitioned into base and collector current noise sources, it is the noise caused by the dc current flow through the collector that usually determines the effect of shot noise upon the RF amplifier performance. The dc base current is usually small in modern bipolar transistors (i.e., $\beta_{dc} > 100$) and thus the noise power generated by the flow of base current will be smaller than the noise power produced by the dc collector current. Also, the ac current gain of the bjt in the 1-2 GHz range will be significantly smaller than the low frequency value, because the current gain decreases as the operating frequency approaches the transition frequency (f_T) of the device. In addition, the source impedance also plays a role in determining the output noise power caused by the flow of base current. The output noise due to shot noise on the base current is greatest when the amplifier input is open circuited. However, in most high frequency preamplifiers designed for radio reception a low impedance source (i.e., an antenna close to 50 Ohms) is normally used, and so this noise power is usually negligible. The interplay between thermal and shot noise sources and the amplifier source impedance will be discussed in more detail in Chapter 3 of this thesis.

The noise figure of the bjt may be quite low when there is no degeneration present. However, it rises very quickly when degeneration at the emitter is added because the thermal noise generated by the emitter resistor appears in the input source loop. The interaction between parasitic circuit capacitances and the resistive loads and feedback networks reduces the bandwidth of the R-C amplifier, because of the parasitic poles that are introduced. The gain of the amplifier, for example, is limited by the size of the collector load resistance which can be used. This is because of the parasitic pole at the collector which limits the high frequency bandwidth of the amplifier when a transistor with a large emitter area is used. In addition, the high frequency performance of the bjt depends upon the collector-emitter voltage as well as the collector bias current, since the transistor transit frequency, f_T , decreases as the collector-emitter voltage decreases. Thus, it is desirable to maintain a large portion of the supply voltage (V_{CC}) across the active device and minimize the voltage dropped across the emitter and collector resistors. However, this places constraints on the load resistance and the emitter area of the bjt for a given bias current and supply voltage. In a broadband amplifier these constraints make it virtually impossible to achieve both low noise and sufficient gain with a single amplifier stage. Another stage must therefore be added in order to isolate the high impedance collector load needed for a large first stage gain from the low impedance (50 Ohm) load. This will increase the amplifier power consumption.

There is a relationship between noise figure and linearity for the simple common-emitter stage with emitter feedback, which can be placed within the context of the receiver preamplifier design. To obtain the widest dynamic range possible, the noise produced by the preamplifier must be minimized independently of the feedback applied to reduce the amplifier distortion. The value of the emitter resistance is the only parameter which can be varied in a low power design, and hence this broadband amplifier stage can be designed either for low distortion or a low noise figure. These two objectives cannot be achieved simultaneously without introducing significant compromises in the preamplifier performance.

The portable telephone handset must be switched-on periodically to monitor transmissions from the base station and to check for incoming calls. Therefore, it is desirable to minimize the preamplifier (and the mixer) bias current in order to extend the battery life, even in stand-by modes. Thus, collector current cannot be arbitrarily chosen in a low-power design and the amplifier distortion cannot be improved simply by increasing the bias current. If the emitter feedback resistor is selected to linearize the stage, the noise figure of the amplifier can be compromised by the thermal noise added by the feedback resistor. If the resistance at the emitter is kept small in order to improve the amplifier noise figure, then the linearity is no better than that of the bipolar transistor alone.

The above discussion can be extrapolated to more sophisticated feedback configurations that are often used for broadband RF amplifiers. The feedback network that linearizes or modifies some other characteristic of the amplifier performance, such as the terminal impedances, introduces dissipation which raises the noise figure of the circuit to an unacceptably high level for a sensitive receiver preamplifier. Thus, a broadband amplifier designed for high frequency operation using only resistive and capacitive passive components cannot achieve the ultimate performance that is possible from the active devices.

On the other hand, circuit performance very close to that of the active device itself can be achieved when resonant-tuned circuits using inductive and capacitive (L-C) passive elements are used, as illustrated in Figure 2-1(b) [35]. These elements can replace resistors and capacitors in a broadband design that are used for output loading, impedance matching and applying feedback to the amplifier. The inductor that is used in place of a resistor at the collector in Figure 2-1(b) can be made resonant with the device parasitics, thereby absorbing the circuit parasitics as part of the tuned circuit. This allows the circuit designer the flexibility to choose a transistor with a large emitter area and also to operate the device at a low current density in order to minimize the amplifier noise figure within a given frequency range. If a resistor were used at the collector as a load, then the parasitic pole at the amplifier output would restrict the transistor size resulting in a poorer noise figure for the

amplifier. Also, the voltage drop due to the current flow through the resistive load is eliminated, because the inductor has relatively little dissipation when compared to a resistor with the same impedance value at microwave frequencies. Thus, the benefits of a high collector-to-emitter voltage, discussed earlier, can be maintained with lower value power supplies when an inductive load is used.

This improvement can be estimated as follows. The quality factor or 'Q' of the inductor is given by the ratio of the inductive reactance to the total dissipation (r_d),

$$Q = \frac{\omega L}{r_d} \quad (2.1)$$

The impedance of a parallel L-C tank circuit at resonance can be approximated by a pure resistance, R_p , where

$$R_p \approx r_d \cdot [1 + (Q)^2] \quad (2.2)$$

This is the load seen at the collector of the simple L-C amplifier at resonance. A collector resistance equal to R_p would provide an equivalent ac load impedance in the R-C amplifier. Thus, there is (approximately) a factor of Q^2 improvement in the load dissipation when a resonant L-C circuit is used in place of a resistive load. This improvement is realized by a reduction in the dc voltage which must be dropped across the load impedance, and the resultant improvement in the amplifier power dissipation.

Emitter degeneration through the use of an inductor in place of a resistor has similar advantages for the amplifier design. The dissipation of an inductor is much smaller than the Ohmic loss of a resistor required for equivalent dissipation and so the thermal noise contributed by the inductor is very small. Consequently, the transistor noise sources dominate the amplifier noise performance because the feedback element does not introduce a significant amount of noise. Proper choice of the inductor size will result in an impedance that is high enough to linearize the amplifier, while not introducing a dc voltage drop in

the high current (i.e., emitter current) path. This allows the supply voltage to be lowered, thereby saving power.

Matching of circuit impedances is another aspect of the receiver circuit design where inductors on-chip offer the designer some advantages. Impedance matching networks are required to ensure the maximum transfer of power between circuits in the receive chain. For example, the interface between the preamplifier and the mixer requires an impedance match from the preamplifier to the off-chip image-reject filter, and again from the filter to the down-converting mixer input. Impedance matching is necessary in this case to ensure that the losses in the receiver front-end are minimized and to reduce signal distortion caused by reflections in the RF path. Each increment of gain at high frequencies is very costly in terms of the power consumed and the design effort required to achieve a manufacturable design. Hence, low-loss networks are required to efficiently interconnect the circuit elements for the highest possible gain in the RF portions of the radio. These impedance transformation or matching networks are often implemented using lumped-element L-C passive components at frequencies in the low GHz range.

Feedback methods have often been used in silicon IC designs to modify the circuit terminal impedances for matching purposes, and active circuitry is usually a part of the feedback network design [36]. The circuitry that is required to implement these feedback schemes consumes valuable power and it also introduces additional sources of noise into the RF signal path. This results in an unacceptable preamplifier noise figure in portable radio applications when the active devices are typically operated close to their gain-bandwidth limits (i.e., greater than $f_T/5$). This is because the forward path gain in a feedback circuit must be large enough to force the circuit response to depend upon the feedback network characteristics alone. There is no such restriction when reactive matching circuits are used, because any impedance transformation can be implemented using series and shunt L or C elements connected at the ports of the amplifier. A feedback loop is not required to modify the input or output impedances of the amplifiers. Thus, similar performance can be achieved from a less advanced IC technology when low-loss L-C matching networks are

employed.

In summary, resonant-tuned circuits offer a number of benefits to the designer of high frequency circuits, and these benefits have been illustrated here by a comparison of a simple tuned (L-C) amplifier and a broadband (R-C) amplifier circuit. The ability to design RF monolithic circuits with reactive (L-C) elements gives the designer more flexibility in the choice of the circuit bias point, active device size (e.g., emitter area of a bjt) and the circuit topologies which can be applied. This flexibility can be exploited to achieve a higher level of performance from a given fabrication technology. However, an on-chip inductance is the key component that is required for the realization of L-C networks for this purpose. The next section of this chapter will summarize the results of a study into the characterization and modeling of monolithic inductors and transformers that have been fabricated in Northern Telecom's sub-micron BiCMOS technology. These components have significant parasitics that must be accounted for in a monolithic circuit, and consequently accurate device models are necessary for computer-aided design. However, it will be shown that they perform well enough to be used in on-chip impedance matching and feedback networks without adding significant losses in many cases.

2.3 Models for Microstrip Components in Silicon BiCMOS Technology

The performance of lumped monolithic inductors in Signetic's 0.8 μm silicon BiCMOS technology was demonstrated by Nguyen and Meyer in 1990 [37]. The inductors were fabricated using a microstrip transmission line wound as a square spiral, and they behaved like a lumped inductance with a few additional parasitic components. Some simple L-C filtering and signal processing circuits using the inductors were also demonstrated [38], although the performance of the circuits was limited by the low quality factor or 'Q' of the inductors, which was less than 5. It will be shown in this work that a low inductor Q is primarily due to the restrictions imposed by the thin interconnect metallization available in most VLSI technologies.

Circuit models have been developed in this thesis for monolithic inductors and transformers fabricated in a production silicon BiCMOS VLSI technology. These models are based on an analysis of coupled microstrip transmission lines. A computer program which extracts a physically-based model of the microstrip components (i.e., a model based upon the physical parameters of the substrate, metallization, and the physical dimensions) suitable for circuit (SPICE) simulation will be described in the following section. The accuracy of the model has been evaluated for variations in metallization thickness, layout geometry and substrate parameters. A number of experimental measurements have also been made in order to confirm the predictions of the computer models, and a summary of these measurements will be presented.

2.3.1 Monolithic Inductors

Lumped-parameter circuit elements can have very wide operating bandwidths if they have physically small dimensions. The minimum dimension of an element fabricated on an integrated circuit is on the order of one micron or less. Consequently, passive circuit elements that are normally fabricated on an IC, such as resistors and capacitors, can be represented by simple lumped circuit parameter models up to very high frequencies (as high as 50 GHz in some cases [39]).

The monolithic inductor is a transmission line that has been wound in a spiral, so it cannot be considered simply as a lumped inductance. In order to model a physical inductor as a lumped inductance, it must have small enough physical dimensions so that the phase shift of a signal voltage or current, over and above that introduced by the inductive reactance, can be neglected. Spiral inductors may behave like lumped circuit elements in the microwave and lower end of the millimetre-wave portion of the frequency spectrum, depending upon their physical dimensions. The necessary condition for this is that these inductors can be modeled as an electrically short section of a transmission line. The term "electrically short" implies that at the highest operating frequency, the transmission line is physically shorter than one-tenth of a wavelength (i.e., $l/\lambda < 0.1$). A simplified single π -section circuit model for a lossless transmission line is shown in Figure 2-2. Note that at

Figure 2-2: Lumped element model of an “electrically short” transmission line.

low frequencies, the ratio (l/λ) is very small. The series impedance will therefore also be small and the shunt impedances will be very large, and the transmission line behaves like an ideal wire interconnection or a short circuit. As the frequency then increases, the input impedance of the transmission line section will depend upon the load impedance, Z_L . When Z_L is an open circuit, the shunt impedances in Figure 2-2 will be the dominant parasitics and so the transmission line input looks capacitive. This is the case in digital logic circuits, where the interconnect wiring can be modeled as a parasitic capacitance at the input to a CMOS gate, which has a high input impedance. However, if the load impedance is very small or close to a short circuit, the series impedance in Figure 2.2 will dominate the transmission line electrical behaviour and the input impedance looks inductive.

For dimensions typically encountered in a commercial IC fabrication process (metal linewidths between $50\text{ }\mu\text{m}$ and $5\text{ }\mu\text{m}$ on a $350\text{ }\mu\text{m}$ thick substrate), the characteristic impedance of the microstrip transmission line will range from 100 to 200 Ohms. It should be noted that the substrate thickness is a factor in determining the characteristic impedance, even for conductive substrates such as silicon. Although the substrate acts as an imperfect conducting plane at low frequencies, the substrate will begin to appear as an insulator to the electromagnetic field propagating along the transmission line at higher frequencies. The substrate behaviour depends upon both the resistivity and the frequency of the propagating wave [40]. However, the substrate tends to behave as a lossy dielectric in modern silicon VLSI processes, where the substrate resistivities are in the 1-100 Ohm-cm range and operation is in the GHz range of frequencies. Thus, the transmission line characteristic impedance is proportional to the ratio of the metal linewidth and the thickness of the substrate.

For a short transmission line (i.e., less than one-tenth of a wavelength long) with a maximum characteristic impedance of 200 Ohms, the largest inductive reactance that can be realized is given by following:

$$\text{Inductive reactance} < 2\pi Z_{0,\text{max}}(l/\lambda) = 40\pi \text{ Ohms} \quad (2.3)$$

This corresponds to an inductance of 20 nH at a frequency of 1 GHz, which is about the largest value of inductance which can be realized on-chip. The smallest inductance value for most practical circuit applications in the 1 to 3 GHz range of frequencies is approximately 1 nH.

Ohmic losses of an inductor fabricated on a silicon IC are caused by dissipation of energy in the semi-conducting substrate and the series resistance (r_s) of the metallization. The inductor quality factor or 'Q' (given by equation 2.1) relates the energy stored in the magnetic field to the energy dissipated by these loss mechanisms.

The simplest transmission line structure to fabricate on an integrated circuit is the microstrip transmission line. It consists of a rectangular conducting strip on the top side of the substrate and a bottom-side conducting plane, with the integrated circuit dielectric layers sandwiched in between as shown in Figure 2-3(b). Microstrip transmission lines fabricated on high quality insulating dielectrics have losses that are dominated by the Ohmic losses of the metallization used to define the top conducting strip [41]. Below 10 GHz, the characteristic impedance and propagation characteristics of a typical microstrip transmission line on an MMIC can be derived from a quasi-static approximation of the electromagnetic field distribution [42], which is shown in part (a) of the Figure. Dispersion of the transmitted signal caused by field components which lie in the direction of the propagating wave are ignored when this approximation is made, which limits its usefulness at higher frequencies. The relationship between circuit parameters of a transmission line model and the physical dimensions of the microstrip line are empirical, and therefore numerical methods must be used to obtain an exact solution for the field distributions.

A spiral microstrip transmission line is the most popular method of realizing an on-chip inductor using a single layer of metallization [43]. An example of a square spiral microstrip inductor layout is shown in Figure 2-4. The spiral configuration allows a long transmission line to be used without consuming a large chip area. The top level of metallization is normally used to minimize the shunt capacitance of the transmission line because parasitic capacitances lower the self-resonant frequency of the inductor. The spiral induc-

(a) Microstrip transmission line

(b) Microstrip transmission line in silicon IC technology

Figure 2-3: Cutaway view of a microstrip transmission line.

Figure 2-4: Microstrip spiral inductor layout (3 turns).

tor, which can be formed as either a circular or polygonal spiral of metal, can have a higher Q-factor than would be possible with a straight piece of transmission line. This is because mutual magnetic coupling between adjacent strips in the spiral allows a larger inductance value to be realized for a given length of metal, which raises the inductor Q-factor. The total line length must be a small fraction of a wavelength, otherwise the inductor cannot be treated as a lumped element. Unfortunately, this is not always the case.

The inductor Q-factor is related to the ratio of the surface area to the dielectric thickness which separates the microstrip spiral from the ground plane [39]. This is because the surface area of the inductor metallization depends upon the total length of the winding, which in turn is proportional to the coil's inductance. Ohmic losses are proportional to the parasitic capacitance of the entire structure, and these capacitances again depend upon the winding length and the dielectric thickness. Thus, it is the volume of the entire structure which determines the total dissipation of the spiral inductor. The Q-factor for a spiral inductor on an ideal dielectric is limited to between 50 and 100 because of these geometric considerations and because of the sheet resistance of the metallization that defines the spiral. The losses introduced by the semi-conducting dielectric in a silicon IC technology further restricts the Q-factor to less than 10 for most commercial IC processes.

Circular and octagonal geometries have also been widely used to implement microstrip spiral inductors. The circular spiral has approximately ten percent greater Q-factor than the square spiral inductor, however, the inductance value for a given diameter is lower than a square spiral of equivalent dimensions [44]. Therefore, the circular spiral requires more chip area for a given inductance value than the square spiral does. Also, the time to generate a photomask for a circular spiral becomes prohibitive because a large number of polygons are needed to adequately define a smooth arc. 'Manhattan' geometries (i.e., the edges of each polygon are aligned to an orthogonal grid pattern) are preferred for this reason and hence the square spiral has become the most widely used configuration. Other geometries (e.g., an octagonal spiral) approximate the circular spiral while at the same time simplifying the mask generation process, by restricting the polygon

shapes which must be digitized for photomask generation. A Q-factor greater than the square spiral but slightly lower than the circular spiral inductor is possible with an octagonal layout (an improvement in Q of between 5 and 10 percent has been reported [44,45]). However, the interaction between the magnetic field components on adjacent sides of a non-rectangular spiral inductor adds extra complexity to the development of a circuit model for the structure. Thus, only the rectangular spiral inductor will be considered in the following discussion.

There are a number of reasons for choosing a single layer of metallization for the inductor winding instead of the three-dimensional windings that are commonly used for discrete inductors. Using the third dimension in an IC process would require the use of metal vias to interconnect the various planar conducting layers. There are at least two metal layers that can be used for circuit interconnections, and in most modern VLSI processes three layers of metallization are available. It would be possible to interconnect these metal layers with vias to define a multi-turn winding for an inductor. However, the vias usually have a higher resistivity than the metal interconnect layers, because tungsten (which has a resistivity three times higher than aluminium) is used for via formation. The added resistance from the vias would increase the series dissipation of the inductor and cause a significant drop in the inductor Q. Also, the intermetal dielectric layers in most IC technologies are on the order of a micron, which does not allow sufficient space for linking magnetic flux between the coil windings. There must be some space at the centre of the inductor to allow flux lines to pass through and link other turns of the inductor. In the planar inductor this is accomplished by leaving space at the centre of the spiral. However, with the three-dimensional coil configuration the space between metallization layers is inadequate for this purpose and so there will be little energy stored in the magnetic field and hence a lower inductance than desired.

The spiral inductor structures, while compact and more space efficient than the straight wire inductor, are more difficult to analyze. The accurate characterization of these structures at microwave frequencies requires an analysis of the fringing fields, parasitics,

groundplane effects and most importantly for silicon IC design, an analysis of the effect of the conductive substrate on the performance of the component. These effects cannot be fully analyzed to yield closed form expressions which adequately predict the inductor behaviour. Computer models must be developed in order to extract the electrical parameters for a circuit model from the inductor specifications.

2.4 The Silicon BiCMOS Fabrication Process

Substrate and metallization properties, which define the properties of a microstrip line in the BiCMOS process, are shown in Table 2-1. A cutaway view of two coupled microstrip transmission lines on silicon shown in Figure 2-5 illustrates some of these parameters. Thin metallization limits the quality factor of microstrip inductors or transformers fabricated using this process, because energy is dissipated by the finite resistivity of the metallization as well as in the conductive substrate. However, the thick intermetal oxide dielectric limits the parasitic capacitance between the top level metal and the substrate, and this helps to improve the self-resonant frequency of these passive components.

Table 2-1: Parameters for a microstrip line in a silicon BiCMOS technology [46].

Microstrip Line Parameter	Value
Substrate resistivity	10 Ω -cm
Substrate (Si) thickness	380 μ m
Sub. dielectric constant	11.7
Oxide (SiO ₂) thickness	5 μ m
Oxide dielectric constant	3.9
Top metal resistivity	0.03 Ω - μ m

The quality of transmission lines fabricated on silicon substrates degrades at high fre-

Figure 2-5: Cutaway view of coupled microstrip lines on a silicon IC.

quencies, because dielectric losses in the conductive substrate increase as the signal frequency increases [25]. However, modern silicon VLSI technologies with multiple levels of metal for circuit interconnections have a relatively low capacitance between the top layer of metal and the substrate. This development combined with substrate resistivities in the 1 to 100 Ohm-cm range can result in an acceptable level of dielectric loss in the 1-3 GHz frequency range. Recognition of this fact has revived interest in exploring the possibilities offered by the integration of microstrip elements on silicon for RFIC designs [37,38,47].

2.5 Computer-Aided Modeling of Inductors and Transformers

Successful integration of high performance RF front-ends depends heavily upon the development of on-chip resonant circuits. Optimization and refinement of silicon circuit designs incorporating on-chip inductors and transformers has been identified by others [48,49] as lacking in the present state of the design art. A computationally efficient, scalable lumped-element model was therefore developed for this work, which can be applied to any configuration of microstrip lines; not just spiral inductors or transformers. A physically-based, lumped-element model is extracted from the circuit layout and substrate parameters, which can then be used in either a time-domain (e.g., SPICE) or frequency domain (e.g., Touchstone) simulation. This approach to component modeling is more efficient than 3-D electromagnetic simulation techniques [50], and is shown in this work to be sufficiently accurate for RF applications up to a few GHz [51].

A circuit model for the microstrip inductor is needed for simulation and optimization in a circuit simulation environment. Simulators which compute the electromagnetic field distribution of planar-type conductor configurations are now commercially available, and these simulators can extract the circuit parameters of the spiral inductor from the field solutions. One disadvantage of the numerical simulation approach is that some sophistication on behalf of the user is required in order to get meaningful results. Another is the constraints that processing speed and memory size place on the structures which can be

analyzed within a reasonable amount of time.

Optimization of the Q-factor in a planar structure requires closely spaced microstrip lines for tight coupling of the magnetic field and wide microstrip lines in order to reduce the Ohmic losses in the microstrip. Hence a large ratio of linewidth to line spacing is necessary, which requires a large amount of computer memory and computation time in order to derive the circuit model parameters, if a typical computer electromagnetic field solver package is employed. Fortunately, it is possible to speed up the analysis by making a number of simplifying assumptions. The lumped element model can be used to approximate the electrical behaviour of each conductor segment of a square spiral inductor, for example. However, the analysis of the electric and magnetic coupling between a group of microstrip lines still requires some numerical computation.

A set of computer programs were written by Rabjohn to analyze coupled microstrip lines on GaAs MMICs, where the substrate is semi-insulating and can be assumed to be ideal. This set of programs are collectively called the General Microstrip Coupling Analysis Package (GEMCAP [50]), and these programs were available as a basis for this work. GEMCAP computes the circuit parameters for a lumped element model, which can then be analyzed by a commercial circuit simulation package. This approach to microstrip inductor modeling was originated by Greenhouse [52], refined by others [53] and was extended to an arbitrary configuration of orthogonal microstrip lines by Rabjohn. It allows any set of parallel conducting strips to be analyzed. The microstrip lines can then be interconnected to form various structures (e.g., spiral inductor, spiral transformer, Lange coupler, interdigitated capacitor, etc.) and the resulting circuit model analyzed in a circuit simulation environment. This flexibility and computational efficiency afforded by this approach to the analysis has been retained in the new version of the program, called GEMCAP2. Numerous revisions and additions have been made to the package in order to analyze semi-conducting dielectrics and to enhance the flexibility of the simulator for circuit optimization. From the original set of GEMCAP programs, only the inductance calculation routine has been retained in GEMCAP2.

As an example of the GEMCAP2 analysis technique, a circuit model can be derived for the pair of coupled microstrip lines illustrated in Figure 2-5. The physical length of a microstrip line on an RFIC is typically less than 1 mm, which is much less than the guided wavelength, and therefore the ratio l/λ is small in the 1-3 GHz frequency range. A lumped-element π -equivalent circuit can therefore be used to accurately model each individual microstrip line. Two such π -equivalents are shown in Figure 2-6, for two adjacent microstrip lines, as well as mutual capacitive coupling between the lines (represented by C_m in the Figure).

The parameters of the lumped-element model for each microstrip line are computed from the layout geometry, and using the substrate and metallization properties listed in Table 2-1. The self and mutual inductances for all parallel line segments are calculated from closed-form expressions, where the non-zero metallization thickness is incorporated in the self and mutual inductance calculations using the geometric mean distance of the conductor cross-section [54].

For example, the self-inductance, L (in nH), of a straight conductor with a rectangular cross-section can be calculated from Grover's formulation for the mutual inductance between two current carrying filaments [55].

$$M = 2l \left[\ln\left(\frac{l}{d}\right) + \sqrt{1 + \frac{l^2}{d^2}} - \sqrt{1 + \frac{d^2}{l^2}} - \frac{d}{l} \right], \text{ in nH} \quad (2.4)$$

where the filamentary conductors are of length l , and are separated by a distance, d , both in μm . The self-inductance of a conductor with rectangular cross-section can be calculated by subdividing the conductor into conducting filaments, and then integrating equation 2.4 over the entire cross-section. Assuming that the length of each filamentary conductor is much greater than the separation between the filaments yields the following result for the self-inductance, L (in nH), of a rectangular conductor over a ground plane,

$$L = 2l \left[\ln\left(\frac{2b}{w+t}\right) + 1.5 - \frac{2b}{l} \right] \quad (2.5)$$

Figure 2-6: Lumped element circuit model for coupled microstrip lines on silicon.

The conductor width and thickness are denoted by variables w and t , respectively, and the separation between the conductor and the ground plane is given by b in equation 2.5.

The mutual inductance, M , between conductors can be determined in a similar manner. It should be noted that equation 2.4 cannot be integrated in closed form when the separation between conductors is comparable to the conductor length. The mutual inductance between filaments is small in such cases, however, and the effects of finite width and thickness can be ignored with only a small loss in the overall accuracy. Thus, equation 2.4 can be used to directly estimate the mutual coupling between conductors. The effect of the current induced in the ground plane must also be accounted for in the mutual inductance calculations [53], while current induced in the substrate can be neglected in the GHz frequency range for both self and mutual inductance computations. This is because the substrate resistivity for the BiCMOS process is sufficiently large [56].

The self and mutual capacitances are computed using a two-dimensional numerical technique developed for coupled microstrip lines [57]. The shunt resistance of the semi-conducting layer can then be estimated directly from the quasi-static capacitance, C_{Si} [40]. Dissipation of the mutual capacitances can be neglected because the microstrip lines are closely spaced. The frequency dependent resistance, r_{sk} , is approximated from closed-form expressions [58], to form a complete lumped-element equivalent circuit representation. The circuit model can be directly used in a time domain or frequency domain circuit simulation along with other active and passive RF elements. The complete model would normally be reduced to a compact model or S-parameter representation for faster optimization of a complex RF circuit.

2.5.1 Microstrip Spiral Inductors

The GEMCAP2 technique can be extended to more than two coupled lines and applied to the analysis of spiral microstrip components, such as an inductor or a transformer. The physical layout of a microstrip spiral is first partitioned into four groups of multiple coupled lines for analysis; one group per side of the rectangular layout. A lumped element

π -section is again used to model each individual microstrip line within a group, where it should be noted that the assumption of “electrically short” transmission lines is normally satisfied, for the outside dimensions of the rectangular spiral are usually less than 1 mm on each side. Assuming $N=8$ microstrip lines per side, for example, there would be $4N$ or 32 lumped element sections, along with the additional interconnecting elements to model the mutual capacitance between strips as in Figure 2-6.

A 9-turn spiral inductor was designed and fabricated in order to test the capabilities of the lumped-element simulation method. This inductor design was first reported in the literature [37] and so it was chosen as a simple benchmark that could be used to compare the capabilities of Northern Telecom’s BiCMOS process with other commercial BiCMOS processes, and also to validate the predictions of GEMCAP2. It would be possible to optimize the inductor design for the best possible circuit performance, such as optimization of the inductor Q-factor, but this is not necessary for model validation. The 9-turn rectangular spiral inductor measures $210\ \mu\text{m} \times 210\ \mu\text{m}$ (see Figure 2-7) and was fabricated in a $0.8\ \mu\text{m}$ BiCMOS process with the substrate properties listed in Table 2-1. The narrow top metal microstrip line (width, $W = 6.5\ \mu\text{m}$) has a high characteristic impedance, which increases the inductance per unit length of the microstrip line and reduces the parasitic capacitances of the structure. The width and thickness of the metallization limits the inductor quality, because energy is dissipated by the parasitic resistance of the metallization as well as in the conductive substrate.

The measured behaviour of this spiral inductor and the performance predicted by the lumped-element computer model are shown in Figure 2-8. A layer of aluminium $1\ \mu\text{m}$ thick was used to fabricate the 9-turn spiral. A low-frequency inductance (which is given by the reactive portion of the measured impedance divided by the radian frequency) of 8 nH was obtained with a self-resonant frequency of approximately 5 GHz. At low frequencies, the resistive component of the impedance is close to the dc resistance of the inductor, which is about 20 Ohms. As the frequency increases, the resistive component of the loss increases, due to losses in the substrate and skin effect in the metal conductors.

Figure 2-7: The 9-turn spiral inductor test structure.

Figure 2-8: Measured and simulated impedances of the 9-turn spiral inductor.

This illustrates the strong interplay between size of the structure, the layout and the substrate parameters. Design of an inductor to fit a particular application would require extensive simulation work in order to determine the number of turns, linewidth and line spacing necessary to achieve the best performance within a given technology. Extraction of a lumped-element component model is faster than other simulation methods, making this type of optimization more practical.

The quality of the spiral inductor, or Q-factor, could be improved by increasing the thickness of the metallization. The measured quality factor for the 9-turn spiral inductor fabricated with 1 μm and 2 μm thick metal layers is plotted in Figure 2-9. A significant improvement in Q-factor was obtained by increasing the thickness of the metal layer from 1 to 2 μm . The Q-factor initially rises with frequency as the reactive component of the impedance increases, peaks, and then decreases due to the increasing energy dissipation at higher frequencies. The measured behaviour of the inductor fabricated with thicker metal also showed close agreement with the predictions of the lumped-element circuit model. These results indicate that inductors suitable for many RFIC applications could be fabricated in silicon production technologies, if a low resistivity metal of adequate thickness were available.

A compact model for the inductor can be derived from the GEMCAP2 lumped equivalent circuit model. The parameters of a single π -section model (e.g., see Figure 2-2) can be adjusted to model the electrical characteristics of a spiral inductor. This technique has been used to fit experimental measurements, however, the model parameters (the shunt parameters in particular) have little physical significance. Frlan [59] used a compact model consisting of one π -section, with electrical parameters that were computed from an analysis similar to that performed by the original GEMCAP program. The series components of the compact model were determined by simply summing the inductance and resistance of each individual microstrip section. Non-quasi-static effects were accounted for in the computation of this series inductance. The capacitances were summed into a single lumped capacitance, with one shunt arm of the π -model representing the outer wind-

Figure 2-9: Effect of metal thickness on the Q-factor of the 9-turn spiral inductor.

ings and the other arm modeling the inner winding parasitics. The accuracy of this model is improved by fitting of the single-section parameters to the electrical characteristics predicted by the complete GEMCAP2 model. This approach is simple to implement with most commercial simulators that have the capability to optimize circuit electrical parameters, and it requires little additional computation time to refine the relatively small number of parameters in a single lumped element section. A single section compact model that was derived by fitting to the GEMCAP2 model of the 9-turn inductor is shown in Figure 2-10. This model is simple enough to be useful for hand calculations in a circuit and it fits the GEMCAP2 model up to the self-resonant frequency of the inductor. However, its parameters cannot be easily adjusted for slight changes in the inductor design because of the non-physical nature of this simple model.

The model predictions obtained from a three-dimensional electromagnetic field simulation of a spiral inductor can also be used as a means of verifying the lumped element model of the GEMCAP2 simulator. A commercial simulator for planar structures, EM-Sonnet, was used for the three-dimensional numerical simulations. A 4.5 turn square spiral 5 nH inductor with a 10 μm wide line and a 5 μm line spacing was selected for this comparison. A small ratio of linewidth to line spacing was chosen to ensure that the memory requirements and simulation time for the numerical computations were not excessive. The substrate and metallization parameters from the BiCMOS process were also used for the simulations. Excellent agreement is seen between the inductor Q-factor simulated using Sonnet (Q_EMS) and GEMCAP2 (Q_GC) over the frequency range of interest (refer to Figure 2-11). A plot of the Q-factor predicted by GEMCAP2 for the same planar spiral on a lossless substrate (Q_Ideal) is also plotted on the Figure for comparison. This demonstrates that the effect of the substrate conduction on the inductor Q-factor is significant at higher frequencies, but also that operation close to the ideal curve is obtained for frequencies below approximately 1.5 GHz. The ability to predict the substrate effects on the inductor performance is key to the design and realization of inductors with acceptable performance in silicon technology. When substrate effects are properly accounted for in a circuit simulation, the inductor design can be optimized to minimize these losses and

Figure 2-10: Compact model for the microstrip inductor.

Figure 2-11: Q-factor comparison from GEMCAP2 and EM-Sonnet simulations.

improve circuit performance.

2.5.2 Microstrip Transformers

An attractive feature of the original GEMCAP program was the capability that it provided to simulate a wide variety of microstrip coupled-line configurations. This capability has been retained in GEMCAP2 and it has been used to extend the inductor analysis to microstrip spiral transformers. The physical layout of a microstrip transformer is first partitioned into four groups of multiple coupled lines for analysis; one group per side of the rectangular layout as was done for the microstrip inductor analysis. A lumped element π -section is again used to model each individual microstrip line within a group, where it should be noted that the assumption of “electrically short” transmission lines is normally satisfied, for the outside dimensions of the rectangular spiral are usually less than 1 mm for a transformer operating in the GHz range of frequencies.

For design optimization, a simplified version of this lumped element model, i.e., a compact model, is then developed by simplifying this lumped element model, as is valid within a more restricted range of frequencies. An example of such a compact model for a transformer of turns ratio 1:n is shown in Figure 2-12. A compact model for a transformer balun is similar to the model shown in this drawing, but with two secondary output ports and a centre-tapped secondary winding. A linear transformer with magnetizing inductance, L_m , forms the core of the model. Parasitic inductances L_p and L_s are placed in series with the primary and secondary windings of the linear transformer to account for non-ideal coupling (leakage) between the windings. Lumped resistors r_p and r_s are placed in series with the leakage inductances to represent losses in the metallization, and lumped capacitors are used to represent electrostatic coupling between the windings, as well as from each winding to the underlying substrate. The low frequency parameters of the compact model are easily determined from the corresponding low frequency parameters of the complete lumped-element model described previously. An estimate of the parasitic capacitances can also be obtained from the complete model, but optimization is required to refine the capacitive parasitic values and minimize the error between the electrical charac-

Figure 2-12: Compact circuit model of a monolithic microstrip transformer.

teristics of the compact and complete lumped-element models. It should be noted that in the process of optimizing the compact model parameter values, their physical significance is lost.

From the simplified transformer circuit model shown in Figure 2-12, it can be easily seen that the transformer will show a bandpass-type frequency response between the primary and secondary terminals, because of the combined effects of the leakage inductances, L_p and L_s , and the parasitic capacitances. At frequencies well below the passband, little of the signal that is applied to the primary terminals can be coupled to the secondary winding. Therefore, the magnetizing inductance must be made large enough that the passband will occur within the desired frequency range by proper selection of the transformer dimensions and the number of turns of metal. However, too large a structure introduces unwanted parasitic capacitances, which will limit the upper bandwidth. It should be noted that the linear transformer (shown at the centre of the diagram in Figure 2-12) has a permeability equal to that of free space, which implies high linearity and low frequency dependent losses in the core material. However, a low permeability core does not tightly confine the magnetic field, so there is a less than perfect coupling between the primary and secondary windings of a monolithic transformer. This results in significant leakage inductances (L_p and L_s in Figure 2-12), which place an upper limit on the bandwidth of the transformer.

If the feed-forward capacitance (C_o) is neglected, the parasitic elements at the input and output of the linear transformer in Figure 2-12 can be combined with the source and load impedances into a single impedance, for example Z_s at the source. The linear transformer has a reasonably high coefficient of coupling (k is between 0.7 and 0.8 for the monolithic transformers here) so it can be assumed that the leakage inductances are relatively small. The impedance seen at the secondary terminals for the combined source impedance Z_s as defined is then approximated by the following ideal transformation equation:

$$Z_{\text{reflected}} = n^2 \cdot [j\omega(L_m) \parallel Z_S] \quad (2.6)$$

This is the impedance reflected from the primary to the secondary and it is simply the parallel combination of the primary inductance and the combined source impedance multiplied by the square of the transformer turns ratio. Appropriate selection of the source reactance can then be used to modify the impedance reflected from the primary to the secondary. For example, a capacitance might be used to force a resonant condition between Z_s and L_m . A real impedance can then be reflected to the secondary. Similar arguments apply for impedances reflected from the secondary back to the primary. This example shows how tuning of the transformer primary and secondary circuits can be used to reduce the effects of the transformer inductances and thus idealize the transformer behavior for frequencies close to resonance. The transformer bandwidth when tuned is still on the order of a few hundred MHz, which is more than adequate for prospective wireless applications.

A photomicrograph of a 1:1 inverting transformer is shown in Figure 2-13. The 3-turn transformer was fabricated with 1 μm thick metallization in the standard BiCMOS process, using a 15 μm wide metal line and a 1.5 μm line spacing, and measures 580 μm on a side. The measured and predicted S_{21} (measured in a 50 Ohm system) for the transformer is shown in Figure 2-14. Again, the behaviour predicted by the lumped-element circuit model agrees well with the measurements. Narrow line spacings were found to increase the magnetic coupling between windings. Such closely spaced wide metal lines are difficult to simulate with many commercial electromagnetic simulators, because the small sub-sections required by moments method simulators lead to long simulation times. The time required to compute a circuit model using the lumped-element approach is almost independent of the layout geometry chosen, which is a significant advantage when comparing this modeling technique to other computational methods. Measured data for two different transformers are shown in Figure 2-14. Both samples were fabricated with the standard BiCMOS process flow, however, after fabrication the substrate underlying one of the transformer samples was removed by etching. This reduces the parasitic capacitance to the substrate and eliminates losses caused by finite substrate conductivity. The measurements

Figure 2-13: 1:1 inverting transformer test structure.

Figure 2-14: Measured and simulated transmission coefficient magnitude (S_{21}) for the inverting transformer.

showed no discernible improvement in performance when the silicon substrate was removed, which indicates that substrate losses do not impair the performance below 3 GHz. In fact a slightly greater loss was measured because of higher contact resistance between the RF test probes and the suspended transformer structure. The minimum transmission loss of about 3 dB is primarily due to resistive losses in the metal and imperfect coupling between the transformer primary and secondary, and could be reduced through the use of thicker metallization and resonant tuning.

2.5.3 The Microstrip Balun

A balun (balun is a contraction of “**balanced-to-unbalanced transformer**”) is useful as a low-loss phase splitter and combiner in various radio frequency circuit applications. Balanced circuits have many useful properties, such as the high power output from a balanced amplifier stage or the wider dynamic range of a balanced mixer circuit. However, these balanced circuits must often be interfaced with single-ended components at RF, such as the interface between a low-noise amplifier and a doubly-balanced mixer stage. A balun can also be used to isolate dc and ac current paths between stages, or to match the impedance levels between circuits. It is a key component in the discrete doubly-balanced mixer designs which have been used for many years in radio receiver and transmitter applications, and therefore it is of particular interest for the development of high performance monolithic radio receivers.

The measured and simulated performance of the transformer balun designed for a doubly-balanced mixer (the mixer will be described in Chapter 4 of this thesis) are shown in Figures 2-15 (magnitude response) and Figure 2-16 (phase response). The measured transmission coefficient (S_{21}) from the primary input to the inverting secondary output is plotted for an on-wafer measurement, using a separate test structure designed specifically for this purpose. The simulation result shown is for a complete GEMCAP2 lumped element model, derived from the layout and substrate parameters as previously outlined. The performance predicted by the transformer model and the experimental measurements differ by less than 0.2 dB in the transformer passband. Excellent agreement has also been

Figure 2-15: Frequency response of the monolithic transformer balun (inverting output).

Figure 2-16: 2:1 balun phase response.

obtained for the primary to non-inverting secondary output response of the balun (not shown) and for the balun phase response (Figure 2-16). The transformer mutual inductance (L_m in the equivalent circuit of Figure 2-12) introduces a quadrature shift in the phase response at low frequencies, and there is a consistent phase inversion between the signals at the balun secondary outputs as shown in Figure 2-16.

2.5.4 Component Tolerances

It is important to characterize the effect of processing and temperature variations upon the parameters of a monolithic component in order to estimate the yield of working circuits that meet the design specifications. The variation of parameters due to fluctuations in the ambient temperature is also required so that circuit operation over a wide temperature range can be ensured during the design phase. Thus, the processing and temperature induced tolerances in the behaviour of the monolithic inductor and transformer are of interest to the RF circuit designer.

The metal lines used in the inductor or transformer layout have dimensions on the order of microns, however, these dimensions are defined photolithographically to within one-tenth of a micron in a sub-micron IC process. Therefore, the magnetic coupling (i.e., self and mutual inductance) is insensitive to variations in the fabrication process. The turns ratio of the monolithic transformer is set by the ratio of the secondary to the primary winding length and by the transformer linewidth and line spacing, and thus the transformer turns ratio is also insensitive to the small lithographic variations in modern silicon IC processes. Simulations predict that the tolerance on the self and mutual inductances of the transformers designed in this work will be less than 3% for a $\pm 0.2 \mu\text{m}$ change in the linewidth and linespacing. This tolerance would also apply to a monolithic inductor. A larger and more subtle tolerance is introduced by variations in the intermetal dielectric oxide thickness and changes in substrate resistivity, which both affect the parasitic capacitances of the inductor or transformer structure. However, simulations also predict that the variation in transformer bandwidth will be less than 5% for a $\pm 1 \mu\text{m}$ change in oxide thickness and a $\pm 50\%$ change in substrate resistivity from the nominal BiCMOS process

parameters listed in Table 2-1. These tolerances are far less than those encountered for other passive monolithic components, such as capacitors and resistors. A third source of variation is the temperature coefficient of resistance for the metallization used. Aluminium has a strong positive temperature coefficient of resistance (approximately 0.4% per degree Celsius) which can cause a large change in the metal losses with increasing temperature. For monolithic inductors this is a severe problem, because this shift in metal resistance will directly affect the component quality factor or Q. However, the effect on the performance of the transformer is not as severe, because the metal losses are in series with the terminal impedances present at the primary and secondary, which are an order of magnitude larger.

2.6 Summary

A lumped-element computer model has been developed which accurately describes the performance of inductors and transformers fabricated in a silicon BiCMOS process over a wide range of layout geometries. Both the measured and simulated results indicate that the quality of the inductors and transformers fabricated in Northern Telecom's silicon BiCMOS process are dominated by losses in the metallization at lower frequency, and that this loss can be reduced through the use of thicker metal in fabrication. Losses introduced by the conductive substrate dominate the component performance at higher frequencies. However, these losses do not significantly degrade the performance in the low GHz frequency range, making these devices potentially useful in many RFIC applications. Skin effect and dielectric losses can be minimized by proper selection of the conductor width, spacing and metal thickness for a given set of substrate parameters. The lumped-element modeling approach is computationally efficient, and could be used to develop optimized inductor and transformer designs for various RF circuit applications.

3. Low-Noise Preamplifier Design

The design objectives for the preamplifier in a radio receiver are: adequate gain and low intermodulation distortion, terminal impedances which match the system impedance (50 Ohms is assumed here) and a low noise figure. From a system perspective, the amplifier gain must be set high enough to minimize the effects of noise introduced by subsequent stages in the receive chain, and “low-noise” implies that the amplifier does not significantly degrade the input signal-to-noise ratio in doing so. Also, the amplifier must be able to handle the largest signal levels allowed for the radio telephone system without producing excessive amounts of distortion. In addition, interfaces at the input and output of the integrated circuit amplifier are, in general, off-chip. Therefore, transmission line effects and impedance matching must be considered in the design. These and some of the other issues surrounding low-noise amplifier (LNA) design will be discussed in the first section of this chapter. This discussion will initially consider discrete amplifier design at RF and microwave frequencies, where the aspects of discrete design that are relevant to a monolithic implementation will be reviewed.

A silicon integrated LNA will then be presented. This circuit is resonant-tuned for a narrowband response using an on-chip transformer feedback network. An analysis of the circuit operation using simplified small-signal models for the preamplifier will be presented, and the characteristics of the transformer-coupled design in terms of linearity, gain and terminal impedances will be described. The two-inductor amplifier (see Figure 2-1(b)) uses two uncoupled inductors as a collector load and as an emitter degeneration impedance. The results of this analysis allows the performance of the transformer-coupled design and the two-inductor preamplifier, which is a derivative of this design, to be compared. However, a quantitative comparison of the effects of magnetic coupling (i.e., the transformer-coupled versus the two-inductor preamplifier) will be deferred until the fourth chapter of this thesis.

Integrated circuit design using monolithic inductors and transformers is a relatively new area of research in silicon technology. The theoretical analysis and the design methodology for resonant-tuned circuits cannot be found in the textbooks or literature written about (silicon) IC design [7]. However, there is an existing body of knowledge in the area of microwave transistor amplifier design, and this information can be used as a basis for a silicon IC implementation. Thus, traditional microwave amplifier design methods will be described in the following section of this chapter. A single-stage amplifier using a bipolar transistor will be assumed in this context because a multistage amplifier would consume more power, which is undesirable in the portable telephone application. A single transistor amplifier that can provide sufficient gain will therefore be assumed for the purposes of this discussion.

3.1 RF and Microwave Preamplifiers

The design aspects of low-noise amplifiers for applications in the microwave frequency range will now be reviewed. There are many circuit configurations which could be used for amplification, however, this discussion will be limited to single-stage amplifiers such as the one illustrated in Figure 3-1. The amplifier consists of an active device and input and output impedance matching networks. The common-emitter configuration is normally used for the transistor because this connection gives the highest gain per stage of amplification. Bias circuitry must also be included to complete the design. However, the bias circuit does not affect the impedance matching at either the amplifier input or output when the amplifier is well-designed and so bias circuit design will not be considered further in this discussion.

Silicon bipolar transistors have been used for many years in RF small-signal amplifier designs. GaAs MESFETs presently offer better performance (i.e., lower noise figure and better linearity) than silicon bjt's above the 2 to 4 GHz frequency range [60]. However, discrete silicon devices can achieve noise figures well below 2 dB at 2 GHz, and they are less expensive than an equivalent GaAs transistor. The transistor is normally treated in the

Figure 3-1: Microwave low-noise amplifier block diagram.

design process as a two-port circuit as shown in Figure 3-1, and the characteristics are described by a set of two-port parameters for simulation (and measurement) purposes. The small-signal y , h -parameters could be used, but s -parameters are preferred for microwave applications because they can be conveniently measured without causing device instability. The small-signal parameters are bias dependent, and therefore the parameters must be obtained from experimental measurements, or from a computer model (such as the Gummel-Poon model in SPICE) at the bias point where the amplifier will normally be operated. The matching networks are normally assumed to be lossless, which is often a reasonable assumption when discrete components are used. In such cases, these networks can be represented as lumped impedances in a Thevenin or Norton equivalent network at the input or output.

3.1.1 Amplifier Stability

When the entire range of passive source and load impedances is considered, the bjt as an amplifier in the common-emitter connection is most often only conditionally stable at lower frequencies, and only absolutely stable at the upper end of its useful frequency range [61]. A large resistance in series with the transistor emitter tends to promote stability, although its degenerative effect also reduces the gain and increases the noise figure of the amplifier. Feedback from the output to the input of the bipolar transistor is caused by the collector-base parasitic capacitance and any impedance that is connected between the emitter and ground terminals. A large emitter area for the bjt is usually selected for low-noise applications so that the thermal noise generated by the base resistance is minimized. This resistance is inversely proportional to the emitter length of the device, and a relatively large device area is necessary in a typical IC technology. Hence, low-noise bipolar devices have significant parasitic capacitances because of the device area required. Feedback via these parasitics, such as between the base and collector, causes instability and oscillations of the amplifier under certain loading conditions at the input or output. Also, impedance matching networks can no longer be designed independently of each other when the isolation between input and output (i.e., between collector and base) is not large. This is because changes in the impedance connected to one terminal will affect the imped-

ance seen at the other.

For most bipolar devices, there is the possibility of oscillation with some combination of source and load impedances, and therefore the input and output terminations must be chosen so that the unstable regime is avoided. A conditionally stable circuit will oscillate when the device is simultaneously matched (i.e., impedance matched at both input and output), since this condition produces the highest gain. For a conditionally stable circuit, some impedance mismatch at either the input, the output, or at both ports is required to prevent oscillations, or other forms of unstable behaviour. Resistive stabilization networks could be added at the input or the output in order to promote stability, or feedback could be used to reduce the gain and stabilize the amplifier. However, RF gain is an expensive commodity, and the addition of lossy networks will require an increase in the amplifier bias current (and power consumption) in order to achieve the desired gain. They also introduce some degradation in the amplifier gain, bandwidth and noise figure. Hence, designing an absolutely stable circuit may result in a higher cost and power consumption in order to attain the desired level of performance. A more popular option is to select source and load impedances for the transistor which ensure that the amplifier remains stable over the anticipated range of operating conditions [62]. The impedance mismatch is then accommodated by adding passive isolation networks at the input and output.

For a low-power design, a small bias current and low-voltage supplies should be used. The operating point (i.e., the bias voltages and currents) affects the input and output impedances of the bipolar transistor. Impedance matching networks can be designed which transform these impedances to match the source and load impedances, (usually 50 Ohms). However, the matching networks must not cause instability or oscillation and they must be physically realizable in order to be useful in a practical implementation.

3.1.2 Harmonic and Intermodulation Distortion

There are numerous non-linear processes within the bipolar transistor that generate harmonic and intermodulation distortion as the input signal is amplified. Many of the elements of the transistor equivalent circuit are non-linear, but in the linearized device model

these elements are approximated by the first-degree terms of a Taylor series expansion for the non-linear function. Hence, one method of accommodating the non-linear behaviour of the bjt is to consider the higher order terms of the Taylor expansion (i.e., second- and third-degree terms), if the series expansion or an explicit function for the non-linearity can be determined either analytically or from curve-fitting of experimentally determined data. Once the non-linearities have been identified, the distortion produced by the circuit can be analyzed using the Volterra series method [63,64]. This method of distortion analysis is implemented in the SPICE circuit simulator, where the integral charge-control model is used to describe the electrical behaviour of the bjt.

The main non-linearities of the bipolar transistor which have been identified by others [65,66] are: the exponential relationship between the base-emitter voltage and the collector current (i.e., the non-linear transconductance), non-linearities in the ac current gain, and the non-linear junction capacitances. Non-linearity of the current gain is caused by recombination in the base at low bias currents, base push-out (which occurs at high collector current densities, i.e., the Kirk effect) and avalanche multiplication, which occurs at high collector bias voltages. In a low-power bjt amplifier design operating at a low supply voltage and bias current, the non-linearities caused by base push-out and avalanche multiplication can often be neglected [67].

A common-emitter amplifier with source impedance R_S and load impedance R_L is shown in Figure 3-2. A small-signal equivalent circuit which is valid at high frequencies is shown in part (b) of the Figure. The resistive portion of the base-emitter impedance is very large compared with the capacitive reactance at high frequencies, and therefore it has not been included in the equivalent circuit model. Thus, this model is only valid at frequencies greater than the beta corner frequency of the transistor,

$$f > \frac{f_T}{\beta_0} \quad (3.1)$$

where f_T is the transition or unity current gain frequency and β_0 is the low-frequency cur-

(a) C.E. Amplifier

(b) H.F. equivalent circuit

Figure 3-2: Common-emitter amplifier and a simplified high-frequency equivalent circuit for distortion analysis.

rent gain of the transistor at the desired operating point.

Intermodulation distortion is of interest in the radio receiver application, because third-order intermodulation products can fall within the channel bandwidth of the receiver, and the resulting interference may cause errors in the received data stream. Assuming the simplified high frequency equivalent circuit of the common-emitter amplifier shown in Figure 3-2(b), Abraham and Meyer [68] derived the following approximate analytical expression for the third-order intermodulation distortion (IM_3).

$$IM_3 \approx \left(\frac{V_o^2}{4} \right) \frac{\frac{C_{jeQ} V_T}{R_L (I_C)^3} + \frac{C_{jeQ} R_L m_{jc} (m_{jc} + 1)}{2 (V_C)^2}}{\tau_b + \frac{C_{jeQ} V_T}{I_C} + C_{jeQ} R_L} \quad (3.2)$$

In equation 3.2, V_o is the peak value of the sinusoidal output voltage across the load resistance R_L , I_C is the collector bias current, V_C is the quiescent collector voltage, m_{jc} is the exponent which characterizes the variation of the collector-base capacitance with the applied voltage, τ_b is the base forward transit time, and V_T is the thermal voltage of the transistor. The emitter-base and collector-base junction capacitances at the quiescent point are given by C_{jeQ} and C_{jcQ} respectively in equation 3.2. The total emitter-base capacitance at the quiescent point of the transistor is defined as

$$C_{b'e} = C_{jeQ} + C_d = C_{jeQ} + g_m \tau_b \quad (3.3)$$

for the base emitter depletion (C_{jeQ}) and diffusion capacitance (C_d) shown in the equivalent circuit of Figure 3-2(b).

The base-emitter depletion capacitance (C_{jeQ}) was assumed constant in order to simplify the derivation of equation 3.2, and hence the non-linearity due to the depletion capacitance has been neglected. However, the non-linear relationship between the base-emitter voltage and the collector current is retained in the analysis. Thus, there are two non-linearities which are present here: the exponential non-linearity (i.e., non-linear

transconductance) and the non-linear collector-base depletion capacitance. The collector-base depletion capacitance is assumed to vary with the bias voltage (V_{CB}) in accordance with the well-known relationship for a p-n junction under reverse bias,

$$C_{jc} = \frac{C_{jc0}}{\left(1 + \frac{V_{CB}}{\phi_{jc}}\right)^{m_{jc}}} \quad (3.4)$$

where C_{jc0} is the depletion layer capacitance with zero external bias and ϕ_{jc} is the built-in potential of the junction.

Equation 3.2 is written in terms of the bjt device parameters. It reveals that the distortion due to the exponential non-linearity (i.e., the term including the emitter-base capacitance in the numerator of equation 3.2) decreases dramatically as the quiescent current increases, because of the cubic term in collector current (I_C^3). This decrease in distortion with increasing bias current has been verified by device measurement and SPICE simulations of intermodulation distortion at high frequencies [69]. The linearity at high frequency could be improved by minimizing the emitter area of the transistor, since this minimizes the emitter junction capacitance. However, decreasing the emitter area also increases the base resistance of the bjt (this resistance is a major source of noise in the common-emitter amplifier) and base push-out (i.e., the Kirk effect) might be encountered as the collector current density increases. Base push-out is unlikely in most low-noise amplifier designs, where the device emitter area is made relatively large in order to reduce the amplifier noise figure, and the bjt is biased well below the current at which the base transit time is minimized.

The distortion introduced by the collector-base capacitance can be reduced by increasing the collector bias voltage (a problem for low-voltage design) or by minimizing the variation in base-collector capacitance with bias voltage. The latter would entail a reduction in the doping and/or a thinning of the epitaxial collector layer of the transistor. A thinner epitaxial layer would have a lower collector-emitter breakdown voltage, while a more

lightly doped collector would result in a lowering of the critical current density where base push-out occurs, and hence a lower peak f_T for the device.

Equation 3.2 indicates that the intermodulation and harmonic distortion can be avoided by increasing the transistor bias current and the power supply voltage. However, a large bias current and a high supply voltage, which would be chosen to achieve high gain and good linearity, cannot be used in a low-power amplifier design. Feedback is an alternative to increasing the bias current for a low-power design, since it is well known that negative feedback can improve the linear input signal range of an amplifier, even though the active device itself might be operating in a relatively non-linear manner [70].

3.1.3 Amplifier Noise

The preamplifier must be operated at a gain and noise figure which yields the lowest overall noise figure for the system. The sources of noise in the amplifier arise from different physical mechanisms, for example, thermal noise is generated by losses (i.e., dissipation) in the circuit, while shot noise is generated when there is a current flow across a semiconductor junction in a bipolar transistor.

The noise generated in any two-port network can be represented by two equivalent input noise generators, an input voltage source connected in series with the input lead and a current source which is connected in shunt with the input, as shown in Figure 3-3. Noise generated by the equivalent input noise sources will be amplified and/or attenuated by the noise-free network in such a way that the output noise power is identical to that produced by the original (i.e., noisy) two-port network. The current source (i_n) represents the sum of the noise generated by all of the noise sources within the circuit with the generator disconnected from the input (i.e., the input open circuited). Similarly, voltage source (e_n) represents the input referred noise generated by all of the amplifier noise sources when the generator is replaced by a short circuit. It can be shown that all the input referred noise of

the network can be partitioned into these two input equivalent noise sources [71].

Figure 3-3: Equivalent source representation of a two-port network.

A practical source has an impedance which lies somewhere between the open and short circuit conditions. In most RF amplifier applications, both the source and amplifier input impedances are close to 50 Ohms. Thus, noise sources which add to the input equivalent noise voltage will tend to contribute a higher proportion of noise, when computing the noise figure of the preamplifier. The influence of each equivalent input noise source upon the circuit noise factor, F , can be determined from the following equation,

$$F = 1 + \left| \frac{i_a Z_G + e_a}{e_G} \right|^2 \quad (3.5)$$

where Z_G is the impedance of the generator, and e_G is the noise voltage produced by the real part of the generator impedance (i.e., $\text{Re}[Z_G]$). Equation 3.5 shows that the noise factor depends upon the choice of generator impedance.

Assuming that the two port network is a bipolar transistor connected in the common-emitter configuration (emitter grounded), the noise power spectral density of the equivalent input voltage source at low frequencies can be written as [23,73]

$$\overline{e_a^2} = 4kTrbb' + \frac{2(kT)^2}{qI_C} \quad (3.6)$$

where k is Boltzmann's constant, T is absolute temperature in Kelvin, rbb' is the base resistance of the transistor and I_C is the dc collector current. Noise power generated by the base resistance dominates in equation 3.6 when the dc collector current is large. However, as the collector current is decreased, the noise contributed by the shot noise related term in the equation increases in significance. For a base resistance of 10 Ohms, the shot noise term in equation 3.6 will equal the thermal noise generated by the base resistance at a collector current of 1.3 mA. This indicates that collector current shot noise will have an important effect upon the noise figure of a preamplifier that is biased at a low current (in order to save power) and driven from a low impedance generator (when e_a dominates).

The equivalent input current source has a power spectral density given by

$$\overline{i_a^2} = 2qI_B + \frac{2qI_C}{|\beta(\omega)|^2} \quad (3.7)$$

where the flicker ($1/f$) noise of the transistor has been neglected. Both of the terms in this equation are directly proportional to the collector bias current. A high dc current gain is useful in suppressing the dc base current (I_B) and the base current shot noise (i.e., the first term in equation 3.7), however, a high current gain is usually achieved at the expense of an increase in the base resistance. At frequencies approaching the transition frequency of the device (i.e., f_T , where the current gain is unity), the effect of the collector current shot noise (the second term in equation 3.7) becomes comparable to the base current shot noise as the ac current gain, $\beta(\omega)$, decreases. Assuming a typical value of 100 for both the low frequency ac and the dc current gains, the base and collector current shot noise terms in equation 3.7 will become equal in magnitude at an operating frequency approximately equal to one-third of the device f_T .

It should be noted that the equivalent input noise sources are not statistically indepen-

dent, in general. The input referred noise voltage (equation 3.6) depends in part upon the noise voltage produced by the flow of collector current, and its associated shot noise, while a portion of the input equivalent noise current (equation 3.7) is related to the same noise source (i.e., the dc collector current). Since both of the equivalent noise sources depend in part upon the same random variable, they are correlated, and the correlation between the two sources must be determined in order to compute the amplifier noise figure. However, the statistical correlation between the equivalent noise sources is usually not known and therefore alternative methods have been developed to characterize the equivalent input noise of a two-port network. Four parameters are required to specify the input equivalent noise powers and the correlation coefficient between the noise voltage and noise current (which is a complex number).

The noise behaviour of a device intended for RF and microwave use is usually described by the following parameter set: the minimum noise factor, $F_{\min}$, the impedance from the generator that results in $F_{\min}$ (i.e., real and imaginary components), and a parameter which is called the normalized noise resistance, r_n [71]. From these four noise parameters, the noise factor, F , for any source impedance can be calculated from the following equation:

$$F = F_{\min} + \frac{4r_n |\Gamma_G - \Gamma_{opt}|^2}{\left(1 + |\Gamma_G|^2\right) |1 + \Gamma_{opt}|^2} \quad (3.8)$$

The noise figure is simply the noise factor expressed in decibels. Here the reflection coefficient, Γ_x , is related to the impedance, Z_x , by the following relationship

$$\Gamma_x = \frac{Z_x - Z_0}{Z_x + Z_0} \quad (3.9)$$

where Z_0 is the characteristic impedance of the transmission line connecting the source (or generator) to the amplifier input. Thus, the optimum and the actual source impedances, Z_{opt} and Z_G respectively, are related to the optimum source reflection coefficient for noise

(Γ_{opt}) and the actual source reflection coefficient (Γ_G) by equation 3.9,

The normalized noise resistance, r_n , characterizes the sensitivity of the minimum noise figure to changes in the generator impedance. It can be defined in terms of the equivalent input noise voltage source,

$$r_n = \frac{\overline{e_d^2}}{(4kT) Z_0} \quad (3.10)$$

or by using the minimum noise figure, the optimum source impedance for noise and the 50 Ohm noise figure (i.e., F_{50}) as parameters,

$$r_n = \frac{R_n}{Z_0} = (F_{50} - F_{min}) \frac{|1 + \Gamma_{opt}|^2}{4|\Gamma_{opt}|^2} \quad (3.11)$$

If the s-parameters for the bjt are known, then these noise parameters can be computed, or they can be measured experimentally with a noise figure test set [72,73].

The source impedance as seen from the base terminal of the bjt (Z_G or Γ_G) can have a large effect upon the noise figure of the amplifier, as shown in equation 3.8. This is because the relative contributions of the amplifier noise sources depend upon the impedance which is connected to the base of the bjt. A noise voltage that appears at the transistor input, such as the thermal noise generated by the base resistance, is most significant when the source impedance is low. On the other hand, a large source impedance will increase the effect that base current shot noise will have upon the amplifier noise figure. In general, the source impedance for maximum power transfer does not result in the lowest noise figure for the amplifier (i.e., Γ_G for a input impedance match is not equal to Γ_{opt}).

3.1.4 Matching Network Design

One approach to the input matching network design for a radio receiver preamplifier is to simply choose the optimum source impedance which gives the minimum noise figure

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for the amplifier [74]. A passive circuit (e.g., a microwave circulator) can then be connected between the antenna and the preamplifier to isolate the signal reflections caused by the impedance mismatch between source (antenna) and load (amplifier input). The output port is normally tuned for the maximum available gain (i.e., the maximum power gain without inducing oscillation). The gain associated with an impedance matched output and a noise matched input can be computed from the small-signal parameters of the bjt.

An alternative is to use a combination of lossless shunt and series feedback around the transistor to modify its terminal impedances [75]. The transistor input impedances are adjusted through the use of feedback to force the optimum source impedance where the noise figure is minimized to be the complex conjugate of the amplifier input impedance. In this condition, the amplifier noise figure is minimized when it is impedance matched to the source. The source impedance in this case is not the generator impedance (usually 50 Ohms), but rather the generator impedance as seen from the transistor base looking back towards the generator and into the input impedance matching network. If lossless (i.e., passive L-C) feedback networks are used, there is no degradation in the noise performance of the transistor. However, the amount of negative feedback that is typically required causes a large reduction in gain. In such cases, another stage of post amplification is required in order to meet the desired specifications for gain.

Amplifier stability over the entire frequency spectrum and input and output loading conditions must also be carefully analyzed when feedback is applied to a high frequency amplifier design [61]. A transient open or short circuit condition (e.g., the antenna is disconnected momentarily) may cause oscillations at a frequency out-of-band.

When properly designed, the dynamic range of a low-noise amplifier that is designed around a discrete bipolar transistor will approach the performance limitations of the bjt itself. Lossless feedback and matching techniques do not modify the signal-to-noise performance of an amplifier, whereas the more conventional lossy and active feedback circuits used in silicon IC designs add a substantial amount of noise power. This is the prime motivation for investigating the use of lossless feedback in a silicon IC preamplifier

implementation. The RF performance of such a narrowband preamplifier circuit will now be analyzed in more detail.

3.2 Analysis of Narrowband Monolithic Amplifier Performance

High frequency amplifiers in a silicon integrated circuit technology have traditionally been designed as broadband circuits using only resistors and capacitors as passive elements. However, tuned circuits offer many performance advantages, as outlined in the previous section of this chapter and the second chapter of this thesis. Hence, a narrowband circuit topology which exploits the performance advantages offered by resonant tuning of inductive and capacitive elements has been chosen for this work.

The schematic diagram of a narrowband monolithic preamplifier is shown in Figure 3-4. Transformer T_1 is connected so that negative feedback is applied by mutual inductive coupling from the amplifier output at the collector of Q_1 back to the emitter, to improve the linearity of the amplifier. Negative feedback also tends to stabilize the amplifier gain as operating parameters such as temperature and supply voltage are varied. The common-emitter connection has been chosen for Q_1 in order to maximize the gain and minimize the noise figure available from a single-stage amplifier [73].

The emitter and collector loops of the preamplifier are magnetically-coupled via the transformer primary and secondary windings, respectively, as shown in Figure 3-4. However, if the magnetic coupling between the primary and secondary windings of the transformer is reduced to zero, the coupled preamplifier is reduced to a simpler common-emitter configuration. This uncoupled, or two-inductor, amplifier consists of a degeneration inductance in series with the emitter as well as an inductive collector load, a configuration which was previously described in Chapter 2 of this thesis (refer to Figure 2-1(b)). In general, the collector and emitter inductors are coupled to some degree when the amplifier is implemented in monolithic form, and so the transformer-coupled amplifier is really a generalization of the two-inductor amplifier. Thus, there are two possible design

Figure 3-4: Coupled low-noise amplifier schematic diagram.

approaches in a monolithic context for the circuit shown in Figure 3-4. Coupling can be minimized (i.e., an uncoupled or two-inductor design) or it can be exploited, as in the transformer-coupled design. In the following discussion, a coupled preamplifier will be analyzed in order to explore the performance benefits and liabilities for the amplifier introduced by on-chip magnetic coupling. It is important to understand the liabilities introduced by coupling, which could result in instability or other degradations in performance if signal interactions between the collector and emitter loops were neglected in the design. A general analysis of the coupled amplifier can be applied to an uncoupled amplifier by assuming that the mutual inductance between the primary and secondary windings of the transformer is zero.

A number of the advantages outlined in Chapter 2 for the narrowband two-inductor amplifier also apply to the more general circuit including magnetic coupling with the transformer. The collector-emitter voltage across transistor Q_1 of the circuit shown in Figure 3-4 is almost equal to the full supply voltage, V_{CC} , because the resistive losses in the transformer primary and secondary windings are small. This allows the transistor to operate in the forward-active mode for supply voltages as low as 0.9 Volts. The transistor can also be operated at a low bias current, since the bandlimiting effects of the device parasitic capacitances at the collector node can be minimized by tuning the collector load to the desired frequency of operation. Thus, low-voltage as well as low-power operation of the preamplifier can be realized. In addition, power that would be consumed at the input by active feedback and terminal impedance modification schemes is eliminated by using the passive L-C matching network formed by L_i and C_i , which can be implemented with high quality-factor off-chip components. The dc bias to the base of transistor Q_1 is fed from the bias port, V_{BB} , through an RF choke, or on-chip, through a large value resistor.

A complete analysis of the narrowband coupled preamplifier has been undertaken in order to establish the interplay between the component and device parameters and the circuit performance. However, the analysis of the amplifier noise figure will be deferred to the next chapter, where the subject of device selection for low noise will be investigated in

more detail. The relationship between circuit parameters and their influence on the amplifier gain, linearity and terminal impedances is often obscured by the complexities of the circuit model used for computer simulation. Insight into circuit behaviour through numerical solutions of the network equations using tools such as SPICE is a “black box” approach to the circuit design, which is very time consuming unless the analysis is limited in scope.

The circuit shown in Figure 3-4 is a multi-path feedback amplifier. The transformer feedback network (T_1) shunts the output of the amplifier at the collector and feeds back a signal in series with the emitter lead of the bipolar transistor. Alternate feedback paths between the output and the input arise from the collector-base feedback capacitance and the interwinding capacitance of the transformer. The signal path through the interwinding capacitance is regenerative and thus it has a destabilizing effect on the amplifier. The interwinding capacitance is small (a few hundred fF in a typical design), and could be neglected in the analysis. However, the interwinding capacitance will be included in the circuit model in order to maintain generality of the solution, and to ensure that all sources of instability are accounted for.

A compact circuit model for the inverting transformer is illustrated in Figure 3-5(a). It consists of a linear transformer which has primary and secondary self-inductances (represented by L_{11} and L_{22} in the Figure) that are connected in series with resistors which represent the Ohmic losses of the transformer windings. The mutual magnetic coupling between the windings is represented by the mutual inductance, M . Signal inversion between the primary and secondary windings is accounted for by the polarity of the dependent voltage sources (Mi_s and Mi_p in the Figure), which are connected in series with the primary and secondary self-inductances as shown in the Figure. The magnitude of the voltage coupled from the secondary back to the primary, for example, depends upon the current flow in the secondary winding, i_s , and the mutual inductance. The transformer primary and secondary shunt parasitics (i.e., Z_p and the shunt resistor-capacitor network connected at the secondary output) and the interwinding parasitic capacitance, C_1 , complete

a) Simplified transformer circuit model

b) h-parameter representation

Figure 3-5: Inverting transformer compact models.

the lumped-element model. The two signal paths through the transformer (i.e., through the interwinding capacitance and also the path via magnetic coupling between windings) add extra complexity to the analysis of the amplifier. A two-port h-parameter representation of the transformer will therefore be derived as an intermediate step in the derivation of the amplifier gain. Hybrid or h-parameters have been chosen because they provide the most convenient representation of the transformer behaviour for the analysis of this particular feedback configuration.

3.2.1 H-Parameter Representation of the Transformer Compact Model

The h-parameters of the transformer compact model shown in Figure 3-5(b) can be used to relate the primary terminal voltage and current, v_1 and i_1 , to the secondary terminal voltage and current, v_2 and i_2 , using the following set of equations:

$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix} \quad (3.12)$$

The shunt parasitics at the primary, modeled by the impedance Z_p shown in Figure 3-5(a), are connected in parallel with the relatively low impedance seen at the emitter of the bjt in the actual amplifier, and can be neglected in order to simplify the derivation of the h-parameter set. The shunt parasitics at the transformer secondary, which consist of 3 capacitors and a resistor in Figure 3-5(a), appear in parallel with the load impedance of the preamplifier (as seen in Figure 3-4), and will be considered as a part of the total load impedance of the amplifier in the following analysis. Given these simplifying assumptions, the input impedance at the primary terminal of the transformer, or h_{11} , is given by the following equation:

$$h_{11} = \left. \frac{v_{\text{primary}}}{i_{\text{primary}}} \right|_{v_{\text{secondary}} = 0} = Z_T \parallel Z_f \quad (3.13)$$

where Z_f is the feedback impedance between the primary and secondary windings (i.e.,

due to capacitance C_f in Figure 3-5), and the short-circuit primary terminal impedance, Z_T , is given by the following equation.

$$Z_T = r_p + sL_{11} - \frac{(sM)^2}{(r_s + sL_{22})} \quad (3.14)$$

This result, written as a function of the complex frequency variable, s , consists of two impedances in series. One is the short-circuited secondary impedance (r_s in series with L_{22}) reflected from the secondary back to the primary winding, which is connected in series with the primary self-inductance, L_{11} , and the resistive loss in the primary winding, r_p . This combination is connected in parallel with the feedback impedance due to the interwinding capacitance (Z_f) in the equation defining the transformer h_{11} (equation 3.13).

The reverse voltage transfer ratio, h_{12} , is given by the following equation:

$$h_{12} = \left. \frac{v_{\text{primary}}}{v_{\text{secondary}}} \right|_{i_{\text{primary}} = 0} = \left[\frac{\frac{-sM}{r_s + sL_{22}} + \frac{Z_T}{Z_F}}{1 + \frac{Z_T}{Z_F}} \right] \quad (3.15)$$

For an ideal transformer without interwinding parasitics (i.e., Z_f approaching infinity), the parameter h_{12} is the inverse of the transformer turns ratio, or $1/n$, where

$$n = \sqrt{\frac{L_{22}}{L_{11}}} \quad (3.16)$$

The reverse transfer ratio defines the desired feedback path from the secondary winding back to the transformer primary. With a finite interwinding capacitance, the voltage transformed from the secondary to the primary is reduced by the signal coupled through the additional feedback path provided by parasitic electrostatic coupling between the transformer terminals. This is described (with reference to Figure 3-5) by a voltage divider between the primary and secondary terminals formed by Z_f and the impedance seen at the

primary with the secondary terminals short-circuited, or Z_T .

The non-inverting signal component coupled through the interwinding capacitance (Z_f) increases with frequency, and because this component of the feedback is regenerative, it tends to destabilize the amplifier as the feedback signal increases in amplitude. Thus, equation 3.15 reveals that the ratio of Z_T to Z_f must be kept small in order to avoid the destabilizing effects of positive feedback.

The forward current transfer ratio, h_{21} , has a similar form,

$$h_{21} = \left. \frac{i_{\text{secondary}}}{i_{\text{primary}}} \right|_{v_{\text{secondary}} = 0} = \left[\frac{\frac{sM}{r_s + sL_{22}} - \frac{Z_T}{Z_f}}{1 + \frac{Z_T}{Z_f}} \right] \quad (3.17)$$

The short-circuited secondary current is, in the ideal case, related to current flow in the primary winding by the inverse of the transformer turns ratio. There is a non-ideality in the current transformation introduced by the interwinding feedback impedance, Z_f , and an additional path for current consisting of a current divider formed by Z_T and the interwinding impedance.

The final transformer h-parameter is the output conductance with the primary open-circuited, or h_{22} , which is given by the following equation:

$$h_{22} = \left. \frac{i_{\text{secondary}}}{v_{\text{secondary}}} \right|_{i_{\text{primary}} = 0} = \frac{(r_s + sL_{22}) + (2sM) + (Z_f + r_p + sL_{11})}{(r_s + sL_{22}) \left[Z_f + r_p + sL_{11} - \frac{(sM)^2}{r_s + sL_{22}} \right]} \quad (3.18)$$

It should be noted that for a large value of Z_f (i.e., a small interwinding capacitance) the output conductance can be approximated by the self-admittance of the secondary winding,

$$h_{22} \approx \frac{1}{(r_s + sL_{22})} \quad (3.19)$$

The relationships between voltage and current at the terminals of the transformer compact model can now be described in terms of the four h-parameters given by equations 3.13 to 3.18. This h-parameter model will now be applied to the analysis of the forward voltage gain and the reverse isolation for the complete preamplifier.

3.2.2 Amplifier Voltage Gain and Isolation

The voltage gain of the amplifier can be found by direct application of Kirchhoff's Laws to the small-signal model of the circuit. Although this direct approach is perfectly valid, the operation of the circuit is obscured by the complexity of the algebraic solution because of the complex interactions between circuit elements in the presence of multiple feedback paths. An alternative to an algebraic solution is to use circuit simulation in order to solve the network equations numerically. This technique is the most practical method for optimization and refining the overall design, but it provides little insight into the circuit operation. A numerical solution is specific to a particular set of component values, and therefore the underlying generalities which define the circuit operation become difficult to identify.

An alternative to a direct analysis or computer simulation of the circuit is to apply an analytical approach that has been developed for more complex systems employing feedback. At a functional or system level, the effects of feedback upon the amplifier performance in areas such as linearity improvement, modification of terminal impedances, etc., can be easily quantified by taking a higher level approach to the analysis. Greater insight into the overall circuit operation can be realized, because the effect of each feedback path, and the interactions between feedback paths that are caused by changes in circuit parameters or circuit loading effects, can be examined and analyzed independently.

Difficulties in the analysis are encountered when attempting to identify the various elements of the feedback system, such as the forward path gain (G), the feedback path transfer function (H), the feedback pick-off point and the summing point for the error signal. The transformer-coupled preamplifier is analyzed using feedback techniques by identifying the various feedforward and feedback paths within the amplifier, and describing

the transmittances (i.e., the transfer function) along each path by a closed form equation. The feedforward and feedback paths which exist in the transformer-coupled preamplifier can be easily identified when the transformer behaviour is represented by a two-port model. The transmittances corresponding to each signal path can then be used to compute the voltage gain and isolation by applying Mason's gain rule [76,77]. One advantage that this approach offers is a considerable simplification of the algebraic manipulations required to obtain the desired solution. Aside from computational elegance, casting the solution in the classical feedback form is also useful when analyzing the improvement in linearity and the modification of the terminal impedances that result from the use of negative feedback.

A simplified small-signal model of the bipolar transistor (see Figure 3-6) will be assumed for this analysis. Here a single lumped capacitance, C_μ in the Figure, is used to model the total collector-base capacitance of the transistor. In the SPICE implementation of the bjt small-signal model, this capacitance is split into two capacitors, which are connected from the collector to the internal and external base terminals respectively. The phase shift of the signal between the extrinsic and intrinsic base terminals as well as the feedback between the collector and base is over-estimated when a single capacitance is substituted for the two capacitor model. Hence, using a single capacitor connected between the internal base and collector nodes represents the worst case condition. The model has also been simplified by neglecting the transistor output conductance, which is small when compared to the other conductances connected to the collector node. The extrinsic resistances at the emitter and collector terminals, which are small for the large area devices used in a typical preamplifier, can also be neglected. In addition, non-quasi-static phenomena, such as excess phase shift of the collector current, have also been ignored. It should also be noted that the transistor noise sources are shown in the model for completeness.

Given the models for the bipolar transistor and the feedback transformer, a small-signal model of the complete amplifier from Figure 3-4 can be drawn, as shown in Figure

Figure 3-6: Simplified high-frequency model for the bipolar transistor.

3-7. Here, the load impedance, Z_L , consists of the parallel combination of the amplifier load resistance, R_L (including packaging parasitics, such as bondwire inductances in Figure 3-4), the collector resistance, R_C , the secondary tuning capacitance, C_S , and the parasitics at the secondary of the transformer, Z_S (see Figure 3-5 a). The base resistance, $r_{bb'}$, is connected in series with the source impedance, and it will be considered as a part of the source for the purposes of this analysis. The effect that the base resistance has upon the voltage and power gain of the amplifier can be accounted for when the loading of the amplifier input upon the composite source impedance is known. This loading will be found from a calculation of the amplifier input impedance at the intrinsic base terminal, (i.e., $Z_{b'}$).

Signal flowgraphs for the forward voltage gain, $V_{out}/V_{b'}$, and the reverse isolation, $V_{b'}/V_{out}$, can be drawn from consideration of the small-signal model of Figure 3-7. A flowgraph for the amplifier voltage gain is shown in Figure 3-8(a), where the individual path transmittances are shown adjacent to each signal path.

The three forward paths and one feedback path shown in Figure 3-8(a) define the forward voltage gain, $V_{out}/V_{b'}$. Selecting the transistor base-emitter voltage as the error signal will be useful when evaluating the improvement in linearity offered by negative feedback via the transformer, compared to other feedback amplifier configurations such as simple emitter degeneration. As previously discussed in section 3.1.2 of this chapter, the signal amplitude across the base-emitter junction has a large influence upon the levels of distortion produced by the amplifier.

The primary active path shown in Figure 3-8(a), consists of a voltage divider from the base input to the base-emitter junction of the transistor (path α_1), which excites the bjt controlled-current source and results in a voltage at the output via the active path, G_{μ} . The loading on the active path is a parallel combination of the load impedance and the loading due to the other feedback paths, which in this case are: the output impedance of the transformer, the load impedance, Z_L , and the loading introduced by the transformer (i.e., $1/h_{22}$ in Figure 3-7).

Figure 3-7: Small-signal equivalent circuit for the transformer-coupled preamplifier.

a) Voltage gain flowgraph

b) Isolation flowgraph

Figure 3-8: Transformer-coupled preamplifier signal flowgraphs.

There is also a passive forward path between the input and the output of the amplifier that accounts for the signal fed-forward from the base-emitter junction of the bjt to the load via the transformer (i.e., path G_x in Figure 3-8). The transformer also feeds back a signal from the amplifier output to the base-emitter junction (path H_x), which subtracts from the signal applied at the input. This is the desired negative feedback signal. It reduces the voltage across the transistor base-emitter junction, thereby reducing the amplifier gain. However, in doing so it also reduces the distortion generated by the bipolar transistor for a given level of signal at the input.

The remaining path shown in the flowgraph of Figure 3-8, is a passive feedforward path via the collector-base capacitance (path G_μ) which is denoted by its impedance, Z_μ . This impedance forms a voltage divider between the feedback impedance and the loading of the components connected at the collector of the transistor.

The voltage gain, A_v , can be computed from the flowgraph transmittances by eliminating the intermediate base-emitter voltage node, thereby reducing the flowgraph to the following expression:

$$A_v = \frac{V_{out}}{V_{b'}} = \frac{G_\mu + \alpha_i (G_a + G_x)}{1 + (G_a + G_x) H_x} \quad (3.20)$$

The signal path through the collector-base capacitance (i.e., path G_μ) will be neglected in the following discussion of the forward voltage gain in order to limit the complexity of the mathematical expressions resulting from the initial analysis. The effect of C_μ upon the amplifier performance will then be added to the analysis, and the results of the full small-signal model compared to the simplified circuit equivalents.

If the feedback internal to the transformer through the interwinding capacitance is neglected in addition to G_μ , then equation 3.19 can be used to describe the loading of the transformer secondary upon the amplifier output (i.e., $1/h_{22}$) and equation 3.20 can be written as

$$A_v = \frac{-\beta(s) [Z_L \parallel (sL_{22} + r_s)] - \frac{(\beta(s) + 1) (Z_L) (sM)}{(Z_L + sL_{22} + r_s)}}{Z_\pi + (\beta(s) + 1) \left(sL_{11} + r_p - \frac{(sM)^2}{(Z_L + sL_{22} + r_s)} \right) + \frac{\beta(s) Z_L (sM)}{(Z_L + sL_{22} + r_s)}} \quad (3.21)$$

The terms in the denominator of equation 3.21 define the impedance seen from the base input of the amplifier (excluding the base resistance). The first term in the denominator is the small-signal base-emitter impedance of the transistor, Z_π , and it is followed by terms which express the impedance from the emitter to the small-signal ground, as seen from the base current loop. The second term in the denominator consists of the impedance due to the self-inductance and Ohmic losses in the primary winding, and the impedance reflected from the secondary back to the primary windings through the transformer. These three impedances are multiplied by the transistor base-emitter current gain (i.e., $\beta(s)+1$) in order to account for the different current flows between the base and emitter current loops. This is an example of the beta transformation property between the emitter and base of the bipolar transistor [70]. The secondary impedance is inverted when it is reflected across the transformer from the secondary back to the primary (i.e., the square of the magnetizing impedance, M , is divided by the sum of the impedances in the secondary loop), which is a well-known impedance transforming property of a linear transformer [78]. The remaining term in the denominator of equation 3.21 arises from the primary voltage produced by a portion of the collector current which flows through the transformer secondary winding; the secondary voltage is fed-back to the input by magnetic coupling and reduces the voltage appearing across the base-emitter terminals of the transistor because of the negative feedback connection.

The two terms in the numerator of equation 3.21 are the sum of the active and passive path gains G_a and G_x , respectively, referred to the base current of the bjt. The collector current, which is beta times the base current, flows through a load equal to a parallel combination of the load impedance and the loading of the transformer secondary at the output. This is the active gain path which appears as the first term in the numerator of 3.21. The second term results from the passive feedforward of signal through the transformer from

the emitter loop to the output, which has been described previously.

The voltage gain can be expressed in terms of the transformer turns ratio, n , by idealizing the behaviour of the transformer. The ideal transformer has perfect magnetic coupling between the transformer windings and the primary and secondary reactances are extremely large in comparison with the terminating impedances. Also, the Ohmic losses in the windings of an idealized transformer are negligible. The following equation relates the mutual and self-inductances of the an ideal transformer,

$$M = \sqrt{L_{11}L_{22}} \quad (3.22)$$

and the transformer turns ratio, n , is given by equation 3.16. When these relationships and the properties of the ideal transformer are applied to the equation for the voltage gain of the preamplifier (equation 3.21), it can be simplified to the following expression,

$$A_{v(ideal)} = \frac{-Z_L \left(\beta(s) + \frac{(\beta(s) + 1)}{n} \right)}{Z_\pi + Z_L \left(\frac{(\beta(s) + 1)}{n^2} + \frac{\beta(s)}{n} \right)} \quad (3.23)$$

The terms in the numerator and denominator of equation 3.23 correspond directly with those in equation 3.21, which were discussed previously. The numerator, when multiplied by the current flowing in to the base of the transistor, defines the voltage developed at the amplifier output. It consists of two components: one due to the collector current generated by the transistor current gain, and the second is a function of the emitter current fed-forward from the transformer primary to the secondary. The input voltage is developed by current flowing through an impedance that is defined by the three terms in the denominator of equation 3.23: base current flow through the small-signal impedance of the emitter-base junction, the emitter current flowing through the impedance reflected across the ideal transformer, and the voltage at the transformer primary that results from the flow of collector current through the amplifier load.

The small-signal base-emitter impedance of the bjt can be approximated by the capac-

itance C_π in the RF and microwave range of frequencies, because the resistive portion of the impedance, r_π , is typically over an order of magnitude larger. It should be recognized that in such cases, an inductance connected in series with the base lead of the transistor will form a series resonant circuit with the base-emitter capacitance. At the series resonant frequency, the impedance between the input lead and the emitter of the bjt can be assumed zero (assuming that the voltage drop across $r_{bb'}$ is insignificant), and the first term in the denominator of equation 3.23 becomes negligible. Thus, the voltage gain may be re-written as follows

$$A_{v(ideal)} = \frac{-Z_L \left(\beta(s) + \frac{\beta(s) + 1}{n} \right)}{\frac{Z_L}{n} \left(\beta(s) + \frac{\beta(s) + 1}{n} \right)} = -n \quad (3.24)$$

Hence, a gain equal to the transformer turns ratio can also be realized by tuning out the effect of the transistor base-emitter capacitance. This is a form of impedance matching, whereby the overall gain of the amplifier is improved by placing a low-loss passive component in series with the amplifier input in order to modify the input impedance. It is a powerful option available to the designer of a narrowband circuit, which cannot be as easily utilized in a conventional broadband R-C amplifier design.

In order to more clearly see the effects of the transistor parameters and the load impedance upon the idealized preamplifier gain, equation 3.24 can be re-written as,

$$A_{v(ideal)} = \frac{-\left(1 + \frac{1}{n}\right) - \frac{1}{n\beta(s)Z_L}}{\frac{1}{n}\left(1 + \frac{1}{n}\right) + \frac{1}{g_m Z_L} + \frac{1}{n^2\beta(s)}} \quad (3.25)$$

where the transconductance (g_m) of the bipolar transistor is related to the ac current gain and the base-emitter impedance by the equation,

$$g_m = \frac{\beta(s)}{Z_\pi} \quad (3.26)$$

The terms including the ac current gain, or $\beta(s)$, in equation 3.25 will normally be small and can be neglected. If the feedback from the output back to the emitter is large, then the $g_m Z_L$ product will be much greater than the transformer turns ratio in equation 3.25. In such cases, the magnitude of the ideal voltage gain becomes approximately equal to the transformer turns ratio. However, in a low-power implementation, the product of the transconductance and the load impedance will be of the same order as the transformer turns ratio. This is a consequence of the amplifier being biased at a low current in order to save power (which results in a low transconductance) combined with a low impedance load (i.e., a 50 Ohm load). Thus, the voltage gain in most cases will be less than the transformer turns ratio. In addition, feedback between the collector and base (through the capacitance C_μ) in the practical (or non-idealized) amplifier will also cause some reduction in the gain as the frequency of operation approaches the bandwidth limitations of the bipolar transistor (e.g., the device f_{MAX}).

The complete solution for the voltage gain of the preamplifier including the effect of all transistor and transformer parasitics is given by the following set of equations:

$$A_v = \frac{-N + \frac{Z_{F1}}{(Z_L \parallel Z_\mu \parallel Z_f)} + \frac{Z_{F2}}{Z_f}}{D + \frac{Z_{F1}}{(Z_L \parallel Z_\mu \parallel Z_f)} + \frac{Z_{F2}}{Z_f}} \quad (3.27)$$

where

$$N = \left(\beta(s) + \frac{Z_\pi}{Z_f} \right) (sL_{22} + r_s) + \left((\beta(s) + 1) + \frac{Z_\pi}{Z_f} \right) (sM) \quad (3.28)$$

$$D = \{ Z_\pi + (\beta(s) + 1) [s(L_{11} + \beta(s)M) + r_p] + \left(\frac{Z_\pi}{Z_f} \right) (s(L_{11} + M) + r_p) \} \quad (3.29)$$

$$Z_{F1} = (\beta(s) + 1) [D(sL_{22} + r_s) - N(sM)] \quad (3.30)$$

and

$$Z_{F2} = (\beta(s) + 1) \{ D(sM) - N(sL_{11} + r_p) \} \quad (3.31)$$

The magnitude of the voltage gain as a function of frequency predicted from equations 3.27 to 3.31 is compared to the other approximate expressions for the voltage gain in the plot of Figure 3-9. The voltage gain predicted for the preamplifier circuit using: an ideal transformer (“ideal-x” as per equation 3.23), the lumped-equivalent or linear transformer model (“linear-x” as per equation 3.21) complete with all parasitics except C_μ of the transistor, the complete small-signal model from Figure 3-7 (“hybrid-pi” from equations 3.27 to 3.31) and a SPICE small-signal simulation for the full bjt and transformer models (i.e., no approximations), are all plotted on the Figure. The parameters assumed for the simplified transformer and bjt models (Figures 3-5(a) and 3-6, respectively) used in this analysis are summarized in Table 3-1. The primary parasitics for the transformer (Z_p in Figure 3-5(a)) are assumed to be negligible. A bipolar device from the BiCMOS process that was 30 times the minimum emitter area allowed by the process design rules ($0.8 \times 120 \mu\text{m}^2$) was assumed for these computations. The transformer design chosen for the calculations has a voltage step-up (i.e., turns ratio) of 1:4.2 from primary to secondary with a magnetizing inductance (M) of 1 nH.

It can be seen that the variation in the parameters of the bjt with frequency (e.g., the ac current gain) has little influence upon the behaviour of the response in the ideal case, as predicted by equation 3.24. However, the preamplifier voltage gain is considerably less than the turns ratio of the transformer because the feedback from the output back to the emitter is not large (i.e., the product $g_m Z_L$ is comparable to ‘n’ in equation 3.25 for a 50 Ohm load impedance). Hence, inductance in series with the base input lead is required to realize a voltage gain close to the turns ratio, even in this idealized case.

The low frequency roll-off of the transformer is accounted for when equation 3.21 is used to predict the gain (i.e., the linear-x in Figure 3-9). For the “linear-x” results plotted in the Figure, the parasitics at the primary terminal of the transformer and the collector-base capacitance of the transistor have been neglected. Thus, it is the assumption of a finite magnetizing inductance and the dominant transformer parasitics at the secondary

Figure 3-9: Voltage gain as a function of frequency for various levels of complexity in the small-signal preamplifier model.

terminal (shown in Figure 3-5(a)) which separates the behaviour of the linear-x and the ideal-x responses shown in Figure 3-9. The linear transformer feeds back less signal from the amplifier output back to the emitter of the circuit, and this causes an increase in the passband gain. However, there is a large error in the gain within the transformer passband when the linear-x response is compared to the SPICE and hybrid-pi simulations. It should be noted that the collector-base capacitance, which is approximately 240 fF for the 30X device, has been neglected for the ideal-x and linear-x calculations. As a consequence of this, the roll-off in the response which results from the feed forward of signal through the collector-base parasitic capacitance as the frequency increases is not accounted for. The effect of the transformer interwinding capacitance is negligible in this particular case. However, the response predicted by the hybrid-pi model demonstrates that the collector-base capacitance has a significant effect upon the behaviour of the amplifier above approximately 1 GHz.

Table 3-1: Transformer and bjt parameters used for computation.

Transformer Parameter (see Figure 3-5(a))	Value	Transistor Parameter (see Figure 3-6)	Value
r_F	0.5 Ω	V_{CC}	1.9 V
L_{11}	0.31 nH	I_{CC}	2.0 mA
r_s	10.5 Ω	I_{BB}	22.7 μ A
L_{22}	5.4 nH	Emitter Area	0.8x120 μ m ²
M	1.0 nH	g_m	0.076 S
C_f	150 fF	r_π	1140 Ω
C_s	90 fF	C_π	1800 fF
C_{sOx}	940 fF	C_μ	240 fF
C_{sS1}	60 fF	C_{CS}	240 fF
r_{sS1}	360 Ω	f_T (SPICE)	5.9 GHz

The analytical predictions from the small-signal model correspond very closely to the

SPICE simulation results when the simplified small-signal bjt and the non-ideal, but lumped-element equivalent, model for the transformer behaviour are assumed. This indicates the importance of including many of the non-idealities that are usually neglected in an analysis at lower operating frequencies. The agreement between the analytical model and the SPICE simulation show that the equations which were derived from the complete flowgraph for the preamplifier (i.e., equations 3.27 to 3.31), carry almost all of the relevant information from the bjt and transformer models that is required to accurately predict the circuit behaviour in the 2 GHz band.

The base-collector capacitance, in particular, has a large effect upon the circuit response in the passband. It can be seen from examination of the gain flowgraph shown in Figure 3-8(a) that the impedance Z_μ affects the circuit response in two ways. One effect is the additional loading at the output (i.e., Z_μ is part of the parallel load impedance for paths G_a and G_x), while the other is the actual signal fed-forward through C_μ . In the example just presented, the loading effect is small at the output because the load impedance Z_L is almost one order of magnitude smaller than Z_μ . The feedforward path, however, is significant at higher frequencies. Its effect could be minimized by neutralization, that is, adding another forward path to cancel the signal fed-forward through C_μ . The existing feedforward path through the transformer might be used for this purpose. Signal fed-forward through Z_μ might also be minimized by decreasing the collector-base capacitance through an improvement in fabrication technology, or by using bjt with a smaller emitter area which has smaller parasitic capacitances but higher extrinsic resistances (e.g., the base resistance, $r_{bb'}$). Minimizing C_μ by reducing the emitter area of the bipolar transistor would help to flatten the passband frequency response, at the expense of a higher noise figure for the amplifier caused by the increased base resistance.

3.2.3 Amplifier Isolation

The signal isolation between the output and the input ports of the amplifier (i.e., reverse isolation) influences a number of important aspects of the amplifier performance. Poor reverse isolation in the preamplifier has a detrimental effect upon the performance of

the radio receiver, because it introduces a path from the local oscillator back to the antenna in the receiver front-end. The reverse isolation has some important consequences for the design of the preamplifier as well. High isolation between the output and the input is desirable in order to simplify the design of the impedance matching networks of an RF amplifier. In cases where the output and input are well isolated, the amplifier can be assumed to operate in a unilateral manner, which allows the input and output matching networks to be designed independently. When the reverse isolation is high, a change in the impedance seen at the output will not affect the impedance seen at the amplifier input port, and vice versa. This results in a considerable simplification of the design task. High signal isolation between ports also improves the amplifier stability, while poor isolation between ports must be accounted for in order to determine the margin of stability and to design proper terminations for the amplifier.

The preamplifier reverse isolation is influenced by feedback from the output back to the input through the collector-base capacitance of the bjt as well as feedback through the transformer. It should be noted that these two signals have opposite phases and so there will be some cancellation at the transistor base terminal. Ignoring the signal fed-back through the collector-base capacitance in most cases will give an upper bound or “worst case” isolation. The transformer steps-down the signal from the output to the emitter by the turns ratio, and when the amplifier is properly matched this reverse signal is attenuated by an additional factor of 2. This attenuation comes from the divider formed by the amplifier input impedance and the conjugate impedance at the input terminal from an impedance matched source. Thus, the worst case amplifier isolation in the matched condition is given by,

$$\text{Isolation (matched I/O)} > \frac{1}{2n} \quad (3.32)$$

and for a transformer turns ratio of 4, the isolation will be greater than 18 dB.

A flowgraph which illustrates the two reverse signal paths through the amplifier is shown in Figure 3-8(b). In this flowgraph, the emitter voltage is used as an intermediate

variable in the flow of signal from the output back to the input. This follows from the topology of the preamplifier circuit. When the contributions from the two reverse signal paths are summed, the amplifier isolation, B_v , can be expressed by the following equation,

$$B_v = \frac{V_{b'c}}{V_{out}} = H_\mu + (H_i \cdot H_{\lambda c}) \quad (3.33)$$

where

$$H_\mu = \frac{Z_{src} \parallel [(\beta(s) + 1)h_{11} + Z_\pi]}{Z_\mu + Z_{src} \parallel [(\beta(s) + 1)h_{11} + Z_\pi]} \quad (3.34)$$

and

$$H_i \cdot H_{\lambda c} = \frac{h_{12}(Z_{src} \parallel Z_\mu)}{(Z_{src} \parallel Z_\mu) + [(\beta(s) + 1)h_{11} + Z_\pi]} \quad (3.35)$$

The impedance Z_{src} denotes the impedance seen looking towards the source from the internal base node of the bipolar transistor. Hence, Z_{src} includes the base resistance of the transistor, $r_{bb'}$, in series with the source impedance and input matching network.

The signal path through the collector-base capacitance, H_μ , includes the effect of the loading at the amplifier input due to the transistor input impedance combined with the transformer primary impedance, h_{11} , which is beta-transformed from the emitter to the base current loop of the amplifier. The reverse signal path through the transformer is loaded by the parallel combination of the collector-base capacitance and the source resistance seen at the base input, as given by equation 3.35. The sum of these two paths defines the reverse isolation between the collector and the internal base node, and it is illustrated graphically in Figure 3-10 for the four cases previously presented in the discussion of the amplifier voltage gain. There is no assumption of an impedance match between the source and the amplifier input in equations 3.33 to 3.35 and a 50 Ohm source was assumed for the

Figure 3-10: Amplifier isolation as a function of frequency for various levels of complexity in the small-signal model. Amplifier.

comparison shown in Figure 3-10. This leads to poorer isolation when compared to the worst case for a matched input as predicted by equation 3.32. The other parameters used for the computations shown in the Figure were identical to those assumed for the analysis of the amplifier voltage gain in the previous section of this chapter (i.e., a 30X bipolar transistor in the BiCMOS process and a transformer turns ratio of 1:4.2 between emitter and collector loops).

It can be seen from Figure 3.10 that the amplifier isolation is aided by the feedback through the transistor collector-base capacitance, which tends to cancel the signal feedback from the output through the transformer. The isolation at 1900 MHz including the effect of C_{μ} is 31 dB, which is an improvement of 12.5 dB when compared to the isolation obtained when the collector-base feedback is removed (i.e., the linear-x case). This indicates that the amplifier stability can be enhanced by the presence of feedback via the capacitance, C_{μ} . The signal isolation is poorest when an ideal transformer is assumed and the collector-base feedback capacitance is neglected (ideal-x in the Figure), since the feedback from the output back to the input is greatest in this case. Assumption of a linear transformer (linear-x) results in a reduction in the feedback through the transformer and an improvement in the amplifier isolation. The highest isolation is realized when a more practical small-signal model is assumed for the amplifier and the signal cancellation due C_{μ} is accounted for. Excellent agreement with a SPICE simulation of the complete amplifier is obtained when the complete expressions which have been derived from the simplified small-signal model of Figure 3-7 (i.e., the hybrid-pi model) are used to describe the signal isolation.

3.2.4 Amplifier Linearity

It is a well-known property of feedback amplifiers that the distortion generated by a non-linearity within the feedback loop is attenuated by the return difference, or the factor $(1+GH)$ [79]. Increasing either the forward (G) or feedback (H) network gains will reduce the amplifier distortion. In the case of the transformer-coupled preamplifier with the error signal defined as the internal base-emitter voltage of the bjt (refer to the signal flowgraph

for the amplifier shown in Figure 3-8), the input signal is reduced by the effect of negative feedback such that the error signal, or $V_{b'e}$, is given by,

$$\text{Feedback Error} = V_{b'e} = \frac{V_{b'}}{(1 + GH)} \quad (3.36)$$

Thus, the return difference defines that fraction of the input signal which appears across the internal base-emitter junction of the transistor. For a given signal amplitude at the internal base node of the bipolar transistor, $V_{b'}$, the fraction appearing across the internal base-emitter junction of the preamplifier is

$$V_{b'e} = \frac{Z_{\pi} V_{b'}}{Z_{\pi} + (\beta(s) + 1) Z_{em}} \quad (3.37)$$

where Z_{em} is the impedance seen at the transistor emitter. It can be seen from equation 3.37 that an increase in the emitter impedance would result in greater negative feedback and a smaller internal base-emitter voltage for a given input signal $V_{b'}$, as expected. Hence, an indication of the improvement in the amplifier linearity for a given choice of transformer turns ratio and bias current could be determined from computation of the return difference, or in a qualitative way by examining the impedance seen at the emitter of the amplifier.

From the signal flowgraph for the transformer-coupled preamplifier shown in Figure 3-8, the return difference can be shown to be,

$$(1 + GH) = \frac{Z_{\pi} + (\beta(s) + 1) \left(sL_{11} + r_p - \frac{(sM)^2}{(Z_L + sL_{22} + r_s)} + \frac{\beta(s)(sM)Z_L}{(\beta(s) + 1)(Z_L + sL_{22} + r_s)} \right)}{Z_{\pi}} \quad (3.38)$$

where the effects of the interwinding and collector-base capacitances have been ignored in order to simplify the resulting expressions. The emitter impedance can be easily identified within the second term in the numerator of this equation. The expression for the emitter impedance can be simplified using equation 3.22 to give the following result,

$$Z_{em} = Z_L \left(\frac{sL_{11} + (\beta(s)sM) / (\beta(s) + 1)}{(Z_L + sL_{22} + r_s)} \right) \quad (3.39)$$

where the Ohmic losses in the transformer windings have been assumed small. The imaginary portion of the load impedance can then be resonated with the self-inductance of the secondary windings. If this is done, the denominator of equation 3.39 can be further simplified to give,

$$Z_{em} \approx \left(1 + \frac{j[Im(Z_L)]}{Re(Z_L)} \right) \bullet j\omega(L_{11} + \alpha(j\omega)M) \quad (3.40)$$

where the emitter-collector current transfer ratio of the bipolar transistor is given by the variable $\alpha(s)$, where

$$\alpha(s) = \frac{\beta(s)}{(\beta(s) + 1)} \quad (3.41)$$

and operation in the sinusoidal steady-state has been assumed (i.e., $s = j\omega$). For a 50 Ohm load and typical resonating circuit values in equation 3.40, the magnitude of the emitter impedance could be a factor of two greater than the impedance corresponding to the transformer mutual inductance, M . It might be expected from examination of equation 3.39 that the degeneration seen at the emitter is proportional to the magnitude of the load impedance. Thus, for a large load impedance, the effect of the secondary self-inductance would be small and the degeneration would be approximately equal to the impedance of the magnetizing inductance alone. However, resonant tuning of the transformer secondary reduces the effect of losses introduced by leakage of the magnetic field, thereby increasing the signal fed-back to the input, as seen in equation 3.40. This technique will be used to improve the preamplifier linearity in a practical implementation.

3.2.5 Amplifier Terminal Impedances

The impedances at the input and output terminals of the amplifier must be known in order to design impedance matching networks and to predict the s -parameters for the

amplifier. A portion of the input impedance was identified in the previous section of this chapter (i.e., the numerator of equation 3.38). This is the impedance seen at the internal base node in the simplified case, where collector-base feedback and transformer interwinding capacitances are ignored. Maintaining these assumptions, the input impedance seen at the external base terminal may be written as follows,

$$Z_{in} = r_{bb'} + Z_{\pi} + (\beta(s) + 1) Z_{em} \quad (3.42)$$

where

$$Z_{em} = \left(sL_{11} + r_p - \frac{(sM)^2}{(Z_L + sL_{22} + r_s)} + \frac{\beta(s) (sM) Z_L}{(\beta(s) + 1) (Z_L + sL_{22} + r_s)} \right) \quad (3.43)$$

The base resistance, $r_{bb'}$, in equation 3.42 is the resistance which connects the internal and external base nodes of the hybrid-pi model for the bjt (see Figure 3-6). The collector-base capacitance has a significant effect upon the input impedance, because the ac signal appearing across this capacitance is larger than the input voltage at the internal base node of the transistor, due to the voltage gain of the amplifier. Thus, the current flow through this capacitance is proportionally larger than it is for the other components connected at the input, which enhances the effect of C_{μ} upon the input impedance (i.e., the Miller effect). The voltage gain of the amplifier (A_v) was previously determined (refer to equation 3.27 from section 3.2.2 of this chapter) and so the input impedance including the effect of collector-base feedback can be written as

$$Z_{in} = r_{bb'} + [Z_{\pi} + (\beta(s) + 1) Z_{em}] \parallel \left[\frac{Z_{\mu}}{(1 - A_v)} \right] \quad (3.44)$$

From equations 3.42 and 3.43 it can be seen that the input impedance of the bjt is increased by negative feedback from the transformer primary connected in series with the emitter lead. The shunt connected signal from the output that is fed-back to the input by the collector-base capacitance will decrease the input impedance, as described by the parallel combination of impedances in equation 3.44. As a consequence of the Miller effect.

the shunt impedance in 3.44,

$$Z_{\text{Miller}} = \frac{Z_{\mu}}{(1 - A_v)} \quad (3.45)$$

introduces some additional dissipation at the input. The dissipation arises from the phase shift associated with the voltage gain, A_v . Assuming that the impedance Z_{μ} is purely capacitive, the phase angle of the Miller impedance, Z_{Miller} in equation 3.45, cannot be exactly 90 degrees at RF. This is caused by an excess phase shift in the voltage gain at higher frequencies (i.e., in excess of 180 degrees) which is introduced by frequency dependent elements in the circuit. Thus, there is a resistive component associated with Z_{Miller} which affects the real portion of the amplifier input impedance and cannot be removed by reactive tuning at the amplifier input.

Table 3-2: Parallel equivalent circuit parameters for the preamplifier at 1.9 GHz.

Amplifier Model	Input Network		Output Network	
	R_{p_i}	C_{p_i}	R_{p_o}	C_{p_o}
ideal-x	571 Ω	0.83 pF	112 Ω	0.89 pF
linear-x	237 Ω	0.97 pF	89.0 Ω	0.57 pF
hybrid- π	137 Ω	1.62 pF	47.0 Ω	0.16 pF
SPICE	167 Ω	1.69 pF	51.3 Ω	0.22 pF

The input impedance of the amplifier at a given frequency can be modeled by a shunt or parallel R-C equivalent circuit (R_p in parallel with C_p at $f = 1.9$ GHz in the Table 3-2). The component values for this equivalent circuit within the DECT frequency band are listed in Table 3-2 for the various levels of complexity in the preamplifier small-signal model, as described previously. There is a large resistive component shunting the input that results from the feedback between collector and emitter when the feedback transformer is assumed to be ideal (ideal-x). This feedback is reduced by the losses in a practical transformer (linear-x in the Table), which results in a drop in the resistive portion of

the parallel equivalent circuit shunting the amplifier input. The addition of a feedback path between collector and base adds an additional capacitance with some dissipation, the effect of which can be seen as a decrease in the resistive portion as well as an increase in the capacitive component of the input impedance, as shown in the Table.

There is a discrepancy between the real components of the shunt equivalent input impedance (R_{pi}) obtained using the hybrid- π model and the SPICE simulation of the complete amplifier. The main source of this error is the single-capacitor approximation of the collector-base feedback capacitance in the simplified hybrid- π model of the bjt, which was discussed previously in section 3.2.2 of this chapter. Distributing the base-collector capacitance across the base resistance, $r_{bb'}$, reduces the effect of the collector-base feedback upon the input impedance, because the voltage gain at the external base (node b) is lower than at the internal base node (b'). Equation 3.45 predicts that the Miller impedance appearing in parallel with the amplifier input increases as the voltage gain is reduced, and as a result, the Miller effect is less severe when the SPICE Gummel-Poon model is used to represent the bjt. Hence, SPICE simulation predicts a larger real portion for the preamplifier input impedance at 1.9 GHz.

Knowledge of the amplifier output impedance is also required in order to match the LNA output to the following stage, which could be either a down-converting mixer or an image-reject filter depending upon the system architecture in a radio telephony application. The output impedance of the preamplifier is reduced by shunt negative feedback via the transformer and the collector-base feedback capacitance. The output resistance of a bipolar transistor is on the order of 10^4 Ohms, and consequently the output impedance of the transistor at low frequencies (i.e., where the current flow through C_μ is negligible) is very large. However, the secondary winding of the transformer and the collector-base capacitance load the preamplifier output, and this loading results in additional paths for the flow of current at the output terminal. The finite reverse gain of the transformer-coupled preamplifier allows ac current to flow from the output node back to the amplifier input (i.e., the base), which excites the dependent current source of the bjt. Current flow-

ing through the base terminal of the transistor will therefore be multiplied by the transistor current gain, adding to the signal current drawn at the amplifier output for a change in the output voltage. This feedback causes a further decrease in the output impedance.

An approximate algebraic solution of the output impedance can be obtained by assuming that

$$Z_{out} = Z_{Lf} \parallel Z_S \parallel Z_{oa} \quad (3.46)$$

where Z_S is the equivalent shunt impedance of the transformer secondary parasitics, Z_{Lf} is the parallel combination of the amplifier load impedance, Z_L , and the transformer interwinding capacitance, Z_f , and Z_{oa} is the output impedance of the rest of the amplifier circuit. In order to simplify the algebraic expressions, the interwinding capacitance is lumped into the load impedance, Z_{Lf} , which is a valid approximation because the impedance at the emitter node of the amplifier is small.

The impedance Z_{oa} can be expressed in terms of the other small-signal model parameters for the preamplifier (see Figure 3-7) by the following equation:

$$Z_{oa} = \frac{(sL_{22} + r_s) \left(\frac{(Z_\mu \parallel Z_{src}) + Z_\pi}{(\beta(s) + 1)} + sL_{11} + r_p \right) - (sM)^2}{Z_{bem} + \left(\frac{\beta(s)}{(\beta(s) + 1)} - \frac{Z_\pi}{Z_\mu} - \frac{r_p + s(L_{11} + M)}{Z_\mu} \right) \left(sM + \frac{(sL_{22} + r_s)Z_{src}}{Z_{src} + Z_\mu} \right)} \quad (3.47)$$

where

$$Z_{bem} = \left(\frac{(Z_\mu \parallel Z_{src}) + Z_\pi}{(\beta(s) + 1)} + sL_{11} + r_p + \frac{(sM)Z_{src}}{Z_{src} + Z_\mu} \right) \left(1 + \frac{sM + sL_{22} + r_s}{Z_\mu} \right) \quad (3.48)$$

and Z_{src} the sum of the base resistance, $r_{bb'}$, and the source impedance connected to the amplifier input terminal (i.e., the transistor base). If feedback through the collector-base capacitance is ignored, then equations 3.47 and 3.48 can be combined and simplified to give,

$$Z_{out} = \frac{(sL_{22} + r_s) \left(\frac{(Z_\pi + Z_{src})}{(\beta(s) + 1)} + sL_{11} + r_p \right) - (sM)^2}{\left(\frac{(Z_\pi + Z_{src})}{(\beta(s) + 1)} + sL_{11} + r_p \right) + \frac{\beta(s)(sM)}{(\beta(s) + 1)}} \quad (3.49)$$

The shunt equivalent R-C output impedances for the various amplifier small-signal models discussed previously are also listed in Table 3-2. A 50 Ohm source resistance in series with the base resistance of the transistor has been assumed for these computations. The real portion of the output impedance is of interest here because the reactive component can be eliminated through resonant tuning at the amplifier output. It can be seen from the data listed in the Table that the output impedance decreases to approximately 50 Ohms when the non-idealities of the monolithic transformer and the transistor collector-base capacitance are accounted for. Also, good agreement is obtained between the predictions of the hybrid-pi model and the SPICE simulation results. As previously noted, the value of the 0.8 pF load capacitance assumed at the amplifier output (C_S in Figure 3-4) could be adjusted to reduce the reactive component of the output impedance to zero, if desired.

3.3 Summary

The issues relevant to the design of a low-noise RF preamplifier for radio receiver applications were reviewed in the first section of this chapter. The important trade-offs in a narrowband RF preamplifier design were highlighted through a discussion of amplifier stability, gain, linearity and impedance matching. The relationship between the dc bias current and the amplifier linearity, which has implications for a low-power preamplifier design, were described in some detail. It was seen that a low bias current and low distortion are mutually exclusive, because the intermodulation distortion is inversely proportional to the quiescent collector current. Thus, alternative methods of reducing distortion such as negative feedback must be considered. The sources of noise that are generated within the bjt were also described. Minimizing the input referred noise of the bjt involves a complex trade-off between the ac current gain of the device, the base resistance and the dc bias currents flowing through the base and the collector terminals. However, the noise

figure of a particular circuit configuration can be predicted if the four noise parameters for the device are known.

The linearity of a common-emitter amplifier at a given bias current can be improved through the application of negative feedback. A narrowband common-emitter amplifier topology which uses transformer coupling to realize a passive feedback network was presented and analyzed in this chapter. The preamplifier could be implemented using either two uncoupled monolithic inductors or with a single monolithic transformer, however, the same analysis applies to both amplifier configurations. The two-inductor or uncoupled amplifier is a special case of the more general transformer coupled preamplifier configuration, where the mutual coupling between the collector and emitter current loops is negligibly small.

The forward and reverse voltage gains of the preamplifier were analyzed by identifying the signal flow paths within the circuit and applying well-known feedback analysis methods. It was seen that the results predicted for a simplified version of the preamplifier circuit agreed well with predictions of a circuit simulator (SPICE) for the complete small-signal model of the amplifier. It was also shown that the collector-base capacitance of the bjt has an important effect upon the amplifier performance which cannot be ignored in the analysis if high accuracy is desired. However, some insight into the circuit operation can be gained if some simplifying approximations are made.

The preamplifier output current is primarily the result of the difference between input signal (at the base of the bjt, neglecting $r_{bb'}$) and the voltage induced in the transformer primary by current flowing in the secondary winding. This potential difference appears across the small-signal base-emitter impedance of the bjt and excites the collector current generator, while the remainder of the signal appears across the impedance reflected from the transformer secondary back to the input loop. For a given source and load impedance, the LNA gain can be adjusted through the selection of the transistor bias current (i.e., modification of the forward gain) or the transformer parameters (e.g., modification of the feedback using the turns ratio or the magnetizing inductance).

The preamplifier gain can be improved by resonant tuning at the input. Placing an inductance of the appropriate value in series with the base lead of the transistor increases the power absorbed at the amplifier input. It was shown that a voltage gain equal to the transformer turns ratio can be realized when the net input signal voltage dropped across the base-emitter impedance (which is predominately capacitive at RF) is removed by tuning the amplifier input using a series inductance.

At the amplifier output, the current flow in the transformer secondary is also enhanced by resonant tuning, where tuning at the secondary can be used to improve the preamplifier linearity. It was demonstrated that the effective emitter degeneration is greater than the magnetizing impedance of the transformer when resonant tuning is applied to the secondary winding.

The feedback introduced by mutual magnetic coupling comes at the expense of a decrease in isolation between the amplifier output and input. However, it should be noted that the collector-base feedback, which has a significant effect in a bipolar design operating at low current because of the emitter area needed to achieve low noise, can be used to neutralize the signal leakage along the passive paths of the amplifier due to the non-ideal isolation of the transformer. This neutralization is important in the radio telephone application, where adequate preamplifier isolation is needed to prevent the strong local oscillator signal from reaching the antenna and being re-radiated, thereby interfering with other users in the system.

The real component of the preamplifier input impedance was shown to be increased by transformer feedback but decreased by collector-base capacitance due to the Miller effect. The LNA output impedance is decreased by feedback through the desired feedback path (the transformer) and the parasitic feedback path through the collector-base capacitance. An output impedance close to 50 Ohms (real) can be obtained for a transformer turns ratio of 4, thus an output matching network is not required.

The preamplifier circuit design for a 1.9 GHz receiver and its experimental perfor-

mance will be described in the following chapter. Negative feedback using a monolithic transformer is implemented in an L-C narrowband LNA suitable for use in a portable radio telephone handset application. Transformer coupling is used to linearize and stabilize the amplifier without incurring a large penalty in the noise figure or power gain of the amplifier.

4. Transformer-Coupled Preamplifier

The implementation of the transformer-coupled preamplifier in a silicon BiCMOS process will be presented in this chapter. The preamplifier circuit, which was analyzed in detail in the third chapter of this thesis, is tuned for a narrowband response using an on-chip transformer feedback network. The low-noise preamplifier is designed to meet the specifications for a DECT-compatible portable radio receiver (outlined in Chapter 1), and it serves two purposes as a demonstration vehicle. The first objective is a validation of the monolithic transformer models in a high frequency (1.9 GHz) radio application. Computer-aided design (CAD) models for the transformer have been used both to analyze and to optimize this amplifier design, using the models that were described in Chapter 2 of this thesis. The other objective is to demonstrate the performance advantages of implementing resonant-tuned circuits on a silicon IC for RF applications.

The first step in the design procedure for the LNA is to determine the degree of coupling between the collector and base-emitter loops of the preamplifier which will result in the optimum performance. The collector load and the emitter degeneration inductances of a common-emitter amplifier can be magnetically-coupled through the use of a transformer, and this connection was analyzed in detail in Chapter 3 of this thesis. However, the design process can be considerably simplified if the mutual coupling between the collector and emitter loops is ignored. Mutual magnetic coupling introduces a strong link between the amplifier input and output loops, and as a result, the loops cannot be analyzed independently by the circuit designer. The additional complexity involved in the analysis and design of a bilateral amplifier, must be justified by some improvement in the level of performance as a result of magnetic coupling. In addition, mutual magnetic coupling between two inductors fabricated on the same substrate will be present in any practical IC layout. The effects of mutual coupling between these inductances, either by design or by default, should be considered for completeness and accuracy in the analysis. Hence, the

performance characteristics of coupled and uncoupled preamplifier circuits will be investigated in the first section of this chapter. The results of this investigation demonstrate that there is a clear benefit in power gain, linearity and power consumption that can be realized when the collector and emitter loops of the amplifier are tightly coupled.

The design of the preamplifier involves a number of steps, such as the selection of a transistor for low-noise amplification at the desired bias point and frequency, impedance matching at the input and output ports, and choosing circuit parameters which will yield the optimum level of power gain and low distortion. These issues will be discussed within the context of the transformer-coupled preamplifier in the remaining sections of the chapter. Experimental measurements for a preamplifier which has been implemented in a sub-micron BiCMOS process will then be presented. The agreement between the amplifier performance predicted from simulations and measured data will be compared and discussed.

4.1 A Comparison of Coupled and Uncoupled Preamplifier Circuits

The benefits of magnetic coupling, as implemented in the transformer coupled preamplifier described in Chapter 3, will now be outlined through a comparison of two preamplifier designs. One configuration, called the uncoupled preamplifier, consists of a common-emitter amplifier with emitter degeneration and collector load inductances, as shown in Figure 4-1(a). In the following analysis of this circuit configuration, it is assumed that there is no magnetic coupling between the two on-chip inductors, L_{CC} and L_{EE} . Magnetic coupling between the collector and the emitter of the amplifier circuit is achieved through the use of a monolithic transformer, as shown in part (b) of Figure 4-1, resulting in the "coupled" amplifier configuration. The objective of this comparison is to quantify the differences, if any, between these two LNAs in terms of the preamplifier performance measures, and to establish whether any of the additional effort required to design the transformer-coupled circuit is justified.

a) uncoupled preamplifier circuit

b) coupled preamplifier circuit

Figure 4-1. Coupled and uncoupled low-noise amplifier schematic diagrams.

The design space for the preamplifier can be investigated by varying the parameters of the transformer, such as the magnetizing inductance and self-inductances, and the losses in each winding. Setting the mutual inductance (M) to zero will decouple the primary and secondary windings of the transformer so that the preamplifier degeneration and load inductances operate independently from each other, as in the uncoupled preamplifier design. Furthermore, if the self-inductance of the primary winding and the transformer mutual inductance are assumed to be zero, the coupled preamplifier is reduced to a simple common-emitter stage without feedback. Hence, the common-emitter amplifier with an inductive collector load (i.e., just the self-inductance of the secondary winding) and the uncoupled amplifier can both be considered as special cases of the more general coupled design. Therefore, the results of the coupled amplifier analysis presented in Chapter 3 of this thesis can be applied to an investigation of the design space for a range of preamplifier configurations. The attributes of the coupled and uncoupled amplifiers and the effects of coupling upon the power gain, isolation and terminal impedances of the preamplifier are adequately described by the small-signal analysis from Chapter 3. However, the amplifier distortion and noise figure in both the coupled and uncoupled cases can be more efficiently studied through the use of circuit simulation, because of the complexities involved in the analysis and the extent of the numerical computations required.

4.1.1 Amplifier Power Gain

The power gain is an important specification for the low-noise preamplifier in a radio receiver because it is the preamplifier gain that will suppress the noise introduced by other components in the receive chain. In order to maximize the signal-to-noise ratio of the received signal, the power gain that can be obtained from the bjt must be maximized at the desired bias points as well as ensuring that the noise produced by the amplifier is as small as possible. The maximum power gain which can be realized from an amplifier is not defined when the amplifier is potentially unstable (i.e., Rollett's stability factor, $k < 1$). Therefore, some resistive damping must be added at the input and output ports in order to ensure stability (i.e., to ensure that $k=1$), and when this is done, the maximum stable gain is defined by the power gain that is achievable when the stabilized input and output ports

are conjugately matched.

The available power gain is defined as the ratio of power available from the amplifier output to the power available from the input signal source.

$$\text{Available Power Gain} = \frac{\text{Power Available at the Output}}{\text{Power Available from the Source}} \quad (4.1)$$

An amplifier that is stable under all possible loading conditions at the input and output ports (i.e., $k \geq 1$), has a maximum available gain that is defined by the power gain when both of the amplifier ports are conjugately matched. The application of negative feedback will reduce the available gain of the amplifier, but the reduction in gain is traded-off against a decrease in the harmonic and intermodulation distortion produced by the amplifier for a given input signal level.

It is useful to compare the available power gain of a common-emitter bjt amplifier without feedback to the power gain that can be obtained from the coupled preamplifier, in order to evaluate the true effect of the transformer feedback. The frequency dependence of the maximum stable gain (as previously defined) for a bjt connected in common-emitter configuration without transformer feedback is illustrated in Figure 4-2 (denoted by BJT on the Figure). The transistor is biased at a collector current of 2 mA with a collector-emitter voltage of 1.9 Volts. Below 3 GHz the bjt is potentially unstable, and so the highest power gain that can be achieved without an oscillation occurring is plotted in this frequency range (i.e., the maximum stable gain). Above approximately 4 GHz, the device is absolutely stable and there is a discontinuity in the slope of the bjt gain curve at the transition point between the conditionally and unconditionally stable regions.

As described previously, the common-emitter amplifier is a special case of the coupled preamplifier where the mutual and the primary self-inductances are assumed to be zero. The maximum available power gain of the transformer-coupled preamplifier is also plotted in Figure 4-2 for comparison, using an identical bjt biased under the same conditions, but connected to a 1:4 turns ratio transformer. The parameters chosen for the transformer-

Figure 4-2: Maximum stable gain for the transformer-coupled amplifier and the bjt.

coupled amplifier shown in the Figure are the same as those used in the sample analysis of the coupled preamplifier circuit from Chapter 3 (refer to Table 3-1 for a summary of the component values). The preamplifier is absolutely stable for all operating frequencies, and consequently the power gain curve shown for the coupled circuit is the maximum available gain for the coupled amplifier. As shown in the Figure, transformer feedback achieves the desired effect; it stabilizes the amplifier and levels the power gain available from the bjt, at the expense of some gain reduction (approximately 3 dB from Figure 4-2) as would be expected with negative feedback.

4.1.2 Amplifier Linearity

The linearity of the common-emitter bjt alone (i.e., without feedback) is very poor, with the third-order intercept at the input typically in the -12 to -20 dBm range. However, for the common-emitter transistor it can be easily improved by adding degenerative feedback from an inductance connected in series with the emitter. If the mutual magnetic coupling between the collector load and the emitter is assumed to be zero, the amplifier with degeneration can be considered as a two-inductor or uncoupled design, as shown in Figure 4-1. An alternative method of applying degeneration at the emitter is to use mutual magnetic coupling, as in the coupled amplifier design. Hence, it is useful to compare the performance of the coupled and uncoupled designs which produce comparable levels of distortion in order to evaluate the effectiveness of transformer feedback versus simple emitter degeneration as a method of linearizing the bjt.

The distortion produced by a common-emitter bjt amplifier was discussed briefly in Chapter 3 of this thesis. A simplified expression for the third-order intermodulation distortion produced by a single transistor amplifier at high frequency was discussed in the third chapter (equation 3.2), and that equation relates the distortion to a number of circuit parameters. The terms in the numerator of equation 3.2 express the effects of distortion due to the non-linear transconductance and the non-linearity of the collector-base depletion capacitance of the transistor. For the device parameters and circuit bias conditions chosen for this study, the non-linear transconductance (related to the first term in the

numerator of equation 3.2) clearly dominates the intermodulation distortion predicted for the bjt. When the contribution of the collector-base junction capacitance to the intermodulation distortion of the transistor is neglected, equation 3.2 can be simplified to give the following approximation for the distortion,

$$IM_3 \approx \left(\frac{V_o^2}{4} \right) \frac{\frac{C_{jeQ} V_T}{R_L (I_C)^3}}{\tau_b + \frac{C_{jeQ} V_T}{I_C}} = \left(\frac{I_o^2}{4 (I_C)^2} \right) \frac{C_{jeQ}}{C_d + C_{jeQ}} \quad (4.2)$$

where I_o is the signal current flowing through load resistance R_L , as shown in Figure 3.2(b). The emitter-base depletion and diffusion capacitances at the quiescent point are given by C_{jeQ} and C_d , respectively, and the quiescent collector current is denoted by I_C . The load current is supplied entirely by the collector dependent current source of the transistor when C_{je} is negligibly small, and this output current is exponentially related to the base-emitter voltage. Hence, equation 4.2 relates the amplifier distortion to the collector current, and also indirectly to the base-emitter voltage of the transistor through the device transconductance. This highlights the importance of limiting the signal voltage appearing across the base-emitter junction, because it is the amplitude of the base-emitter voltage which drives a significant portion of the distortion produced by the common-emitter amplifier. Negative feedback is often applied to an amplifier for this purpose.

From the relationship between the intermodulation distortion and the circuit parameters predicted by equation 4.2, it is reasonable to assume that the distortion produced by either of the amplifier configurations (coupled or uncoupled) for a given input signal level can be lowered by reducing the voltage appearing across the base-emitter junction of the bipolar transistor. The base-emitter voltage in either the coupled or uncoupled amplifier configuration is given by equation 3.36 (refer to Chapter 3). This equation predicts that an increase in the return difference, $1+GH$, will reduce the base-emitter voltage for a given level of signal at the internal base terminal of the transistor. If the return difference for the coupled and uncoupled amplifier designs were made equal, then the base-emitter voltages

for a given level of input signal would also be approximately equal. In that case, similar levels of intermodulation distortion would be expected from both amplifiers, given the previous assumptions.

Thus, if the effect of the collector-base capacitance is neglected, equation 3.37 can be used to predict the return difference for both the coupled and uncoupled amplifiers. Likewise, this equation can also be used predict the emitter inductance in the uncoupled amplifier that is required to match the return difference for the coupled amplifier, from a given set of circuit parameters. For the coupled amplifier parameters listed in Table 3-1, an emitter inductance for the uncoupled amplifier of 1.7 nH is predicted to give a return difference for the uncoupled amplifier that equals the return difference for the coupled design. Of course, the same active device operating under identical bias conditions must be used in both amplifier configurations. Under these conditions, the linearity of the uncoupled amplifier should be comparable to the linearity of the transformer-coupled LNA.

4.1.3 The Uncoupled Amplifier Design

Given a value of emitter inductance for the uncoupled amplifier which will result in a similar amount of negative feedback for both coupled and uncoupled preamplifiers, the remaining component values for the uncoupled amplifier must be selected in order to perform a quantitative comparison of preamplifier performance. It is important that the circuit components are chosen in such a way that one design is not favoured over another. The components selected for the uncoupled amplifier are listed in Table 4-1. The components chosen for the sample analysis of the transformer-coupled preamplifier in Chapter 3 of this thesis (refer to Table 3-1), are also assumed here for the coupled preamplifier circuit. Also, the amplifier bias point and the small-signal transistor parameters assumed in the analysis from the third chapter (also from Table 3-1) will be used here as well.

The collector inductance for the uncoupled amplifier which is listed in Table 4-1 was selected so that a Q-factor that is close to the optimum for the BiCMOS process at 1.9 GHz would be realized. This results in a large impedance at the collector when the load is resonant-tuned, and under these conditions the gain for the uncoupled amplifier is

close to its maximum. The collector load of the uncoupled preamplifier is resonated with the capacitive portion of the complex load impedance, Z_{Luc} (uncoupled load) in Figure 4-1, in order to match the output of the preamplifier to the load. Simulations of monolithic inductors using the GEMCAP2 model for the microstrip inductor have shown that a monolithic inductance of 5 nH will have peak Q close to 1.9 GHz, so this inductance value was selected for the collector load of the uncoupled amplifier. A Q-factor of 5 was assumed for both the collector and emitter inductors in the uncoupled amplifier design, which is slightly optimistic for the BiCMOS process. Knowing the inductor Q-factor and the inductance, the dissipation at 1.9 GHz for the simplified model of the inductor (R_{dC} and R_{dE} in Figure 4-1(a)) is easily computed using equation 2.1 (i.e., the equation defining inductor Q).

Table 4-1: Uncoupled circuit and bjt parameters used for comparison.

Circuit Parameter (see Figure 4-1(a))	Value	Transistor Parameter (see Figure 3-6)	Value
V_{CC}	1.9 V	Emitter Area	$0.8 \times 120 \mu\text{m}^2$
I_{CC}	2.0 mA	g_m	76 mS
I_{BB}	22.7 μA	r_π	1140 Ω
L_{CC}	5.0 nH	C_π	1800 fF
R_{CC}	12.5 Ω	C_μ	240 fF
L_{EE}	1.7 nH	C_{CS}	240 fF
R_{dE}	4.0 Ω	f_T	5.9 GHz

4.1.4 Simulated Amplifier Performance Comparison

The amplifier power gain is maximized when the preamplifier input and output are matched to the source and to the load, respectively. The maximum power gain for each preamplifier (coupled and uncoupled) has been determined from small-signal simulation, and the results are plotted in Figure 4-3. It is also useful to include the power gain of the

Figure 4-3: Simulated maximum available gain for the common-emitter bjt and the coupled and uncoupled preamplifiers.

grounded-emitter bjt as a benchmark for comparison, and thus the maximum stable power gain for the bjt without feedback is also plotted on the Figure. The bjt bias conditions used to derive these results are identical to those used for the two LNA designs ($V_{CE} = 1.9$ V, $I_C = 2$ mA). The coupled and uncoupled preamplifiers are absolutely stable for all operating frequencies, consequently the power gain curve shown in the Figure represents the maximum gain available from each amplifier in the matched condition. Transformer feedback in the coupled preamplifier stabilizes and levels the power gain available from the bjt, at the expense of some gain reduction caused by the application of negative feedback. Emitter degeneration in the coupled preamplifier also stabilizes the amplifier, however, there is a significant reduction in the maximum power gain which can be obtained for approximately the same amount of feedback. It should also be noted that an impedance matching network will be required to interface the high impedance at the uncoupled amplifier output (i.e., the collector tank circuit at resonance) to the input of the following stage (usually a 50 Ohm load). The coupled design should not require any additional matching components at the output when driving a low impedance load if properly designed.

The emitter degeneration inductance (L_{EE} and R_{dE} in Figure 4-1(a)) which results in the same third-order intercept point for the uncoupled as for the coupled amplifier was determined from a computer simulation of the non-linear models for each preamplifier circuit. From a harmonic balance simulation, it was determined that an uncoupled amplifier with an emitter inductance of 2 nH in series with a resistance of 5 Ohms (i.e., Q factor of 5 at 1.9 GHz) yields the same third-order intercept as simulated for the coupled amplifier. This is slightly larger than the 1.7 nH predicted from equation 3.38, however, there are a number of factors which were neglected in the simplified computation of the emitter inductance, such as non-linearity of the transistor current gain, non-linearity of the collector-base capacitance, and the effect of the source impedance upon the amplifier distortion characteristics.

The simulated performance of the coupled and uncoupled amplifier designs is summarized in Table 4-2. From the data listed in the Table it can be seen that the maximum power

gain of the coupled preamplifier is approximately 4.5 dB greater when transformer coupling is used to implement the degenerative feedback. This result was simulated at a bias current of 2 mA and a supply voltage of 2 V, for identical amplifier input intercept points.

Table 4-2: Performance comparison for coupled and uncoupled amplifiers at 1.9 GHz.

Specification	Transformer-Coupled Amplifier	Uncoupled Amplifier ($L_{CC}=5\text{nH}$, $L_{EE}=2\text{nH}$, Q-factor =5)
Bias current, I_{CC} , in mA	2 mA	2 mA
Input TOI (unmatched), in dBm	0.5 dBm	0.5 dBm
Gmax at 1900MHz	10.8 dB	6.2 dB
I_{CC}/L_{EE} for equal Gmax and TOI at 1900MHz	-	3.7 mA with 1.4nH L_{EE}
TOI at input for equal Gmax and I_{CC} at 1900MHz	0.5 dBm	-7.3 dBm
Minimum noise figure for equal TOI and I_{CC}	2.1dB	2.3dB

The improvement in performance offered by transformer coupling may be quantified in a number of different ways, and some of these alternative measures for comparing performance are also listed in Table 4-2. The coupled amplifier achieves the same power gain and linearity as an uncoupled amplifier requiring almost double the bias current. To obtain this comparison, the bias current and the emitter degeneration inductance of the uncoupled amplifier was varied in simulation until a maximum power gain of 10.8 dB was obtained at an input intercept point (TOI) of +0.5 dBm. An increase in bias current of 1.7 mA was required in order to achieve this, as listed in the fourth entry of Table 4-2. The simulation results also demonstrate that transformer coupling offers an 8 dB improvement in the input third-order intercept point, when coupled and uncoupled amplifiers with the same maximum power gain and bias current are compared (see the fifth entry in Table 4-2). The degeneration inductance at the emitter of the uncoupled amplifier was decreased to 0.5 nH in order to equalize the power gains of the coupled and uncoupled amplifiers. When this is

done without adjusting the bias current of the uncoupled amplifier, the input intercept point drops by 8 dB to -7.3 dBm as shown by the data listed in the Table. These result indicates that transformer coupling improves the efficiency of the preamplifier, by offering lower power consumption for the same linearity and power gain, or alternatively, greater linearity for the same gain and power consumed.

The minimum noise figure predicted from simulation is almost identical for the two amplifiers. However, the coupled amplifier would yield a better noise figure for the receiver overall. This is because the higher power gain from the transformer-coupled LNA will suppress more of the noise generated by the mixer and the other components in the receive chain. The lower gain of the coupled amplifier is less effective in suppressing noise sources in the mixer and from the other post-mixer stages in the receiver.

4.1.5 Comparison of Power Gains for the Coupled and Uncoupled Amplifiers

The large difference in the maximum power gain between the coupled and uncoupled amplifiers will be investigated by examining the characteristics of each circuit, and then determining which parameters of the uncoupled circuit contribute to the comparatively low power gain observed in simulation. In order to achieve this insight, the amplifier power gain must be expressed in terms of circuit quantities such as voltage gain and the terminal impedances. The analysis from Chapter 3 will therefore be used to model the circuit performance and a comparison will be made between the coupled and the uncoupled designs.

The power gain of an amplifier is defined by the equation

$$\text{Power Gain} = \frac{\text{Power Absorbed by the Load}}{\text{Power Input to the Amplifier}} = \frac{\text{Re}\left(V_L I_L^*\right)}{\text{Re}\left(V_{in} I_{in}^*\right)} \quad (4.3)$$

where V_L and I_L are the load voltage and the current flowing through the load, and V_{in} and I_{in} represent the input voltage and the current flowing from the source, respectively. This power ratio can also be expressed in term of the series equivalent input impedance, Z_{in} ,

and the series equivalent load impedance, Z_L , as follows

$$\text{Power Gain} = \frac{|V_L|^2 R_c(Z_L)}{|Z_L|^2} \cdot \frac{|Z_m|^2}{|V_m|^2 R_c(Z_m)} \quad (4.4)$$

The ratio

$$\frac{R_c(Z_L)}{|Z_L|^2} = \frac{1}{R_L} \quad (4.5)$$

where R_L is the real or resistive portion of the shunt equivalent load impedance. Thus, equation 4.4 can be re-written in terms of the shunt equivalent resistances of the amplifier input, r_{pi} , and the load resistance as

$$\text{Power Gain} = \frac{|V_L|^2 r_{pi}}{|V_m|^2 R_L} = \frac{|A_v|^2 r_{pi}}{R_L} \quad (4.6)$$

A conjugate match at both the input and output of the amplifier will result in the maximum available power gain as described previously. In the matched condition, the output matching network will transform the load impedance to match the real part of the amplifier output impedance, r_{po} . Thus, equation 4.5 can be written in terms of the maximum available power gain as

$$\text{Maximum Available Power Gain} = \frac{|A_v|^2 r_{pi}}{r_{po}} \quad (4.7)$$

Equation 4.6 expresses the maximum power gain in terms of the amplifier voltage gain, A_v and the real components of the amplifier input and output impedances. These parameters for the coupled and uncoupled amplifier designs are listed in Table 4.3 for comparison.

Table 4-3: Gain and terminal impedance data at 1900 MHz.

Parameter	Transformer-Coupled Amplifier	Uncoupled Amplifier ($L_{CC}=5\text{nH}$, $L_{EE}=2\text{nH}$, Q-factor ≈ 5)
Shunt equivalent input resistance, r_{Pi}	170 Ω	57.0 Ω
Shunt equivalent output resistance, r_{Po}	61 Ω	140 Ω
Magnitude of Forward Voltage Gain, A_v	2.15	3.36

The voltage gain of the uncoupled amplifier is larger in magnitude than the voltage gain of the coupled amplifier, while the power gain of the coupled amplifier is substantially larger than the power gain of the uncoupled amplifier (as seen in Figure 4-3). However, it should be realized that the output load resistance for the uncoupled amplifier is more than twice as large as the load for the coupled amplifier (i.e., 140 vs. 61 Ohms as listed in the Table). As a result, the power delivered to the load for a given input signal level,

$$\text{Power Output}|_{V_{in}} = \frac{|V_o|^2}{r_{Po}} \bigg|_{V_{in}} = \frac{|A_v|^2}{r_{Po}} \quad (4.8)$$

is virtually the same for both designs.

The voltage gain for both amplifiers was shown to be proportional to the load impedances in Chapter 3 of this thesis (see equation 3.27). Hence, it might be expected that the power output defined by equation 4.7 would favour the uncoupled amplifier, because the load impedance for this amplifier is larger when matched. However, the forward gain of the uncoupled amplifier is reduced by the signal fed-forward through the collector-base capacitance (C_μ) of the bjt. The signal fed-forward via C_μ in the coupled design is partially cancelled by the signal fed-forward through the transformer, and thus the voltage

gain for the coupled amplifier is less affected by the collector-base feed-forward path. As a result, the coupled amplifier can deliver a comparable amount of power to the load despite having a lower output impedance.

The input impedance must also be considered. The coupled amplifier has a larger input impedance and so it requires less power to realize a given input signal amplitude. As a result of this, the transformer-coupled amplifier requires less input power from the source in order to deliver a comparable amount of output power to the load, hence it has a higher maximum power gain.

4.1.6 Summary of the Amplifier Comparison

These results demonstrate that there is a clear advantage in preamplifier performance that is realized by coupling the collector and emitter loops with a monolithic transformer. The simulation results presented in this section have shown that a 1.9 GHz transformer-coupled preamplifier will produce over 4 dB greater maximum available power gain than a two-inductor (uncoupled) amplifier with comparable noise figure, power dissipation and linearity.

The feedback introduced by mutual magnetic coupling comes at the expense of a decrease in isolation between the input and the output of the amplifier. However, it should be noted that collector-base feedback via the parasitic depletion capacitance of the bipolar transistor has a significant effect upon a low-noise bipolar preamplifier operating at low current in order to conserve power. The collector-base capacitance is significant because a large emitter area is required to minimize thermal noise from the transistor in most sub-micron silicon VLSI technologies. The feedforward through the collector-base capacitance that is implied by a large area device can be neutralized by the signal fed-forward through the transformer, resulting in a net improvement in the overall signal isolation for the preamplifier. This option is not available to the designer of a two-inductor preamplifier.

The differences in maximum power gain between the uncoupled and coupled amplifi-

ers were shown to be the result of the application of feedback in each case, and the effect of this feedback upon the amplifier's terminal impedances. In the case of the coupled amplifier, feedback via the transformer tends to lower the real part of the output impedance and raise the real part of the input impedance (for the parallel equivalent circuit model). Emitter degeneration has little effect upon the output impedance of the uncoupled amplifier, and therefore an external matching network is required in order to realize the maximum available power gain into a 50 Ohm load. Impedance matching to a low impedance load at the coupled amplifier output does not require a separate matching network, because the real portion of the output impedance is very close to the desired load impedance (i.e., 50 Ohms).

An inductance connected in series with the emitter can be used to achieve a near 50 Ohm (real) impedance at the input to the uncoupled amplifier. However, it is likely that due to packaging and on-chip component tolerances, some tuning is required in order to achieve a good quality impedance match between the source and the preamplifier input in manufacture (e.g., a return loss of greater than 15 dB). Thus, the requirement for an input impedance matching network for the coupled preamplifier is not a serious disadvantage of the design.

4.2 Transformer-Coupled Preamplifier Design

The objectives for the preamplifier in a hand-held portable receiver application were discussed in Chapter 1 of this thesis. For this work a preamplifier power gain of approximately 12 dB was chosen as a compromise between the overall receiver sensitivity and the input signal level which will overload the first down-converting mixer.

The spurious free dynamic range of the receiver is the single most important performance specification for the receiver front-end. It is defined by the difference between the overload point and the minimum discernible or acceptable signal level at the RF input. The minimum signal level, or receiver sensitivity, is determined by the receiver noise fig-

ure (NF), which can be estimated from Friis' formula [19]. The upper limit of the receiver dynamic range is usually determined by the distortion and gain compression characteristics of the first down-converting mixer, when the preamplifier gain is sufficient to suppress the mixer's noise.

The selection of component values for a preamplifier design that meets the target specifications for a hand-held cordless receiver application will now be outlined. A transformer-coupled circuit, as shown in Figure 4-4 (complete with input matching network and bondwire parasitics), will be used to exploit the advantages described in the previous section for transformer coupling.

Selection of the bias point and emitter area for bipolar transistor Q_1 is the first step in the design process. The transit frequency (f_T) and transconductance of the bjt depend upon the choice of bias current, I_{CC} . Device parasitics, which are important to the RF performance specifications such as the noise figure, terminal impedances, and bandwidth for the preamplifier, are influenced by the collector bias voltage and the emitter area of the transistor. The bias conditions are determined in part by the available supply voltage, but also by the limited amount of current which can be supplied by a battery in a portable receiver with small physical dimensions. Thus, the selection of the bias conditions and the active device size are crucial to the preamplifier performance.

Once the bias point and the active device have been chosen, a transformer must be designed in order to implement the coupled-feedback network. The feedback will have an influence upon the power gain and linearity of the amplifier, as discussed in the previous sections of this chapter. Hence, the transformer design must be optimized for the best possible performance given the desired amplifier specifications. Since the coupled preamplifier is a narrowband design, the amplifier must be tuned in order to achieve the maximum linearity and transfer of power from the input to the output. Consequently, the selection of reactive component values needed to implement the input matching and output load networks will then be described, completing the design.

Figure 4-4: Transformer-coupled preamplifier schematic diagram.

4.2.1 Device Selection for Low Noise

The dominant noise sources in this amplifier are thermally generated noise from the base resistance of Q_1 and shot noise generated by the flow of bias current in the collector. The collector load resistor (R_C) shown in Figure 4-4 is used to match the impedance at the collector of Q_1 to the load. The resistance required in an actual circuit is large relative to the load impedance (50 Ohms is assumed here for the load), hence its contribution to the amplifier noise figure is negligible because it appears at the output. Resonant-tuning of the collector circuit adds some flexibility in the choice of the emitter area for Q_1 by resonating out stray capacitances, which is important when attempting to optimize the stage for the best possible noise figure.

In addition, the Ohmic losses of the monolithic transformer are small, and consequently the losses due to the transformer have a minimal effect upon the amplifier noise figure. The primary winding of a step-up transformer designed for a coupled preamplifier will have a dissipation on the order of one Ohm or less, because the primary is typically constructed from a number of turns connected in parallel. For example, the primary winding of a 1:4 step-up transformer would consist of 4 turns of a planar spiral connected in parallel. Thus, the dc resistance of the primary, which appears in the input loop of the amplifier, is very small and it contributes little to the overall noise figure. The dissipation of the transformer secondary winding appears at the amplifier output, and assuming sufficient gain in the preamplifier design, it too can be neglected. Since the noise figure of the bjt is not degraded significantly by the dissipation of the monolithic transformer, the minimum noise figure of the preamplifier is almost completely dependent upon noise generated within the bjt (i.e., the thermal and shot noise). Therefore the minimum noise figure of the bjt alone and the minimum noise figure for the complete preamplifier (assuming a nearly lossless feedback network) are nearly equal.

An analysis of the noise figure for the complete preamplifier is complicated by the number of feedback paths within the amplifier, however, the equivalent source representation for the bjt, which was also presented in the third chapter of this thesis, reveals that

aside from the transistor noise sources, the current gains (dc and ac), and the impedance seen at the emitter have a strong influence upon the noise figure of an amplifier in the common-emitter configuration.

Since the relative contribution of the transistor noise sources to the overall signal-to-noise ratio depends upon the source impedance seen at the transistor input terminal (i.e., as seen from the base of Q_1 in Figure 4-4), there is an optimum source impedance which will result in the lowest noise figure. In general, this optimum noise match is not equal to the conjugate of the transistor input impedance that would be required for maximum power transfer, as explained in section 3.1.3. An inductor can be placed in series with the emitter lead of the bjt to modify the optimum noise match [75], and under certain conditions the minimum noise figure and the maximum power transfer at the input can be achieved simultaneously, making this approach very attractive. However, a large series inductor is required in practice, and therefore two stages of amplification would be needed to achieve a gain of 12 dB. This increases the circuit complexity and the power consumption, a single-stage amplifier design is preferred.

Thus, the amount of feedback which can be applied to the preamplifier is limited by the constraints of gain and power consumption. With only a small amount of feedback applied, it can be assumed that a transistor selected for the optimum noise figure in the common-emitter configuration (i.e., without feedback) should give close to the optimum noise figure in the final preamplifier design.

Some insight into the optimization of microwave bipolar transistor noise figure comes from an analysis by Fukui [80], who derived an analytical solution for the transistor noise figure based upon the hybrid- π model for the bjt. The results of the analysis show that the minimum noise figure at high frequency for the device can be estimated from the following formulation for the minimum noise figure, $NF_{\min}$,

$$NF_{\min}|_{\text{high frequency}} = 1 + h \left(1 + \sqrt{1 + \frac{2}{h}} \right) \quad (4.9)$$

where

$$h = g_m r_{bb'} \left(\frac{f}{f_T} \right)^2 \quad (4.10)$$

Here it is assumed that the dc and low frequency current gains (β_{dc} and β_o) of the transistor are large. These current gains depend upon a number of factors such as the technology (e.g., base doping), the collector current and the ambient temperature. The dc and ac current gains for a $0.8 \times 120 \mu\text{m}^2$ bjt in the BiCMOS process (i.e., the device used in the previous circuit examples) are both approximately 90 at a collector current of 2 mA, so this condition is normally fulfilled. There is an additional restriction; the dc current gain should satisfy the following condition

$$\beta_{dc} > 10 \left(\frac{f_T}{f} \right)^2 \quad (4.11)$$

Assuming that the ratio of the operating frequency to the transit frequency is less than one-third, and a dc current gain of 90, this restriction will also be satisfied.

Fukui's estimate for the high frequency minimum noise figure (equations 4.9 and 4.10) indicate that the collector bias current, which determines the transconductance (g_m) and the transit frequency (f_T) of the device, must be selected in conjunction with the device size in order to minimize the transistor noise figure. As the frequency increases, the factor h also increases, which results in an increase in the minimum noise figure as predicted by equation 4.9 for a typical bipolar device. Thus, the dominant term in the noise figure for a common-emitter amplifier at high frequencies is

$$\text{Noise Figure} \propto g_m r_{bb'} \left(\frac{f}{f_T} \right)^2 \quad (4.12)$$

This is consistent with the dominant noise sources being collector current shot noise (since collector current density determines f_T) and the thermal noise generated by $r_{bb'}$, as previously outlined in Chapter 3 of this thesis. At a given frequency, temperature and bias

current, only $r_{bb'}$ and f_T in equation 4.12 will vary with emitter area. Thus, the device emitter area can be increased in order to reduce $r_{bb'}$, until the collector current shot noise causes an unacceptable degradation of the noise figure because of a reduction in the transistor f_T .

The trade-offs involved in the device selection for the preamplifier can be illustrated by comparing the 50 Ohm noise figure for various transistor emitter areas and bias currents. The results of this investigation are summarized in the plots of Figures 4-5 and 4-6, which were generated from computer simulations using the SPICE Gummel-Poon model for the bjt.

The 50 Ohm noise figure for $0.8 \times 60 \mu\text{m}^2$ (15X minimum size) $0.8 \times 120 \mu\text{m}^2$ (30X) and $0.8 \times 180 \mu\text{m}^2$ (45X) emitter areas is plotted as a function of frequency in Figure 4-5. The flat portion of the noise figure curve (i.e., below 500 MHz) corresponds to the region where the noise figure is dominated by the thermal noise introduced by the base resistance of the transistor. As the emitter area of the bjt increases, the base resistance decreases, causing the noise figure to improve at low frequencies for a larger emitter area transistor and a constant collector current of 2 mA. As the operating frequency begins to approach the device f_T , the gain of the transistor begins to decrease and hence the collector current shot noise begins to dominate. For a constant collector current, the transistor transit frequency is lowest for the larger area devices, and therefore the noise figure of the 45X transistor increases more rapidly with frequency than the other transistor designs, as seen in Figure 4-5. Within the DECT frequency band (i.e., 1900 MHz), it is clearly shown in the Figure that a 30X transistor has the lowest 50 Ohm noise figure for a 2 mA bias current.

The variation of the 50 Ohm noise figure with bias current and frequency for the 30X transistor is plotted in Figure 4-6. The noise figure at low frequencies is inversely proportional to the collector current, which indicates that the low frequency behaviour is dominated by both the base resistance and the collector current shot noise when the transconductance of the bjt is small (i.e., below 2 mA). This behaviour is predicted by the input equivalent voltage source for the bipolar transistor (refer to equation 3.6), as

Figure 4-5: Noise figure as a function of frequency for various device sizes biased at a constant current of 2 mA.

Figure 4-6: Noise figure as a function of frequency for a 30X transistor at different collector bias currents.

described in Chapter 3 of this thesis. The input equivalent voltage source dominates the low frequency behaviour when the source impedance is low, which is the case here for a 50 Ohm source impedance. At high frequencies (i.e., above approximately 1500 MHz), the transistor parameters that dominate the noise performance are related by equation 4.12. As the collector current increases from 1 mA to 4 mA, the transit frequency of the transistor initially increases with the increase in bias current, however, a region of almost constant f_T is quickly reached. In this regime, the capacitance implied by charge diffusing through the base of the transistor dominates the frequency dependence of the current gain, and the f_T becomes almost constant with changes in the bias current. Equation 4.12 predicts that the high frequency noise figure of the transistor in this case will depend only upon frequency and the transconductance, behaviour which is supported by the simulation results plotted in Figure 4-6 for frequencies above 2 GHz. The simulations show that in this frequency range, a bias current of approximately 2 mA will result in the minimum 50 Ohm noise figure for the 30X device.

The number of emitter stripes used in the device design was also investigated. The base resistance for a given emitter area can be reduced by using a large number of transistors with short emitter stripes connected in parallel. This is commonly done in low frequency designs, where a much larger base area will be used in order to minimize $r_{bb'}$ at the expense of increased collector-base capacitance [81]. However, it was found in this case that multiples of the longest possible emitter stripe produced the best noise performance at a low bias current. This optimum is rather broad and is not critically dependent on the number of emitter stripes used or the total emitter area.

Power gain at the desired bias current must also be considered in the device selection process. The 15X and 30X devices will both produce a power gain of better than 12 dB at 1.9 GHz when simultaneously matched in a 50 Ohm system and biased at 2 mA. However, the maximum power gain of the 45X device is barely 12 dB, which does not leave sufficient margin for the losses introduced by the transformer and the impedance matching networks used in the low-noise amplifier. The simulated maximum stable gain for a com-

mon-emitter and the transformer-coupled amplifiers using a 30X transistor biased at 2 mA are shown in Figure 4-2. At 1900 MHz, the power gain of the transformer-coupled amplifier is close to 11 dB, while the common-emitter amplifier will produce a power gain of approximately 14 dB at the same frequency and bias current. A $0.8 \times 120 \mu\text{m}^2$ emitter area transistor (i.e., 30X) was selected for the preamplifier because it produces sufficient gain and also the least amount of noise at a low (i.e., 2 mA) bias current.

4.2.2 Step-Up Transformer Design

The next step in the design process is to specify the parameters for the step-up transformer, T_1 , as shown in Figure 4-4. The three parameters which must be determined are the primary and secondary self-inductances (L_{11} and L_{22} respectively) and the mutual inductance between the windings, M . The coupled amplifier topology uses the transformer to provide negative feedback from the amplifier output back to the emitter of transistor Q_1 , which influences the gain and linearity of the amplifier as previously described. Thus, the parameters of the transformer must be carefully chosen in order to meet the desired specifications for power gain and linearity.

The transformer turns ratio, n , which is defined by equation 3.16 in terms of the transformer self-inductances, is chosen to achieve the desired amplifier power gain. The base-emitter impedance of the transistor, which is predominantly capacitive at RF for the 30X device, is made resonant with an inductance placed in series with the base lead when the source is impedance matched to the amplifier input. It was shown in section 3.2.2 of Chapter 3 that when this is the case, the amplifier power gain is approximately equal to the square of the transformer turns ratio (i.e., n^2) near the resonant frequency. Thus, the turns ratio can be defined in terms of the desired power gain, and this is used to (partially) determine the self-inductances of the transformer. A power gain of 12 dB requires a turns ratio of 4, and therefore

$$n = 4 = \sqrt{\frac{L_{22}}{L_{11}}} \quad (4.13)$$

from equation 3.16.

The secondary of the transformer will be resonant-tuned using a capacitor placed in parallel with the secondary winding (i.e., C_S in Figure 4-4). The transformer secondary should be designed so that the Q-factor of the winding is close to maximum at the desired operating frequency. In this way, the dissipation at the amplifier output caused by losses in the metallization and the conductive substrate, which define the finite Q of the transformer, will have the least effect upon the amplifier performance. This information can be determined from simulations using the GEMCAP2 model for the microstrip transformer, which was described in Chapter 2 of this thesis. For the substrate and metallization parameters of the BiCMOS process used in this study, a secondary inductance of 5 nH yields close to the optimum Q-factor at 1900 MHz.

The desired third-order intercept point for the preamplifier can be used to determine the mutual or magnetizing inductance of the transformer from the analysis of linearity presented in Chapter 3 of this thesis (refer to equation 3.40). There is a relationship between the linearity of the amplifier and the magnitude of the impedance seen at the emitter of Q_1 for both coupled and uncoupled amplifier designs, as discussed in section 4.1.1 of this chapter. As a first step, a simulation of an uncoupled amplifier circuit is used to define the magnitude of the emitter impedance which will yield sufficient linearity at the desired operating frequency. Assuming that the output of the coupled preamplifier is resonant-tuned, the mutual inductance, M , which will result in the same emitter impedance for the coupled amplifier is estimated using equation 3.40. The imaginary component of the load impedance that is specified in equation 3.40 is related to the self-inductance of the transformer secondary winding, since

$$j[Im(Z_L)] = (j\omega L_{22})^* \quad (4.14)$$

at resonance. The magnetizing inductance is defined as,

$$M = k\sqrt{L_{11}L_{22}} \quad (4.15)$$

where k is the coefficient of coupling, which quantifies the reduction in mutual magnetic coupling between transformer windings caused by leakage of the magnetic field in the planar transformer structure. The coefficient of coupling for a monolithic transformer is typically between 0.7 and 0.8, depending upon the layout of the primary and secondary windings. Combining equations 4.13 to 4.15, the imaginary component of the load impedance required to resonate with the transformer secondary self-inductance can be expressed as a function of the turns ratio and the coefficient of coupling, k , and the magnetizing inductance at the transformer secondary as follows

$$j[Im(Z_L)] = \left(\frac{n(j\omega M)}{k} \right)^* \quad (4.16)$$

Substituting equation 4.16 into equation 3.40, and assuming an appropriate value for the coupling coefficient, k , the magnetizing inductance required to achieve the impedance Z_{em} at the emitter of Q_1 can be computed. For the parameters chosen in this design, the magnetizing inductance will yield a much higher third-order intercept than demanded by the DECT specification. It is possible to modify the transformer layout to reduce the coefficient of coupling and decrease the magnetizing inductance, if desired. The gain would no longer be limited to the turns ratio in this case, and a larger gain could be realized if desired. However, it is expected that a portable radio receiver operating in a typical environment, such as an office building, will be limited in performance by the distortion caused by interfering signals (both co-channel and adjacent channel interferers). Hence, the third-order intercept of the preamplifier should be kept as large as possible in order to improve the robustness of the receiver in the presence of interference. Thus, the magnetizing inductance in this design will be made as large as possible by using the minimum spacing between conductors in the planar transformer layout. This ensures the maximum possible feedback between the output and the input of the amplifier, and a high third-order intercept. This should also improve the stability of the amplifier with respect to variations in the circuit parameters, as is well-known for negative feedback amplifiers.

4.2.3 Input and Output Impedance Matching

The series inductor (L_i in conjunction with the bondwire inductance L_{bond} Figure 4-4) and a shunt capacitor (C_i) transform the impedance of the source as seen at the base terminal of the preamplifier. The source impedance transformation can be used to optimize either the power gain or the noise figure of the LNA. At the amplifier output, the collector load resistor and capacitor (R_C and C_S) are used to impedance match the amplifier output to the load.

The input matching components (i.e., L_i and C_i) could be chosen to strike a compromise between the amplifier noise figure and the quality of the input impedance matching. However, without a good impedance match between the antenna and the LNA input, additional components would be required for antenna-amplifier isolation which increases receiver cost, size and weight. Therefore, a high quality impedance match is needed in order to transfer as much power from the antenna as possible without reflections. In this design the LNA input is impedance matched to the source, and there is a slight increase in the noise figure as a result.

At the input, the source resistance, R_{src} , must be matched to the resistive component of the preamplifier input impedance, R_{series} . The input impedance of the preamplifier from a SPICE simulation at 1900 MHz is listed in Table 3-2 (i.e., for a matched, or 50 Ohm output impedance). The input equivalent circuit consists of a 170 Ohm resistor in parallel with a capacitance of 1.7 pF. This corresponds to a series connection of a 1.8 pF capacitor (C_{series}) and a 13 Ohms resistor (R_{series}) at the same frequency. The source (i.e., the antenna) and the amplifier input can be matched over a narrow band of frequencies using the two matching components shown in the amplifier schematic diagram (Figure 4-4): a capacitor, C_i , which shunts the 50 Ohm source and the series inductor, $L_i + L_{\text{bond}}$. The values for these matching components can be calculated using the standard design procedure for a two-element L-C matching network [73]. These component values are then be entered into a circuit simulator for optimization and refinement of the design.

For the transformer-coupled preamplifier, the bondwire inductance at the amplifier

input (L_{bond} in Figure 4-4) contributes a portion of the series inductance needed at the input (1 nH is assumed here for the bondwire inductance), while the remaining inductance (approximately 4.3 nH) can be realized using either a lumped element inductor or a short section of a transmission line. A shunt capacitance of 2.8 pF is required for C_i , which could be implemented either as a lumped capacitance (i.e., surface-mount chip capacitor external to the IC package) or as an open or short-circuited transmission line stub on a circuit board [61].

A similar two-element matching network is used at the amplifier output (see Figure 4-4), where the inductance is the bondwire in series with the output (L_{bond}) and the matching capacitor shunts the transformer secondary (C_S). The resistive component of the tank circuit at the collector of the bjt is larger than the load resistance for a 50 Ohm load, and thus the matching capacitor must be connected in parallel with the transformer secondary.

The output impedance is strongly affected by the transformer feedback and feedback through the collector-base capacitance, C_{μ} . The output impedance of a bjt without feedback has a large real component due to the small output conductance of the device. Application of negative feedback lowers the output impedance so that an additional matching network is not necessary at the output, simplifying the overall LNA design. When the total capacitance at the amplifier output (which is dominated by the secondary capacitance C_S in Figure 4-4) is made resonant with the self-inductance of the transformer secondary winding, the output impedance of the amplifier is approximately 60 Ohms, real (refer to Table 4-2). Thus, a large value resistance in parallel with the amplifier output (i.e., R_C in Figure 4-4) can be used to trim the output impedance of the amplifier and achieve an impedance match to the (50 Ohm) load. The value of R_C required to achieve this is approximately 280 Ohms.

4.2.4 Amplifier Stability

As explained in section 3.1 of Chapter 3, stability is an important issue in feedback amplifier design, especially at radio frequencies. The preamplifier must be stable for input and output terminations that are drastically different from the intended 50 Ohm source and

load impedances (such as an open circuit) and it must be stable in all frequency bands. The bipolar transistor is potentially unstable at low frequencies where the power gain is large, and hence resistive damping is often added to the matching networks to dampen oscillations, even in single-stage amplifiers. This is undesirable because resistive losses increase the thermal noise level. The transformer feedback network used in this design bandlimits the low and high frequency ranges of the response, ensuring that the amplifier will be absolutely stable even when lossless matching networks are used.

The stability of the preamplifier can be determined using Rollett's stability factor, k , which is defined in terms of the s-parameters of the amplifier by the equation

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (4.17)$$

and Δ is the determinant of the two-port s-parameters,

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (4.18)$$

The amplifier is unconditionally stable if k is greater than one and the magnitude of the determinant, Δ , is less than one. Computer simulations predict absolute stability for this design in all frequency bands, and no oscillatory tendencies have been noted in practice.

4.3 Experimental Measurements and Discussion of Results

A 1.9 GHz low-noise preamplifier (LNA) using passive L-C feedback via a monolithic transformer has been fabricated in a mature silicon BiCMOS process. A monolithic transformer consisting of coupled microstrip lines has been implemented to lower the operating voltage and the current consumed by the receiver preamplifier. In addition to allowing a lower operating voltage, the transformer in the preamplifier is used as a low-loss feedback element that has been exploited to achieve a low noise figure in the preamplifier, while maintaining the benefit of negative feedback to linearize the stage with an acceptable power gain.

The amplifier bias supply shown in Figure 4-4 (V_{BB}) was not included on the prototype front-end testchip and off-chip biasing was used. However, circuits which could be used to implement this bias source on-chip can be found in the existing literature [82,83]. The transconductance of the bipolar transistor must be kept constant with variations in both the supply voltage and ambient temperature, because many of the small-signal characteristics of the amplifier are sensitive to changes in the bjt transconductance. One method of achieving this was presented by Heaney, et al in [84].

4.3.1 Fabrication Process

Northern Telecom's 0.8 μm BiCMOS process was used to fabricate the preamplifier and mixer circuits. Bipolar devices were chosen for the front-end circuit implementation because of their superior unity power gain frequency (f_{MAX}) when compared to MOS devices fabricated in the same technology (refer to Table 3-1 of Chapter 3 for a summary of the 30X bipolar transistor small-signal parameters). These npn bipolar devices are optimized for digital applications with a 5 Volt power supply, and a relatively high transistor transit frequency (f_T) is achieved through the use of a polysilicon emitter contact. However, the area required to electrically contact the extrinsic base region results in large collector-base capacitance and a large base resistance ($r_{bb'}$ for the 30X transistor is approximately 10 Ohms) when compared to bipolar IC processes that are optimized for RF performance. This limits the transistor f_{MAX} and the power gain that can be achieved by a preamplifier connected in the common-emitter configuration, as well as limiting the minimum amplifier noise figure (NFmin). Resonant-tuning using inductance can be used to reduce the effect of transistor parasitics on the circuit performance, but a transistor with a large emitter area is needed to minimize the noise introduced by the base resistance.

4.3.2 Circuit Layout Considerations

A photomicrograph of the low-noise preamplifier test circuit is shown in Figure 4-7. The preamplifier transformer was fabricated using aluminum metal 1 μm thick, with a linewidth of 15 μm and a line-spacing of 1.8 μm . The inverting step-up transformer design consists of a total of 8 turns and measures 400 μm on each side. The secondary

Figure 4-7: Low-noise preamplifier testchip photomicrograph.

winding is a continuous 4 turn spiral and the primary winding consists of 4 single-turns connected in parallel, resulting in the desired 1:4 transformer turns ratio. The active area required by the amplifier is $0.65 \times 0.55 \text{ mm}^2$. The pad configuration used for the LNA testchips was chosen to facilitate both on-wafer characterization using coaxial microwave probes and wirebonding of the IC into a commercially available microwave package.

4.3.3 Experimental Results

The measured and simulated performance of the low-noise amplifier is summarized in the column at the right side of Table 4-4. These experimental measurements were obtained from a packaged device biased at a supply voltage of 1.9 V and a bias current of 2 mA. Both the LNA and mixer were packaged using a commercially available ceramic surface mount package for testing and characterization purposes. Ground path inductance of the preamplifier was minimized through the use of multiple wire bonds between the LNA common connection and the package ground. Simulations show that this emitter-to-ground inductance reduces the amplifier gain but does not affect its stability. Spurious oscillations or other unstable behaviour were not observed during testing of the amplifier.

A noise figure of 2.8 dB was measured for the silicon LNA. A 3.5 nH series inductor (L_i) and a 2.5 pF shunt capacitor (C_i) were connected at the amplifier input as shown in Figure 4-4 to achieve a good 50 Ohm input match (VSWR of 1.2). The minimum noise figure of 2.1 dB was determined from on-wafer measurements of the amplifier using the ATN NP-5 noise measurement system [72]. This data indicates that the noise figure of the amplifier could be further reduced at the expense of the quality of the input impedance match (i.e., higher VSWR) if desired. No attempt was made to impedance match the output of the LNA, however, an acceptable VSWR of 1.4 was achieved with the packaged device.

The third-order intercept point (IP3) characterizes the level of third harmonic distortion generated by the LNA. This transformer-coupled amplifier achieves a high input intercept for the chosen bias current. Harmonic distortion is generated by the non-linear capacitances of the bjt and by the non-linear (exponential) relationship between the collec-

tor current and the base-emitter voltage (i.e., the diode non-linearity). Distortion produced by the diode non-linearity will be higher here because a low dc collector current is used. In addition, a bjt operating at a low bias current has large parasitic capacitances and can therefore generate significant amounts of harmonic distortion, even at low input power levels. A transistor with the same emitter area as that used in the LNA here and operated under identical bias conditions was found to have an input third-order-intercept point of -11 dBm. Thus, an 8 dB improvement in the input intercept point of the device is achieved through the use of transformer-coupled feedback in this amplifier configuration.

Table 4-4: Low-noise preamplifier performance summary.

Low-Noise Amplifier	0.3 μ m GaAs E/D MESFET	0.5 μ m GaAs- JFET	Measured 0.8 μ m Si- Bipolar	Simulated 0.8 μ m Si- Bipolar
Supply Voltage	2.0 V	3.0 V	1.9 V	1.9 V
Supply Current	1.0 mA	4.0 mA	2.0 mA	2.0 mA
Frequency	1.9 GHz	1.9 GHz	1.9 GHz	1.9 GHz
Noise Fig. (50 Ω)	-	2.8 dB	2.8 dB	2.9 dB
Min. Noise Figure	2.0 dB	-	2.1 dB	1.9 dB
Gain	12.2 dB	18.1 dB	9.5 dB	10.5 dB
IP3 (input)	-7.1 dBm	-11.1 dBm	-3 dBm	-3.5 dBm
Input VSWR	1.36	1.5	1.2	1.15
Output VSWR	1.77	3.1	1.4	1.03
Isolation	-	21 dB	21 dB	30 dB

A plot of the measured and simulated amplifier gain is shown in Figure 4-8. The band-pass shape of the LNA frequency response is the result of resonant-tuning the input matching network. The peak gain of 9.5 dB was obtained from the packaged device at a frequency of 1900 MHz. There are slight differences between the experimental measurement and the simulated curves, which can be attributed to modeling errors, tolerances in the input matching network components and losses introduced by the package and test fix-

Figure 4-8: Frequency response of the low-noise amplifier.

ture. The power supply decoupling network causes the measured gain to increase at lower frequencies, where the quality of the ac ground at the transformer secondary is poor.

The amplifier isolation measured for the packaged device is 10 dB lower than predicted by the computer simulation, which was expected. This is because parasitic coupling within the package and the test fixture was not included in the simulation, and there is a significant amount of mutual coupling (both capacitive and inductive) between package leads and bondwires. However, the measured isolation is adequate for wireless receiver applications.

The specifications for two recently reported 1.9 GHz GaAs LNAs are shown in the left column of the Table 4-4 for comparison. The silicon bipolar LNA outperforms the 0.5 μm GaAs JFET preamplifier [85] in all reported specifications except power gain. The LNA fabricated in the fine-line E/D MESFET process demonstrated the best combined noise figure, gain and power consumption specifications as of its publication date [86]. This GaAs IC has approximately 2.5 dB more gain at one-half the supply current of the silicon LNA developed in this work. The GaAs amplifier input intercept point (IP3) is 4 dB lower than the silicon LNA, in part because a small bias current was chosen for the design. However, the quality of the input and output matching of the GaAs amplifier is poorer (i.e., a higher VSWR), and it should be noted that the process used to fabricate the E/D MESFET amplifier [87] is considerably more sophisticated.

4.4 Summary

A monolithic microwave preamplifier designed for low-power hand-held telephone applications has been presented in this chapter. This preamplifier design uses a monolithic adaptation of microwave low-noise amplifier design methods, which were originally developed for resonant-tuned discrete circuits.

The advantages offered by magnetic coupling between the collector and base-emitter loops to implement a feedback network for the preamplifier rather than simple emitter

degeneration were examined in this chapter. The performance of a transformer-coupled preamplifier and a tuned preamplifier design using an emitter degeneration inductance (i.e., an uncoupled preamplifier) were compared using computer simulation. It was shown that the transformer-coupled amplifier achieves a higher power gain for the same bias current and linearity when both input and output ports are conjugately matched to the source and load, respectively. The power gain at 1.9 GHz for the uncoupled amplifier was seen to be 4.5 dB lower than a coupled design with the same third-order intercept point at a bias current of 2 mA. The simulations also predicted that the uncoupled amplifier would require almost double the bias current of the coupled amplifier in order to achieve comparable power gain and linearity. When viewed in terms of an improvement in amplifier linearity, the third-order intercept point of the coupled amplifier (again, from simulation) is approximately 8 dB greater than the simulated intercept point of the uncoupled amplifier with the same maximum power gain and bias current.

A design procedure for the coupled preamplifier was also described. The relationship between the emitter area, bias current and the noise figure for a bjt in the common-emitter connection were outlined, and the transistor for the preamplifier was selected on the basis of its potential for power gain at the desired bias point as well as low-noise performance. It was shown that the specifications for the step-up transformer required by the preamplifier can be determined from the gain and linearity specifications. In addition, resonant-tuning at the transformer secondary was used to improve the amplifier linearity and simplify matching of the output impedance to a 50 Ohm load. A simple two-element L-C matching network is used to match a 50 Ohm source to the preamplifier input port.

The measured performance of the transformer-coupled preamplifier meets or exceeds the requirements of the DECT specification (outlined in Chapter 1 of this thesis) in all respects except gain. The measured gain of 9.5 dB at 2 mA bias current could be increased, if required, by increasing the amplifier bias current. It is estimated that an increase of 50% in the bias current would result in a 2 dB improvement in the gain when the amplifier is properly matched at the input and output. The noise figure with an imped-

ance matched input is slightly below 3 dB, and could improved by approximately 0.75 dB if the source impedance resulting in the optimum figure were used. The linearity of the amplifier exceeds the requirements for DECT at a 2 mA bias current, which would make the hand-held receiver less sensitive to interference when it is used in an actual system. In addition, the power consumption of the preamplifier is below 4 mW when operating from a 1.9 V power supply. This level of performance compares favourably with some recently reported narrowband preamplifier designs fabricated in GaAs technologies, and it is superior to the performance demonstrated by broadband silicon BiCMOS designs.

5. Mixer Design

The RF mixer in a radio receiver is one of the most important and, from a theoretical standpoint, poorly understood components in the radio receiver. The non-linear nature of the mixing process makes analysis of some important performance aspects of the mixer, such as the signal-to-noise ratio, a formidable task. Consequently, discrete mixer circuits have primarily evolved through experimental refinement, rather than a design evolution based upon a solid theoretical foundation and engineering principles. The factors which influence the noise figure of a single diode mixer, for example, have been known since the early days of radio [88,89,90]. However, a consistent theoretical analysis of single-diode mixer noise was not published until 1978 [91].

The present state-of-the-art in discrete and silicon integrated mixer circuits will be reviewed in the first sections of this chapter. The purpose of this review is twofold. The first objective is to gain an understanding of the circuit techniques which can achieve the best possible performance at radio frequencies. The second objective is to identify and analyze the performance limitations of conventional silicon integrated circuit designs. A new integrated circuit mixer is then described which extends the RF performance limits that can be achieved in silicon IC technology. This improvement has been achieved by adapting transformers, which are used to advantage in discrete circuits, into the monolithic circuit design. This use of the monolithic transformer in this application follows on from the development of the silicon transformer CAD models and their successful application in a transformer-coupled preamplifier design, which was presented in the previous two chapters.

The mixer in a radio receiver is an analog multiplier which down-converts the received signal from the radio frequency (RF) band to an intermediate frequency (IF), or directly to the baseband for demodulation and detection [24]. The effectiveness of the

mixer as a down-converter between RF and IF bands is measured by the degradation in signal-to-noise ratio and the distortion of the IF signal. The impedances at the mixer ports must be well-defined and controlled, because in a typical radio receiver implementation, the mixer interfaces with off-chip signals at all three I/O ports. Isolation of large signals such as the local oscillator (LO) from the smaller signals at the other mixer ports, such as the (potentially) tiny received signal at the mixer RF input, must also be considered. This last concern is particularly important in a direct conversion receiver design, as described in the discussion of receiver architectures in Chapter 1. In addition, the power consumption of the mixer circuit in a portable hand-held unit like the cordless telephone must be minimized in order to extend the battery life and “talk time”.

The choice of the circuit topology for the mixer in a cordless radio receiver must satisfy these and a number of other design restrictions. Factors such as cost effectiveness, the intended operating frequency and the system performance specifications provide additional constraints. In general, the optimum mixer performance can be expected from balanced rather than single-ended topologies. Active devices used for mixing usually ensure that there is some gain in the conversion from RF to IF, while passive circuits will have a conversion loss in the mixing process. It is anticipated that the mixer must also be compatible with silicon monolithic technology in order to meet all of the above criteria for cordless telephone applications such as DECT.

The terminology used to characterize high-frequency mixers and some of the common circuit topologies will be outlined in the following section of this chapter. These circuits have been used in both discrete and IC mixer designs. A new mixer circuit is then presented which demonstrates improved RF performance and lower power consumption when compared to the other conventional silicon and GaAs IC mixer implementations.

5.1 Mixer Performance and Characterization

There are a number of unique technical terms that are used to describe the perfor-

mance capabilities of a mixer intended for RF applications [92]. The range of the input signal from the minimum detectable level to the overload point defines the dynamic range. It is customary to specify the upper limit of the mixer dynamic range, or the signal overload point, from the mixer's distortion and gain compression characteristics, while the lower limit (i.e., the minimum detectable signal level) is determined by the mixer noise figure (NF). These limitations define the performance capabilities of the receiver to a large extent, although noise introduced by the mixer is suppressed by the addition of a low-noise preamplifier. Aside from these two main performance specifications, other important mixer characteristics are: the port-to-port signal isolation, the port impedances as a function of frequency and the mixer conversion gain.

The conversion gain (or conversion loss in the case of a passive mixer) is a measure of the efficiency with which the radio frequency (RF) input signal is translated to an intermediate frequency (IF) at the output port. Mixing of the input and local oscillator (LO) signals results in frequency sidebands at the IF port, where the upper and lower sidebands are the sum and difference of the LO and RF frequencies respectively. The amplitude of the desired IF sideband is related to the RF and LO signal amplitudes, however, the LO amplitude is usually maintained constant. Therefore, the conversion gain can be defined as the ratio of the IF sideband power to the RF input signal power at a given power level for the local oscillator.

At low input levels, the signal power at the mixer RF port is linearly related to the upper or lower sideband power level (i.e., the conversion gain is constant). However, the linear operating range of the mixer is limited by a number of factors such as the power supply voltages and the non-linear behaviour of active devices. The 1-dB conversion gain compression point defines the RF input power level that causes a 1 dB decrease in the mixer small-signal conversion gain.

The signal leakage from one port to either of the other two mixer ports is mainly due to circuit imbalances. The mixer port isolation is defined as the ratio of the power input at a given port and the leakage or feedthrough signal power present at another port. High isola-

tion therefore implies that the amount of leakage or feedthrough between mixer ports is small. Port-to-port signal isolation is important to the overall receiver performance. Local oscillator energy appearing at the RF or IF ports could result in unwanted signal radiation (e.g., LO power leakage to the RF port could reach the receiving antenna) or create additional frequency sidebands through mixing action and intermodulation between signals. Proper measurement of RF feedthrough to the IF port and RF-IF port isolation requires that the LO signal be applied to the mixer (with the IF port properly terminated and typical input signal levels) in order to more accurately reflect the actual device operating conditions.

The intermodulation distortion characteristics of a mixer are characterized by the third-order intercept specification. The intercept point is measured by applying two signal frequencies at the mixer RF input (the two-tone test) and observing the third-order distortion products at the mixer IF output. Third-order distortion products are considered important because they fall within the desired channel bandwidth and could interfere with the received signal, as discussed in the introductory chapter of this thesis. The third-order intercept point when referred to the mixer input, is related to the output intercept by the mixer conversion gain.

5.2 Mixer Circuit Topologies for RF Receivers

An ideal down-converting mixer in a radio receiver produces an IF output signal only at the sum and difference frequencies between the RF and the local oscillator (LO) input signals. However, in a practical circuit there are a number of spurious components that are generated by the mixing process, some of which may be suppressed through the use of balanced circuitry. Also, the circuit complexity and the minimum noise figure which can be realized for a given topology are related. An elaborate circuit topology which places more active and passive components and their associated noise sources in the RF signal path and will usually have a higher noise figure [93].

Unwanted mixing products can be suppressed by keeping all of the RF input levels to the mixer as low as possible and the amplitude of the local oscillator as large as possible. This ensures that the desired IF signal will be stronger than all of the undesired components caused by inter- and cross-modulation effects. However, control over the dynamic range of the RF level at the mixer input is usually not implemented in a practical receiver because of cost and reliability considerations. The upper limit on the RF signal is normally determined by the level of third-order distortion produced by the mixer, rather than large-signal compression of the mixer's conversion gain characteristic [92].

Mixer circuits can be divided into three separate classes: single-ended, singly-balanced and doubly-balanced circuit topologies [73]. Examples of diode mixer implementations for these three circuit topologies are shown in Figure 5-1. These circuits are usually implemented using discrete components, although monolithic implementations in Gallium Arsenide (GaAs) technologies have been developed for applications in the 1 to 5 GHz range. All of these diode mixer circuits operate on the same basic principle. A large local oscillator signal switches the diode or diodes in and out of conduction, and the forward biased diode provides a conducting path for the signal from the RF port to the IF port. Switching of the diodes results in a chopping action between the RF input and the IF output at a rate determined by the period of the local oscillator signal. This non-linear chopping of the RF signal at the LO rate generates the desired sum and difference of the LO and RF input frequencies, however, a large number of spurious components are also generated by harmonics of the LO that appear as a result of large-signal switching of the diodes.

The simplest circuit consists of a single diode and three filter networks as shown in Figure 5-1(a). Although there is no inherent isolation between the ports, signal isolation is achieved through the use of filters if the RF, LO and IF frequencies are sufficiently separated. The circuit is simple and has the lowest conversion loss of the three diode mixer configurations shown in the Figure, and therefore it is often used at very high frequencies (i.e., millimetre-wave band) where balun or transformer construction is impractical. How-

a) single diode mixer

b) singly-balanced diode mixer

c) doubly-balanced diode mixer

Figure 5-1: Common discrete RF mixer topologies.

ever, this type of mixer is sensitive to variations in the port impedances and there is little suppression of spurious mixing products. Also, the linearity of a the single diode mixer is poor [93].

Many of the disadvantages of the single-ended diode mixer also apply to the single-ended transistor mixer, which was commonly used in the inexpensive transistorized radios manufactured during the 1960's. The single transistor mixer circuit is capable of high conversion gains when carefully designed (as high as 30 dB in some cases), but the dynamic range and port isolation of the circuit are, like its single diode counterpart, very poor.

A number of high frequency filters are required to isolate each port of a single diode or transistor mixer. Monolithic high frequency filtering is a technology still in the early development stages, and the out-of-band rejection (on the order of 40dB), linearity and power consumption required for the radio receiver application is beyond the current state-of-the art in integrated circuit technology. A large number of external components would be required to implement a single active or passive mixer of sufficient quality for radio telephony applications. This increases the cost and limits the reliability and manufacturability of the circuit.

The balanced mixers offer better port-to-port isolation than is possible with a single-ended circuit, without using high frequency filters. The singly-balanced diode structure (refer to Figure 5-1b) has a slightly higher conversion loss and requires more local oscillator power to operate than the single diode mixer, because the RF and LO signals are divided between two diodes. However, there is some isolation between ports and some suppression of spurious RF and LO input signals, depending upon which port is balanced.

The doubly-balanced mixer topology offers the best performance in terms of port isolation and suppression of spurious products. The diode version shown in Figure 5-1(c) also has the highest conversion loss and requires the most local oscillator power of the three diode circuits shown. It can also handle large signal inputs because input power is divided amongst a larger number of active devices. However, diode mixers are difficult to

integrate in a VLSI technology because fast switching diodes with a low on-resistance are not available in most processes (diode switching speed on the order of a hundred picoseconds is required). The silicon Schottky barrier diode would be suitable for this application, however, these devices are not available in most production silicon technologies [82].

A disadvantage of the diode mixer for portable radio receiver applications is the large local oscillator power that is required to switch the diodes. The diode mixer circuits are passive because bias current is not required to operate the mixer, but in order to maximize the third-order intercept and 1-dB compression point of a diode mixer, a high oscillator drive power is required. Typically, between 10 and 20 mW is required to fully switch the two series connected diodes, which are usually large area devices so that the diode dynamic impedance when forward biased is small. Buffering of the oscillator output at this power level will consume a (theoretical) minimum of 20-40 mW of dc power if a 50% efficient (i.e., linear) buffer is used. This would require between 6 and 12 mA of current from a 3 Volt power supply, and in practice, a buffer capable of driving a low impedance load would probably consume twice this amount of current. In addition to the power consumed by the LO driver, radiation of a large amplitude LO signal within a highly integrated receiver will interfere with other circuitry and impair the system performance. If the buffer is not integrated with the mixer diodes, which is usually the case, then there is the additional expense of the packaging and area on a circuit board required to interconnect the buffered LO to the mixer.

The doubly-balanced diode mixer can be modified by replacing the diode switches with FET switches (either MOSFET or MESFET devices have been used). Little local oscillator power is then required because the LO signal is now applied to the high impedance gates of the FETs, but a large signal swing (especially in the case of the MOSFET) is necessary in order to achieve the desired ratio of "on" to "off" channel resistance [94]. Large area devices are needed to maximize this ratio and thereby minimize circuit losses and noise. This leads to a large LO port input capacitance that causes limitations in the frequency response. As well, large transient currents are required at the LO frequency.

Incomplete switching of the FETs will result in higher levels of intermodulation distortion due to modulation of the ON channel resistance. However, the FET square law I-V characteristic may help reduce the level of odd-order IMD produced at the mixer output.

The most widely used analog multiplier in silicon monolithic technology is based on the Gilbert multiplier circuit [95]. This all-bipolar-transistor multiplier is shown connected as a doubly-balanced mixer in Figure 5-2. The RF input is converted to in-phase and anti-phase signal currents by the differential transistor pair, Q_1 and Q_2 , and fed to the upper four transistors, Q_3 to Q_6 (often referred to as the switching quad), which are driven by the local oscillator signal. Differential to single-ended conversion is normally required at the mixer IF port, because most passive IF filters are single-ended, although a balanced filter could be designed. The IF outputs of the mixer can be buffered to a low impedance load (e.g., 50 Ohm) by a single-ended output buffer circuit, or the differential IF signal can be combined by a passive power combining circuit to drive the following IF stages. The emitter degeneration resistor, R_{ee} , improves the linear range of the RF input differential amplifier and it is connected so that no dc bias current flows through the resistor. This is done to ensure that the voltage drop across all components in the bias current path between the power supply and ground is as large as possible. Even so, the minimum supply voltage (V_{CC}) for this circuit is approximately 3 Volts.

For small input signal levels (on the order of millivolts) at the LO and RF inputs, the circuit of Figure 5-2 functions as a four quadrant analog multiplier. However, in order to minimize the noise contributed by the upper four transistors, the LO input is normally driven with a large amplitude signal. This minimizes the period of time when all four transistors in the quad are in the active region and contribute noise to the IF output. Ideally, the large LO drive signal multiplies the RF signal current at the collectors of Q_1 and Q_2 by a switching function which alternates between +1 and -1 at the LO frequency (ω_{LO}).

The Fourier components of this switching function can be represented by the following series:

Figure 5-2: An IC mixer based upon the Gilbert multiplier.

$$F_t = 4/\pi \cdot \cos(\omega_{LO}t) - 4/3\pi \cdot \cos(3\omega_{LO}t) + 4/5\pi \cdot \cos(5\omega_{LO}t) - \dots \quad (5.1)$$

and the signal current fed to the switching quad for an RF input signal voltage, V_{RF} is

$$I_{CQ_{1,2}} = \frac{V_{RF}}{(R_{ee} + 2r_e)} \quad (5.2)$$

where r_e is the dynamic emitter resistance of transistors Q_1 and Q_2 .

The differential IF signal voltage is given by the product of equations 5.1, 5.2 and the collector load resistance, R_C ,

$$V_{IF}(t) = \frac{V_{RF} R_C}{2(R_{ee} + 2r_e)} (4/\pi \cdot \cos((\omega_{LO} \pm \omega_{RF})t) - 4/3\pi \cdot \cos(3(\omega_{LO} \pm \omega_{RF})t) + \dots) \quad (5.3)$$

The down-converted or difference component at the IF output is of interest for the radio receiver application. The conversion gain is the ratio of the down-converted IF and the RF input signals, which is given by the coefficient of the first term in equation 5.3.

When the LO input signal is zero, the cross connection of the switching quad transistors will cause cancellation of the RF signal at the IF output. Ideal multiplication of the switching function with the RF signal results in no harmonic content at the fundamental frequency of the LO or any of its harmonics, as seen from equation 5.3. Thus, the circuit is doubly-balanced, and both LO and RF signals are suppressed at the IF output by the circuit topology without the need for additional high frequency filtering.

The supply voltage for the Gilbert multiplier is limited to a minimum of approximately 2.5 to 3 Volts, which limits the minimum power consumption for this type of mixer at a given bias current. The Gilbert multiplier has a total of 3 active devices and a load resistor connected in series between the power supplies (V_{CC} and ground in Figure 5-2). The voltage drop from collector to emitter that is required to bias the active devices into the forward active region places a lower limit on the power supply voltage which can be used.

Many of the limitations of the Gilbert multiplier as an RF mixer arise from design constraints imposed by the input differential pair [96]. The linear range of the mixer, for example, is determined by the linearity of the input pair. This is approximately equal to the input voltage required to force all the bias current through one of the two transistors, either Q_1 or Q_2 . It can be shown that this voltage is on the order of the bias current/emitter degeneration resistance product, and hence the linear range of the mixer can be improved by increasing the degeneration at the emitter of the input pair. This could be accomplished by either increasing the total bias current from Q_7 and Q_8 , or by increasing R_{ee} . However, a large bias current increases both the power dissipation and the noise from transistor shot noise sources, and an increase in the emitter degeneration resistance also degrades the signal-to-noise ratio at the IF output. Thus, using emitter degeneration to reduce distortion will increase the noise figure of the Gilbert multiplier and as a result, realizing a dynamic range suitable for radio receiver applications has proven difficult with near-micron silicon production technologies using this circuit.

The bipolar transistor in the Gilbert multiplier adds both thermal and shot noise to the signals being processed, as compared to the diode mixer which has only the shot noise on the diode current contributing to the mixer noise figure. Thermal noise generated by the base resistance of the input pair is important, because the mixer conversion gain cannot be used to suppress this noise source. Thus, for minimum noise figure, the input pair must be designed as a low-noise preamplifier which suppresses noise introduced by the switching quad [97]. However, this design constraint conflicts with the desire for low distortion. A high degree of linearity is needed from the input pair in order to increase the upper limit of the mixer dynamic range. These limitations on amplifier design have been described in section 2.2 of this thesis, where the trade-offs between linearity and noise involved in the design of R-C amplifiers were outlined. These same limitations apply to the design of the Gilbert multiplier input stage.

Another disadvantage of the Gilbert multiplier, when it is used as a high frequency mixer, is the relatively high input impedance of the differential input pair of transistors at

RF. When the mixer RF input is driven from another circuit on the same chip, impedance matching is not an issue. However, the RF signal source for the mixer is an off-chip image-reject filter in current portable radio receiver architectures, such as the one shown in Figure 1-2. When driven by an off-chip source, an impedance match is necessary at the mixer RF input, and off-chip components are required for the best performance (i.e., low dissipation and low tolerance). This increases the receiver parts count and makes an integrated solution less attractive in terms of cost and performance when compared to a discrete implementation, where components can be selected for optimum performance and lowest cost.

Table 5-1: Discrete and silicon integrated doubly-balanced mixer comparison.

Mixer Type	Doubly-Balanced Diode Ring (discrete, Merrimac DMM-2A)	Gilbert-DBM (silicon IC, National Semiconductor)
RF/LO Frequency Range	1500 to 4200 MHz	DC to 3000 MHz
IF Frequency Range	DC to 1000 MHz	DC to 1900MHz
LO power (nominal)	+7dBm (7 to 13 dBm range)	-5 dBm
Conversion Gain	-7.5 dB	6 dB
SSB Noise Figure	7.5 dB	17 dB
Input Third-Order Intercept Pt.	+12 dBm	-8 dBm
LO-to-RF Isolation	25 dB	30 dB
LO-to-IF Isolation	15 dB	30 dB
RF-to-IF Isolation	10 dB	17 dB
Minimum Supply Voltage	N/A	3 V
Supply Current	N/A	10 mA

The performance of a doubly-balanced diode ring mixer and a silicon monolithic Gilbert-type mixer are compared in Table 5-1. The diode mixer offers considerably better RF performance, specifically, a much lower noise figure and higher third-order intercept at the mixer input. The isolation between ports of the mixer is comparable between these two

designs, partly because of the doubly-balanced structure of both these mixers, but also because some circuit trimming is used in the manufacture of discrete mixers. Excellent dynamic range is offered by the diode ring mixer. However, the power needed to drive the mixer LO input is more than 10 dB higher than the Gilbert mixer. Also, a discrete or hybrid component design cannot be integrated with other receiver circuits onto a single IC chip in order to reduce the production costs of the radio receiver.

The Gilbert multiplier is compatible with silicon monolithic technology and it performs adequately as an RF mixer in applications such as the transmitter up-converter, where the mixer dynamic range is not critical to the overall transmitter performance. A higher level of performance must be demonstrated, however, if silicon IC technology is to compete effectively with discrete and hybrid RF circuit technologies in hand-held radio receiver applications. A silicon bipolar mixer which uses an on-chip transformer balun to achieve both a low noise figure and a wide dynamic range will be discussed in the following section of this thesis.

5.3 The Transformer-Coupled Mixer

The design objectives for the hand-held receiver are to minimize the noise figure and distortion produced by the mixer while consuming as little power as possible from the battery. This must be achieved with a small number of external components in order to conserve layout area and to minimize the component and manufacturing costs for the circuit. The Gilbert multiplier has been widely used in silicon IC applications because it does not require high-quality filters at the RF or LO ports to suppress spurious components. Differential pairs are used to convert the single-ended inputs to balanced currents within the mixer, which eliminates the transformers that are used for this purpose in the discrete (diode) mixer implementations. However, the Gilbert multiplier, when used as a down-converting mixer, is limited by the performance of the input differential pair as was discussed in the previous section.

5.3.1 Mixer Design

The transformer-coupled mixer is a new silicon monolithic mixer design, which offers an improvement in performance when compared to the Gilbert multiplier. The input differential pair of the previous Gilbert multiplier circuit acts like an "active" balun circuit, because it splits the RF input signal into two components, one which is in-phase and the other which is anti-phase to the RF input signal. An alternate method of deriving differential signal currents uses a monolithic transformer balun to split the RF input signal into differential components, which are then fed to the switching quad of transistors as shown in Figure 5-3. It will be shown that this circuit configuration retains many of the benefits of the Gilbert multiplier, such as the balanced topology and compatibility with silicon monolithic circuit technology, while allowing more flexibility to design a mixer that has wide dynamic range and operates with very low power consumption.

A balanced circuit is required to obtain good port-to-port isolation and rejection of spurious signals, and the switching quad from the Gilbert multiplier is well-suited to monolithic integration. Transformer coupling of the RF input signal retains the advantages of a doubly-balanced topology while improving upon the performance of the active circuit used to generate differential RF signal currents in Gilbert's multiplier. The radio frequency (RF) input signal to the mixer (see Figure 5-3) is split into in-phase and anti-phase components by balun T_1 . These signals are then fed to the cross-coupled switching quad of transistors, Q_1 to Q_4 . Bias current is fed from current source Q_5 to the switching quad through the centre-tap in the balun secondary. The signal current is chopped by the transistor quad at the local oscillator (LO) rate in order to down-convert the input signal from RF to the desired intermediate frequency (IF). The down-converted RF input signal is buffered to a 50 Ohm load using the on-chip Darlington buffer (Q_6 and Q_7), or alternately, the IF output can be impedance matched using an external matching network (e.g., balun T_2 shown in Figure 5-3). The balun turns ratio for the external matching network is chosen to match the impedance at the collectors of the mixer switching quad and the load at the IF output. Package and bondwire parasitics have a relatively small influence on the IF port matching

Figure 5-3: Doubly-balanced mixer schematic diagram.

and a good impedance match can be achieved through the proper selection of the turns ratio for T_2 and the collector load resistance, R_C .

The input from the local oscillator is terminated on-chip by resistor R_{LO} . Most external microwave sources are single-ended and therefore a single-ended-to-differential signal conversion would be required to couple the generator to the LO input. An external passive balun could be used or another on-chip balun could be designed for this purpose, however, this would require greater chip area. The eventual design goal for a PCS product application is an integrated RF front-end where the local oscillator source (i.e., a voltage-controlled oscillator or VCO) would be integrated on-chip with the receiver front-end. In that case, the differential signal could be derived directly on-chip from the oscillator output without adding another balun at the LO inputs.

The doubly-balanced connection of this mixer will cancel even-order spurious components at the IF output. This is important in a monolithic mixer implementation, where spurious signals can interfere with other circuits integrated on the same IC through parasitic coupling paths. The local oscillator signal (LO) is normally much larger than either the RF or the IF signals, and thus high isolation is necessary between the LO inputs and the other ports to prevent the local oscillator signal from leaking back to the antenna, or overloading the IF circuitry. The LO and IF ports are isolated by the symmetric connection of transistors Q_1 to Q_4 , and matching of these devices in a monolithic context allows an LO-IF isolation of greater than 40 dB to be achieved in practice. The LO and RF ports are isolated by the balun and thus symmetry in the balun response between the inverting and non-inverting ports is necessary to achieve good LO-RF isolation.

The balun T_1 is tuned by capacitors placed in parallel with the primary and secondary terminals. When properly tuned, the source at RF and its associated impedance will appear as a resistor and a voltage source in series at the secondary terminals. The load impedances seen by the two sides of the transformer secondary are the emitters of the switching quad. They can be modeled as an inductor in series with a resistor. The inductive reactance

can be absorbed into the tuning network at the balun secondary, and consequently, only the real portion of this impedance must be matched to the transformed signal source. When this is done, the large-signal emitter resistance defines the transformer load. The emitter resistance depends upon the bias current (via Q_5) and the signal amplitude at the LO input to the mixer.

At a bias current of 2.5 mA, the load at the balun secondary is almost 50 Ohms (resistive) when the LO port of the mixer is driven by a large amplitude sinusoid (-3 dBm input power). This impedance cannot be matched with a 1:1 turns ratio balun because the resistive losses of the transformer windings must be added to the primary and secondary impedances. Modifying the transformer turns ratio to a 4:5 step-up achieved the desired match without altering the bias current.

The source impedance as seen by each pair of transistors in the switching quad, r_{SRC} , can be approximated by the following equation:

$$r_{SRC} = \frac{n^2 \cdot 50 + r_{T1}}{2} \quad (5.4)$$

where 1:n is the balun turns ratio and r_{T1} represents the resistive losses of the transformer windings. Close to ideal behaviour of the transformer can be assumed here because the balun primary and secondary are resonant tuned. The LO inputs of the switching quad are driven with a large amplitude signal, and therefore two of the transistors in the quad are biased in the active region, and the other transistors in the quad are cut-off for a large portion of each cycle (e.g., when LO+ is much larger than LO-, Q_1 and Q_4 are "on" and Q_2 and Q_3 are cut-off in Figure 5-3). The transistors biased in the active mode, operate in the common-base configuration and amplify each phase of the received signal to the intermediate frequency output. The transformed source resistance (r_{SRC}) degenerates the common-base amplifier and extends its linear range of operation. The transformer has been used to advantage here to match the source impedance to the mixer and improve the mixer linearity without causing a significant increase in the overall noise figure. This is because

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no additional dissipation has been added to the circuit other than the losses in the transformer windings, which are relatively small. Linearization of conventional IC mixers, such as the Gilbert-type balanced demodulator, will require the addition of degeneration resistance which causes a large degradation in the mixer noise figure when high linearity is desired.

The noise introduced by the mixing process is difficult to determine analytically [91]. The balun introduces some loss at the mixer input because of dissipation in the windings, but this decrease in the signal-to-noise ratio can be easily computed from linear network theory. However, the non-linearity caused by large-signal operation of the switching quad cannot be treated in a simple way. When the quad is switched hard in either direction, only two of the transistors are active and the circuit is operating in a common-base amplifier configuration. The RF signal coupled to the quad by the balun is amplified to the collector load at the IF outputs. There is some degradation caused by the dominant transistor noise sources of the common-base amplifier, which are collector current shot noise and thermally generated noise from the base resistance. Operating the mixer at a low bias current reduces the shot noise contributed by each active device. However, the switching speed of the transistors in the quad is also important to lowering the noise figure. When the LO inputs are close to the same potential, very little of the signal at the mixer RF input appears at the IF output, because of the balanced circuit connection. All four transistors in the quad are forward biased in this condition and contribute noise to the IF output. Thus, the signal-to-noise ratio at the IF output is very low during the switching interval, and fast switching of the transistor quad is needed to reduce this portion of each LO cycle. Switching speed is not the only consideration, because of the trade-off between emitter area and the base resistance of the bipolar transistor. Careful selection of the emitter area for the transistors in the switching quad is therefore required in order to achieve a good mixer noise figure. A compromise is needed between a small transistor which can switch quickly between states and a larger transistor with less thermally generated noise from the transistor base resistance, $r_{bb'}$.

The non-linear noise analysis capability of a harmonic balance simulator (Hewlett-Packard's MDS simulator) was used to compute the mixer noise figure. From these simulations it was confirmed that collector current shot noise and thermally generated noise from the transistor base resistance were the dominant sources of noise. The relationship between the local-oscillator input signal level and the noise figure was also investigated, and a transistor emitter area for transistors Q_1 to Q_4 in Figure 5-3 was selected which resulted in a simulated noise figure of 10.5 dB (single-sideband). Simulations also predict that the 100 Ohm on-chip termination resistor, R_{LO} , increases the noise figure of the mixer by approximately 1 dB. It is likely that this reduction in noise figure is related to the amplitude of the local oscillator signal appearing at the mixer LO inputs. Increasing the amplitude of the LO signal can decrease the mixer noise figure, because the IF signal-to-noise ratio is dependent upon the switching speed of the transistors in the quad, as previously discussed. Hence the noise figure could be improved by either integrating the LO source on the same chip as the mixer, or by using a reactive matching network at the LO input.

5.3.1 Circuit Layout Considerations

The balun for the mixer was fabricated using the standard BiCMOS process flow (aluminum top-level metal 1 μm thick) with a linewidth of 15 μm and a line-spacing of 1.8 μm . The design of the balun can be clearly seen in the photomicrograph of the complete mixer shown in Figure 5-4. The balun consists of 9 turns of top level metal and measures 425 μm on each side. It is symmetrically wound so that the centre-tap can be precisely located and the losses in both halves of the secondary winding equalized [98]. Primary and secondary microstrip lines are interleaved to maximize the mutual coupling between the windings and each half-turn is interconnected along the horizontal line of symmetry that runs across the centre of the testchip. The mixer occupies a circuit area (excluding bonding pads) of 0.85 x 0.65 mm². The layout of the mixer testchip facilitates both on-wafer characterization using coaxial microwave probes and wirebonding of the ICs into a microwave package.

Figure 5-4: Doubly-balanced mixer photomicrograph.

5.3.2 Experimental Results

The measured performance of the doubly-balanced mixer is summarized in Table 5-2. The mixer was packaged and tested at a supply voltage of 1.9 V and bias current of 2.5 mA. An input power of -5 dBm was used to drive the local oscillator input, giving a single sideband noise figure of 10.9 dB in a 50 Ohm system (i.e., with no additional noise matching network). The LO drive signal was coupled from the single-ended generator output to the differential inputs of the mixer using an external passive balun. A very low RF input VSWR of 1.17 was achieved without additional matching components. The on-chip Darlington buffer was used for initial testing of the mixer at wafer probe. This buffer circuit consumes additional power in order to interface the mixer IF output to a low impedance (50 Ohm) environment, and therefore it is more efficient to use a passive differential-to-single ended matching circuit at the IF port. Thus, an external transformer balun (transformer T_2 in Figure 5-3) was used to match the mixer output to a 50 Ohm load for testing and characterization of the packaged devices.

Table 5-2: Doubly-balanced mixer performance summary.

Mixer	0.5 μm GaAs-JFET	Measured 0.8 μm Si-Bipolar	Simulated 0.8 μm Si-Bipolar
Supply Voltage	3.0 V	1.9 V	1.9 V
Supply Current	4.0 mA	2.5 mA	2.5 mA
RF Frequency	1.9 GHz	1.9 GHz	1.9 GHz
LO Frequency	1.66 GHz	1.8 GHz	1.8 GHz
SSB NF (50 Ω)	10.8 dB	10.9 dB	10.5 dB
Conversion Gain	5.7 dB	6.1 dB	6.3 dB
IP3 (input)	2.3 dBm	2.3 dBm	1.1 dBm
RF Port VSWR	1.2	1.17	1.15
LO-RF Isolation	13 dB	32 dB	80 dB
LO-IF Isolation	5 dB	47 dB	52 dB

Recently reported results for a low-power 1.9 GHz monolithic mixer fabricated in a 0.5 μm GaAs technology are also listed in Table 5-2 for comparison [85]. A 3 V power supply is required by the cascoded transistors of the GaAs mixer and hence that circuit dissipates more power. The noise figure and linearity of the silicon bipolar mixer (indicated by the high third-order intercept point, or IP3 at the input) are comparable to the results demonstrated for the GaAs design. The doubly-balanced configuration used for the silicon mixer, when compared to the singly-balanced GaAs design, resulted in a clearly superior LO-RF and LO-IF port isolation of 32 dB and 47 dB, respectively. As discussed earlier, high LO-IF isolation is desired in order to suppress spurious frequency components at the mixer IF output in a monolithic receiver implementation, and LO-RF isolation is necessary to prevent the LO signal from leaking back to the antenna. The LO-RF isolation of the silicon mixer, while more than adequate, is degraded by parasitic signal paths that exist on-chip, within the IC package and on the test fixture. These signal paths were not accounted for in the simulation. Good agreement between measurement and simulation for all other specifications was obtained from both harmonic balance (Libra) and time-domain (SPICE) circuit simulators.

5.4 Summary

Doubly-balanced integrated circuit mixers are required for down-conversion in a highly integrated radio receiver. The doubly-balanced circuit topology generates fewer spurious components in the mixing process than the singly-balanced mixer, and as a result there are fewer potential interferers emanating from the mixer. These spurious components could disturb the operation of other receiver circuits implemented on the same chip, or leak back to the receive antenna and interfere with other users in the radio system. Doubly-balanced circuits implemented using diodes and discrete transformer baluns offer very wide dynamic range when used in a radio receiver application, however, these mixers cannot be integrated in a low-cost silicon VLSI technology. An alternative to the diode mixer topologies in a BiCMOS process is Gilbert's bipolar analog multiplier. Unfortunately, the

dynamic range of the Gilbert multiplier is hampered by the limitations of the differential input pair of transistors.

The large difference in performance between discrete diode mixers and broadband silicon mixers (such as the Gilbert mixer) which are offered on silicon ICs for radio receivers is a severe handicap to the adaptation of silicon monolithic technology in high performance cellular and cordless radio applications. In this work, a silicon IC mixer has been implemented using a monolithic transformer balun as the input stage to a doubly-balanced switching quad of bipolar transistors. This mixer circuit has demonstrated low-power consumption in a design that is compatible with a production VLSI technology, and it offers performance comparable to low-power singly-balanced mixers fabricated in GaAs technology.

6. Conclusions and Recommendations

Monolithic transformers fabricated using coupled microstrip lines have been used in this work to further the design art of wireless receiver circuits in silicon IC technology. Performance specifications comparable to some recently reported results in GaAs technology were realized through the use of transformers implemented in a production BiCMOS process with standard process metallization. These circuits could be used to implement a portable radio receiver that is compatible with the DECT standard for digital cordless telephones. In addition to allowing an operating voltage below 2 Volts at 1.9 GHz, the monolithic transformer has been exploited as a low-loss feedback element to achieve a receiver preamplifier noise figure of 2.8 dB. The benefit of negative feedback was used to raise the amplifier input intercept to -3 dBm. A monolithic transformer balun has been used to efficiently couple the single-ended input signal from the preamplifier to a doubly-balanced mixer, thereby realizing a +3 dBm input intercept point and a 10.9 dB single-sideband noise figure at a low bias current. The power dissipation for the entire receiver front-end is less than 9 mW, which is a direct consequence of the efficiency offered by narrowband design methods.

At Gigahertz frequencies, monolithic inductors and transformers are required for the implementation of narrow band circuits on a silicon chip, and it has been demonstrated that the electrical behaviour of these components can be accurately described using a lumped-element circuit model. The modeling approach used in this work is based upon a general analysis of microstrip lines, which results in a high frequency model that can be used in a circuit simulator (i.e., the GEMCAP2 model), either for simulation or for optimization of RF circuits on a silicon IC. Examples of inductors and transformers that were fabricated in a production silicon BiCMOS process were presented, and the accuracy of the model was compared to experimental measurements and predictions from 3-D electromagnetic simulations. Excellent results were obtained in both cases, which validates this approach to

component modeling for silicon RFIC design purposes. The model is scalable and provides sufficient accuracy for the design of microstrip components (i.e., inductors, transformers, etc.) on moderate to high resistivity substrates (1 to 10 Ohm-cm or greater).

The performance characteristics of the transformer-coupled preamplifier were analyzed in detail in this thesis, and the advantages of transformer-coupling when compared to simple inductive emitter degeneration in the narrowband preamplifier were quantified. Magnetic coupling was shown to be an important tool which can be exploited to improve the performance of a high-frequency preamplifier, rather than simply a parasitic effect which should be minimized by careful circuit layout practices.

Excellent agreement has been obtained between the predictions of a simplified circuit model and SPICE simulations of the amplifier performance at RF using more elaborate circuit models for the transistor and transformer. However, the design equations which resulted from the complete analysis do not lend themselves to simple insights into the design problem unless some simplifying assumptions are made. Some care is required when utilizing the simplified expressions for the purposes of design at RF and microwave frequencies. It was shown that neglecting the collector-base feedback capacitance, for example, can introduce a large error in the theoretical predictions.

The theoretical formulations derived in this thesis can also be applied to a non-magnetically coupled, but narrowband, amplifier with an emitter degeneration inductance and a tuned collector load. The predictions from computer simulation were not verified experimentally for the uncoupled amplifier in this work. However, it is expected that the close agreement seen between simulation and measurement for the coupled amplifier would also apply to the uncoupled circuit topology.

A companion doubly-balanced integrated circuit mixer using a transformer was described in the thesis and it has also demonstrated low-power consumption in a design that is compatible with a production VLSI technology. The experimental measurements show that this design offers performance comparable to some recently reported singly-bal-

anced mixers fabricated in GaAs technology. In order to realize this level of performance, the mixer circuit incorporates a monolithic transformer balun as the input stage to a doubly-balanced switching quad of bipolar transistors. The doubly-balanced topology generates fewer spurious components in the mixing process than the singly-balanced mixer, which is a desirable property for an integrated circuit mixer. Spurious components could disturb the operation of other receiver circuits implemented on the same chip, or couple back to the receive/transmit antenna and interfere with other users in the system.

The circuit designs developed during the course of this research work lend themselves to a higher level of integration for the radio receiver front-end in silicon technology. It is therefore recommended that a fully-integrated down-converter, perhaps based upon the image-reject architecture, should be pursued to achieve a more fully-integrated, low-cost monolithic radio receiver.

6.1 Recommendations for Further Work

The results of this work have been based upon bipolar devices in silicon technology, however, it appears that sub-micron CMOS devices will also be capable of operating in the low GHz frequency range. Narrowband circuit techniques are also applicable to MOS devices, and the advantages in linearity offered by FET's make these devices particularly attractive for new low-power integrated RF designs. It remains to be seen whether the benefits offered by CMOS will overcome the advantages of silicon bipolar in the 2 GHz frequency band. In such a case, the narrowband design techniques using transformers from this thesis work would carry over well to a CMOS implementation for the radio. Therefore, this would be a very appropriate time to begin a research project on a transformer-based CMOS receiver.

The maximum achievable magnetic coupling was used in the experimental test circuits reported in this thesis, however, magnetic coupling could be used as another design parameter to trade-off power gain, isolation and amplifier linearity specifications. For example, it is possible that some modification of the circuit parameters could achieve a

simultaneous noise and impedance match at the input. This could be used to further reduce the noise figure of the preamplifier. For the BiCMOS process used in this study, it is estimated that the LNA noise figure could be reduced to approximately 2 dB if simultaneous noise and impedance matching were possible. Other design objectives, such as linearity or power gain, could also be optimized by varying the magnetic coupling between the input and output, as well as the other parameters normally available to the designer.

The GEMCAP2 simulator of this thesis can be used to provide valuable insight into the behaviour of microstrip spiral inductors fabricated in silicon. Optimization of the quality factor of inductors fabricated in silicon BiCMOS technology (or other silicon technologies) depends upon the proper selection of the conductor linewidth, line spacing, number of turns, etc. An understanding of the trade-offs involved in the design of spiral inductors and transformers in silicon technology, and how this design space differs from that for microstrip components fabricated on higher resistivity substrates, could be obtained from further study using computer simulation of inductor and transformer performance.

7. References

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