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HYBRID SEMICONDUCTIVE/SUPERCONDUCTIVE MICROWAVE INTEGRATED CIRCUITS

Jeffrey William Smuk, M.Eng.

**A thesis submitted in partial fulfillment of the requirements for the
degree of Doctor of Philosophy**

**Ottawa-Carleton Institute of Electrical Engineering
Department of Electronics
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Carleton University
Ottawa, Canada
December 1991**

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**"HYBRID SEMICONDUCTIVE/SUPERCONDUCTIVE
MICROWAVE INTEGRATED CIRCUITS"**

submitted by Jeffrey William Smuk, M.Eng. in partial fulfillment of
the requirements for the degree of Doctor of Philosophy

Thesis Supervisor (Carleton)

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Carleton University
December 1991

ABSTRACT

This thesis explores hybrid semiconductive/superconductive Microwave Integrated Circuit (MIC) technology that may be applied in future communications and radar systems. The potential for obtaining microwave performance advances by operating conventional semiconductive circuits and the recently discovered High Temperature Superconductor (HTSC) materials at cryogenic temperatures is investigated. Both technologies are successfully combined in the realization of Ku-band hybrid semiconductive/superconductive oscillator and amplifier MICs.

The potential of semiconductive microwave circuit operation at cryogenic temperatures is discussed first. Both MIC and Monolithic Microwave Integrated Circuit (MMIC) technology are described and their limitations are noted. Experiments determining the microwave parameters of three-terminal active devices are performed over temperature.

A novel measurement technique is developed to characterize microwave devices and circuits at cryogenic temperatures. By combining the Through-Reflect-Line calibration technique with a cooled apparatus, fully corrected S-parameters of MIC and MMIC devices are obtained in real time at frequencies up to 20 GHz. A liquid nitrogen immersion apparatus is used to validate the measurement concept at 77K while a cryocooler-based apparatus is employed for extremely accurate measurements at low temperatures. The performance and internal behaviour of FETs, HEMTs and Pseudomorphic-HEMTs are determined at room temperature and 77K. At 77K, some of the devices operate at significantly higher frequencies.

The second area studied is superconductive microwave circuits. Superconductor theory and previous experimental results with Low Temperature Superconductors (LTSCs) are described. Several advantages, including high speed, low power consumption and low noise, are identified. Disadvantages limiting the wide scale application of LTSCs, including 4K operating temperature and low saturation levels of

active devices, are discussed. Experiments comparing the performance of HTSC and similar normal metal passive microwave circuits are carried out.

The cryocooler-based apparatus is used to characterize thin-film circuits at frequencies up to 40 GHz and at temperatures as low as 15K. Transmission responses of HTSC, gold and copper planar passive circuit elements compatible with MIC and MMIC technology are determined. At 77K, passive distributed Ku-band circuits fabricated of HTSC material exhibit over twenty times higher quality factors than similar circuits using conventional metals.

These low loss passive HTSC circuits are combined with three-terminal active semiconductive devices in the design and fabrication of hybrid semiconductive/superconductive Ku-band MICs at 77K. The two technologies are successfully combined in a superconductively-stabilized MMIC feedback oscillator and a superconductively-matched low-noise HEMT amplifier. The oscillator is the first reported to combine MMIC and HTSC components in an assembly which was completely cooled, while the low-noise amplifier is the first to integrate HEMT and HTSC elements. Both circuits demonstrate that it is now possible to integrate HTSC and semiconductive technologies.

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CHAPTER 1 INTRODUCTION

1.1 OVERVIEW

In the preceding two decades, progress in the performance and miniaturization of high speed electronics has been impressive. This progress was mainly accomplished through evolutionary developments in the field of semiconductor processing. In particular, the reduction in the feature size of monolithic integrated circuits resulted in improved performance at little additional cost. However, today, the increasing complexity and expense of the processing technology required for future advances are expected to retard this progress.^[1] In addition, even if the current miniaturization techniques prove to be economically viable for the next generation of high speed circuits, it is predicted that fundamental physics will limit the performance of these ultra-miniature devices when operated at room temperature.^[2,3] Therefore, to continue improving the performance of high speed circuits while controlling costs, as demanded by high performance system designers, the circuit designer will have to harness other technologies to obtain the additional degrees of freedom required.

One degree of freedom seldom considered by electrical engineers is operating temperature. Specifically, low temperatures, long utilized by solid-state physicists, appear to offer several advantages for high speed electronic systems. In addition to improving the operation of conventional semiconductive circuitry, low temperatures also allow superconductors to become available to the designer. In the past, the expense, bulk and poor reliability of low temperature refrigeration systems limited the widespread use of cryoelectronics. Today however, this argument is no longer valid due to the maturity of refrigeration technology. In the remaining portion of this overview, the operation of electronic circuits at cryogenic temperatures will be briefly explored and the maturity of cryogenic refrigeration technology will be

discussed. Lastly, the exploitation of this regime to produce high speed circuits possessing performance presently unattainable will be proposed as the thrust of this thesis.

At cryogenic temperatures, below 120K, conventional semiconductive circuitry exhibits many advantages. They include higher Qs due to reduced metal resistivity and substrate loss, higher operating speed due to enhanced carrier mobility, higher power densities and insensitivity to external temperature changes due to active environmental control, improved reliability due to a reduction in the rate of thermally activated failure mechanisms and lower thermal noise.

Both digital and analog semiconductive electronics benefit from lower temperatures. In digital computers, the requirement to minimize interconnection delays has led to compact high performance machines, but the high power densities associated with these designs has resulted in poor reliability. To improve reliability, early air-conditioned computers have been superseded by sophisticated liquid cooled units such as the fluorinert cooled CRAY and the liquid nitrogen cooled ETA.^[4] Additionally, to reduce "on-chip" power density and electric fields which limit reliability, power supply voltage has been gradually reduced from 12V to 3.3V in production devices and 1V circuits are under development. In the latter case, a 77K ambient temperature is required to provide an adequate noise margin.^[5] As well as the enhanced reliability offered at 77K, speed improvements are also commonplace. For CMOS technology, a doubling in speed has been demonstrated.^[6] For high speed analog electronics, the application of cryogenic temperatures has been mainly limited to low-noise microwave receivers where the thermal noise component has been minimized. An example is radioastronomy where low-noise amplifiers using high electron mobility transistors operating at or below 77K are presently competing with MASERs and parametric amplifiers to obtain noise temperatures comparable with the galactic background.^[7]

The other significant advantage of cryogenic temperatures is that they allow the circuit designer access to devices from the field of superconductivity. Previously limited to operating in liquid helium, at 4K, superconductors have recently undergone a revolution due to the discovery of copper-oxide based ceramics which remain superconducting above the temperature of liquid nitrogen. To be precise, the highest temperature at which superconductors operate, the critical temperature, has risen from 23K to 125K.^[8] Thus, superconductive electronic circuits capable of functioning at liquid nitrogen temperatures should be available for use in high performance systems.

Materials that remain superconductive at elevated temperatures are referred to as High Temperature SuperConductors (HTSCs) and a demonstration of one unique property of superconductors, the Meissner effect, is shown in Figure 1.1 Here, an yttrium-barium-copper-oxide disk, cooled in liquid nitrogen, levitates a permanent magnet cube. Since liquid nitrogen is a more effective and lower cost coolant than helium, superconductive technology with its low losses and other unique properties is now the focus of intensive investigation. Considerable effort is also being expended on developing new compounds with higher critical temperatures which would reduce or remove the cooling requirement.

The outlook for using HTSCs to achieve significant performance advances in both high speed digital and microwave electronics appears promising. Work is presently underway to achieve the same performance at 77K with HTSCs as was previously achieved at 4K with Low Temperature SuperConductors (LTSCs). Note that LTSC circuits developed over a decade ago exhibit performance levels that have yet to be attained with semiconductive technology. For example, the fastest digital switch is a LTSC Josephson junction, while microwave oscillators utilizing LTSC resonant cavities have short term stabilities superior to atomic clocks.^[9] Only the expense and bulk of the 4K cooling equipment has limited the use of LTSCs. However, the higher critical

temperatures of the new materials will free cryoelectronics from the liquid helium limitation, allowing their widespread use.

Figure 1.1 Meissner Effect Demonstration

One problem with both LTSC and HTSC technology, the lack of a three-terminal device exhibiting gain,^[10] may now be solved due to the higher operating temperatures of HTSCs. Although the Josephson junction has been used as the active element in LTSC electronics, it is a two-terminal device which limits its usefulness compared with a three-terminal device. Furthermore, no HTSC Josephson tunnel junction has been developed to date, and it is predicted that considerable time and effort

will be required to overcome the serious materials problems which prevent their fabrication. Fortunately, compared with room temperature operation, semiconductors exhibit superior properties in the temperature regime believed appropriate for HTSC operation. In particular, MOSFET and MESFET device performance peaks at temperatures from 30K to 50K and they should operate well at 77K, which is the design temperature for HTSC operation.^[11] Therefore, the possibility of utilizing semiconductive devices for the required three-terminal gain function exists. Hence, for the first time^a, semiconductive and superconductive technologies may operate in conjunction to produce high performance electronic systems.

For the circuit designer concerned with the feasibility of operating electronics at cryogenic temperatures, it should be noted that cryogenic refrigeration technology is a mature area. Furthermore, decreased operating temperatures may be regarded as an evolutionary development in operational environment control. However, fundamental thermodynamics makes 77K operation more efficient, and therefore, more feasible than 4K operation. Therefore, the author believes the prospect for widespread use of cryogenic systems will be limited to temperatures at 77K or above and the work discussed here is concentrated at 77K.

Systems capable of maintaining a substantial thermal load at 77K are presently available. For short duration, inexpensive open loop cooling is provided by mounting circuits on cold fingers immersed in liquified gases such as nitrogen (77K boiling point), hydrogen (20K boiling point) and helium (4K boiling point). In addition, for long duration, reliable closed cycle refrigerators requiring only electric power for their compressors are now both affordable and efficient.^[12] The mass production of closed cycle systems and the use of newer topologies such as pulse tube

^aAlthough semiconductor devices may operate at 4K, they require substantial doping modifications to prevent carrier freezeout which degrades their performance.

technology are expected to substantially reduce the cost, allowing their widespread use.^[13,14] The possibility of sharing a common refrigeration system among several analog and digital systems may further reduce the cost of attaining cold temperatures. For example, fire-and-forget munitions presently under development will integrate infra-red and millimeter wave sensors as well as powerful digital signal processors in close proximity, lending themselves to the shared cooling approach.^[15,16] As an alternative to active cooling, man also possesses the capability to transport his machines into an inherently cool environment, namely space. In deep space, only passive radiators are required to achieve cryogenic temperatures.^[17] Hence, the application of circuits requiring cryogenic temperatures to the rapidly growing area of space electronics looks promising.

Reflecting on the considerable potential of operating electronics at cryogenic temperatures and the maturity of low temperature refrigeration technology, it was decided to investigate the suitability of the cryogenic environment for high speed electronic circuits. Although both digital and microwave circuits are worthy of investigation, this work concentrates on microwave circuitry which has seen little low temperature activity. In particular, the microwave properties of semiconductive active devices and HTSC passive structures are investigated at cryogenic temperatures. For practical considerations, hybrid semiconductive/superconductive microwave integrated circuits possessing significant performance advantages at 77K are the objective. Areas expected to benefit from this work include passive circuits such as high Q resonators for filters and multiplexers, low-loss high speed interconnection networks and antennas as well as active circuits such as ultra-stable oscillators and narrow band low-noise amplifiers.

Although discrete microwave integrated circuit technology is used for the circuits fabricated herein, monolithic technology using patterned HTSC layers for passive structures and device interconnections on a common semiconductive substrate with its three-terminal active devices may be possible.

1.2 ORGANIZATION

The thesis organization is outlined in the block diagram of Figure 1.2. As shown, it is initially divided into two sections concerned with semiconductive microwave circuits and superconductive microwave circuits operated at cryogenic temperatures. In each section, a theoretical chapter summarizing the performance expected by operating at cryogenic temperatures is followed by an experimental chapter discussing measurement techniques, results and analysis. Results from these sections are combined to allow hybrid semiconductive/superconductive microwave circuits which possess high levels of performance to be constructed. The final chapter contains a summary and discusses future work.

Figure 1.2 Thesis Structure

Chapter 2 discusses the reasons for operating Microwave Integrated Circuit (MIC) and Monolithic Microwave Integrated Circuit (MMIC) technology at cryogenic temperatures. The chapter begins with a general introduction to these two planar fabrication techniques which are used in the majority of semiconductor-based microwave systems. This is followed by a summary of the present advantages and disadvantages of both techniques at room temperature. Finally, areas that are expected to benefit from 77K operation are discussed.

Experimental work on characterizing semiconductive microwave circuits at 77K is described in Chapter 3. A novel method to accurately determine the vector characteristics of microwave devices at 77K is discussed first. Results of applying this method to measure both active and passive constituent elements of MICs and MMICs are summarized. An improved method with enhanced accuracy is also discussed and the results of measuring three generations of three-terminal semiconductive devices are described. Small-signal models are closely fitted to the results, allowing the internal behaviour of these devices to be observed with temperature.

Superconductive microwave circuits are considered in Chapter 4. A discussion of the unique properties exhibited by superconductors is followed by reviews of LTSC and HTSC technology. In each review, the history, theory, processing and microwave circuits constructed with superconductor technology are discussed. Lastly, microwave circuits that have the most to gain from substituting HTSCs for normal metals are described.

Experiments to determine the feasibility of replacing normal metals with HTSCs in passive MICs are described in Chapter 5. The apparatus and technique capable of determining the quality factor of passive superconductive circuits at temperatures as low as 15K are discussed. HTSC thin-film processing techniques used by various suppliers and the fabrication techniques employed at the Communications Research

Centre (CRC) are briefly described. Results of characterizing many HTSC thin-film MICs are summarized.

Chapter 6 describes the development of hybrid semiconductive/superconductive microwave integrated circuits operating in the Ku-band. Both a completely cooled HTSC resonator stabilized MMIC feedback oscillator and a superconductively matched low-noise HEMT amplifier are reported for the first time.

Finally, Chapter 7 summarizes the earlier chapters, lists the contributions of this work to the two fields of superconductor and semiconductor technology and discusses the possible areas of future work. Some of the most promising applications for this technology are proposed.

CHAPTER 2 SEMICONDUCTIVE MICROWAVE CIRCUITS: BACKGROUND

2.1 INTRODUCTION

Microwave electronics is one of the most performance driven fields of electronics engineering. With the military and space industries constituting a significant portion of the market, cost considerations are normally overshadowed by performance requirements. However, today, the area responsible for the majority of previous advances, semiconductor processing technology, is reaching barriers that are expected to require considerable effort to overcome and the question of whether alternative technologies could produce comparable gains at a competitive price is being asked. In this chapter, I hope to partially respond to this question by examining the performance gains expected by cryogenic cooling of conventional semiconductive microwave circuits.

In addition to allowing conventional circuits to perform better, cryogenic temperatures also allow devices requiring a cryogenic environment to become available to the circuit designer. Also, as the size of conventional devices is reduced in the future, thermal noise and quantum phenomena such as tunneling through thin insulators are predicted to limit their operation at room temperature and a cooler environment is believed crucial for these circuits to attain their full potential.^[2]

Even though little work has been attempted by microwave engineers at cryogenic temperatures, it appears that performance improvements comparable to those expected from the next generation of semiconductive devices may be possible by simply cooling present day devices. The performance improvements anticipated at cold temperatures include lower losses, higher frequency of operation, higher power density, improved reliability, lower thermal noise and more stable circuit characteristics over a

wide range of ambient temperatures. Note that lower losses should allow higher Q structures to be realized. Fundamental limitations should prevent similar Q improvements through future semiconductor processing advances. The possibility of combining the gains made with both semiconductor processing advances and low temperature operation also exists for the construction of high performance microwave systems where cost is of secondary importance.

In this chapter, the present room temperature semiconductive microwave circuit technology will be reviewed, improvements expected from cryogenic operation will be quantified and some areas that may yield the largest performance improvements at 77K will be identified. In particular, Microwave Integrated Circuit (MIC) and Monolithic Microwave Integrated Circuit (MMIC) fabrication technologies will be summarized. A discussion of the advantages and disadvantages of circuits fabricated using both technologies operated at room temperature will be followed by a summary of the present performance limitations imposed by semiconductor processing. How cryogenic temperatures may overcome some of the performance limitations common to both MICs and MMICs will also be discussed. Finally, specific performance areas will be chosen for further experimental investigation, as described in the next chapter.

2.2 MIC and MMIC TECHNOLOGY

An overview of both MIC and MMIC technology will be presented in this section. A general description of both technologies will be followed by an in-depth look at their advantages and disadvantages as well as future trends for fabricating high performance microwave systems. These two fabrication technologies are presently used in the majority of microwave systems today and it appears that they will continue to play a major role in the future. In addition, both technologies are accessible in-house at CRC and through the DND funded MMIC foundry access program overseen at CRC.

2.2.1 Microwave Integrated Circuits (MICs)

A two-stage amplifier using MIC fabrication technology is shown in Figure 2.1.^[18] Here, discrete active and passive microwave devices are attached to the surface of a planar low-loss substrate. This example is typical of the most basic MICs, where a single metal layer is patterned to provide transmission lines that are used to construct distributed matching elements and to interconnect the discrete devices. Bond wires are used to connect the discrete devices into the circuit.

Figure 2.1. Two-Stage 28-28.5 GHz MIC Amplifier^[18]

A wide variety of relatively inexpensive MIC substrates are available to the designer. Metal layers, usually gold or copper, are deposited on the substrates using either thin-films etched by photolithographic techniques or thick-films directly screened and fired to produce transmission lines. The masks required are normally inexpensive, because line dimensions are quite large, and may be generated quickly. Both microstrip and coplanar waveguide transmission lines are commonly used.

Conductive epoxy or solder may be used to attach the devices onto the substrate. A wide variety of discrete devices, both active and passive, are available from commercial suppliers. Among the passive devices, resistors, capacitors, ultraminiature chokes, ferrites and dielectric puck and YIG sphere resonators are available. The active devices include a selection of diodes and transistors such as silicon BJTs for low-noise/low-cost applications below 10 GHz and GaAs MESFETs, HEMTs and Heterojunction Bipolar Transistors (HBTs) for small signal, low-noise and power applications at frequencies above 4 GHz.

Normally, the active devices constitute the largest share of the material cost of an MIC. Although unpackaged devices are cheaper and provide higher performance, their assembly requires expensive equipment and skilled operators. The cost of the required processing equipment is near \$1M. A typical MIC requires less than a week to pattern the substrate, attach the discrete components and interconnect them with bond wires. Substrates usually measure a few centimetres square and are from 0.005" to 0.025" thick. The substrates are normally attached to a metal carrier which provides heat sinking and a mechanical support for the circuit inside its housing. Since the circuit elements are well separated and the technology is relatively mature, accurate modelling software is widely available and high first design iteration success rates are possible. Bond wires are a major reliability limitation; they are hard to inspect following fabrication and are mechanically fragile.

One of the main advantages of MIC technology is the wide selection of devices available. Of prime importance are devices which are not available in other technologies, such as close tolerance (0.1%) laser-trimmed resistors, bias line chokes, stacked capacitors which use the vertical dimension to attain large capacitance in a small footprint, pin diodes for switching and attenuation functions, Gunn diodes for oscillators, hyperabrupt varactor diodes for linearly tuned VCO's and various three-terminal active devices including internally matched power FETs, both normal and pseudomorphic

HEMTs and HBTs. However, a major problem with discrete active devices is the wide variation in their electrical characteristics within a lot and from lot to lot. For small systems, testing of the individual devices to allow closely matched devices to be chosen is another approach, but such testing substantially inflates the final cost.

Variation in the placement and length of bond wires used to connect the discretes creates changing parasitic effects which become a significant problem in the manufacture of repeatable circuits at frequencies above 10 GHz. Fortunately, the large size of an MIC allows tuning elements to be bonded into the circuit to achieve optimum performance. Again, this step is manually intensive, which raises the assembly cost.

The distributed matching used in most MICs results in Q s of 100 to 200 at 10 GHz. These are useful in high Q circuits and the addition of dielectric puck and YIG sphere resonators allows the fabrication of extremely stable oscillators and narrow-band frequency selective filters with loaded Q s of over 1000. On the other hand, the large distributed matching networks limit broad bandwidth designs.

Another advantage of MIC technology is the wide selection of substrates available to the designer. Room temperature properties of some of the available substrates and the carriers to which they are attached are listed in Table 2.1. The low-loss substrates such as sapphire and quartz allow the highest Q planar circuits to be fabricated, while substrates such as BeO, with a thermal conductivity approaching that of metals, allow high power densities to be realized. Also, circuits patterned on ferrites exhibit non-reciprocal characteristics. Although silicon may be used for motherboards in high density multi-chip modules, normally when semiconductor substrates are used, active and passive devices are processed into their surface, forming MMICs. This approach will be discussed later.

Material	Relative Permittivity ϵ_r	Dielectric Loss Factor (at 10 GHz)	Specific Thermal Conductivity $K_{Th}(W/cm-K)$	Thermal Coefficient of Expansion $\Delta l/l(ppm/K)$
Alumina (Al_2O_3 99.5% pure)	9.8	0.0001	0.37	6.3
Sapphire	9.4	0.0001	0.42	6.0
Quartz glass	3.8	0.0001	0.017	0.55
Beryllium oxide (BeO 98% pure)	6.3	0.006	2.1	6.1
Titanium oxide (TiO_2)	85	0.004	0.05	7.5
Barium Tetratitanate ($BaTi_4O_9$)	37	0.0005 (6 GHz)	0.02	9.4
Gallium Arsenide (semi-insulating $\rho = 10^7-10^9 \Omega-cm$)	12.9	0.002	0.46	5.7
Silicon (highly resistive $\rho=10^3 \Omega-cm$)	11.9	0.015	1.45	4.2
Ferrite	9-16	0.001	0.03	11
PTFE (glass reinforced)	2.55	0.001	0.003	106
Aluminum	----	----	2.2	24
Copper	----	----	3.9	17
Kovar	----	----	0.17	5.3
Thermkon 70M	----	----	1.8	6.5

Table 2.1. Properties of Technologically Important Substrates and Carriers.^[19,20,21]

To lower assembly cost and improve reliability, lumped element MICs, referred to as Miniature Hybrid MICs (MHMICs) have been developed. Here, passive devices such as resistors, capacitors, inductors and transformers are fabricated on a common MIC substrate using thin-film processing. Only active devices such as transistors, diodes and MMICs need to be wire bonded into the circuit. Since the overall circuit is smaller, this technology allows wider bandwidth MICs to be fabricated. However, the lumped elements used for matching are lossier than distributed elements and MHMICs require more complex and expensive processing. Approximately five precision masks are used, resulting in a longer turn-around time of around one month. In addition, the modelling software for these more compact circuits is not yet refined. These considerations should limit its replacement of conventional MIC circuitry.

However, it is well suited to forming the motherboards used in the integration of MMICs in a miniature package where the reduced cost and lower loss of MIC substrates, compared with semiconductors, allows large high performance passive circuits to be made more economically. Such circuits include power combiner/divider networks for balanced circuits, high Q resonant structures for filtering and bias decoupling and stabilization networks for amplifiers and oscillators

2.2.2 Monolithic Microwave Integrated Circuits (MMICs)

MMIC technology is essentially an extension of discrete transistor technology wherein the additional passive circuit elements required for a complete microwave circuit are fabricated on a common low-loss semiconductor substrate. Initially developed at Texas Instruments in 1964 using silicon substrates, this technology was transferred to GaAs substrates in 1974 at Plessey, thereby extending the frequency of operation.^[22] Due to its higher bandgap, GaAs possesses resistivities approximately two thousand times higher than silicon and this, combined with its higher low-field mobility, has led to its domination of the MMIC market for frequencies above 4 GHz. Higher mobility super lattice substrates such as AlGaAs/GaAs/AlInAs have been used to develop MMICs with higher frequency, lower noise and higher output power capabilities.^[23,24]

A typical GaAs MMIC is shown in Figure 2.2. The circuit elements and their interconnections are formed atop a planar high resistivity semiconducting substrate. The passive elements may include resistors (metal film and bulk semiconductor), capacitors (interdigitated and overlay), inductors, transformers and transmission lines which are used for element interconnection and distributed matching at higher frequencies. Interconnections are normally microstrip or coplanar waveguide transmission lines formed from several thin-film metal layers. The active elements include diodes and transistors.

Figure 2.2. A Typical MMIC Circuit^[25]

To construct an MMIC, complex processing is required. Photolithography and liftoff processing are used to pattern the many layers required for the circuit. Usually at least ten masks are required to define and interconnect the elements. In high performance processes, the gate of the MESFET is defined using direct-write electron beam lithography to achieve sub-micron gate lengths. A typical MMIC circuit will be a few millimeters square, allowing it to be repeated many times on the 2", 3" and 4" diameter wafers used for MMIC fabrication. For example, a one square millimeter circuit may be repeated approximately 4,000 times on a 3" wafer. Once the circuits are defined on the wafer, it is diced to free the individual circuits, referred to as die, for mounting into packages.

Due to the high costs of establishing a MMIC processing facility, many existing facilities are offering their services to external users for a fee. These facilities, costing upwards of \$10M, are referred to as foundries and the typical

fabrication cost to produce a few completed wafers, using the same mask set, is around \$50K. In large quantities, the cost of a completed 3" wafer will be below \$10K leading to a minimum fabrication cost of a few dollars for a one square millimeter circuit. The lower fabrication costs of commercial foundries has led to their wide use. However, drawbacks of using a foundry compared with using an in-house facility include a lengthy four to six month turn-around time and restricted access to higher performance processing techniques.

The small size of a MMIC, typically a few millimeters square, allows their use in some unique applications. For example, the millimeter wave focal plane array for antenna feeds is one system where the small size of the MMICs allows the required small inter-radiator spacing to be achieved. In addition, their small size and light weight should allow more functions to be incorporated in the same package previously used for MICs, allowing a greater degree of redundancy to be achieved at the subsystem level, increasing reliability. Regrettably, the small spacing between circuit elements in a MMIC makes circuit parasitics significant and they must be considered in any design. To accomplish this, powerful CAD tools are used. However, even with the latest commercial CAD tools, a first iteration success is unlikely and further iterations are normally required due to modelling inadequacy and the deviations in processing characteristics from lot to lot. Although CAD software is being improved, new designs are becoming more compact to lower chip cost, compounding this problem.

Since the elements are interconnected by patterning thin-film metal layers, bond wires are only required for off-chip connections which include RF input/output, bias and grounding. As most MMICs are internally matched to 50Ω , the effect of these bond wires on microwave performance is usually negligible. This reduction in the number of bond wires and their use in non-critical connections enhances the reliability and repeatability of MMICs and allows their use at higher frequencies. The main failure mechanism is no longer bond wires but rather the interdiffusion of Schottky barrier and ohmic contacts into the substrates.^[26]

A unique advantage for the MMIC designer is the freedom to customize the circuit elements in order to attain the required performance. In addition to forming a wide range of resistor, capacitor, inductor and transformer values and diodes or FETs with various gate lengths or widths, novel active and passive structures are also possible. For example, the segmented dual-gate FET shown in Figure 2.3 is a dual-gate FET in which the second gate has been divided into four sections whose widths are binary weighted. By varying the DC bias on the second gate segments to control the drain current, various gain responses may be achieved.^[27] Note that no analog to this element is available using discrete devices at microwave frequencies. The close proximity of MMIC elements also allows the designer to obtain devices with closely matched characteristics within a circuit and over a small section of a wafer. Thus, circuit topologies requiring closely matched devices such as current mirrors and balanced amplifiers may be realized. Additionally, the gain and phase variations of devices located nearby on the same wafer will track closely with temperature, easing the compensation required in large systems such as active array antennas.

Figure 2.3. A Segmented Dual-Gate FET.

The common substrate and doping profile that all MMIC devices share create several disadvantages such as a reduction in the selection of active devices and a compromise in their inherent performance. Due to the tradeoffs made in standardizing on a common profile, devices such as PIN diodes which require a p^+ implant and hyperabrupt varactors which require a non-uniform doping profile are not presently available in MMIC technology. In addition, since small-signal gain, low noise figure and high power devices each require different doping profiles for optimum performance, only one of these device types may be optimized on each wafer. Although the possibility of utilizing different implants to achieve more than a single type of active device on the same wafer exists^[22], the added complexity required has prevented its use by most commercial foundries. GaAs substrates also limit power handling due to its poor thermal conductivity, which is one-third that of silicon at room temperature. Although 2" wafers may be thinned to 35 μm and 3" wafers to 90 μm and via holes added to help remove the heat, these back-side fabrication steps substantially increase the cost of processing a wafer due to its mechanical fragility.^[28] Furthermore, the thinned substrates have larger leakage currents due to their reduced ground plane isolation, which increases transmission line loss and reduces gain. Even for a substrate thickness of 250 μm , the resistive transmission lines and substrate leakage results in Q_s of only 50 at 18 GHz for most lumped elements.^[29] Element Q_s may be improved by using distributed matching structures, however, large size limits their use to millimeter wave frequencies and above and the losses are still worse than for similar MIC structures due to the higher dielectric loss tangent. Thus, the stability of oscillators and noise figure of amplifiers using MMIC technology has not been able to match that of MICs. Additionally, MMICs are a planar technology, which increases the parasitic capacitance of most circuit elements compared with discrete devices. Therefore devices such as varactor diodes suffer from low capacitance variations and low upper frequency limits.

Their small size gives MMICs a large bandwidth capability. With amplifier bandwidths in excess of 40 GHz now demonstrated, MMICs are finding many applications in the electronic warfare and radar fields.^[30] However, the small size also makes them difficult to tune after fabrication. Although ultrasonic and laser cutters may be used to remove transmission lines on finished chips, the equipment is expensive and its use negates the low testing and assembly cost characteristic of MMICs.^[31] To help alleviate this problem at microwave frequencies, the design philosophy has changed and yield rather than performance is being optimized.^[32] By designing circuits that are relatively insensitive to processing variations, higher first iteration success rates are achieved and the cost is reduced.

2.2.3 Summary

In many applications, it is often unclear whether MIC or MMIC technology is appropriate. For small numbers of low complexity circuits, where low noise figure, narrow bandwidth or high power as well as short turn-around time are required, MICs should be used. If large quantities of small, light weight, complex and wideband circuits are required, MMIC technology should be chosen. For other requirements, the choice is less clear and in any particular subassembly, both technologies may find a use. In the highest performance systems, a combination of both technologies has been found to be optimum. One example is transmit/receive modules for active array antennas in which the low noise and high power sections use MICs while the switching, gain and phase control and intermediate power amplification sections use MMICs.^[33]

Recapping, both MIC and MMIC technology have been briefly introduced. In the next section, some limitations common to both will be described and it will be seen that cryogenic operation may overcome some of these limitations.

2.3 PERFORMANCE IMPROVEMENTS OFFERED BY CRYOGENIC OPERATION

Performance limitations common to both MIC and MMIC technology that are expected to be extended through cryogenic operation will be discussed in this section. It will be seen that the Q , maximum frequency of operation, power density, reliability, noise figure and temperature stability will be enhanced at cryogenic temperatures. To begin, the major factors limiting circuit performance at room temperature including the losses of the transmission lines and lumped elements as well as the inherent performance of the active devices will be described. How the performance of these circuit elements will be improved at 77K will be discussed and the gains expected in specific areas will be quantified.

2.3.1 Quality Factor (Q)

Both MIC and MMIC technology use planar transmission line structures. The most common are microstrip and coplanar waveguide (CPW) as shown in Figure 2.4 a) and b), respectively.

Figure 2.4. Common Planar Transmission Lines^[19]

Of the two, microstrip is the most common due to its realizability, compact size, low ground plane loss and low radiation loss. CPW is mainly used at and above millimeter-wave frequencies where the top side ground planes provide low inductance grounding. Low inductance via hole grounds can be achieved in microstrip but they are difficult to fabricate and may possess significant inductance.

In microstrip, the characteristic impedance, Z_0 , of the transmission lines depends on the aspect ratio, w/h , as identified in Figure 2.4a). Distortions of the electromagnetic fields at the abrupt dielectric discontinuity of the air/substrate interface result in a hybrid propagation mode referred to as quasi-TEM. Full-field analysis of such non-TEM structures is complex and empirically derived expressions are often used for design purposes. For example, the characteristic impedance may be described by equation 2.1 for $w/h > 1$ and $t \ll h$.^[34] Note that since the electromagnetic fields are not fully confined to the substrate, they fringe into the air, lowering the effective permittivity, ϵ_{eff} , below the dielectric constant of the substrate. Overall, the wider the line, the lower its impedance and propagation speed. For realizable impedance values, ϵ_{eff} is roughly seven and eight on alumina and GaAs, respectively. A standard 50Ω line on either substrate requires w/h close to unity.

$$Z_0 = \left(\frac{120\pi}{\sqrt{\epsilon_{\text{eff}}}} \right) \left(\frac{w}{h} + 1.393 + 0.667 \left(\frac{w}{h} + 1.444 \right) \right)^{-1} \quad (2.1)$$

$$\epsilon_{\text{eff}} = \left(\frac{\epsilon_r + 1}{2} \right) + \left(\frac{\epsilon_r - 1}{2} \right) \left(1 + \frac{10h}{w} \right)^{-0.56}$$

C. $\mathcal{N}$ is another quasi-TEM structure. For an infinitely thick substrate, its characteristic impedance and effective permittivity are described by equation 2.2, where K is the elliptic integral of the first kind.^[35] In this case, the characteristic impedance decreases as the aspect ratio, w/d in Figure 2.4b, increases. For finite

substrate thickness, there is a similar dependence on the aspect ratio, and for typical MMIC geometries, a 50Ω impedance value requires an aspect ratio of approximately 0.5.

$$Z_o = \left(\frac{30\pi}{\sqrt{\epsilon_{\text{eff}}}} \right) \frac{K\left(\sqrt{1 - \left(\frac{w}{d}\right)^2}\right)}{K\left(\frac{w}{d}\right)}, \quad \epsilon_{\text{eff}} = \left(\frac{\epsilon_r + 1}{2} \right) \quad (2.2)$$

The loss mechanisms in both transmission line structures are comprised of resistive conductor loss, substrate loss, which includes both dielectric loss in insulators as well as leakage current loss in semiconductors, and radiation loss. Overall, the Q is degraded by each contribution as shown in equation 2.3. Each mechanism will be described in the following, as well as the loss reduction expected by operating at cryogenic temperatures.

$$\frac{1}{Q_{\text{total}}} = \frac{1}{Q_{\text{conduction}}} + \frac{1}{Q_{\text{dielectric and leakage}}} + \frac{1}{Q_{\text{radiation}}} \quad (2.3)$$

At DC, the resistive heating of metal conductors carrying high current densities may lead to electromigration. To prevent this, in GaAs MMICs, current densities are usually kept under $10,000 \text{ A/cm}^2$. For a $1 \mu\text{m}$ thick layer, this leads to a design rule of $10 \text{ mA}/\mu\text{m}$ of conductor width which may create isolation problems for the bias circuits feeding the drains of large FETs. This problem may be alleviated by reducing the ambient temperature. For example, the DC resistivity of bulk gold versus temperature is shown in Figure 2.5. At 77K, the resistance is around one-sixth that of room temperature. Similarly, copper and aluminum show reductions of one-eighth and one-tenth, respectively. Note that the thermal resistance of the substrates on which the conductors are attached decreases when cooled, further lowering the temperature of the

conductors. Therefore, existing bias lines should be able to carry bias currents an order of magnitude larger when operated at 77K.

Figure 2.5. DC Resistivity of Bulk Gold Versus Temperature^[36]

One must also consider that the DC resistance reduction may be less if extremely thin films are used due to the "size effect". This means that if one of the conductors dimensions approaches the mean free path of the carriers, the resistivity will increase and the resistivity will drop more gradually during cooling than for bulk material.^[37] At low temperatures, this effect sets the temperature at which little significant resistivity reduction will occur. As can be seen in Figure 2.6, copper films under 1 μm thick exhibit little resistance reduction at temperatures below 77K. However, this thickness is typical of MIC and MMIC conductors so a reduction in the DC resistance of around an order of magnitude at 77K still appears feasible.

Figure 2.6. Electrical Resistivity of Copper Thin-Films Versus Temperature^[37]

The resistive loss mechanism is a more severe problem at higher frequencies due to the limited penetration of electromagnetic fields inside a conductor. Since these fields penetrate a finite distance, referred to as the skin depth, δ , the material exhibits a frequency dependent surface resistance, R_{AC} , which is proportional to the square root of the frequency over the conductivity as shown in equation 2.4.^[37]

$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \sigma}} \quad ; \quad R_{AC} = \sqrt{\frac{\pi f \mu_0}{\sigma}} \quad (2.4)$$

Although accurate at and above room temperature, the classical skin depth mechanism does not predict the AC loss behaviour at lower temperatures. In particular, as the temperature is lowered and the mean free path, l , of the electrons increases to a value exceeding the skin depth, the surface resistance reaches the anomalous limit given

by equation 2.5 rather than following the classical rolloff.^[37] This is shown in Figure 2.7 where the limiting resistance occurs at lower temperatures for lower frequencies. For 77K operation, the AC resistivity for both gold and copper is reduced by a factor of approximately four. Since little resistivity reduction occurs below 77K for frequencies near 10 GHz, there is little advantage of operating passive microwave circuits constructed of normal metals at colder temperatures.

$$R_{\text{limit, anomalous}} = \left(\frac{\sqrt{3} \pi f^2 \mu_0^2 l}{4\sigma} \right)^{\frac{1}{3}} \quad (2.5)$$

Figure 2.7. AC Resistance Ratio of Bulk Copper Versus Temperature^[37]

In semiconductors, where a large number of free carriers exist, leakage currents through the semiconductor substrates to which the devices are attached is the main substrate loss mechanism. These currents are normally caused by thermally excited carriers overcoming the bandgap of the substrate. At equilibrium, the average energy that an electron may possess is Boltzmann's constant multiplied by the absolute temperature. For example, at 300K, 77K and 4K, the electron energies are 0.026 eV,

0.0067 eV and 0.00036 eV, respectively. Since the probability of an electron being excited from the valence to conduction band follows the Fermi-Dirac distribution, an exponential drop in leakage with temperature is expected for pure materials.^[38] In addition, the effect of any impurities freezing out at low temperature may also provide large increases in resistivity. For example, since some of the lowest dopant activation energies for GaAs and silicon are silicon (0.0058 eV) and phosphorus (0.045 eV), respectively, many unwanted impurities are frozen out at temperatures below 77K, reducing the density of free carriers and further lowering the substrate loss.^[38] This has allowed silicon to be used as a low-loss microwave substrate for LTSCs operated at 4K. The dramatic increase in the resistivity of GaAs with temperature is shown in Figure 2.8. By extrapolating to 77K, the resistance is expected to increase approximately eight orders of magnitude from its room temperature value, making it a second order effect.

Figure 2.8. Electrical Resistivity of Bulk GaAs Versus Temperature.^[36]

For substrates with bound charges such as insulators, the substrate loss is predominantly dielectric loss. Here, the loss is created by the electron cloud encircling the bound charges oscillating and transferring energy to the lattice in the form of heat. In this case, the substrate loss is expressed by the loss tangent, which is defined to be the ratio of the imaginary to real component of the dielectric constant.^[39] This loss has also been found to decrease at lower temperatures. For example, the loss tangent of sapphire versus temperature is shown in Figure 2.9. By extrapolating to 77K, the loss tangent is expected to drop approximately two orders of magnitude from its room temperature value. This has recently been confirmed in dielectric resonators, where similar Q improvements at 77K have been observed.^[40]

Figure 2.9. Loss Tangent of Sapphire Versus Temperature.^[36]

Radiation loss is the last loss mechanism that will be discussed. Since resistive losses are proportional to the square root of frequency while radiation losses are proportional to the cube of frequency,^[11] at higher frequencies radiation loss

dominates. For MMICs, the transition frequency where radiation losses dominate is around 40 GHz. As this loss should be unaffected by temperature, radiation losses should dominate at lower frequencies when the circuits are cooled, and other transmission line topologies or special packaging may be required to reduce this effect. One promising topology is stripline as shown in Figure 2.10. Here, the radiation is reduced due to the two ground planes confining the electromagnetic fields. Another advantage of stripline is the uniform dielectric, where $\epsilon_{\text{eff}} = \epsilon_r$; this supports TEM propagation and prevents geometric dispersion, allowing higher speeds to be achieved. However, this topology is difficult to manufacture and tune, since the circuit elements are placed in the middle of the dielectric sandwich.

Figure 2.10. Stripline Transmission Line Structure.^[19]

The effect of these losses on the Q of present MIC and MMIC circuits will now be discussed. Additionally, the performance enhancement expected at 77K will be described. Finally, applications of these higher Q circuits will be detailed.

As discussed earlier, the three loss mechanisms are conductor resistance, substrate loss and radiation. To minimize these effects in room temperature circuits, the interconnect lines may be plated up from an initial sputtered or evaporated height of under a micrometer to approximately 5 μm . For MESFET gates where submicron lengths are used, the aspect ratio limits their maximum height and normally 'T' and mushroom cross-sections are used to lower the resistance.^[41] Another approach is to widen the

transmission lines within realizable limits. A problem with widening lines is the higher substrate leakage, which is significant when using thinned semiconductor substrates in order to dissipate heat or to form low inductance ground connections. Radiation loss may be reduced through the removal of transmission line discontinuities, reduction of substrate height, use of electromagnetically shielded enclosures and minimization of the overall circuit area.

As previously noted, the AC resistance at 77K of 1 μm metal thin-films at 10 GHz should be one-quarter of its room temperature value, the substrate resistance for GaAs should be eight orders of magnitude higher, while the dielectric loss of sapphire should be two orders of magnitude lower, leading to the possibility of higher Q circuits at 77K. In addition, since the DC resistance at 77K is approximately one-tenth the room temperature value, a corresponding reduction in the width of the DC bias lines should lead to smaller bias networks with reduced RF effects. For cases where matching and biasing are combined, such as the FET drain choke for MMICs, this size reduction should allow higher power or frequency of operation to be achieved.

As discussed in the next section, a reduction in the drain-to-source resistance of FETs also occurs at 77K. Typical values for MOSFETs reveal an 'ON' DC resistance of one-quarter the room temperature value at 77K.^[42] Therefore, when used in a passive configuration such as a switch, FETs should exhibit lower insertion loss, increasing the Q of the circuit in which they are embedded.

2.3.2 Maximum Frequency of Operation

The maximum frequency of operation of both MICs and MMICs is mainly determined by the active device employed. In addition to the majority carrier field effect devices such as the MESFET and HEMT, minority carrier devices such as the BJT and HBT are also available. The operation of these devices and the advantages of using them at cryogenic temperatures will now be discussed.

The most widely used active device at microwave frequencies is the GaAs MESFET. Figure 2.11 shows its basic structure, in which source and drain pads bound a channel whose current is controlled by the gate. With the drain biased positive with respect to the source, electrons travel from source to drain. The channel region below the gate becomes partially depleted of electrons when the Schottky barrier gate is deposited, forming a space charge region which restricts the channel current, I_{CH} , to the value I_{dss} . As the gate-to-source potential, V_{GS} , becomes negative, the depletion layer expands, restricting the drain-to-source current, I_{CH} , further. At $V_{GS} = V_p$, $d = W$ and $I_{CH} = 0$, the channel is "pinched off". For sub-micron gate length devices, this is typically a volt or two. Therefore, by varying V_{GS} , I_{CH} may be modulated, producing gain if the modulated power is larger than the gate power.^[43]

The channel under the influence of the gate may be divided into three regions: Region I, where the electric field is less than the saturated value, Region II, where the electric field is greater than the saturated value and Region III, which is the space charge extension of length X into the drain region. Region I behaves like a resistor whose extent is controlled by V_{GS} .^b As the stored charge is modulated by V_{GS} , it also behaves as a capacitor. In Region II, the electrons are limited to their saturated velocity, v_{sat} . Thus, a constriction in d , controlled by V_{GS} , determines the channel current. Region III is the most complex region due to the ionic charge across which most of V_{GD} is applied. This charge creates non-transverse electric fields which affect the entire device.^[44]

The equivalent model, shown in Figure 2.12, has been found to accurately predict the small-signal performance of the MESFET at microwave frequencies. Approximate locations of some of the model elements are indicated in Figure 2.11. The

^b Although bulk GaAs exhibits negative resistance due to a peak in the carrier velocity-electric field characteristic, in a highly doped channel with large transverse electric fields at room temperature, carrier velocity monotonically increases with electric field until saturating.

Figure 2.11. MESFET Structure.^[44]

Figure 2.12. Small-Signal MESFET Model^[44]

most important elements are the gate-to-channel capacitance, C_{gc} , the drain-to-source capacitance, C_{ds} , the transconductance, $g_m = \partial I_{ds} / \partial V_{gs}$, and the gate-to-drain capacitance, C_{gd} , at higher frequencies. This model predicts the frequency response initially rolling off at $1/f$ due to the lower impedance seen across C_{gc} and hence, the Schottky barrier as the frequency increases. This is followed by a $1/f^2$ rolloff due to C_{ds} shunting the drain-to-source resistance with a lower impedance as the frequency increases.

Closed-form equations which allow an understanding of the small-signal operation of the MESFET structure of Figure 2.11 are shown in Table 2.2. S' and D' are virtual source and drain; they do not include any ohmic losses. Only bounds for X and R_{ds} are given since exact results require the numerical solution of the complex carrier velocity-electric field relationship and the two dimensional electric field components in Region III. Equations for the parasitic elements C_{pgd} , G_{pgd} , C_{pg} and C_{pd} are not included, as they are mainly geometric capacitances which are dependent on the plan view layout of the device. Similarly, G_{gs} and G_{pgd} are also not included as they are second order loss generators and are normally fitted through correlations with the intrinsic elements.^[44]

A common figure of merit for MESFETs is the cut-off frequency, f_T . This is the frequency where the magnitudes of the input and output current are equal and is given by equation 2.6, provided high frequency parasitics are neglected. To improve f_T , most effort has concentrated on decreasing gate length. Considering that L_G/W ratios in excess of three are required to fully pinch off the channel, the channel depth must also be decreased, which requires an increase in doping density to maintain current levels. Provided the doping density can be achieved, C_{gc} will decrease while the transconductance and f_T will increase, extending the useful frequency regime of the FET.^[32]

$$f_T = \frac{g_m}{2\pi C_{gc}} \quad (2.6)$$

ELEMENT	EQUATION
L_g	$\frac{\mu_0 d Z_G}{m^2 L_G}$; m = number of gate fingers
C_{gc}	$\frac{\epsilon Z_G L_G}{d} \left(1 + \frac{X}{2 L_G} - \frac{2d}{L_G + 2X} \right)$
C_{gd}	$\frac{2\epsilon Z_G}{1 + \frac{2X}{L_G}}$
C_{ds}	$C_{ds1} + C_{dpp}$
gm	$\frac{\epsilon v_{sat} Z_G}{d}$
τ	$\frac{1}{v_{sat}} \left(\frac{X}{2} - \frac{2d}{1 + \frac{2X}{L_G}} \right)$; $\tau < 0$ has no physical significance
d	$\left[\frac{2\epsilon(V_{S'G} + V_{B0})}{qN} \right]^{1/2}$; V_{B0} = Schottky Barrier Potential (~0.8V)
X	$\leq \left[\frac{2\epsilon}{qN(V_{S'G} + V_{B0})} \right]^{1/2} (V_{D'G} + V_{B0})$; $V_{D'G} = V_{D'S} + V_{S'G}$
I_{CH}	$qNv_{sat}(W-d)Z_G$
R_i	$\frac{v_{sat} L_G}{\mu_N I_{CH}}$
R_{ds}	$\geq \frac{4V_{D'S'}}{I_{CH}}$
R_g	$\frac{\rho Z_G}{3m^2 h L_G}$; m = number of gate fingers
R_d	$\frac{L_{GD} - X}{qN\mu_N W Z_G \left(1 + \frac{2v_{sat}(W-d)}{\mu_N W} \frac{\epsilon}{qNd} \right)}$
R_s	$\frac{L_{SG}}{qN\mu_N W Z_G}$

Table 2.2. Closed-Form MESFET Element Formulae^[44]

Today, 0.25 μm gate length MESFETs are available as both discrete devices and through MMIC foundries. Since the channel doping density is limited, the channel depth may not be reduced much below 0.1 μm and therefore, gate lengths below 0.25 μm appear unfeasible. Hence, the maximum frequency of operation of MESFETs is considered to be around 50 GHz.^[45]

To define a 0.25 μm gate length device requires expensive direct-write electron-beam lithography where a focussed electron-beam patterns the photoresist directly on the wafer. Using this method, gate lengths of 0.1 μm have been fabricated. Since the electron-beam sequentially scans the wafer, it is a slow process, lowering throughput and increasing cost. X-ray lithography, presently under development, should solve this problem since it has wide area coverage similar to optical lithography except with a higher energy/lower wavelength source. However, it is expected to require a decade to develop X-ray opaque masks and more economical exposure sources.^[46]

A relatively new device is the HEMT. Simultaneously invented in 1980 at both Thomson and Fujitsu,^[7] the HEMT is physically identical to a MESFET except for the active layer doping profile. In a HEMT, the active layer is modulation doped in the vertical dimension to create a "super lattice" which gives the HEMT its superior performance. Only recently has Molecular Beam Epitaxy (MBE) processing technology been able to create the abrupt changes in the vertical doping profile required to form HEMTs.^[47]

The vertical structure of a conventional HEMT is shown in Figure 2.13a). Notice that the active layer is a sandwich of a doped tertiary compound AlGaAs, a thin layer of pure (undoped) AlGaAs and a pure binary compound GaAs. At the AlGaAs/GaAs interface, a heterojunction forms. Due to the higher bandgap of AlGaAs, the electrons in this doped layer migrate through the thin space of pure AlGaAs into the pure GaAs forming a two-dimensional electron gas. In the undoped GaAs, these mobile carriers are

free of coulomb scattering effects. That is, they are unhindered in their movement by collisions with donor ions which would decrease their average velocity. Hence, HEMTs have a higher electron mobility, resulting in superior microwave performance.^[48]

a) Conventional^[49]

b) Pseudomorphic^[50]

Figure 2.13. HEMT Cross Sections

In practice, HEMTs have higher transconductances and drain-to-source resistances which increase their gain compared with MESFETs. It is common for 0.5 μm gate length HEMTs to match 0.25 μm gate length MESFETs in performance. In addition, the super lattice sets the spacing between the gate and the conductive channel, allowing 0.1 μm gate length devices to function. Thus, HEMTs are expected to be useful for frequencies to 100 GHz.^[51]

A more recent development is the pseudomorphic HEMT^[50], in which the undoped GaAs layer is replaced with the lower bandgap material InGaAs as shown in Figure 2.13b). By making this substitution, the electron density and mobility in the

two-dimensional electron gas increases, further improving the transconductance. Both types of HEMT may be described by the same basic MESFET circuit model. However, additional parasitic elements may be required at millimeterwave frequencies.

The materials engineering equipment required to grow epitaxial layers only tens of atoms thick with the abrupt interfaces required for HEMTs is very expensive. In addition, the devices fabricated thus far have been on an R&D scale and therefore, the question of whether this process will be transferable to a production environment at a reasonable cost remains unanswered.

At cold temperatures, field effect device performance improves due to improved carrier mobility, higher active region conductivity and higher semi-insulating substrate resistance. The higher mobility reflects the faster carrier velocities from drain to source, which improves the frequency of operation by increasing the transconductance. The higher conductivity leads to lower drain and source resistances, increasing the frequency of operation and decreasing the noise. The higher resistance of the semi-insulating GaAs, due to the freeze out of unwanted carriers, should reduce some of the circuit parasitics such as the substrate leakage currents to ground which have appreciable effects at higher frequencies.

Since the lattice vibrations are reduced at lower temperatures, the carriers in both MESFETs and HEMTs encounter fewer collisions, enhancing their mobility as shown in Figure 2.14. In the MESFET, collisions with the ionized dopant impurities limit the improvement. However, since the two-dimensional electron gas flows in an undoped layer in the HEMT, substantial mobility improvements are achieved. It should be noted that for both devices, for sub-micron geometries, the carrier temperature is much higher than the lattice temperature, creating hot electrons. The velocities of hot electrons tend to saturate at values which are less temperature sensitive than shown and velocities only 50 to 100% higher are normally achieved in HEMTs at 77K.^[7]

Figure 2.14. Electron Mobility Versus Temperature for Modulation-Doped (GaAs/AlGaAs) and Uniformly-Doped GaAs.^[2]

The effect of lower temperatures on conductivity for doped silicon, GaAs and InSb is shown in Figure 2.15. Since conductivity is proportional to the product of carrier concentration and mobility, this quantity reflects the effect of dopant freeze out in addition to enhanced mobility. Overall, it is seen that conductivity peaks at temperatures from 30 to 100K for these materials. Note that at very cold temperatures, 4K, dopant freeze out is extensive and device performance degrades severely.^[52]

Figure 2.15. Semiconductor Conductivity Versus Temperature.^[52]

Thus far, only majority carrier devices have been considered. Although BJTs and HBTs may be operated successfully at 300K, they are minority carrier devices which should limit their use at low temperatures. For BJTs, this has been due to the rapid reduction in the minority carrier lifetimes at cold temperatures caused by the movement of the Fermi level towards the valence or conduction bands, depending on whether p-type or n-type material is used. This movement uncovers traps, increasing their capture cross section.^[37] This effect is clearly shown for InSb in Figure 2.16 where τ_n , the minority carrier lifetime, drops two orders of magnitude while τ_p , the majority carrier lifetime, increases by an order of magnitude at 77K. Since the diffusion length is proportional to the square root of the carrier lifetime, extremely thin bases would be required to prevent emitter-collector current from recombining with base current. Thus, for most BJT devices, current gain is less than one at 77K, negating their usefulness.^[7] Although little has been reported on HBTs at low temperatures, devices were not available and both minority carrier devices were not considered in this work.

Figure 2.16. Variation of InSb Carrier Lifetime With Temperature^[52]

2.3.3 Power Density

Another area that is expected to benefit is the power density of both MICs and MMICs due to the enhanced thermal conductivity of most pure materials at low temperatures. Again, the power density limit at room temperature will be identified and the expectations of 77K operation described.

The main device in which power density becomes a limiting factor is the power FET. Its structure is similar to the MESFET discussed earlier. Usually, power FETs have a gate periphery exceeding one millimeter to achieve large drain currents which may be modulated to provide large output power levels while their doping profile and contact spacing are optimized for high breakdown voltage. Careful thermal design is required to ensure that electromigration along the gate, source and drain contacts as well as interdiffusion of the Schottky and ohmic contacts into the substrate does not occur.

Normally, this entails careful layout of the devices where gate fingers are well separated and other power devices are positioned as far away as possible. In addition to thermal limits, avalanche breakdown of the gate-to-drain Schottky barrier limits maximum voltage that the structure can support. Also, the difficulty of matching to the large input gate capacitance and low output resistance limits the maximum size of a single power FET cell. These considerations have led to the output power of fabricated devices being proportional to the inverse of the frequency squared as shown in Figure 2.17. This relationship is a result of both the length of the gate fingers and the overall width of the cell being constrained due to the requirement to keep both of these dimensions under $\lambda/10$ to allow efficient matching.^[51]

Figure 2.17. MMIC Power Amplifier Output Power Versus Frequency.^[51]

The thermal conductivity versus temperature for some pure materials is plotted in Figure 2.18. Summarizing, the improvement at 77K compared to 300K for GaAs is ten times, alumina is four times and gold is eight times. Note that for impure and composite materials, the thermal conductivity degrades at lower temperatures (not shown). For example, both Kovar and silver epoxy are roughly half as thermally conductive at 77K. Therefore, provided pure materials are used and devices are solder attached, significantly improved heat transfer is possible at 77K.

Figure 2.18. Thermal Conductivity Versus Temperature for Various Materials.^[2]

The order of magnitude improvement in the thermal conductivity of GaAs at 77K should be beneficial for both MIC and MMIC power FETs. Electromigration and channel heating should no longer be a design consideration for conventionally laid out devices. In addition, decreasing the width of the source and drain fingers should allow power FETs to be compacted, extending the power-frequency envelope. In addition, the increase in gain of cooled MESFETs, although only a few dB, should significantly improve the power added efficiency of millimeterwave power amplifiers by reducing the number of power FET stages where gains of 4 to 5 dB/stage occur.

2.3.4 Reliability

Closely related to power density, reliability should also be substantially improved at low temperatures. In the following, failure mechanisms common to both MICs and MMICs as well as the longevity improvements anticipated from 77K operation will be discussed.

The primary failure mechanism for MICs has been the MESFET, which degrades over time if the ohmic and Schottky junctions are operated at elevated temperatures. The failure mechanism consists of the interdiffusion of the junction metals into the GaAs substrate. Studies on MMICs also show that the MESFET determines their reliability.^[26] The only difference between the two technologies is that the larger MMIC substrates have higher thermal conductivities which lower the temperature drop across the substrate. A secondary failure mechanism has been electromigration in the bias lines as previously discussed.

Since both interdiffusion and electromigration are electrochemical reactions, they have an exponential dependence on temperature. For elevated temperatures, the reliability has been shown to follow the Arrhenius expression of equation 2.7. Here, A is a constant, E_a is the activation energy, K is Boltzmann's constant ($8.61 \times 10^{-5} \text{ eV/K}$) and T is the absolute temperature. For GaAs interdiffusion,

a common value for E_a is 1.5 eV.^[26] A selection of lifetime curves for a range of activation energies, shown in Figure 2.19, demonstrates how a small drop in the channel temperature improves longevity.

$$\text{Failure Rate} = Ae^{-E_a/KT} \quad (2.7)$$

Figure 2.19. Lifetime Versus Channel Temperature for Various Activation Energies.^[26]

By applying equation 2.7, one obtains a lifetime 57 orders of magnitude higher at 77K than at room temperature (channel temperature reduced from 400K to 100K). Since this result is so unbelievable, some have applied a more empirically based T^6 law to obtain a lifetime increase of around five orders of magnitude at 77K.^[36] Note that both expressions predict a considerable increase in longevity at 77K which should allow the circuit designer to operate the devices harder, leading to further miniaturization. It should be noted that no experimental data to support these predictions have been performed and it is expected that at least initially, thermal cycling problems will limit lifetime.

2.3.5 Noise Reduction

Noise reduction has received more attention at cold temperatures than any other area of cryogenic microwave electronics. Confined mainly to radioastronomy, where the background noise temperature is 4K, considerable work on developing inexpensive and reliable alternatives to parametric amplifiers and MASERs has been underway for over a decade. In this section, noise will be discussed and the expectations of operating at 77K will be described.

The noise in any semiconductor device is usually a composite of three components: thermal noise with a white spectrum caused by phonon effects, shot noise caused by the quantum effect of electron-hole pairs being generated and recombined, and 1/f or flicker noise of unknown origin which has a 1/f spectrum that extends to a few MHz.^[53] Only the thermal component will be described here.

Noise figure is defined to be the signal-to-noise ratio at the input divided by the signal-to-noise ratio at the output. The noise figure of most low-noise amplifiers is mainly determined by the noise contributed by the first stage transistor. For a FET, the noise characteristics depend on the input match and the four noise parameters shown in equation 2.8.^[54] Here, NF_{min} is the minimum noise figure possible, which occurs when the source admittance ($g_s + jb_s$) is equal to the optimum noise admittance ($g_o + jb_o$). The parameter r_n , referred to as the equivalent noise resistance, is a measure of the sensitivity of the noise figure to source mismatch. A lower value allows wider bandwidth low-noise amplifiers to be fabricated.

$$\text{Noise Figure} = NF_{min} + \left(\frac{r_n}{g_o} \right) \left[(g_s - g_o)^2 + (b_s - b_o)^2 \right] \quad (2.8)$$

For MESFETs, equation 2.9 models the minimum noise figure correctly. K_f is normally between 2.5 and 3 for high quality substrates. The equation also holds for HEMTs with K_f values between 1.5 and 2. NF_{min} is proportional to the square root of the gate and source resistances divided by the transconductance, so HEMTs, with their higher g_m and lower gate to source resistance, feature superior noise properties. Although K_f is proportional to channel current due to the direct correlation with current fluctuations, g_m falls off quickly as pinch off is approached. Thus, an optimum current level, normally from 10% to 20% of I_{dss} , is required to minimize noise. The abrupt doping profile of the HEMT allows g_m to be maintained at lower channel currents and thus, are the choice for lowest noise.^[44,55]

$$NF_{min} = 1 + 2\pi K_f f C_{gs} \sqrt{\frac{R_g + R_s}{g_m}}, \quad K_f = 2 \sqrt{\frac{\mu_n I_{CH}}{V_{sat} g_m}} \quad (2.9)$$

For the lowest noise requirements, such as in radioastronomy, low temperatures have been applied. The larger g_m and the lower gate and source resistances previously discussed lowers F_{min} and makes the device less sensitive to the input match, while the input transmission line and matching circuits are less lossy. Note that the insertion loss of the input matching circuitry directly contributes to noise figure.

Experiments have shown that the noise temperature reduction with temperature follows equation 2.10, where x is 1.5 for conventional MESFETs and 1.7 for HEMTs, T_n is the noise temperature and T_d is the physical temperature of the device.^[56] That is, the degree of improvement from cooling HEMTs is more pronounced than for MESFETs.

$$\frac{T_{nCOLD}}{T_{n300K}} = \left(\frac{T_{dCOLD}}{T_{d300K}} \right)^x ; \quad NF = 1 + \frac{T_n}{T_o}, \quad T_o = 290K \quad (2.10)$$

Some recent results at room temperature and 13K for both MESFETs and HEMTs over frequency are shown in Figure 2.20. The HEMTs, which at 13K compare favourably with MASERS, have been specially doped to provide optimum performance at this temperature.^[57]

Figure 2.20. Noise Performance of Cryogenic and Room Temperature Devices^[57]

2.3.6 Insensitivity To Ambient Temperature

Another benefit from cryogenic operation is the lack of sensitivity to changes in the external ambient temperature. This is a severe problem in many systems where phase and gain compensation circuits must be used to provide stable characteristics over a large temperature fluctuation. For example, in avionics, operating temperatures may range over most of the -55°C to $+125^{\circ}\text{C}$ temperature specification.

Typical gain and return loss deviations of a MMIC amplifier over temperature are shown in Figure 2.21. Although variable attenuators and phase shifters may be used to compensate for the deviations with temperature, they add to the circuit complexity, increasing cost and lowering reliability. Clearly, the liquid/gas phase change of a liquid nitrogen bath or a controller integrated with a refrigerator will maintain a constant temperature irrespective of ambient temperature, implicitly solving this problem.

Figure 2.21. Gain and Return Loss of an MMIC Amplifier Over Temperature.^[58]

2.4 SUMMARY

In this chapter, MIC and MMIC technologies were briefly introduced, their room temperature limits and some performance areas that may benefit from low temperature operation were discussed. In particular, six performance areas that should improve at low temperatures were identified: higher Q, higher frequency of operation, higher power density, greater reliability, lower noise and insensitivity to ambient temperature.

Of the six areas, higher Q and frequency of operation are investigated in this thesis. Although promising, noise improvement at 77K is not studied since a complex test facility is required and considerable work has already been done.^[57,59,60] Power density was not investigated due to the requirement of a high power test facility with an increased cooling requirement. Since reliability enhancements are only relevant once other performance advantages from 77K operation have been clearly demonstrated and experiments to confirm this would be difficult to implement within a reasonable timeframe, this area was also not considered. In addition, the more stable operating characteristics with ambient temperature resulting from liquid nitrogen cooling are implicit and do not require any confirmation. Therefore, the experiments described in the following chapters focus on the areas of frequency of operation and Q to confirm the expectations presented here. Specifically, room temperature and 77K characterization of MIC and MMIC three-terminal active semiconductor devices are discussed in Chapter 3, while low temperature Q characterization of passive structures fabricated from gold and copper is described in Chapter 5.

CHAPTER 3 SEMICONDUCTIVE MICROWAVE CIRCUITS AT 77K: EXPERIMENTAL WORK

3.1 INTRODUCTION

Although the advantages of operating semiconductive microwave circuits at low temperatures have been known for some time, little experimental work has been conducted thus far. Reasons for this lack of activity include the difficulty of cooling devices in practical applications, little incentive to pursue this technology and the difficulty of obtaining accurate S-parameters of microwave devices operated at cryogenic temperatures. However, today, the practicality and incentive issues have been overcome due to the maturity of low temperature refrigeration systems as well as the performance potential of low temperature semiconductive and superconductive circuits combined with the present economic barriers to performance advances using processing technology alone. Only the measurement of microwave devices whose true characteristics are masked by the losses and delays of the input/output cables and test fixtures remain as an obstacle. This chapter describes how recent advances in network analyzer calibration techniques have been combined with a novel apparatus to overcome this problem, allowing microwave devices to be accurately characterized at cryogenic temperatures.

This experimental work concentrates on three-terminal active devices. As previously stated, the lack of a three-terminal gain element in superconductive technology shall make semiconductive gain elements essential in the construction of a hybrid semiconductive/superconductive high performance system. Although higher levels of performance are possible by tailoring the doping profile of the active devices for cryogenic operation^[61], this has not been considered because such optimization was not available with the MIC and MMIC devices used here.

Previewing the chapter, a novel cryogenic microwave characterization procedure and apparatus will be discussed first. The success of this step allows a variety of cooled MIC and MMIC devices to be characterized and qualitatively analysed at frequencies up to 20 GHz. An enhanced calibration procedure and apparatus will be described which improves on the earlier proof-of-concept work. Three generations of three-terminal microwave semiconductor devices are measured and analysed at 297K and 77K. FETs, HEMTs and Pseudomorphic-HEMTs (P-HEMTs) are accurately characterized over the frequency range from 1 GHz to 20 GHz, allowing small-signal models to be closely fitted at both temperatures. By determining the performance improvement offered by low temperature operation, the suitability of the three devices for use at cryogenic temperatures is determined.

3.2 CRYOGENIC VECTOR MEASUREMENT APPARATUS AND TECHNIQUE

In this section, the measurement apparatus and technique developed to obtain small-signal S-parameters of MIC and MMIC elements at 77K will be discussed. Before explaining the technique, the additional measurement problems created by operating microwave circuits at 77K will be described. A discussion of an existing method and its drawbacks will be followed by a discussion of the novel approach, developed in this work, that provides real-time, broadband, de-embedded S-parameter measurements at 77K. The method relies on the Through/Reflect/Line (TRL) calibration technique whose theory will be developed before detailing the experimental apparatus and technique. Lastly, the accuracy of this technique will be discussed.

In addition to the normal de-embedding required to obtain accurate S-parameters of microwave devices at room temperature, problems created by low temperature operation must also be overcome. These problems include condensation on the devices when operating below the dew point and the changing amplitude and phase of

the input/output cables or waveguides and test fixture with temperature. Condensation creates changes in the effective dielectric constant since the permittivity of both water and ice is far higher than that of air ($90 > \epsilon_r(\text{H}_2\text{O}) > 60$).^[62] Normally a dry nitrogen or vacuum atmosphere is required to solve this problem. Figure 3.1 illustrates the variation in the amplitude and phase of the input reflection coefficient, S_{11} , with temperature as a 0.085" semi-rigid coaxial cable, terminated in a short circuit, is cooled from 297K to 77K. Note that the plots are normalized to the 297K values. As shown, after reaching thermal equilibrium, the two-way phase change is approximately linear with frequency with a peak of -75° at 26.5 GHz while the amplitude change is non-linear with frequency with a peak of 1 dB. A similar experiment with a 0.118" K-cable produced a reduced phase change of -7° and a larger amplitude change of 1.2 dB. This illustrates the errors of applying a room temperature calibration once the apparatus is cooled.

Figure 3.1. Amplitude and Phase Changes of a 0.085" Cable Over Temperature.

Although the cables could be de-embedded if the conventional short/open/ 50Ω load (SOLT) standards could be used at 77K, early experiments showed

that both the 50Ω load and short circuit deviated significantly from their room temperature calibration kit definitions when cooled. Even if successful, this method would not solve the problem of de-embedding the test fixture, whose characteristics also change with temperature.

Before discussing the calibration technique developed which solves these problems, an existing method will be described and its drawbacks identified. In this case, no test fixture was used.^[63] Short lengths of high thermal resistivity, ultraminiature cable with a 0.004" Be-Cu inner conductor and stainless steel outer conductor were attached directly to the device under test. Since this cable could support a large temperature gradient, phase and gain changes of the cable were minimized. This allowed a conventional room temperature calibration to be corrected by manually de-embedding the estimated cable changes following a measurement. Results of MESFETs operating at 90K were obtained for frequencies up to X-band. Drawbacks to this method include a test temperature above that of the liquid nitrogen bath, the requirement to construct the cables, since they are not available commercially, and if multiple devices are to be measured, the difficulty of manually de-embedding the different coaxial cables.

In this work, custom apparatus and test fixtures were fabricated to overcome the calibration and condensation problems. Application of the TRL technique allows the calibration to be performed in-situ at cryogenic temperatures, intrinsically removing the effects of both the cables and test fixture on the measurements.

The theory underlying the TRL calibration technique will now be developed. Although it will be seen that this explanation is mathematical in nature and not easily visualized, unlike the SOLT method, the end result of de-embedding systematic errors to obtain corrected S-parameters is similar.

At any temperature, the major problem with obtaining accurate vector measurements of microwave devices rests with the cancellation of systematic errors through a process referred to as calibration. These errors are shown in Figure 3.2 as the eight ϵ_{ij} terms representing the S-parameters of error boxes A and B on the input

and output of the device under test. Included in these boxes are the amplitude and phase effects of the cables and test fixtures as well as the imperfect reflectometers of the network analyzer itself. For devices mounted on microstrip, the largest error is normally the coax-to-microstrip transition discontinuity which is difficult to model, and therefore, difficult to remove analytically. Hence, a calibration to determine the characteristics of the error boxes so their effects may be cancelled is required to obtain the true S-parameters $[S]$ of the device.^[64]

Figure 3.2. Two-Port Measurement System Including Error Model Coefficients.^[64]

Rather than using precision short, open and 50Ω standards, a TRL calibration is performed by connecting three transmission line standards: a through, a line slightly longer than the through and high reflection terminations, as shown in Figure 3.3. Here, two-port measurements of the through and the line which is longer by length l , eight S-parameters in all, and two one-port reflection measurements of high reflection coefficient transmission lines are required. For the reflection standards, either open or short circuit terminations may be used to provide the reflection

coefficient, Γ , which is assumed identical at both ports. Provided that the characteristic impedance of all lines is known and identical, a wide bandwidth calibration, normalized to this impedance, may be achieved.

Figure 3.3. TRL Procedure and Assumed S-Parameters of Transmission Line Standards.^[64]

These ten measurements may be used to obtain the two error box coefficients by solving a system of linear equations with matrix algebra.^[65] To begin, it is useful to rearrange the scattering relationship shown in equation 3.1 into the form shown in equation 3.2 where $\mathbf{R}$ is the wave cascading matrix.

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned} \quad (3.1)$$

$$\begin{pmatrix} b_1 \\ a_1 \end{pmatrix} = \frac{1}{S_{21}} \begin{pmatrix} -S_{11}S_{22} + S_{12}S_{21} & S_{11} \\ -S_{22} & 1 \end{pmatrix} \begin{pmatrix} a_2 \\ b_2 \end{pmatrix} = \mathbf{R} \begin{pmatrix} a_2 \\ b_2 \end{pmatrix} \quad (3.2)$$

Note that the $\mathbf{R}$ matrix for two or more two-ports in cascade is simply the product of the individual $\mathbf{R}$ matrices. Therefore, if we let the cascading matrices of the two-port error boxes A and B be denoted by $\mathbf{R}_a$ and $\mathbf{R}_b$, respectively, while $\mathbf{R}_t$ represents their cascade "through" connection. Then

$$\mathbf{R}_t = \mathbf{R}_a \mathbf{R}_b \quad (3.3)$$

while if $\mathbf{R}_d$ represents the "line" combination

$$\mathbf{R}_d = \mathbf{R}_a \mathbf{R}_l \mathbf{R}_b \quad (3.4)$$

where $\mathbf{R}_l$ represents the line which has been inserted.

Solving equation 3.3 for $\mathbf{R}_b$ gives

$$\mathbf{R}_b = \mathbf{R}_a^{-1} \mathbf{R}_t \quad (3.5)$$

so that $\mathbf{R}_b$ may be obtained from $\mathbf{R}_a$ and $\mathbf{R}_t$. Next, equation 3.5 is used to eliminate $\mathbf{R}_b$ from equation 3.4 yielding

$$\mathbf{T} \mathbf{R}_a = \mathbf{R}_a \mathbf{R}_l \quad (3.6)$$

where

$$\mathbf{T} = \mathbf{R}_d \mathbf{R}_l^{-1} \quad (3.7)$$

which may be found from the parameters of the through and line two-ports.

If γ and l represent the propagation constant and length of the delay line, respectively, then assuming the line is nonreflecting,

$$\mathbf{R}_l = \begin{pmatrix} e^{-\gamma l} & 0 \\ 0 & e^{\gamma l} \end{pmatrix} \quad (3.8)$$

Finally, letting the elements of $\mathbf{R}_a$ and $\mathbf{T}$ be represented by r_{ij} and t_{ij} , respectively, expansion of equation 3.6 gives equation 3.9 where five unknowns, $\mathbf{R}_a$ and γl , are expressed in four linear equations.

$$\begin{aligned} t_{11} r_{11a} + t_{12} r_{21a} &= r_{11a} e^{-\gamma l} \\ t_{21} r_{11a} + t_{22} r_{21a} &= r_{21a} e^{-\gamma l} \\ t_{11} r_{12a} + t_{12} r_{22a} &= r_{12a} e^{\gamma l} \\ t_{21} r_{12a} + t_{22} r_{22a} &= r_{22a} e^{\gamma l} \end{aligned} \quad (3.9)$$

By measuring the unknown high reflection coefficient standard, Γ , on port A, equation 3.10 may be obtained.

$$\Gamma_{\text{measured}_a} = \frac{\frac{r_{11a}}{r_{22a}} \Gamma + \frac{r_{12a}}{r_{22a}}}{\frac{r_{21a}}{r_{22a}} \Gamma + 1} \quad (3.10)$$

Similarly, solving at port B, equations 3.11 and 3.12 are obtained.

$$\begin{aligned} t_{11}r_{11b} + t_{12}r_{21b} &= r_{11b}e^{-\gamma l} \\ t_{21}r_{11b} + t_{22}r_{21b} &= r_{21b}e^{-\gamma l} \\ t_{11}r_{12b} + t_{12}r_{22b} &= r_{12b}e^{\gamma l} \\ t_{21}r_{12b} + t_{22}r_{22b} &= r_{22b}e^{\gamma l} \end{aligned} \quad (3.11)$$

$$\Gamma_{\text{measured}_b} = \frac{\frac{r_{11b}}{r_{22b}} \Gamma + \frac{r_{12b}}{r_{22b}}}{\frac{r_{21b}}{r_{22b}} \Gamma + 1} \quad (3.12)$$

Since Γ is assumed identical at both ports A and B and T may be derived from measurements, the ten equations in ten complex unknowns, R_a , R_b , γl and Γ , may be solved. Illustrating the solution for a single term of R_a : From equation 3.9, equations 3.13 through 3.15 may be derived where r_{11a}/r_{21a} , r_{12a}/r_{22a} and $e^{2\gamma l}$ may be determined.

$$t_{21} \left(\frac{r_{11a}}{r_{21a}} \right)^2 + (t_{22} - t_{11}) \left(\frac{r_{11a}}{r_{21a}} \right) - t_{12} = 0 \quad (3.13)$$

$$t_{21} \left(\frac{r_{12a}}{r_{22a}} \right)^2 + (t_{22} - t_{11}) \left(\frac{r_{12a}}{r_{22a}} \right) - t_{12} = 0 \quad (3.14)$$

$$e^{2\gamma l} = \frac{t_{21} \left(\frac{r_{12a}}{r_{22a}} \right) + t_{22}}{t_{12} \left(\frac{r_{21a}}{r_{11a}} \right) + t_{11}} \quad (3.15)$$

analyzer is connected to a microwave test fixture using K-cables held inside a high thermal resistivity stainless steel tube to minimize liquid nitrogen boiloff. A dry nitrogen atmosphere is maintained within the shroud to prevent condensation from forming. The aluminum shroud also shields the device under test from electromagnetic interference. The cables and test fixture are stationary while the cryoflask is raised to cool the device, eliminating any gain or phase deviations due to cable flexure.

Figure 3.4. Liquid Nitrogen Immersion Apparatus.

The TRL technique allows the effects of the test fixture's microstrip transmission lines and microstrip-to-coax launchers, as well as the interconnecting cables, to be mathematically removed, resulting in real-time de-embedded measurements. By measuring the standards and devices at the same temperature, only the minor effect of the wire bonds connecting the device remain to be stripped. The

phase and amplitude errors caused by the cable and test fixture characteristics changing with temperature are inherently corrected.

Although the TRL technique assumes that the launchers and microstrip input/output lines on every standard and device test fixture are identical, separate test fixtures for each standard and measured device are used to ensure repeatable connections at 77K. Since the launchers and input/output lines on the different test fixtures are not identical, the accuracy normally obtained using commercial TRL test fixtures at room temperature is degraded.^[66]

Gold microstrip transmission lines patterned on 0.010" thick alumina substrates form the standards as well as the input/output lines of the measurement test fixtures. The standards required to provide a calibration from 2.5 GHz to 20 GHz include a zero length through, a reflection standard whose gap between the opens corresponds to the space occupied by the device and a line 0.101" longer than the through. The resulting standard definitions and class assignments for the 8510 Calibration Kit are shown in Appendix I.

MIC devices are silver epoxied onto 0.020" or 0.050" wide ridges on the measurement test fixtures and thermocompression wire bonded into the circuit. A complete set of standards and two mounted devices are shown in Figure 3.5. The right angle bends in the microstrip transmission lines were required due to the limited cryoflask opening which prevented a straight through topology. To ensure phase and amplitude accuracy, the microstrip lines and launcher recesses are kept to a tolerance of 0.001". Both the alumina and the centre pins of the K-connector spark plug launchers are attached using indium/lead solder to ensure a solid connection at 77K. Although the test fixtures were initially specified to be fabricated from kovar which possesses the same thermal expansion coefficient as alumina, machining difficulties resulted in gold plated brass being used. The small size of the alumina substrates allowed the test fixtures to survive tens of thermal cycles before the alumina substrates delaminated.

Figure 3.5. Calibration Standards and Devices on Test Fixtures - counterclockwise from top left - Through, Line, Open, Interdigitated Capacitor, Gould 0503 MESFET.

The frequency and time domain one-port characteristics of a typical through standard with a matched load on the output, at room temperature, are shown in Figure 3.6a) and b), respectively. Its input return loss, $|S_{11}|$, shown to be greater than 20 dB up to 15 GHz, is mainly limited by the three reflections dominating the time

domain response. The largest reflections occur at the two coax-to-microstrip launchers, while the third discontinuity is the 50 Ω male load on the output which was substituted for the 50 Ω female calibration load. The microstrip bends have a secondary effect compared with the launchers. The insertion loss (not shown) is linear with frequency. At 20 GHz, its value is approximately 1 dB.

Figure 3.6. Return Loss of a Through Standard.

Since the accuracy of this method rests with the different calibration and test fixtures being closely matched, considerable care was taken to ensure this. Every test fixture was characterized and those with significant deviations from a launcher discontinuity peak of 0.050 were not used. In all, only half the test fixtures met this specification. A typical characterization is shown in Figure 3.7 for a test fixture with a 0.020" raised ridge whose gap has been bridged using bond wires. The return loss degradation, shown in Figure 3.7a), is primarily due to the bond wire discontinuity which occurs half-way between the launcher discontinuities as shown in Figure 3.7b). The insertion loss of this test fixture is similar to that of the through.

Figure 3.7. Return Loss of a 0.020" Wire Bonded Gap.

To perform a 77K TRL measurement, the cryoflask was slowly raised to immerse the cold finger in liquid nitrogen. Copper-constantan thermocouples mounted on the test fixture allowed the temperature of the system to be maintained by controlling the immersion depth to within one millimeter. As liquid nitrogen has a dielectric constant of 1.45, its effect on the phase of the measurements is significant. Therefore, it was important that the circuit remained above the liquid-to-gas transition area where boiling can create time varying measurement errors.^[67] Thermocouples mounted on the K-cables inside the stainless steel feed tube were used to monitor the thermal properties of the system. Approximately 45 minutes after immersion, the system reached thermal and electrical equilibrium, allowing a measurement to be taken. To change the test fixture, the flask was lowered and a heater warmed the test fixture to room temperature after an additional 45 minutes. The three standards and the measurement test fixture were thermally cycled using this method, resulting in a calibration requiring six hours and each device measurement requiring an additional two hours.

Since the standards and device to be measured are mounted on different test fixtures, measuring the same standards used to calibrate does not reflect the true accuracy of this method because they are defined by the calibration kit to be ideal. For example, the results of reconnecting the through calibration standard following a 77K calibration, shown in Figure 3.8, only demonstrate the excellent repeatability of the connections.

Figure 3.8. $|S_{11}|$, $|S_{21}|$ and $\angle S_{21}$ of Reconnected Through Calibration Standard at 77K.

Therefore, to determine the accuracy expected, other sets of "identical" standards were measured following the calibration. A typical "identical" through, as shown in Figure 3.9, reflects the actual accuracy of this method. Repeatability has degraded from better than 40 dB to 23 dB.

Figure 3.9. $|S_{11}|$, $|S_{21}|$ and $\angle S_{21}$ of an "Identical" Through Standard at 77K.

The results of measuring several "identical" through standards mounted on different test fixtures over the 2.5 GHz to 20 GHz band and following calibrations at both 77K and 297K are summarized in Table 3.1. Deviations from an ideal through standard ($S_{21} = 1\angle 0$, $S_{11} = S_{22} = 0$) are shown for both the reconnected calibration standard as well as different standards. Since the $|S_{21}|$ deviations were random and centred about 0 dB, they are quoted in peak-to-peak units whereas the angular S_{21} deviations were found to increase linearly with frequency and the values quoted are the 20 GHz errors. The "Calibration Standard" data is included to show the accuracy possible using a test fixture having identical launchers and input/output lines for all measurements. As a result of using different test fixtures at 77K, the return loss is degraded 17 dB while the magnitude and phase errors of S_{21} increase. A reduction in accuracy at 77K compared with room temperature is also evident. Since this reduction is minor for the "Different Standard", room temperature measurements may be used to obtain an estimate of the accuracy of this method at cryogenic temperatures. Overall, the accuracy of the transmission measurements is ± 0.05 dB in magnitude and a few degrees in angle at 20 GHz, while the reflection measurements are similar to those achieved with a conventional SOLT calibration where 50Ω loads having 25 dB return loss at 20 GHz are used.

	297K		77K	
	Calibration Standard	Different Standard	Calibration Standard	Different Standard
Minimum Return Loss (dB)	>50	>25	>40	>23
$\Delta S_{21} _{\text{pk-pk}}$ (dB)	<0.02	<0.08	<0.06	<0.10
$\Delta\angle S_{21}$ (deg.)	<0.5	<2.0	<0.8	<3.0

Table 3.1. Accuracy of a Through Standard at 297K and 77K

Although the accuracy of the transmission parameters is good, reflection measurements are less acceptable. Measurements of open reflection standards revealed phase ripple of 10 degrees peak-to-peak above 10 GHz when remeasuring the standard. They are mainly a result of the test fixture launchers not being identical.

In summary, a technique has been developed to provide real-time, broadband, de-embedded S-parameter measurements of microwave devices operated at 77K. It applies the TRL calibration technique in-situ at cryogenic temperatures for the first time within a custom liquid nitrogen immersion apparatus.

3.3 PROOF OF CONCEPT 77K MEASUREMENTS

This section describes the measurement of an MIC capacitor and several MESFET devices. The results are used to verify the measurement technique and to evaluate the changes in their characteristics over temperature.

The measurement of a 0.5 pF interdigitated capacitor, measuring 0.035" x 0.025" and fabricated using thin-film gold deposited on alumina, shown in Figure 3.10a), will be discussed first. The input reflections of the capacitor, grounded at one terminal, at room temperature and 77K are compared in Figure 3.10b). Overall, the capacitor is less lossy at 77K, which agrees with the expected behaviour of an interdigitated capacitive structure whose ohmic finger resistance has decreased when cooled, improving its Q. The slight counterclockwise phase shift may be caused by a decrease in capacitance and/or parasitic series inductance of the cooled capacitor. Effects of the phase ripple calibration error are observed when comparing the relative position of the 10 GHz and 15 GHz markers. The additional inductance of the 0.0007" diameter bond wires has not been removed from these results to demonstrate the extent of de-embedding offered by this technique. Conventional manual techniques may be used to strip away these effects.

a) Microphotograph

b) Response at 300K and 77K

Figure 3.10. Interdigitated MIC Capacitor

An unpackaged Gould 0503 $0.3\ \mu\text{m} \times 300\ \mu\text{m}$ π -gate MESFET, shown in Figure 3.11a), was also measured. Both the 77K and room temperature measurements were made with a 3.5V drain bias and an I_{CH}/I_{DSS} ratio of 0.2. The four S-parameters at the two temperatures are plotted in Figure 3.11b). Again, the effects of the bond wires have not been removed. The input reflection curves at the two temperatures are almost identical, indicating that the gate-to-channel capacitance and resistance are relatively insensitive to temperature. A large increase in the magnitude of transmission gain is coupled with a small counterclockwise phase shift at 77K. This larger magnitude leads to a 1.5 dB increase in the MSG/MAG over the entire band. Both S_{12} curves indicate a reverse isolation of approximately 20 dB. The slightly larger 77K value is probably due to the increase in transmission gain. The output reflection coefficient is smaller in magnitude at 77K, indicating lower drain-to-source resistance due to the higher mobility resulting from a reduction in the thermal scattering of the carriers.

A TriQuint Semiconductor $1\ \mu\text{m} \times 200\ \mu\text{m}$ T-gate MESFET, diced from their MMIC Process Control Monitor, was also characterized at low temperatures. This device, shown in Figure 3.12a), was operated at $I_{DSS}/2$ with a 4V drain bias resulting in the room temperature and 77K responses shown in Figure 3.12b). Except for the smaller increase in transmission gain and the smaller decrease in output resistance upon cooling to 77K, its behaviour is similar to that of the Gould device discussed earlier.

For both MESFET's, only transmission gain and output reflection coefficient appear temperature sensitive. This suggests that room temperature FET models may be applied at 77K with only slight modification, as will be confirmed in later sections.

a) Microphotograph

b) Response at 300K and 77K

Figure 3.11. Gould MESFET

a) Microphotograph

b) Response at 300K and 77K

Figure 3.12. TriQuint MESFET

Although these measurements exhibit resonances above 10 GHz due to launcher variation between test fixtures, it should be noted that these were the most accurate 20 GHz cryogenic microwave vector measurements when published.^[68] This cryogenic measurement technique has been referenced in an overview paper on MMIC measurement techniques^[69] and has already been applied in the realization of cryogenic Ka-band low-noise amplifiers for the radioastronomy community.^[70]

The test fixture and apparatus were subsequently modified to further increase the accuracy of the technique. The excellent improvement which resulted is described in the following section.

3.4 ENHANCED CRYOGENIC VECTOR MEASUREMENT APPARATUS AND TECHNIQUE

Although more closely matched test fixtures should extend the resonance free region of the earlier method to higher frequencies, this was found extremely difficult to realize in practice. Therefore, a new cryogenic split-block test fixture was developed for use with the TRL calibration technique. Also, a cryocooler was used in place of a liquid nitrogen dewar with a larger mouth, allowing lower temperatures to be achieved. In the following, the repeatability of the technique and the measurement of a transmission line at 297K and 77K are demonstrated from 0.1 GHz to 20 GHz.

The apparatus, illustrated in Figure 3.13, consists of a customized cold head on an RMC Cryosystems LTS-22-IR helium refrigerator coupled with the HP8510B. Semi-rigid coaxial cables connect the test fixture to coaxial feedthroughs which in turn are connected to the test ports of the HP8510B. The use of 0.118" K-cables results in a minimum temperature of 50K being obtained at the test fixture. Additional details on the operation of the refrigerator may be found in Section 5.3.

Figure 3.13. Cryocooler-Based Apparatus

As before, the effects of the coaxial cables and test fixture at cryogenic temperatures are intrinsically calibrated out by applying the TRL technique in situ. The split-block test fixture, shown in Figure 3.14, provides the calibration standards as well as the input/output lines to connect the device under test. To perform a calibration from 0.1 GHz to 20 GHz, a zero length through formed by connecting the halves of the test fixture directly together, open reflection standards formed by separating the halves and a 0.101" long transmission line mounted on a shim sandwiched between the halves, are sequentially cooled and measured. Since the same input and output lines are used for the standards and measurement test fixture, greater accuracy and higher frequency measurements are possible. Removable connections for the through and line standards and the device are made with gold bond wires to ensure solid connections at cryogenic temperatures. Test fixture construction is similar to that discussed earlier. However,

high temperature teflon K-launchers, required to withstand the repeated thermal cycling during thermocompression bonding, are used. In addition, the test fixture material was changed from brass to Thermkon 70M (an 85%Mo/15%Cu metal matrix) to achieve a better thermal expansion match with the larger alumina pieces.^[20,71] Unlike kovar, it was possible to machine this metal matrix into complex 3D shapes. However, gold plating to provide solderability and wire bond grounds proved difficult; the steps required are shown in Appendix II.

Figure 3.14. Split-block Test Fixture with Line Standard: Disassembled and Assembled.

Approximately one hour is required to reach 77K, while 30 minutes is required to return to room temperature. Thus, a full two-port calibration requires 4.5 hours, and each device measurement requires an additional 1.5 hours for the thermal transitions. The wire bonding time slightly lengthens the procedure.

Measurements of the split-block through connection at room temperature are shown in Figure 3.15. Return loss is better than 13 dB and insertion loss is below 1.5 dB to 26.5 GHz. The coax-to-microstrip launcher discontinuities still dominate the overall reflection of the test fixture. The bond wire connection discontinuity is also evident between the launchers. Since the characteristics of the bond wires may change from connection to connection, this limits the accuracy of this method. As the magnitude of the wirebond discontinuity is smaller than that of the launchers, performance superior to the earlier method using separate test fixtures is expected.

Figure 3.15. Split-Block Through Characteristics.

Measurements of the reconnected standards from 0.1 GHz to 20 GHz, following calibrations at 77K and 297K, are summarized in Table 3.2. Deviations of the standards from an ideal through ($S_{21} = 1\angle 0$, $S_{11} = S_{22} = 0$) and an ideal open ($S_{11} = S_{22} = 1\angle 0$) are shown. The deviations increase linearly with frequency, so the values noted are approximately the errors at 20 GHz. Larger deviations evident at 77K are due to the drift of the network analyzer during the lengthened calibration and verification cycle.

		297K	77K
THROUGH	Minimum Return Loss (dB)	>35	>30
	$\Delta S_{21} $ (dB)	<0.05	<0.10
	$\Delta\angle S_{21}$ (deg.)	<1.0	<3.0
OPEN	$\Delta S_{11} $ (dB)	<0.05	<0.10
	$\Delta\angle S_{11}$ (deg.)	<2.0	<3.0

Table 3.2. Deviations of Reconnected TRL Calibration Standards

Qualitatively, the accuracy of this technique at 297K is similar to that of a wafer prober measurement which is the current state of the art in room temperature characterization.^[72] Most deviations are twice those of a wafer prober calibration checked after a few hours, the time required to bond and re-bond the standards into the test fixture. Only the through return loss is substantially worse than the 50 dB typical of a wafer prober. Time domain analysis indicates this is due to variations in the bond wire connections and is the inherent limit of this technique.

To verify the accuracy of this technique, a 0.202" long transmission line (twice the length of the line standard) was measured following a calibration. The author has used this method to validate room temperature wafer prober calibrations at frequencies up to 50 GHz. Measurements at 297K and 77K are shown in Figure 3.16. The return loss at 77K is slightly degraded due to the reasons discussed earlier.

Extremely small reductions in insertion loss and transmission delay time at 77K, due to the lower ohmic resistance and physical shrinkage of the line, are observed. Again, bond wires have not been de-embedded.

Figure 3.16. Response of a 0.202" Transmission Line at 297K and 77K^[73]
 (Markers at 5, 10 and 15 GHz: $\Delta \nabla$ 297K $\blacktriangle \blacktriangledown$ 77K)

In summary, an enhanced measurement technique has been developed which provides extremely accurate, real-time, broadband, de-embedded S-parameters of microwave devices operated at cryogenic temperatures. It applies the TRL calibration technique in-situ at cryogenic temperatures within a custom cryocooler apparatus to obtain measurements that are similar in accuracy to those of a room temperature wafer prober for the first time.^[73] This contribution to the measurement of cryogenic electronics has recently been acknowledged.^[74]

3.5 CHARACTERIZATION AND MODELLING OF THREE-TERMINAL SEMICONDUCTIVE DEVICES AT CRYOGENIC TEMPERATURES

In this section, three generations of three-terminal microwave semiconductive devices are measured and analysed at 297K and 77K. FETs, HEMTs and Pseudomorphic-HEMTs (P-HEMTs) are accurately characterized over the frequency range from 1 GHz to 20 GHz using the split-block test fixture and the TRL calibration technique discussed above. Accurate characterization allows small-signal models to be closely fitted to the devices at both temperatures. Analysis of the changes in the intrinsic model elements with temperature allows the suitability of the three devices for use at cryogenic temperatures to be determined. The performance improvement offered by low temperature operation is described.

To characterize these three-terminal semiconductive devices, die are silver epoxied onto 0.020" wide shims sandwiched within the test fixture and connected with 0.0007" diameter gold bond wires. A P-HEMT mounted on the split-block test fixture is shown in Figure 3.17.

Figure 3.17. Split-block Test Fixture with P-HEMT: Disassembled and Assembled

The devices under test included a $0.3\mu\text{m} \times 280\mu\text{m}$ NEC NE673 FET, which has been widely used for earlier CRC projects, a $0.25\mu\text{m} \times 100\mu\text{m}$ Fujitsu FHR10X HEMT, which was demonstrated to be suitable for cryogenic low noise amplifiers^[75] and a $0.25\mu\text{m} \times 150\mu\text{m}$ Comsat LNF001 P-HEMT^[76], which was the only P-HEMT available at the time of this work.

Measured and modelled S-parameters of a NE673 FET, a FHR10X HEMT and a LNF001 P-HEMT at both 297K and 77K are shown in Figures 3.18, 3.19 and 3.20, respectively. The temperature and frequency are identified by marker symbols placed at 5, 10 and 15 GHz. Again, the effects of the input/output bond wires on these results have not been removed to demonstrate the extent of de-embedding offered. The measurements are relatively resonance free, allowing subtle changes in all S-parameters to be observed. However, major changes with temperature reduction are again confined to the increased transmission gain and decreased output impedance. The rougher traces at 77K are due to the drift of the network analyzer during the lengthened calibration and measurement cycle. Operating conditions for the devices, biased for minimum noise figure, are shown in Table 3.3. As the P-HEMT is an enhancement device with little channel current at $V_{gs} = +0V$, its I_{DSS} values are quoted where transconductance is maximum, at $V_{gs} \sim +0.5V$.

	NE673		FHR10X		LNF001	
	297K	77K	297K	77K	297K	77K
$V_D(V)$	3	3	2	2	2	2
$I_{DSS} (mA)$	34	26	26	26	18	11
$I_{CH} (mA)$	13	10	5	5	6	6

Table 3.3. Three-Terminal Semiconductor Device Bias Conditions

2

**PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT**

Figure 3.18. Measured and Modelled Responses of a NE673 FET

Figure 3.19. Measured and Modelled Responses of a FHR10X HEMT

Figure 3.20. Measured and Modelled Responses of a LNF001 P-HEMT

As these devices include gate recesses, non uniform doping profiles, a complex carrier velocity-electric field relationship and two-dimensional electric field components, the equations presented earlier in Section 2.3.2 are not sufficient to model the experimental data. Fortunately, Gascode of England invested 30 man-years of effort in developing physics-based software packages which use finite element analysis to accurately model these devices. S-parameter data may be fitted to a small-signal model using 'Fetlink' and S-parameters may be generated based on the physical description of the device using 'Fetbase'.^[77]

The three-terminal device model shown earlier in Figure 2.12 was fitted to the measured S-parameters using Fetlink software. Although originally developed for FETs operating at room temperature, Figures 3.18 through 3.20 illustrate how closely this physics-based program fits all three devices at both temperatures. The model elements for the devices at both temperatures as well as the calculated cutoff frequencies are shown in Table 3.4. Fetlink requires an R_g value, which in this case is obtained through an initial optimization with Supercompact; all other element values result from the fit. Negative values for L_s , R_d and R_s are due to the non-physical basis of the equivalent circuit model.^[78] The zero value of R_i at 77K for the HEMT is not physically possible and shows the software or measurement accuracy may need to be improved if small gate periphery devices are to be correctly analysed at cryogenic temperatures. The software assumes room temperature mobility characteristics which will probably need to be modified for 77K modelling. Input/output inductance values for the same device differ at the two temperatures due to different bond wires being used to connect the die into the test fixture following calibrations at each temperature. In the case of the LNF001, the device was wafer probed at room temperature.

	NE673		FHR10X		LNF001	
	297K	77K	297K	77K	297K	77K
gm (mS)	50.9	72.8	26.9	42.5	37.5	55.7
Cgc (pF)	0.309	0.317	0.116	0.113	0.185	0.322
Ggs (mS)	0.137	0.213	0	0.077	0.037	0.134
Rds (Ω)	230	124	334	232	461	371
Ri (Ω)	3.7	1.9	2.2	0	7.5	1.5
τ (ps)	3.5	2.9	1.9	0.8	4.2	2.1
Cgd (pF)	0.024	0.035	0.015	0.021	0.011	0.011
Cds (pF)	0.100	0.093	0.058	0.063	0.035	0.070
Lg (nH)	0.119	0.125	0.135	0.161	0.007	0.161
Rg (Ω)	2	2	1	0.5	2	1
Ld (nH)	0.104	0.202	0.089	0.148	0.100	0.100
Rd (Ω)	-0.24	-2.1	2.8	5.6	-11.9	1.5
Ls (nH)	0.021	0.017	0.021	0.024	-0.002	0.009
Rs (Ω)	1.0	1.8	0.8	1.0	-1.8	0.75
Cpg (pf)	0.01	0.01	0.02	0.02	0	0
Cpd (pf)	0	0	0	0	0	0
Cpgd (ff)	15	2	6	0	14	5
Gpgd (mS)	0	0	0.007	0	0.039	0
f_T (GHz)	24.3	32.9	32.7	50.5	30.4	26.6

Table 3.4. Linear Model Element Values of Three-Terminal Semiconductor Devices

At 77K, the NE673 exhibits a large increase in transconductance, a small drop in transit time and an improved output match, resulting in a cutoff frequency increase of 35%. The FHR10X shows the largest increase in transconductance, the largest decrease in transit time and a smaller drop in output resistance, resulting in a 54% higher cutoff frequency. This follows from the increased carrier mobility at lower temperatures due to fewer phonon collisions in the lightly doped layer which confines the 2-D gas in a HEMT. The LNF001 exhibits a large increase in transconductance, a large decrease in transit time and the smallest drop in output resistance. Again, this is due to the enhanced mobility of the 2-D gas in the P-HEMT structure. However, a substantial increase in C_{gc} results in a 13% drop in cutoff frequency! An increase in C_{ds} at 77K is also observed. Both capacitance effects are believed due to defects in the super lattice, which create deep levels, decreasing depletion zone widths. It should be noted that these were early sample devices and production devices are still not commercially available. A similar problem was encountered with early HEMTs wherein traps created negative resistance bias regions and memory effects at low temperatures. HEMTs are now processed with cleaner MBE techniques and passivated with SiO to alleviate these problems; similar improvements are anticipated for the P-HEMTs.^[59]

Of the three devices characterized, the FHR10X exhibits the largest performance improvement at cryogenic temperatures due to its mobility enhancement and defect free structure.

These results and technique should be useful to the field of cryogenic microwave electronics, where small-signal equivalent models are required for both gain and noise matching. They have recently been accepted for publication.^[79]

3.6 SUMMARY and CONTRIBUTIONS

Techniques to characterize microwave devices and circuits in real time at cryogenic temperatures using both a liquid nitrogen immersion and a cryocooler-based apparatus were developed for the first time. Fully corrected S-parameters of MIC and MMIC devices were obtained in real time at frequencies up to 20 GHz. The enhanced technique, with an accuracy comparable to a wafer prober operating at room temperature, allowed changes in the small-signal circuit elements of three generations of three-terminal semiconductive devices to be observed over temperature.

Combining the TRL calibration technique with a cooled apparatus to obtain extremely accurate measurements, as described in this work, has already been applied by several researchers in the field of cryogenic electronics for both test fixture measurements and recently, for cryogenic wafer probing.^[80] The proof-of-concept technique was adapted at Fujitsu in the realization of cryogenic low-noise amplifiers for the Japanese radioastronomy community,^[70] while the enhanced technique has been referenced by those involved in the High Temperature Superconductivity Space Experiment at the Naval Research Lab.^[74] This technique will also play a key part in developing hybrid semiconductive/superconductive microwave integrated circuits operating at liquid nitrogen temperatures, as discussed in later sections of this work.

CHAPTER 4 SUPERCONDUCTIVE MICROWAVE CIRCUITS: BACKGROUND

4.1 INTRODUCTION

In the preceding decades, superconductive electronics has been developed using Low Temperature Superconductor (LTSC) technology. Both passive and active microwave circuits with unrivalled performance have been realized. Passive microwave structures which apply the low loss and dispersion properties of superconductors include high Q resonators/filters and transmission lines capable of carrying picosecond duration pulses. Active superconductive circuits apply the Josephson tunnel junction, a two-terminal device, which may be controlled by a magnetic field or current in close proximity. A variety of microwave and millimeterwave circuits have been formed with Josephson junctions due to their strong nonlinear behaviour, low noise and high frequency capability. In addition, compact high performance digital circuits using Josephson junction switches coupled with picosecond-capable transmission lines out perform semiconductive designs. Excellent shielding from electromagnetic radiation may also be obtained due to the Meissner effect, while the metallic nature of LTSCs provides high levels of radiation resistance.

Overall, the performance of LTSC-based circuits is superior to that of semiconductor-based circuits. However, the necessity of operating LTSC electronics at 4K has limited their use due to the expense, bulk and inefficiency of helium refrigeration systems.

Recent discoveries of High Temperature Superconductors (HTSCs) operating at temperatures in excess of 77K, see Figure 4.1, are expected to revolutionize superconductive electronics provided that several materials problems are overcome. Processing problems coupled with material characteristics of HTSCs make the possibility of fabricating Josephson tunnel junctions in this technology extremely remote in the near term.^[10] However, this lack of an active element may be remedied, since semiconductors operated in the HTSC temperature regime exhibit superior

performance compared to room temperature devices. In particular, MOSFET and HEMT three-terminal semiconductor devices which are more versatile design elements than the two-terminal Josephson junction may be combined with HTSCs to provide gain.^[11] Therefore, the possibility of repeating the excellent performance of liquid helium cooled LTSCs with HTSCs operated at higher temperatures exists and if HTSCs exhibit comparable performance at or above 77K, widespread use of these devices in electronic systems is anticipated.

Figure 4.1. Highest Temperature Superconductor Versus Time^[81]

This chapter will focus on superconductive microwave circuits. Although LTSC technology is viewed as impractical for wide scale use in microwave systems, it has seen extensive development which should be directly applicable to HTSCs. Therefore, both LTSC and HTSC technology will be discussed. For each technology, their history, theory, processing, anticipated microwave performance and demonstrated results as well as their advantages and disadvantages will be discussed. Lastly, the experimental work on HTSC-based microwave circuits will be proposed.

4.2 LOW TEMPERATURE SUPERCONDUCTORS (LTSCs)

Following a brief history of LTSCs, it will be shown that superconductors are a distinct state of matter requiring their own theories. Properties of superconductors relevant to high speed electronics will be discussed. Thin-film deposition techniques used to form active and passive superconducting circuits as well as the performance achieved to date with LTSCs will be described. Finally, advantages and disadvantages of LTSC technology will be discussed.

4.2.1 History

Initially discovered in 1911 by Onnes,^[82] one of the first to liquefy helium, LTSC technology has been developing for over seven decades as summarized in Table 4.1. In the late '50s and early '60s, the development of the Bardeen-Cooper-Schrieffer (BCS) and Josephson theories led to extensive work on lead-based superconductors by both the U.S. military and IBM. Since lead is unstable at room temperature and cold flows, extensive reliability problems were encountered which caused both efforts to be scaled down. In the '70s and '80s, a shift from lead to niobium allowed several impressive circuits to be demonstrated, such as high speed digital logic for supercomputers and low-noise microwave receivers for radioastronomy. Today, the Japanese, working on their fifth-generation computer project, have taken the lead in digital superconductive electronics and recently demonstrated a 4-bit microprocessor running at 770 MHz^[83] while in the U.S., the SDI funded "Terahertz" project is concentrating on microwave/millimeterwave/infrared superconductive electronics.^[84] A significant milestone was achieved in 1987 when the Hypres 70 GHz sampling scope became the first commercial microwave product to use superconductive electronics.^[85]

DATE	DEVELOPMENT	INVESTIGATOR(S)
1911	Mercury Superconductors at 4K	Kammerleigh Onnes
1933	Meissner Effect	Meissner & Oschenfeld
1935	Energy Gap	Heintz & Fritz London
1954	A15-Niobium-Alloys ($T_C > 10K$)	Hulm & Hardy
1956	Cooper Pair	Leon Cooper
1957	BCS Theory	Bardeen, Cooper & Schrieffer
1961	Josephson Theory	Brian Josephson
1973	"High Temperature" Nb ₃ Ge ($T_C = 23K$)	
1987	PSP-1000 Digital Sampling Scope	Sadeg Faris

Table 4.1. Summary of LTSC Developments^[8,84,86]

4.2.2 Theory

The basic theory required to appreciate superconductivity will now be developed. Quantum mechanics will be used to develop the London^[87], BCS^[88] and Josephson^[89] theories which describe the operation of passive and active superconducting circuits. The Two-Fluid and London theories will explain the loss and dispersion behaviour of superconductors at high frequencies. BCS theory will introduce the concepts of Cooper pairs, critical current density, energy gap parameter and the energy-carrier density profile of a superconductor. This theory will be applied to single particle tunneling in SIS and NIS junctions. Lastly, Josephson's expressions will be used to explain the Josephson junction.^[90]

Phonon (lattice vibration) energies in normal metals are significantly smaller than the kinetic energies of the conduction electrons at low temperatures and the time for the current to decay after a forcing field is removed, the relaxation time, τ , is longer than the collision time. The conduction mechanism is therefore quite different

than at room temperatures and the resistance is proportional to the fifth power of temperature near absolute zero. Additionally, lattice irregularities due to imperfections or impurities cause energy changes in the system at absolute zero, creating conduction losses which are expressed by the residual resistivity.

In superconductors, there is an abrupt decline in the resistance to immeasurably small values at a temperature above absolute zero which is referred to as the critical temperature, T_c . This behaviour is believed due to electrons forming Cooper pairs which behave as super carriers that are free of energy taxing collisions. The equations in 4.1 describe the force, F , and current density, J , for a superconductor with no carrier collisions, where n electrons of charge e and mass m are travelling at velocity v . Combining, one obtains equation 4.2 which is referred to as the London equation. The current and electric field relationships are identical to that of a lossless inductor.

$$F = m \frac{dv}{dt} = -eE \quad ; \quad J = -nev \quad (4.1)$$

$$\mu_0 \lambda_L^2 \frac{dJ}{dt} = E \quad ; \quad \text{where} \quad \lambda_L = \sqrt{\frac{m}{ne^2 \mu_0}} \quad \text{is the London penetration depth} \quad (4.2)$$

Although superconductors exhibit negligible losses at DC (approximately 25 orders of magnitude lower than normal conductors), AC losses dependent on frequency and temperature may be significant. This is due to the existence of normal as well as super carriers for any temperature above absolute zero. The normal carriers are accelerated and decelerated by the changing fields, dissipating energy and causing losses. The Two-Fluid model shown in Figure 4.2 may be used to quantify these losses. Here, the total number of conduction particles, n , is divided into n_s superconductive carriers and n_n normal electrons corresponding to the lossless inductor and lossy resistor, respectively. As the frequency increases, the larger voltage drop across the

inductor will increase the power dissipated in the resistor. Hence, loss is predicted to scale with the square of frequency in superconductors. The magnitude of the AC losses is also determined by the proportion of superconducting to normal carriers, which varies as the fourth power of the ratio of operating temperature divided by the critical temperature, as shown in equation 4.3.^[88]

$$\frac{n_n}{n} = \left(\frac{T}{T_c}\right)^4, \quad \frac{n_s}{n} = 1 - \left(\frac{T}{T_c}\right)^4 \quad (4.3)$$

Figure 4.2. Two-Fluid Model^[91]

The predicted loss versus frequency for niobium ($T_c = 9.3\text{K}$) at various temperatures is shown in Figure 4.3 for both the Two-Fluid model (dotted) and the more accurate Mattis-Bardeen model (solid).^[92] Compared with room temperature circuits using conventional metal conductors, losses measured for niobium at 4K are four orders of magnitude lower at 10 GHz and two orders lower at 100 GHz. Near 1 THz, the losses increase rapidly as the material becomes normal since the electron energy exceeds the superconductor energy gap, as will be discussed later, and the Two-Fluid model becomes invalid. Therefore, to obtain acceptable performance, LTSCs are normally operated at temperatures below half to two-thirds of T_c and at frequencies well below 1 THz.^[91]

Figure 4.3. Niobium Loss Versus Frequency and Temperature^[91]

The magnetic behaviour of superconductors also differs from that of normal conductors. Using Maxwell's expressions listed in equation 4.4 for a material with no collisions such that it follows the London equation, equation 4.5 may be derived. Here, the penetration of an electromagnetic field into the material is effectively limited to the London penetration depth, λ_L , rather than the skin depth as in a normal metal.^[87] This results in the Meissner effect, whereby a superconductor electromagnetically shields its interior by excluding any initial internal magnetic field as it is cooled below its critical temperature, recall Figure 1.1. Here, the superconductor assumes a lower energy state by generating circulating surface currents that will cancel its internal magnetic field. This behaviour is unlike a perfect conductor which would maintain its internal magnetic flux, demonstrating that a superconductor is indeed a unique state of matter.^[93]

$$\nabla \times \mathbf{H} = \mathbf{J} \quad , \quad \nabla \times \mathbf{E} = -\mu_0 \frac{\partial \mathbf{H}}{\partial t} \quad (4.4)$$

$$\nabla^2 \mathbf{H} = -\frac{\mathbf{H}}{\lambda_L^2} \quad (4.5)$$

Since the London penetration depth for niobium is only 350Å, thin-film deposition techniques may be used to form low-loss superconductive transmission lines which have negligible dispersion.^[91,94] The low dispersion is caused by the London penetration depth being frequency independent and much smaller than the skin depth at microwave and millimeterwave frequencies. The dispersion of niobium transmission lines at a variety of temperatures are shown in Figure 4.4. Note that up to the frequency corresponding to the energy gap, the phase velocity is constant, indicating zero dispersion. Thin-films may also be deposited on enclosures to form excellent electromagnetic shields for use in severe EMI and EMP environments. Another property, useful in space and military applications, is the high tolerance of passive structures to ionizing radiation due to their metallic nature.

Figure 4.4. Niobium Phase Velocity Versus Frequency at Various Temperatures^[91]

To further explain the behaviour of LTSCs, the quantum mechanics based BCS theory is used.^[88] In a low energy phonon environment (at low temperature), a lower energy state can be realized if the carriers form Cooper pairs in which each pair contains particles with equal and opposite momentum. This maximizes the number of energy states available to the pair following a phonon collision, minimizing the system energy. Therefore, an electron-electron attractive force may exist over regions where the spatial energy structure is relatively constant, while any lattice imperfections or fields that change quickly with distance will limit the attractive interaction distance. This distance over which one carrier may influence another inside a superconductor is referred to as the coherence length, ξ ; it is of critical importance in the design of Josephson junctions as will be seen later.

Current is carried in a superconductor by the centre of mass of the pairs moving at some velocity. Since this velocity is the sum of the velocity vectors of the individual particles of the Cooper pair, as the velocity increases, the vectors will converge, the momentum of the particles will no longer be opposite and the number of states available following a phonon collision will be reduced. As the velocity is increased further, a point will be reached where appreciable energy changes occur during a collision and energy is dissipated. The current corresponding to this velocity limit is referred to as the critical current density, J_C . As the temperature is increased, the phonon energies rise and the critical current decreases. Once T_C is reached, the critical current goes to zero and the material becomes normal. There is also a limit on the magnetic field strength that a superconductor may shield itself from. This is called the critical magnetic field, H_C , it also decreases as the operating temperature rises. Therefore, the values of the three parameters: temperature, current density and magnetic field strength determine whether a material is superconductive. They are interrelated as illustrated in Figure 4.5 where 3D critical surfaces dividing the superconductive and normal regions are drawn for HTSCs, regions A and B, and LTSCs, regions C and D. Note that regions A and C are bulk material while regions B and D are thin-films.^[8]

Figure 4.5. T_c Versus J_c Versus H_c [8]

The magnitude of the energy drop due to pairing of carriers is proportional to the critical temperature of the superconductor and is represented by the energy gap parameter, Δ . Typical values for the energy gap in metal superconductors are one to three meV.^[91] The energy gap decreases at higher operating temperatures, similar to the critical current. This represents the diminishing energy advantage of the superconducting state compared with the normal state as phonon energies rise. Also, at high frequencies, the electron energy may exceed the energy gap, driving the material to the normal state, increasing the losses and dispersion as shown earlier.

The density of states in a superconductor at varying energy levels differs from that of semiconductors and normal metals. The density of states varies as the square root of energy in semiconductors and is approximately constant with energy in metals. In contrast, the density versus energy profile of a superconductor is zero below the energy gap, infinite at the energy gap and decays to the normal carrier density as the

energy increases, as shown in Figure 4.6. Although the energy gap parameter is similar to the energy gap between the valence and conduction bands of a semiconductor, the infinite density of states available at relatively low energies is unique.

Figure 4.6. Superconductor Energy State Density^[91]

The singularity in the energy-density characteristic may be exploited using a tunnel junction to produce the strongest known electronic nonlinearity. One type of tunnel junction is the superconductor-insulator-superconductor (SIS) which is formed by placing a thin insulator between two superconductors. Once the bias applied across the insulating barrier exceeds the energy gaps in each superconductor, single particle tunneling will occur, causing a sudden jump in the current through the junction as shown in Figure 4.7. This jump will be limited by the critical current of the junction. Similar behaviour occurs with a normal-insulator-superconductor (NIS) tunnel junction structure. However, as only one side of the junction possesses the infinite energy state density, the nonlinearity is weaker. The knee in the current-voltage characteristic of both devices occurs at a few millivolts due to the small

magnitude of the energy gap parameter in LTSCs. Therefore, this strong nonlinear characteristic, which exhibits a zero to infinite conductance transition at a bias corresponding to the energy gap, may be applied in a variety of sensitive microwave and millimeterwave circuits.^[91]

Figure 4.7. SIS Current-Voltage Characteristic

As the tunneling mechanism is not affected by a polarity reversal of the bias, the superconducting tunnel junction is a reciprocal device. A rectifier is not available in superconducting electronics technology.

In addition to the abrupt knee on the current-voltage characteristic of a tunnel junction, a sharp current spike at zero voltage is also observed in SIS junctions with very thin insulators, as shown in Figure 4.8. Although originally ignored by experimenters, in 1961 this "current with no applied voltage" was explained by Josephson^[89], who used quantum mechanics to develop the mechanism of Josephson tunneling and today, these devices are referred to as Josephson junctions. In summary, the theory states that in the absence of an applied bias, current may flow in an incomplete superconductive ring provided that a very thin insulator completes the ring. The energy of the system decreases if the quantum mechanical systems on either side of the insulator are coupled. To provide this coupling, current may flow through the

insulator creating a phase drop such that the two systems are coherent. If the phase of the two systems were initially equal on both sides of the insulator, the overall system would be coherent and no current would be required to flow. Similarly, if the phase difference was $\pi/4$, the two systems would be uncoupled and at an energy maximum, the maximum required current would flow through the insulator, causing a $\pi/4$ phase drop which would couple the systems and lower the energy. Therefore, the magnitude of this DC supercurrent depends on the initial phase across the insulator. This dependence is expressed by Josephson's first equation which states that the supercurrent is equal to $j_0 \sin \phi$ where ϕ is the phase angle across the insulator and j_0 is a parameter depending on the magnetic field strength and the geometry of the insulator.

Figure 4.8. Josephson Tunnel Junction Current-Voltage Characteristic^[95]

Note that j_0 is proportional to $n_s e^{-\alpha d}$ where n_s is the number of superconducting pairs, d is the length of the insulator and α is a decay parameter which is inversely proportional to the coherence length. Therefore, the Josephson junction insulator must be of dimension similar to the coherence length for useful currents to flow. Since LTSC coherence lengths are typically 40 nm, it is extremely difficult to fabricate repeatable devices due to the very thin insulator thickness.^[91]

The Josephson junction model consists of a current source, capacitor and conductance in parallel as shown in Figure 4.9. As both the current source and conductance are functions of the instantaneous electric and magnetic field strengths, extensive computations are required to predict the complex current-voltage characteristic of a Josephson junction.

Figure 4.9. Josephson Junction Equivalent Circuit^[91]

Since the voltage change from the superconducting $V = 0$ state to the normal $V = \Delta$ state is on the order of millivolts, Josephson junction digital switches exhibit power-delay products two orders of magnitude below that of the best semiconducting circuit elements such as MOSFETs and HEMTs operated at 77K.^[3] The strong nonlinearity exhibited by Josephson junctions at low voltage levels is also applied in low-noise microwave receiver circuits including detectors, mixers and parametric amplifiers.

Since an external magnetic field may modulate the critical current of a Josephson junction, extremely small magnetic field gradients may be detected by connecting a superconducting loop. This configuration is called a Superconducting QUantum Interference Device or SQUID and its sensitivity exceeds that of earlier magnetometers by two orders of magnitude.^[90]

Oscillators may also be formed using SQUIDs. Electrically, the difference between a Josephson junction and a SQUID is the addition of a superconducting loop which adds a shunt inductance to the three element Josephson junction model. This allows the

SQUID to resonate and, like conventional circuits, the resonant frequency depends on the magnitude of the inductance of the loop and the capacitance of the junction. Both microwave and millimeterwave oscillators have been constructed.

4.2.3 Processing

LTSC processing technology involves thin-film deposition and oxidation steps. The schematic, layout and cross section of a typical circuit is shown in Figure 4.10. The process is very similar to semiconductor integrated circuit fabrication and only differs with the addition of Josephson junctions, which are marked with 'X's on the schematic. In fact, a silicon wafer is commonly used as the substrate upon which the metal layers are deposited and oxidized due to its excellent surface finish, large area and low price. The most difficult processing step is the formation of repeatable pin-hole

Figure 4.10. Hypres LTSC Fabrication Process^[84]

free oxide layers required for the Josephson junction insulators, which must be only hundreds of atoms thick to obtain practical j_0 values. It is extremely important for the junctions to be repeatable for, unlike three-terminal devices, these two-terminal devices do not possess excess gain that may be sacrificed for processing tolerance. To this end, initial work on lead has been abandoned in favour of niobium which is more stable while niobium:nitride, with a higher T_C , is being developed.^[84]

4.2.4 Microwave Circuit Performance

Some examples of the performance achieved with LTSC electronics will now be described. Although superconducting digital circuits presently offer the highest performance available, only analog circuits which have been developed in the microwave and millimeterwave bands will be considered in this work.

As well as possessing low losses, superconducting transmission lines are also capable of transmitting picosecond duration pulses due to their low dispersion. Low characteristic impedance (1-5 Ω) parallel plate transmission lines have carried 1 psec pulses 10 mm with negligible distortion. Therefore, analog signal processors that exceed the performance of optical-based designs may be realized with superconductive transmission lines. Their time-bandwidth products of 1,000 above 10 GHz have allowed the construction of tapped delay lines forming pulse compressors/expanders, convolvers and extremely narrow band filters at microwave frequencies. In order to test circuits operating at 100 GHz, on-chip network analyzers using superconducting transmission lines have also been fabricated. A multi-tapped delay line with power detectors at each tap is used to determine the reflection coefficients at each port using the same principle as a slotted line VSWR meter with multiple probes.^[96]

The low loss of superconductors may also be used to construct extremely high Q resonators. For example, a 500 MHz stripline niobium resonator with a Q of

100,000 has been fabricated. Similarly, cavity resonators with short term stability superior to cesium/rubidium atomic clocks have been developed.^[9]

Superconductive technology is presently being developed for use in the front ends of low-noise receivers operating in the microwave/millimeterwave and far infrared bands. Components including antennas, filters, amplifiers, mixers and local oscillators operating at 10 GHz have been developed and the frequency range is presently being extended to 100 GHz. Target applications include inter-satellite millimeterwave communications and strategic reconnaissance radiometers.^[9] Some experimental results for various components are listed below.

Filter: The low loss removes the complexity constraint on conventional filters, allowing large numbers of sections to be used. For example, the close agreement between the predicted and measured results of a C-band chirp filter with a 2.6 GHz bandwidth and a 40 nsec delay time is shown in Figure 4.11.^[96]

Figure 4.11. Chirp Filter Amplitude Responses^[96]

Antenna: The resistive losses which normally dominate the radiated power in RF wire antennas and the typical 1 dB noise floor at 100 GHz set by metal antennas are eliminated by using superconductors.^[96]

Mixer: X-band superconducting-Schottky mixers with 0.1 dB noise figure and 7 dB conversion loss have been constructed. SIS mixers, which feature even higher performance, are presently being arrayed to increase their power handling capability from microwatts to milliwatts and to ease their matching requirements.^[96]

Amplifier: SQUID parametric amplifiers typically have 10 dB gains and noise figures of 0.09 dB and 0.14 dB at 8 and 94 GHz, respectively. They are presently being arrayed to ease matching and increase their saturation level.^[96]

Local Oscillator: Oscillators may incorporate superconducting high Q planar or cavity resonators to improve their phase noise performance. For example, a niobium resonator with a Q of over one million was used to stabilize a 1 GHz 0.5W oscillator. A 20 dB phase noise improvement compared to a conventional approach resulted in a spectral purity of -120 dBc/Hz at 1 kHz.^[94] In addition, VCOs with extremely large bandwidths using SQUIDs have been built at 8 and 100 GHz. They are also presently being arrayed to increase their output power.^[96]

Overall, impressive receiver performance has been demonstrated with active LTSC circuits. However, all active circuits suffer from low power saturation levels which make interfacing to conventional semiconducting electronics extremely difficult. Thus, unless these circuits can be arrayed to increase output power, LTSCs are unable to pass their information to conventional semiconducting electronics where considerable post processing of signals is presently accomplished.

4.3 HIGH TEMPERATURE SUPERCONDUCTORS (HTSCs)

This section will provide an overview of the recently discovered copper-oxide HTSCs.^c A discussion of their brief history will be followed by a description of the mechanism believed responsible for their extraordinary properties. These properties will be used to predict their expected microwave and millimeterwave performance. Both bulk and thin-film processing will be described and surface resistivity measurements will be summarized. Finally, the advantages and disadvantages of HTSCs will be discussed.

4.3.1 History

The superconductivity field was revolutionized by Bednorz and Müller in April of 1986 with the discovery of $\text{La}_{1.85}\text{Ba}_{0.15}\text{CuO}_4$ with a T_c of 35K.^[97] This was followed by the discovery of even higher T_c materials as shown in Figure 4.1. In February of 1987, Chu and Wu fabricated $\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$ (YBCO) with a T_c of 95K^[98], February of 1988 saw Maeda's $\text{Bi}_2\text{SrCa}_2\text{Cu}_2\text{O}_8$ (BSCCO) achieve a T_c of 110K^[99] and in March of 1988, Hermann and Sheng demonstrated a T_c of 125K with $\text{Tl}_2\text{Ba}_2\text{Ca}_2\text{Cu}_3\text{O}_{10}$ (TBCCO).^[100] Although materials with T_c s as high as 162K have been reported, they do not survive thermal cycling to room temperature.^[101] From a microwave applications perspective, the discovery of the thallium material is exciting since operating with liquid nitrogen pumped down to its 63K triple point will come close to achieving a normalized temperature ratio (T/T_c) of one-half. Thus, performance similar to that of niobium:nitride at 4K should be possible. With the considerable effort now underway on developing higher T_c material, further breakthroughs are anticipated.

^c Although copper-less HTSCs have also been developed, they will not be considered since they have much lower T_c s.

4.3.2 Theory

As HTSCs have broken the upper T_C bound of 30K predicted with BCS theory, a new theory of electron-electron interaction is presently being sought and this area is subject to considerable controversy.^[102] However, it is agreed that copper-oxide planes are responsible for the superconductivity, while other atoms in the compound establish the correct lattice structure and spacing. The YBCO lattice diagram, shown in Figure 4.12, indicates the position of these planes. It is orthorhombic with lattice constants: $a = 3.856\text{\AA}$, $b = 3.870\text{\AA}$ and $c = 11.666\text{\AA}$. From the chemical composition of the yttrium, bismuth and thallium compounds, it was felt that the larger the number of planes per unit cell, the higher the T_C . However, experimental work on rather unwieldy four- and five-plane compounds has not achieved higher T_C s.

Figure 4.12. YBaCuO Lattice Diagram^[103]

Similar lattice structures for BSCCO and TBCCO give all HTSC families anisotropic behaviour. Major differences in J_C , H_C , λ_L , ζ and Δ occur along the different axes.^[104] BSCCO is the most anisotropic, followed by YBCO and TBCCO. In YBCO, critical currents parallel to the planes are two orders of magnitude higher than in the orthogonal directions.

HTSCs have larger London penetration depths and energy gaps as well as reduced coherence lengths and energy state densities compared with LTSCs. Comparing c-axis oriented YBCO at 77K with Niobium at 4K, λ_L is four times larger at 1,400 to 2,000Å, Δ is ten times larger at 20 to 30 meV, ζ is one-tenth at 20 to 48Å and the density of carriers, which are holes, is one-tenth.^[94,104,105] The large ranges for these values result from the recent nature of this field.

The operation of HTSCs in liquid nitrogen, at a higher percentage of T_C , leads to a strong temperature dependence of many parameters. Of utmost importance is carrier density, which affects loss as shown earlier in equation 4.3. A more subtle effect is the temperature dependence of the London penetration depth, shown in equation 4.6^[106], which results in 77K values being approximately 50% higher than at absolute zero. As this dependence is strongest near T_C , bulk YBCO, BSCCO and TBCCO, at 81%, 70% and 62% of T_C , respectively, are more sensitive to temperature fluctuations than niobium in helium, at 45% of T_C . In thin-films, where the T_C s are somewhat lower, a significant effect is seen on the inductive component of the surface impedance, Z_S , shown in equation 4.7. The kinetic inductance is the result of energy being stored in the kinetic energy of carriers moving in phase quadrature to the applied electric field. Although only 0.1% of the geometric inductance in most planar transmission lines, kinetic inductance is directly proportional to the penetration depth. Thus, the resonant frequency in high Q microwave circuits such as narrow band filters is a strong function of temperature.

$$\lambda_L(T) = \frac{\lambda_{L0}}{\sqrt{1 - \left(\frac{T}{T_C}\right)^4}}, \quad \lambda_{L0} = \text{penetration depth at 0K} \quad (4.6)$$

$$Z_s = R_s + j\omega L_s; \quad R_s = 2\pi^2 f^2 \mu_0^2 \lambda_L \left(\frac{T}{T_C}\right)^4, \quad L_s = L_{\text{geometric}} + L_{\text{kinetic}}, \quad L_{\text{kinetic}} \propto \lambda_L \quad (4.7)$$

4.3.3 Processing

There has been considerable effort expended on HTSC processing. Both bulk and thin-film ceramic materials have been produced.^[8]

Bulk HTSCs are fabricated by mixing powders of the constituent elements, sintering and annealing in an oxygen atmosphere. An example of bulk material is the YBCO disk shown in the Meissner effect demonstration of Figure 1.1. Although possessing high T_C s, due to their high porosity and random grain orientation, J_C s of only 10^3 A/cm^2 have been achieved.^[8,107] Bulk material is also sensitive to moisture or other contaminants and is brittle after firing.

Although considerable work will be required to make flexible wires from HTSCs, their brittleness is of little concern if they are deposited as thin-films on rigid substrates. Yttrium, bismuth and thallium compounds have all been deposited as polycrystalline and single crystal thin-films with J_C s considerably higher than bulk material. For example, J_C s of 10^6 A/cm^2 demonstrated with YBCO at 77K should be adequate for microelectronic applications where 10^5 A/cm^2 is required.^[108] Even though λ_L is quadrupled in HTSCs, films $1 \mu\text{m}$ thick should be sufficient for high performance microwave structures. Thus a variety of thin-film deposition techniques, illustrated in Figure 4.13, including conventional electron-beam co-evaporation, DC and RF sputtering as well as unconventional techniques such as pulsed laser ablation and MOCVD/MBE, are presently being investigated.^[109] All methods require a long duration, high temperature anneal at 700 to 850°C in the presence of oxygen to obtain the correct crystal phase. When the film is deposited and annealed simultaneously in a high oxygen partial pressure, no post anneal is required and it is referred to as an in-

situ process. Since vacuum is maintained, no impurities are introduced, resulting in the highest quality films. Presently, laser ablation is the method of choice due to its speed and mechanical simplicity. For example, a sputtered film requiring 10 hours to deposit may be obtained in 10 minutes with laser ablation.^[110]

Figure 4.13. HTSC Deposition Techniques^[109]

Single crystal films must be grown on substrates which have the same perovskite crystal structure and thermal expansion coefficients as HTSCs. The lattice spacing of several substrates are compared with YBCO in Figure 4.14. FWHM refers to

the full width at half maximum of the X-ray rocking curve, which is a measure of crystal quality. As shown for several suppliers, the closer the lattice match, the higher the film quality. In addition, to aid current flow, the substrate must be cut so the copper-oxide planes will align tangential to the surface. The c-axis is perpendicular to the surface and such films are referred to as c-axis oriented. Early on, substrates from the synthetic diamond industry, including strontium titanate and yttrium stabilized zirconia, produced the highest T_C s and J_C s. However, these substrates have either a high dielectric constant or loss tangent which limits their use in microwave circuits. Thus, entirely new substrates with lower loss and dielectric constant, such as lanthanum gallate^[111] and lanthanum aluminate^[112], have been developed. Properties of several substrates at 77K are summarized in Table 4.2: the large ranges and omissions of some parameters are due to the recent development of these materials.

Figure 4.14. X-ray Rocking Curve Widths of YBCO Deposited on Several Substrates^[113]

Material	Relative Permittivity ϵ_r	Dielectric Loss Factor $\tan \delta$	Thermal Coefficient of Expansion $\Delta l/l(\text{ppm/K})$
Strontium Titanate (SrTiO_3)	1,900	0.06	11.1
Yttrium Stabilized Zirconia (ZrO_2)	25.4	0.0075	10.3
Magnesium Oxide (MgO)	9.6	0.00004	13.0
R-plane Sapphire ($\alpha\text{-Al}_2\text{O}_3$)	10	0.000000015	8.8
Lanthanum Gallate (LaGaO_3)	23.1	0.0001	?
Lanthanum Aluminate (LaAlO_3)	24.0	0.00003	~10
Lanthanum Strontium Aluminate (LaSrAlO_3)	17-27	0.00005	7.4
Neodymium Gallate (NdGaO_3)	20-25	0.001 (300K)	?
YBCO	----	----	10-12

Table 4.2. X-band Properties of HTSC Substrates at 77K^[20,111,113,114]

Additional problems presently limit most of these substrates in microwave applications. Magnesium oxide, being hygroscopic, may exhibit larger dielectric losses due to water absorption. Due to the closeness of the a and b lattice constants, many of these crystals, in addition to the superconductor itself, may exhibit twinning where the a and b crystal orientation is randomly interchanged.^[104] Twinning causes changes in dielectric constant and limits surface roughness. This has been a major problem in lanthanum gallate and lanthanum aluminate due to the processing temperatures spanning the twinning transition temperatures of 150°C and 450°C, respectively. Lanthanum strontium aluminate and neodymium gallate should be free of this problem due to their higher transition temperatures. Presently, lanthanum aluminate has been found to be adequate for microwave films in which conductor loss, rather than dielectric loss, limits performance. As the dielectric Q factor is proportional to the inverse of loss tangent, only lower loss substrates will allow higher Q factors to be achieved. For example, lanthanum aluminate will limit Q to

approximately 30,000. Thus, considerable effort on growing films on lower loss conventional MIC substrates such as sapphire is underway. Unfortunately, aluminum poisons the superconductor during the anneal, lowering its T_C , while thermal mismatches crack the films. Thus, several materials are being deposited as thin buffer layers between the superconductor and the sapphire to stop this migration and ease the thermal mismatch.^[113]

Due to the HTSC coherence length being equivalent to the thickness of ten atomic layers for c-axis oriented material and only an atomic distance for ab-axis oriented material as well as the high surface roughness of HTSC films, the fabrication of thin insulators required for Josephson tunnel junctions is a difficult problem which has yet to be solved. Most effort is underway in Japan where the construction of an active HTSC element is seen to have considerable commercial potential.^[115] For an overlay SIS junction, ab-axis oriented material is grown to allow the longer coherence length to be aligned vertically. Thus, different substrates and crystal cuts are used. Present work is concentrated on understanding the surfaces. Considerable work is required to achieve the smoothness required to form Josephson junctions, as the surfaces are easily damaged.

One promising area of HTSC processing is ohmic contact formation. Both gold and silver thin-film contacts annealed in oxygen exhibit resistivities below $10^{-9} \Omega\text{-cm}^2$.^[116] Note that this result is near the resolution limit of the equipment and $10^{-12} \Omega\text{-cm}^2$ resistivities are predicted.^[105] Hence, connecting to HTSCs with conventional wire bonding techniques is feasible.

Another area that has seen rapid progress is patterning of HTSCs. Methods successfully used include stencil masks, wet etching and ion milling. After wet etching, T_C s are normally lowered by a few degrees. Line widths of $25 \mu\text{m}$ are routinely achieved with $5 \mu\text{m}$ edge roughness which is limited by the grain-by-grain etching mechanism.^[117] An oxygen post anneal at roughly 500°C for 30 minutes has been

shown to rejuvenate the T_C and repair edge damage due to etching.^[118] For ion milling, T_C is not degraded and 1 μm features are possible.^[119]

4.3.4 Microwave Characterization

The microwave performance of HTSCs is expected to follow that of LTSCs with their values normalized to T_C . For example, thallium compounds operated at 77K should have losses similar to niobium at 4K as shown in Figure 4.3. However, the lower density of superconducting carriers should produce losses an order of magnitude higher, while the higher energy gap should extend the knee in the curve to 10 THz and allow devices to operate in the far infrared band; infrared detectors ten times more sensitive than Schottky devices are anticipated.^[120] Note that HTSCs operated at 4K should possess even higher performance due to the very low proportion of normal carriers present ($T/T_C < 0.04$).

Several methods, including waveguide, coaxial and planar resonators, have been used to determine the microwave surface resistivity of HTSCs. The waveguide cavity method utilizes a method similar to that used to determine the loss tangent of low-loss substrates. Here, a larger niobium cavity is cooled to 4K while the HTSC, mounted on a temperature controlled stage, is introduced inside. Q measurements are converted to surface resistivities.^[121] Although complete HTSC cavities have also been fabricated with bulk material, their poor surface quality has produced disappointing results.^[122] Another bulk material apparatus is the coaxial resonator, in which an HTSC inner conductor is placed inside a much larger copper outer conductor. Since the proportion of losses in each conductor varies with the square of the radius, the inner conductor losses dominate.^[123] Both stripline and microstrip patch resonators have also been fabricated.^[124]

Surface resistivity results as of early 1991 are summarized in Figure 4.15 for copper, niobium and YBCO at various temperatures over a wide frequency band. The low surface resistivity of YBCO is clearly demonstrated. At 10 GHz and 77K, the surface resistivity of patterned YBCO is under $0.2 \text{ m}\Omega$ which is superior to OFHC copper at $9 \text{ m}\Omega$. Theoretical $1/f^2$ plots are also shown and at lower frequencies, the conductive loss advantage is even more pronounced. However, for patterned circuits, saturation is reached due to the dielectric loss limit. Presently, the surface resistivity of unpatterned films are approximately twice that of the theoretical limit while patterned films are an order of magnitude higher.^[125] Considering that film loss has decreased by roughly an order of magnitude in the last two years, the theoretical limit should be approached shortly.

Figure 4.15. Copper and YBaCuO Surface Resistivities^[125]

4.3.5 Practical Considerations

In addition to allowing semiconductors and superconductors to coexist, the higher T_c of HTSCs provides other advantages. Assuming liquid nitrogen is used as an expendable cryogen, the 60:1 higher latent heat of vaporization and 30:1 cost reduction compared with liquid helium should lower cooling costs by over three orders of magnitude. For a closed loop mechanical refrigeration system, the 25:1 higher Carnot efficiency at 77K versus 4K and lower capital costs should result in operating costs being two orders of magnitude lower.^[12] Higher temperature closed loop and open loop systems should also be lighter, allowing superconductors to be used in mobile applications.

Another advantage is the higher energy gap, which should extend the operating frequency of superconductive electronics by an order of magnitude.^[126]

The primary disadvantage of HTSCs is the immaturity of the processing technology. However, although a Josephson junction will not be available soon, considerable effort on improving thin-films has led to rapid improvements in J_c and surface resistivity. Similarly, early films which were degraded by humid and vacuum environments have been superseded by films which are much more stable. Passivation layers are now available for additional protection, and hermetic sealing is a well developed packaging method that negates this problem.^[127]

For certain applications, the higher operating temperatures of HTSCs may be considered a disadvantage. Thermal noise is proportional to temperature, thus 77K operation will increase this component over nineteen times compared with 4K operation. This limits their use in extremely low noise and ultra low power digital applications.

Another disadvantage is the toxicity of some of the elements used in all HTSCs. Although little is known about the toxicity of HTSC compounds, they are expected to be more benign than their constituent elements. The most volatile and toxic element

used is thallium, a former rat poison. Thallium is a cumulative poison with a toxicity higher than barium as found in YBCO and lower than arsenic as found in GaAs.^[128] Its high vapour pressure, as shown in Figure 4.16, creates a significant danger during the high temperature processing steps if proper precautions are not taken. Therefore, a special facility for safely depositing thallium compounds is required. Safety precautions for handling HTSC circuits should also be followed.^[129]

Figure 4.16. Vapour Pressure of Thallium, Lead and Niobium Versus Temperature^[128]

Power handling is just beginning to be investigated. HTSC thin-films are presently able to handle milliwatt power levels rather than the watts that low temperature superconductors are capable of. Although non-linear distortion effects need further investigation, these films appear sufficient for insertion into low power electronics, as found in receiver front ends.

4.4 SUMMARY

LTSC technology possesses several advantages including high speed, low power consumption and low noise as well as intrinsic EMP and radiation hardness. Its main disadvantage is the 4K operating temperature, which is impractical for most applications. In addition, the supply of helium is limited which also hampers wide scale use of LTSCs. The low power saturation levels of LTSC active elements are also a disadvantage when interfacing with semiconductive electronics, while the higher power handling capability of passive structures are an advantage in high power systems. Thus, their application has been limited to a few fixed systems such as radioastronomy receivers, instrumentation and supercomputers.

Due to the higher operating temperature of HTSCs, the cooling problem is expected to be substantially overcome, providing the opportunity to obtain LTSC performance with liquid nitrogen cooled HTSCs in a wide range of applications, including mobile systems. Microwave and millimeterwave characterization of YBCO and TBCCO has demonstrated that surface resistivity several orders of magnitude superior to copper is possible at 77K. Fundamental properties of HTSCs should limit the use of Josephson tunnel junctions in the near term. However, the possibility of operating three-terminal active semiconductive devices in combination with passive HTSC structures in a microwave system should allow high performance active circuits to be realized. Near term applications should include resonators for filters and oscillators, shielding and RF antennas, where low loss is exploited, and analog signal processors and high speed interconnects, where both low loss and low dispersion are utilized.

Considering the characteristics of HTSCs and the previous experience with LTSCs, experiments to compare both normal and HTSC-based planar passive structures at microwave frequencies are required. As much work was already completed on characterizing unpatterned HTSC films, patterned planar passive circuits compatible with MIC/MMIC technology were chosen for investigation, as described in the next chapter.

CHAPTER 5 SUPERCONDUCTIVE MICROWAVE CIRCUITS: EXPERIMENTAL WORK

5.1 INTRODUCTION

Microwave and millimeterwave surface resistivities of HTSC thin-films over an order of magnitude lower than copper at 77K, described in Chapter 4, create the possibility of achieving high performance passive circuitry. Since little work on passive microwave HTSC structures using a planar circuit topology compatible with the dominant MIC processing technology had been performed at the beginning of this thesis, it was decided to explore this area. The use of MIC technology allows the resulting circuits to be widely applied. In particular, both HTSC and normal metal MICs with similar layouts were fabricated and measured. No active HTSC circuits have been attempted due to the considerable problems associated with Josephson junction fabrication.

In this chapter, HTSC thin-film deposition strategy, test apparatus, procedure and experimental results are discussed. Deposition and processing techniques employed by external organizations and CRC will be described. Details of a custom cryogenic vector measurement apparatus for microwave and millimeterwave characterization of thin-film circuits at temperatures below 77K are also included. Experiments comparing the Q of HTSC thin-film and conventional gold and copper conductors, passive MICs at cryogenic temperatures are described and the results analysed.

5.2 THIN-FILM PROCESSING

Although CRC has considerable expertise in thin-film MIC fabrication using normal metals, it has none in thin-film deposition of HTSC ceramics. In addition, HTSCs are composed of elements that include copper, barium and thallium which are toxic and contaminate vacuum deposition equipment, so dedicated processing equipment is required. Therefore, HTSC and copper thin-films were obtained from external sources. Considering that the HTSC family most suitable for microwave circuitry was not clear at the start of this work and the high risk associated with developing HTSC thin-films, five external sources, which processed all three major families, were utilized. Four Canadian sources included: the National Research Council (NRC) in Ottawa, Canadian Thin Films Ltd. (CTF) of Port Coquitlam, McMaster University in Hamilton, and the Defence Research Establishment - Valcartier (DREV) in Quebec. All were informal collaborations except for CTF, whose films were supplied under a contract awarded by Defence Research Establishment - Pacific (DREP) in Victoria and CRC. In addition, in the last year of this work, commercial suppliers became available and films were purchased from Superconductor Technologies Inc. (STI) of Santa Barbara. CRC processed some of the HTSC films and fabricated conventional gold baseline circuits.

At NRC, a multi-source electron beam evaporation system was initially used to deposit copper and YBCO films. The copper films were used as another normal metal baseline. Early YBCO results were disappointing due to stoichiometry inconsistencies, and a laser ablation system was developed which produces high quality single-sided films on sapphire and lanthanum aluminate substrates.

YBCO films were grown by pulsed laser deposition using an excimer laser with a wavelength of 248 nm. By initially depositing a cerium oxide (CeO_2) buffer layer on sapphire, NRC was one of the first to successfully deposit high quality YBCO on this low loss substrate. R-plane sapphire substrates are heated from behind with a

nicrome ribbon to a temperature of about 720°C and an oxygen pressure of 0.2 Torr is maintained during film growth. CeO₂ and YBCO ceramic disc targets are mounted on a rotatable copper disc as shown in Figure 5.1. Immediately upon completion of the CeO₂ buffer layer, the copper disc is rotated to bring the YBCO target into the laser beam path to grow the YBCO thin-film. Following deposition, the vacuum chamber pressure is raised to 500 Torr of pure oxygen and the substrate is allowed to cool to room temperature. Typically, a one minute deposition time grows a CeO₂ layer about 10 nm thick while a 20 to 35 minute deposition time grows YBCO films about 300 to 500 nm thick. The DC electrical characteristics are measured using photolithographically defined four-point probes. The resistance ratio from 295K to 100K is about 2.8 and T_c is 89±1 K. The critical currents at 77K are about 2×10^6 A/cm².^[110] Deposition on lanthanum aluminate is similar except for the omission of the buffer layer.

Figure 5.1. NRC Laser Ablation Deposition Apparatus^[110]

McMaster University utilized a laser ablation system similar to that described for NRC. Single-sided YBCO films were deposited on 0.3" square magnesium oxide substrates. T_c of an unpatterned film was measured to be 91K with a transition width of 3K as shown in Figure 5.2. Critical current was not measured.

Figure 5.2. Resistance vs Temperature of McMaster YBCO Thin-Film^[130]

CRC designs the masks, supplies substrates and performs patterning and contact formation on the NRC and McMaster films. Patterning moved from stainless steel stencil masks to a conventional photoresist/wet etch using ethylene-diamine-tetraacetic acid (EDTA) or hydrochloric acid (HCl) as etchants.^[128] A saturated solution of EDTA etches at 0.1 $\mu\text{m}/\text{min}$ while a 0.1% solution of HCl is quicker at 4 $\mu\text{m}/\text{min}$. T_c is lowered by approximately 4K after patterning. Although most structures only require 250 μm wide lines, features as small as 25 μm are possible. Contacts are obtained by

lifting off a 1 μm thick gold layer and a 0.03 μm thick titanium adhesion layer which are deposited by electron beam evaporation. Contact resistivity of a 0.050" square pad was measured to be 0.8 Ω . Although high, this is sufficient for connecting to a lightly coupled microwave resonator in a 50 Ω system.

In the contract with CTF, TBCCO thin-film microwave devices were produced for CRC.^[131] TBCCO was expected to provide higher microwave performance at 77K and higher tolerance to stoichiometry deviations and atmospheric contaminants, compared with YBCO. RF sputtering from a single composite target is used to deposit 1 to 2 μm thick films at a 0.8 to 0.9 $\mu\text{m/hr}$ deposition rate. This is followed by a post anneal in a thallium rich environment at temperatures up to 900°C. To obtain better morphology, initial work on the 2223 phase with a T_c of 125K was abandoned in favour of a 2212/2223 mixed phase compound with a T_c of 110K. The films are polycrystalline with some orientation leading to J_c s of under 50,000 A/cm^2 at 77K and an average T_c of 108K with a 10K transition width. Both magnesium oxide and lanthanum aluminate were used as substrates.^[128]

CTF patterned and made contact to these single-sided films using masks designed and supplied by CRC. Wet etching with 3% HCl is capable of defining 5 μm features. T_c drops from 2 to 10K after patterning. Figure 5.3 shows the resistance versus temperature characteristic of a film before and after patterning. Contact was made by bonding initially to small gold plated kovar shims epoxied to the input/output lines and later to 0.2 μm of DC sputtered gold. The gold contacts were found to have poor adhesion, making bonds extremely marginal. At CRC, the circuits were assembled into test fixtures for microwave characterization.

Figure 5.3. Resistance vs Temperature of CTF TBCCO Thin-Film^[128]

Although no microwave characterization of BSCCO thin-films has been reported, it was felt that this family should also be investigated. Therefore, a collaboration was arranged with DREV to magnetron sputter BSCCO on magnesium oxide and lanthanum aluminate. To date, no films have been obtained.

STI deposits TBCCO films by laser ablation followed by a high temperature anneal. The oxides are laser ablated onto polished lanthanum aluminate using an apparatus similar to that discussed for NRC. This amorphous film is heated to 830°C to 900°C under controlled thallium and oxygen pressures to form a film whose composition is mainly 2212 phase with good c-axis orientation and a T_c of 105K. Film thickness is $0.90 \pm 0.05 \mu\text{m}$, which is triple the typical thickness obtained with YBCO, and J_c s are at least 10^6 A/cm^2 at 77K. This process has been used to deposit double-sided films on 1

cm² square and, recently, 2" diameter substrates. Bondable contacts are formed by depositing and annealing 0.7μm thick gold, resulting in low resistivity, 10⁻⁵ Ω-cm², ohmic contacts. Surface resistivity at 10 GHz is 0.2 to 0.3 mΩ. The rapid improvement in the Q of a 2.3 GHz linear resonator used for process development is shown in Figure 5.4.^[132]

Figure 5.4. Loaded Q History at STI^[132]

Interfacing with STI is similar to accessing a commercial GaAs foundry. Computer files containing Autocad layouts are sent via modem to STI, who manufacture the masks and process the HTSC films. Unlike a GaAs foundry, films are processed quickly and our processed films were delivered within two weeks of mask submission. Once received, they were assembled into test fixtures for microwave characterization. Currently, the charge for a patterned double-sided 1 cm² film with gold contacts is around \$2K, while a 2" wafer is approximately \$15K.

5.3 MEASUREMENT APPARATUS AND PROCEDURE

Transmission measurements of simple distributed resonators allow direct determination of the quality of patterned films. Although the final goal is to develop superconductive microwave circuits operating successfully at 77K, in anticipation that processing problems may initially produce films with reduced T_c s, the measurement apparatus was developed to be capable of achieving lower temperatures. In addition to diagnosing poor films, the capability to sweep the temperature over a wider range allows the material to be more completely characterized.

A customized helium refrigerator which is capable of cooling a 0.25 Watt thermal load to temperatures below 10K, briefly discussed in Chapter 3, is used. This refrigerator, commonly called a cryocooler, is integrated with a Hewlett-Packard 8510B or a Wiltron 360A network analyzer to perform cryogenic microwave measurements on HTSC thin-films up to 26.5 GHz and 40 GHz, respectively. The temperature response of the cryocooler during a no-load cool-down is shown in Figure 5.5.

Figure 5.5. Cryocooler Temperature Versus Time

A simplified schematic for the cryocooler cooling circuit is shown in Figure 5.6. Its operation is similar to that of a common household refrigerator, where helium gas has replaced Freon as the working fluid in order to achieve lower temperatures. It follows the Gifford-McMahon cycle where valves A and B alternately open and close allowing high pressure helium gas into and out of the cold head. Upon entering, the gas expands, absorbing heat.^[12] The resulting low pressure gas is then returned to the water cooled compressor where it gives up its heat. To achieve extremely low temperatures, the entire cold head is evacuated using a vacuum pump to eliminate conduction and convection heat loss and a radiation shield, connected thermally to the first stage cold station which is capable of sinking two watts of heat at 77K, reduces radiation heating of the second stage cold station. In practice, the additional thermal mass of the radiation shield significantly prolongs the cool-down time. Once removed, temperatures sufficient to test the films were achieved in a workable time frame. During a measurement, a silicon diode thermometer and a resistance heater mounted on the second stage cold station maintain the temperature to within 0.5K of a set value. To speed the return to room temperature, dry nitrogen is introduced into the cold head to increase the heat transfer and the heater is biased.

Figure 5.6. Cryocooler Cooling Circuit Schematic

The method of forming microwave connections to the cooled circuit mounted on the split-block test fixture is similar to that used for the enhanced cryogenic vector characterization technique discussed in Section 3.4. Therefore, the apparatus shown earlier in Figure 3.13 is used. To achieve lower temperatures, special high thermal resistance semi-rigid coaxial cables were purchased. These included beryllium-copper and silver-plated stainless steel cables which have thermal resistances four and one-hundred times larger and attenuations similar to and ten times larger than copper cables, respectively.^[133] Originally, the cables leading from the circuit mounted on the second stage cold station to the room temperature vacuum ports were thermally anchored to the first stage cold station to reduce radiation loss. This was discontinued since the additional conduction loss through the cables significantly prolonged the cool-down time. For cooling the test fixture with the halves directly connected to perform a through calibration, a temperature of 50K was achieved after two hours when connected with conventional K-cables while 15K was achieved in one and a half hours using beryllium-copper cables. Although much higher than the no-load temperature of 8.5K, these temperatures were sufficient and the stainless steel cables were not required. Additional mass on the cold stage also lengthened the cool-down time. After lightening holes were machined in the test fixture and centre sections, the through standard could be cooled to 77K in one hour.

Distributed ring and linear resonators are commonly used to determine the Q of microwave circuits. Power may be capacitively or inductively coupled into the resonant structure. Transmission maxima will occur at integer multiples of the fundamental resonant frequency. Measured Q , Q_L , is simply the inverse of the 3 dB bandwidth and insertion loss must be measured to allow the unloaded Q , Q_0 , to be determined by equation 5.1. Q_0 is normally used since it is unaffected by resonator loading.

$$Q_0(f) = \frac{Q_L(f)}{1 - |S_{21}(f)|} \quad (5.1)$$

For the ring resonator shown in Figure 5.7, power is capacitively coupled through a gap of length s into the ring. When the centreline circumference is an integer number of wavelengths, it will resonate and transmission maxima will occur. At the frequency of interest, the ring should preferably be at least four wavelengths in circumference to remove any surface wave modes and to minimize field distortion due to the twisted conductor.^[19]

Test Transmission-Line Resonator:

Figure 5.7. Ring Resonator Topology^[19]

Half wavelength linear resonators are simply straight transmission lines of length $\lambda/2$ at the resonant frequency. A capacitively coupled version is shown in Figure 5.8. Although this type of resonator is easy to fabricate due to the mask simplicity, discontinuities at the ends radiate, lowering the Q .^[19]

Figure 5.8. $\lambda/2$ Straight Resonator Topology^[19]

As a ring resonator is essentially two linear resonators in parallel, if the material in the two halves is not identical, the effective lengths will differ and the fundamental mode will split into two resonant peaks. If the discontinuity is small, the two peaks will be closely spaced. In a linear resonator, a similar discontinuity will allow two higher frequency resonances to coexist. For example, a material defect located at one-third the length of the resonator creates two resonances at one and one-half and three times the fundamental, in addition to the fundamental. Thus the ring resonator allows film uniformity to be probed while the linear resonator reduces the possibility of multiple resonances appearing in the passband.

Ring resonators, straight resonators and hairpin resonators were used in the following experiments. A hairpin resonator is simply a $\lambda/2$ resonator folded back on itself.^[134] This allows the input/output lines to be on the same edge of the substrate for

use with the earlier liquid nitrogen immersion apparatus. Using the cryocooler apparatus, both ring and linear resonators are used to determine the Q of normal and superconductive thin-films over temperature, as described in the following section.

As only the transmission parameter, S_{21} , is required to evaluate Q_0 , the effects of the coaxial cables and test fixture are calibrated out using the standard "response" calibration method. The split-block test fixture provides the through calibration standard as well as the input/output lines to connect the device under test. A single through measurement of the two connected halves constitutes a "response" calibration. Thus, a series of calibrations for many temperatures and frequency ranges may be easily obtained. Test fixture construction is similar to that discussed earlier, while removable connections for the through and the device under test are made with ultrasonic bonded 0.0005" x 0.003" gold ribbons to ensure solid connections at cryogenic temperatures for measurements up to 40 GHz. With only the bonding tool heated, ultrasonic bonding ensures that the sensitive HTSC films are not degraded due to excessive heating. The split-block test fixture with a linear resonator clamped to the centre section is shown in Figure 5.9.

Figure 5.9. Split-Block Test Fixture with X-Band YBCO Linear Resonator Mounted

As the quality of the superconductive films improve and Q exceeds 1000, radiation loss becomes significant and a cover must be added to limit this loss. In this work, some of the better films were measured with a cover screwed onto the centre section of the test fixture above the resonator to reduce radiation losses. Cover height must be below that of a waveguide beyond cutoff, but not so low as to add conduction losses.

5.4 EXPERIMENTAL RESULTS

The comparison of passive planar microwave circuits using both normal metal and HTSC conductors was accomplished by measuring a variety of microstrip resonators. This was dependant on the use of high quality films which only became available in the past year. Inaccuracy of commercial CAD programs in simulating resonator coupling and the lack of double-sided films also hampered this work. Producing superconductive resonators with the correct coupling was empirically solved by fabricating masks incorporating a wide range of coupling gap lengths and widths. The double-sided film availability problem was initially solved by sandwiching two separate films together to form the guiding structure and microstrip ground plane in early experiments. Later, double-sided films became available from STI, allowing conventional assembly techniques to be employed.

Room temperature experiments were conducted to empirically establish the gaps required to lightly load normal metal resonators. For example, the room temperature broad band transmission response of a hairpin resonator with a 0.009" wide gold line deposited on 0.010" thick alumina with 0.004" coupling gaps, designed to have its first resonance at 3.60 GHz, is shown in Figure 5.10. This clearly shows the periodic behaviour of a distributed resonator in the frequency domain. Analysis of additional narrow band measurements yields a Q_0 of 60 at 3.63 GHz with an insertion loss of 40.5 dB. This information is used to design first pass HTSC resonators. In this

work, a series of HTSC films with different coupling gaps are measured and, by trial and error, the correct coupling is obtained. Insertion losses ranging from 10 to 40 dB at the frequency of interest allow Q_L to be close to Q_0 . The resonant frequency measured is assumed to be the same as the unloaded resonant frequency.

Figure 5.10. Transmission Response of a Gold Hairpin Resonator

As patterning using photolithography was unrefined at the start of this work, stencil masks in which film deposition occurs through a metal mask were developed first. Requiring precision machining, they are limited in resolution, difficult to fabricate and may contaminate the HTSC films during the high temperature deposition steps. A photo of a stencil mask fabricated for the NRC collaboration, a 0.003" thick stainless steel plate with a 0.010" wide by 0.250" long slot, is shown in Figure 5.11. On 0.010" thick sapphire, the resulting linear resonator has a fundamental resonance at 11.4 GHz. Coupling is adjusted by sawing the substrate the correct distance away from the ends of the deposited resonator. The four holes are for substrate alignment.

Figure 5.11. Photograph of $\lambda/2$ Resonator Stencil Mask

To overcome the limitations of stencil masks, conventional photolithography was successfully developed at an early stage of this work. Eleven masks incorporating various resonators and calibration standards were designed and laid out. CADD5 software running on a 386 personal computer was used for layout. Rubilith was cut on an Aristomat 8320 and hand peeled to form 20X masters which were photoreduced onto glass emulsion masks at a commercial photolithographic shop. As films were limited to 1 cm² substrates, or smaller, 1 cm² became the standard reticle for all masks. Since glass masks with a 2" to 3" square working area could be handled in our mask aligners, many different 1 cm² layouts, bracketing the coupling gap size, were included on each mask. Some of these masks will be described next.

One of the early masks developed for the CTF program is shown in Figure 5.12. Initially, it was felt that CPW structures would be the easiest to produce since only a single high quality film is required. Therefore, the upper half of this mask contains linear CPW resonators with a range of coupling gaps. In practice, contacts were difficult to fabricate and thus the grounding that this structure requires could not be

realized. Instead, the C-band ring resonators in the lower half were studied. The microstrip structure is obtained by inverting a second unpatterned HTSC film under the

Figure 5.12. Mask #90-3 for Processing at CTF

block test fixture with brass clamps and teflon gaskets. All other MICs using single-sided films are assembled in a similar way. Additional structures in the right column include four-point probes for J_c measurements and a line definition test pattern. Small triangles are alignment markers used to accurately place the mask over the substrate, while the smaller crosses are used to align the contact and HTSC layers. A ring resonator fabricated at CTF using this mask is shown in Figure 5.13.

Figure 5.13. Photograph of CTF TBCCO Ring Resonator

A development mask for processing NRC and McMaster films at CRC is shown in Figure 5.14. It is mainly comprised of linear resonators with a variety of coupling gaps and line widths of 0.010", 0.020" and 0.040" as well as their contact areas. In practice, 0.010" wide contacts could not be lifted off, so only 0.020" and 0.040" wide structures were successfully fabricated.

Figure 5.14. Mask #91-2 for NRC and McMaster Collaborations

A layout of a double-sided 1 cm^2 film fabricated at STI is shown in Figure 5.15. Due its high cost, as much circuitry as possible is included on the substrate, which was diced into four pieces at STI. In addition to the Ku-band linear resonators at the top and bottom, matching structures for a low-noise amplifier, discussed in the

following chapter, were also included. Linear resonators were chosen due to their reduced area requirement. 50Ω feed lines couple into low impedance resonators whose large width reduces the effect of substrate voids, film pin-holes and degraded edges. In addition to the gold ohmic contacts on the top surface, shown shaded, a gold deposition over the TBCCO ground plane allows the substrates to be attached to gold plated kovar carriers using low melting point, 150°C , indium/silver solder. The carriers are screwed onto the centre sections of the test fixture.

Figure 5.15. Mask #91-4 for Processing at STI

A more recent internal mask for both NRC films and in-house gold resonators is shown in Figure 5.16. The lower left area includes four linear resonators placed inside a 1" square to allow fabrication with CRC's standard MIC process on 1" X 1" X 0.010" alumina. To achieve the same 14 GHz resonant frequency as an STI TBCCO resonator grown on lanthanum aluminate, due to differences in the dielectric constant and substrate thickness, these gold resonators are 60% longer. The linear resonators on the right are for patterning NRC films and have a structure identical to the STI resonators except for wider input/output feed lines required to obtain 50 Ω impedances and for contact lift off.

Figure 5.16. Mask #91-6 for NRC Collaboration and Gold Baseline

Transmission responses of a one year old ring resonator processed at CTF and a first iteration linear resonator processed at STI are shown in Figure 5.17 and 5.18, respectively. For the CTF film, periodic transmission maxima appear when the temperature drops from room temperature to 58K. However, the multiple peaks at the fundamental indicate poor film uniformity. With a Q_0 of 70 at 4.9 GHz and 58K, this film is worse than a similar gold or copper structure at 77K. Surface resistivity and magneto-optic measurements performed at the University of British Columbia and the Royal Military College, respectively, confirmed this. At 2.98 GHz and 77K, the surface resistivity was $15\text{m}\Omega$, while the magneto-optic technique failed to image the film at 4K indicating a J_c under $10,000\text{ A/cm}^2$.^[128,135] The 13 GHz resonator processed at STI, with a 0.1" high cover, demonstrates an excellent Q_0 of 4,630 at 77K. These figures illustrate some of the tremendous range of Q_0 observed over the course of the experiments.

Figure 5.17. Response of CTF TBCCO Ring Resonator at 58K (upper) and 297K (lower)

Figure 5.18. Transmission Responses of a TBCCO Linear Resonator at 77K

Experimental results for a variety of HTSC resonators are summarized in Table 5.1. They are in chronological order to illustrate the rapid progress made. Normally, a group of films from each supplier was characterized over a few days and, for brevity, only the best result is included. For comparison, results for normal metal resonators are shown in Table 5.2. In this case, early work with copper showed performance similar to gold and was abandoned in favour of gold, the material of choice for most MICs, allowing circuits to be quickly processed at CRC.

HTSC and normal metal resonators are compared graphically in Figure 5.19 where Q_0 , at approximately 60K, is plotted on a log scale versus time. The Q_0 values have been normalized to 10 GHz by scaling the superconductor results with the square of frequency and the gold result with the square root of frequency. Data at 60K is chosen since early films required this temperature to function. In both cases, the input power is approximately -24 dBm.

Film Description Supplier/Material/ Substrate	Resonator Description	Q ₀ , T	f ₀ (GHz)	Date (m/d/y)
McMaster - YBCO - 0.020" MgO	0.300" X 0.009" linear - substrate sandwich	60, 60K	7.50	9/10/90
McMaster - YBCO - 0.020" MgO	0.200" dia. X 0.009" ring - substrate sandwich	110, 60K	7.50	9/27/90
CTF - TBCCO - 0.020" LaAlO	0.200" dia. X 0.020" ring - substrate sandwich	70, 58K	4.90	9/27/90
NRC - YBCO - 0.020" MgO	0.300" X 0.020" linear - substrate sandwich	285, 55K	7.78	1/14/91
NRC - YBCO - 0.010" Sapphire	0.394" X 0.020" linear - substrate sandwich	1460, 77K 2010, 52K	5.822 5.834	3/28/91
STI - TBCCO- 0.020" LaAlO with NRC - YBCO - 0.010" Sapphire ground plane	0.840" X 0.020" meander with 0.040" coupling gaps substrate sandwich	5020, 77K 5590, 50K	2.360 2.362	4/16/91
NRC - YBCO - 0.010" Sapphire	0.200" x 0.040" linear with 0.048" coupling gaps substrate sandwich	1070, 60K	10.290	5/21/91
NRC - YBCO - 0.020" LaAlO	0.200" x 0.020" linear with 0.052" coupling gaps substrate sandwich	1460, 80K 1630, 60K	7.013 7.028	5/22/91
STI - double sided TBCCO - 0.020" LaAlO	0.197" x 0.040" linear with 0.025" coupling gaps (second harmonic) no cover low cover - 0.1"	1220, 100K 1040, 77K 1870, 60K 1350, 100K 4630, 77K 4660, 60K	12.988 13.016 13.016 13.001 13.022 13.027	5/31/91
STI - double sided TBCCO - 0.020" LaAlO	0.185" x 0.040" linear with 0.035" coupling gaps (second harmonic) no cover low cover - 0.1" high cover - 0.25"	910, 100K 3260, 77K 2320, 60K 1800, 100K 6160, 77K 7590, 60K 850, 100K 10400, 77K 13830, 60K	13.685 13.707 13.713 13.698 13.711 13.717 13.673 13.707 13.713	8/14/91
NRC - YBCO - 0.010" Sapphire	0.200" x 0.040" linear with 0.030" coupling gaps substrate sandwich	950, 77K 1050, 60K	10.39 10.41	8/19/91

Table 5.1 Overview of HTSC Resonator Performance

Thin Film Description (Metal/Substrate)	Resonator Description	Q ₀ , Temperature	f ₀ (GHz)
Copper 1.5 μ m double-sided on 0.010" alumina	0.200" diameter X 0.009" wide ring with 0.004" coupling gaps	122, 297K	14.76
		299, 77K	14.60
Gold 2.5 μ m double-sided on 0.010" alumina	0.200" diameter X 0.009" wide ring with 0.004" coupling gaps	193, 297K	14.52
		283, 77K	14.65
Gold 2.5 μ m double-sided on 0.010" alumina	0.394" X 0.009" linear with 0.006" coupling gaps	113, 297K	11.42
		169, 77K	11.52
Gold 2.4 μ m double-sided on 0.010" alumina	0.293" X 0.040" linear with 0.006" coupling gaps	304, 297K	13.973
		413, 100K	14.095
		445, 77K	14.101
		475, 60K	14.103
	0.004" coupling gaps	224, 297K	13.953
		374, 100K	14.077
		421, 77K	14.082
		463, 60K	14.086

Table 5.2. Overview of Normal Metal Second Harmonic Resonator Results

Figure 5.19. Summary of the Improvement in HTSC Technology with Time

Overall, the considerable increase of HTSC Q_0 within a year is illustrated. Although McMaster and CTF films never became superior to gold, these early measurements allowed the procedure to be refined. NRC films with double the Q of gold were quickly developed but then stagnated at this level. During the summer of 1991, these were among the highest Q s for patterned YBCO films deposited on sapphire. STI films exhibit the highest Q_0 . Ku-band resonators have Q s over twenty-three times larger than similar gold structures at 77K.

Radiation loss has a significant effect on the Q of STI resonators at microwave frequencies, due to the substantially lower conduction loss component discussed in Chapter 2. In this case, much of the improvement in Q is from the proper choice of a cover, which reduces radiation loss, in addition to better film quality. Covers at both 0.1" and 0.25" above the substrate were evaluated; a cover height of 0.25", which had negligible effect on centre frequency, gave the highest Q . The addition of a 0.25" high cover increases Q_0 from 3,260 to 10,400 at 77K. This implies that cryogenic on-wafer probing of high Q structures will be limited, since implementing a cover to reduce radiation on-wafer appears difficult.

One must be cautious in extrapolating future progress from Figure 5.19. Although patterned films with an order of magnitude lower conduction loss are theoretically possible, substrate and radiation losses will become more important as film quality improves. On lanthanum aluminate, Q s approximately twice the present value may be the limit, while greater improvement should be possible on lower loss substrates.

Figure 5.20 shows the dependence of Q_0 on the input power level for a Ku-band STI resonator with 0.025" coupling gaps and a 0.1" high cover, resulting in 9 dB of insertion loss at 77K. Only a small improvement in Q is seen for power levels below -14 dBm, which is the highest power available from the Wiltron 360A test set, including cable losses. Note that the measurement at -74 dBm is near the noise floor and is of questionable accuracy. Similar insensitivity to power was observed in the X-band YBCO resonators from NRC. Higher power measurements of an L-band resonator at 77K with 20 dB insertion loss, carried out at STI, show that Q declines significantly as power level increases above -10 dBm and Q is halved at approximately 2 dBm. For a microstrip line, this degradation is due to the higher powers requiring current densities in excess of J_c to be supported in the edges of the top conductor.^[136] Thus one must operate these circuits below -10 dBm to achieve the highest Q and to avoid nonlinear effects.

Figure 5.20. TBCCO Ku-Band Resonator Performance versus Input Power

Q and centre frequency changes with temperature for an STI resonator with a 0.25" high cover and a 0.035" coupling gap and a gold resonator with a 0.006" coupling gap are shown in Figure 5.21 and 5.22, respectively. For the gold resonator, Q increases approximately 14% and resonant frequency shifts up 0.06% as the temperature drops from 100K to 60K while for the HTSC, the Q increases approximately fifteen times and the frequency shifts up 0.3% over the same temperature range. The higher temperature sensitivity of the superconductor Q may be explained from the two-fluid model as it is operating at a large percentage of T_C . Similarly, the larger temperature sensitivity of the superconductor resonant frequency is due to the kinetic inductance effect, which is appreciable when operating near T_C . Even though temperatures may be maintained to within a degree by active cooling, for narrow band superconductive filters, this high temperature sensitivity is not desirable.

Figure 5.21. Q_0 and f_0 of a TBCCO Linear Resonator versus Temperature

Figure 5.22. Q_0 and f_0 of a Gold Resonator versus Temperature

Insertion loss is difficult to accurately simulate due to the high dielectric constant of lanthanum aluminate. As the dielectric constant was in excess of 17.8, Supercompact could not be used. Fortunately, Touchstone was able to handle the dielectric. However, unlike Supercompact, Touchstone lacks a model for the asymmetric coupling gaps found in most of the later linear resonators. Thus, the results quoted include simulations assuming the coupling gap width is the size of the narrow feed lines, referred to as "narrow", and the size of the resonator width, referred to as "wide". Figure 5.23 shows the simulated and measured insertion losses for the gold on alumina and TBCCO on lanthanum aluminate Ku-band linear resonators. For a 10 dB insertion loss, the superconductor requires approximately five times larger coupling gap lengths due to the higher dielectric constant of the substrate and low conductor losses. Simulations using the two coupling gap width assumptions bracket the measurements for the normal resonator, as expected, while the superconductor measurements with both a

low cover and no cover are closer to the narrow simulation. The stronger temperature dependence of insertion loss for the superconductor is not shown. Insertion loss for the gold resonator with a 0.006" gap increases from 15 to 13 dB as the temperature drops from 297K to 60K while for the superconductor with a 0.025" gap, it increase from 15 to 11 dB from 100K to 60K. Larger changes are seen when covers are added above the superconductive resonators. Such high sensitivity to cover height makes accurate simulation difficult.

Figure 5.23. Insertion Loss versus Resonator Coupling Gap Length

It was also difficult to predict the resonant frequency of the superconductive resonators. For instance, the two iterations targeting a 14.0 GHz resonator at STI produced resonances at 13.0 GHz and 13.7 GHz. Measured and simulated centre frequencies for a selection of gold, YBCO and TBCCO circuits are summarized in Table 5.3. Overall dimensions were determined from optical micrometer measurements.

Linecalc is used to determine the effective dielectric constant of the linear resonators, and assuming they behave as perfect transmission lines with no fringing capacitance, the resonant frequency is calculated. Touchstone is again used to take the asymmetric coupling gaps into account using the earlier "wide" and "narrow" approximations. Linecalc gave the poorest agreement for the superconductors but good agreement for gold circuits. Again, the wide and narrow approximations bracket the gold measurements, however, the wide gap gives better agreement for the TBCCO (unlike insertion loss) and worse agreement for the YBCO.

Film Description	Resonator Description	Measured f_0 (GHz), Temperature	Linecalc f_0 (GHz)	Touchstone f_0 (GHz)
NRC - YBCO - 0.020" LaAlO	0.200" x 0.020" linear with 0.052" coupling gaps and 0.020" feed lines substrate sandwich	7.013, 80K 7.028, 60K	7.33	6.79
NRC - YBCO - 0.010" Sapphire	0.200" x 0.040" linear with 0.030" coupling gaps and 0.020" feed lines substrate sandwich	10.39, 77K 10.41, 60K	10.77	10.11 (wide) 10.38 (narrow)
STI - double sided TBCCO - 0.020" LaAlO	0.197" x 0.040" linear with 0.025" coupling gaps and 0.006" feed lines no cover	12.988, 100K 13.016, 77K 13.016, 60K	13.72	12.958 (wide) 13.507 (narrow)
Gold 2.5 μ m double-sided on 0.010" alumina	0.394" X 0.009" linear with 0.006" coupling gaps and 0.009" feed lines	11.42, 297K 11.52, 77K	11.62	11.50
Gold 2.4 μ m double-sided on 0.010" alumina	0.293" X 0.040" linear with 0.006" coupling gaps and 0.009" feed lines	13.973, 297K 14.095, 100K 14.101, 77K 14.103, 60K	14.19	13.918 (wide) 14.208 (narrow)

Table 5.3. Simulated and Measured Centre Frequency of Normal and HTSC Resonators

Although insertion loss and centre frequency are difficult to model, other behaviour is even more difficult to explain. For instance, the third harmonic of the STI resonators was not well supported, resulting in Q_s similar to normal metal resonator values. Although some degradation is expected due to frequency squared loss dependence,

the main effect is probably due to surface waves and radiation loss. Thus, thinner 0.010" substrates would be recommended for frequencies around 20 GHz. Similarly, no attempt was made to predict Q_0 , which was a strong function of cover height. Therefore, an empirical approach, utilizing many design iterations, is presently required to realize high Q HTSC circuits.

5.5 SUMMARY and CONTRIBUTIONS

HTSC thin-film processing strategy, a cryogenic test apparatus capable of microwave and millimeterwave transmission measurements and the results of measuring both HTSC and normal metal resonators were discussed in this chapter.

High quality YBCO and TBCCO thin-films were obtained from four external organizations in the past year. Laser ablation and RF sputter deposition techniques employed by these organizations, as well as the conventional photoresist/wet etch patterning and contact lift off processes developed at CRC to fabricate microstrip circuits, were described.

A custom cryogenic measurement apparatus for characterization of thin-film circuits at frequencies up to 40 GHz and at temperatures as low as 15K was developed. The Q_0 of HTSC, gold and copper thin-films, patterned into a variety of distributed ring and linear resonators, were determined through lengthy transmission measurements following a standard "response" calibration.

Producing superconductive resonators with the correct insertion loss was accomplished by fabricating masks incorporating a wide range of coupling gaps. Microstrip resonators were constructed by sandwiching two separate single-sided films together until double-sided films became available from STI. To reduce radiation losses in better films, covers were required.

Low power Q_0 of HTSC thin-film passive MICs at cryogenic temperatures showed rapid progress in the past year. At 10 GHz and 77K, Q_0 of superconductive resonators increased from 30 to 10,400. This latter value is over twenty times larger than similar gold structures and, in the future, Q_0 s approximately two times higher on lanthanum aluminate and ten times higher on lower loss substrates appear feasible.

At low power levels, below -10 dBm, Q_0 is relatively insensitive to power. However at intermediate levels, Q_0 may be severely degraded due to the critical current limitation and non-linear effects will occur. Thus, these high Q HTSC circuits are capable of functioning at power levels typically found in receiver front ends.

High temperature sensitivity of superconductor Q_0 , resonant frequency and insertion loss, were observed. These effects arise mainly from operating close to T_C and for future 77K circuitry, higher T_C materials would be of benefit.

Insertion loss and resonant frequency of superconductive resonators fabricated on lanthanum aluminate were difficult to accurately simulate with conventional microwave design tools. Considering the complex behaviour shown above 20 GHz, the high sensitivity of insertion loss with temperature and the significant effects of covers on Q_0 and insertion loss, an empirical design approach should be required for some time.

Overall, the major contribution of these measurements was to show that distributed circuits fabricated of HTSC materials are capable of significantly higher Q s compared with conventional metals at 77K. In addition, the characterization of patterned YBCO films deposited on sapphire was one of the first. Combined with the significant improvements in three-terminal semiconductive device performance demonstrated earlier at 77K, it was decided to design and fabricate hybrid semiconductive/superconductive MICs, as detailed in the next chapter.

CHAPTER 6 HYBRID SEMICONDUCTIVE/SUPERCONDUCTIVE MICROWAVE CIRCUIT DEVELOPMENT

6.1 INTRODUCTION

Considering that semiconductive and superconductive technologies excel in different areas, greater performance may be possible by combining them in hybrid semiconductive/superconductive microwave circuits. For example, superconductive tunnel junctions are difficult to fabricate with LTSC technology and appear a long way off with HTSC technology, while semiconductive junctions are routinely fabricated. Also, circuit Q s are limited to low values with normal MIC/MMIC metals, while extremely high values may be realized with superconductive thin-films. Hence, the attempt to integrate these technologies using MIC technology is described in this section. Specifically, semiconductive active devices are combined with HTSC passive structures at cryogenic temperatures.

Some of the most promising candidates for the hybrid semiconductive/superconductive approach include low phase noise oscillators, low-noise receivers, compact power amplifiers, millimeterwave phased array antennas and low loss switching matrices, as shown in Figure 6.1a), b), c), d) and e), respectively. For the oscillator shown in Figure 6.1a), performance superior to dielectric resonators using high Q superconductive planar structures combined with cooled low-noise semiconductive devices may be possible. Such a circuit would be especially useful in MMICs where bulky dielectric resonators are difficult to integrate. The possibility of reducing the losses of the antenna and input matching network while lowering the noise of the active semiconducting element in a low-noise receiver is shown in Figure 6.1b). A compact power amplifier, as shown in Figure 6.1c), should also benefit. Here, the lower loss of the superconductive power divider/combiner coupled with the

miniaturization of the power FET cells should reduce size and increase power added efficiency. Present millimeterwave phased array antennae are limited by the losses in the signal distribution networks. The use of a HTSC distribution network should allow larger arrays to be formed as shown in Figure 6.1d). Another area where losses are important is switching matrices as shown in Figure 6.1e). Again, HTSCs combined with the lower insertion loss of cooled HEMT switches should allow more complex switching to be achieved.

a) Oscillator

b) Low-Noise Receiver

Figure 6.1. Hybrid Semiconductive/Superconductive Possible Applications

Experience from the earlier cryogenic semiconductor and superconductor experiments has been applied to successfully demonstrate some of these hybrids.

Experiments to determine the performance offered by cooling three generations of three-terminal active semiconductive devices showed significant improvement at 77K. The Fujitsu FHR10X HEMT had the largest performance improvement at 77K, exhibiting a 54% higher cutoff frequency. Therefore, these HEMTs will be used where possible.

Passive superconductive microwave circuits demonstrated the excellent performance of commercially available HTSC thin-films. TBCCO resonators at 77K were similar in performance to dielectric resonators, demonstrating Ku-band Q_0 s over twenty times higher than gold. Therefore, these films were chosen for this work.

In the following sections, the design, fabrication and assembly of feedback oscillator and low-noise amplifier hybrid semiconductive/superconductive MICs are described. The feedback oscillator uses GaAs FET MMIC low-noise amplifiers for gain and a high Q TBCCO linear resonator for stabilization. For the first time, the entire oscillator is cooled. The low-noise amplifier is a subset of the receiver shown earlier and uses HTSC distributed stubs to match a FHR10X HEMT. No other paper to date has described a successful implementation of this type of circuit. Both MICs were designed to operate in the Ku satellite uplink band (14.0 to 14.5 GHz), since this frequency range is within the 1 to 20 GHz limit of the measurement apparatus and HTSC films possessing a surface resistivity significantly superior to copper are available.

6.2 SUPERCONDUCTIVELY-STABILIZED MMIC FEEDBACK OSCILLATOR

Recognizing that to fully exploit the high Q resonators requires they be lightly loaded, the feedback architecture shown in Figure 6.2 was chosen, rather than the single FET approach shown in Figure 6.1b). In summary, only signals in the passband of the filter are allowed to circulate through the loop, being amplified to overcome the losses of the other components and transmission lines. For the signal to be reinforced at resonance, the sum of the phase delay through the loop must be $2n\pi$ radians where n is an integer.^[137] Output power is obtained by coupling off a portion of this power. Provided the narrow band filter is lightly loaded, its Q will be close to Q_0 , resulting in the highest phase stability.

Figure 6.2. Feedback Oscillator Block Diagram

Recently, STI demonstrated a 10.2 GHz HTSC resonator stabilized feedback oscillator with performance superior to a dielectric resonator stabilized oscillator; phase noise was -126 dBc/Hz versus -120 dBc/Hz at 100kHz.^[138] However, only the resonator is cooled while the remaining circuitry operates at room temperature. In this work, the entire oscillator was cooled for the first time to see if additional performance improvements could be obtained.

As a rule of thumb in feedback oscillator design, the small-signal gain of the amplifier must exceed loop losses by at least 3 dB to ensure oscillation is sustained.^[137] In this design, TBCCO Ku-band linear resonators operating at their second resonance with responses similar to those shown earlier in Figure 5.18, are used. Therefore, approximately 10 to 20 dB of filter loss and 3 dB of coupling loss must be overcome.

Although L-, C-, X- and millimeterwave band MMIC amplifiers had been designed at CRC through several foundry accesses, none covered the 14 GHz resonant frequency selected here. Fortunately, Comsat labs had developed a two-stage Ku-band MMIC amplifier and supplied some sample die.^[139] They use quarter micron GaAs FETs with a 150 μm wide first stage driving a 300 μm wide second stage. Cascading two die provides 2.7 dB noise figure with 28.5 dB associated gain at room temperature over a band from 13.75 to 14.75 GHz.

A photograph of a two chip module fabricated for the high gain amplifier function is shown in Figure 6.3. The die are silver epoxied to 0.006" high posts machined on a 0.025" thick kovar carrier. These posts mate with ultrasonic drilled holes in a 0.010" alumina substrate which is attached to the carrier with indium/lead solder. The die are thermocompression bonded with 0.0007" gold wires to the interconnecting 50 Ω transmission line and bias pads. Bias is decoupled with 100 pF chip capacitors and 2K Ω chip resistors are in series with the gates for protection. These components are silver epoxied to the substrate and connected with ultrasonic ribbon bonds. Biasing the first stage for noise and the second for gain requires 75 mA at 3V, for a total power consumption of 225 mW per die.

Figure 6.3. Photograph of Four-Stage Ku-band MMIC Amplifier Module

A rat race coupler splits the power between the output port and the feedback loop. This is a three branch transmission line directional coupler where 50Ω transmission lines are placed at $\lambda/4$ multiples around a 70.7Ω ring transmission line, producing 3 dB coupling. Unlike a two branch coupler, the rat race strongly attenuates frequencies at half the passband frequency which is important as a second harmonic linear resonator is used in the feedback loop. Supercompact simulated transmission responses into the loop and the output port, labelled "feedback" and "thru", respectively, are shown in Figure 6.4. At 14 GHz, the feedback path has 3.4 dB of loss while the output is attenuated 3.6 dB. Of utmost importance is the 13.8 dB notch in the feedback path at the 7 GHz fundamental, ensuring that loop gain will only be sufficient to support oscillation at the second harmonic. This circuit was also fabricated on 0.010" alumina which was indium/lead soldered to a 0.025" thick kovar carrier. The unused port is terminated with a laser trimmed 50Ω chip resistor.

Figure 6.4. Rat Race Coupler Transmission Responses

The gains and phases of the components at 14 GHz are indicated on the block diagram of Figure 6.5. The amplifier and resonator values are measured results, while the coupler and phase adjustment line values are Supercompact simulations. With four stages of amplification, gain appears sufficient to overcome the loop loss. To obtain the correct phase drop around the loop at resonance, assuming the small-signal phase response as an approximation, the phase adjustment line was sawn from a 1" square substrate to have a total length of 0.622". This was also fabricated on 0.010" alumina which was indium/lead soldered to a 0.025" thick kovar carrier.

Figure 6.5. Block Diagram of Superconductively-Stabilized Oscillator

The masks used to construct the rat race coupler, phase adjustment interconnect line and two-chip MMIC amplifier module are shown in Figure 6.6a), b) and c), respectively. Fine lines are sawing guides. These three alumina substrates and the TBCCO resonator, soldered to kovar carriers, were attached to a gold plated brass fixture with #00-96 screws, forming the oscillator shown in Figure 6.7. The resonator (not visible) is covered by a 0.10" high gold plated brass cover to minimize

radiation loss. A K-connector sparkplug launcher is used for RF output while five DC feedthroughs, connected to phosphur-bronze wires, bias the MMIC amplifiers. Ceramic decoupling capacitors supplement the capacitance of all feedthroughs. Assembly was complicated by the need to thermocompression bond the MMICs, which required heating the entire fixture. However, by ultrasonic bonding the resonator into the circuit last, it was not exposed to excessive heating.

Figure 6.6. Oscillator Mask Set

Figure 6.7. Photograph of Superconductively-Stabilized Oscillator

The oscillator was fastened using machine screws to the second stage cold head of the cryocooler for testing. Output was fed through a K-cable to an HP8569A spectrum analyser. Once oscillating, the amplifiers self-biased themselves. Approximately 80 mA of drain current at 2.5V was found to produce the cleanest spectra. The narrow band output spectrum at 40K is shown in Figure 6.8. Due to the lower resonant frequency of the linear resonators, the oscillations are centred at 13 rather than 14 GHz. As only a single coaxial K-cable connected the oscillator, thermal leakage was considerably reduced, allowing measurements to be made down to 14K. The oscillator locked up to the resonator at temperatures below 94K.

Figure 6.8. Narrow Band Oscillator Spectrum at 40K

The raw data from spectrum analyser measurements has been corrected to obtain SSB phase noise by using equation 6.1; the factor of 1.2 comes from the non-ideal

nature of the filters and 2.5 dB comes from log amplifier errors at low power levels.^[140] Noise power levels over a range of temperatures at 100 KHz and 1 MHz from the carrier are shown in Figure 6.9. At 100 kHz offset, a phase noise minimum occurs around 40K. Similar behaviour does not occur at 1 MHz. The minimum may be due to the higher Q in the TBCCO resonator being countered by degradation in the FET $1/f$ noise as dopants freeze out. Although close-in performance is similar to an HP8530 sweeper, it is approximately 25 dB worse than a dielectric resonator oscillator at room temperature. For example, the best phase noise, at 40K, was -95 dBc/Hz at 100 kHz from the 13 GHz carrier.

$$\text{SSB Phase Noise (dBc/Hz)} = \text{Raw Noise (dBc)} - 10 \log(\text{resolution bandwidth} \times 1.2) + 2.5 \quad (6.1)$$

Figure 6.9. SSB Oscillator Phase Noise versus Temperature

Improved phase noise performance should be possible by increasing the Q of the resonator. Using a 0.25" cover instead of the 0.1" cover or by reducing the power level at the resonator should increase its Q significantly. However, the major cause of the degradation in phase noise can be seen in the wide band spectrum shown in Figure 6.10. Spurious oscillations, appearing at many frequencies, are evident. By mixing with the fundamental, these secondary oscillations are creating additional phase noise, limiting spectral purity.

Figure 6.10. Wide Band Oscillator Spectrum

These secondary oscillations appear to be caused by a reduction in amplifier stability as it is cooled. S-parameter measurements of the MMIC amplifier module at 77K, shown in Figure 6.11, reveal input reflection coefficients greater than one from 5 to 11 GHz with up to 27 dB of associated gain. Considering that the reflection coefficients of the resonator at frequencies other than its 7 and 14 GHz resonances are near unity, it is highly possible that these reflections are building up to create secondary oscillations. Once created, mixing inside the saturated amplifier probably forms the intermodulation products evident in Figure 6.10.

Figure 6.11. S-Parameters of MMIC Amplifier Module at 77K

In an attempt to remove the secondary oscillations, Eccosorb MFS-117^[141] blocks were placed on the microstrip lines to attenuate the reflections and gain of the amplifier, however, these oscillations could not be removed without quenching the fundamental. This illustrates the difficulty of varying the gain in the loop for this "all cooled" approach. Similarly, phase adjustments were difficult to make; a new phase adjustment substrate would have to be sawn apart and attached.

In summary, a cooled MMIC feedback oscillator stabilized by a HTSC linear resonator has been successfully demonstrated for the first time. However, secondary oscillations are presently limiting its phase noise performance. Pending the availability of more stable MMIC amplifiers, a more frequency selective attenuator should be used to improve the phase noise, rather than using broadband Eccosorb blocks. Stabilization networks discussed for the low-noise amplifier in the next section may be appropriate.

6.3 SUPERCONDUCTIVELY-MATCHED LOW-NOISE HEMT AMPLIFIER

As one of the first hybrid semiconductive/superconductive low-noise amplifiers to be attempted anywhere, the design was kept as simple as possible and proven components were used in its assembly. Distributed matching structures were made by patterning TBCCO films grown on lanthanum aluminate substrates, processed at STI, while the FHR10X HEMT was chosen as the active device.

The HEMT was matched for gain using open circuit stubs shunting the input and output 50Ω transmission lines. As Supercompact could not handle the high dielectric constant of the substrate, Touchstone was used for design simulation. Measured 77K S-parameters, shown earlier in Figure 3.19, were used. They are referenced in the S-parameter data file "FUJ77.OUT" shown in the amplifier Touchstone

listing in Appendix III. A schematic of the resulting amplifier is shown in Figure 6.12; the mask layout was shown earlier in the middle of Figure 5.15. Bias is fed through the middle of high impedance/low impedance quarterwave transmission line networks on the gate and drain. These networks are positioned opposite the open shunt stubs to cancel their effects at 14 GHz. In addition, a 50Ω resistor in series with a 100 pF capacitor are added in the middle of the bias networks to help stabilize the amplifier at low frequencies. On the gate, bias is also passed through a $2K\Omega$ resistor for protection.

Figure 6.12. Schematic of Low-Noise Amplifier

Although complex multi-stub matching would more fully exploit the lower loss offered by HTSC films, they were not used due to space constraints and the basic design principle of simplicity. Following the same reasoning, DC blocking capacitors on the input and output were omitted.

A photograph of the assembled amplifier is shown in Figure 6.13. The TBCCO thin-films, on lanthanum aluminate substrates, are attached to a 0.015" thick

gold plated kovar carrier with low temperature indium/silver solder. 50Ω and $2K\Omega$ laser trimmed chip resistors and 100 pF multilayer chip capacitors are attached to the substrate with low temperature Epo-Tek H20E silver epoxy.^[142] A 0.020" high ridge with a depression 0.004" deep and 0.020" square was machined on the carrier, allowing the HEMT to be epoxied down and its sources grounded. The HEMT is thermocompression wire bonded into the circuit while ultrasonic bonded 0.0005" x 0.003" ribbons connect the other components, input/output transmission lines and DC bias lines to the circuit.

Figure 6.13. Photograph of Low-Noise Amplifier

S-parameters of the amplifier were obtained using the enhanced cryogenic measurement technique described in Chapter 3. Figure 6.14 shows the amplifier, mounted on a carrier, fastened with #00-96 machine screws to the centre section of a split-block test fixture and biased through two filtercons. To obtain noise figure, the earlier cryocooler apparatus was slightly modified. Instead of connecting to the network analyser, an HP346C noise source was connected to the input SMA vacuum feedthrough on the cryocooler shroud, while the output feedthrough was connected to a 10 to 18 GHz circulator, 1 to 26 GHz mixer and HP8970B noise figure meter, as shown in Figure 6.15. A through, formed by ribbon bonding the two halves of the test fixture together, was measured to calibrate out the losses of the input cables and mixer noise figure. The Ku-band repeatability of reconnecting the through was ± 0.1 dB in noise figure and ± 0.02 dB in gain as shown in Figure 6.16. The noise figure dropouts are caused by the mixer and are either narrow band or above the frequency of interest. After calibration, the test fixture was broken apart and the centre section was inserted.

Figure 6.14. Photograph of Low-Noise Amplifier Mounted on Test Fixture

Figure 6.15. Noise Figure Apparatus

Figure 6.16. Noise and Gain Repeatability of a Through Standard

Magnitude plots of the four S-parameters at both room temperature (active markers) and 77K are shown in Figure 6.17. At 77K, bias is the nominal design current of 5 mA with 2V on the drain. At room temperature, the high resistance of the TBCCO bias lines prevents any drain current from flowing at this drain voltage. This demonstrates the added difficulty of testing this type of circuit. In effect, it must be cooled for over an hour before any determination of its condition may be made. The small input and output reflections at room temperature illustrate that the TBCCO matching structures are lossy in the normal state. At 77K, the input and output return losses show a match around 14 GHz, with a corresponding gain of 15.5 dB.

Figure 6.17. Amplifier Magnitude Responses at 77K ($I_{CH} = 5$ mA) and 300K

A comparison of measured and modelled gain and return loss is shown in Figure 6.18. Measured gain is approximately 5 dB higher than modelled, while a second peak around 6 GHz is more pronounced in the measured results, hinting at a possible stability problem. On the input, the measured match occurs at the simulated frequency. On the output, two notches straddle the single design frequency notch. Both measured return losses are worse than the over 12 dB predicted, with values in the 3 to 8 dB range. Overall, it is a reasonable first iteration fit considering the poor accuracy of the modelling software demonstrated in Chapter 5.

a) Transmission Gain

b) Input and Output Return Loss

Figure 6.18. Measured and Modelled Amplifier Responses ($T=77K$, $I_{CH}=5$ mA)

Uncorrected noise figure over a 10 to 16 GHz band is shown in Figure 6.19 for the nominal bias condition. A noise minimum of 1.7 dB occurs around 13.2 GHz. However, this value has not been corrected for the input losses of the K-cables and test fixture which directly contribute to noise figure. By connecting short and open centre section standards, following a short/open/load one-port calibration at the vacuum feedthrough, the 14 GHz input loss was measured to be 1.4 dB at 77K. Thus the corrected noise figure at the 14 GHz design frequency is near 0.4 dB (29K noise temperature). Compared with Figure 2.20, performance is between that of conventional FET and HEMT MIC amplifiers operating at 13K.

Figure 6.19. Uncorrected Amplifier Noise Figure ($T=77K$, $I_{CH}=5\text{ mA}$)

To investigate the best noise figure bias condition, gain and noise figure measurements at drain currents from 0.5 to 10 mA were performed and the results are plotted in Figure 6.20. A noise figure minimum occurs at around 3.5 mA, rather than the recommended room temperature value of 5 mA. One unexpected and interesting result is the extremely high level of gain shown for very minute bias levels. For example, to obtain 10.7 dB of gain with only 0.5 mA flowing is extraordinary, demonstrating extremely low power consumption provided the higher noise figure of 1 dB is tolerable. Hence, a more complex amplifier with many intermediate power gain stages should require considerably less power if a hybrid approach is followed.

Figure 6.20. Gain and Corrected Noise Figure versus Amplifier Drain Current at 77K

Overall, a low-noise HEMT amplifier using HTSC distributed matching was demonstrated for the first time. Although its present noise figure is similar to a conventional cooled MIC, it should be remembered that this is the first reported result and improvements are expected using this new semiconductive/superconductive topology. Moderate gain is achievable with extremely low drain current.

6.4 SUMMARY and CONTRIBUTIONS

Cryogenic semiconductor and HTSC technologies were successfully applied in the development of a superconductively-stabilized MMIC feedback oscillator and a superconductively-matched low-noise HEMT amplifier. The oscillator is the first reported to combine MMIC and HTSC components in an assembly which was completely cooled, while the low-noise amplifier is the first to integrate HEMT and HTSC elements.

Oscillator phase noise is approximately 25 dB worse than a room temperature dielectric resonator oscillator, due to spurious oscillations. This degradation was mainly due to the unstable MMIC amplifier. Cooling the entire oscillator hampered attempts to adjust the gain and phase through the loop, making it difficult to verify that it was configured for optimum performance.

The low-noise amplifier featured an excellent noise figure and high gain. Lower noise figure is anticipated by matching for noise rather than gain. Transmission and return loss measurements deviated from simulations, showing that considerable work remains to be done before a successful first iteration circuit is possible.

The major contribution resulting from the successful realization of these hybrid semiconductive/superconductive circuits was to clearly demonstrate that it is possible to integrate these technologies. Both circuits were inconclusive in determining the performance advantage of this approach and future experiments are needed to confirm that combining semiconductive and superconductive microwave components will result in the highest level of performance. This work was recently submitted to the 1992 Microwave Theory and Techniques Symposium.

of/de

3

A resolution test chart featuring various patterns of horizontal and vertical lines of different thicknesses. Numerical values are placed next to the patterns, indicating resolution levels. The values include 1.0, 1.1, 1.25, 1.4, 1.6, 1.8, 2.0, 2.2, 2.5, 2.8, 3.2, 3.6, 4.0, 4.5, 5.0, 5.6, 6.3, 7.1, 8.0, 9.0, and 10.0. The chart is used to measure the resolving power of imaging systems.

PIONEER IN METHYLENE BLUE TESTING SINCE 1974

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CHAPTER 7 CONCLUSIONS and RECOMMENDATIONS

7.1 SUMMARY

Recognizing that the present strategy of relying solely on semiconductor processing advances to achieve higher levels of performance is limited, other technological advances were exploited. In particular, the potential for microwave performance advances by operating conventional semiconductive circuits and the recently discovered HTSC materials at cryogenic temperatures was investigated in this thesis. These areas are complementary, as the development of an active HTSC device appears distant and normal metals used in semiconductive passive structures are lossy, while active semiconductive devices are readily available and passive superconductive structures feature the highest Qs.

The potential of semiconductive microwave circuit operation at cryogenic temperatures was discussed first. As both MIC and MMIC technology are the dominant fabrication techniques, they were described and their limitations noted. How some of these performance limitations may be extended by operating at cryogenic temperatures was discussed. It was predicted that the Q of planar transmission line structures, as found on MICs and MMICs, should improve at low temperatures due to reduced conductor and substrate losses. Also, the frequency of operation and noise performance of active devices are expected to improve at cryogenic temperatures due to the lower resistivity and higher transconductances of MESFET and HEMT devices. Higher thermal conductivities of pure materials, GaAs included, coupled with the greater effectiveness of liquid cooling at 77K should also allow higher power density and/or reliability to be achieved. In addition, the constant operating temperature associated with a liquid-to-gas phase change or controlled cryocooler should provide stable circuit characteristics, irrespective of changes in the external ambient temperature. Considering the

significance of each area expected to improve from low temperature operation and the work previously performed, frequency response of three-terminal active semiconductive devices and quality factor of passive metal transmission lines were concentrated on in experiments.

In order to verify the predicted performance advantages of semiconductive microwave circuits at cryogenic temperatures, a novel measurement technique in which a TRL calibration was performed in-situ was developed. Both a liquid nitrogen immersion and a cryocooler-based apparatus were developed. Although the procedure was slow, fully corrected S-parameters of MIC and MMIC devices could be obtained in real time at low temperatures for the first time. After verifying the measurement technique, experiments determined the performance improvement from cooling active semiconductive devices to 77K. By using the enhanced measurement technique, changes with temperature were observed in the small-signal equivalent circuit elements of three generations of three-terminal active semiconductive devices. The Fujitsu FHR10X had the largest performance improvement at 77K, exhibiting a 54% higher cutoff frequency.

The second area studied was superconductive microwave circuits. Superconductor theory and previous experimental results were described and the 4K operating temperature which limits the application of LTSCs was identified. This limitation is largely overcome by using the recently discovered HTSCs at 77K. Using theory originally developed for LTSCs, the expected microwave performance of HTSCs was predicted to be superior to normal metals. Measurements, carried out elsewhere, demonstrated microwave/millimeterwave surface resistivities of HTSCs superior to copper at 77K. Fundamental problems limiting the fabrication of HTSC Josephson junctions were identified, reinforcing the requirement to utilize semiconductive active devices for gain functions.

Experiments concentrated on planar HTSC circuit elements compatible with MIC and MMIC technology. In particular, passive HTSC distributed microstrip resonators were compared with similar normal metal structures to verify that the lower surface resistivities may produce higher Q patterned circuits. Yttrium and thallium HTSC thin-films were obtained from external organizations. Patterning, contact fabrication and resonator integration undertaken at CRC was described. A cryocooler-based apparatus capable of characterizing thin-film circuits at frequencies up to 40 GHz and at temperatures as low as 15K was detailed. The Q_0 of films patterned into a variety of distributed ring and linear resonators was determined through lengthy transmission measurements following a standard "response" calibration. Commercial CAD software was found to be inadequate in designing low loss HTSC circuits on high dielectric constant substrates and the fabrication of eleven masks to empirically obtain resonators with the correct resonant frequency and coupling characteristics was required. In the past year, measurements of these superconductive resonators showed an increase in Q_0 from 30 to 10,400, at 10 GHz and 77K; the latter result is over twenty times larger than that of similar gold structures. Overall, these measurements demonstrate that distributed circuits fabricated of HTSC materials are capable of significantly higher Qs than conventional metals at 77K for power levels typically found in receiver front ends.

These results, combined with the significant improvements in three-terminal active semiconductive device performance demonstrated earlier at 77K, led to the design and fabrication of hybrid semiconductive/superconductive Ku-band MICs. The two technologies were successfully combined for the first time in the demonstration of a completely cooled superconductively-stabilized MMIC feedback oscillator and a superconductively-matched low-noise HEMT amplifier.

7.2 CONTRIBUTIONS

The major contribution of this work was the development of a cryogenic microwave characterization apparatus and technique.[68,73,79] By combining the TRL calibration technique with cooled apparatus, extremely accurate measurements are obtained. This technique has been applied by Japanese and American researchers in the field of cryogenic electronics for both test fixture measurements and cryogenic wafer probing. This technique was critical to the development of hybrid semiconductive/superconductive microwave integrated circuits operating at liquid nitrogen temperatures.

Measurements of passive resonators showed that distributed circuits fabricated of HTSC materials are capable of significantly higher Qs compared with conventional metals at 77K. Several suppliers discovered the quality of their films from these measurements.[143]

The successful realization of the hybrid semiconductive/superconductive oscillator and amplifier circuits is the first initiative which clearly demonstrates that it is possible to integrate these technologies. This work was recently submitted for presentation at the Microwave Theory and Techniques Symposium.

7.3 FUTURE WORK

Many possible improvements in apparatus, procedure and devices are described in this section. To realize high performance hybrid semiconductive/superconductive MICs and to make them practically viable, accurate simulation of HTSC passive structures, measurement accuracy and throughput, refrigeration technology, active semiconductive and superconductive devices, better substrates for HTSC film deposition, and circuit topology selection will require additional development. Further downstream, this may lead to the fabrication of Monolithic Semiconductive/Superconductive Microwave Integrated Circuits (MSSMICs).

Inaccurate CAD simulation of simple passive high Q HTSC resonators demonstrated that considerable design tool development will be required if more complex and useful circuits are to be realized. For example, an area well suited to utilizing HTSC films is in the filters of multiplexers for spacecraft communications systems. For example, Figure 7.1 illustrates the much reduced volume and mass of an edge coupled HTSC microstrip filter (placed on a quarter) which is intended to perform the same function as a conventional dielectric resonator filter.^[144] However, in this case only low order filters have been successfully fabricated and they are subject to considerable tuning problems due to the high Q of these materials, while high order filters are required.

Although only conventional linear circuit simulators were evaluated in this work, finite element simulations such as EMSIM and EM may provide better results and should be evaluated. If they are also inaccurate, custom software will need to be developed. The resulting models will be required for the design of more complex circuits, such as high order filters.

Figure 7.1. Dielectric Resonator and Equivalent HTSC Microstrip Filter^[144]

Although the present S-parameter measurement apparatus is a considerable improvement over previous attempts, its accuracy and throughput could be further improved. The present cryocooler apparatus may be upgraded to higher frequencies and could obtain fully corrected S-parameters over a range of temperatures without repeating the lengthy calibration sequence. The frequency range of the present setup could be extended by replacing the connectors and cables with higher frequency components. An added benefit is that the smaller cables and test fixtures would have less thermal mass and leakage, reducing the cool-down time. Presently, a TRL calibration may only be made at a single temperature, since the correction algorithm resides in the network analyser firmware. By measuring the standards over a range of temperatures

and storing the data, this data could be post processed with the TRL algorithm, providing calibration sets for several temperatures.

To improve measurement throughput, a cryogenic wafer prober could be constructed. Indeed, several already exist.^[80,145] However, they use coplanar waveguide probe heads which lack covers, limiting their use to low Q circuits. Therefore, a challenge would be to construct an on-wafer cryogenic measurement facility capable of characterizing high Q HTSC components.

Similarly, noise figure measurement accuracy could be improved by using a cryogenic "cold" reference, rather than the room temperature reference in the present noise source. This should become important as low-noise receivers are refined.

In a related area, cryogenic refrigeration technology will require mass, volume and reliability advances to allow semiconductive/superconductive MIC technology to become widely applied. Considering the high temperature sensitivity of HTSC circuits, refrigerators will have to be more stable than those developed for LTSCs. Furthermore, as HTSC circuits have unique requirements, cryogenic refrigerators will have to be redesigned for this technology rather than the IR systems currently in dominance.^[146]

Advances in both semiconductive and superconductive active devices which operate at cryogenic temperatures would directly benefit the hybrid MICs.

In regard to active semiconductor three-terminal devices, P-HEMTs and InP HEMTs, the present performance leaders at room temperature, should be evaluated further for possible application in cryogenic electronics. Tailoring the doping profile to optimize low temperature performance should also be investigated. Advances in the architecture of bipolar devices, such as HBTs, may allow them to operate at low temperatures in low phase noise applications such as oscillators.

Although active superconductive devices based on Josephson tunnel junctions appear far off and were dismissed in this work, the possibility of developing a

novel HTSC structure that exhibits gain does exist. For example, Sandia labs recently demonstrated a three-terminal HTSC transistor with 13 dB gain at 4 GHz by using a control electrode in close proximity to a weak link to modulate its current. Although comparable to an early FET in performance, its power consumption is two orders of magnitude lower; bias current is similar to a FET while voltage is only 20mV.^[147] Although noise properties remain unknown, this is a serious advance in solving the gain problem in HTSCs and may allow completely HTSC MICs to be fabricated.

HTSC thin-film deposition technology is presently in its infancy and considerable improvements are anticipated. Most progress should come from the proper selection of substrate. Q_0 s approximately two times higher on lanthanum aluminate and ten times higher on lower loss substrates appear feasible in the near future. An increase in the critical temperature of new compounds, which would provide even higher performance at 77K, is more speculative. Such advances would allow topologies other than distributed microstrip to be contemplated. For example, to obtain a further size and mass reduction, lumped element components may be fabricated. However, for this to occur will require processing advances in multi-level crossovers for inductors and dielectrics for capacitors. Lower loss should also allow the substrate height to be reduced to decrease the radiation loss in millimeterwave passive structures. For even higher Q s, cooled dielectric resonators may be combined with unpatterned HTSC films to reduce the volume.^[40] Although incompatible with planar microwave circuits, Q s well in excess of 100,000 should lead to less complex filter architectures. On a more practical level, current films still require basic testing of long term stability in various environments to ensure their wide use.

Reviewing the hybrid semiconductive/superconductive circuits reveals several areas where improvements are expected in the near term. In the oscillator, more stable MMIC amplifiers should prevent spurious modes from degrading phase noise. In addition, lower power levels into the resonator and a cover optimized to reduce

radiation loss should improve performance. Similarly, amplifiers using other active semiconductor devices should be evaluated to see their effect on spectral purity. Although the low-noise amplifier demonstrated the possibility of combining the two technologies to obtain excellent noise figure, from a systems perspective, it would be more attractive to have a complex filter on the input such that both the channel filter and amplifier functions may be combined in one unit.^[80]

Looking further into the future, the possibility of fabricating monolithic circuits with hybrid semiconductive/superconductive technology also exists. Specifically, the deposition of superconductive films directly on a semiconductor substrate such as GaAs or silicon may produce exceptional performance. Significant benefits to millimeterwave MMICs are predicted, as transmission line losses presently limit the complexity of these circuits. However, in order for such a technology to be realized, the problem of depositing HTSCs at a temperature compatible with MMIC processing must be solved. In addition to the normal problem of metal depositions contaminating the semiconductor substrate, the semiconductor substrate may contaminate the HTSC. Although some techniques have lowered the annealing temperature to around 650°C, the superconductive crystal phase is formed above 550°C, limiting further reductions.^[11] More promising is the use of buffer layers to separate the semiconductor and superconductor layers. Recently, YBCO has been grown on silicon using this technique.^[148]

At the device level, if HTSC processing advances allow thin-films to be deposited on GaAs, several applications may exist. For example, if the gate metal in a MESFET structure is replaced with HTSC material, gate resistance may be lowered. Since the gate height may also be reduced, easier fabrication of sub-micron gate length devices should be possible, making higher frequency and lower noise devices possible. Such devices, combined with high Q superconductive planar structures, should produce higher performance MMICs.

APPENDIX I 8510 TRL CALIBRATION KIT DESCRIPTION

Standard		Offset		Frequency (GHz)	
No.	Type	Delay (ps)	Zo (Ω)	Minimum	Maximum
14	Delay	0	50	2.5	20.5
15	Delay	22	50	2.5	20.5
18	Open	0	50	2.5	20.5

Standard Definitions

	A	B	C	D	E	F	G	Standard Class Label
TRL Through	14							Thru
TRL Reflect	18							Open
TRL Line	15							Line

Standard Class Assignments

APPENDIX II THERMKON 70M PLATING PROCEDURE

1. Ultrasonic degrease. Rinse.
2. Swab with green pad and comet. Rinse.
3. Etch clean in 30% NaOH for 2 to 5 minutes. Rinse.
4. Ultrasonic rinse in DI water for 1 minute.
5. Ultrasonic rinse in hot DI water at 160 to 180°F.
6. Anodic etch in 15% NaOH at 25A/sq. ft. for 5 to 8 minutes. This removes the Mo skeleton from the outer surface, exposing the copper.
7. Rinse in tap and DI water.
8. Dip in 1:1 HCl for 15 seconds.
9. Rinse well.
10. To fill the pores, electroless nickel strike 200 μ inches thick.
11. To improve adhesion, diffuse nickel into the matrix by placing parts into a tube furnace at 700°C for 15 minutes in an argon reducing atmosphere.
12. Shut down the furnace & cool to room temperature with gases flowing.
13. Activate the nickel in 30% HCl. Rinse.
14. Nickel strike and nickel plate another 100 μ inches. Rinse.
15. Gold strike and gold plate for a total thickness of 100 μ inches.

APPENDIX III TOUCHSTONE LISTING of SEMICONDUCTIVE/SUPERCONDUCTIVE LOW-NOISE AMPLIFIER

SUPER.CKT
SUPERCONDUCTING MATCHED MIC 14GHZ LNA
APR 16 91

DIM
TNG UM

VAR
L1\1002.2
L2\913
L3\1366.3
L4\742.7

CKT
MSUB ER=24 TH=500 T=0.5 RHO=0.01 RCTH=0
TAND TAND=0.00003
MLIN 1 2 W=182 L=1750
MCROS 2 11 3 4 W1=182 W2=25 W3=182 W4=182
MLIN 3 5 W=182 L=L1
MLEF 4 W=182 L=L2
MLIN 11 12 W=25 L=1633
MLEF 12 W=500 L=1078
CAP 12 13 C=100
RES 13 0 R=50
S2PA 5 6 20 FUJ77.OUT
IND 20 0 L=0.1
MLIN 6 7 W=182 L=L3
MCROS 7 15 8 9 W1=182 W2=25 W3=182 W4=182
MLEF 9 W=182 L=L4
MLIN 15 16 W=25 L=1633
MLEF 16 W=500 L=1078
CAP 16 17 C=100
RES 17 0 R=50
MLIN 8 10 W=182 L=1580
DEF2P 1 10 AMP

FREQ
SWEEP 1 20 1
SWEEP 11 17 0.25

OUT
AMP S11
AMP S21
AMP S12
AMP S22
AMP K
AMP K GR2
AMP DB[S11] GR1
AMP DB[S21] GR1
AMP DB[S12] GR2
AMP DB[S22] GR1

GRID
RANGE 0 20 5
GR1 -20 15 5
RANGE 1 5 0.5
GR2 -10 0 2

OPT
FREQ 13.99 14.01 0.02
AMP MAG[S11]=0
AMP MAG[S22]=0

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