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**AN EXAMINATION OF THE GETTERING EFFECTIVENESS OF
BOROPHOSPHOSILICATE GLASS FORMED AT LOW PRESSURE**

**by
Brian A.F.S. Sutherland**

**A thesis submitted to the Faculty
of Graduate Studies and Research
in partial fulfillment of the
requirements for the degree of**

Master of Engineering

**Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University**

January 1990

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submitted by Brian A.F.S. Sutherland, in partial fulfillment
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Master of Engineering

Thesis Supervisor

Chairman, Department of Electronics

**Department of Electronics
Faculty of Engineering
Carleton University**

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Abstract

Borophosphosilicate glass (BPSG) of dopant content 4wt%B and 4wt%P was deposited as an interlevel dielectric over MOS devices. Oxygen:hydrides ratios of 1:1, 2:1 and 3:1 were used for film deposition in an LPCVD reactor. The BPSG films were compared to control samples of SiO₂ and PSG films to evaluate the effect of oxygen:hydrides ratio on sodium gettering effectiveness. Intentional sodium contamination was introduced into the devices using evaporation of NaCl followed by an Na⁺ drive-in. The number of mobile impurities in the MOS devices was evaluated using temperature-bias stress testing (TBST). The results showed that the BPSG films trapped 85% or more of all mobile sodium in conditions of heavy contamination and prolonged heating. BPSG formed at a 1:1 oxygen:hydrides ratio was better than the other BPSG and PSG groups at gettering sodium. In addition to being superior getters, the 1:1 samples had higher boron content (and possibly less P content) than the other BPSG films, indicating that B₂O₃ may play a role in gettering. A trapping mechanism is proposed in which the addition of B to SiO₂ creates non-bridging oxygen, which can serve as cation traps. The flatband voltage shifts of uncontaminated MOS capacitors were found to be larger for devices with doped interlevel dielectrics than for devices with SiO₂ films; the hypothesis that the shift is due to a polarizable species (possibly P₂O₅) is developed. It is concluded that LPCVD BPSG formed with a 1:1 oxygen:hydrides ratio is a viable candidate to replace PSG as an interlevel dielectric, due to its high gettering effectiveness, lower flow temperature, lesser auto-doping of the gate oxide, lower stress, slower etch rate, and few particulates and defects.

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I am indebted to many people for their assistance in the completion of this work. To recognize each of them and their contribution would require a document of considerable length; instead I will give them brief mention here (and proper thanks in person).

I dedicate this work to Yolanda, whose faith and love made it possible. During the course of the project Yolanda and I were blessed with daughters Sarah and Amanda who provided much joy and some perspective. I deeply appreciate the encouragement and understanding of my family and friends.

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1.0 Introduction

Silicate glasses are essential ingredients for the fabrication of silicon integrated circuits. The thermally grown field oxide is used as an impurity mask, a surface passivator and an insulator for overhead conductive layers. The gate oxides of field-effect transistors are thermally grown, have few impurities and high breakdown voltage. Deposited silica films are used as insulators between layers of conductive materials (such as polysilicon or aluminum), passivating overcoats and filling for substrate isolation trenches.

Miniaturization of integrated circuits has dramatically increased the ratio of vertical-to-horizontal device dimension, allowing great circuit density but challenging the capability of traditional processing practices. One difficulty that has arisen is inadequate electrical continuity of aluminum that is deposited over the sharp SiO_2 steps at substrate contact windows. Elimination of such defects is achievable through chemical and heat treatment of the interlevel dielectric. A popular solution is to dope the deposited glass with phosphorus, boron or both¹. The impurities lower the glass softening temperature such that it flows under high temperature, which allows tapering of the sharp edges that would otherwise be present. Boron is roughly three times more effective² than phosphorus for reducing glass fusion temperature. It is desirable to reduce the softening temperature as much as possible (to minimize dopant redistribution during heating), but there are limits to the quantity of B and P that can be added to the glass while retaining its physical, chemical and electrical stability.

¹ The modified oxides are termed "phosphosilicate glass" (PSG), "borosilicate glass" (BSG) and "borophosphosilicate glass" (BPSG) respectively.

² Per unit weight, usually expressed as "wt%".

A very attractive property of P-doped films is the ability to immobilize ("getter") mobile alkali ions. These cations cause serious electrical instabilities when allowed to move freely in oxide layers near the silicon surface. In field-effect transistors they cause the threshold voltage to drift over time and change with changing bias. Bipolar transistors suffer from low gain, high noise and poor leakage. Trapping these contaminants is required to produce good quality integrated circuitry, so the deposited glass plays an important role in providing device stability. In borophosphosilicate glass (BPSG) the primary purpose of the P content is to supply alkali ion gettering.

BPSG is well suited for use in high density silicon circuits. In addition to its low fusion temperature and contaminant gettering, it has relatively low residual stress and a low etch rate. Since it is a relatively new material much effort is being invested to determine how deposition parameters affect its composition and behaviour. It is commonly formed in one of three types of chemical vapour deposition reactor, which operate at atmospheric pressure (APCVD), low pressure (LPCVD) or use plasma enhancement (PECVD). The reactor type and conditions affect most characteristics of the film.

One deposition parameter which has been observed to influence film composition in all types of reactors is the mole ratio of oxygen to the total amount of hydrides in the forming gas. Variation in this ratio can result in differences in deposition rate, number and size of particulates in the film, dopant uniformity and quantity, as well as the chemical state of impurities. The magnitude and nature of these effects are altered by other deposition conditions such as temperature and pressure, so finding the optimum deposition recipe is a difficult and complex pursuit.

1.1 Motivation for This Research :

The need to investigate the effect of oxygen:hydrides ratio on the gettering effectiveness of BPSG arose through discussion with Process Technology Limited, a manufacturer of chemical vapour deposition systems. One of their clients (a major semiconductor manufacturer) had reported that a number of MOS devices with BPSG overcoats were exhibiting unacceptable threshold voltage drift. The films had been deposited in an LPCVD reactor using a low oxygen:hydrides ratio (near 1:1). The target concentrations for B and P in the glass were moderate (not revealed). It was assumed that the cause of the electrical instability was drift of Na^+ in the gate oxide; the speculation was that these mobile cations had penetrated the BPSG passivation layer.

Since the target level of phosphorus in the glass was considered high enough to provide gettering, focus was given to the BPSG recipe. It was suggested that the low oxygen:hydrides ratio could cause phosphorus in the film to be incompletely oxidized, forming P_2O_3 instead of P_2O_5 , which is generally considered the active ingredient in sodium gettering. Learn [36] had demonstrated that the chemical state of phosphorus in LPCVD films was dependent upon the oxygen:hydrides ratio used. A search for existing information on the effect of oxygen:hydrides ratio on gettering efficiency revealed that information on the subject was lacking. Some conflicting results were found on the effect of deposition system on gettering performance. Kern and Smeltzer [30] reported that gettering qualities of BPSG appear to be good for various CVD systems, whereas Avigal [2] reported that BPSG films formed with plasma enhancement were superior to BPSG and PSG samples deposited at

atmospheric pressure. Avigal also observed that borosilicate glasses were as good at immobilizing sodium as PSG ones, indicating that P_2O_5 is not the only sodium-trapping compound and that gettering may be sensitive to the glass composition and/or structure.

Given the paucity of information on the subject, it was decided to test the hypothesis that gettering effectiveness depends upon the oxygen:hydrides ratio being high enough to convert phosphorus into P_2O_5 . It was also hoped that insight into the gettering mechanism of LPCVD BPSG could be gained.

1.2 Structure of the Manuscript :

This report is partitioned into six chapters and one appendix. The title and intent of each chapter is as follows :

- **Introduction** describes the motivation for the project and the organization of the thesis.
- **Background** summarizes the results of previous research in areas relevant to this work.
- **Methodology** describes the method used to test the hypothesis, and includes the rationale behind the choices made.
- **Results** presents the empirical data in a distilled form.
- **Analysis** discusses the results and proposes explanations for the observed phenomena.
- **Conclusions** summarizes the findings of this research.
- **Appendix A** describes a measurement automation program that was written for, and employed in this work.

2.0 Background

This chapter surveys what has been done in prior research on BPSG and ionic impurity gettering. Detail is included where it pertains to this project.

2.1 Requirements for Deposited Dielectric Films :

General requirements for an interlevel dielectric are high breakdown voltage, low defect and particulate density, low stress¹, chemical stability and compatibility with adjacent materials. Failure due to shorts between conductive layers can be avoided if the deposited films have conformal coverage and few pinhole defects. Open failures can be reduced by tapering the sharp profile steps to allow more consistency in the cross-section of the deposited metal lines [45]. Smoothing of the topology is commonly done by modifying the film chemistry to lower its softening temperature, then flowing the glass to achieve the degree of planarization desired [29,30,38,49,56,57]. Boron and phosphorus are very effective at reducing the viscosity of SiO₂ films, and are used elsewhere in the process, so they are usually chosen.

Often two heating steps are performed, one to smooth the topology prior to opening contact windows ("flow") and one to taper contact windows after they have been etched open ("reflow") [12,19,27,29,30,37,42,48,56]. The combination of time and temperature for these steps causes dopant redistribution, which spreads and deepens junctions such that problems arise, such as subthreshold leakage, punchthrough and excessive Miller capacitance [1,30,38,43]. To reduce these effects, effort has been made to lower the temperature used [1,18,29,30,11] and/or shorten the duration of the steps [40].

¹ Low mechanical stress avoids cracking and permits the use of thicker films [29,56].

Since glass fusion temperature drops linearly with B or P content, the standard method is to add as much dopant to the glass as possible while retaining its electrical and chemical stability.

Doped-oxide films are principally used as interlevel dielectrics, but they can also be used as passivation overcoats [2,12,25,36,38,43,57] which protect the circuitry from the environment, isolation trench filling [6] (the insulating fill must have low stress) or as a solid-state doping source [29,38].

2.2 The Effects of Doping SiO_2 with Boron and Phosphorus :

When boron and/or phosphorus is introduced into silicon dioxide some of the physical and electrical characteristics are considerably altered. The softening temperature can drop hundreds of degrees, residual stress lowers, chemical stability worsens, and etch rate can vary broadly. Deterioration of dielectric properties, polarization and immobilization of ionic charge all can affect the electrical behaviour of the material.

2.2.1 Physical Effects :

2.2.1.1 Flow Temperature :

Film flows so that its surface energy is minimized; the amount of flow depends primarily upon the film viscosity and initial surface energy, and secondarily upon the ambient gas type, pressure, deposition system and geometry of the underlying structure [4,10,29,55]. Heating, doping and selection of gas type are common ways of reducing the film viscosity.

All flow and reflow steps use elevated temperature to reduce the viscosity until the glass softens and physical rearrangement occurs. The rate

of flow is proportional to temperature, such that time and temperature can be traded off to achieve a given degree of flow [1,4,29,30,38,43]. Rapid isothermal heating [4,19,27,30,38,40,45] is promising because the time-temperature product can be tailored to give the desired flow angle with minimal dopant redistribution. The wafers are abruptly brought to high temperature (800-1200°C) for times of less than 1 minute using an incoherent lamp array. This technique features lower time-temperature products¹, shallower junction depths, lower sheet resistance and less wafer warpage than for devices processed in furnace tubes, but often exhibit serious film defects.

SiO₂ reaches its softening temperature at 1160°C, a temperature at which dopant redistribution occurs rapidly. Adding B and/or P softens the glass by disrupting the regularity of the glass structure with local distortions, weakening the network and thereby lowering its viscosity [38]. The addition of phosphorus decreases the softening point of silica by 17-27°C/wt%P, with flow angle decreasing at a rate of roughly 4.5°/wt%P [1,11,25,29,30,38,43,49,54]. Thus, to get flow to occur at temperatures below 900°C, or achieve planarization, the P content must exceed 10-12wt%. At such high concentrations the film becomes chemically unstable (see section 2.2.1.3), so PSG glasses are limited to flow above 950°C [4].

For each 1wt% increase in B content, a monotonic reduction of 40-65°C in flow temperature is achieved [4,5,18,27,30,38,43,54]. Boron has a greater effect than phosphorus largely due to the light nature of B (for equal wt% of each element there will be 2.9 times as many B as P atoms). Also, the linked-

¹ Prior research [27,29] has shown that for BPSG films of 4wt%B and 4wt%P in N₂, rapid isothermal heating flow after 30 seconds at 1100°C is equivalent to furnace tube flow after 30 minutes at 925°C.

ring structure of B_2O_3 has weak inter-ring bonds, due to substitutional B in BO_3^{3-} eliminating a bridging O bond from a neighbouring SiO_4^{4-} tetrahedron [50]. In contrast, the P_2O_5 structure consists of sheets of PO_4^{4-} tetrahedra, which are linked to adjacent tetrahedra, making it inherently stronger [38,43]. There is interaction between B and P in BPSG films : at less than 4wt% B, BPSG is softened when P_2O_5 is added; near 4.5wt%B the amount of P_2O_5 has little effect; above 4.5wt%B the addition of P_2O_5 raises the fusion temperature [38,43].

Annealing, flow and reflow are done in an N_2 , O_2 or steam ambient, with N_2 having the least softening effect upon the glass. Flow can be accomplished at a lower temperature (25-30°C) in O_2 and much lower (50-70°C) in steam [1,2,4,5,17,18,27,29,30,49,54,57]. Alternatively, the time of heating can be lessened for a given temperature, with steam heating requiring half of the time needed as for heating in N_2 [4]. Problems which arise with steam heating are oxide growth in the contact windows and the production of corrosive acids through reaction of water and glass constituents [4,30,54].

Many studies have shown BPSG fusion to occur at temperatures 100-350°C below that of similar PSG films [2,4,10,18,27,29,30,38]. Examples of flow¹ conditions for BPSG films are given in Figure 1.

2.2.1.2 Film Stress :

Mechanical stress in doped SiO_2 films is usually of much smaller magnitude than for undoped SiO_2 [2,11,25,29,30,36,37,47,56]. The presence of B and/or P typically reduces the film stress to low-compressive, though low-tensile stress may occur in strongly doped glasses or after densification. The

¹ Nominally 40° reduction in flow angle.

method of deposition influences the stress type and size, with LPCVD and PECVD yielding the lowest stress magnitude. Such films improve reliability by lowering crystallographic damage and wafer warpage, and allow formation of thicker films.

Figure 1 : Examples of BPSG Flow Conditions

Bor% / Pot%	Temp. [°C]	Time [min]	Ambient	CVD Type	Reference
2.0 / 4.0	925	30	steam	LPCVD	18
2.1 / 3.6	988	60	N ₂	(not CVD)	38,43
2.1 / 6.4	963	60	N ₂	(not CVD)	38,43
2.5 / 5.0	920	n/a	steam+O ₂ +N ₂	LPCVD	36
3.0 / 5.0	920	30	N ₂	PECVD	48
3.0 / 5.4	800	30	steam	PECVD	2
3.4 / 4.5	1000	30	N ₂	APCVD	30
3.5 / 4.0	850-925	30	steam	LPCVD	18
3.5 / 4.0	650-925	30	N ₂	LPCVD	18
3.6 / 4.7	820	60	N ₂	(not CVD)	38
4.0 / 4.0	980	30	N ₂	PECVD	54
4.0 / 4.0	925-950	30	N ₂	APCVD	29
4.0 / 4.0	900-925	30	steam	APCVD	29
4.0 / 4.0	825-850	30	N ₂	PECVD	48
4.0 / 5.0	870	30	N ₂	PECVD	54
4.1 / 3.7	925-950	30	N ₂	APCVD	30
4.1 / 4.7	900	20	N ₂	PECVD	19
4.1 / 6.6	900	20	N ₂	PECVD	19
4.3 / 7.2	900	20	N ₂	PECVD	19
4.5 / 4.0	900	5+25	steam+N ₂	LPCVD	49
4.5 / 4.0	800	30	steam	LPCVD	49
4.6 / 3.1	820	60	N ₂	LPCVD-T	4,5
4.7 / 4.1	825-850	30	N ₂	APCVD	30
5.0 / 4.0	875	40	O ₂	APCVD	27
5.0 / 4.0	825-850	30	N ₂	APCVD	29
5.0 / 4.0	800-825	30	steam	APCVD	29
5.0 / 5.0	820	30	N ₂	PECVD	54
5.5 / 3.5	850	60	N ₂	LPCVD-T	6
5.6 / 3.1	780	60	N ₂	LPCVD-T	4,5
5.7 / 2.5	800	30	steam	PECVD	2
5.7 / 3.1	725-750	30	N ₂	APCVD	30
6.0 / 1.8	853	60	N ₂	(not CVD)	38,43
6.0 / 3.0	725-750	30	N ₂	APCVD	29
6.0 / 3.0	700-725	30	steam	APCVD	29
6.0 / 3.6	843	60	N ₂	(not CVD)	38,43
6.5 / 4.0	880	30	N ₂	PECVD	54
6.8 / 2.9	720	60	N ₂	LPCVD-T	4,5

Notes : "n/a" means Information not available; "LPCVD-T" means LPCVD with TEOS

2.2.1.3 Chemical Stability :

The excellent stability of SiO_2 makes it a desirable insulator and passivation overcoat. Silica doped with phosphorus and/or boron is more porous, permitting H_2O to enter the glass and react with the P and B to form phosphoric and boric acids [1,2,4,5,10,11,25,29,30,37,38,43,44,57]. The acids in these hygroscopic films reduce chemical stability and are prone to leeching to the surface, which can cause surface devitrification, corrosion of aluminum and detachment of photoresist. The amount of acid which precipitates depends to some extent upon the deposition method used and subsequent densification [4,27,29,30], but chiefly upon the quantity of dopants in the film.

As-deposited CVD glasses tend to have poor chemical and electrical stability, each of which is improved significantly by densification. The amount of phosphorus is limited to less than 7wt% in PSG and 4-5wt% in BPSG; at higher levels the films are useless [1,2,4,10,11,29,30,38]. Boron is limited to less than 4-5wt% to keep BPSG films reliable [4,5,30,38,43], with boric acid precipitation worst in LPCVD films [4]. These limitations impose a boundary for how much of the glass softening can be achieved through doping and how much heating will be required. Gettering performance is not strongly limited, since these concentrations are high enough to provide virtually complete sodium trapping. To improve stability, dopant concentration can be limited near the outer surface, glasses can be immediately annealed following deposition, densification and storage can be done in dry ambient gas and adhesion promoter can be used to aid photoresist application [4,11,27,30,43,54].

2.2.1.4 Etch Rate :

The etch rate of B and P doped films in HF solutions¹ is directly affected by the quantity of each element [2,4,5,11,16,18,27,29,30,37,48,49,51,54,59]. The etch rate increases with rising P content and decreases with increasing B content. These effects are not strongly affected by deposition conditions or subsequent processing steps.

2.2.2 Electrical Effects :

2.2.2.1 Dielectric Properties :

The breakdown electric field for BSG, PSG and BPSG varies from 1.5 times higher to an order of magnitude lower than for SiO₂ films [3,29,30,51]. Though dielectric strength can be diminished by doping, breakdown through film flaws, pinholes and shorts is generally eliminated. LPCVD films have higher dielectric strength than APCVD glasses, due in part to lower particulate density [4,30]. Leakage currents tend to be 1-2 orders of magnitude higher than for thermal SiO₂ [51]. The dielectric constant can vary from 3.8 to 4.5 depending on dopant concentration, deposition and annealing conditions [29,30].

2.2.2.2 Polarization :

The application of a potential difference across a doped film can cause polarization of the P and B complexes, resulting in a change in the substrate space charge, which shifts the flatband and threshold voltages. The amount of shift depends upon the magnitude and duration of applied electric field and

¹ Slow rates are preferred because they allow controlled feature etching. A more thorough discussion of etch rates is contained in section 2.6.

² Pure, or buffered with NH₄F ("BHF"), or diluted with HNO₃+H₂O ("P-etch").

dopant concentration in the film. This polarization is entirely reversible, though the electrical instability that it introduces can seriously degrade device behaviour [1,2,29,31,33,51].

Two polarization effects have been observed, one fast and one slow [3,17,51]. The fast one saturates within milliseconds at 200°C and is thermally activated with an energy of 1.0 eV. Film polarizability for this process does not vary with size or polarity of electric field and is proportional to the square root of P_2O_5 content [3,17,51]. The slow process occurs above 100°C with activity beginning after several hours at 200°C. It is independent of polarity of the electric field and depends strongly on the P_2O_5 concentration [3,51]; a causal mechanism of ion migration through the oxide has been proposed [51].

Polarization in P-doped oxides can be attributed to the pairing of oppositely charged P sites. In P_2O_5 , P substitutes into two Si positions in SiO_4^{4-} tetrahedra, one P site having a relative positive charge (PO_4^{3-}) and one having a non-bridging oxygen (PO_5^{4-}) [3,17,50]. In the presence of an electric field the non-bridging oxygen can move to the positively-charged sites as depicted in Figure 2 (after [3]).

2.2.2.3 Immobilization of Ionic Charge :

The addition of phosphorus to SiO_2 has been shown to immobilize mobile cations [2-4,8,12,17,22,27,30-32,39,43,44,51,56,58,59,61]. A weaker effect has been suggested for boron in silica [2], but no strong correlation has been determined [4,5,11,29,30,43]. A complete discussion of the gettering effects of P and B in oxides is contained in section 2.4.

Figure 2 : Polarization Mechanism for P_2O_5

2.3 Mobile Ionic Impurities in SiO_2 :

Thermally grown and deposited SiO_2 are excellent insulators for the gate, field and interlevel dielectrics in silicon circuitry. However, the electrical behaviour of silicon devices is degraded by the action of mobile ionic impurities drifting and diffusing through these oxides.

2.3.1 Electrical Effect :

The effect of charge residing in the oxide is to induce a charge of opposite polarity in the substrate. The amount of induced charge relates inversely to the distance of the oxide charge from the substrate [12,21,52,61]. In MOS Field-Effect-Transistors the induced charge shifts the flatband (and therefore threshold) voltage, causing source-drain conduction to vary with history of gate bias [17,22,44,61]. In bipolar transistors the effect manifests itself as low current gain, low breakdown voltage, high junction leakage and

high noise [12,44]. The presence of Na^+ in the oxide also strongly influences the radiation sensitivity of underlying devices : ionizing radiation liberates sodium, which then drifts to the surface and perturbs the space-charge balance there [24]. To retain satisfactory performance for most silicon devices, mobile charge concentrations must be kept near or below 10^{10} ions/cm².

2.3.2 Incorporation :

Many of the substances used in the fabrication of MOS devices are sources of contamination (particularly sodium) [8,12,33,24,44,62]. Precautions are taken : laboratory chemicals are purified, quartzware is usually treated with HCl to getter sodium, and low-sodium filaments are used in aluminum evaporation. Nevertheless, alkali ions do get into the wafers through furnace tubes and boats, evaporator fixtures, gaseous ambients and reactants, chemical etchants and solvents, beakers, tweezers and human handling. Sodium contamination is usually kept in the 10^9 - 10^{10} ions/cm² range in modern fabrication lines, but can vary from 10^8 - 10^{12} ions/cm² [8,17,22,44].

2.3.3 Chemical Nature :

The most common mobile impurities are small, light, alkali ions : Li^+ , Na^+ and K^+ [12,44,52]. Though lithium is the most mobile, it is rare and has only been detected in trace amounts in glass. Na^{+1} has the smallest radius of the common ions and moves freely above 110°C [12,14,17,22,31,34,44,52]. No bias-stress flatband shift is generally observed unless there is Na^+ detected also [61]. Potassium stays at the gate/oxide interface below 200°C, begins moving above 225°C and moves freely (though slowly) above 300°C [7,13].

¹ Sodium in SiO_2 moves entirely as Na^+ [17].

Rubidium and Cesium are uncommon and are immobile below 400°C [13]. Type II elements have been observed to be immobile in silicon dioxide.

2.3.4 Release and Movement :

The as-processed distribution of Na^+ in an oxide customarily consists of high concentrations near the silica boundaries and an even distribution through the bulk [8,14,15,22,52,61]. This affinity for boundaries is probably due to potential wells¹ (non-bridging oxygen atoms behave as hole traps) which capture and hold the cations [7,13-15,22,24,32]. Movement away from either interface is emission-limited with a number of activation energies [7,14,17,22,34,35,53]. The portion of the total number of contaminant ions that is mobile depends exponentially on temperature, with emission rate a monotonically decreasing function of time [34,35]. Once released, ionic sodium moves with high mobility (possibly assisted by interaction with hydrogen) at a constant rate, regardless of direction [7,22,34,35].

2.4 Gettering of Mobile Ions :

The chief means of reducing the effect of mobile alkali ions is to minimize their quantity through clean fabrication materials and equipment. As an adjunct, gettering of the impurities can be accomplished through the introduction of chlorine anions or cation traps in doped glasses. Though effective, gettering can only be relied upon for impurity concentrations of less than 10^{15} ions/cm², since even held cations will be partially compensated in the substrate space-charge region [3,17,22].

¹ The number of wells at SiO_2/Si boundary exceeds 5×10^{12} traps/cm² [7,8].

2.4.1 Chlorine Anions:

A mixture of O_2 and HCl is often introduced into quartz furnace tubes used for processing. This "HCl clean" works by reacting Cl^- with Na^+ to form a volatile NaCl complex which evaporates during heating, or inactive salts upon cooling [33,39]. This reduces the mobile ion concentration (by more than an order of magnitude), with no change in other characteristics [33]. A similar technique is sometimes employed in the growth of the gate oxides, where the oxidizing gas is a mixture of O_2 and 2-6% HCl [44].

2.4.2 Phosphorus-Doped Glasses:

Phosphosilicate glass getters sodium [2-4,8,12,17,22,27,30-32,39,43,44,51, 56,58,59,61]. Sodium cations in PSG+ SiO_2 films have been observed to be entirely held in the PSG layers or at the PSG/ SiO_2 interface [3,8,61]. When a PSG layer is added to a SiO_2 film containing Na^+ and K^+ , the contaminants are quickly and uniformly redistributed and trapped within the PSG upon heating [3,8,61]. Thus, PSG films of small polarizability are very useful in stabilizing surface charge against impurity movement [17].

Gettering appears to require phosphorus in the P_2O_5 oxidation state. The presence of P_2O_5 both slows the transport rate¹ and increases the activation energy required to liberate trapped Na^+ [11,17,61]. The mechanism is that P_2O_5 polyhedra produce two substitutional atoms for Si (in SiO_4^{4-} tetrahedra), providing a free positive charge and a non-bridging O^- [3,17], which can capture mobile cations as pictured in Figure 3. The depth of these P-related traps is larger than most other traps in the silica, such that a higher

¹ Up to 8 orders of magnitude for 10^{13} ions/cm² in 4wt%P glass [17].

activation energy is required to launch ions, and therefore the traps in the P-doped glass will be less likely to emit their captives. The movement of Na^+ in PSG is therefore emission rate-limited, temperature-induced and is comprised of drift in the applied electric field. This motion decreases sharply as the concentration of P_2O_5 in the glass rises, due to the higher number of non-bridging O^- sites [3,17].

Figure 3 : Gettering Mechanism for P_2O_5

2.4.3 Boron-Doped Glasses:

The major reason for including phosphorus in BPSG is to supply gettering, since B_2O_3 has been assumed to provide little gettering effect [4,5,11,29,30,43]. However, studies by Avigal [2] have shown gettering for all compositions (0-3wt%B/0-7.4wt%P), with some BSG films better than PSG ones. This indicates that gettering is not just a function of $\text{P}=\text{O}$ bond, could be caused by boron complexes, and is sensitive to the glass structure. Glasses co-doped with B and P have shown gettering as effective as for PSG films of similar P content [2,29,30].

2.4.4 Heating Effects:¹

High temperature steps (densification, flow, reflow) allow much of the mobile charge present in the glass to settle into available trap sites, usually within the first 10 minutes [2,17,57]. Heating also has the effect of changing most P-Si bonds into P=O type bonds, which converts PH_3 and P_2O_3 into P_2O_5 , thereby providing effective gettering of sodium [23,57].

2.5 Effect of Deposition System :

Three types of deposition systems are commonly employed to fabricate BPSG : APCVD, PECVD and LPCVD. APCVD allows rapid deposition rate and good dopant uniformity but has poor step coverage and high particulate and defect density. PECVD features low particulate and defect density and good step coverage but complexity of the reaction and incorporation of toxic compounds remain problems. LPCVD reactors have the lowest deposition rates but produce conformal films with few defects, particulates or unstable chemicals.

2.5.1 Atmospheric Pressure Deposition (APCVD) :

APCVD features a simple deposition system and allows high throughput, so it appears attractive for large volume processing lines. Deposition entails the reaction of B_2H_6 , PH_3 , SiH_4 , and O_2 at 330-460°C and room-ambient pressure [26,27,29,30,49]. The utilization of reactant gas is poor, partially due to mutual inhibition of the hydride components². Temperature also affects composition : as it decreases B content rises and P content declines, with more

¹ Section 2.5.4 contains further discussion of densification.

² Diborane inhibits the oxidation rate of phosphine, so that P content drops with increasing B content [29,30].

P in P_2O_3 than in films formed at higher temperature¹. Oxygen:hydrides ratios are high - 20:1 and 30:1 are the common choices from the range of 10:1 to 60:1. Increasing the oxygen:hydrides ratio reduces deposition rate, number of particulates and defects, and boron content of the glass. Growth rates of up to 1600 Å/min are possible, though film quality degrades severely at rates above 1000 Å/min. APCVD offers very good thickness uniformity ([27] reported +/- 1.5% over a 100 mm wafer) and smooth dopant profile. The weakest aspect of APCVD films is their high density of particulates and defects, commonly more than an order of magnitude higher than for similar PECVD or LPCVD films. Film stress tends to be higher than for other CVD films and is tensile as-deposited, and compressive after densification or fusion [29,30,37]. Step coverage is poor, as is the stability of the as-deposited glass [27,30]. Densification improves the stability significantly (see section 2.5.4).

2.5.2 Plasma Enhanced Deposition (PECVD) :

Plasma Enhanced CVD systems use a relatively complex reaction to produce high quality films with good step coverage. Once the wafer substrate is heated to 300-450°C, films are formed through the reaction of B_2H_6 , PH_3 , SiH_4 , N_2O and O_2 in an ionizing rf field at pressures of 0.6 to 2.35 Torr [2,30,47-49,54]. The $N_2O:SiH_4$ ratio is kept above 30:1 in order to yield good dopant uniformity. Growth rates of 300-3800 Å/min have been reported [47,48], with variation due to rf power, substrate temperature and dopant content². Film thickness variation is +/- 2-5% (over a 100 mm wafer) [19,30,47,48,54], with low particulate and defect densities : 0.06-0.15 defects or particles(<2 µm)/cm² have

¹ P_2O_3 in low temperature BPSG is roughly 25% of total P, as opposed to 10% for high temperature films.

² Growth rate relates inversely with phosphorus content

been reported [19,30,48,54]. Excellent dopant uniformity has been observed for films of 0-6wt%B and 0-11wt%P [30,48,54], though incorporation of PH_3 and other reagent gases in a non-oxidized form is a problem for PECVD films. The amount of P held in P_2O_3 and PH_3 is relatively large [11,23,49], so densification is imperative. The glass quality improves with increasing oxygen:hydrides ratio [54], and has been noted to get better than similar APCVD films [2]. Other characteristics of PECVD films include low intrinsic stress [2,47], good adhesion [2] and excellent step coverage.

2.5.3 Low Pressure Deposition (LPCVD) :

Films of very good quality have been deposited in low pressure CVD systems [2,4-6,18,25,36,38,40,55]. LPCVD films suffer from low deposition rate but characteristically have the highest uniformity, fewest flaws and best step coverage of deposited oxides.

Standard LPCVD reactors operate at pressures of 0.1-0.3 Torr and temperatures of 300-500°C [18,30,36,37]¹. Most systems utilize the reaction of B_2H_6 , PH_3 , SiH_4 , and O_2 , though BCl_3 and trimethylborate (TMB) can also be used as boron sources² [4-6,18,25,30,38]. Gas flow can be perpendicular or parallel to the wafers. The growth rate tends to be low (75-230 Å/min [18,25]) and depends on wafer spacing, pressure, temperature, gas flow rate, oxygen:hydrides ratio and dopant content [25,36,37]. The slow formation yields good thickness uniformity (+/- 2.7% over 100 mm wafer [18]) with very low particulate and defect counts : <0.2 particles(<2 µm)/cm² [2,4,5,30]. Dopant

¹ When LPCVD systems use decomposition of tetraethylorthosilicate (TEOS), pressures of 0.25-0.5 Torr and temperatures of 620-700°C are used [4-6,38].

² BCl_3 enhances P incorporation but can incorporate excessive HCl in the film [4,18,30]. TMB is attractive because it is roughly 2000 times less toxic than diborane [4-6,25,38].

uniformity is also superior, with B and P distribution held to within $\pm 0.2\text{wt}\%$ over a 100 mm wafer [4,5,18,36,37]. B is incorporated as B_2O_3 , and content increases as B_2H_6 mole ratio increases and/or temperature decreases [37,38]. Phosphorus is incorporated as P_2O_5 , P_2O_3 and PH_3 and increases as pressure and/or temperature decrease [4,11]. Stress is usually low-compressive [36,37] and step coverage is excellent [30], as is film adhesion [4,5].

The oxygen:hydrides ratio most strongly affects the chemical state of dopants in the glass, particularly phosphorus [36]. Below a ratio of 1.5:1 the amount of PH_3 and P_2O_3 in the film increases as the ratio diminishes. PH_3 content also climbs as oxygen:hydrides ratio rises above 1.5:1, while P_2O_3 content rises slightly. The quantity of P_2O_5 is inversely related to the other species, and is maximized at an oxygen:hydrides ratio of 1.5:1, therefore this ratio is commonly chosen [18,37,30]. The low ratio case can be explained by the relative scarcity of bonding oxygen, but the high ratio case indicates that simple analysis is insufficient. The gettering efficiency of the film should follow the P_2O_5 content variation, since other P-compounds do not appear to contribute significantly to gettering [23,57].

2.5.4 Film Densification :

Immediately following deposition of the BPSG layer a heat treatment is performed to reorder the glass structure, reduce film defects, minimize fixed charge and fast surface states, free trapped gases and chemically stabilize any elemental components. This anneal is done at temperatures near the glass softening point (typically above 700°C) and can be used as the flow step if desired. Oxygen bearing ambients allow rearrangement of the silica at lower temperatures than inert ones, so steam is often chosen (though the moisture

can react with B and P to form acids) [27,57]. Densified BPSG flows at lower temperatures, has fewer flaws, has greater stability (electrical and chemical) and etches more slowly than as-deposited films [2,27,29,30]. The heat converts interstitial P in P-Si bonds into substitutional P in P=O bonds and allows PH_3 and P_2O_3 to fully oxidize into P_2O_5 , which improves alkali ion gettering [23,36,54]. A deleterious effect is that often boron and phosphorus move to the film boundaries, gathering at the Si interface (where some diffuses into the substrate), or evaporating out of the top of the glass¹ [2-5,27,51,57]. This effect is attenuated when an inert ambient gas is used [27]. It is standard practice to densify newly-deposited BPSG films despite these drawbacks.

2.6 Methods of Determining Glass Composition :

The composition of thin dielectric films is difficult to determine accurately [43, 49]. Some of the methods used to analyze BPSG are as follows :

- Wet chemical colourimetric methods [10,18,23,29,30,36,37,43,49] are slow and destructive, but are accurate and are used to calibrate other methods. These techniques involve dissolution of the film in a solvent solution, followed by spectrophotometric analysis of the precipitates.
- "Ion Chromatography" [4,5,23,30,54] also involves examination of dissolved samples, but focuses on anions in the sample (rather than precipitates). It is useful for identifying oxidation states of B and P.
- "Electron Microprobe" [19,29,30,36,54] utilizes an electron beam to excite X-rays in the sample. The emissions are analyzed to determine elemental type and quantity. It is limited by the low electron beam

¹ Near 1000°C blisters can form in the glass when impurities boil off [57].

energy required for thin films.

- "Secondary Ion Mass Spectroscopy" [4,5,11,18,27,29,30,37] is used when information on dopant content and profile is desired. Bombardment with a stream of neutral ions results in emission of secondary ions in the sample material. SIMS is relatively inaccurate and often causes charging of the sample films during testing.
- "Infrared Spectroscopy" [2,4,5,27,29,30,49] is a rapid, non-destructive technique that involves examination of the infrared absorption spectra of the test sample. Since the absorption peaks for P=O and B-O overlap a Fourier Transform is used to extract estimates for the actual peaks.
- Less common methods include "Electro-Chemical Spectroscopic Analysis" [47,57], "Auger Electron Spectroscopy" [57], "Neutron Activation" [8,61] and "X-Ray Fluorescence" [27,29,30,54].

The etch rate of B- and P-doped SiO₂ is a good compositional indicator and easy to determine¹, so it is widely used [2,4,5,11,16,17,27,29,30,49,51,54,59]. Phosphorus increases the etch rate, while boron slows it², as does densification [2]. As B content approaches 5wt% the effect on etch rate in BHF saturates, such that no further rate decrease is observed [4]. These effects are observed regardless of CVD system used [37]. Since etch rate varies with several conditions, it is most useful for estimation of B and P content rather than for precise determination.

¹ Timing the etching of contact windows yields an in-process estimation of etch rate.

² The rise is roughly exponential with increasing P₂O₅ content [16,51,54].

2.7 Methods of Determining Ionic Impurity Concentration :

2.7.1 Flame Photometry :

Flame Photometry has been used in several experiments [47,62]. This technique uses spectral analysis of the pyrolytic decomposition of the material under study; the spectrum is compared with that of a control substance of known sodium concentration. This method is capable of resolving sodium in concentrations of 10^{10} ions/cm² or more and has the advantages of being quick, inexpensive and capable of analyzing a range of materials. Its disadvantages are that it is destructive, difficult to calibrate, and results are difficult to reproduce.

2.7.2 Aqueous Radiotracer :

Another chemical method involves application and drive-in of sodium isotopes, which are then tracked using a radiotracer analyzer [8,29,61]. Na²²Cl, Na²⁴OH, Na²⁴Cl or Na²⁴Br⁸² in an acid-free solution is applied (in solution or by evaporation) to the wafer surface, then the wafer is heated¹ to allow the sodium isotope to permeate the underlying glass. The wafers are thoroughly rinsed in de-ionized ("DI") water and alcohol to remove surface deposits, then progressively etched and at each depth an autoradiogram is taken. The number of sodium ions remaining in the film must be calculated using the measured radioactivity and corrected with the decay constant of the isotope [2,29,61]. This method offers mediocre resolution of sodium concentration (at best 10^{11} ions/cm²), is time-sensitive (due to radioactive decay) and time-consuming (due to progressive etches).

¹ At 500-600°C for 16-22 hrs [8,29].

2.7.3 Neutron Activation :

Neutron Activation involves irradiating the sample with a neutron flux, which creates isotopes of the constituent elements of the glass. The isotopes are counted with a radiotracer after successive etches to determine sodium (or other element) profile. Like other radiotracer techniques it is destructive, elaborate, lengthy and is unreliable for concentrations below 10^{12} ions/cm².

2.7.4 Current-Based :

The above methods have the disadvantage of destroying the samples under test, making them undesirable for in-process testing. The "Triangular Voltage Sweep Test" (TVST) is a non-destructive method which quantifies ionic impurities through observation of the electrical effect of their movement [13,35,58,59]. After heating the sample, rising and falling voltage ramps are applied to the gate of the device and the gate/substrate current is recorded. The resultant I-V curve is rectangular (quasistatic displacement current) with superimposed peaks due to ionic impurity displacement current. The area under each peak is directly proportional to the number of mobile impurities. The combination of gate bias and temperature at which these peaks appear are signatures for different elements (i.e. peaks for Na⁺ and K⁺ appear in separate portions of the curve). The benefits of this method are that it is quick, non-destructive, sensitive (resolution to 10^9 ions/cm²), and allows differentiation of types of impurities and transport mechanisms. Drawbacks are that sensitive measurement equipment is needed (current measured in picoAmps), noise immunity is poor, area under the curve is difficult to measure¹, ion peaks will

¹ The baseline under the ion peak is not flat, it is parabolic.

not appear if the experimental parameters (ramp slew rate, voltage range, temperature) are not chosen properly, and oxide leakage and semiconductor property changes can introduce extra peaks that throw off the baseline curve.

A similar method [34] involves measuring the displacement current induced during repetitive short-duration triangular voltage pulses applied to the MOS structure. The flatband voltage shift is derived from the current measurements and is then differentiated with respect to time. The result is proportional to total ionic current. This procedure has the same advantages and disadvantages as the TVST method, except that the noise immunity is better due to the good stability of the flat-band measurement.

A variation of the TVST is the "Thermally Stimulated Ionic Current" (TSIC) test [7,17,22,53]. The difference is procedural : under a constant bias the temperature¹ is ramped and the gate-substrate current is measured. The bias can then be reversed and measurements repeated. The movement of mobile ions is characterized by peaks of current, with different elements moving at different temperatures. The advantages and disadvantages are virtually identical to those of the TVST.

2.7.5 The Temperature Bias Stress Test :

The most widely used non-destructive measurement technique is the "Temperature Bias Stress Test" (TBST) [2,12,13,15,21,22,24,29,31-33,35,39,51,52,61]. The test involves electrothermal stress of a MOS capacitor : a voltage is applied between the gate and substrate of the device while temperature is elevated for a given duration and then returned to the start temperature. The flatband

¹ In reference [7] the temperature ranged from -53 to +207°C

voltage changes due to shift of mobile ionic impurities and polarization of the dielectric. Figure 4 depicts a cross-sectional view of the MOS capacitor and illustrates alkali ion movement during negative- and positive-bias stressing.

Figure 4 : Ionic Movement During Electrothermal Stress

The test conditions are chosen such that virtually all of the mobile oxide charge is shifted from one oxide boundary to the other, with the charge magnitude determined by multiplying the flatband voltage shift by the oxide capacitance per unit area, and dividing by the elementary electron charge. The stress parameters (electric field, temperature, time) strongly influence the amount of shift [17]. The positive features of the TBST are that it is non-destructive, simple, relatively quick, and can resolve charged impurities at $<10^9$ ions/cm² concentrations; the negatives include the need for correction for polarization of the oxide and the fact that any change in surface state density during stress affects the results [35]. TBST measurements often serve as the basis with which the accuracy of other methods is gauged.

2.8 Methods of Contamination :

In order to observe the effect of BPSG on the movement of ionic impurities, it is important to keep the level of contamination constant across each sample wafer and between wafers being compared. As-processed sodium levels can vary over several orders of magnitude [8,17,22,44], so comparative studies commonly use intentional contamination at levels high enough to mask as-processed variation and low enough not to change the characteristic behaviour of the oxide. A survey of contamination methods follows.

2.8.1 Aqueous Solutions:

Aqueous solution contamination has been used in several (particularly early) studies [7,29,39,46,52,61,62]. The procedure involves rinsing samples in solutions of known sodium content, followed by a drying step. Impurities are adsorbed directly onto the wafer surface, after which mobile species may venture into the device strata. The relationship between the amount of Na^+ and K^+ in the solution and in the contaminated oxides is roughly linear [7]. In SiO_2 the number of surface sites available for cation adsorption is limited to about 10^{15} sites/cm² [46]. The drying step has a profound effect upon the uniformity of contamination - allowing the samples to dry through evaporation in a laminar flow hood results in a large variation¹ in sodium concentration, regardless of whether the sodium comes from a water- or alcohol-based solution. This is due in part to sodium being drawn (by surface tension) to remaining wet areas, causing the contamination to be light in the first-to-dry areas and heavy in the last-to-dry areas. It is common for the

¹ The amount varies depending on the strength of the solution.

variation in Na^+ level to be more than an order of magnitude over a 50 mm wafer [7,8,61]. Blow-drying with N_2 is more effective in achieving uniform contamination, though it results in reduced sodium levels. It is typical for the sodium contamination to vary by $\pm 25\%$ over a 100 mm wafer.

Radioactive sodium in an aqueous solution is applied when radiotracer analysis is used (see section 2.7.2). Sodium isotope concentrations of up to 1×10^{14} ions/cm² have been reported using this approach, with a moderate degree of variation in uniformity [8].

2.8.2 Diffusion and Implantation :

Diffusion of NaCl has been used to obtain uniform distributions of sodium. Concentrations of 10^{10} to 10^{15} ions/cm² (following the required drive-in heat treatment) have been reported [3]. Ion implantation of Na^+ has been used to provide heavy, uniform impurity levels (to 10^{15} ions/cm²) [24,30].

2.8.3 Evaporation :

Sodium species have been successfully evaporated onto Si devices at various stages of fabrication [3,7,14,15,17,22,34]. Filaments of tungsten or molybdenum are used, which often contain small amounts of sodium and larger amounts of potassium [7,13,24,33]. This allows the filament to be used as the chief contaminating source if desired, with in-situ contamination of the gate electrode an option [15]. Tungsten filaments have been observed to produce alkali ion concentrations up to 10^{12} ions/cm². Usually the filament is charged with sodium using adsorption of NaCl [3,14,17,22], NaOH [34], or NaI [17] from an aqueous solution¹. The sodium compound that coats the wafer

¹ The choice of anion does not affect the mobility of Na^+ in the silica [17].

dissociates on heating, with the Na^+ moving into the underlying oxide and the larger halogen ions staying on the surface, where they can be removed with DI water rinses. To ensure an even coating, the evaporator chamber pressure must be low enough to make the mean free path of the sodium much longer than the distance from the filament to the target. Uniform contamination levels of 10^{11} - 10^{15} ions/cm² have been achieved using evaporation [15,17,34].

2.8.4 Contaminant Drive-in :

All of the above methods produce a layer of ionic sodium on the outer surface of the oxide. To redistribute the sodium throughout the MOS structure it is necessary to heat the sample. The temperature is kept relatively low to avoid significant dopant diffusion in the substrate; 400°C is typical, with 300-600°C having been reported [2,3,8,15,29,39,46]. The duration of heating depends upon the thickness and dopant content of the glass layer, with time increasing more than an order of magnitude for doped glasses. Times of 20-30 minutes are common for SiO_2 films, while 12-24 hours has been used for doped glasses. An atmosphere of N_2 is used to prevent further oxide growth.

3.0 Methodology

This chapter describes the procedures used and discusses the rationale behind the decisions that were made in the construction of this experiment.

3.1 Choice of Sample Groups :

The main objective of this research project is to examine the effect that varying oxygen:hydrides ratio has upon the gettering effectiveness of BPSG. Thus, there is a requirement to study at least two BPSG films for a relative comparison. Having a greater number of BPSG film samples is desirable in order to find an optimum oxygen:hydrides ratio. The number of film types should be limited though, so that an adequate number of samples of each type can be tested without requiring an excessive amount of lab time.

An oxygen:hydrides ratio of 1.5:1 is typical for LPCVD BPSG films [18,30,36,37]. At lower ratios the phosphorus does not oxidize completely, causing phosphine to be included in the silica [36]. Ratios above 2:1 are less common, possibly because phosphine appears in glasses formed with high oxygen:hydrides ratios [36]. PTL¹ had indicated that films formed with a 1:1 ratio were inefficient at trapping Na⁺ but films made using a 3:1 ratio were effective. This range of ratios appeared most promising for scrutiny - 1:1 is on the low end of useful ratios, 3:1 is relatively high. A 2:1 oxygen:hydrides ratio is common and thus can be used to supplement the extremes.

A film thickness of 0.5 μm was chosen for the deposited films². The quantity of phosphorus should be high enough to arrest alkali ion movement

¹ Process Technology Limited of Oromocto, New Brunswick.

² This is a common thickness for interlayer dielectrics.

[2-5,8,12,17,29-32,39,43,44,51,56,61] without too strong a polarizability [3,17,51]. The amount of boron should be high to lower reflow temperature. Since BPSG films tend to instability when the composition exceeds roughly 4wt%B and 4wt%P [1,2,4,10,11,25,29,30,37,38,43,44,57], glasses of this composition are attractive for their ability to curb ionic transport, soften at low temperature and remain stable. Being of the most practical use, the composition of 4wt%B/4wt%P was chosen for study.

It is also useful to compare the gettering characteristics of BPSG films with known standards. Wafers coated with SiO₂ can give an accurate estimation of the total number of contaminant ions in a gate oxide, since small alkali ions (such as Na⁺ and K⁺) move freely in SiO₂. Thus, for a set of wafers all processed identically with the exception of the deposited film types, the SiO₂ samples can indicate the absolute number of mobile impurities¹ while the BPSG samples can be compared to this standard to determine how many of the ions were immobilized in the film.

It is also useful to get a measure of how well BPSG films getter relative to the standard passivation material, PSG, so that applications for each material can be identified. The amount of phosphorus in the film must be high for optimal gettering yet low enough to be stable. It is also preferable to make it equal to that of the BPSG films to make a comparison based only on the role of BPSG process parameters (not skewed by a P% mismatch). For these reasons a composition of 4wt%P was deemed suitable.

¹ It is assumed that ionic contamination will be virtually uniform over all wafers processed together. Care must be taken to minimize contamination during deposition of the SiO₂ film - this is the only differing step between sample types.

To assure that enough functional sample devices were available for testing over several contamination runs, a large group size was required. It was decided that at least 10 wafers of each type of film would be produced, so three lots of 20 wafers¹ were fabricated. To examine the MOS structures in more detail, it was decided that the end wafers of the initial two lots would be pulled at intermediate steps of formation. This left fifty-six wafers as candidates for film deposition.

With the above criteria in mind, the sample groups chosen for this research consist of three experimental and two control sets as follows :

- BPSG with 1:1 oxy:hyd ratio; 4wt%B/4wt%P; 12 wafers
- BPSG with 2:1 oxy:hyd ratio, 4wt%B/4wt%P; 12 wafers
- BPSG with 3:1 oxy:hyd ratio, 4wt%B/4wt%P; 12 wafers
- SiO₂; 10 wafers
- PSG of 4wt%P; 10 wafers

3.2 Method of Preparing the Test Wafers :

The goal of wafer preparation was to produce all five sets of wafers so that they differed only in their passivation layer, but were otherwise identical. To achieve this objective the steps up to deposition of the overhead dielectric were executed in the same way for each wafer. Each deposited film was of the same thickness, and the phosphorus content of the PSG and BPSG films was chosen to be the same. Following film deposition the final process steps were carried out in the same way for each wafer.

¹ The laboratory capacity is twenty wafers per lot.

3.2.1 Pre-Deposition Processing :

Each sample wafer began as 2 Ω -cm p-type <100> silicon. The wafers were given an "RCA clean" [28] and 1 μ m thick field oxide was grown using an O₂/steam/O₂+HCl sequence¹, followed by a 40 minute anneal in N₂. Device wells were opened using BHF etch² until the Si surface was exposed. Following an RCA clean, 0.05 μ m gate oxides were grown in dry O₂, followed by a 40 minute, 1100°C N₂ anneal. Gate polysilicon of 0.4 μ m thickness was deposited onto the oxide using LPCVD, then gate patterns were formed by plasma etching. Source and drain diffusion windows were opened using BHF and the wafers were again RCA cleaned. Doping was done using predeposition of P accompanied by an O₂ drive-in to form 0.9 μ m deep source and drain wells. At this point the wafers were ready for deposition of the passivation layer.

3.2.2 Deposition of Dielectric Films :

BPSG: Process Technology Limited coated three sets of twelve wafers with BPSG, using oxygen:hydrides ratios of 1:1, 2:1 and 3:1 respectively. The target composition for each 0.5 μ m film was 4wt%B and 4wt%P. Depositions were done in an LPCVD reactor at low temperature, then were given a 30 minute 700°C N₂ densification. To open contact windows a BHF etch was used.

SiO₂: 10 wafers were covered with a 0.5 μ m layer of SiO₂, deposited using LOTOX³. Deposition was followed by a 15 minute, 1000°C N₂ anneal in a P drive-

¹ 10/180/30 minutes respectively. 2% HCl in O₂ was used to restrict Na⁺ content.

² "Buffered HydroFlouric Acid" - 9:1 NH₄F:HF

³ LOTOX is the PTL trade name for SiO₂ deposition in their LPCVD reactor.

in tube. Trace phosphorus was probably incorporated at this point, but of an inconsequential amount¹. Contact windows were then opened using BHF etch.

PSG: 10 wafers were coated with a 0.5 μm layer of PSG. The film was deposited using phosphorus-doped LOTOX, beginning with undoped oxide deposition and concluding with PSG deposition². The mixed-mode deposition has two advantages : it prevents the PSG from autodoping the source and drain wells during film reflow, and it allows a more tapered etch profile in the contact windows since the lower-doped film near the bottom of the wells etches more slowly than the heavier doped upper layers. Contact windows were etched (using BHF) immediately following application of the PSG. Next the wafers were given a 1.5 minute 1075°C N₂ anneal.

3.2.3 Post-Deposition Processing :

Following deposition of the passivation film and opening of the contact windows³, aluminum was electron-beam evaporated onto the top-sides of the wafer, to a thickness of 1 μm . The metal was then patterned using phosphoric acid etchant. Next, 0.5 μm of aluminum was electron-beam evaporated onto the backs of the wafers⁴ and annealed in H₂ for 20 minutes at 450°C.

Figure 5 depicts a MOS device formed using the above procedure.

1 The TBST results substantiate this assumption (see Results).

2 12 minutes of SiO₂; 13 minutes of PSG.

3 Immediately prior to Al evaporation the windows were cleared of unwanted SiO₂ growth using "BD etch".

4 For good electrical contact to the substrate during probing.

Figure 5 : MOS device Structure

3.3 Method of Contaminating SiO₂ with Sodium :

To allow a valid comparison of the gettering effectiveness of different materials it is important to keep the level of ionic contamination constant between the samples being compared. This level will vary due to differences in processing¹, exposures to impurities during handling and deviations in any contamination procedure used. As described in the preceding section, care was taken to process all of the test wafers in as similar a manner as possible to minimize that source of variation. Some variation occurred because the BPSG wafers were sent to a remote laboratory (PTL) for film deposition and thus were handled differently than the control samples (SiO₂ and PSG). TBS testing

¹ The wafers are subjected to 30-40 steps in which impurities can be incorporated.

of all wafers in their as-processed form showed that the variation was 1-2 orders of magnitude¹ over roughly 50 samples (see Results Figures 11 and 12).

Another source of inaccuracy is measurement error. The testing method chosen for this experiment (see section 3.4) had a characteristic error of measurement of approximately 2.5×10^8 ions/cm², which when compared with the nominal contamination level of 5×10^9 ions/cm² is significant. To extract a trend from data which contains measurement error within an order of magnitude of the quantity being measured demands a large sample size or alternate way to neutralize the effect of the error. An effective way to negate the effects of measurement error and permutations in as-processed impurity levels is to intentionally contaminate the samples [2,3,7,8,14,15,17,22,24,29,30,34,39,46,61,62]. At high impurity levels the error in measurement is insignificant relative to the mean. If the level of deliberate contamination is much higher than the as-processed count, this makes further comparison between samples more relevant, since all start from the same point. For these reasons, it was decided to intentionally contaminate the samples in as uniform a way as could be found. An optimal method would be consistent in the amount of sodium on each test area on a wafer and over each wafer in a Contamination Run. The methods that were pursued will be described now.

3.3.1 Aqueous Solution Method :

The first method of contamination attempted in this work used an aqueous solution as the source of impurities. In a plastic beaker a solution of DI water (250 ml) and NaCl (25 g) was stirred for 5 minutes, at which point no NaCl sediment was observed. A test wafer was immersed for 5 minutes in the

¹ As-processed levels of 10^9 - 10^{12} ions/cm² have been reported [8,17,22,44].

slowly stirring solution, held with Teflon tweezers. The wafer was then removed and blown dry with N₂. Once dry, the wafer was baked for 1 hour at 300°C to drive the adsorbed sodium into the wafer dielectric. After a cooling period (15 minutes) the wafer was rinsed with DI water, blown dry, rinsed again and dried again to remove surface salt deposits. At this point the wafer was placed on the prober chuck and TBS tests were done on four capacitors. The results showed mobile impurity levels from 4.1×10^{11} to 3.78×10^{12} ions/cm². The curves were not stable and repeat tests of the same area would result in marked variation of the readings¹. Though this method of contamination featured simple equipment, ease and brevity, the results showed that it failed to provide uniform contamination and therefore was not useful for doing comparisons between test areas or between wafers.

3.3.2 Evaporation Method :

Given the limitations of aqueous solution contamination, evaporation of sodium onto the wafer was tried to determine if it would be more effective. It offered the possibility of more even distribution of contaminant and the capacity for all five wafers to be coated simultaneously.

3.3.2.1 Procedure :

Preparation for evaporation involved these steps :

- (i) The filament was coated with NaCl (detailed in section 3.3.2.2).
- (ii) The inner surface of the bell jar was cleaned using 2-propanol.
- (iii) The evaporator water supply was opened, all valves and switches were placed in OFF or closed positions and AC power was switched on.

¹ The factor of difference between readings was as high as 2.6.

- (iv) The system was "roughed" to 0.2 Torr and then "backed"¹. The diffusion pump was allowed to run for >30 minutes to warm it up.

To perform evaporation the procedure was as follows :

- (1) The filament was affixed to the electrode bars, then the wafers and magnets were placed on the chuck, arranged as shown in Figure 6. The bell jar was then replaced.

Figure 6 : Position of Wafers During Evaporation

- (2) The bell jar was pumped down to pressures in the $6-17 \times 10^{-6}$ Torr range².
- (3) The filament power was turned on and the current adjusted until the filament radiated white light.
- (4) After 30 seconds of evaporation the power was turned OFF.

¹ "Roughing" is the higher pressure (to 0.2 Torr) pump-down of the system.
"Backing" is the pump-down of the diffusion pump exhaust line.

² These pressures produced mean free paths of 3 to 9m.

(5) The bell jar was brought to atmospheric pressure and then removed.

The wafers and filament were then removed, or the second filament was substituted and the wafers were re-positioned (see section 3.3.2.3).

When evaporation was complete the system was roughed, backed, the diffusion pump was allowed to cool for 30 minutes and then power and water supplies were shut off.

3.3.2.2 Filament Preparation :

A tungsten filament of conical-basket shape was selected¹ as the carrier for the contaminant. A plastic beaker was filled with 250 ml of DI water and 25 g of NaCl, then the beaker was covered and agitated for 5 minutes using a Corning PC-353 platform set at maximum stir speed. The filament was placed in the saline solution for 20 minutes, during which the stir speed was decreased in stages. The filament was then lifted from the water, dripped dry, then wrapped in dextilose paper and plastic for transport. This procedure was followed for all Contamination Runs, either as the sole method of filament charging or preliminary to further contamination.

Contamination Run#1 was carried out using the filament preparation described above. The post-contamination testing (see Figure 13) revealed contamination in the samples was increased by a factor of 20-100, but the levels fell short of the target of 10^{12} ions/cm² by a factor of 2-6. An apparent gradient was observed : areas nearest the filament had contamination levels 2-5 times higher than those furthest away.

¹ Tungsten usually contains small amounts of sodium and potassium. The basket shape offered a large capacity.

To reduce the effect of the gradient upon the amount of Na^+ that would reach the gate oxides of the samples studied, the dosage of NaCl on the filament was increased for subsequent contamination runs. To deposit a heavier dose of NaCl onto the samples for Contamination Run#2, some crystalline NaCl paste was placed on the filament after aqueous charging, and allowed to dry. The resultant contamination levels were in the range of $1\text{-}2 \times 10^{12}$ ions/cm² as desired, making any variation due to gradient a smaller percentage of the total contamination level. The process was repeated for subsequent Contamination Runs. A drawback of using NaCl paste was that some salt crystals would drop from the filament basket onto the chuck and wafers, causing disproportionate amounts of surface salt in those areas.

3.3.2.3 Double Evaporations :

An improvement to the NaCl evaporation procedure was introduced for Contamination Runs#4 and #5. To ensure that the evaporated NaCl film was uniform over the various wafer types, double evaporations were used, with the wafers re-positioned between evaporations. The two filaments were first charged in solution, then a small amount of NaCl paste was spread over the tungsten windings. Following the first evaporation the wafers were moved (see Figure 6), with the BPSG 1:1 and 2:1 wafers switched, the PSG and BPSG 3:1 wafers switched and the SiO_2 wafer rotated 180°. No gradient of impurity levels was noted for either of these contamination runs.

3.3.2.4 Sodium Drive-in :

After evaporation of sodium onto the wafer, a heating of the wafer is required to allow Na^+ to move from the surface into the underlying oxide

layers. Prior research has revealed that Na^+ moves freely in SiO_2 at temperatures above 100°C , with mobility increasing as temperature rises [7,12,17,22,31,34,35]. However, increasing temperature leads to destruction of contact metal and diffusion of dopants throughout the device. 300°C was chosen as a compromise, high enough to allow the sodium to move but low enough to keep the circuit structures stable. For Contamination Run#5 the temperature was reduced to 200°C .

To determine the optimal bake time an experiment was performed. Four similar wafers¹ were contaminated with sodium (using the evaporator) and then baked at 300°C for varying periods. The two wafers given a 1 hour drive-in showed impurity levels of $1\text{-}3 \times 10^9$ ions/cm² - equivalent to uncontaminated samples. The two wafers given a 3 hour drive-in measured impurity levels of $4\text{-}9 \times 10^9$ ions/cm². The first two wafers (1 hour bake) were then returned to the oven for a 16 hour drive-in. Post-bake testing showed impurity levels of $55\text{-}120 \times 10^9$ ions/cm². It was decided that 24 hour drive-ins would be used to ensure sodium permeation of the MOS dielectrics. The wafers were allowed to cool in an open oven for 30 minutes, then on a Kimwipe for an additional 15 minutes. The wafers were then placed in a wafer carrier until TBS tested.

3.4 Method of Measuring Mobile Ionic Impurity Concentration :

The "Temperature Bias Stress Test" (TBST)² was used to determine the concentration of mobile ionic impurities in the gate oxides of the MOS devices studied in this work. A description of the laboratory apparatus, measurement automation program, TBST procedure and choice of testing parameters follows.

¹ These wafers contained deposited SiO_2 films.

² A discussion of the TBST is included in section 2.7.5

3.4.1 Apparatus :

The equipment used to execute the TBS tests is illustrated in Figure 7.

Figure 7 : Apparatus

To contact the MOS capacitors two probes in a small probe station were used. The station had a chuck equipped with a vacuum port in the centre, a heating coil which was externally controlled, plumbing for cooling water, a thermocouple for temperature sensing and a connector for electrical contact to the wafer substrate. The probe station was enclosed in a lidded black box to

shield the wafers from airborne debris and ambient light. A vacuum pump was attached to the chuck port so that wafers were held firmly during probing. To aid placement of the probe tips a monoscope was used. A SIGNATONE S-1004 Thermal Controller was used to control thermal cycling of the probe chuck. The probes and chuck were connected to an HP4280A C-V meter for data acquisition, with the C-V meter controlled by an HP9816 microcomputer (via the HPIB bus). The computer had hard and soft disk drives for data storage. An HP7475A plotter was connected so that hard copies of the C-V plots could be made. A stopwatch was used to time the stress cycles.

3.4.2 Automation Program :

To satisfy the requirement of accurately determining the voltage shift between TBST curves a C-V meter with data storage capability was chosen. Given precise data acquisition, another requirement was to be able to derive the oxide capacitance, flatband capacitance and voltage shift at flatband (all needed to compute the number of mobile impurities) from the data in a reliable (and preferably quick) way. A further requirement was to perform the TBS testing in a consistent and rapid manner. Storage and graphical display of the data were also deemed useful. To fulfill all of the above criteria, a computer and plotter were added to the apparatus and a testing automation program was written. A brief description of the program sections and analysis routines follows. A more detailed description is included as Appendix A.

The MAIN MENU allows the user access to each of the set-up, testing, and output display and analysis program sections. Preparation for testing is done using the SET PARAMETERS and BIAS VOLTAGE menus. These menus show the

present settings of the test parameters, and allows the user to alter them as desired. These menus branch to the MAIN, RUN C-V TEST and PLOT menus.

Execution of the C-V test is handled by the RUN C-V TEST menu. The C-V meter is initialized with the test parameters and measurements commence. When measurement is complete the data are transferred to the computer, sorted to determine capacitance and voltage limits and then plotted on the screen. Graphs can be enhanced and manipulated through use of the PLOT menu. The user is given a number of data storage and display options, and can access the COMPUTE DEVICE PARAMETERS menu which is used for analysis.

To determine device properties, or the voltage shift between C-V curves, the COMPUTE DEVICE PARAMETERS menu is called. The CALCULATIONS option uses the C-V data and information on capacitor area, gate type, temperature and fixed charge to compute substrate type, oxide and inversion capacitances, oxide thickness, maximum depletion width, substrate doping density, bulk potential, flatband capacitance, and the theoretical and empirical flatband and threshold voltages. The VOLTAGE SHIFT option displays the voltage shift and number of mobile impurities responsible for such a shift at the calculated flatband capacitance. The routine also calculates the voltage shift and number of impurities at any capacitance value that the user enters.

The equations used in the CALCULATIONS module are based upon the depletion approximation developed by Grove [20]. The routine first derives material permittivities and thermal potential, then deduces the substrate doping type. Minimum and maximum capacitances are used for inversion and oxide capacitances respectively.

Oxide thickness is estimated using :

$$t_{ox} = (\epsilon_{ox} \cdot A_c) / C_{ox}$$

where ϵ_{ox} $\equiv$ oxide permittivity, A_c $\equiv$ capacitor area and C_{ox} $\equiv$ oxide capacitance.

The maximum depletion width is approximated using the simplification :

$$W_{max} = \epsilon_{si} \cdot A_c \cdot (1/C_{inv} - 1/C_{ox})$$

where ϵ_{si} $\equiv$ silicon permittivity and C_{inv} $\equiv$ inversion capacitance.

The substrate doping is then determined iteratively, using :

$$N = [4\kappa T \cdot \epsilon_{si} \cdot \text{LOG}(N/n_i)] / (q \cdot W_{max})^2$$

where N $\equiv$ doping density, κ $\equiv$ Boltzmann's constant, T $\equiv$ temperature,

n_i $\equiv$ intrinsic carrier density and q $\equiv$ electron charge.

The bulk potential is computed using :

$$\phi_b = [\kappa T \cdot \text{LOG}(N/n_i)] / q$$

The theoretical flatband capacitance is then determined using :

$$C_{fb} = \{(C_{ox})^{-1} + (A_c \cdot q \cdot [N \cdot \epsilon_{si} / \kappa T]^{0.5})^{-1}\}^{-1}$$

The program estimates empirical flatband voltage by interpolating the C-V curve at the theoretical flatband capacitance.

Theoretical flatband voltage is found using :

$$V_{fb} = \phi_m - (Q_f \cdot q \cdot A_c / C_{ox}) - \chi_{si} - E_g / 2 - P_t \cdot \phi_b$$

where ϕ_m $\equiv$ gate work function, Q_f $\equiv$ fixed charge, χ_{si} $\equiv$ silicon electron affinity, E_g $\equiv$ silicon energy bandgap, P_t $\equiv$ +1 for p-type Si, -1 for n-type Si.

This voltage is used to help calculate the theoretical threshold voltage :

$$V_{th} = V_{fb} + 2\phi_b + P_t \cdot (A_c / C_{ox}) \cdot [4\epsilon_{si} \cdot q \cdot N \cdot \phi_b]^{0.5}$$

The empirical threshold voltage is estimated by substituting the empirical flatband voltage into the above equation.

When the voltage shift at flatband capacitance (or any other point) is determined, the number of mobile impurities is computed assuming that the

voltage shift is caused by a sheet of charges moving from the gate-oxide boundary to the oxide-substrate boundary :

$$Q_{\text{imp}} = (\Delta V \cdot C_{\text{ox}}) / (q \cdot A_c) \quad ; \text{where } \Delta V \equiv \text{voltage shift.}$$

The program is menu-driven and has been written with the intent that the user should not require any documentation to use the program effectively. Throughout the program validity checks are done on parameter entries and integrity checks are performed on HP-IB transactions. Error-handler routines catch and attempt to remedy common faults while the program is running.

3.4.3 Temperature Bias Stress Test Procedure :

The following preparatory steps were done prior to testing :

- (i) The chuck, probes and tweezers were cleaned with 2-propanol.
- (ii) The C-V meter¹, microcomputer and hard drive, plotter, vacuum pump and thermal controller were turned on and the water supply opened.
- (iii) The time and temperature controls were set on the thermal controller.
- (iv) The wafer was placed on the chuck and the vacuum activated.
- (v) The "CVPLOTPLUS" program was loaded into the computer and RUN.

The double-cycle TBS test procedure was performed as follows :

- (1) Using the program, test parameters² were set and -5 V input as the bias.
- (2) The probe tips were positioned over the pads and lowered slowly, using the C-V meter to indicate contact. The probe box lid was then closed.
- (3) Thermal stressing was initiated; at 35°C the bias was enabled and the stopwatch started.

¹ The HP4280A was powered up at least 30 minutes prior to testing, to ensure precision in measurement.

² A discussion of key parameters is contained in section 3.4.4.

- (4) During the temperature rise and fall the probe tips were lifted and repositioned several times, to minimize pad damage.
- (5) When the wafer cooled to 35°C the bias was disabled and timing halted.
- (6) C-V measurements were then taken to complete the negative cycle.
- (7) Steps 1-6 were then repeated, using +5 V for bias.
- (8) Following data acquisition, the flatband voltage shift and corresponding impurity concentration were determined using the program.

All test results were saved and hard copies of the curves were plotted.

3.4.4 Determination of Test Parameters :

Prior to performing any testing, the test parameters had to be chosen. In the TBST the parameters consist of stress voltages, stress temperatures, stress times, C-V measurement temperature, measurement start, stop and step (incremental) voltages and speed of C-V measurements. It has been reported that the amount of sodium movement is exponentially dependent upon electric field and temperature, proportional to the square root of bias time and linearly related to the initial sodium concentration [17]. Since each parameter can influence the amount of sodium movement or the error in measurement, consideration was given to each.

Stress Voltages :

Accurate assessment of the number of drifting impurities which cause a flatband voltage shift depends upon moving the impurities from one oxide boundary to the other. In MOS devices with polysilicon gates¹ the sodium

¹ When an Al gate electrode is used the sodium tends to accumulate in the numerous gate/oxide border traps [7,8,13-15,22,24,32,35]

charge is generally distributed throughout the oxide with some pile-up near the interfaces [4,7,13-15,22,24,32,52]. The first step in the TBST is to negatively stress the MOS device in order to accumulate the mobile charge at the gate/oxide boundary. This can then be followed with positive stress to drive the mobile species to the oxide/silicon boundary¹.

5 V is the most common level used in MOS circuitry, so it was chosen as the stress bias. The oxide thickness for the sample capacitors was approximately 0.05 μm , so the electric field in the oxide was nominally 1 MV/cm. Electric fields of 0.5-2 MV/cm have been used extensively in other TBS testing [7,13-15,17,29,31,33,39,46,52,53,61]. It is desirable to use the same applied bias for both stress cycles so that ion drift dependence on electric field does not cause variation in the results. To meet the above criteria the stress voltages were set at -5 V and +5 V respectively.

Stress Temperatures :

Stress temperatures in the 140-300°C range have been used extensively in earlier work [7,13,15,17,29,31,33,35,39,46,51,52,61]. These temperatures are low enough not to alter the film structure in any significant way and to avoid dopant redistribution. To allow Na^+ ions to move without also shifting the K^+ distribution the temperature should be kept below 225°C [13]. It is desirable to use the same temperature for both stress cycles so that ion drift dependence on temperature does not cause variation in the results. With these criteria in mind, 200°C was selected as the stress temperature for both cycles.

¹ Measurements of the flatband shift in each stress cycle was done on several devices. The negative cycle accounted for roughly 20% of the total shift.

Stress Times :

The stress time at a given temperature must be chosen to allow sufficient drift of the mobile ions across the oxide. Many studies have successfully drifted sodium using 3-15 minutes at temperatures near 200°C [7,14,15,29,33,46,51,52,61]. The stress time should be short enough such that any polarizable complexes in the oxide would not go through the "slow" polarization process (less than 3 hours for a stress temperature of 200°C [51]). For these reasons 10 minutes was chosen as the stress time at 200°C, with the total stress time (including temperature rise and fall) being 15 minutes. The resulting temperature/time characteristic is illustrated in Figure 8.

Figure 8 : Thermal Profile for a TBST Cycle

Testing Temperatures :

Each C-V measurement set was done at approximately the same temperature to minimize any effect that thermal variation might have on the

samples¹. To restrict the sodium drift during measurements, a temperature at which sodium is relatively immobile was chosen : 20°C. Another consideration was whether to delay testing until the temperature had stabilized or to perform measurements while the temperature was still decreasing (measurement always follows a stress cycle). To perform the measurements during the falling edge of the temperature-time curve required each stress cycle plus measurement to be roughly 17 minutes in duration with the temperature varying 1-8°C during the 2 minutes needed to acquire a full C-V curve of data. To delay until the temperature stabilized to $\pm 1^\circ\text{C}/\text{minute}$ would require each stress cycle plus measurement to be 22 minutes in duration. The former option was chosen, with care taken to ensure that the temperature at which measurements began was the same for both stress cycles on a given sample. This way the temperature variation was the same for each set of curves being compared, with the benefit of saving considerable time².

Start, Stop and Step Voltages :

Measurement of capacitance was done at discrete levels of applied voltage. The endpoint voltages and total number of voltage points were kept the same for all samples to avoid any skew in voltage shift due to testing bias.

The test had to begin at a bias that was negative enough to accumulate the surface of all samples, even after a large shift due to movement of alkali ions during stress. The target concentration for contamination was 10^{12} ions/cm², which would result in a voltage shift of approximately -2.5 V (given the nominal gate capacitance of the sample capacitors). Allowing margin for

¹ Grove et al [21] have stated that varying the measurement temperature has the greatest influence on minority carrier equilibration.

² $450 \text{ samples} \times 2 \text{ cycles/sample} \times 0.833 \text{ hrs/cycle} = 75 \text{ hours.}$

contamination levels as high as 2.5×10^{12} ions/cm², the start voltage was chosen to be -6.5 V relative to the flatband voltage. The nominal flatband voltage of the devices was -1.5 V, so the start voltage was chosen to be -8 V.

To completely capture the falling edge of the C-V curve it was necessary to apply bias until inversion or deep depletion occurred. Preliminary studies showed that the nominal inversion voltage for uncontaminated samples was +0.2 V. This voltage could be pushed positive by mobile ions under negative stress, so a stop voltage of +2 V was chosen to give some margin.

To gauge the number of mobile impurities, the shift in voltage between two C-V curves must be accurately computed. Thus, it was necessary to choose a small step voltage between successive voltage points. The C-V characteristic drops roughly 20 pF over 2 V, so 50 mV steps were chosen to assure that no two capacitance measurements were separated by more than 1 pF and sufficient points were available to obtain a reliable assessment of the voltage shift.

The Speed of C-V Measurements :

An HP4280A C-V meter was used to acquire the C-V measurements. The capacitance measurement at each voltage point can be made at one of three speeds, "Slow", "Medium" and "Fast" [60]. The measurement speed affects the TBST in several ways.

- The slower the measurement speed, the better the charges in the substrate can remain in equilibrium with the instantaneous dc bias [21].
- The accuracy of the capacitance value is proportional to the length of time taken for measurement. "Slow" measurements are the most accurate.
- The applied voltage will cause mobile impurities to drift during the measurement time, giving a distorted C-V curve. The post-contamination

samples have larger quantities of oxide impurities and therefore are the most strongly affected. The measurement time will determine how strong an effect this mechanism has on the data, so "Fast" measurements are preferred.

- Measurements are subject to variations in ambient conditions (light, temperature, etc.) and disruption¹. "Fast" data sets are least affected.

"Medium" speed offers a compromise for all of these issues.

Accuracy is essential to the determination of flatband voltage shift, which is used to estimate the mobile ion impurity density in a sample. The flatband capacitance is used as the nominal comparison point to evaluate voltage shift, so the accuracy of capacitance readings is critical. In an uncontaminated sample the level of mobile impurities is typically 1-10 billion ions/cm², which is enough to cause a flatband voltage shift of only 2-20 mV. To assess the precision of measurement at different speeds, C-V measurements at each speed were done for a MOS capacitor and compared. Several tests of this kind were performed and from them these accuracies were estimated :

$$C_t - 0.2 \text{ pF} < \text{"Slow"} C_m < C_t + 0.3 \text{ pF}$$

$$C_t - 0.3 \text{ pF} < \text{"Medium"} C_m < C_t + 0.5 \text{ pF}$$

$$C_t - 0.4 \text{ pF} < \text{"Fast"} C_m < C_t + 1.6 \text{ pF}$$

where C_m represents the measured and C_t represents the true capacitance of the device. Examination of the data for this study showed negligible drift of the C-V curve as a function of speed. On the basis of the above information "Slow" speed was selected for further TBS testing.

¹ I lost many data sets due to vibration getting to the probe station. The usual causes were someone closing the lab door or someone walking heavily by!

3.4.5 Organization of the Test Samples :

To observe how consistent the contamination and gettering action was across each wafer, a number of areas on each wafer were examined. The central dice on each wafer were chosen as candidates, since these areas usually have the best consistency in fabricated structures and are highest in yield. Prior to any intentional contamination all wafers of each film type were tested for as-processed contamination at a minimum of four points.

It was intended that complete pre- and post-contamination TBS tests would be done on each MOS capacitor, however an unforeseen problem disqualified this in practice. After the wafers had been completely processed, extensive TBS testing was done. Early into the testing it was observed that the thermal cycling during a stress cycle caused physical movement of the wafer relative to the probes used to contact the gates. The combination of movement and probe pressure inflicted considerable damage upon the gate pad metal and occasionally upon the capacitor structures themselves. To remedy this problem, steps were taken to restrict wafer movement and minimize probe pressure. Several sheets of foam were inserted between the lab bench and the probe station to eliminate any movement from probe station vibration. To alleviate the thermal effect the probes were repeatedly lifted and repositioned¹ during heating and cooling. To decrease probe pressure, the probe tips were first centred over the pads and lowered until almost touching, then slowly lowered until contact was indicated by the C-V meter. These measures reduced the pad scoring a great deal, but not enough that a pad could

¹ This took about 5 seconds per probe and was done typically 6 times per cycle.

be used for the four cycles¹ required for complete pre- and post-contamination TBS testing. This limitation may not have arisen had the contact pads been of greater size (ie. 100 μm x 100 μm).

Given the limitations described above, pre- and post-contamination comparison was done using a different technique. Prior to TBS testing every test area in the central portion of the wafer was given a fast C-V measurement to determine which capacitors were functional. Prior to contamination 4-8 samples were TBS tested, each sample positionally separated from another by one die vertically and horizontally. After contamination the adjacent 4-8 samples were TBS tested. The resulting "chessboard" pattern is illustrated in Figure 9. If any of the central devices was previously found to be unfit then the nearest functional die was used instead. Having the test areas interleaved in this fashion makes for good correlation of pre- and post-contamination device characteristics, which should reflect in the test results.

To examine the consistency of gettering behaviour over several wafers, five contamination runs were performed. Following TBS testing of each wafer prior to contamination, five sets of five wafers² were grouped together for subsequent contamination. Each wafer in a group had a large number of good devices in the centre and a low standard deviation of contamination levels across the wafer. The testing pattern shown in Figure 9 was used for each wafer in each contamination run.

¹ Negative and positive bias stresser for each of two tests.

² One of each film type described in section 3.1.

Figure 9 : Test Area Pattern

LEGEND :

- 1 : Pre-Contamination Test Area**
- 2 : Post-Contamination Test Area**
- a : Alternate Test Area**

3.5 Statistical Analysis :

For each wafer/contamination combination the TBS test results were grouped and the distribution of mobile impurities was estimated using the mean and standard deviation (see details below). The difference between the means was used as an indication of the gettering effectiveness for each film. A statistical comparison of means was used to determine whether observed differences were significant at a chosen confidence level.

The flatband voltage shifts and impurity concentration levels were spread over several orders of magnitude, with the natural logarithms of the data points having an approximately normal distribution (see Figure 19).

Thus, the derivation of means and standard deviations was done using the natural logarithms of the measurements. The following formulae were used :

$$\begin{aligned}\text{Sample Mean : } \mu &= \frac{(\sum \ln(x_i))/n}{c} & i = 1 \text{ to } n \\ \text{Sample Variance : } \sigma^2 &= \frac{[\sum (\ln(x_i) - \ln(\mu))^2]/(n-1)}{c} & i = 1 \text{ to } n\end{aligned}$$

where x_i represents the flatband voltage or impurity concentration for sample#i and n is the number of samples. (The sample standard deviation is the square root of the variance).

It was assumed that the contaminant quantities were normally distributed, but since the sample sizes in this project were 4-8 points per grouping (except for pre-contamination testing), the Student-t distribution was used to do statistical analysis of means [41].

To evaluate whether the difference between means was statistically significant at a given confidence level the following equations were used [41] :

$$\begin{aligned}t &= (\mu_1 - \mu_2) / s_{\mu_1 - \mu_2} & \text{using :} \\ s_{\mu_1 - \mu_2}^2 &= [\sum (x_1 - \mu_1)^2 + \sum (x_2 - \mu_2)^2] \cdot [n_1 + n_2] / [n_1 \cdot n_2 \cdot (n_1 + n_2 - 2)]\end{aligned}$$

where μ_1 and μ_2 are the sample means, $s_{\mu_1 - \mu_2}$ is the "pooled" sample standard deviation, n_1 and n_2 are the sample sizes, and x_1 and x_2 are sample values. If "t" exceeds the value derived from the Student-t distribution for the chosen confidence level¹ then the difference between means is statistically significant. In this work confidence levels of 95, 98 and 99% were used.

¹ The values used in this work are copied from reference [41].

4.0 Results

This section presents the results of the Temperature Bias Stress Testing, grouped by contamination run. These measurements are discussed in the Analysis chapter.

A scaled replica of a TBST graph is illustrated in Figure 10. The program used to perform C-V measurement for TBS testing is detailed in Appendix A.

4.1 Pre-Contamination TBST Results :

Figure 11 shows the distribution of flatband voltage shifts, organized by film type. The data are separated into groups on a logarithmic scale in order to represent several orders of magnitude of variation.

Figure 12 exhibits the flatband shift measurements in terms of equivalent number of impurities transported across the oxide. The observed variation is somewhat lower than that reported in previous studies [8,17,22,44]. Some of the shift in the doped-oxide film samples is attributable to polarization effects (see section 5.1.2.3). Measurement error contributes less than $\pm 10^9$ ions/cm² variation to the data.

4.2 Contamination Run#1 :

The pre- and post-contamination TBST measurements for Contamination Run#1 are depicted in Figure 13. A double-column graph type with a logarithmic y-axis is used so a comparison of impurity concentration levels (pre- and post-contamination) can be done for each wafer and between wafer types. Note that "Sample Number" refers to the sequence of testing and not to specific test areas (ie. pre- and post-contamination Sample#n is not the same

test area). The difference between pre- and post-contamination data demonstrates that mobile impurities are present.

4.3 Contamination Run#2 :

Figure 14 portrays the test results for Contamination Run#2. The high degree of change in impurity levels is evidence of the strong NaCl dose evaporated onto the wafers.

4.4 Contamination Run#3 :

A heavy NaCl film was successfully evaporated in Contamination Run#3. The test results are presented in Figure 15.

4.5 Contamination Run#4 :

In order to increase the statistical confidence of the results, the sample size was doubled. Two evaporations were used to guarantee a heavy film of NaCl. To obtain a uniform layer of NaCl the wafers were re-positioned after the first evaporation (see section 3.3.2.3). Figure 16 depicts the measurements taken following Contamination Run#4.

4.6 Contamination Run#5 :

The measurements for the final contamination run are demonstrated in Figure 17. Contamination was done using two evaporations to deliver a heavy, uniform dose of NaCl. The larger sample size was used for this Run also.

The mean impurity levels for each Contamination Run are illustrated in Figure 18.

Figure 10 : TBST Graph

Figure 11 : Pre-Contamination Flatband Voltage Shift Distribution

Figure 12 : Pre-Contamination TBST Results

Figure 13 : TBST Results - Contamination Run#1

Figure 14 : TBST Results - Contamination Run#2

Figure 15 : TBST Results - Contamination Run#3

Figure 16 : TBST Results - Contamination Run#4

Figure 17 : TBST Results - Contamination Run#5

Figure 18 : TBST Results - Synopsis

5.0 Analysis

This chapter includes a discussion of the test results and explanations are proposed for the observed phenomena.

5.1 Pre-Contamination Characteristics :

5.1.1 Flatband Shift :

The distribution of flatband voltage shifts that is shown in Figure 11 contains some interesting trends. The flatband voltage shifts for the SiO₂ control samples approximate a normal distribution, with a mean¹ of 5.2 mV. The BPSG 1:1, 2:1 and 3:1 films approximate a broader normal distribution with higher means - 8.9, 5.6 and 8.4 mV respectively. The PSG films have a mean of 19.3 mV. The sample sizes for these distributions range from 45 to 52, so the larger voltage shifts for the doped-film samples appear to have statistical significance. This will be confirmed in the next section.

5.1.2 Impurity Profiles :

The pre-contamination TBST results presented in Figure 12 show that there is roughly 2 orders of magnitude variation in equivalent impurity levels. The natural logarithm of the impurity concentrations are distributed as shown in Figure 19. The data approximates a normal distribution, thus logarithms have been used in the statistical analysis of the results. The magnitude and variation of the Na⁺ concentration is moderately lower than that reported elsewhere [8,17,22,44].

¹ The means listed in this paragraph are logarithmically weighted (see 3.5 and 5.1.2).

Figure 19 : Distribution of the Natural Logarithms of Impurity Concentrations

The differences in means between the SiO₂ control samples and the other samples were analyzed at a 98% statistical confidence level. The disagreement was found to be statistically significant for the 1:1, 3:1 and PSG samples. The contrast between the SiO₂ and PSG samples is striking, particularly since these samples were most similar in their fabrication and handling. The possible causes of disagreement are measurement error, different levels of mobile or immobile oxide charges, and oxide polarization.

Measurement Error :

The characteristic error for voltage in the TBST is roughly 1 mV, which when compared to the measurement data is somewhat significant. However, the large sample sizes (45-52 points) for each of the glass types tends to filter deviations due to this error. The disparity between the means of the SiO₂ and PSG data is at least 7 mV (with a 98% confidence level). It is therefore improbable that the source of deviance is due to measurement error.

Oxide Charges :

Immobile oxide charges are almost certainly not the cause of the difference in voltage shifts, since they would shift the negative- and positive-stress curves a like amount, and therefore their influence would be negated. The wafers went through several high temperature treatments (oxidation, densification, reflow, Na⁺ drive-in), any of which should have minimized fast surface states and annealed out radiation-induced charge [20]. Of note :

- The fixed surface-state charge is a function of substrate orientation, oxidation and annealing conditions, all of which are the same for all of the samples. It is not a function of oxide thickness, applied bias or other conditions which lead to motion of sodium ions in the oxide [20].
- Differences in fast surface states are an improbable explanation, since the processing for the samples was virtually identical and all samples went through similar elevated (>500°C) temperature steps. Variations in fast surface state density would be evidenced by dissimilar shapes of C-V curves, which was not observed.
- Processing, testing and storage of the samples involved no known irradiation and testing was done in a shielded metal box.

It is possible that during the PSG formation step¹ the wafers were exposed to sodium at a significant level. However, PSG has been shown to provide virtually complete gettering of sodium at low and moderate levels of contamination [2-4,8,12,17,27,30-32,39,51,56,58,59,61] so the level would have to be large to cause the excess flatband shifts observed. Such evidence suggests that mobile impurities are rarely worse in a PSG passivated film than in an

¹ For other fabrication and testing steps the SiO₂ and PSG wafers were handled alike.

undoped glass. No other reports of contamination during PSG deposition were noted by other users of the same facilities, so a substantial mismatch of pre-contamination sodium levels is viewed as doubtful.

Polarization :

The excess flatband voltage shifts could be due to a quantity of P_2O_5 (or certain other oxidized dopants) in the gate oxide polarizing under the stress bias. Previous research [1-3,17,29,33,51,58] has demonstrated polarization to be prevalent in P-doped oxides when electrothermally stressed, and the probable mechanism has been identified (see Figure 2). The amount of polarization depends upon the concentration of polarizable complexes in the glass, applied electric field and bias time. The gate oxides in this study have no deliberate doping, but trace amounts of P (and B) are incorporated during fabrication. The gate oxide begins as thermally grown SiO_2 with a thickness of 500 Å; in subsequent steps dopants are incorporated in the oxide as follows:

- Phosphorus enters the oxide during pre-deposition and drive-in of the source and drain junctions and gate, densification, flow, reflow, and Na^+ drive-in.
- B and P diffuse into the silica from adjacent BPSG/PSG during high temperature steps.
- Substrate B moves into the oxide during growth and heating steps.

The dopant which becomes part of the gate oxide will react with the existing material to form P_2O_5 (and B_2O_3), which can be polarized in response to an applied bias; the amount being enhanced by elevated temperature. The quantity of P (and B) that finds its way into the oxide is minute, such that the electronic effect of these species is also small. The impurities near the gate

electrode will have little effect upon the surface charge because of their distance from the substrate. The dopants of concern are those near the surface and the various molecules near the sidewalls.

The TBST parameters in this work were chosen to allow saturation of "fast" polarization and no "slow" polarization. The model of Snow & Deal [51] can be used to estimate the amount of polarizable dopant in the oxide using the following equation :

$$\Delta V_{fb} = -(K_o x_g \chi_p V) / \{K_g [(K_g + \chi_p) x_o + K_o x_g]\}$$

where K_o and K_g represent the dielectric constants of the glass and oxide layers, x_g and x_o are the thicknesses of the glass and oxide layers, χ_p is the polarizability of the glass and V is the applied bias. [51]. Assuming that $K_o = K_g$, $x_o = 500 \text{ \AA}$ and $\chi_p = 0.75^1$ and using $V = 10 \text{ V}^2$ the equation above can be used to find the depth of polarizable glass that could cause the observed shifts. Most of the voltage shifts for BPSG and PSG samples ranged from 0-20 mV (see Figure 11). The above equation suggests that an equivalent layer of PSG 0-6 $\text{\AA}$ thick would be responsible for the observed shifts; this corresponds to roughly 1 dipole length for B_2O_3 or P_2O_5 .

If P_2O_5 structures contribute a polarization shift they should also provide a moderate gettering action. Evidence of this hypothesis would be an inverse relationship between the pre- and post-contamination flatband voltage shifts, or equivalent number of impurities in each case³. The relationship between these variables is plotted in Figure 20 for each of the Contamination Runs (designated by "CR#n").

¹ This value assumes PSG as examined in [51].

² Polarization should shift flatband by the same magnitude in both stress cycles.

³ Equivalent impurity level is superior, for it corrects for oxide thickness variation.

Figure 20 : Pre-/Post-Contamination Relationship in BPSG and PSG Samples :

included in Figure 20 are closest-fit lines for each of the Contamination Runs. In all data sets there is an inverse relationship between the pre- and post-contamination mean impurity levels, with the slope of the line roughly dependent upon the amount of deposited sodium¹. The correlation between these levels supports the proposal that polarizable gettering species are responsible for much of the pre-contamination flatband voltage shift.

The assumption that the observed shift (in the PSG and BPSG samples) is due to polarization appears to be reasonable. In subsequent analysis the post-contamination data will be corrected to eliminate this shift, in order to focus on the shift caused by mobile sodium (as detailed in the next section).

¹ The impurity level means on the SiO₂ samples were (in order of CR#; $\times 10^9$ ions/cm²): 353, 1401, 867, 707, 1168

5.2 Comparison of BPSG and SiO₂ Samples :

For each of the Contamination Runs the mobile ionic impurity concentration in the SiO₂ control samples was several orders of magnitude higher after contamination. The mean contamination increase for each of the five Runs was 347, 1399, 867, 706 and 1166 $\times 10^9$ ions/cm² respectively. In all Contamination Runs the increase was much lower in BPSG and PSG film samples, typically by more than an order of magnitude. Statistical analysis of the differences in contamination levels between the SiO₂ sample groups and the other film groups showed that in all but one of the fifty comparisons the difference was statistically significant at a confidence level above 99%. All of the doped-glass samples proved far superior to SiO₂ in gettering mobile Na⁺.

A figure of merit was developed for assessing the gettering performance of these dielectrics - the percentage of mobile ions that are frozen by the passivation film. This "Getter%" is obtained by dividing the number of mobile ions from intentional contamination by the total number of sodium ions which would have gotten into the gate oxide if the passivation film were undoped. The numerator is computed by subtracting the mean of the pre-contamination data from the mean of the post-contamination results¹. The denominator is derived the same way, but using the SiO₂ data². A table of Getter% for each glass type and Contamination Run is displayed in Figure 21.

¹ Doing so also corrects for polarization, as it should be equal for both pre- and post-contamination stressing.

² The pre-contamination level is subtracted so the numerator/denominator ratio relates only to the intentional contamination and not as-processed levels.

Figure 21 : Getter Effectiveness as "Getter%"

	CR#1	CR#2	CR#3	CR#4	CR#5	Wavg
BPSG 1:1	99.8	98.0	99.0	77.5	97.8	92.4
BPSG 2:1	79.7	88.6	85.0	89.9	79.0	84.5
BPSG 3:1	49.8	97.1	85.5	93.2	92.3	86.2
PSG	93.1	99.8	79.7	99.0	91.3	93.1

Effectiveness is shown as percentage of total Na⁺ dose that is immobilized.
 "CR#" refers to Contamination Run#: "Wavg" is the weighted average%

The weighted average is calculated using :

$$\text{Wavg} = [\sum \{\text{Getter\%}(j) \cdot \text{\#samples}(j)\}] / [\sum \text{\#samples}(j)] \quad j = 1 \text{ to } 5$$

None of the films gettered all of the mobile sodium, but a third of the BPSG samples gettered to within 3% of all impurities. From the Getter% data it is clear that all BPSG films significantly depress the number of sodium ions which get into the gate oxide and remain mobile. Any of these glasses should substantially stabilize the underlying device in the presence of considerable Na⁺ contamination (up to 10¹² ions/cm²).

5.3 Comparison of BPSG and PSG Samples :

As expected, the PSG film samples were very effective getters of sodium. The data in Figure 21 reveal that typically more than 93% of the Na⁺ ions were stopped by this glass. The weighted average getter% was highest for PSG, barely ahead of the BPSG 1:1 layer; further analysis confirms the similarity of these films. In Figure 22 the mean Na⁺ concentrations after contamination are compared for BPSG and PSG glassed samples. The superior film in each case is listed, along with a comment on whether the difference is statistically significant at a confidence level of 95%.

Figure 22 : Comparison of BPSG and PSG Film Samples

The table below states which of the sample groups showed superior gettering for each Contamination Run# and whether the difference between means is significant at a 95% confidence level.

	CR#1	CR#2	CR#3	CR#4	CR#5
BPSG 1:1 vs PSG	1:1 / yes	PSG / no	1:1 / yes	PSG / yes	1:1 / yes
BPSG 2:1 vs PSG	PSG / yes	PSG / yes	2:1 / yes	PSG / yes	PSG / yes
BPSG 3:1 vs PSG	PSG / yes	PSG / yes	3:1 / no	PSG / yes	3:1 / no

The BPSG 1:1 samples exhibited noticeably better gettering performance than the PSG samples in three of the Contamination Runs, the PSG was superior in one Run and the samples were similar in the other Run. Thus the BPSG 1:1 films used in this work are at least as effective as the PSG films of similar P content, and possibly better.

The BPSG 2:1 samples were poorer getters of mobile sodium than the PSG films in four of the five Runs, with PSG inferior in the other. The one situation in which PSG is worse was based on only four measurements and appears to be an anomaly.

The BPSG 3:1 film samples were inferior to the PSG samples in three of the Runs and similar to them in the other two Runs. The results suggest that PSG is a better sodium getter by a moderate amount.

Although PSG was the most effective getter, it also had the greatest apparent polarization, which in itself changes the surface potential. Since alkali impurity levels in an unintentionally contaminated device will be low, the polarization of the oxide may cause a greater flatband shift than the ions

that remain mobile. It appears that the BPSG 1:1 films are as effective or better at gettering sodium, demonstrate less polarization¹, and flow at much lower temperatures than PSG, making them good substitutes for PSG as an interlayer dielectric or passivation film.

5.4 Comparison of BPSG Types :

5.4.1 Gettering :

Though all BPSG films provided strong gettering, there are differences between the glasses. The films are compared for each Run in Figure 23.

Figure 23 : Comparison of BPSG Sample Groups

The table below states which of the sample groups showed superior gettering for each Contamination Run# and whether the difference between means is significant at a 95% confidence level.

	CR#1	CR#2	CR#3	CR#4	CR#5
BPSG 1:1 vs 2:1	1:1 / yes	1:1 / yes	1:1 / yes	2:1 / no	1:1 / yes
BPSG 1:1 vs 3:1	1:1 / yes	1:1 / no	1:1 / no	3:1 / yes	1:1 / yes
BPSG 2:1 vs 3:1	2:1 / yes	3:1 / yes	3:1 / no	3:1 / no	3:1 / yes

The BPSG films with a 1:1 oxygen:hydrides ratio were superior to those formed with a 2:1 ratio in four of the five Runs, with the samples being similar in the other Run. Figure 21 shows that the 1:1 ratio films typically immobilize 8% more Na⁺ than the 2:1 ratio ones. Clearly the 1:1 glasses are better getters.

The comparison between the 1:1 ratio samples and their 3:1 counterparts again shows a dominance of 1:1 films in gettering effectiveness. The 3:1 samples excel in one Run but the 1:1 samples were better or similar in the remaining Runs. The weighted average of Getter% for the 1:1 samples shows

¹ The ratio of BPSG:PSG mean pre-contamination flatband voltage shifts is 0.46.

roughly 6% more impurities trapped than for the 3:1 samples (see Figure 21).

The BPSG 3:1 film samples were superior to the 2:1 films in two of the Runs, inferior in one and similar in two. The weighted average Getter% for the 3:1 films is approximately 2% higher than that of the 2:1 films, as seen in Figure 21. The evidence indicates a slight superiority of 3:1 ratio glasses.

The results show that the gettering effectiveness of these films is a weak function of the oxygen:hydrides ratio employed in their formation. For films with similar growth rates, flow properties, dielectric strength, residual stress and other qualities an oxygen:hydrides ratio of 1:1 is preferred.

5.4.2 Film Composition :

Film etch rate is commonly used to evaluate the composition of BPSG films [4,5,17,27,29,30,48]. Using a buffered hydrofluoric acid etch of 9:1 $\text{NH}_4\text{F}:\text{HF}$, the etch rate of each glass sample¹ (as densified) was calculated. The details appear in Figure 24.

Figure 24 : Etch Rates of BPSG Films

¹ The etch rates of SiO_2 and PSG samples averaged 730 and 1290 Å/min respectively.

The graph demonstrates the similarity of the 2:1 and 3:1 ratio films, and the distinctive composition of the 1:1 ratio glass. The etch rates indicate that either the boron content of the 1:1 samples is higher than in the other samples, or the phosphorus content of the 1:1 silica is lower, or both. The pre-contamination data furnish some evidence that decreasing P content is not the reason: the mean flatband voltage shifts (principally due to P_2O_5 polarization) for each of the BPSG groups are within a few millivolts of each other. Kern and Schnable have reported [29] that boron content rises with decreasing oxygen:hydrides ratio for APCVD BPSG, and showed that the etch rate of 4wt%P BPSG halves when the boron content rises from 4wt% to 5wt%. Also, decreasing P content worsens gettering, and the 1:1 samples were the best getters. It is reasoned that the lower etch rate is due to higher B content in the BPSG films formed with a 1:1 oxygen:hydrides ratio.

The variations in etch rate are probably not caused by differences in the chemical state of the phosphorus in the glass. All films had a target P content of 4wt%, with the phosphorus initially in any of the PH_3 , P_2O_3 or P_2O_5 molecular forms. After the 30 minute 700°C densification step in N_2 the PH_3 and P_2O_3 complexes should have converted to P_2O_5 or evaporated out [23,57]. The high etch rates of 2:1 and 3:1 samples indicates that the P content after densification remained high. It is possible that B was lost in densification, for the relatively small atomic radius and low ionization potential of B allow it to move easily within the SiO_2 strata. Local boron depletion at glass surface has been observed in other work [4,5,27].

An intriguing possibility is that B_2O_3 polyhedra may trap sodium, and that the 1:1 ratio glasses are more effective getters because of this. Studies of

BPSG gettering have shown that it is as good or better than PSG [29,30], though it is widely assumed that gettering is a function of the P_2O_5 in the glass and not B_2O_3 [4,11,29,30,43]. However, Avigal [2] has shown that borosilicate glasses were as effective at gettering as BPSG and PSG films¹, implying that gettering is sensitive to properties of the glass other than the P_2O_5 content. Two proposed gettering mechanisms for B_2O_3 are illustrated in Figure 25.

Figure 25 : Proposed Gettering Mechanisms for B_2O_3

¹ PECVD was used for BSG and BPSG samples; APCVD was used for PSG samples.

Part a) of Figure 25 shows a representation of the SiO_2 structure. Part b) depicts the effect of boron atoms substituting for Si atoms in SiO_4^{4-} tetrahedra. A BO_3^{3-} polyhedron results [50,59], with one non-bridging oxygen (having a negative charge), which can capture a sodium cation. Gettering for B_2O_3 in a ring structure in the SiO_2 network is depicted in part c). Non-bridging oxygen sites are created along the ring periphery because the B_2O_3 polyhedra have no available bonding electrons for the adjacent SiO_4^{4-} tetrahedra.

Though the silica structure is less regular than the above depiction, considerable non-bridging oxygen sites should be caused by substitutional boron. At 4wt%B and 4wt% P the ratio of Si:B atoms in doped- SiO_2 will be approximately 3.7:1 (the ratio of Si:P atoms is roughly 10.7:1). Thus, many cation traps should be created when boron is added to the film.

5.5 Comparison of Results with Previous Research :

The examination of BPSG films formed at low oxygen:hydrides ratios that motivated this project indicated that their gettering performance was poor [9]. The results obtained in the present study differ with that previous set. There is no strong evidence to show that the gettering properties of LPCVD BPSG films deteriorate at low oxygen:hydrides ratios or are improved at high ratios. A different trend is indicated in this work : that gettering is excellent at low oxygen:hydrides ratios, less effective at high levels and least effective (but still good) at median ratios. Possible explanations for the discrepancy between the results from PTL's client and those presented here include differences in dopant concentrations, polarization, measurement error, or other compounds in the films. Measurement error is a doubtful cause since most of these results are statistically significant at a 95% confidence level. There is no evidence for

or against unexpected compounds, so focus is given to the other candidates.

Dopant Concentrations :

Previous research has shown that gettering efficiency is proportional to dopant content [17]. It is possible that the BPSG films studied by PTL's client had low quantities of B and P (which has a strong Na^+ trapping mechanism). Low oxygen:hydrides ratios suppress P incorporation in APCVD BPSG [29]; a similar effect may occur in LPCVD BPSG. At low ratios the amount of phosphorus incorporated as P_2O_5 may be as low as 75% of the total [36]. Other P-compounds (and B) can be lost during densification [36,49,54] so the dopant quantity in the final glass structure could have been significantly lower than expected. The BPSG films used in the present work contained relatively high dopant levels (4wt%B and 4wt%P) and were effective sodium getters.

Polarization :

Analysis of the BPSG films prior to intentional contamination showed that polarization was a probable cause for much of the flatband voltage shift. It is plausible that the MOS devices under the BPSG in the previous study had noticeable shifts due to polarization, which were interpreted as ionic shifts in the oxide. Polarization is often overlooked in MOS capacitor testing.

6.0 Conclusions

The results of this research show that borophosphosilicate glass of substantial dopant content (near 4wt%B/4wt%P) is an effective sodium getter when formed in an LPCVD reactor with oxygen:hydrides ratios between 1:1 and 3:1. Citing the "Getter%" figure of merit developed in this work, all BPSG films were observed to immobilize 85% or more of all alkali impurities in conditions of heavy contamination and prolonged high temperature exposure. As much as 99.8% of mobile impurities were trapped in some test cases.

The hypothesis that low oxygen:hydrides ratios inhibit formation of gettering sites is not supported by the TBST results; an opposing trend is indicated. The BPSG films formed at a low oxygen:hydrides ratio (1:1) were the most capable Na^+ getters, surpassing other BPSG and PSG samples in effectiveness. The 1:1 samples were also noted to be different in composition from the 2:1 and 3:1 films. The lower quantity of oxygen in the reaction may have encouraged boron incorporation, as evidenced by the slower etch rate of the 1:1 films compared to the 2:1 and 3:1 glasses.

The superior gettering ability of the 1:1 films, coupled with the apparently higher B content (and possibly lower P content) suggests that B_2O_3 has a role in sodium trapping. Two gettering mechanisms for B_2O_3 are proposed here, in which the substitution of B for Si in an SiO_4^{4-} tetrahedron, or the presence of B_2O_3 rings adjacent to SiO_4^{4-} tetrahedra, result in non-bridging oxygen which can trap cations. Though this effect is not as strong as for P_2O_5 gettering, it does suggest that an optimal BPSG film can have more boron and less phosphorus to achieve the requirements of lowest flow temperature with adequate electrical stability.

Testing of devices prior to intentional contamination revealed that polarization is apparent in the gate oxides when BPSG or PSG is used as an interlevel dielectric. Devices with BPSG overcoats had 1-1.5 times more flatband voltage shift than devices with SiO_2 overhead, while those with PSG showed nearly 4 times greater shift. The trace amounts of P_2O_5 in the gate oxide serve to getter impurities but also polarize when electrically stressed. The inverse relationship between pre- and post-contamination equivalent impurity levels supports the proposal that polarization of P_2O_5 is responsible for the pre-contamination shift. Analysis of polarization showed that a monolayer of P_2O_5 would account for the observed instability. It is possible that the electrical effect of polarization was interpreted as that of ionic drift in the study that motivated this research project.

The Temperature Bias Stress Test was used to obtain information about the movement of mobile ions in the MOS gate oxides. The implementation of this test along with some display and device property derivation routines in an automatic test program made the execution of testing precise, consistent and straightforward. The statistical analysis of flatband voltage shifts (or equivalent impurity concentrations) was found to be most relevant when the natural logarithms were used.

LPCVD BPSG formed at a 1:1 oxygen:hydrides ratio with significant dopant content is a strong candidate to replace PSG as an interlevel dielectric or passivation layer. Such films should feature few particulates or defects, thickness and dopant uniformity, low residual stress, slow etch rate, low fusion temperature and effective gettering of mobile sodium.

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Appendix A: C-V Measurement Program

This program allows the user to perform C-V testing in a consistent, reliable and rapid manner. It offers graphical output and data analysis, can save and recall data and has many other features. A Hewlett-Packard HP9816 computer was used to control the TBS testing. The HP4280A C-V meter and HP7475A plotter were linked to the computer via the HP1B bus¹ as shown in Figure 7. The program is written in HP BASIC and is entitled "CVPLOTPLUS".

The program directs the user through equipment connection, test parameter entry, C-V measurement, graphic output and calculation of device properties through a set of inter-connected menus. The macro-structure of the program is depicted in Figure 26. From each menu the user can select special functions (such as setting the start voltage, normalizing graph axes, etc) or branch to another menu by pressing one of the function keys on the HP9816. Each menu screen displays the function key assignments and gives a synopsis of the options available. The intent is that the user should not require any documentation to effectively utilize the program.

Figure 26 : Program Structure

¹ HP1B addresses : C-V meter = 27, plotter = 05.

The routines which are used to prepare for testing are shown in Figure 27. When the program is loaded and "RUN" is pressed, an **INITIALIZATION** display appears on the screen describing the test equipment configuration. When the user has satisfied all of the conditions mentioned, a press of the <CONT> key causes the **MAIN MENU** to be displayed. Default settings for test parameters and device attributes are loaded into program registers from a data file entitled "CV_PARAM", which is also on the hard disk. From the **MAIN** menu the user can get to any of the other major menus or quit the program.

Figure 27 : Test Preparation Routines

The **SET PARAMETERS MENU** provides the user with the ability to alter any of the testing parameters. The menu screen displays start, stop, step and bias voltages, delay and hold times, sweep mode, measurement speed and

the number of test points. The function keys allow access to seven subroutines, each of which changes a particular parameter. This menu can exit to the MAIN, RUN C-V TEST or BIAS VOLTAGE menus.

The START VOLTAGE, STOP VOLTAGE, DELAY TIME, HOLD TIME and MEAS SPEED routines display the present setting and then prompt the user for a new value. The input is checked for validity¹ then the routine returns to the SET PARAMETERS menu. The STEP VOLTAGE code proceeds in a similar way, but does extra validity checks to ensure that the step voltage is consistent with the start and stop voltages and does not cause an excessive number of test points². The SWEEP MODE option invites the user to select either a single sweep (from start-stop voltage) or a double sweep (a start-stop-start voltage sequence). The number of test points is found and the user notified if the number is excessive.

The BIAS VOLTAGE MENU is used to set a voltage to be applied to the device under test and to start or stop the application of the bias. The menu screen shows the present bias setting and function key assignments. This menu can exit to the SET PARAMETERS, C-V TEST, PLOT or MAIN menus.

The START BIAS option configures the C-V meter, sends the bias setting and enables the bias application. The user gets a message to confirm that the voltage is applied. STOP BIAS disables the bias, then displays a confirmation message. The CHANGE BIAS routine displays the present bias setting, then prompts the user for a new value which is checked for valid range³.

The program portions which are used to execute the testing, produce

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- 1 Allowable ranges are -100 V to +100 V, +.003 s to 650 s and 'F'(fast), 'M'(medium) or 'S'(slow). The routines will not return until a valid input is received.
 - 2 A maximum of 680 points are permitted. The routine will not return until a valid input is received.
 - 3 The allowable voltage range is -100 V to +100 V. The routine will not return until a valid input is received.

graphical output and do analysis of the data are shown in Figure 28.

Figure 28 : Testing, Output and Calculations Routines

The **RUN C-V TEST MENU** screen displays all of the present test parameter settings and defines the function key used to commence testing. From this menu the user can go to the **SET PARAMETERS**, **BIAS VOLTAGE**, **PLOT** or **MAIN** menus.

When the **START C-V TEST** key is pressed the program saves the present graph limits (C and V), configures the C-V meter for testing, calibrates the capacitance of the cable connecting the probe station to the meter and then writes all of the test parameters into the meter registers. The testing then begins and a function key is defined to abort the test if desired. When the C-V meter returns a message to the computer, the status is checked to determine whether the test succeeded. If no failure occurred¹ then the program reads all test data from the meter, determines the capacitance and voltage limits for the data² and then plots the resultant graph on the screen.

The graph plotting routine first clears the graph bit-map, then displays the generic graph structure, which includes a 10x10 background grid with accented and labelled axes, time and date of plot, test parameters and graph title. C-V curves are then printed in order of acquisition, with distinctive colours and line types (ie. solid, dashed) to delineate them. Samples of each line and its label are printed on the right side of each graph. Up to 10 curves are permitted on a single graph³. If an error occurs while plotting then an error-handling routine notifies the user of the problem and suggest possible remedies for the cause. When the user is ready to proceed a press of the <CONT>

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- 1 If the test failed then the user is notified and suggestions are made for remedying the cause of failure.
 - 2 All data points are examined to determine the minimum and maximum values of capacitance and voltage, these limits are compared with the limits for the rest of the graph lines and the graph limits are modified if required. When the limits are determined then a 10x10 background grid is created for the graph.
 - 3 If 10 curves are already on the graph then the program begins a new graph.

key brings up the PLOT MENU.

The **PLOT MENU** menu is used to produce graphical output of C-V data. The **PLOT** menu screen re-defines the function keys, allowing the user control over several aspects of the graph, plus the ability to get a paper plot, save or retrieve C-V data, or calculate device properties from the data. A brief discussion of each option follows. This menu exits to the **RUN C-V TEST** menu.

The **GRAPH TITLE** option allows a title (1-30 characters) to be printed at the top of the graph. The **LABEL C-V LINE** option allows a label (1-15 characters) to be attached to a given curve. The label and a sample of the line are printed at the right side of the graph. The **NORMALIZE CAP** routine scales all of the capacitance axes labels by the maximum measured capacitance. The axes title is also altered, listing "[C/Cmax]" as units. The **NEW GRAPH** function resets a number of graph parameters and clears the graph bit-map.

The **HARD COPY** code begins by checking for a valid communication link with a properly connected HP7475A plotter which is ready for service. If these conditions are met then the graph is written to the plotter¹. The **PLOT** menu is invoked as soon as the hard copy is completed. An example of a hard copy plot is shown in Figure 10 (see section 4.0).

The **AXES MENU** menu displays the present values of capacitance and voltage limits for the graph, and allows the user to change any of these values. After the user selects which of the limits to change, input of a new value is prompted. The entered value is examined to assure that it is reasonable² and consistent with its related limit ($C_{max} > C_{min}$; $V_{max} > V_{min}$). This menu exits to a

¹ If plotting fails then the user is notified, the type of error, plotter ID and status are displayed along with suggestions for remedying the cause of the problem.

² The allowable capacitance range is 0 to +1000 pF; voltage range is -100 V to +100 V. The routine will not return until a valid input is received.

routine which calculates new axes and grid values for the graph and then displays the graph, before returning to the PLOT menu.

The **DISC MENU** offers choices for storage and retrieval of data files. The options access either the hard or floppy disk drives and include saving the last C-V curve, recalling a C-V curve, and listing all files on the chosen disk. This menu exits to the PLOT menu.

The **SAVE** options require the user to input a name for the data file to be created, then it writes the file length and data points onto the selected disk. After successful creation of the file and transfer to disk, the user gets a confirmation message. The **RECALL** options require the user to input the name of the data file to be retrieved, from which it reads the file length and data points into program space. The limits of capacitance and voltage for the new data is compared with those of the present graph and the graph is adjusted if required. The user gets a confirmation message if there were no problems with the recall. The **LIST** options display the files in the chosen disk directory.

If any problem occurs during a disk operation an error-handling routine alerts the user and suggests possible cause.

The **COMPUTE DEVICE PARAMETERS MENU** screen displays the present settings for device area, gate type¹, temperature and fixed charge and defines function keys for various options. This menu can be used to input information about the device under test, to calculate the oxide thickness, substrate doping density, flatband and threshold voltages (theoretical and empirical), or to determine the voltage shift between two adjacent C-V curves at a given capacitance.

¹ Aluminum, n⁺polysilicon or p⁺polysilicon

The entry options for CAPACITOR AREA, GATE TYPE, TEMPERATURE and FIXED CHARGE each display the present setting for the parameter and prompt the user for a new value. The input is checked for validity¹ and then writes the value into the "CV_PARAM" data file. Each routine exits back to the COMPUTE DEVICE PARAMETERS menu.

Analysis of device properties is based on the depletion approximation MOS model developed by Grove [20]. The CALCULATIONS module begins by deriving material permittivities and thermal potential and then deduces the substrate doping type by comparing the capacitances at the minimum and maximum test voltages². The minimum measured capacitance is used to approximate the inversion capacitance. The maximum measured capacitance is used to approximate the oxide capacitance. The thickness of the oxide is estimated using :

$$t_{ox} = (\epsilon_{ox} \cdot A_c) / C_{ox}$$

where ϵ_{ox} = oxide permittivity, A_c = capacitor area and C_{ox} = oxide capacitance.

The maximum depletion width is approximated using the simplification :

$$W_{max} = \epsilon_{si} \cdot A_c \cdot (1/C_{inv} - 1/C_{ox})$$

where ϵ_{si} = silicon permittivity and C_{inv} = inversion capacitance.

The substrate doping is then determined iteratively³, using :

$$N = [4\kappa T \cdot \epsilon_{si} \cdot \text{LOG}(N/n_i)] / (q \cdot W_{max})^2$$

where N = doping density, κ = Boltzmann's constant, T = temperature,

n_i = intrinsic carrier density and q = electron charge.

The bulk potential is then computed using :

- 1 Capacitor area can be +1 μm^2 to +25 cm^2 ; gate type can be Al, p⁺polySi or n⁺polySi; temperature can be 0 to 1415 K; fixed charge can be +10⁸ to +10¹⁵ ions/cm².
- 2 If $C(V_{min}) > C(V_{max})$ then substrate is assumed to be p-type; otherwise it is assumed to be n-type.
- 3 Iteration ceases when successive calculations of N differ by less than 10⁹ /cm³.

$$\phi_b = [\kappa T \cdot \text{LOG}(N/n_i)]/q$$

The theoretical flatband capacitance is then determined using :

$$C_{fb} = \{ (C_{ox})^{-1} + (A_c \cdot q \cdot [N \cdot \epsilon_{si} / \kappa T]^{0.5})^{-1} \}^{-1}$$

The program then estimates the empirical flatband voltage by interpolating the C-V curve at the theoretical flatband capacitance.

The theoretical flatband voltage is computed using :

$$V_{fb} = \phi_m - (Q_f \cdot q \cdot A_c / C_{ox}) - \chi_{si} - E_g/2 - P_t \cdot \phi_b$$

where ϕ_m = gate work function, Q_f = fixed charge, χ_{si} = silicon electron affinity, E_g = silicon energy bandgap, P_t = process type (+1 for p-type Si, -1 for n-type Si). This voltage is used to calculate the theoretical threshold voltage :

$$V_{th} = V_{fb} + 2\phi_b + P_t \cdot (A_c / C_{ox}) \cdot [4\epsilon_{si} \cdot q \cdot N \cdot \phi_b]^{0.5}$$

The empirical threshold voltage is estimated by substituting the empirical flatband voltage into the above equation.

When the computations are complete the program displays the results. A press of the <CONT> key sends the user back to the COMPUTE DEVICE PARAMETERS menu.

The **VOLTAGE SHIFT** routine determines the voltage shift between two adjacent C-V curves and calculates the number of mobile ionic impurities that would be responsible for such a shift.

The code begins by checking that there is more than one line on the graph. If there is, the shift at the flatband capacitance is calculated and displayed, then the user is asked to input a capacitance at which the voltage shift is to be determined. Any number entered is checked to assure that it lies between the capacitance limits of the graph¹. Once a valid capacitance is received the routine searches for the test points nearest the input value on the

¹ If it's out of range the user is notified and prompted until a valid entry is received.

last C-V curve. An interpolation is then done between these two points to get the voltage corresponding to the input capacitance value. The line search and interpolation procedure is then repeated on the C-V curve preceding the last one. The interpolated voltages for the two lines are then differenced to determine the voltage shift. The number of mobile impurities is computed assuming that the voltage shift is caused by a sheet of such charges moving from the gate-oxide boundary to the oxide-substrate boundary :

$$Q_{imp} = (\Delta V \cdot C_{ox}) / (q \cdot A_c) \quad ; \text{where } \Delta V \equiv \text{voltage shift.}$$

The voltage shift and number of impurities are then displayed. When the user has examined the shift at a number of points a press of the <ENTER> key returns the program to the PLOT menu.

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