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ONE-DIMENSIONAL MODELLING
OF NON-RECTANGULAR IGFETS

by

Emil F. Girczyc

A thesis submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

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The undersigned recommend to the Faculty of Graduate Studies
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ABSTRACT

The drain characteristics of a non-rectangular IGFET operating in the triode and subthreshold regions are shown to be identical to those of a rectangular device of appropriate 'effective' aspect ratio. The effective aspect ratio of the device can be calculated by conformal mapping techniques, or by two-dimensional numerical methods. Experimental data are presented for IGFETs having a variety of non-rectangular configurations: these verify the 'scaling' results derived by the above analysis. A qualitative investigation of non-scaling aspects of device performance such as saturation drain conductance, gate capacitance, and small geometry effects is also performed. Finally, a systematic approach to the design of integrated circuit components containing non-rectangular IGFETs is formulated.

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LIST OF SYMBOLS

C_g	Gate capacitance of an IGFET
C_{ox}	Oxide capacitance
D	Diffusion coefficient
g_d	Drain conductance
$g_{d,sat}$	Saturation drain conductance
g_m	Transconductance
I_d	Drain current
$\underline{j}$	Surface current density
J	Current density
k	Boltzmann's constant
L	Length of a rectangular IGFET
L_e	Effective length of a non-rectangular IGFET
N_b	Number of squares added by the corner region of a bent IGFET
N_e	Effective number of squares of a bent IGFET
N_r	Number of squares in the rectangular portion of a bent IGFET
$P, P(V)$	Artificial surface potential
$P(I, J)$	Surface potential in 2D numerical program
q	Magnitude of the charge of an electron
Q_b	Channel depletion layer charge (per unit surface area)
Q_g	Gate charge (per unit surface area)
Q_m	Mobile channel charge (per unit surface area)
T	temperature
$T(W)$	Conformal transformation

T'	Derivative of the conformal transformation
V	Surface potential
V_d	Drain potential
V_g	Gate potential
V_s	Source potential
W	Width of a rectangular IGFET
W_d	Width at the drain end of a bent IGFET
W_e	Effective width of a non-rectangular IGFET
W_s	Width at the source end of a bent IGFET
ψ	Potential
μ	Mobility
$\mu(V)$	Gate field dependent mobility

CHAPTER 1

INTRODUCTION

A major concern in integrated circuit layout is minimizing silicon area. For a given fabrication process, a set of layout design rules is determined from process limitations. The designer must use clever layout techniques to achieve a minimum circuit area without violating these rules.

A significant area reduction is often possible by allowing designers to bend the gates of very long or wide IGFETs resulting in a non-rectangular gate geometry (see Fig. 1.1). It is found that the presence of a bend does not significantly change the form of the dc characteristics of the device from those of a rectangular IGFET, but it does change the effective aspect ratio of the device. Thus it is necessary to adjust the length or width of the device to compensate for the bend.

Designers have developed several rules of thumb to

(1) Throughout this thesis, the term "non-rectangular" IGFET refers to an IGFET with an arbitrary gate plane geometry. The term "bent" IGFET is reserved for a transistor consisting of rectangular regions separated by bends as shown in Figure 1.1. The source and drain can lie along the solid (transistor has bend along its width) or dashed (bend along its length) lines. It is further assumed that all the rectangular regions of a bent transistor have the same length (width).

(a)

(b)

(c)

(d)

(e)

(f)

Source and drain can be on solid or dashed lines

Fig. 1.1: Common gate plane geometries of IGFETs

- a) Rectangular
- b) L-shaped
- c) U-shaped
- d) Z-shaped
- e) W-shaped
- f) 45 degree L-shaped (L45)

estimate the effective aspect ratio of bent transistors (1). These range from assuming that a 90 degree corner region contributes nothing to the aspect ratio, to assuming that the corner contributes one square to its centerline length. Then there are the moderates who give the corner a half a square weighting. No simple rules of thumb are available for an arbitrarily shaped non-rectangular transistor (see Fig. 2.2.1). Associated with these rules of thumb is the practice of increasing the length or width by an additional amount to allow for the uncertainty in the estimate. This, perhaps unnecessarily, reduces the amount of area saved by bending the device.

This design methodology has long been used to design functional digital integrated circuits. However, the uncertainty of this approach makes it inadequate for designing analogue or sensitive digital circuits reliably. Accurate circuit simulation is necessary to determine the process sensitivity and noise characteristics of these circuits.

The arbitrary increase in transistor length or width is also unacceptable for cells that are to be entered into a cell library. Any increase in the area of a library cell is undesirable as the cell will be used hundreds of times on various chips. Further, if a cell library approach is to be used effectively, accurate characterization of each cell is necessary. If accurate simulation of non-rectangular transistors is not available, then this characterization must be performed experimentally on fabricated cells.

The most direct approach to modelling a non-rectangular IGFET is with a two or three-dimensional simulator. Tarique [1] has recently described a two-dimensional numerical program to analyse a non-rectangular IGFET. The program employs the gradual channel approximation and a simple expression for the bulk charge to remove the dependence of the analysis on the direction perpendicular to the semiconductor surface. In this respect, the analysis is analogous to a simple one-dimensional model and is restricted to IGFETs operating in the triode region. No mention is made of the saturation region or of second order effects such as short channel and narrow width effects.

Unfortunately, the cost of running even this simple two-dimensional simulator at the circuit level is prohibitive and a more efficient approach for simulating these devices is necessary. As shown in Figure 1.2, the shapes of the I_d versus V_d characteristics of a bent transistor do not differ significantly from those of a rectangular transistor. This suggests that it should be possible to add a correction factor to a one-dimensional IGFET model to describe the effect of the non-rectangular geometry. This is analogous to the use of correction factors to model other two-dimensional effects such as short channel and narrow width effects [2,3]. This thesis demonstrates the validity of this approach.

An analysis of the IGFET in the triode and subthreshold regions shows that the expression for the drain current is

(a)

(b)

Fig. 1.2: The drain characteristics of a rectangular and a bent IGFET

- a) rectangular IGFET ($W/L=120/6$)
- b) W-shaped IGFET ($W/L=120/6$)

independent of the gate plane geometry. In other words, the drain current of a non-rectangular IGFET is the same as that of a rectangular IGFET with an effective aspect ratio which depends on the device geometry. This effective aspect ratio can be determined by conformal mapping techniques, or by two-dimensional numerical methods as discussed in Chapter 2.

An array of bent transistors was fabricated (see Chapter 3) and the drain current of these devices is shown to agree excellently with that predicted by the above approach (Chapter 4).

Chapter 5 presents a qualitative discussion of the saturation region, small geometry effects, gate capacitance and drain breakdown voltage from a one-dimensional modelling aspect. When possible, simple experimental rules are determined for predicting these effects. The thesis concludes with a methodology for designing circuits with bent transistors.

CHAPTER 2

A ONE-DIMENSIONAL NON-RECTANGULAR IGFET MODEL

2.1 Introduction

To calculate the drain current of an IGFET directly, it is necessary in general to solve simultaneously Poisson's and the current continuity equation in three dimensions. Such an approach requires a large amount of computer time to solve for the drain current at a fixed bias condition. The cost of this approach for simulating circuits with several transistors is prohibitive. It is necessary to sacrifice some of the accuracy of the above approach in exchange for a reduced complexity of the analysis and computing time.

With several simplifying assumptions, it is possible to obtain a one-dimensional closed form solution for the drain current of the IGFET in the triode region [4,5,6]. This simple model can then be extended to describe the saturation region and various second order effects [2,3,7]. The accuracy and speed of such one-dimensional models are suitable for circuit level simulations.

The final form of the expressions which result from a one-dimensional IGFET analysis depend on the manner in which the general problem is simplified. One common point in all analysis is to note that the current density does not vary

across the width of the device. An integration is performed across the width which produces a direct dependence of the drain current on the device width (W). A subsequent integration of the current density along the length of the channel yields an inverse dependence of the drain current on the gate length (L). Thus, the drain current is proportional to the ratio of the width of the device to the length (W/L). This parameter is termed the aspect ratio of the device and is a fundamental device design parameter.

In the analysis of a non-rectangular transistor, the assumption that the current density is constant across the channel is invalid. The usual analysis breaks down at this point. A modified approach is required to obtain the necessary simple expression for the drain current of a non-rectangular device.

When the source-drain potential of an IGFET approaches zero, the surface potential is governed by Laplace's equation (ie. the IGFET can be considered as a gate controlled resistor having a uniform sheet resistance for a given gate voltage). Under these circumstances, conformal mapping techniques can be used to obtain an effective aspect ratio for the device. As the drain-source potential rises, it seems reasonable to expect that there should not be a major change in this effective aspect ratio. In fact, it is shown in the next section that the effective aspect ratio remains constant throughout the triode region even though the sheet resistance of the surface channel is not uniform.

2.2 Application of Conformal Mapping Techniques to Non-rectangular IGFETs

Conformal mapping techniques have long been used to calculate the capacitances and resistances of irregular shapes in which the potential is governed by Laplace's equation [8]. This approach is not directly applicable to IGFETS because the potential of the surface channel does not satisfy Laplace's equation. However, simplifying assumptions used to obtain a one-dimensional expression for the drain current of a rectangular IGFET are sufficient to allow a non-rectangular IGFET operating in the triode and subthreshold regions to be analysed by conformal mapping techniques (even though the surface potential still does not satisfy Laplace's equation).

The following assumptions are made in most one-dimensional analyses of IGFETs(1):

- i) The gradual-channel approximation. It is assumed that the electric field perpendicular to the semiconductor surface is much larger than the horizontal electric field. This also implies that the horizontal electric field is not a function of depth into the silicon. The application of Gauss'

(1) The analysis here is performed for an n-channel device, but applies equally well to a p-channel device with the appropriate modifications

law at the surface of the semiconductor yields an expression for the mobile channel charge (Q_m) in terms of the gate (V_g) and surface potential (V) and the bulk charge per unit surface area (Q_b) [4]:

$$Q_m = -C_{ox}(V_g - V) - Q_b \quad (2.2.1)$$

where V_g and V are taken with respect to the same reference potential (eg. the source) and at flat band $V_g = V$, (ie. V_g includes the effects of oxide charge and the work function difference between the gate and the semiconductor).

ii) The bulk charge can be expressed as a function of the surface potential [4]. This reduces equation (2.2.1) to:

$$Q_m = -C(V_g - f(V)) \quad (2.2.2)$$

where $f(V)$ is a function of V which depends on the expression used for Q_b .

iii) The mobility (μ) is constant, or at most is a function of the surface potential ($\mu(V)$). While μ varies significantly, the integrations involved in solving for the drain current have an averaging

effect on μ . Thus satisfactory results can be obtained by replacing μ by an average value which is independent of the horizontal electric field (ie. neglect velocity saturation in the triode and subthreshold regions [6]).

iv) Einstein's relation for the diffusion coefficient (D) is assumed valid (2):

$$D = (kT/q) \cdot \mu \quad (2.2.3)$$

v) The current is assumed to be due to minority carriers only.

An additional requirement which is implicit from the physics of the problem is that the functions are continuously differentiable throughout the region and that the region is simply connected.

The general expression for the drain current of an IFGET is given by the continuity equation (3):

(2) This is not actually necessary for the analysis performed here [6], but it does simplify the equations.

(3) It is not assumed that the drift current dominates. Hence the analysis is applicable to both the triode and subthreshold regions. Further, no assumptions have been made about the channel charge components Q_m and Q_b , other than that they can be expressed as a function of the surface potential. Thus, the approach is applicable to models which assume that Q_m contributes to the surface potential [5].

$$I_d = -q \iint_S (\mu n \text{ grad } \psi - D \text{ grad } n) \cdot d\underline{s} \quad (2.2.4)$$

where n is the mobile carrier density, S is a surface across the channel perpendicular to the semiconductor surface and ψ is the three-dimensional potential. The application of the gradual channel approximation reduces the surface integral to a line integral:

$$\begin{aligned} I_d &= -\int_1 \underline{j} \cdot d\underline{N} \\ &= -\int_1 (\mu Q_m \text{ grad } V - D \text{ grad } Q_m) \cdot \underline{N} dl \end{aligned} \quad (2.2.5)$$

where l is a path across the channel, dl points in the direction of l , $\underline{N}$ is the unit normal to this path and $\underline{j}$ is the surface current density (4):

$$\underline{j} = \mu(V) Q_m'(V) \text{ grad } V - D \text{ grad } Q_m(V) \quad (2.2.6)$$

Applying the chain rule for derivatives to the last term on the right hand side and substituting equation (2.2.3) for D yields:

$$\underline{j} = \mu(V) Q_m(V) \text{ grad } V - \mu(V) (kT/q) Q_m'(V) \text{ grad } V$$

(4) The current density vector is taken to point from the source towards the drain and $\underline{N}$ points in a direction such that $\underline{j} \cdot d\underline{N}$ is positive.

$$= \mu(V) [Q_m(V)' - (kT/q) Q_m'(V)] \text{grad } V \quad (2.2.7)$$

where

$$Q_m' = dQ_m(V)/dV \quad (2.2.8)$$

From equation (2.2.7) it is found that:

$$\text{curl } \underline{j} = 0 \quad (2.2.9)$$

This is a sufficient condition to ensure that the current density can be expressed as the gradient of a scalar potential, P [9]:

$$\underline{j} = \text{grad } P \quad (2.2.10)$$

Assuming steady state conditions:

$$\text{div } \underline{j} = 0 = \text{div grad } P \quad (2.2.11)$$

Thus P satisfies Laplace's equation and conformal mapping techniques can be used to solve for P . Indeed equation 2.2.10 is exactly that of a linear resistor obeying an artificial potential P instead of the real potential V . Equating equations (2.2.10) and (2.2.7) yields an expression for P in terms of V :

$$\text{grad } P = \mu(V) [Q_m(V) - (kT/q) Q_m'(V)] \text{grad } V \quad (2.2.12)$$

$$= P'(V) \text{grad } V$$

where

$$P'(V) = \mu(V) [Q_m(V) - (kT/q) Q_m'(V)]$$

This is exactly the chain rule for differentiation, and so:

$$P'(V) = dP/dV$$

$$P = P(V) \quad (2.2.13)$$

which denotes that P is a scalar function of V defined by (2.2.12).

The fact that P is a function of V allows us to determine the boundary conditions for P immediately from equations (2.2.12) and (2.2.13). Along the source and drain boundaries, V is a constant. From equation (2.2.13) P will also be constant there. Equation (2.2.12) states that the gradient of P is everywhere parallel to the gradient of V . Thus, the boundary condition $\text{grad } V = 0$ satisfied at the sides of the transistor implies that $\text{grad } P$ is also zero at the sides of the transistor. It follows that an equipotential of P is also an equipotential of V (5).

The drain current of an arbitrarily shaped IGFET can now

be calculated. The first step is to find a conformal transformation which maps the transistor onto a rectangular boundary with the source and drain on opposite sides of the rectangle (see Fig. 2.2.1). The current density is then calculated in the transformed plane where the current flow is one-dimensional:

$$\begin{aligned} \underline{j} &= g \text{ grad } P \\ &= [(P(V_d) - P(V_s))/L_e] \underline{e}_x \end{aligned} \quad (2.2.14)$$

where L_e is the length of the rectangle between the source and the drain in the transformed plane, V_d and V_s are the drain and source potentials, and $\underline{e}_x$ is the unit vector in the x direction. To find the total drain current, $\underline{j}$ is integrated across the width of the rectangle in the transformed plane (W_e) which yields:

$$I_d = (W_e/L_e) (P(V_d) - P(V_s)) \quad (2.2.15)$$

Here again, the transistor behaves as a resistor satisfying an artificial surface potential P (6). It is shown in the next section that an expression for the drain current

(5) It should be noted that this approach is not restricted to analysing IGFETs. It is applicable to any situation where a vector field can be expressed as the product of one variable and the gradient of that variable when the divergence of the vector field is zero.

..... electric field lines
 --- equipotentials of the surface potential

Fig: 2.2.1: Gate plane geometry of a non-rectangular IGFET in the physical and transformed planes.

- a) actual device geometry (w-plane)
- b) transformed device geometry (z-plane)

can also be derived in terms of the real potential ϕ (7). This allows us to analyse non-rectangular IGFET's with existing one-dimensional models.

2.3 A One-dimensional Expression for the Drain Current of a Non-rectangular IGFET

In the last section, an expression was derived for the drain current of a non-rectangular IGFET. One approach to modelling non-rectangular transistors is to rewrite an existing one-dimensional model in terms of the artificial potential ϕ and calculate the drain current of the device using equation (2.2.15). However, the analysis presented is applicable only to the triode and subthreshold regions. It would be necessary to rederive the expressions for the saturation region in terms of ϕ . Also new expressions would be required for second order effects, such as narrow width and short channel effects. Another disadvantage of this

(6) This is why a transistor with a small drain to source potential behaves like a resistor. Under these conditions:

$$\phi'(V) = [Q_m(V) + (kT/q)Q_m'(V)]\mu(V) = K$$

$$\phi(V) = K V + K_2$$

where K and K_2 are constants.

(7) In fact, from (3) above, the drain current can be expressed in terms of any variable, x , such that ϕ can be expressed as a scalar function of x . Thus, for example, it is possible to derive an expression for the drain current in terms of quasi-Fermi potentials [5].

approach is that P is not a physical quantity, but a mathematical entity as defined by equation (2.2.12). By working in terms of P , the analysis is removed one step from the physics of the device.

It will now be shown that an expression for the drain current of a non-rectangular IGFET can also be derived in terms of the real potential V . This is done by exploiting the properties of conformal transformations and the fact that P is a scalar function of V . The result is that the expression for the drain current of a non-rectangular IGFET is exactly the same as the expression describing a rectangular device with W/L replaced by an effective aspect ratio W_e/L_e . The ratio W_e/L_e is defined completely by the conformal transformation involved.

In the last section, the following expression was used for the drain current of an IGFET:

$$I_d = - \int_1 (\mu Q_m \text{grad } V - D \text{grad } Q_m) \cdot \underline{N} \, dl \quad (2.2.5)$$

Again, it is assumed that μ and Q_m are scalar functions of V and (2.2.5) can be rewritten as:

$$I_d = - \int_1 \mu(V) [Q_m(V) - (kT/q) Q_m'(V)] \text{grad } V \cdot \underline{N} \, dl \quad (2.3.1)$$

By choosing an equipotential as the path of integration, μ , Q_m , and Q_m' are all constant along the path of integration and can be taken outside the integral. Also,

by definition, grad V will be perpendicular to this path and grad $V \cdot \underline{N}$ can be replaced by dV/dN with the sign depending on the direction of the integration. A positive sign can be chosen (without any loss of generality) and (2.3.1) becomes:

$$I_d = -\mu(V) [Q_m(V) - (kT/q) Q_m'(V)] \int_1 (dV/dN) dl \quad (2.3.2)$$

A conformal transformation, $z=T(w)$, is now performed to map the non-rectangular transistor from the w -plane onto a rectangle in the z -plane as shown in Figure 2.2.1. A solution of P in the transformed plane will result in equipotentials of P given by the equation $x=\text{constant}$ and that grad P will be in a direction parallel to lines $y=\text{constant}$ (see Fig. 2.2.1). But by definition, grad P is everywhere parallel to grad V and equipotentials of P are also equipotentials of V (1). Thus, in the transformed plane, V and grad V are both functions only of x and (2.3.2) can be written in terms of the transformed variables x and y :

$$I_d = -\mu(V) [Q_m(V) - (kT/q) Q_m'(V)] \int_0^{W_e} \frac{dV}{dx} \frac{dx}{dN} \frac{dl}{dy} dy \quad (2.3.3)$$

where W_e is the width of the rectangle in the transformed plane. Since the mapping is conformal:

(1) The value of V at a point r in the z -plane is defined to be the value of V at the point s in the w -plane which is mapped into r by the conformal transformation.

$$dN/dx = dl/dy \quad (2.3.4)$$

and the expression for the drain current simplifies to:

$$I_d = -\mu(V) [Q_m(V) - (kT/q) Q_m'(V)] \int_0^{W_e} dV/dx \, dy$$

Since dV/dx is independent of y , it can be moved outside the integral:

$$I_d = -\mu(V) [Q_m(V) - (kT/q) Q_m'(V)] dV/dx \int_0^{W_e} dy$$

$$= -\mu(V) [Q_m(V) - (kT/q) Q_m'(V)] dV/dx \, W_e \quad (2.3.5)$$

Multiplying both sides by dx and integrating from the source to the drain:

$$\int_0^{L_e} I_d \, dx = -W_e \int_{V_s}^{V_d} \mu(V) [Q_m(V) - (kT/q) Q_m'(V)] dV \quad (2.3.6)$$

$$I_d L_e = W_e (F(V_d) - F(V_s))$$

$$I_d = (W_e/L_e) (F(V_d) - F(V_s)) \quad (2.3.7)$$

where L_e is the length of the rectangle in the transformed plane and $F(V)$ is the indefinite integral:

$$F(V) = -\int \mu(V) [Q_m(V) - (kT/q) Q_m'(V)] dV \quad (2.3.8)$$

The function $F(V)$ depends only on the choice of the expression for the mobile channel charge and the mobility(2). The important result is that $F(V)$ is independent of the surface geometry of the device. Thus, $F(V)$ is the same for a rectangular and non-rectangular device. In other words, the drain current of a non-rectangular IGFET is the same as that of a rectangular transistor with an aspect ratio W_e/L_e .

The parameter W_e/L_e depends only on the device geometry and not on the operating conditions of the IGFET. It is therefore possible to calculate this parameter a priori and enter it directly to an existing one-dimensional expression for the drain current of the IGFET. An immediate consequence of this is that the small signal parameters (g_d, g_m) of a non-rectangular transistor will also be the same as those of a rectangular transistor with an effective aspect ratio W_e/L_e .

2.4 Determination of W_e/L_e by Conformal Mapping Techniques

The effective aspect ratio of a non-rectangular transistor was shown in the previous two sections to be equal to the ratio of the length and width of the rectangle that the

(2) Comparing equations (2.3.7) and (2.2.15), it is seen that $F(V)$ and $P(V)$ are actually the same function (to within an additive constant). Indeed, (2.3.8) is just the integral form of (2.2.12).

boundary is mapped into by a conformal transformation. Unfortunately, this transform can only be solved explicitly for relatively simple boundaries such as a transistor with a single bend. For more complex shapes, it is necessary to resort to two-dimensional numerical methods as described in the next section.

A bent transistor has been defined to be a transistor consisting of rectangular sections separated by corners (see Figure 1.1). Since the same transform will be used for a transistor with a bend along its length as for a transistor with a bend along its width, it becomes inappropriate to work in terms of W_e/L_e . Instead, further development is done in terms of the effective number of squares, N_e which is defined as the aspect ratio (W_e/L_e) of a transistor with a bend along its width. A transistor with a bend along its length has an aspect ratio $1/N_e$. It is also conceptually convenient to subtract the number of squares contained in the rectangular section (N_r) and to consider the remainder as the effective contribution of the corner (N_b) as shown in Figure 2.4.1. This notation is useful as two bends are found to behave as isolated bends if they are separated by more than one square.

The conformal transformation that maps an arbitrary shape into a rectangle depends only on the original shape. Thus, the transformation used for an IGFET is the same as that used for a resistor or capacitor and the library of results derived for non-rectangular resistors and capacitors

$$N_e = N_{r1} + N_{r2} + N_b$$

$$N_e = N_{r1} + N_{r2} + N_b$$

$$N_e = N_{r1} + N_{r2} + N_{b1} + N_{b2}$$

$$N_e = N_{r1} + N_{r2} + N_{r3} + N_{b1} + N_{b2}$$

Solid lines are source and drain boundaries

Fig. 2.4.1: Separation of a bent IGFET into rectangular and corner regions.

can be applied directly to non-rectangular IGFET's.

A summary of calculations of the effective aspect ratio of resistors with a single bend is given by Hall [8]. For a single 90 degree bend with no corner rounding, the conformal transformation from the w to the z -plane is [10]:

$$w = -\frac{2b}{\pi} \tan^{-1} \left\{ \frac{g}{b} \sqrt{\frac{t+1}{t-g^2/b^2}} \right\} + \frac{g}{\pi} \log \left\{ \frac{\sqrt{t-g^2/b^2} + \sqrt{t+1}}{\sqrt{t-g^2/b^2} - \sqrt{t+1}} \right\} \\ + b + ig \\ t = \exp(iz\pi/U) \quad (2.4.1)$$

where g and b are the lengths of the two arms on the w -plane and U is the length of the rectangle in the z -plane. If the two arms have the same length ($g=b$), then the corner section contributes 0.5587 squares. Thus, the moderate's rule of thumb (0.5 square) is a reasonably good estimate in this case.

If the inside corner has a nonzero radius of curvature, r , the effect of the corner can be expressed as [11].

$$Nb = 0.5587 - 0.4381(r/L)^{4/3} \quad (2.4.2)$$

where L is the length of the straight portion of the transistor. This expression results from an expansion of exponentials which is valid for r much less than L , but it found to yield reasonable results for r as large as $1/2 L$.

A conformal mapping of a transistor with two bends results in elliptic functions. The limiting cases for a U-shaped IGFET are given by Hall [8]. If the separation of the two bends is zero, each bend adds 0.459 of a square to the aspect ratio. If the bends are separated by a large distance, each bend will add 0.5587 of a square (behave as two isolated bends). Two bends separated by one square add approximately 0.523 squares each. For a Z-shaped transistor, the limiting cases are two isolated bends (large separation) and a rectangular transistor (no separation).

The analysis for two bends separated by a finite amount is accomplished by two successive Schwarz-Christoffel transformations. A transformation is used to map the bent transistor onto the real axis in an auxiliary t-plane and then to map the real axis of the t-plane to a rectangular boundary in the z plane [10]. The second transform has the form:

$$w = A \exp(t) + B \exp(-t) \quad (2.4.3)$$

where A or B may be zero. The first transform results in an incomplete elliptic function of the third kind for both a U-shaped and Z-shaped transistor.

The U-shape has been solved in terms of theta functions by Cockroft [12]. To calculate N_e , only the solution on the boundary is necessary. This can be solved in terms of the complete and incomplete elliptic function of the third kind [13]. The differential form of the transform for a $1/2$

U-shape is:

$$\frac{dw}{dt} = A \left\{ \frac{t-d}{(t-a)(t-b)(t-c)} \right\}^{1/2}$$

where $a > b > c > d$

For the Z-shape, the transform is:

$$\begin{aligned} \frac{dw}{dt} &= \frac{A}{t-c} \left\{ \frac{(t-b)(t-e)}{(t-a)(t-d)} \right\}^{1/2} \\ &= \frac{A[t^2 + (b+e)t + be]}{(t-c)[(t-a)(t-b)(t-d)(t-e)]^{1/2}} \end{aligned} \quad (2.4.6)$$

where $a > b > c > d > e$

A two dimensional mapping allows for the arbitrary placement of three points. The ends of the transistor have been mapped into infinity which leaves two more arbitrary selections. The remaining points and the constant A must be found by integrating between two roots of (2.4.5) or (2.4.6) and equating this to the w-plane distance between the two points. This is a very tedious process to do from tables. Further, tables of the incomplete elliptic integral of the third kind or theta functions are necessary, both were unavailable.

The integration of dw/dt can also be done numerically. However, if a numerical integration is to be performed, a more general and direct approach is to use two-dimensional numerical methods to find the effective aspect ratio, as

described in the next section.

2.5 Calculation of Aspect Ratios by Numerical Methods

It is obvious from the treatment of an IGFET with two bends that the method of conformal mapping is limited to very simple shapes. It is necessary to find another method of calculating the effective aspect ratio of a non-rectangular IGFET. In this section, it is shown how to calculate the parameter W_e/L_e by two-dimensional numerical methods.

Tarique [1] has shown that it is possible to calculate the drain current of a non-rectangular IGFET by numerically solving Poisson's equation in two dimensions. From Section 2.3, an alternative approach is to calculate the effective aspect ratio by two-dimensional techniques and then use an expression based upon a one-dimensional analysis to calculate the drain current. The second is the only feasible approach for circuit level simulations which cannot bear the cost of two-dimensional simulations.

From Section 2.2, an expression for W_e/L_e in terms of the drain current and the artificial potential P is:

$$W_e/L_e = I_d / (P(V_d) - P(V_s)) \quad (2.5.1)$$

Conceptually, reverse the conformal transformation (ie. map the rectangle into the desired non-rectangular boundary)

and recall that the drain current is the integral of grad P along a specified curve. As before, the numerical value of this integral and the numerical value of P are preserved under the conformal transformation. This results in the following method of calculating the effective aspect ratio of a non-rectangular device. First, Laplace's equation is solved with constant (but not equal) values of potential along the source and drain boundaries. Then, the flux is calculated by summing grad P along a line across the width of the shape. The effective aspect ratio of the device is, by equation (2.5.1), the ratio of the flux to the difference of the boundary potentials, P.

A simple finite difference program to solve Laplace's equation for an arbitrary geometry is given in Appendix 1. The program reads an array of initial values and a line across which the flux is to be calculated from a data file (see Appendix 2). The device proper is assumed to lie entirely in the subset of this array obtained by deleting the first and last rows and columns. This outside boarder allows simple application of a Neumann boundary condition which is assumed to hold on the boundary of the subset array. The source and drain are defined by setting the initial values of these regions equal to "1" and "11" respectively, (Dirichelet boundary condition) (1). Thus, the effective aspect ratio of the transistor is:

$$N_e = \text{FLUX}/10$$

$$(2.5.2)$$

where FLUX is the output of the program.

The program solves for the potential P using Thom's "20" formula [14] (2):

$$P(I,J) = (4*S1+S2)/20 \quad (2.5.3)$$

$$S1 = P(I-1,J)+P(I+1,J)+P(I,J-1)+P(I,J+1)$$

$$S2 = P(I-1,J-1)+P(I+1,J-1)+P(I-1,J+1)+P(I+1,J+1)$$

The convergence of the process is guaranteed, although not necessarily fast.

The gradient of the potential perpendicular to a horizontal line segment is then approximated as:

$$\text{grad } P = P(I,J)-P(I,J-1)$$

For a vertical line, the perpendicular flux is given by:

(1) This allows us to describe bent IGFETs with a bend along their width which is preferable to solving an IGFET with a bend along its length as the larger source and drain imply that the method will converge to a solution faster. As stated in Section 2.4, the effective number of squares for a transistor with a bend along its length is $1/N_e$.

(2) This was preferred over the simple 4-point approximation: $P(I,J) = S1/4$ because the first error term of the "20" formula is of order six when solving Laplace's equation.

$$\text{grad } P = P(I,J) - P(I-1,J)$$

Since the horizontal and vertical step size are equal, the total flux crossing a line is just the sum:

$$\text{FLUX} = \sum_{\text{FL}} \text{grad } P \quad (2.5.4)$$

where FL is the specified line.

The program will approximate corner rounding to the nearest grid point. After the solution has converged, the program is able to halve the mesh size and iterate further to increase the accuracy of the result.

The accuracy of the program was determined by calculating the effective aspect ratio of L and U shapes (see Fig. 1.1) which can also be solved by conformal mapping techniques. Table 2.5.1 shows that the error in calculating the effective aspect ratio by numerical methods was less than one percent when the mesh was refined. With the exception of the U shape, the error was less than one percent with only five internal mesh points across the rectangular portion of the transistor (see Appendix 2). If the rectangular portion of the IGFET is subtracted and all of the error is associated with the corner region, the error is still less than one percent for the L-shape and only three percent for the U-shape. Results were obtained for the L-shape with different lengths of the straight portion. As shown in Table 2.5.1, the results are the same when the arms

SHAPE	Nr.	Mesh Points	Numerical	Ne Conformal	Ne	Error (%)	Nb
RECTANGLE	1.0	10	0.999	1.0	-0.1		
L (flux line along inside edge of L)	2.5 2.5	6 12	3.0900 3.0678	3.0587	1.0 0.3	5.6 1.6	
L (flux line at center of L)	2.5 2.5 3.0	6 12 24 40	3.0863 3.0688 3.0626 3.5613	3.0587	0.9 0.3 0.1 0.1	4.9 1.8 0.7 0.5	
L ⁻ (flux line along outside edge of L)	2.5 2.5,	6 12	3.0860 3.0713	3.0587	0.9 0.4	4.9 2.3	
U (no separation between arms)	1.5	6 12 24	2.0270 1.9969 1.9830*	1.969	3.0 1.4 0.7	12.4 6.0 3.0	

* Failed to converge totally

Table 2.5.1 Accuracy of 2-D Numerical Solution

are one and one-and-a-half squares.

There was also little dependence on the position of the line across which the flux was calculated. The accuracy in calculating the effective aspect ratio of the corner (Nb) varied by only one percent as the line was moved from the source edge of the transistor to the drain edge. All results for other shapes were calculated by positioning the flux line near the center of the shape and having one square on each side of the bend.

In all of the cases, the error could have been reduced by reducing the mesh size and tightening the convergence criterion. However, the error is already small when compared with changes in the aspect ratio caused by processing uncertainties such as corner rounding, etching and misalignment.

The effective aspect ratio for a number of transistors with two bends are given in Table 2.5.2. Results are also presented for a transistor with a 45 degree bend. While the program is applicable to arbitrary shapes, the analysis was restricted to shapes for which experimental data could be obtained from test structures (see Chapters 3 and 4).

SHAPE	BEND SEPARATION	MESH POINTS	CORNER ROUNDING	Nr	Ne	Nb
Z	L/3	12	Ø	2	2.900	0.900
	2L/3	24	Ø	2	3.001	1.001
		6	L/3	2	2.795	0.795
	L	24	Ø	2	3.215	1.215
		6	L/2	2	2.801	0.801
	4L/3	12	Ø	2.33	3.505	0.586
		12	L/2	2.33	2.945	0.306
	2L	12	Ø	3	4.143	0.571
		12	L/2	3	3.524	0.262
	L	24	Ø	3	3.966	0.483
U	4L/3	24	Ø	3.33	4.417	0.542
	2L	24	Ø	4	5.121	0.565
L45		10	Ø	1.4	1.710	0.310
Z45	L/3	12	Ø	2	2.893	0.893

TABLE 2.5.2 Effective aspect ratios of corner

regions of bent IGFETs

CHAPTER 3

EXPERIMENTAL METHODS

3.1 Sample Devices

An array of bent transistors was designed to verify the theory of the previous chapter. The array included sample devices of each bent shape shown in Figure 1.1. Devices were fabricated both with bends along their width and with bends along their length. For geometries with more than one bend (ie. U, Z and W), several devices were fabricated with a varying separation between the bends to check for proximity effects.

The devices were designed in families to test for device scaling. The family of small devices (S) employed a minimum dimension of 6 microns for both length and width. Large (scaled) devices (L) had gate lengths of 22 microns for devices with bends along their width. Large devices with bends along their length had a channel width of 18 microns. Large (but not scaled) devices (C) were fabricated to investigate the effect of 90 and 45 degree bends on gate capacitance.

Each device is described by an alphanumeric code. The first letter of the code identifies the transistor family (Large or Small). The second letter of the code denotes the

direction of the bend. If the bend is along the length of the transistor (ie. appears on the field oxide mask), it is denoted by an L. A bend along the width of the transistor (ie. appears on the gate level mask) is denoted by a W. Each transistor in a given family has the same gate length (width) in the rectangular region and the same centerline width (length). The third letter describes the shape of the transistor as given in Figure 1.1. Transistors with a bend along their width have an additional letter to denote if the source (S) or drain (D) has a smaller gate perimeter (ie. is on the inside of the bend). The letter is not necessary for Z and W shaped transistors which have equal source and drain perimeters. For transistors with two bends, a number is added which denotes the amount by which the center of the two bends are separated (in microns). Thus, LWUS38 denotes a large U-shaped transistor which is bent along its width. The source is on the inside of the U and the center of the two arms are separated by 38 microns. A complete listing of devices fabricated is given in Table 3.1.1.

The devices were fabricated in a polysilicon gate, enhancement NMOS process at Bell Northern Research labs, Ottawa. Optical and electrical measurements were performed to determine the actual device dimensions (as listed in Table 3.1.1). The gate length was optically measured on the LW devices to be 24.4 μm . 2.1 μm was then subtracted for sideways diffusion of the source and drain under the polysilicon gate, resulting in a gate length of 23.3 μm . This

FAMILY	MEASURED DIMENSION (W/L)	SHAPE	BEND SEPARATION
LW	360/22.3	R	
	360.4/22.3	L	
	360.4/22.3	U	38
	359.6/22.3		120
	360/22.3	W	90
LL	18/360.4	R	
	18/360.4	L	
	18/360.0	U	24
	18/360.8		120
	18/360.4	W	90
SW	120/6.3	R	
	60/6.3	R/2	
	120/6.3	L	
	120/6.3	U	40
	120/6.3	Z	2
	120/6.3		4
	120/6.3		8
	120/6.3		16
	120/6.3		32
	120/6.3	W	30
SL	6/120	R	
	6/120	L	
	6/120	U	40
	6/120	Z	2
	6/120		3
	6/120		6
	6/120		16
	6/120		32
	6/120	W	30
CW	116/98	IL	
	300/98	3L	
	300/98	3L45	

Table 3.1.1 A List of Fabricated Bent IGFETS

calculation implies an underetch of $0.4 \mu\text{m}$ and this value was added to the designed value of all gate lengths (1).

The width of the devices was difficult to determine optically because of the taper of the oxide. The width was determined electrically by comparing the current to the large wide rectangular device (LWR) to the current of the large long rectangular device (LLR):

$$W(\text{LLR}) = \frac{I_d(\text{LLR})}{I_d(\text{LWR})} \frac{L(\text{LLR})}{L(\text{LWR})} W(\text{LWR}) \quad (3.1.1)$$

The mean value of the width calculated was equal to the designed dimension and this was assumed to hold for all the transistors in the array.

The internal rounding of a polysilicon corner was measured to be $2.0 \mu\text{m}$. Assuming $1 \mu\text{m}$ sideways diffusion, the internal radius of of the channel becomes $3.0 \mu\text{m}$. The field oxide taper made it difficult to measure the rounding of the field oxide corners accurately. The best estimate was again $3 \mu\text{m}$.

Finally, a photograph was taken of the alignment marks to calculate the increase in length or width caused by misalignment of the field oxide and polysilicon levels. The misalignment was estimated as $0.2 \mu\text{m}$ in both horizontal directions and is included in the dimensions listed in Table

(1) All devices were widely separated so there should not have been any proximity effects. To achieve better accuracy would have required optical measurement of each transistor.

3.1.1 for the large (L) devices. (2)

To reduce the pin count, the transistors in a given family were laid out in a string such that the source of one transistor was also the drain of the next device. All devices in the SW, SL, LL and LW families had a common gate contact. The C family of devices were fabricated with individual gate connections to allow the measurement of gate capacitance.

3.2 Measurement Techniques

The drain current and small signal parameters of individual IGFET's were measured using the circuits of Figures 3.2.1 and 3.2.2. In Figure 3.2.1, the output of the op-amp is a voltage which is proportional to the current in the transistor. Thus, the chart recorder plots the drain current of the IGFET as a function of the drain voltage. Connections 1 and 2 can be interchanged to plot the drain current as a function of the gate voltage for a constant drain voltage.

In the circuit of Figure 3.2.2, two op-amps have been added to superimpose a 300 Hz, 20 mv ac signal upon the dc potential applied to the drain or gate of the IGFET. The

(2) No correction for misalignment was calculated for the small (S) devices. Instead, two L-shapes were laid out in opposite directions and the average current was used. The SWZ and SLZ shapes are not alignment sensitive.

Fig. 3.2.1: Circuit used to measure I_d as a function of V_d and V_g

Fig. 3.2.2: Circuit used to measure the small signal parameters of an IGFET.

output of the ac/dc converter is proportional to the transconductance, g_m , if the ac signal is added to the gate potential. If the ac signal is added to the drain potential, the output of the ac/dc converter is proportional to the drain conductance, g_d .

The results obtained with these circuits confirmed that the characteristics of a bent IGFET are indistinguishable in form from those of a rectangular device. However, since the bend was a small portion of the total transistor, these methods were not accurate enough to confirm that the effective aspect ratio was equal to that predicted by the analysis of Chapter 2. The accuracy was also insufficient to determine if the correction factor calculated for the triode region was applicable to the saturation region and to investigate the effect of the bend on second order characteristics such as short channel effects.

To achieve the accuracy required, the drain current of the bent device was compared directly with the drain current of a rectangular device having the same nominal gate length (width) and centerline width (length) for devices with a bend along their width (length). The circuit employed for this direct comparison is shown in Figure 3.2.3. OA1 performs a current to voltage conversion as in Figure 3.2.1. Since R_1 and R_2 are of equal value, the current flowing in R_2 is equal to the current flowing in the reference transistor N_1 . The difference in the current in the two transistors is forced through R_3 . The output of the second op-amp

$$R1 = R2 = R3/10$$

Fig. 3.2.3: Circuit used to directly compare the drain current of two IGFETs

is:

$$V_{O2} = R3(I(N2) - I(N1)) = R3 \Delta I_d \quad (3.2.1)$$

and the recorder plots $\Delta I_d = (I(N2) - I(N1))$ against the current in the reference device, $I(N1)$.

Resistors were chosen for $R1$ and $R2$ which matched to four digits when measured with a Hewlett-Packard 3465B digital multi-meter. The absolute accuracy of the resistors was better than 0.1 percent. The ratio $R3/R2$ was also accurate to 0.1 percent. All op-amps had JFET input devices to eliminate any input bias current. The op-amp offset voltage was adjusted to be less than 0.2 mv.

The gate capacitance of C series transistors was measured with a Boonton 72B capacitance meter as shown in Figure 3.2.4. Unfortunately, the frequency of the oscillator in the capacitance bridge is fixed at 1 MHz and the data exhibited high frequency characteristics in the inversion region (see Section 5.5). The capacitance of an isolated pad on the IC showed no bias dependence. The absolute capacitance of the pad was 0.38 pf.

Fig. 3.2.4: Measurement of gate capacitance.

CHAPTER 4

EXPERIMENTAL RESULTS

The measured value of the drain current of a bent IGFET operating in the triode region was found to agree excellently with the value predicted in Chapter 2. The agreement is especially good for large devices (LL and LW families) which are less susceptible to process variations across the die than the smaller devices (SW and SL families).

Figures 4.1 and 4.2 show sample plots of the difference (ΔI_d) between the drain current of a Z-shaped IGFET (I_{db}) and the drain current of a rectangular device (I_{dr}) versus the drain current of the rectangular device. Figure 4.3 plots ΔI_d vs I_{dr} for an L-shaped transistor. In the triode region, the curves are almost a straight line with slope equal to the difference in aspect ratios as predicted in Chapter 2. The change in slope in Figure 4.3 marks the point at which devices enter saturation and is discussed in Section 5.2. A summary of the measured and calculated effective aspect ratios of bent IGFETs is given in Table 4.1.

The experimental values of W_e/L_e were determined from the ΔI_d vs I_d plots generated by the circuit shown in Figure 3.2.3.

In Chapter 2, it was shown that the drain current of an

Fig. 4.1: ΔI_d vs I_d plot for three Z-shaped IGFETs with bends along their length.

Fig. 4.2(a): ΔI_d vs I_d plot for Z-shaped IGFETs with different bend separations; bend along length (NLZ family).

Fig. 4.2(b): ΔI_d vs I_d plot for Z-shaped IGFETs with different bend separations; bend along width.

Fig 4.3(a) ΔI_d vs I_d plot for an L-shaped IGFET; drain on outside of L.

Fig. 4.3(b): ΔI_d vs I_d plot for an L-shaped IGFET;
drain of inside of L.

IGFET SHAPE	----- Ne -----		----- Nb -----	
	THEORY*	MEASURED	THEORY*	MEASURED
LWL	15.02 c	15.06	0.529 c	0.57
LWU ₁₂₀	14.53 c	14.53	0.529 c	0.53**
LWW	13.65 c	13.73	0.529 c	0.55**
LLL	19.54 c	19.54	0.519 c	0.52
LLU ₁₂₀	19.08 c	19.11	0.519 c	0.53**
LLW	18.09 c	18.16	0.519 c	0.53**
CW1L	0.633 n	0.630	0.47 n	0.466
CW3L	2.62 c	2.64	0.558 c	0.58
CW3L45	2.96 n	2.95	0.31 n	0.30
SWL (Die 1)	18.44 c	18.36	0.39 c	0.27
	18.38 n		0.34 n	
SWL (Die 3)		18.47		0.42
SWU ₄₀	17.73 n	17.71	0.34 n	0.33**
SWZ2 (Die 3)	18.61 n	18.79	0.90 n	0.99***
SWZ4 (Die 3)	18.18 n	18.37	0.80 n	0.99***
SWZ8 (Die 3)	17.67 n	18.00	0.31 n	0.46**
SWZ16 (Die 3)	17.72 n	17.94	0.34 n	0.44**
SWZ32 (Die 3)	17.72 n	17.91	0.34 n	0.43**
NLZ2	19.80 n	19.25	0.90 n	0.63***
NLZ3	19.35 n	18.72	0.85	0.36***
NLZ6	18.80 n	18.64	0.40 n	0.32**
NLZ16	18.68 n	18.50	0.34 n	0.25**
NLZ32	18.68 n	18.47	0.34 n	0.24**

* c denotes value obtained by conformal mapping;
n denotes value obtained by numerical methods

** two corner are considered separate (see Fig. 2.4.1)

*** two corners are considered together

Table 4.1 Comparison of Measured and Calculated

Aspect Ratios of Bent IGFETs

arbitrarily shaped IGFET has the form:

$$I_d = (W_e/L_e) (F(V_d) - F(V_s)) \quad (2.3.8)$$

This allows us to calculate the effective aspect ratio of a bent transistor, $(W_e/L_e)_b$, from the slope of the ΔI_d vs I_d plot and the aspect ratio of the rectangular device, $(W/L)_r$:

$$\begin{aligned} \text{slope} &= \Delta(I_d/I_{dr}) \\ &= (I_{db} - I_{dr})/I_{dr} \\ &= \frac{[(W_e/L_e)_b - (W/L)_r][F(V_d) - F(V_s)]}{(W/L)_r [F(V_d) - F(V_s)]} \\ &= \frac{(W_e/L_e)_b}{(W/L)_r} - 1 \end{aligned}$$

Hence,

$$(W_e/L_e)_b = (1 + \text{slope}) (W/L)_r$$

where the suffix is used to denote a bent (b) or a rectangular (r) device.

As in Sections 2.4 and 2.5, it is convenient to think in terms of numbers of squares N_e , N_r and N_b . Thus, for a device with a bend along its width, we can write:

$$N_{eb} = (1 + \text{slope}) N_{er}$$

$$N_{bb} = N_{eb} - N_{rb}$$

$$= (\text{slope}) N_{er}$$

For a device with a bend along its length, this becomes:

$$1/N_{eb} = (1 + \text{slope}) / N_{er}$$

$$N_{eb} = N_{er} / (1 + \text{slope})$$

$$N_{bb} = N_{eb} - N_{er}$$

$$= (\text{slope}) N_{er} / (1 + \text{slope})$$

The agreement between calculated and measured values of N_e is better than one percent. For the large devices (LW and LL), the difference between calculated and measured values of N_b (the contribution of the bend) is less than five percent. The agreement in the value of N_b is not as good for small devices in which the effects of oxide thickness and etching variations are more pronounced. This is exemplified by Figure 4.4 which shows the difference in drain current between two 'identical' rectangular transistors on the same die, for several dice.

The data obtained for small devices also demonstrates the sensitivity of bent transistors to misalignment of the

Fig. 4.4: ΔI_d vs I_d plot for two rectangular devices on the same die.

Fig. 4.5: ΔI_d vs I_{dr} curves for two L-shaped IGFETs on the same die showing the effect of misalignment.

polysilicon and field oxide layers. Figure 4.5 shows the difference in ΔI_d vs I_{dr} plots for two L-shaped IGFETs with different orientations on the same die. The value of N_b recorded in Table 4.1 for the SWL device is the average value of N_b of these two devices, and is thus insensitive to misalignment(1).

The drain conductance (g_d) and transconductance (g_m) of bend and rectangular IGFETs are compared in Figures 4.6 and 4.7 respectively. Throughout the triode region, the characteristics again appear identical except for the scaling of the aspect ratio. This is what we would expect as the small signal parameters, g_m and g_d are defined as the derivatives of I_d with respect to V_g and V_d respectively. Since the expression for the drain current of a non-rectangular transistor is the same as that of a rectangular device with an effective aspect ratio, the small signal parameters of a non-rectangular device will be the same as those of the rectangular device modified by the same effective aspect ratio W_e/L_e . Unlike the saturation conductance (see Section 5.2), the transconductance of a non-rectangular IGFET is governed by the same correction factor W_e/L_e in both the saturation and triode region of operation. This is because

(1) In a circuit, however, only one device will be fabricated. Thus, when IGFETs with shapes which are sensitive to misalignment (eg. L and L45 in Fig. 1.1) are used in a circuit, it is necessary to estimate the possible effects of misalignment on the aspect ratio of the device. The circuit must be designed to operate with sufficient electrical margin under a worst case condition.

Fig. 4.6: Drain conductance of rectangular and bent IGFETs.

Fig. 4.7: Transconductance of rectangular and bent IGFETs (SW-family)

gm is a source region controlled parameter and the assumptions made in Chapter 2 are still valid in the source region of a saturated IGFET [7] (2).

The agreement between experimental and theoretical data presented in this chapter verifies the analysis developed in Chapter 2 and leads to the following design methodology. The circuit is first designed assuming that all transistors will be rectangular. If a non-rectangular transistor is included in the layout, the circuit performance will not change from the initial design if the effective aspect ratio of the final device is equal to the original designed value. The next chapter discusses the limitations of this approach caused by saturation and second order effects.

(2) In saturation the boundary of the source region (ie. the region between the source and the drain space charge region) is different than the boundary of the device in the triode region, and thus the effective aspect ratio will also be different. However, for reasonably large devices the difference between the two boundaries will be small and the same correction factor applies. This is confirmed by Figure 4.7 (to one significant digit of the correction factor).

CHAPTER 5

NON-SCALING DEVICE PARAMETERS

5.1 Introduction

The analysis of a non-rectangular IGFET performed in Chapter 2 is valid for a large device operating in the triode and subthreshold regions. For a long channel device, the current in the saturation region is essentially constant, with a value defined by the limit of the triode region model. As the length of the channel decreases, the drain conductance of the device increases, and the associated increase in drain current must be accounted for in an IGFET model. It is found, experimentally (see Fig. 4.3 and 4.5), that the correction factor necessary to describe the saturation drain conductance is different than that used to describe the current in the triode region. Experimental results also indicate that small geometry effects (short channel and narrow width effects) are different for rectangular and non-rectangular IGFETs. Again, this difference cannot be simply related to the triode region parameters. This departure from the triode region analysis arises when certain assumptions made in Chapter 2 become invalid and these effects, in a rectangular IGFET, are two-dimensional in nature. However, these effects can often be described by

simple extensions to the triode region model [2,3,7].

In a non-rectangular IGFET, the causes of the above characteristics become three-dimensional in nature. Without simplifying assumptions to reduce these to two-dimensions, we cannot obtain quantitative results by conformal mapping techniques. Further, the above characteristics do not scale; that is, they depend on the physical device dimensions rather than on a dimension-less parameter such as the aspect ratio. This non-scaling feature is also true of other device parameters such as gate capacitance and drain breakdown voltage. Unfortunately, the dependence of these effects on the physical device dimensions and geometry is different in each case, and no simple rule can be found to simulate all of them with an existing one-dimensional model.

It is also important to note that these properties are not symmetric with respect to the interchange of the source and the drain (see Fig. 4.3). If correction factors are to be used to relate these properties to those of a rectangular device, then the correction factors must depend on the direction of current flow. In order to model these properties a one-dimensional model must be modified to accept a device dependent parameters for each of the above effects and to adjust these parameters according to the direction of current flow in the device.

5.2 Saturation Conductance

When an IGFET enters the saturation region, the gradual channel approximation is no longer valid at the drain end of the device. This results in a change in the effective aspect ratio of the device and appears as a change in the slope of the ΔI_d vs I_d curves (see Fig 4.3. and 4.5).

The most common approach to modelling an IGFET in the saturation region is to divide the model into two parts, a source region where the gradual channel approximation is valid and a drain region where the approximation is not valid [7]. The boundary of the two regions is defined as the point where the horizontal electric field is a specified fraction of the vertical electric field (ie. where the gradual channel approximation is violated to a specified degree). The drain current of the device is calculated by applying the triode model to the source region and correcting by a factor determined from the drain region.

The correction factor for the drain region is based on the observation that the expression for the current density is the same in the source and drain region:

$$\underline{j} = (kT/q) \mu Q_m \text{ grad } V \quad (5.2.1)$$

where μ is an effective mobility which accounts for high field effects and we have neglected the diffusion current. The expression for Q_m in the source region is the same as in the triode model. In the drain region, Q_m , if significant compared with the depletion layer charge, is obtained from a

two-dimensional numerical solution of the physical equations governing the device.

From Figure 4.3, we see that the slope of the ΔI_d vs I_d curve is approximately constant in the saturation region. Thus, it should be possible to derive a correction factor to describe this region in a manner analogous to the correction factor used for the triode region. Unfortunately, problems arise in trying to apply El-Mansy-Boothroyd, or any other available, model directly for this purpose.

The value of grad V (used to define the boundary between the source and drain regions) is not constant along an equipotential in a non-rectangular transistor. Thus the boundary between the source and drain section of the model described above is not an equipotential (1) and the expression for Q_m is no longer a function only of the surface potential, V_s .

The analysis could be modified to define the boundary of the source and drain region as the point at which grad V is a specified fraction of the vertical electric field in the transformed plane. However, since the transformed plane

(1) Of course, it is possible to perform another conformal transformation to map the drain section into a rectangle. However, this is not a simple matter as it would first be necessary to determine the boundary between the source and drain region which is dependent on the bias conditions as well as the shape of the transistor. Further, the value of P is not a constant along the boundary of the source and drain regions so the second transformation does not reduce the problem to a one-dimensional one.

is symmetrical with respect to the interchange of the source and drain, this approach cannot describe the dependence on the direction of current flow (see Fig. 4.3). Finding a solution for the drain saturation current remains a two-dimensional problem.

A conformal mapping can provide qualitative information about the saturation region. (The discussion here is restricted to bent transistors which can be mapped onto a rectangle by relatively simple conformal transformations.) Consider the L-shaped transistor depicted in Figure 5.2.1. The dotted lines represent equipotentials of the surface potential when the device is operating in the triode region. From Chapter 2, these equipotentials will be mapped into straight lines when the boundary of the device is mapped onto a rectangle (Fig. 5.2.1). We now apply the criterion that the boundary of the source and drain region is the point at which the horizontal component of the electric field ($\text{grad } V$) is some fraction ($1/K$) of the vertical electric field (E_v). Assuming that the IGFET is just entering saturation, a locus of constant $\text{grad } V$ in the transformed plane is approximately a straight line (as in the triode region) and the source drain boundary condition can be written as:

$$\begin{aligned} E_v &= K \text{ grad } V(w) \\ &= \frac{K \text{ grad } V(z) T'}{\mu [Q_m - (kT/q) Q_m']} \end{aligned}$$

..... equipotentials in the triode region

- - - source-drain region boundary in saturation

Source and drain can be along side 1 or 2.

Fig. 5.2.1: Comparison of equipotentials in the triode region and the source-drain region boundary.

a). physical coordinate plane

b). transformed coordinate plane

$$\approx K \text{ grad } V(z) T' / \mu Q_m$$

(5.2.2)

where T' is the derivative of the conformal transformation $z = T(w)$ and we have assumed that the drift current dominates. It is the presence of T' in the above equation which causes the source-drain region boundary to deviate from the equipotential as shown by the dashed line in Figure 5.2.1. For regions far removed from the bend, the source-drain region boundary approaches an equipotential, as it is in a rectangular device.

The El-Mansy-Boothroyd model of an IGFET operating in saturation is a two step process. First, the triode model is used to calculate the drain current that would flow if the potential at the source-drain region boundary appeared at the physical drain. The calculated current is then increased by a factor corresponding to the reduction, ΔL , in the length of the source region. This correction factor is dependent on the saturation conductance and the actual drain voltage.

For an IGFET with a bend along its length, the saturation conductance is small (due to the length of the device). Further, the region near the drain is rectangular and we would expect the drain characteristics to be the same as those of a rectangular device. For an IGFET with a bend along its width, Figure 5.2.1 shows that the length of the drain region ΔL is not constant across the device. When the drain is on the outside of the bend, the average value

of ΔL is smaller than for a rectangular device (2) and less increase of the drain current after pinchoff is expected. When the drain is on the inside of the bend, the average value of ΔL is larger than for a rectangular device, and a larger value of the saturation conductance is expected. This is confirmed by Figure 4.3 where the drain conductance is proportional to the slope of the curve.

As stated previously, it is difficult to extend the above qualitative analysis to obtain quantitative results. It is found however, that two very simple rules can be employed to obtain a bound on the size of the saturation conductance of a bent IGFET. These bounds can then be used in performing worst case simulation of circuits which include bent devices.

To calculate the drain conductance, we can differentiate the general expression for the drain current (the integral of equation (5.2.1)) with respect to the drain voltage:

$$g_d = \frac{\partial I_d}{\partial V_d} = \frac{\partial}{\partial V_d} \left(\int_l (kT/q) \mu Q_m \text{grad } V \right) \cdot N \, dl$$

where l is a path across the width of the device. In the triode region, we can apply a conformal transformation and

(2) In a rectangular device, the source-drain boundary would be the same equipotential that the source-drain boundary of the bent device approaches asymptotically, i.e. the dotted line in Figure 5.2.1.

solve for g_d in the transformed plane. This results in:

$$\begin{aligned} g_{db} &= -(W_e/L_e) \frac{\partial}{\partial V_d} \int_{V_s}^{V_d} \mu Q_m dV \\ &= -(W_e/L_e) \mu Q_{md} \\ &= g_{dr}(W_e) \end{aligned} \quad (5.2.3)$$

where Q_{md} is the mobile carrier density at the drain end of the channel. g_{db} is equal to $g_{dr}(W_e)$, the drain conductance of a rectangular transistor of aspect ratio W_e/L_e , as Q_{md} is a function only of V_d . However, when the IGFET enters saturation, Q_{md} is no longer a function only of the surface potential and g_d is no longer equal to $g_{dr}(W_e)$.

It is expected that the portion of a bent transistor far removed from the bend will behave like a rectangular transistor of length L , the actual length of the straight portion of the device. Thus, L_e in (5.2.3) is set equal to L . We assume that the electric field is constant across the width of the device (3), and adjust the value of Q_{md} so that when (5.2.1) is integrated it yields the correct value of drain current. This results in an average value for the minority carrier density of a bent transistor (Q_{mdb}) of:

(3) The goal of this analysis is to relate the characteristics to those of a rectangular device, where this is valid. This assumption will cause an underestimate of the drain conductance when the drain is on the outside of the bend.

$$Q_{mdb} = Q_{mdr} (W_e/W_d)$$

where Q_{mdr} is the minority carrier density at the drain of a rectangular device of length L , and W_d is the physical width of the drain. Substituting this value of Q_{md} into 5.2.3 yields:

$$g_{db,sat} = (W_e/W_d) g_{dr,sat}(W_e) \quad (5.2.4)$$

This expression is compared to the measured value of saturation drain conductance in Table 5.2.1. The experimental value of $g_{d,sat}$ is related to the slope of the ΔI_d vs I_d curves by:

$$\begin{aligned} \text{measured slope} &= \Delta(I_d(b) - I_d(r)) / \Delta I_d(b) \\ &= \Delta I_d(b) / \Delta I_d(r) - 1 \\ &= V_{ds} g_{db,sat} / (V_{ds} g_{dr,sat}) - 1 \\ &= g_{db,sat} / g_{dr,sat} - 1 \quad (5.2.5) \end{aligned}$$

where $g_{dr,sat}$ is the drain conductance of the reference device of dimensions (W/L) . The slope predicted by equation (5.2.4) is

DEVICE	DIE	DRAIN ON OUTSIDE		DRAIN ON INSIDE		
		Experimental Slope	$\frac{W e^2}{W d} - 1$	Experimental Slope	$\frac{W e^2}{W d} - 1$	$\frac{W s}{W} - 1$
LWL	L1	-0.066	-0.106	.037	0.012	0.062
LWL	L2	-0.076		.036		
LWU120	L1	-0.145	-0.200	.034	0.028	0.124
LWU16	L1	-0.150		.021		
SWL	S1	-0.076*	-0.090			
SWL1	S8	-0.066		-0.012	0.006	0.050
SWL2	S8	-0.072		-0.017		
SWU40	S8	-0.135	-0.173			
CW1L		-0.81	-0.824	.75	1.012	0.84
CW3L		-0.30	-0.443	.22	0.115	0.34
CW3L45		-0.17	-0.281	.12	0.081	0.14

* Average of SWU and SWL2

Table 5.2.1 Comparison of Experimental and Predicted Values of $g_{d,sat}$ for a Bent IGFET

$$\begin{aligned}
 \text{slope} &= g_{db,sat}/g_{dr,sat} - 1 \\
 &= g_{dr,sat} (W_e/W_d) (W_e/W) / g_{dr,sat} - 1 \\
 &= \frac{W_e^2}{W W_d} - 1
 \end{aligned}$$

From Table 5.2.1 it is seen that the expression always provides a lower limit of the conductance when the drain is on the outside of the bend. When the drain is on the inside of the bend, the predicted value is below the measured value in half of the cases and so, does not provide an upper bound as desired. However, the value of $g_{d,sat}$ predicted by this equation is within 10 per cent of the measured value and this should be adequate for most design purposes.

If a definite upper bound is required, the drain conductance of a bent IGFET has been found to be smaller than that of an IGFET with a width equal to the source width of the device (see Table 5.2.1):

$$g_{db,sat} < g_{dr,sat} (W_s/W_e)$$

Another method of modelling the change of saturation conductance is to change the length of the device. In the earlier discussion, it was pointed out that the average length of the drain region in a bent transistor is larger than that of a rectangular transistor when the drain is on

the inside of the bend. Entering a length shorter than the physical length of the straight portions into the model will achieve the same effect. When the drain is on the outside of the bend, the lower saturation conductance can be modelled by slightly increasing the length entered into the model (5). Unfortunately, no easy method has been found to calculate the amount by which the length should be increased or decreased.

5.3 Short Channel Effects

The analysis of an IGFET in Chapter 2 assumed that the depletion layer charge, Q_b , could be expressed as a function of the surface potential. This implies that Q_b is caused entirely by the gate electric field (ie. that the gradual channel approximation applies) and is a valid assumption near the center of the channel. Near the source and drain boundaries, a significant fraction of the depletion layer charge is supported by the electric field associated with the reversed biased source or drain junction [2]. This interaction of the gate and source or gate and drain electric fields appears as a reduction in the threshold voltage of the device. This threshold voltage shift becomes signif-

(5) This can be seen to occur experimentally in Figure 4.4 where the etching variation across the die has produced two rectangular transistors of slightly different lengths. The curves for die 8 and die 2 resemble the ΔI_d vs I_d curves of a bent vs rectangular transistor.

icant for devices with small channel lengths and is termed the short channel effect.

The magnitude of this threshold voltage shift is dependent on the three-dimensional geometry of the source and drain junctions, (1). This difference manifests itself in two ways. First, it is observed that there is a smaller V_t shift in a bent transistor than in a rectangular device having the same length as the straight portion of the bent device. This appears as a change in slope of the ΔI_d vs I_d curve as the substrate bias is changed as shown in Figure 5.3.1. Second, the source and drain periphery are of different width. Since the width of the junction depletion layer is bias dependent, there will be a larger fraction of the gate charge supported by the junction field when the drain is on the outside of the bend than when it is on the inside of the bend. This causes a separation of the ΔI_d vs I_d curves in the linear region of operation (see Fig. 5.3.1).

The first effect can be easily incorporated into a one-dimensional model by increasing the gate area of the device to compensate for the reduced interaction between the electric fields while maintaining the same aspect ratio (W_e/L_e). The second effect is small and modelling it is not necessary.

(1) This parameter will be significant in IGFETs with a bend along their width only.

Fig. 5.3.1 (a): Difference in short channel effects for rectangular and L-shaped IGFETs; $V_{bs}=0$, $V_{gs}=5.5$ V

Fig. 5.3.1 (b): Difference in short channel effects for rectangular and L-shaped IGFETs; $V_{bs} = -15V$, $V_{gs} = 7.2V$.

5.4 Narrow Width Effects

Narrow width effects are caused by fringing of the electric field at the sides of the IGFET. This gives rise to an increase in the depletion layer charge, and hence, to an increase in the threshold voltage [3]. An IGFET with a tapered field oxide will also appear to widen as the gate voltage increases as the inversion layer spreads under the field oxide layer.

Narrow width effects were observed in transistors with a bend along their length. The straight portion of the device has the same narrow width characteristics as the equivalent rectangular transistor. The fringing pattern on the outside of the bend will support a smaller Q_b per unit length than the rectangular portions. The fringing pattern on the inside of the corner is shared between the two adjacent sides, again resulting in a smaller Q_b than for the rectangular regions (1). For a tapered edge, the spreading of the depletion layer also changes the effective radius of curvature of the corner. Further investigation is required to obtain quantitative results of narrow width effects in bent IGFETs.

(1) The inside of the corner is more important as this is where the current density is the highest. Both the V_t shift and the change in corner radius cause a curvature in the linear region of the ΔI_d vs I_d curves. (see Fig. 5.4.1)

Fig. 5.4.1: Narrow width effects in an L-shaped IGFET (NLL)

5.5 Gate Capacitance

The gate capacitance of an IGFET is defined to be:

$$\begin{aligned}
 C_g &= \left. \frac{dQ_g}{dV_g} \right|_{V_s, V_d, V_b} \\
 &= - \iint_S \frac{\partial}{\partial V_g} [Q_m(V) + Q_b(V)] ds \\
 &= \iint_S \frac{\partial}{\partial V_g} [C_{ox}(V_g - V)] ds \\
 &= C_{ox} \iint_S \left[1 - \frac{\partial V}{\partial V_g} \right] ds \quad (5.5.1)
 \end{aligned}$$

where C_{ox} is the oxide capacitance and the surface S is the oxide-semiconductor interface.

Equally, C_g can be defined in terms of the derivatives with respect to V_s , V_d , and V_b :

$$\begin{aligned}
 C_g &= C_{gs} + C_{gd} + C_{gb} \\
 &= -\partial Q_g / \partial V_s - \partial Q_g / \partial V_d - \partial Q_g / \partial V_b \quad (5.5.2)
 \end{aligned}$$

These are components of the complete capacitance matrix of the device that is necessary in practical IGFET models [15].

When the channel region is depleted ($V_g < V_t$) or when $V_d = V_s$, dV/dV_g is constant throughout the channel. Equation (5.5.1) reduces to:

$$C_g = C_{ox} (1 - dV/dV_g) A_s \quad (5.5.3)$$

where A_s is the area of the gate plane geometry.

When the channel is inverted and $V_d \neq V_s$, dV/dV_g is a function of position and equation (5.5.1) cannot be solved easily for an arbitrary gate geometry. In the triode region, conformal mapping techniques can be used to solve for the surface potential V . However, ds is modified by T' , the derivative of the conformal transformation and the expression for the gate capacitance in the transformed plane is:

$$C_g = C_{ox} \int_0^{W_e} \int_0^{L_e} \left[1 - \frac{\partial V(z)}{\partial V} \right] \frac{1}{(T')^2} dx dy \quad (5.5.4)$$

$$= C_{ox} \left(A_s - \int_0^{W_e} \int_0^{L_e} \frac{\partial V(z)}{\partial V_g} \frac{1}{(T')^2} dx dy \right)$$

In saturation, the only significant component of gate capacitance is C_{gs} and equation (5.5.4) becomes:

$$C_g \approx C_{gs} \approx -C_{ox} \iint_{S_s} \left[1 - \frac{\partial V(z)}{\partial V_g} \right] \frac{1}{(T')^2} dx dy \quad (5.5.5)$$

where S_s is a surface corresponding to the source region of the device, which again is bias dependent.

Unfortunately, these equations could not be verified as the experimental measurements of gate capacitance (see Fig. 5.5.1 to Fig. 5.5.3) exhibited high frequency characteristics (the inversion capacitance is not equal to the accumulation capacitance). The value of capacitance in the

Fig. 5.5.1: Gate capacitance of a rectangular IGFET ($V_{bs}=0$)

Fig. 5.5.2: Gate capacitance of an L-shaped IGFET,
drain on outside of bend ($V_{bs} \neq 0$)

Fig. 5.5.3: Gate capacitance of an L-shaped IGFET, drain on inside of bend ($V_{bs}=0$)

accumulation region (far left in Fig. 5.5.1 to Fig. 5.5.3) is equal to C_{ox} as expected. The capacitance is equal in all three cases which verifies equation (5.5.3). In the saturation region, the gate capacitance is experimentally measured to be proportional to the gate area between the drain and a line 0.7 of the distance from the drain to the source which agrees with a simplified analysis along the lines of Sah [16]. It is necessary to perform capacitance measurements at a lower frequency before anything definite can be said about the gate capacitance of a non-rectangular IGFET.

5.6 Drain Breakdown Voltage

Two mechanisms exist for drain breakdown in IGFETs: avalanche breakdown and punchthrough. Both of these effects are governed by three-dimensional electric fields in the semiconductor and are difficult to analyse quantitatively (1). It is expected that avalanche breakdown will occur at a lower drain voltage when the drain is on the inside of the bend. In this case, the electric field is larger at the corner than along the straight portion of the device. When the drain is on the outside of the bend, the electric field at the corner is lower than the electric field of the straight portion, and the straight portion will break down

(1) As with the short channel effect, these are significant only in devices which have a bend along their width.

first. Similarly, the source to drain junction separation is less in the straight portion of the device than at the bend. Thus, punchthrough will occur in the straight portion before it occurs at the corner.

Figure 5.6.1 compares the breakdown of 6 μm rectangular (a) and bent device with the drain on the inside (b) and outside (c) of the bend. The difference in breakdown voltage is less than half a volt in all three cases. This implies that the straight portions of the device are breaking down first. (Avalanche breakdown does not occur at a low drain voltage when the drain is on the inside of the bend because of a relatively large rounding of the gate corner (3 μm) when compared to the radius of curvature of the junction (1 μm).)

It is concluded that no special treatment of drain breakdown is necessary for devices in processes where the radius of curvature of the gate corner is approximately three times the radius of curvature of the junction. However, the drain breakdown voltage is process dependent and an investigation should be performed to confirm the above observations in any given process.

(a)

(b)

(c)

Fig. 5.6: Drain junction breakdown of rectangular and L-shaped IGFETs

- a) rectangular (SWR)
- b) L; drain on inside (SWL)
- c) L; drain on outside (SWL)

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CHAPTER 6

CONCLUSIONS

6.1 Summary

It has been shown that conformal mapping techniques can be employed to calculate a steady state solution of Poisson's equation if the charge density can be expressed as a scalar function of the potential. This allows us to analyse an IGFET in the triode and subthreshold regions by conformal mapping methods. The result of this analysis is that the expression for the drain current of a non-rectangular device is equivalent to the expression for a rectangular IGFET with W/L replaced by an effective aspect ratio. Thus, it is possible to model a non-rectangular IGFET with existing one-dimensional IGFET models which were derived assuming a rectangular geometry.

The effective aspect ratio of a non-rectangular transistor can be calculated as the width to length ratio of the rectangle that the boundary is mapped into by a conformal transformation. This allows us to apply the results of conformal mappings of resistors and capacitors directly to IGFETs. For geometries which cannot easily be transformed into a rectangle, the aspect ratio of the device can be calculated by two-dimensional numerical methods.

A number of bent transistors were fabricated to verify the above theory. The measured drain current is found to agree excellently with the predicted value in the triode and subthreshold regions.

When the IGFET enters saturation, the gradual channel approximation is no longer valid near the drain. This results in a change in the correction factor required to relate non-rectangular IGFETs to rectangular devices. A qualitative analysis is presented which provides limiting values for the drain conductance in the saturation region.

The other non-scaling device parameters investigated are short channel and narrow width effects, gate capacitance, and drain breakdown voltage. Both short channel and narrow width effects were found to be smaller in bent IGFETs than in rectangular devices. An expression was derived for the gate capacitance of a non-rectangular IGFET. Unfortunately, reliable experimental data were not available to confirm these relationships. Finally, for devices of the size investigated (6 μm) the drain breakdown voltage of a bent IGFET was found to be equal to that of a rectangular device.

6.2 Designing With Non-rectangular IGFETs

The fact that the expression for the drain current of an IGFET is independent of the gate plane geometry implies that the design methodology used informally by IC designers

(see Chapter 1) is in fact, valid.

The circuit can first be designed assuming that all transistors will be rectangular. If it is convenient, a non-rectangular device can be inserted at the layout stage. The effective aspect ratio of the non-rectangular device is made equal to designed value of W/L . If the device is a simple geometry, its aspect ratio can be calculated from a dictionary of effective aspect ratios [8]. The effective aspect ratio of complicated geometries can be calculated by two-dimensional numerical methods.

The designer can then apply the qualitative analysis of Chapter 5 to determine if the current predicted by a one-dimensional model will be an under or over estimate. For example, the saturation conductance of a bent device will be smaller than that predicted by a one-dimensional model if the drain is on the outside of the bend, larger if the drain is on the inside of the bend. If the corresponding decrease (increase) in current will, increase the electrical margin of the circuit, no further analysis is necessary. If the circuit margin is decreased by this shift, the circuit can be resimulated with the saturation conductance replaced by its lower (upper) bound to determine the worst case circuit margin. In determining the worst case margin, the designer must also include the effects of possible misalignment of the mask levels during processing.

Finally, the designer may want to use bent devices to obtain a performance, as well as area, enhancement. For

example, if a small signal circuit parameter of interest is governed by the saturation drain conductance, the parameter can be increased by placing the drain on the inside of a bend while at the same time having the current through the device, and hence the power consumption, decrease.

6.3 Suggestions for Further Studies

The quantitative analysis presented in this thesis is restricted to a large device operating in the triode and subthreshold regions. An IC designer cannot realize the full potential of non-rectangular IGFETs until quantitative results are available for the non-scaling device parameters discussed in Chapter 5.

While limiting values of the saturation drain conductance can be used to obtain operational circuits, accurate prediction of the saturation conductance is necessary to characterize a cell by simulation techniques; no such limiting values were placed on short channel or narrow width effects. Further study is also required of the gate capacitance to find a method, possibly numerical, of relating the components of the gate capacitance of a non-rectangular IGFET to those of a rectangular device.

Finally, the method of relating Poisson's and Laplace's equation described in Chapter 2 could be extended to other non-rectangular geometries such as VMOS devices.

APPENDIX 1

PROGRAM LISTING OF LAPLACE2

```

C 2D SOLUTION OF LAPLACE'S EQUATION BY FINITE
C DIFFERENCE METHOD.
C ALSO CALCULATES EFFECTIVE W/L OF SHAPE
C
C EXPECTED FORMAT FOR DATA FILE:
C
C MAXX,MAXY,NCL,DELTA,SCALE
C INITIAL VALQES (MAXX*MAXY)
C
C CL (NCL*2) CENTERLINE OVER FOR EFFECTIVE W/L
C
DOUBLE PRECISION P(200,200),B(100,100),CORNER(10,5)
INTEGER CL(25,2),SCALE
READ(15,*) MAXX,MAXY,NCL,DELTA,SCALE,NRC
READ(15,*) ((P(I,J),I=1,MAXX),J=1,MAXY)
READ(15,*) ((CL(I,J),J=1,2),I=1,NCL)
IF(NRC.LT.1) GO TO 28
READ(15,*) ((CORNER(I,J),J=1,5),I=1,NRC)
RO=10000
19 IF(NRC.LT.1) GO TO 28
DO 27 I=1,NRC
NCLX=CORNER(I,1)
NCLY=CORNER(I,2)
NCUX=NCLX+DABS(CORNER(I,3))
NCUY=NCLY+DABS(CORNER(I,3))
NCX=CORNER(I,1)
NCY=CORNER(I,2)
IF(CORNER(I,3).LT.0) NCX=NCX-CORNER(I,3)
IF(CORNER(I,4).LT.0) NCY=NCY-CORNER(I,4)
RSQOLD=(CORNER(I,3)+RO)**2
RSQNEW=(CORNER(I,3)+.353)**2
DO 27 J1=NCLX,NCUX
DO 27 J=NCLY,NCUY
D=(J1-NCX)**2+(J-NCY)**2
27 IF(D.LE.RSQOLD.AND.D.GE.RSQNEW) P(J1,J)=CORNER(I,5)
28 RO=1
CALL LAPLCE(P,DELTA,MAXX,MAXY)
CALL SFLUX(P,CL,NCL,FLUX,D)
WRITE(16,30) FLUX,D
WRITE(16,31) ((CL(I,J),J=1,2),I=1,NCL)
SCALE=SCALE-1

```



```

      IF(SCALE.LT.0) GO TO 20
C      REFINE NET
      DO 23 I=1,MAXX
      DO 23 J=1,MAXY
23      B(I,J)=P(I,J)
      MAXXM1=MAXX-1
      MAXYM1=MAXY-1
      DO 21 I=1,MAXXM1
      I2=I+I
      I2M1=I2-1
      DO 21 J=1,MAXYM1
      J2=J+J
      J2M1=J2-1
      P(I2M1,J2M1)=B(I,J)
      P(I2M1,J2)=(B(I,J)+B(I,J+1))/2
      P(I2,J2M1)=(B(I,J)+B(I+1,J))/2
21      P(I2,J2)=(B(I,J)+B(I,J+1)+B(I+1,J)+B(I+1,J+1))/4
      MAX2X=MAXX+MAXX-1
      MAX2Y=MAXY+MAXY-1
      P(1,MAX2Y)=B(1,MAXY)
      P(MAX2X,1)=B(MAXX,1)
      DO 25 I=1,MAXXM1
      P(I+I,MAX2Y)=(B(I+1,MAXY)+B(I,MAXY))/2
25      P(I+I+1,MAX2Y)=B(I+1,MAXY)
      DO 26 I=1,MAXYM1
      P(MAX2X,I+I)=(B(MAXX,I)+B(MAXX,I+1))/2
26      P(MAX2X,I+I+1)=B(MAXX,I+1)
      DO 22 I=1,NCL
      CL(I,1)=(CL(I,1)-1)*2+1
22      CL(I,2)=(CL(I,2)-1)*2+1
      MAXX=MAXX*2-1
      MAXY=MAXY*2-1
      IF(NRC.LT.1) GO TO 19
      DO 29 I=1,NRC
      CORNER(I,1)=CORNER(I,1)*2-1
      CORNER(I,2)=CORNER(I,2)*2-1
      CORNER(I,3)=CORNER(I,3)*2
29      CORNER(I,4)=CORNER(I,4)*2
      GO TO 19
20      WRITE(17,32) ((P(I,J),I=1,MAXX),J=1,MAXY)
30      FORMAT('1','FLUX=',F15.6,'D=',F10.1/'0','CENTERLINE'/)
31      FORMAT(' ',2I10)
32      FORMAT(' ',10F7.4)
      STOP
      END

```

```

C
C      SUBROUTINE LAPLCE(P,DELTA,MAXX,MAXY)
C
C      P=POTENTIAL MATRIX, 0 OR 10 = BOUNDARY VALUE
C      DELTA= CONVERGENCE CRITERIA
C      MAXX,MAXY=X,Y DIMENSION OF P (ACTUAL DIM=200*2)
C
      DOUBLE PRECISION P(200,200),A,S1,S2

```

```

MAXXM2=MAXX-2
MAXXM1=MAXX-1
MAXYM2=MAXY-2
MAXYM1=MAXY-1
C   SET ITERATION COUNT
NITER=0
C   SET NEUMANN BC
10  DO 11 I=1,MAXY
    P(1,I)=P(3,I)
11  P(MAXX,I)=P(MAXXM2,I)
    DO 12 I=1,MAXX
        P(I,1)=P(I,3)
12  P(I,MAXY)=P(I,MAXYM2)
C   SOLVE NET FOR INCREASING INDEX WITH '20' FORMULA
    DO 14 J=2,MAXYM1
        DO 14 I=2,MAXXM1
            IF(P(I,J).EQ.0.OR.P(I,J).EQ.10) GO TO 14
            S1=P(I,J+1)+P(I,J-1)+P(I-1,J)+P(I+1,J)
            S2=P(I-1,J-1)+P(I-1,J+1)+P(I+1,J-1)+P(I+1,J+1)
            P(I,J)=(4*S1+S2)/20
14  CONTINUE
    FCONV=0
C   SET BOUNDARY FOR SECOND PASS
    DO 15 I=1,MAXY
        P(1,I)=P(3,I)
15  P(MAXX,I)=P(MAXXM2,I)
        DO 16 I=1,MAXX
            P(I,1)=P(I,3)
16  P(I,MAXY)=P(I,MAXYM2)
C   SOLVE NET FOR DECREASING INDEX
    DO 13 NJ=1,MAXYM2
        DO 13 NI=1,MAXXM2
            J=MAXY-NJ
            I=MAXX-NI
            A=P(I,J)
            IF(A.EQ.0.OR.A.EQ.10) GO TO 13
            S1=P(I,J+1)+P(I,J-1)+P(I-1,J)+P(I+1,J)
            S2=P(I-1,J-1)+P(I-1,J+1)+P(I+1,J-1)+P(I+1,J+1)
            P(I,J)=(4*S1+S2)/20
            IF(DABS(A-P(I,J)).GT.DELTA) FCONV=FCONV+1
13  CONTINUE
C   CHECK ITERATION COUNT AND CONVERGENCE
    NITER=NITER+1
    IF(NITER.LT.200.AND.FCONV.GT.0) GO TO 10
    IF(FCONV.GT.0) WRITE(16,30) FCONV,DELTA
30  FORMAT('1','FCONV=',F10.0,'FOR DELTA=',F9.6)
    RETURN
    END

```

C
C

SUBROUTINE SFLUX(P,CL,NNCL,FLUX,D)

C
C
C
C

SUBROUTINE TO CALCULATE THE FLUX CROSSING A LINE

C
DOUBLE PRECISION P(200,200)
INTEGER CL(25,2)
D=0
NCL=2
NX=1
NY=0
IX=CL(1,1)
IY=CL(1,2)
FLUX=-(P(IX,IY)-P(IX,IY-1))/2
11 FLUX=FLUX+P(IX-NY,IY)-P(IX,IY-NX)
D=D+1
IX=IX+NX
IY=IY+NY
IF(IX.EQ.CL(NCL,1).AND.IY.EQ.CL(NCL,2)) GOTO 10
IF(IX.GT.200.OR.IY.GT.200)GO TO 12
GO TO 11
10 NCL=NCL+1
NX=1-NX
NY=1-NY
IF(NCL.LE.NNCL)GO TO 11
FLUX=FLUX+(P(IX-NX,IY)-P(IX,IY-NY))/2
RETURN
12 FLUX=99999
RETURN

END

APPENDIX 2

SAMPLE DATA FILE FOR LAPLACE2

[illegible]

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END

0 610 6.8 3

FIN