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ASYNCHRONOUS SAMPLING WATTMETER

by

Philip William Jones

A thesis submitted to the Faculty of Graduate Studies
and Research in partial fulfillment of the requirements
for the degree of

Master of Engineering

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada

August, 1992

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ASYNCHRONOUS SAMPLING WATTMETER

submitted by Philip William Jones
in partial fulfillment of the requirements for
the degree of Master of Engineering

Thesis Supervisor

Chair, Department of Electronics

Carleton University
September 11, 1992

ABSTRACT

This thesis is concerned with the design and construction of a wattmeter/watthour meter utilizing asynchronous sampling and two processors operating in tandem. One processor is a digital signal processor with a fast multiplier, capable of creating and storing the sum-of-products for ΣV^2 , ΣI^2 and $\Sigma V.I$ for three phases over a large number of cycles. The other processor is a microcontroller which uses the stored data to calculate and display 8 power parameters for each of the three phases. One of the parameters is frequency, which is measurable in the range of 34 to 63 hertz. The meter has an accuracy of better than approximately 0.03% for periodic nonsinusoidal waveforms having up to 50 harmonics.

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P. W. J.

August, 1992

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CHAPTER 1
INTRODUCTION

1.1: Background

Electrical power is one of the great resources of Canada. There are large hydro-electric generation sites and reserves in many areas of Canada, especially in the North. Canadian utility companies supply large amounts of power for consumption either within Canada or south of the border. In order to sell electrical power effectively, means must exist for accurately measuring that power.

This thesis is concerned with such power measurement. It will point out some of the problems with present measuring instruments and some ways of overcoming them.

The type of meter employed for electrical power measurement depends on the electrical value being measured and on the accuracy required in the measurement. Wattmeters are used for measuring power or energy flow, whereas watt-hour meters are used for measuring power or energy consumed over an interval of time. Electrical utilities are also interested in a number of power-related measurements. The peak power used over short periods (15-minute periods are often selected) is important since the size of supply wiring and transformers needed by a customer is partially determined by the customer's peak load. Capacitive or inductive loads cause a reactive power to flow back and forth in the supply wiring. This so-called reactive power does not perform useful work, and its presence is not sensed on a wattmeter. However, it may result in a need for larger wiring and transformers, so utility companies are very interested in measuring reactive power. The apparent power and the power factor, both of which will be defined subsequently, are related to the reactive power and are also of interest.

The accuracy required of a wattmeter or a watthour

meter depends on a number of factors. For instance, a house normally consumes a relatively small amount of power when compared to an office building or a factory. Therefore, a meter used to measure the amount of power consumed over time by a household would be expected to be less accurate than a meter used to measure the amount of power consumed over time by a factory or an office building. Similarly, even more accurate meters would be expected to monitor the quantity of power which passes through transmission lines that connect power utility companies, for instance, the lines that connect Ontario Hydro and Quebec Hydro. For a typical house a 1% error in measuring 1,000 kilowatthours (kWh) at \$0.05 per kWh equates to only \$0.50, whereas for a power company a 1% error in measuring 1,000 gigawatthours (GWh) might equate to approximately \$100,000. The ultimate accuracy in wattmeters and watthour meters is found in institutions that provide calibration standards, such as the National Research Council. It goes without saying that the more accurate the wattmeter or watthour meter used, the greater the cost of the meter. For instance, the mechanical watthour meter found in most homes costs less than a hundred dollars and has an accuracy on the order of one percent. Calibration meters found in institutions such as the National Research Council have an accuracy about one thousand times greater, and may cost tens of thousands of dollars.

The construction of wattmeters and watthour meters has evolved with the introduction of new technologies. The original types of wattmeters and watthour meters were mechanical, and because of their simplicity and low cost such meters remain in heavy use. The circuitry and operation of a simple single-phase mechanical wattmeter is illustrated in Figure 1.1.

Mechanical wattmeters and watthour meters suffer from a series of disadvantages that limit their accuracy. Movement of a spindle or a disc converts a small amount of

FIGURE 1.1:
THE CIRCUITRY OF A SINGLE-PHASE MECHANICAL WATTMETER

In this meter, the current feeding the load generates a magnetic field by means of coils L1 and L2. These coils have a very low impedance, so the current is essentially determined by the load. The potential across the load drives a small current through coil L3, which has a high resistance and generates a field proportional to load voltage. Coils L4 and L5 act to reduce the load current by the small current passing through coil L3, and thus compensate for the current required to run the wattmeter. The instantaneous torque on the rotating coil L3 is proportional to the product of the load current and load potential, i.e. the instantaneous power. The rotation integrates the instantaneous power to give watthours. As it moves under the permanent magnet, the aluminum disc generates eddy currents which act as a continuous brake on its rotation and thus the rotation of coil L3.

energy to friction, which may introduce significant error if the meter is reading low values. Also, due to inertia a spindle or disc will continue to rotate momentarily after removal of the energy field, creating a further inaccuracy. Further, the interaction of the magnetic fields on mechanical meters will vary slightly with the relative position of the coils; the disc of the mechanical watthour meter has to be individually trimmed in each meter to obtain the best result. Variation in temperature may also affect the relative movement of the mechanical parts.

The advent of electronics introduced wattmeters based on the multiplication of analog signals proportional to voltage and current. One type of analog electronic meter, capable of 0.1 percent accuracy or better, is based on a pulse-area principle. Pulses are generated with a height proportional to the load current, and a pulse duration proportional to the load voltage. The area is then proportional to power, and the integral of the area is proportional to watthours (energy). Figure 1.2 shows the operation of a meter, described in a 1974 United States patent [MAR, 1974], that utilizes this principle.

Limitations on the accuracy of analog electronic wattmeters stems from the difficulty of obtaining analog components having an accuracy above approximately 0.1%. Higher accuracy requires extra care, hand calibration, and controls on temperature and other environmental factors. Analog wattmeters having an accuracy above approximately 0.2% are very difficult to build.

1.2: Digital Wattmeters

The introduction within the last decade or so of inexpensive, high-accuracy operational amplifiers, analog-to-digital (A/D) converters, and single-chip processing

FIGURE 1.2: WAVEFORMS IN AN ANALOG ELECTRONIC WATTMETER

In this meter, the input voltage waveform and a generated triangular control waveform are the inputs to a comparator which has an output that controls an electronic switch through which is fed the current waveform. If ' T ' is the time taken between peaks of the triangular control waveform and ' t ' is the time during which the voltage waveform has a voltage above that of the control waveform, then the width of the hatched areas is a function of t/T , i.e. the width varies with the magnitude of the input voltage waveform. Since the height of hatched areas varies with the magnitude of the input current waveform, the area of the hatched areas is proportional to the product of the input voltage and current waveforms.

devices has led to the introduction of digital electronic wattmeters and watthour meters. By sampling instantaneous voltage and current values, digital electronic wattmeters are capable of determining not only active power, but also apparent power and thus the power factor. The addition of a timing algorithm allows such wattmeters to also act as watthour meters, measuring energy consumption and peak demand. The choice of a sampling period synchronized to an external clock may also provide a means for determining the frequency of the measured signal.

A band-limited signal having no frequencies in its spectrum above F hertz is determined uniquely by sampling values of the signal at uniform intervals spaced no greater than $1/(2F)$ apart, i.e. sampling at or above the Nyquist sampling frequency. In other words, if a signal has a frequency spectrum of up to 10 hertz, sampling the signal at least 20 times per second should allow one to exactly determine the signal. By using a phase-lock loop circuit, one may synchronize sampling of a waveform to the period of the waveform and by sampling at more than twice the highest frequency component one can, in theory, exactly determine the waveform. The difficulty with using synchronous sampling to obtain an exact measure of the power represented in voltage and current waveforms is that the highest frequency harmonic in such waveforms may be very high. Although the voltage waveform seen by an end-user may closely resemble the steady-state sinusoidal waveform that is produced at a power company and has little harmonic content, the current waveform is often nonsinusoidal due to the effect of motor controllers and rectifiers. Switching loads may produce step changes and spikes. Though the current waveform maintains the periodicity of the voltage waveform, nonlinearities may result in harmonics at very high frequencies. For example, Figure 1.3 illustrates a series of simulated nonsinusoidal current waveforms used by the National Research Council of

FIGURE 1.3: SIMULATED CURRENT WAVEFORMS USED FOR TESTING
WATTMETERS AT THE NATIONAL RESEARCH COUNCIL OF CANADA

Canada for testing the accuracy of wattmeters and watthour meters [FIL, 1988].

1.2.1: Synchronous Sampling

Each of the current waveforms illustrated in Figure 1.3 has been created from a very high number of harmonics of the fundamental frequency. A unique determination of each waveform should be possible by using synchronous sampling with a Nyquist sampling frequency at least twice as high as the highest harmonic in the waveform. Such unique determination might be difficult, if not impossible, for the current waveforms of Figure 1.3 because of the high frequency of the harmonics represented in those waveforms. If one synchronously samples a periodic waveform that is known to contain harmonics with a maximum frequency greater than half the sampling rate, an 'aliasing error' will be present. Another error in synchronous sampling results from phase jitter, as the phase-lock loop circuitry attempts to lock onto the sampled waveform.

1.2.2: Asynchronous Sampling

An alternate way to sample repetitive periodic waveforms with very high frequencies is to asynchronously sample such waveforms over a large number of periods of the waveform. Asynchronous sampling refers to sampling a waveform at time intervals that are set by an external clock and are independent of the period of the sampled waveform. The recent advent of relatively-cheap digital signal processing chips, containing fast multipliers and capable of using a range of powerful multiply/accumulate instructions at high clock speeds, suggested an asynchronous sampling scheme cap-

able of measuring the power in voltage and current waveforms with very high harmonics. Asynchronous sampling can, for repetitive waveforms, include the effects of high frequency harmonics using a much lower sampling rate than synchronous sampling.

Asynchronous sampling over a number of periods of a waveform is illustrated by use of Figure 1.4, in which five periods of a repetitive periodic waveform are illustrated. Because the asynchronous sample spacing is generally set by a clock external to the sampled waveform, the position at which the final asynchronous sample in the fifth period is taken normally differs slightly from the position at which the first asynchronous sample is taken in the first period. This error (referred to as 'truncation error' in the literature on asynchronous sampling; see Chapter 2) can be made very small if the time between samples is chosen such that a multiple of that time closely approximates the duration of a discrete number of sampled waveform periods. With respect to Figure 1.4, the effect of the asynchronous sampling is that 24 samples/period are effectively obtained by slower sampling over 5 periods. More generally, if N total samples are gathered over C periods of a repetitive periodic waveform it is shown in Chapter 2 that the maximum 'truncation error' from such sampling approximates $1/N$, i.e. the larger the number of samples used, the smaller the maximum error. The number of harmonic frequencies that are represented in the result will be larger with asynchronous sampling than with synchronous sampling since a period will have effectively been sampled at N samples/period rather than the actual N/C samples/period.

FIGURE 1.4: EXAMPLE OF ASYNCHRONOUS SAMPLING

1.3: The Meter Constructed for this Thesis

In this work, a combination meter was constructed which was switchable between asynchronous and synchronous sampling. The two types of measurement can be compared.

The meter may be used asynchronously on signals having a fundamental frequency up to approximately 63 Hz; that range covers the major fundamental frequencies of power transmission. Parameters may be measured in up to 3 phases simultaneously, and any of them individually displayed. The meter can sense how many phases (1, 2 or 3) are being simultaneously measured, and a total or average value of the particular parameter over the measured phases can be displayed. For instance, a total value for the power consumption over the measured phases can be displayed, whereas an average value for the power factor over the measured phases can be displayed. A calibration mechanism is part of the meter; using that mechanism, the meter calculates multiplication constants from initially-entered high-precision voltage and current inputs, and uses those constants to evaluate the magnitude of subsequent voltage and current inputs.

Two processors are used in tandem, one to continuously gather data and the other to analyze that data at defined intervals. The arrangement is optimized to measure the power in a three-phase electrical system operating at a nominal frequency of 60 hertz. Variable conditioning of the input voltage and current, in association with a software calibration algorithm, allows the wattmeter/watthour meter to be utilized with a wide range of voltages and currents. The system is optimized, however, to measure a RMS voltage of 120 volts and a RMS current of 5 amperes. Those values were selected because utility companies normally sample power in their transmission lines by using voltages and currents reduced through very high quality instrument transformers to those ranges.

The data gathering processor is a Texas Instruments' TMS320C25 digital signal processing chip operating with a cycle time of 100 nanoseconds. This processor scans incoming digitized voltage values for zero-crossings, and during an interval between selected zero-crossing uses large internal memory registers for summing successive values of V^2 , I^2 and $V.I$ computed from voltage and current samples taken in that interval. After each interval, the summed V^2 , I^2 and $V.I$ values -- as well as some other values -- for the three phases are written to a memory area that is external of the TMS processor and is accessible for a read operation by the analyzing processor. The summed values and sample count in the interval between the selected zero-crossings are then used by the analyzing processor in calculating V_{RMS} and I_{RMS} . Since the number of asynchronous samples gathered over a selected number of voltage waveforms at 60 Hz may be calculated, the sample count can also be used to calculate the frequency of the voltage waveform.

The algorithm used in the data gathering processor allows other features of the voltage and current waveforms to be tracked, including the peak voltage and current values during the sampling interval and the comparative position of those values in the voltage and current waveforms. The latter comparison allows a determination to be made as to whether a power factor calculated using the V^2 , I^2 and $V.I$ summed values is capacitive or inductive.

The analyzing processor, an Intel 8096 microcontroller chip, performs an analysis on each set of summed values during the time that the data accumulating processor is gathering the next set of summed values. The analysis provides values for V_{RMS} , I_{RMS} , Apparent Power, Active Power, Power Factor, Frequency, Power Consumption, and 15-Minute Peak Power Demand. Each of the 8 parameters is calculated for each of the 3 phases, as well as a total (or average) value for each of the 8 parameters. The resulting 32 values

are selectively presentable on a 12-character LED display according to the setting on a pair of dials, one for parameter selection and one for phase selection. An autoranging algorithm is used for properly positioning the parameter values on the LED display.

Tests were conducted at the National Research Council of Canada to compare the accuracy of measurements from the wattmeter/watthour meter against known standards. The accuracy of the meter was found to be in the order of 0.03 percent for 60-hertz waveforms.

The next chapter of the thesis will describe the theory behind the operation of this meter. Then, a short literature survey is presented, followed by chapters on the design and construction of the meter. The final chapters relate to the the test results and some conclusions.

CHAPTER 2

THEORY

The Introduction described in general terms how the wattmeter/watthour meter of this thesis utilizes a digital signal processing device and microcontroller device to collect at high speed a series of discrete voltage and current values, and to then calculate and display a series of parameters based on those values. This chapter first describes the general equations relating to power measurement, then those relating to the power in periodic sinusoidal and non-sinusoidal waveforms. Next, differences between synchronous and asynchronous sampling of waveforms are described, including the errors in such sampling. The chapter then develops the equations that are used to transform asynchronously sampled voltage and current waveforms into a series of power parameters, including active power, apparent power, power factor, frequency and 15-min. kVA demand.

2.1: The Power Equations

2.1.1: Generally

The instantaneous electrical power produced by a voltage waveform $e(t)$ driving a current waveform $i(t)$ can be expressed at any point in time as:

$$P_{inst} = e(t) \cdot i(t) \quad (\text{EQUATION 1})$$

and the energy transferred in the two waveforms over a time interval 'T' can be expressed as:

$$\text{Energy} = \int_0^T e(t) \cdot i(t) \cdot dt \quad (\text{EQUATION 2})$$

The average electrical power contained in the two waveforms over the time interval 'T' can be expressed as:

$$\text{Power}_{\text{avg}} = \frac{1}{T} \int_0^T e(t) \cdot i(t) \cdot dt \quad (\text{EQUATION 3})$$

2.1.2: Periodic Waveforms

With respect to periodic waveforms, 'T' in Equation 3 is selected as one period of 'e' and 'i', or a multiple of that period, i.e. $T=n/f$, where 'n' is a positive integer, and 'f' is the frequency of the waveform of period 'T'. For a periodic waveform, Equation 3 becomes:

$$\text{Power}_{\text{avg}} = \frac{1}{T_{\text{per}}} \int_0^{T_{\text{per}}} e(t) \cdot i(t) \cdot dt \quad (\text{EQUATION 4})$$

The total power contained in a periodic voltage or current waveform may be equated to the power delivered to a resistive load in a direct current circuit through the concept of 'effective value'. The effective value of a periodic waveform $x(t)$ can be evaluated by:

$$X_{\text{eff}} = \sqrt{\frac{1}{T_{\text{per}}} \int_0^{T_{\text{per}}} [x(t)]^2 \cdot dt} \quad (\text{EQUATION 5})$$

where ' T_{per} ' is the period of the waveform $x(t)$.

The value for X_{eff} is usually termed the root mean

square (RMS) value of the waveform $x(t)$. Here $x(t)$ may represent voltage or current, giving V_{RMS} or I_{RMS} respectively. V_{RMS} and I_{RMS} are artificial quantities that allow power produced by alternating current to be compared to power produced by direct current.

By convention, the term 'apparent power' is defined as the square root of the product of V_{RMS} and I_{RMS} , and usually designated by the letter 'S'. Apparent power in a sinusoidal or nonsinusoidal periodic waveform is then:

$$\text{Apparent power (S)} = \sqrt{\frac{1}{(T_{\text{per}})^2} \int_0^{T_{\text{per}}} [v(t)]^2 \cdot dt \int_0^{T_{\text{per}}} [i(t)]^2 \cdot dt}$$

(EQUATION 6)

2.1.2(a): Periodic Sinusoidal Waveforms

Using Equation 4, the average power in a sinusoidal voltage waveform $V_{\text{peak}} \cdot \sin(\omega t)$ and associated current waveform $I_{\text{peak}} \cdot \sin(\omega t - \phi)$ is:

$$\begin{aligned} \text{Power}_{\text{avg}} &= \frac{1}{T_{\text{per}}} \int_0^{T_{\text{per}}} V_{\text{peak}} \cdot \sin(\omega t) \cdot I_{\text{peak}} \cdot \sin(\omega t - \phi) \cdot dt \\ &= \frac{1}{T_{\text{per}}} \int_0^{T_{\text{per}}} \left[\frac{V_{\text{peak}} \cdot I_{\text{peak}} \cdot \cos(\phi) \cdot (1 - \cos(2\omega t))}{2} - \right. \\ &\quad \left. \frac{V_{\text{peak}} \cdot I_{\text{peak}} \cdot \sin(\phi) \cdot \sin(2\omega t)}{2} \right] \cdot dt \end{aligned}$$

(EQUATION 7)

The two integrands of Equation 7 are illustrated in Figure 2.1. The first integrand of Equation 7 is equal to

FIGURE 2.1: ACTIVE AND REACTIVE POWER COMPONENTS OF A SINUSOIDAL WAVEFORM

Graph of the first
term in Equation 7

Graph of the second
term in Equation 7

the instantaneous 'real power', designated $P.(1-\cos(2\omega t))$, where 'P' is equal to $(V_{\text{peak}} \cdot I_{\text{peak}}) \cdot (\cos(\phi))/2$, often referred to as 'active power'. The second integrand of Equation 7 is equal to the instantaneous 'reactive power', designated $Q \cdot \sin(2\omega t)$, where

$$Q = \frac{V_{\text{peak}} \cdot I_{\text{peak}}}{2} \cdot \sin(\phi) \quad (\text{EQUATION 8})$$

The real power is unidirectional, alternating symmetrically around an average value $V_{\text{peak}} \cdot I_{\text{peak}} \cdot \cos(\phi)/2$. That value is equal to $V_{\text{RMS}} \cdot I_{\text{RMS}} \cdot \cos(\phi)$, since V_{RMS} and I_{RMS} for sinusoidal waveforms are $V_{\text{peak}}/\sqrt{2}$ and $I_{\text{peak}}/\sqrt{2}$, respectively. Reactive power flow alternates in direction symmetrically around zero. Though having an average value of zero, reactive power does have a mean square average of $(V_{\text{peak}} \cdot I_{\text{peak}} \cdot \sin(\phi))/2$, which equates to $V_{\text{RMS}} \cdot I_{\text{RMS}} \cdot \sin(\phi)$.

Since $\sin^2(\phi) + \cos^2(\phi) = 1$, for a sinusoidal waveform it follows that:

$$S^2 = P^2 + Q^2 \quad (\text{EQUATION 9})$$

Another relationship between the active power (P) and the apparent power (S) is the power factor. It is equal to $\cos(\phi)$:

$$\text{Power factor} = \frac{P}{S} = \frac{\text{Active power}}{\text{Apparent power}} = \cos(\phi) \quad (\text{EQUATION 10})$$

Figure 2.2 illustrates sinusoidal voltage and current waveforms, and the resulting power waveforms.

2.1.2(b): Periodic Waveforms Generally

The active power for a periodic waveform, whether

FIGURE 2.2: VOLTAGE AND CURRENT SINUSOIDAL WAVEFORMS

(a) Voltage and Current In-Phase (Resistive Load)

(b) Current Leading Voltage (Capacitive Load)

(c) Current Lagging Voltage (Inductive Load)

(d) Current Leading Voltage (Resistive/Capacitive Load)

In case (a), the voltage is applied across a load that is resistive only; the voltage and current waveforms are in-phase with a power factor of 1, i.e. $\cos(0^\circ)=1$, and the active power is at a maximum; the reactive power is zero. In cases (b) and (c), the voltage is applied across a load that is reactive only. The amount of power entering the capacitive element in case (b) or the inductive element in case (c) equals the amount of power leaving the respective reactive element. Once power is no longer applied to the particular reactive element, a small amount of power stored within that element is given up. In cases (b) and (c), the current leads and lags the voltage by 90° , respectively, and in both cases the power factor is 0, ($\cos(-90^\circ)=\cos(90^\circ)=0$). The reactive power is at a maximum, and the active power is zero. In case (d), the current leads the voltage by 45° , the power factor is $\cos(-45^\circ)=1/\sqrt{2}=0.7071$, and both active and reactive power exist.

sinusoidal or not, can be found from expanding the waveform in a Fourier Series and calculating the power from an equation analogous to Equation 7. Omitting the direct current component, the active power is:

$$P = \sum_{n=1}^{\infty} \frac{(V_{\text{peak}})_n \cdot (I_{\text{peak}})_n \cdot \cos(\phi_n)}{2} \quad (\text{EQUATION 11})$$

where 'n' represents the number of harmonics in the waveform. For a bandlimited signal, 'n' goes up to some finite value 'N'.

A possible definition for the apparent power for a general periodic waveform requires substituting:

$$v(t) = \sum_{n=1}^{\infty} (V_{\text{peak}})_n \cdot \sin(n\omega t) \quad (\text{EQUATION 12})$$

$$i(t) = \sum_{n=1}^{\infty} (I_{\text{peak}})_n \cdot \sin(n\omega t - \phi_n) \quad (\text{EQUATION 13})$$

into Equation 6, where as in Equation 11, 'n' represents the number of harmonics in the waveform, and for a bandlimited signal, 'n' goes up to some finite value 'N'.

2.2: Sampling of Bandlimited Periodic Waveforms

One practical approach for determining the power in periodic waveforms involves taking samples of the voltage and current waveforms at time intervals and then extrapolating the power in those waveforms. One early often-cited reference describing such sampling is [TUR, 1974].

For a periodic bandlimited waveform, the value of $(V_{\text{peak}})_n$ and $(I_{\text{peak}})_n$ for each harmonic 'n' in Equation 11 can be found by taking 2N equally-spaced samples over the period of the waveform, and applying a discrete Fourier transform

to those samples. The active power in each harmonic can be found from those values, and Equation 11 can be used to find total active power.

2.2.1: Synchronous Sampling of Voltage and Current

2.2.1.1: Active Power and Apparent Power

The instantaneous value of a bandlimited periodic waveform can be exactly determined from samples if the sampling frequency is: (i) greater than twice the highest harmonic, and (ii) a harmonic of the period. If (i, and (ii) both apply, the original waveform can be determined from the harmonics obtained from the discrete Fourier transform, and constructed from a finite set of samples. Although not requiring that (ii) apply, the sampling theorem requires an infinite number of samples.

The active power present in the voltage and current waveforms can be found by sampling those waveforms and using the equation:

$$\text{Active power (P)} = \frac{\sum_{i=1}^n V_i \cdot I_i}{n} \quad (\text{EQUATION 14})$$

where 'n' stands for the total number of voltage and current samples summed in the running total, and 'i' identifies the sets of instantaneous voltage and current samples (1 to n). Conditions (i) and (ii) above must apply.

One can extend the concepts of apparent power and power factor to non-sinusoidal signals. The apparent power in the voltage and current waveforms can be determined from:

$$\text{Apparent power (S)} = \frac{\sqrt{\left(\sum_{i=1}^n V_i \cdot V_i\right) \cdot \left(\sum_{i=1}^n I_i \cdot I_i\right)}}{n} \quad (\text{EQUATION 15})$$

2.2.1.2: Reactive Power and Power Factor

There is no longer a definition that is universally agreed upon for reactive power. One definition, introduced by Fryze [FRY, 1932] defined reactive power as the geometric difference between apparent power and active power following Equation 9, i.e.

$$\text{Fryze reactive power (Q}_f\text{)} = \sqrt{S^2 - P^2} \quad (\text{EQUATION } \quad ,$$

It is possible to calculate the reactive power from synchronous sampling if this definition is used.

Another definition for reactive power [BUD, 1927] extends the definition of Equation 8 and defines:

$$Q = \sum_{n=1}^{\infty} \frac{(V_{\text{peak}})_n \cdot (I_{\text{peak}})_n \cdot \sin(\phi_n)}{2} \quad (\text{EQUATION 17})$$

Equation 17 will give a value for reactive power that is less than Q_f (Equation 16), and the geometric difference is called the distortion power D , defined as:

$$\text{Distortion power (D)} = \sqrt{S^2 - P^2 - Q^2} \quad (\text{EQUATION 18})$$

It is more difficult to calculate Q and D than Q_f from synchronous sampling, since $\sin(\phi_n)$ must be calculated for 'n' frequencies.

In the same way, the definition of power factor can be extended to the nonsinusoidal case by extrapolating sinusoidal formulas.

In this thesis, the power factor for nonsinusoidal periodic waves will be defined as:

$$\text{Power factor} = \frac{P}{S} = \frac{\sum_{i=1}^{\infty} V_i \cdot I_i}{\sqrt{\sum_{i=1}^{\infty} (V_i)^2 \cdot \sum_{i=1}^{\infty} (I_i)^2}} \quad (\text{EQUATION 19})$$

The wattmeter/watthour meter of this thesis calculates the active power, apparent power and power factor, but does not calculate a value for reactive power. The power factor of 3-phase systems is discussed in Section 4.4 of Chapter 4.

2.2.1.3: Errors in Synchronous Sampling

Although synchronous sampling under ideal conditions should provide exact values for active power, apparent power and the power factor, using Equations 13, 14 and 15, respectively, there will be some errors in electronic digital wattmeters for the following reasons:

- (1) harmonic content with frequencies too high for the sampling rate (for practical purposes the sampling rate should be perhaps 3 times the highest frequency in the waveform);
- (2) phase jitter in the phase lock loop circuit, resulting in the sampling interval not being an exact multiple of the periodic waveform;
- (3) errors in the analog circuitry, including the current shunt and voltage divider;

- (4) errors in the analog-to-digital conversion, mainly in the form of quantization error;
- (5) errors due to finite word length in the processor.

Asynchronous sampling, discussed below, adds yet a further source of error, referred to in the literature as 'truncation error'.

2.2.2: Asynchronous Sampling of Voltage and Current

Synchronous sampling of a waveform involves 'locking in' on the period of the waveform, for instance, by use of phase-lock loop circuitry. As set out in the previous section, it is theoretically possible with synchronous sampling to exactly reconstruct a bandlimited periodic waveform from samples if the sampling frequency is at least twice the frequency of the highest harmonic in the waveform. As also set out, phase jitter on the phase-lock loop circuit and other factors limit the synchronous sampling accuracy.

Now consider the situation where a waveform is no longer synchronously sampled, but is asynchronously sampled. Asynchronous sampling refers to sampling a waveform at time intervals that are not divisions of the period of the sampled waveform but instead are fixed intervals set by an external clock. This is illustrated in Figure 2.3, in which the waveform is not sampled at the zero-crossing points.

2.2.2.1: Advantages and Drawbacks

Since samples are taken at time intervals independent of the period of the waveform, it is possible to determine the frequency of the waveform by comparing the relative separation of consecutive zero-crossing points in terms of

FIGURE 2.3: ASYNCHRONOUS SAMPLING OF A SINUSOIDAL
VOLTAGE WAVEFORM

the number of sample points in that waveform period. This ability to determine waveform frequency is an advantage for asynchronous sampling over synchronous sampling.

Another advantage of asynchronous sampling is the ability to sample a repetitive waveform over several cycles at a slow rate and have an effective sampling rate equal to the true sampling rate times the number of cycles sampled. This can greatly reduce aliasing problems. This is more fully described in Section 1.2.2 of Chapter 1.

One drawback with asynchronous sampling is that a greater number of samples must be taken to give accuracy comparable to synchronous sampling. It has been shown [STEN, 1984] that the maximum error in power calculations resulting from asynchronous sampling of voltage and current waveforms is under certain conditions equal to $1/n$, where 'n' is the number of asynchronous samples that are gathered within a summation interval comprising a chosen number of the waveforms.

2.2.2.2: Calculation of Asynchronous Error

Figure 2.4 is reproduced from [STEN, 1984]. In the figure, 'V' and 'I' are peak values for the voltage and current waveforms, respectively, and 'β' represents the relative phase angle between those waveforms. The starting voltage phase angle is represented by 'α', and the interval between samples is represented by 'Δ'. The 'k'th. voltage and current samples are then given by:

$$\begin{aligned} V_k &= V \sin(k\Delta + \alpha) \\ I_k &= I \sin(k\Delta + \alpha + \beta) \end{aligned}$$

If the power is measured using n samples (k = 0 to n-1), the power can be expressed as:

FIGURE 2.4: WAVEFORM SCHEMATIC FOR CALCULATION OF ASYNCHRONOUS ERROR [STEN, 1984]

X - Sample Values

⊗ - Values used in Summation

$$W = \frac{V \cdot I}{2} \cdot \left[\cos(\beta) - \frac{1}{n} \sum_{k=0}^{n-1} \cos(2k\gamma + 2\alpha + \beta) \right] \quad (\text{EQUATION 20})$$

The true power is the first term in this expression and the summation term is the truncation error 'E'. Stenbakken shows that the summation for the truncation error E (the summation part of Equation 20) can be done analytically to yield:

$$E = \frac{V \cdot I \cdot \sin \delta}{2n \sin \gamma} \cdot \cos(2\alpha + \beta - \delta - \gamma) \quad (\text{EQUATION 21})$$

where ' δ ' is a 'truncation angle' as shown in Figure 2.4.

With respect to Equation 21, if the summation interval $n\gamma$ is approximately synchronized with the input signal such that the truncation angle δ is the same size or smaller than one sample interval γ , and if $\gamma < \pi/2$, the maximum truncation error occurs when the cosine term in Equation 21 is equal to +1 or -1 and when $\sin \delta = \sin \gamma$. Under those conditions, the maximum error is:

$$E_{\max} = \frac{V \cdot I}{2n} \quad (\text{EQUATION 22})$$

One can see intuitively from Figure 2.3 why this is the expected error from asynchronous sampling. For example, if 10 samples are taken over the duration of the waveform of Figure 2.3, the first sample might by chance be taken at a point that is located 0.9 of a sample spacing after the first positive-going crossing point and the last sample might be taken at a point located 0.9 of a sample spacing before the second positive-going crossing point. In such case one would have 9 complete sample spacings plus almost another full sample spacing on each side of the 1st. and

10th. samples, i.e. the 10 samples would be representative of 11 sample spacings rather than 10 sample spacings. The error in this situation, which approximates the worst case scenario for asynchronous sampling, can be seen to be approximately 1 part in 10. That error is reduced either if the width of the sample spacing is increased such that 10 samples more closely represent 10 sample spacings, or if the width of the sample spacings is decreased such that 11 samples are taken over 11 sample spacings. Intuitively, it can be seen that the greater the number of samples used the smaller the error; for instance, if 20 samples are taken over the period of the waveform the maximum error approaches $1/20$. For accurate asynchronous power measurement it is desirable to collect as many samples as is possible before performing calculations, and to use a series of periods of a waveform rather than a single period. Ideally such asynchronous sampling would be performed continuously, with sampling, calculation and display functions being handled by separate but interfacing processors each dedicated and optimized for one of the aforementioned functions.

2.2.2.3: Wattmeter Considerations

The foregoing factors are suggestive of a wattmeter having the following features:

- (1) sample spacing should be as short as possible;
- (2) samples should be gathered over not just one waveform period, but over a number of periods; and,
- (3) sample gathering should be separated from calculation and display functions so as to allow one processor to dedicate its time to gathering samples, i.e. the use of two or even three processing units.

Each of these three items will next be further considered.

2.2.2.3(a): Short Sample Spacing

Short sample spacing would suggest the desirability of collecting sample values just as quickly as the sampling mechanism can handle the input. This approach is only compatible with continuous sampling if one has processors available that are able to handle fast multiplication of sample values, continuous summation of the products of the multiplication, calculation of parameters using the summed products, and driving of output displays to show the parameter values.

2.2.2.3(b): Use of a Number of Periods

To reduce the truncation error, it is desirable to use perhaps 10 or 100 60-hertz periods and gather samples between a first positive-going or negative-going zero crossing and a matching zero crossing 10 or 100 periods later. The truncation error is then $1/((\text{number of periods}) \cdot (\text{number of samples/period}))$. For instance, if sampling is such that approximately 100 samples are gathered over each period and calculations are performed after continuous sampling of 100 periods, the 'truncation error' would be $1/((100) \cdot (100))$, i.e. 0.01%.

2.2.2.3(c): More Than One Processor

Regarding separation of the sample gathering from the calculation and display functions, digital signal processor chips now often have a fast multiplication unit capable of efficiently multiplying and summing the individual power product values but not of efficiently determining

a square root or of driving power display outputs. This is suggestive of two processors working together to share the various functions, namely, a digital signal processor device as the front-end of the wattmeter and a microcontroller or microprocessor as the back-end manager of the meter.

2.3: A Wattmeter Using Asynchronous Sampling

2.3.1: General Considerations

Based on the foregoing factors, a wattmeter was designed that asynchronously sampled voltage and current waveforms continuously, using 117 voltage periods to comprise each sampling interval and with 256 samples being taken over each voltage and current period (at 60 hertz). Short comments follow on why those values were chosen --- Chapter 4 (Meter Design) explains the choices more fully. For purposes of comparison, the meter was also capable of synchronously sampling the voltage and current waveforms.

It was desirable to sample the waveforms 2^k times each period, for reasons that included ease of division. The sample spacing was selected such that 2^8 (256) samples fitted closely into a 60-hertz period. The next fastest sampling rate would have required 2^9 (512) samples be fitted within each period of a 60-hertz waveform; however, that rate would not have allowed sufficient time for sample collection and processing by the asynchronous routine in each of the three phases.

The reason for choosing 117 cycles developed from several considerations. It was desirable to collect as many samples as possible before analyzing their content; as discussed above, accuracy with asynchronous sampling is dependent on gathering samples in batches as large as possible. The size of the common memory between the processors and the

need for the output display to track input changes over reasonably short intervals led to a choice of sampling interval of approximately two seconds. Two seconds equates with 120 periods of a 60-hertz signal, and therefore as a starting point 120 periods was considered. However, no more accuracy is obtainable from 120 periods than from 2 periods. Working downward, the accuracy of 119 periods could be obtained from 7 periods, and the accuracy of 118 periods could be obtained from 59 periods. The first prime number encountered is 117, and therefore each sampling interval was chosen to be the length of 117 periods. Each sampling interval of a 60-hertz waveform would then include $(117) \cdot 2^8$ samples.

Based on the foregoing, the approximate size of each $V_i \cdot I_i$, $(V_i)^2$ and $(I_i)^2$ summed value transferred by the front-end processor to the common memory approximately every two seconds was:

$$(117) \cdot (2^8) \cdot (2^{16})^2$$

which equated to the use of three 16-bit storage locations in the front-end processor and common memory for each of the summed values for each of the three phases.

2.3.2: Frequency Measurement

With an asynchronous wattmeter, frequency is determined by counting the number of samples gathered over a specified number of waveform periods and comparing that value with the number of samples that should exist at a given frequency. For instance, over 117 periods one should encounter $(117) \cdot (256)$ samples at 60 hertz with this wattmeter --- more samples at lower frequencies, and fewer samples at higher frequencies. The frequency can be found by using:

$$\text{Frequency} = \frac{(117).(256)}{(\text{Number of Samples})} \cdot (60 \text{ hertz})$$

(EQUATION 23)

2.3.3: Power Consumption (Energy) Measurement

Power consumption is the product of the active power and time. The units of measurement are kilowatthours. For each phase, the power consumption (in kWh) was found by creating a running total which was increased during every sampling interval (approximately every 2 seconds) by the active power calculated for that sampling interval divided by 1800. The value of 1800 assumes that each sampling interval is 2 seconds long, which is not the case; in fact, the value depends on the frequency of the voltage and current waveforms. For instance, if the waveforms remain at 60 Hz or close to it (as most hydro power supplies do) the divisor used in the power consumption calculation more accurately should be 1846, i.e. $(3600).(60/117)$. To account for waveforms with constantly-fluctuating frequency, one could use an interrupt on the front-end processor to create a clock independent of the waveform frequency --- and record active power against that clock. Such correction was not implemented in the prototype meter.

These same comments apply to the discussion of 15-min. kVA demand in the next section.

2.3.4: 15-Minute kVA Demand Measurement

Figure 2.5 illustrates the calculation of 15-min. kVA demand. Unlike power consumption, which involves a continuously increasing value, 15-min. kVA demand is a value representing the average maximum power consumed over a 15-

FIGURE 2.5: CALCULATION OF 15-MIN. KVA DEMAND

minute interval. The value for 15-min. kVA demand for a phase is initially set to zero. Then 450 consecutive active power values are calculated and summed to determine a base 15-min. kVA demand value; this region of summed values is illustrated with lines sloping upwardly to the right in Figure 2.5. When the next (451st.) active power value is calculated, that value is added to the base value and the 1st. value is deleted. Thus, a new 15-min. kVA demand value is calculated that comprises the aggregate of the 2nd. to 451st. active power values. This new aggregate value, represented by the lines that slope upwardly to the left in Figure 2.5, is then compared to the base value comprising the aggregate of the 1st. to 450th. active power values. The higher of the two aggregate values becomes the new base 15-min. kVA demand value. During the next sampling period a further aggregate active power value (the 452nd.) is calculated and added to the aggregate of the 2nd. to 451st. values, then the 2nd. value is deleted, and the new running total is compared to the base value; the larger of the two aggregate values becomes the new base value. In this way, at any time the wattmeter is able to display the largest aggregate of 450 consecutive active power values calculated to that time for each phase. In Figure 2.5, the largest value is represented by the region having horizontal lines.

The 15-min. kVA demand values, as well as the power consumption values, are automatically stored for subsequent retrieval during periods when the wattmeter is turned off.

The peak power demand measurement scheme described here has been implemented in many electronic wattmeters. More commonly, older meters operated by mechanically integrating the rotation of the wheel of a watthour meter. The integrator pushed a pointer which was not spring-loaded, so it remained at the maximum value to which it was pushed; at the end of each demand period the integrator was reset. Such wattmeters would give a reading different from the

reading of this wattmeter. However, a small change in the programming of this wattmeter would allow it to mimic the operation of the older integrating meters.

2.4: Summary

This chapter has discussed the theory behind the wattmeter of this thesis, and in particular the equations it uses with asynchronous sampling of voltage and current waveforms to calculate a series of parameters related to power in the waveforms. The next chapter is a literature survey of digital electronic synchronous and asynchronous sampling wattmeters. Chapter 4 discusses the design of the meter of this thesis, and Chapter 5 discusses its construction.

CHAPTER 3

LITERATURE SURVEY

3.1: Introduction

A brief review of the literature on digital electronic wattmeters is presented next. Because of a universal interest in power measurement and a growing availability of microprocessors, the literature on digital electronic wattmeters comes from many countries and is in many languages.

3.2: Synchronous Sampling Wattmeters

3.2.1: Using One Processor

In 1974 Raymond Turgel of the National Bureau of Standards in the United States presented a paper [TUR, 1974] which has become a basic reference on the design of digital wattmeters.

Based on computer simulation, Turgel determined how many samples are required for a synchronous sampling wattmeter to have 0.01% accuracy, given the presence of random noise with peak values of 100 parts/million. Other factors included in the simulation were timing uncertainty, the presence of harmonics, and resolution error. Among the conclusions of the simulation were:

- not more than 512 sample points in a waveform period are required;
 - a resolution corresponding to 15 bits for the measured voltage and current is adequate;
 - the sampling rate must be at least 40 kHz to resolve frequency components up to 10 kHz;
 - sampling uncertainty can vary up to 50 ns.
- Turgel built a wattmeter based on the foregoing

factors, and utilizing a phase-lock loop circuit to control a pair of sample-and-hold amplifiers. The phase-lock loop circuit was capable of creating pulses between 20 kHz and 40 kHz, using 9 range settings. That allowed, for instance, division of a 60-hertz input into 512 sampling points per cycle, but division of a 6-kHz input into only 4 sampling points per cycle. A pair of 14 bit (+ sign) A/D converters with two's-complement output were used; a minimum of 25 microseconds was required between conversions. Each power calculation was made on a minicomputer, and took approximately one second. As Turgel points out, the wattmeter was therefore not capable of 'real time' measurement.

Turgel's experimental results agreed to within 0.02% with the readings on a test electrodynamic wattmeter and a differential thermal voltage converter in the frequency range of direct current to 1 kHz. Between 1 kHz and 5 kHz, the error was somewhat larger.

Omran et. al [OMR, 1987] describe a microprocessor-controlled sampling digital power, RMS voltage and current, and power factor meter. The voltage and current inputs are each 8-bit, and are fed to separate A/D converters. Phase-lock loop circuitry is connected to the voltage input, and 512 voltage and current samples are taken over each waveform period. Using the summation of products for $\sum V_i \cdot I_i$, $\sum (V_i)^2$ and $\sum (I_i)^2$, V_{RMS} , I_{RMS} and power factor are determined. A lead/lag indicator is determined by counting the number of samples from a voltage crossing point to the respective maximum voltage and current levels positions, and comparing those positions. The accuracy of measurement is stated to be 0.05% over a frequency range of 30 to 70 hertz.

Hill and Alderson [HILL, 1981] describe a digital wattmeter based on an 8-bit microprocessor. The microprocessor determines the period of a sampled waveform by using

an internal counter and interrupts generated by a pair of negative-going crossing points. The negative-going crossing points do not have to be successive, and the authors state that more than one waveform cycle can be utilized. Voltage and current samples are taken at equal time intervals, each calculated by dividing the time between the selected pair of negative-going crossing points by the desired number of samples in that period. Each computation of average power uses a minimum of 30 samples. A single 11-bit (+ sign) A/D converter is used, with the voltage and current inputs being multiplexed. In the frequency range of direct current to 1 kHz, full scale accuracy of better than 0.5% was obtained. A similar design, but using a different 8-bit microprocessor and lacking an estimate on its accuracy, is presented in [SONI, 1983].

V. V. Athani [ATH, 1985] uses a similar system to Hill and Alderson, in that the time between successive zero crossing points is used as a base time to be divided by the number of samples to be taken over the waveform period. A 16-bit microprocessor and 8-bit A/D converter are utilized, and 16 samples are taken over each voltage and current waveform period for three phases. Using the voltage and current samples, V_{RMS} , I_{RMS} and average active power are calculated for each phase. Active power, power factor, reactive power (defined using $\sqrt{S^2 - P^2}$), and 30-min. kVA demand are also calculated. The reference provides no estimate of accuracy.

A digital metering system adapted to be fitted to an electrical distribution system is described by Charles Ho and Leonid Triger in [HO, 1987]. This digital system, which can be fitted to 3-phase systems operating at anywhere between 120 volts and 30 kilovolts, is intended to replace traditional analog meters. An 8-bit microcontroller is used, with voltage and current samples being gathered between a

successive pair of voltage zero crossing points. A wide range of parameters are measured by the system, including reactive power (defined in the same way as in the foregoing V. V. Athani reference), current demand and kVA demand. The system incorporates non-volatile RAM to cover power failure. By comparing the time between successive voltage zero crossing points with the output of a crystal oscillator, the system is able to measure frequency. No accuracy estimate is provided.

3.2.2: Using Two Processors

H. C. Wood et. al [WOOD, 1987] describe a real-time digital meter that utilizes two single-board microcomputers, one controlling the other. The controlled unit performs the calculation and display functions while the controlling unit gathers and sorts the data. A phase-locked loop circuit is utilized in a similar way as in the preceding Ho and Triger reference --- to both synchronize the sampling to the waveform period and to provide a basis of comparison with an oscillator for frequency determination. Two memory banks are employed, with one bank being filled with new data while calculations are being performed on the other. This continuous sampling approach can be contrasted with the discontinuous sampling used in references such as Turgel, in which sampling ceases during calculation periods (the wattmeter of this thesis also utilizes continuous sampling and processors that operate in tandem). Samples are accumulated over 32-cycle intervals, which equate to approximately 0.5 seconds; the display also changes each 0.5 seconds. The general accuracy of the meter was found to be 0.5%, with a frequency accuracy of better than 0.04% over the range 55 to 65 hertz.

3.3: Asynchronous Sampling Wattmeters

Stenbakken [STEN, 1984] provides a widely-cited error analysis for asynchronous sampling wattmeters (see Chapter 2). Other more recent references on asynchronous sampling error are [LU, 1988] and [SRIN, 1986].

The Stenbakken wideband sampling wattmeter, which is described in association with the error analysis, is shown in block diagram form as Figure 3.1. Voltage and current analog inputs are each fed into a track-and-hold (T/H) amplifier and a 12-bit A/D converter that are triggered by an external clock; the clock is also connected to a 16-bit sample counter. The A/D converter outputs are connected to a 35-bit multiplier/accumulator (only $\Sigma V_i \cdot I_i$ is stored). A cycle counter records the number of waveform periods. A 16-bit microcontroller controls the wattmeter.

When compared against a standard thermal wattmeter (having an accuracy of ± 50 parts/million), the Stenbakken wattmeter agreed to within $\pm 0.03\%$ over the frequency range from 40 hertz to 2 kHz for phase angles of 0° and $\pm 60^\circ$. The test signal inputs were 120-volt and 5-ampere sinusoidal waveforms, but the accuracy with significant harmonics up to 100 kHz was anticipated to be less than $\pm 0.1\%$.

N. Yamazaki and Y. Ikeda [YAM, 1982] describe an asynchronous sampling wattmeter utilizing an 8-bit microprocessor. A block diagram of the wattmeter is shown in Figure 3.2. Asynchronous voltage and current samples are gathered over a large number of waveform periods, which are defined by voltage zero-crossing points. The two authors indicate that although the 8-bit A/D converter has a theoretical resolution of only $\pm 0.78\%$, the technique of using a number of waveforms improves the overall wattmeter accuracy to $\pm 0.1\%$.

FIGURE 3.1: BLOCK DIAGRAM OF THE STENBAKKEN WATTMETER

FIGURE 3.2: BLOCK DIAGRAM OF THE YAMAZAKI/IKEDA WATTMETER

Hamid Riaz [RIAZ, 1985] constructed an asynchronous sampling wattmeter having an 8-bit microprocessor, a pair of 12-bit A/D converters and a dedicated multiplier/accumulator chip (27-bit output). The voltage input was connected to the microprocessor to allow zero-crossing detection. Sample rate was selected under program control and was a function of the number of harmonics in the waveforms. An innovative feature was microprocessor control of the gain of the voltage and current amplifiers. The meter had a measurement uncertainty of $\pm 0.1\%$ of full scale range under restricted test conditions.

Michael F. Matouka [MAT, 1982] describes a digital power/energy meter for systems with nonsinusoidal waveforms. Unlike the Stenbakken and Yamazaki/Ikeda wattmeters, the asynchronous sampling wattmeter of Matouka does not detect zero-crossings of the sampled waveforms. Instead, the wattmeter samples voltage and current at a rate of 1 million samples per second for a period of 0.5 seconds. Calculation of V_{RMS} , I_{RMS} , and energy then proceeds using a sample count of 0.5 million. Instead of a microprocessor, Matouka uses a large-scale integrated circuit for multiply/accumulate. The circuit, which operates approximately 3000 times faster than a microprocessor, can multiply two 10-bit numbers in 0.15 microseconds and accumulate 2^{16} products. Matouka analyzes the 'truncation error' with this type of asynchronous sampling, and concludes that such truncation error is inversely proportional to the length of the measurement interval. For the frequencies of interest to the author (approximately 10 kHz), the truncation error is below 0.5%. However, for lower frequencies such as a power frequency of 60 hertz, Matouka indicates that some means would need to be found to relate the sampling interval to the period of the sampled waveforms.

3.4: Other Power Measurement Devices

O. P. Malik, G. S. Hope and J. Chang [MAL, 1981] describe a microprocessor-based power measurement device that utilizes a Fourier series technique. A rate of 240 hertz is selected for sampling sinusoidal voltage and current waveforms. Two microprocessors are used in cascade. One controls data acquisition and the computation of active and reactive power, while the other handles analog and digital display of information. The data acquisition microprocessor controls a multiplexed 12-bit A/D converter, and the microprocessors share a hardware multiplier. Both active and reactive power were stored in blocks of 1024 sample points. The accuracy of the device is in the order of 1%.

A measurement device for nonsinusoidal systems using a Fourier series technique is presented in a paper by G. Acciani and M. Savino [ACC, 1984].

CHAPTER 4

METER DESIGN

The asynchronous sampling wattmeter/watthour meter of this thesis was designed to take advantage of the best features of the processing chips available at the time. This chapter explains why two processors were utilized instead of one, and how each processor was selected. The various trade-offs involved with the data exchange between the two processors are described, and flow charts of the software algorithms utilized with both processors are presented.

4.1: Two Processing Chips Rather Than One

The fast repetitive multiplication and summation operations required for calculating $V_i \cdot I_i$, $(V_i)^2$, and $(I_i)^2$ from the instantaneous voltage values V_i and instantaneous current values I_i are suited to a digital signal processor which has a fast multiplier. The multiplication in general purpose microprocessors is much slower, often performed by shift-and-add algorithms.

On the other hand, management and display of the power data calculated by the digital signal processor suggests the use of a microprocessor or microcontroller. Digital signal processors are not well-suited to management functions, such as running displays.

The foregoing factors suggest a front-end digital signal processor accepting a fast flow of instantaneous voltage and current values, performing a series of fast multiplications on those values, and summing the products of the multiplications. That digital signal processor or the back-end microprocessor can then perform the additional calculations required for power determination, namely, division and

calculation of square roots. The back-end device handles the display of the calculated values. Exact division of the duties between the front-end device and the back-end device are determined by balancing the following factors:

- (1) The time between samples, i.e. successive V_i and I_i values, had to be sufficient to allow for the necessary multiplications on the sampled data, the summing of the products, and the transfer of the summed products to a transfer RAM area.
- (2) The time between the transfers of the summed products between the front-end and back-end devices had to be sufficient to allow the back-end device to calculate parameters from the summed products and display those parameters.
- (3) The aggregate number of voltage and current samples involved in each transfer of summed products was equal to the number of times that the sampling time in (1) divided into the transfer time in (2). For best accuracy of the meter, that aggregate number of samples had to be as large as was possible within the capabilities of the processing devices used.

Multiple-processor power measurement systems are mentioned in the literature. For instance, [WOOD, 1987] describes a system that utilizes an Intel 8051 microprocessor for data acquisition and initial data manipulation (to calculate RMS voltage and RMS current) and utilizes a BASIC-52 microcontroller to subsequently compute power factor, energy and frequency. This system samples 3-phase voltage and current signals synchronously, and determines frequency by using a crystal oscillator reference. [HOPE, 1981] describes a system that utilizes two 6800 microprocessors,

one for data acquisition and one for output display.

4.2: Choice of the Processing Devices

Because the front-end device had to be capable of performing a series of very rapid multiplications of voltage and current ($V_i \cdot I_i$, $(V_i)^2$, and $(I_i)^2$) during each sampling time, it was preferable to utilize a device having a fast multiplier. Texas Instruments' family of TMS320 digital signal processing (DSP) devices have a 16-bit by 16-bit fast multiplier which operates over a single instruction cycle time. When this design was initiated, the TMS320C25 device had a 100-nanosecond instruction cycle time which was the fastest multiply on a widely-available processor. It also had the added benefit over the earlier TMS320C10 devices of having a more powerful set of multiply/accumulate instructions, allowing execution of certain operations in fewer instruction cycles. The TMS320C25 was therefore selected as the front-end device for the wattmeter. One drawback of the TMS320C25 relative to the TMS320C10 at the time of selection was the lack of an EPROM version of the former, with consequent need for external EPROM chips; however, it was decided to utilize the external EPROM chips for the program code with the intention of entering the code onto an EPROM version of the TMS320C25 when such device became commercially available. Some advantages were gained by using the external EPROM chips, including: a reduction in the complexity of programming of the digital signal processing device, and a reduced risk of damaging that device.

The Intel 8096 microcontroller chip was selected as the back-end device for handling data display and other management functions. Primary factors in the choice of that device were its 16-bit data bus for handling the data passed from the front-end processor, its data manipulation instruc-

tions, its prioritized interrupt sources, and its multiple output ports allowing output values to be displayed in various formats. Other microcontrollers were considered, such as the 8-bit Intel 8051 and the Motorola 8-bit devices, but it was decided that they were incapable of handling the data flow rates from the front-end device.

The various trade-offs in device selection should become clearer in Chapter 5 where the actual construction detail of the wattmeter is discussed. The line demarcating the duties assigned to the front-end device from those assigned to the back-end device reflected the ability of each device to best handle those duties. For instance, even though the front-end device was capable of multiplying and summing the sampled voltage and current values for each of 3 phases over the summation interval, it was not efficient at dividing those aggregated values by the number of samples that they represented, nor in determining the square root of the quotients; the back-end device handled those calculations as part of its duties.

As set out in Chapter 2, accumulated data was passed from the front-end processor to the back-end processor approximately every two seconds. The reason for using that interval was dictated in part by the need to display changes in parameter values at reasonable intervals, and in part by the characteristics of the selected processors and the fast transfer RAM used to pass data between them. To amplify on these considerations:

- (1) Two seconds was considered to be the longest reasonable time allowable between changes to parameter values in the display. At least one second was needed to update those values.
- (2) Two seconds allowed the gathering of samples over the 117 cycles mentioned in Chapter 2. Given the speed of the front-end processor and

the software executed between samples, 2^8 samples could comfortably be gathered over each cycle. The resulting approximately $(117) \cdot 2^8$ samples for each of three phases over 2 seconds utilized approximately 45 bits of three 16-bit internal registers in the front-end processor for each phase.

- (3) The short write routine of the front-end processor and the small size (64 16-bit words only) of available RAM chips fast enough (at the time of building the wattmeter) to act as transfer RAM between the two processors were two more factors that pointed toward the use of three 16-bit values for each of $\Sigma V.I$, ΣV^2 and ΣI^2 in each phase.

4.3: The Front-End Processor

4.3.1: The Software

Figure 4.1 presents a general schematic overview of the initialization routine and the three phase routines utilized by the front-end processor for both its asynchronous and synchronous modes; the synchronous mode was added to allow comparisons with the asynchronous mode. Figure 4.2 presents a more detailed schematic view of the asynchronous routine utilized to gather data values in one of the three phases, and the calculations performed by the front-end processor on those values. The routines are obviously highly dependent on the choice of the TMS320C25 as the front-end processor; use of a different front-end processor would have required changes to the routines.

FIGURE 4.1: INITIALIZATION AND PHASE ROUTINES
OF THE FRONT-END PROCESSOR

FIGURE 4.2: ASYNCHRONOUS PHASE ROUTINE

With respect to Figure 4.1, the asynchronous initialization routine first includes a 1-second delay to allow the back-end processor to fully initialize itself. A series of counter values for use in the asynchronous routines are then loaded with initial values. The initialization routine then tests to see how many of the 3 phases have an alternating voltage waveform. Each phase that has an alternating voltage waveform is then tested for a '+' to '-' transition by measurement of three positive voltage values in a row, followed by three negative values in a row. Unless six voltage values are encountered in that order, the wattmeter does not move beyond the initialization routine. The wattmeter keeps track of how many alternating voltage waveforms it encounters, and that number (between 0 and 3) is passed to the back-end processor.

Following the initialization routine, if the asynchronous mode is selected, the program moves to three identical asynchronous routines, one for each of the three phases being measured by the wattmeter. If the synchronous mode is selected, the program shifts to three corresponding synchronous routines after passing through a synchronous initialization routine. During each pass through the three asynchronous routines or the three synchronous routines an external input pin on the front-end processor is examined to see which measurement mode is to be performed. After being shifted to the synchronous measurement mode, therefore, the wattmeter may as easily be shifted back to the asynchronous mode.

Each of the 3 asynchronous routines and each of the 3 synchronous routines has a calculation segment and a write segment; the calculation segment operates during every pass, whereas the write segment is activated only at the end of a data gathering interval (approximately two seconds). During each write segment, summed values of $V_1 \cdot I_1$, $(V_1)^2$ and $(I_1)^2$ as well as other parameters, such as the total number of asyn-

chronous samples represented in the summed values and the value and position of peak voltage in the measured voltage waveform, are transferred from their internal RAM storage area in the front-end processor to high-speed external RAM. After a write operation has occurred in all three phases, the back-end processor is advised of the data transfer, and proceeds to retrieve the data from the external RAM. During the following interval the back-end processor analyzes the retrieved data and displays the results; during that same interval the front-end processor is gathering a further set of data.

As reflected in Figure 4.2, each asynchronous routine begins by reading a voltage value and a current value. Each voltage and current values is squared, and those values are added to a respective running total stored in three 16-bit registers within the front-end processor. A $V_i \cdot I_i$ value is also calculated, and stored in three other registers. The routine next reads a data bit entered by the initialization routine to determine if an alternating voltage is involved. If the voltage is not alternating, a separate short subroutine is entered in which a first counter holding $(117) \cdot 2^8$ is decremented, and the write subroutine entered on that counter reaching zero. If the voltage is found to be alternating, the main routine checks to see if the most significant bit (MSB) of the 16-bit voltage sample is '0', and if so, checks to see if the MSB on the previous pass through the routine was '1'. If both criteria are met, the routine determines that a voltage zero-crossing has occurred and decrements a second counter (a period counter initially holding 117). It then loads a third counter with 240. This third counter is decremented during each pass through the asynchronous routine, and until the third counter reaches zero the software does not again test for a voltage zero-crossing. Since there are approximately 256 samples/cycle we choose to ignore any zero-crossings occurring before the

240th. sample. Such crossings would be spurious, and possibly caused by a very high 2nd. or 3rd. harmonic. Once the third counter has been decremented to zero and the hunt has begun for a voltage zero-crossing, the software stores the MSB of the voltage samples examined. If a voltage sample MSB of '0' is encountered the stored MSB of the voltage sample taken during the previous pass through the routine is examined. A determination of a voltage zero-crossing is made only when a voltage sample MSB of '0' is combined with a stored voltage sample MSB of '1' from the previous pass.

Once the second counter in phase has been decremented to zero, voltage and current samples for that phase have been gathered over 117 periods. At that point a subroutine is entered which writes the contents of the front-end processor's internal storage registers to the transfer RAM. The write subroutine also resets the sample counter to 0, sets the first counter to $(117).2^8$, sets the second counter to 117, and resets the internal $\Sigma V.I$, ΣV^2 and ΣI^2 storage areas in the front-end processor to zero. The write routine also decrements a phase counter shared by the three phases, and checks to see if the phase counter is zero. If it is zero, the XF pin of the front-end processor is toggled to alert the connected back-end processor that the transfer RAM is ready to be read (see Figure 4.2). The write routine that toggled the XF pin then loads 3 into the phase counter.

Besides summed $V_i.I_i$, $(V_i)^2$ and $(I_i)^2$ values for each phase being transferred to external RAM during each write pass, the following other parameters for each phase are also transferred:

- (1) the value for 'i', i.e. the number of samples that are included in the summed values;
- (2) the peak value of V and I and the location of those peaks, all of which are determined during the passes through the 117th. waveform.

4.3.2: Asynchronous/Synchronous Capability

If an external TMS320C25 input designated 'asynchronous/synchronous' is toggled, the front-end processor stops cycling through the three asynchronous routines and starts cycling through three synchronous routines, as shown in Figure 4.1. Toggling the external input from asynchronous to synchronous also switches the length of the sampling intervals from the 21.7-microsecond periods determined by a timer interrupt of the TMS320C25 to an input signal from an external phase-lock loop circuit. The phase-lock loop circuit is capable of dividing each waveform period into 2^k samples, where 'k' has a value between '1' and '9'.

The synchronous phase routine is simpler than the asynchronous phase routine in that no search is conducted for voltage zero-crossings. The write subroutine for the synchronous phase routine is triggered after $(117).2^8$ samples have been taken. Thus if a 'k' value of 8 is selected the display changes approximately every 2 seconds (as with the asynchronous routine), but if say a 'k' value of 6 is selected, i.e. 64 samples per waveform period, the display changes approximately every 8 seconds. The time to execute the synchronous routine was sufficiently short that 2^9 , i.e. 512, samples per waveform period was possible.

For comparison between the asynchronous sampling and synchronous sampling, a 'k' value of 8 was used, since this approximated the asynchronous sampling rate.

Frequency cannot be determined during synchronous sampling, and the display software was written to give a blank frequency display during such sampling.

4.3.3: Frequency Determination

In order to accurately measure frequency, it was

necessary that at the 60-hertz frequency of primary interest the number of asynchronous samples fitting into one period of an exact 60-hertz waveform should match as closely as possible with 2 to a power, in other words, 2^k where 'k' is an integer. One reason for that choice was the ease of division possible with 2 to a power. Another reason for choosing 2 to a power related to the comparison possible with synchronous sampling.

It was found that the asynchronous phase routine of the front-end processor could execute all of the steps set out in the algorithm of Figure 4.2 (including the write subroutine, when needed) in approximately 200 100-nanosecond instruction cycles, i.e. 20 microseconds. Therefore, sample spacing of slightly greater than 20 microseconds was desirable, and it was also desirable to match as closely as possible the time interval of 2^k samples with the period of a 60-hertz waveform. The value for 'k' had to be 8 or less in order for the asynchronous phase routine to have time to execute. A samples/period value of 2^8 was first considered. Based on the following considerations, that value turned out to be the most appropriate one to use.

If 2^8 , i.e. 256, samples are taken over the period of an exact 60-hertz waveform in each of three phases, the time taken between each sample is:

$$\frac{1 \text{ second}}{(3 \text{ phases}) \cdot (60 \text{ periods}) \cdot (256 \text{ samples/period})}$$

which is equal to 0.0000217013889 seconds, i.e. 217.014 100-nanosecond instruction cycles.

Although this choice automatically creates an error of about 0.006%, i.e. 14/217014 in the measurement of waveform frequency, other choices investigated resulted in other difficulties. For instance, 512 samples/period at 60 hertz was ruled out because: (1) 108.5 instruction cycles for each

sampling routine would require a divisible instruction cycle, and (2) 10.85 microseconds was not a sufficient time to execute the program developed for the asynchronous phase routine. On the other hand, 128 samples/ period resulted in a lower sampling rate with no improvement in frequency measurement accuracy.

The wattmeter was optimized for measuring power at the common 50 and 60 hertz supply frequencies by the choice of values for the period counters and interrupt timing in the front-end processor. Frequencies higher than approximately 63.7 hertz could not be measured because, after location of a voltage zero-crossing, the asynchronous software did not test for a further zero-crossing for 240 sample periods. As the frequency increased, two voltage zero-crossings would occur in less than the 240 sample periods. The highest measurable frequency (assuming samples taken just subsequent to one voltage zero-crossing and just prior to the next zero-crossing) was:

$$F_{\max} = \frac{(256)}{(240+1)} \cdot (60 \text{ hertz}) = 63.7 \text{ hertz}$$

The limitation on the lowest measurable frequency was the capacity of the 16-bit sample counter in the transfer RAM, which at 60 hertz held a count of $(117) \cdot (256) = 29,952$. The lowest measurable frequency was found to be approximately 34 hertz.

4.4: The Back-End Processor

Once the summed $V_i \cdot I_i$, $(V_i)^2$ and $(I_i)^2$ values and the other parameters for the three phases have been transferred to the external RAM by their respective write routines, the

third write routine toggles an external pin of the TMS320C25 to signal the back-end processor to read the external RAM.

The back-end processor transfers the values for the three phases to its internal memory, and starts processing that data. Eight parameters are extracted from the data for each phase, and an aggregate or an average of the values in the three phases is also calculated. Each of the 32 values is written to a respective address in a display RAM. A pair of rotary switches determine which one of the series of 32 values in the display RAM appears on a 12-digit 7-segment display. The first rotary switch chooses between each of three phases and an aggregate or average value for the three phases, and the second rotary switch allows a choice between the 8 parameters. The contents of the particular display RAM address defined by the pair of rotary switches are continuously displayed. The rotary switch choices are:

<u>First Rotary Switch</u>	<u>Second Rotary Switch</u>
Phase 1	V_{RMS}
Phase 2	I_{RMS}
Phase 3	Apparent Power
Aggregate or	Active Power
Average	Power Factor
	Frequency
	Power Consumption
	15-Min. kVA Demand

Figure 4.3 illustrates the initialization routine, the calibration routine, and one of the phase routines for the back-end processor.

The initialization routine sets up a display RAM with parameter abbreviations (KW., HZ., etc.), then enters a one-second delay routine while it waits for the analog circuitry on the input board to stabilize, and then resets the front-end processor. The calibration routine is then

FIGURE 4.3: INITIALIZATION, CALIBRATION AND PHASE
ROUTINES FOR THE BACK-END PROCESSOR

Initialization

- set up display RAM
- 1-second delay routine
- reset front-end processor

entered. Along with the phase 1, 2 and 3 routines and the aggregate/average routine, the calibration routine is executed each time the back-end processor retrieves data from the common memory.

The calibration routine initially activates two external interrupt inputs --- one an indicator that the power supply to the meter has been disconnected, and the other an indicator from the front-end processor that common memory is ready to be read. The back-end processor then transfers the data held in the common memory to its own RAM area. While still in the calibration routine, the back-end processor next checks to see if it should equate a calculated V_{RMS} or I_{RMS} value with a calibration input on a set of manually-adjustable switches. If the indicator is that such calibration should occur, the back-end processor calculates a new calibration factor for V_{RMS} or I_{RMS} by dividing the calibration input by the calculated value. All subsequent calculated values are then multiplied by the particular calibration factor during passage through the particular phase routine. As a simple example, if V_{RMS} initially calculated from input data equates to 80.0 but that value actually represents $V_{RMS} = 8.00$ volts, the calibration factor will be 0.100; if a subsequent value of 100.0 were calculated from input data, that value would become $V_{RMS} = 10.0$ volts when multiplied with the calibration factor. V_{RMS} and I_{RMS} for each of the three phases can be independently calibrated in this manner. When passing through the calibration routine, the back-end processor also checks to see if the power consumption or the 15-min. kVA demand memory storage locations for any of the three phases should be set to zero. Unless it receives an indication that V_{RMS} or I_{RMS} has to be calibrated or a storage location zeroed, the back-end processor takes no action when passing through the calibration routine.

The back-end processor then sequentially enters the three phase routines. V_{RMS} and I_{RMS} are calculated from the

raw data retrieved from the common memory, and the calibration factor is applied to each. Apparent power is then calculated as the product of the calibrated V_{RMS} and I_{RMS} values.

Once calculated for each phase, V_{RMS} , I_{RMS} and the apparent power value for each of the three phases as well as their aggregate value are written to 12 display RAM addresses. Apparent power is calculated for each phase by multiplying together the V_{RMS} and I_{RMS} values for the phase, and dividing by 1000. A power factor value is calculated using $(\sum V_i \cdot I_i) / ((\sum V_i \cdot V_i) \cdot (\sum I_i \cdot I_i))$ for each of the three phases and an averaged power factor value (see * below) is calculated, and those 4 values are inserted into respective display RAM addresses. The relative peak voltage and peak current positions, as measured by the front-end processor on the last waveform of each phase, is used to determine if the power factor value for the respective phase should be preceded by a '+' sign (capacitive loading) or a '-' sign (inductive loading). The active power in each phase is calculated by multiplying the power factor for the phase by the apparent power for the phase; those values and an aggregate active power value are inserted into a further 4 respective display RAM addresses.

The back-end processor (8096) calculates 3 other parameters from the data that is transferred from the front-end processor. The other parameters are frequency, power consumption and 15-min. kVA demand. Chapter 2 indicates the equations used for calculating these parameters for each of the three phases. An average frequency value and aggregate power consumption and 15-min. kVA demand values were also

* For an unbalanced polyphase system, The American National Standard Code for Electricity Metering indicates that it is more normal to calculate an 'Interval Power Factor' defined as $(P \cdot t) / \sqrt{(P \cdot t)^2 + (Q \cdot t)^2}$. In this equation, 'P' is the total active power of the system, 'Q' is the total reactive power of the system, and 't' is time. [ANSC, 1982]

determined. The 12 values for the 3 parameters were then loaded into respective display RAM addresses.

After running through the calibration routine and the three phase routines, the back-end processor enters an endless loop. In that loop it continuously examines a value transferred on the data bus as an output from the address rotary switch inputs and representing an address pointer to the display RAM area. The back-end processor enters the contents of the particular display RAM address into the 12-digit 7-segment display.

The existing calculation and display routines for the 8096 back-end processor occupy it for approximately half of each 2-second data gathering interval. That leaves time for that processor to carry out other functions in the time remaining. For instance, it could download the display RAM information to a distant computer by modem or to a connected computer through a serial connection. Although the hardware for downloading data through those alternate outputs was installed on the output board, the associated software for the 8096 processor was not written.

Other designs for asynchronous digital electronic wattmeters can be found in [RIAZ, 1985] and [YAM, 1982].

4.5: Summary

The general design considerations of the wattmeter/watthour meter have been discussed in this chapter. The construction of the meter is described in the next chapter.

CHAPTER 5

METER CONSTRUCTION

5.1: Introduction

The wattmeter/watthour meter consists of an input board and an output board, and a main (mother) board into which both the input board and output board fit. Both the TMS320C25 front-end processor and the 8096 back-end processor are mounted on the main board, and power is supplied to the input and output boards through the main board. This chapter contains a description of the meter hardware.

5.2: The Wattmeter Hardware

The full circuitry of the wattmeter is illustrated in 6 schematic drawings, Figures A1 to A6, in Appendix A. The apparatus is also shown in 4 photographs in Appendix B.

5.2.1: The Input Board

Figure 5.1 is a general block diagram of the input board of the wattmeter; detailed schematic drawings of that board are shown in Figures A1 and A2 of Appendix A.

The wattmeter was adapted to receive an alternating current sample input of approximately 5 amperes and an alternating voltage sample input of approximately 120 volts.

The 5-ampere current input was fed through a shunt consisting of twenty parallel 2.0-ohm resistors (Vishay No. S102K) with high temperature stability (less than 1.0 ppm/degree C resistance fluctuation). Each of the 20 resistors had each of its leads soldered to a respective one of a pair

FIGURE 5.1: GENERAL BLOCK DIAGRAM OF THE INPUT BOARD

of 2.5-inch by 2.0-inch copper plates, each 1/16-inch thick. The effective resistance of the 20 parallel resistors was 0.1 ohms, and a RMS voltage of approximately 0.5 volts was produced between the copper plates for a 5-ampere current.

The 120-volt voltage input was divided between a 500-kilohm resistor and a 2-kilohm resistor. Both resistors were made by Vishay, with the same 1.0 ppm/°C temperature coefficient as in the current shunt. Whenever the word Vishay is used to modify resistor in the following text, that temperature stability is implied. A RMS voltage of approximately 0.5 volts was produced across the 2-kilohm resistor for a 120-volt input.

As illustrated in Figure 3.1, both the current and voltage inputs shared a common analog ground on the input board; that ground was also connected to the analog ground input of a pair of analog-to-digital (A/D) converters on the input board, as will be more fully described subsequently. Each of the voltage and current inputs was connected to an Analog Devices OP-27E ultra-low-noise, high-precision operational amplifier (op-amp). The OP-27E op-amp was chosen for its ultra-low input voltage noise and its low offset voltage drift over time. The voltage and current inputs were each amplified by a factor of five across a respective inverting op-amp circuit, as illustrated in Figure 5.1.

Each of the two OP-27E op-amp outputs was fed to the positive analog input of a respective Crystal Semiconductor CS5016-JC16 16-bit A/D converter. The common analog ground, which was connected to the positive input of each OP-27E op-amp through a respective parallel pair of 10K-ohm and 50K-ohm resistors, was connected to the negative analog input of the A/D converters. An overload indication and protection circuit was connected to each of the two OP-27E op-amp outputs to protect the A/D converters, as illustrated in Figure 5.1. Zener diodes limited the A_{IN} analog inputs into each A/D converter to a value between approximately

+4.7 volts and -4.7 volts. Each overload indication circuit consisted of three '084 op-amps, the first configured as a comparator for testing if the respective OP-27E op-amp output was above approximately 4.5 volts, the second configured as a half-wave rectifier having an output only when comparator input voltages were above 4.5 volts, and the third configured as an inverter connected to the gate of a transistor connected serially with an indicator light-emitting diode (LED).

In Figure 5.1 the A/D converter for the current measurement is shown on the left and the A/D converter for the voltage measurement on the right. Both converters have, as common inputs:

- a voltage reference of approximately 4.5 volts provided by an Analog Devices 584KH voltage reference chip;
- a CLKIN input provided by a 4.000000 MHz crystal;
- a RESET input (shown as the 'C' input from the main board in Figure A2 of Appendix A); and,
- analog +5 volt V_A^+ and -5 volt V_A^- power supplies created from +15 volt and -15 volt power lines on the input board by 7805 and 7905 voltage regulators, respectively.

Digital +5 volt V_D^+ and -5 volt V_D^- power supplies for both A/D converters were created from the analog power supplies to the converters using 10-ohm resistors, as recommended by the manufacturer. The analog +5 volt V_A^+ and -5 volt V_A^- power supplies for the A/D converters were created from the outputs of 7805 and 7905 voltage regulators (having respective +15 and -15 volt power line inputs) to help prevent noise reaching the A/D converters from the power lines of the power supply. The Analog Devices 584KH voltage reference chip is rated at 50 μ V peak-to-peak maximum noise output.

Conversion in each A/D converter is by successive approximation and is triggered by putting the HOLD input low. Conversion time is $16.25 \mu\text{s}$, with the analog input held constant during that time. The digital outputs are latched such that one set is held until the end of the next conversion. The asynchronous trigger signal is the same signal used to read the digital outputs of the two A/D converters (the TINT interrupt of the TMS processor at $21.7\text{-}\mu\text{s}$ intervals). The input board has an alternate synchronous trigger signal produced by a phase-lock loop circuit connected through three 084 op-amps to the output of the OP-27E op-amp that samples the voltage input. The first 084 op-amp converts the output of the OP-27E op-amp into a square wave, the second 084 op-amp rectifies the square wave, and the third 084 op-amp inverts the rectified wave. The resultant signal is then fed to a phase-lock loop circuit consisting of 4040, 4046, 4050 CMOS chips and a rotary switch with 9 positions. Rotation of the rotary switch creates a clock signal having a period $(1/2^k)$. (period of voltage waveform), where 'k' has a value between 1 and 9.

A double-pole, double-toggle (DPDT) switch allows selection as a trigger input to the HOLD pin on the A/D converters between the synchronous signal created by the phase-lock loop circuit and the asynchronous signal created on the main board (shown as the 'A' input from the main board in Figure A2). The selected trigger input from the DPDT switch was fed to a pair of first 74121 monostable vibrator chips, each of which created a fixed delay of 2.0 microseconds. The output of each first 74121 chip was in turn fed to the input of a respective second 74121 chip, each second 74121 chip being capable of creating a variable delay of between 0 and 2.0 microseconds. The output of each second 74121 chip was connected to the HOLD pin of a respective one of the A/D converters, allowing conversion start times for the two converters to be independently set to begin anywhere between 2

and 4 microseconds after the synchronous or asynchronous signal trigger times.

Besides directing either the synchronous or asynchronous signal to the HOLD pin on the converters through the delays of the 74121 chips, the DPDT switch determines the output of a flip-flop (shown as the 'D' output of the input board in Figure A2 of Appendix A). Figure A3 shows that the 'D' input to the main board connects with the BIO pin of the TMS320C25 processor. The software of the TMS processor uses the state of the DPDT switch, as reflected by the state of the BIO pin, to determine if the synchronous or asynchronous signal is being used to trigger the A/D converters on the input board, and chooses between the synchronous and asynchronous subroutines (both of which are described in Chapter 4).

The synchronous signal produced by the phase-lock loop circuit also leaves the input board as output 'B' (see Figure A2) after having a delay of approximately 0.3 microseconds inserted by a 74121 chip.

The 5-volt, 15-volt, -15-volt and GND power lines of the input board are supplied by pins on that board that enter the connector which supports the input board on the main board.

5.2.2: The Main Board

In Appendix A, Figures A3, A4 and A5 taken together are detailed schematic drawings of the circuitry on the main board of the computer. Figure 5.2 is a general block diagram of the main board.

The main board was equipped with three connectors for receiving three respective input boards, one for each phase of a three-phase power line. However, only one of the input boards was actually built. Each of the three connectors had DIP switches for connecting its 16 voltage input

pins and 16 current input pins to GND when no input board was in the connector; the MSB (most significant bit) voltage and current input pins were connectable to GND through respective inverters (each 1/6 74S04) because of the 2's-complement input format required by the TMS320C25 processor. One of the three connectors (the phase-1 connector) had an additional set of DIP switches allowing its 16 voltage input pins and 16 current input pins to be alternately set to either GND or 5 volts to simulate invariant digital voltage and current inputs for testing the main board without the input board.

Figure A3 illustrates the 16-bit voltage input, 16-bit current input, and the A, B, C and D lines that connect to the input board. It also illustrates the 16-bit phase-2 voltage input. The phase-2 current input and the phase-3 voltage and current inputs are not shown, but each of those inputs is similarly connected through a respective pair of 74ALS373 gate chips. The Y4, Y5 and Y6 select outputs of the 74ALS138 decoder chip (illustrated next to the TMS processor) are each connected to enable an output from a respective one of the three phases not shown.

Line A connects to the Y1 output of the 74ALS138 decoder chip. An active low on the Y1 output connects the 16-bit phase-1 voltage to the data bus of the main board, and after a delay of 2 to 4 microseconds, acts to trigger the HOLD line on the A/D converters on the input board. Line C connects to a pin on the 8096 processor; when the 8096 processor places that pin low, the TMS320C25 processor and the A/D converters on the input board are simultaneously reset. The main board also has a manual RESET pushbutton switch which can be used to reset the TMS processor. Lines D and B are connected to the BIO input and INTO interrupt input of the TMS processor, respectively.

The previously-mentioned 74ALS138 decoder chip has its address inputs connected to the A0, A1 and A2 address

lines of the TMS processor, and its select inputs connected to the R/W, IS and STRB outputs of the TMS320C25 processor.

The TMS processor takes values sequentially from each of the six 16-bit inputs using the 74ALS138 decoder chip --- a voltage and current value for each of the 3 phases. For each phase, the TMS processor accumulates the 16-bit voltage and current values into respective 48-bit storage areas within the processor, each area using 3 sequential 16-bit locations. For each phase, the 3 storage areas hold the $\Sigma V.I$, ΣV^2 and ΣI^2 values. After values have been summed over a period of approximately 2 seconds, as more fully described in Chapter 4, the TMS320C25 processor transfers the summed values from the internal storage areas to a pair of MCM2018-35 high-speed RAM chips (henceforth referred to as transfer RAM). It then resets its internal storage locations, and signals the 8096 processor that the transfer RAM has been loaded by changing the state of the XF pin (which is connected to an input on the 8096 processor).

The instructions for the TMS320C25 processor are stored in a pair of TMS27C292-3 EPROM chips. Of the various available versions of this EPROM chip at the time the meter was built, the '-3' (30-ns access time) version had to be used for compatibility with the fast cycle time of the TMS processor. The same EPROM chips were also used to hold the program code of the 8096 processor. A special programmer was built to program these EPROM chips, which were used in pairs --- one of each pair holding the lower 8 bits of program code and the other of each pair holding the upper 8 bits of program code. The select inputs of the EPROM chips are connected to the STRB output, PS output and R/W output, respectively, of the TMS320C25 processor.

The pair of transfer RAM chips are surrounded on each side by a set of three 74ALS373 three-state gate chips, one set controlling inputs to the RAM chips from the TMS processor and the other set controlling outputs from the RAM

chips to the 8096 processor. One of each set of 74ALS373 chips gates 6 address lines and 2 control lines, while the other 2 chips of each set gate the 16 data lines.

The WR enable of the TMS processor is connected to the output enable (pin 1) of the three gate chips separating that processor from the transfer RAM, and also forms one of the two control line gated by those chips. When the WR enable of the TMS processor goes low, the 16 lines of the data bus, the 6 address lines A0 to A5, and the WR and chip select lines are simultaneously connected between the TMS processor and the pair of transfer RAM chips. The data in the internal storage locations of the TMS processor is then passed to the transfer RAM. The capacity of the transfer RAM is only 64 16-bit words; of 16 words allocated for each phase, 15 are used as follows:

<u>Word Number</u>	<u>Contents</u>
1	Number of samples over 117 cycles;
2	Sample number of the peak V value in cycle 116;
3	Peak V value;
4	Sample number of the peak I value in cycle 116;
5	Peak I value;
6,7,8	Accumulated V.I total for the phase;
9,10,11	Accumulated V.V total for the phase;
12,13,14	Accumulated I.I total for the phase;
15	'1' if the accumulated V.I total is negative.

Once notified by means of the XF output of the TMS processor that the transfer RAM is loaded, the 8096 processor transfers the stored data from the transfer RAM to a pair of SRM2264C RAM chips (henceforth referred to as 8096 RAM) under its control before beginning to make calculations and display results based on those calculations. The calculation and display software of the 8096 processor had to run in less than the approximately 2-second intervals between reloading of the transfer RAM with fresh data by the TMS

processor; in fact, the 8096 software executed in about one second.

The 8096 processor utilizes an address/data multiplexing system developed by Intel. The multiplexing is controlled by the ALE (Address Latch Enable) output of the processor. A 8096 processor has a bus cycle in which the AD_0 - AD_{15} pins initially carry address information followed by data information; the ALE output of the processor goes from high to low during the address portion of the cycle to latch the address information onto an address bus. In this circuit, the ALE output is used to latch the outputs of a pair of 74ALS373 chips which have their inputs connected to the data bus; the outputs of those chips connect to the address bus. Because of a nuance in the Intel system of addressing, the A0 address line created by the latching of the D0 data line by the ALE signal is not used for addressing 16-bit data in external RAM and ROM by the 8096. For instance, the 3 pairs of TMS27C292-3 ROM chips (henceforth referred to as 8096 ROM) carrying the instructions for the 8096 processor each have address inputs A0 to A10 connected to respective address lines A1 to A11 of the 8096 address bus. Similarly, the address inputs A0 to A5 of the 8096 RAM chips are connected to respective address lines A1 to A6 of the 8096 address bus. In the result, the 8096 is only capable of addressing 32K of words.

Address lines A10 to A15 of the 8096 address bus are connected to a pair of 74ALS138 3-to-8 decoder chips, as shown in the upper center of Figure A5 of Appendix A. The decoder chip connected to address lines A13 ' A15 is continuously active, while the other decoder chip is activated by one of the active-low outputs of the first decoder chip. This arrangement results in the following memory map:

<u>Address</u>						<u>Element(s) Addressed</u>
<u>A15</u>	<u>A14</u>	<u>A13</u>	<u>A12</u>	<u>A11</u>	<u>A10</u>	
0	0	0	X	X	X	Reserved by 8096 (not addressed)
0	0	1	0	X	X	1st. Pair of TMS27C292-3 ROM
0	0	1	1	X	X	2nd. Pair of TMS27C292-3 ROM
0	1	0	0	X	X	3rd. Pair of TMS27C292-3 ROM
0	1	1	X	X	X	Pair of X2001P-20 NOVRAM
1	0	X	X	X	X	Pair of SRM2264C RAM
1	1	0	0	0	0	Pair of MCM2018-35 RAM
1	1	0	0	0	1	Integer Word Calibration Switches
1	1	0	0	1	0	Fraction Word Calibration Switches
1	1	1	0	0	X	Output Board - Display
1	1	1	0	1	X	Output Board - Rotary Switches
1	1	1	1	0	X	Output Board - Modem

With reference to Figure A5, the main board holds a pair of X2001P-20 NOVRAM (non-volatile RAM) chips (henceforth referred to as NOVRAM) capable of holding 64 words. NOVRAM is a cross between ROM and RAM in that it can accept information written to it, as does RAM, and will retain that information even when power is removed, as does ROM. In this wattmeter NOVRAM was used for retaining calibration values and accumulated power consumption values during the intervals when power was removed from the meter. The NOVRAM was used in association with the power sensing circuit that is shown in the upper right of Figure A5. That sensing circuit, which comprises a pair of 4N25 optocouplers and a 1455 timer chip, is connected to the EXTINT interrupt of the 8096 processor; it activates an interrupt subroutine which executes during the brief interval between power interruption and depletion of capacitance on the power supply below a critical value (an interval approximately one second long) to store calibration and power consumption values in the NOVRAM. The NE (nonvolatile enable) input on the NOVRAM is connected to the 8096 processor; when the processor places that input low, data stored as RAM on the NOVRAM is transferred to nonvolatile storage.

Integer and fraction calibration DIP switches are used to deliver values between 0.0 and 65535.99998 for calibrating voltage and current values in the meter. The meter calibration also involved DIP switches, shown connected to the Port 0 inputs P0.0 to P0.5 on the right side of the 8096 processor in Figure A5. Two of the Port 0 inputs were used to select among the 3 phases, and two more of those inputs were used to select between: voltage calibration, current calibration, zeroing the power consumption storage area, and zeroing the 15-min. kVA demand storage area. The final two Port 0 inputs were used to control the on/off state of the calibrate routine. Calibration is discussed more fully in the description of the software in Chapter 4.

5.2.3: The Output Board

Figure 5.3 is a general block diagram of the output board of the wattmeter. A detailed schematic drawing can be found in Appendix A as Figure A6.

As set out in Chapter 4, a pair of rotary switches determine what parameter from what phase is to be displayed:

<u>Rotary Switch 1</u>	<u>Rotary Switch 2</u>
Phase 1	V_{RMS}
Phase 2	I_{RMS}
Phase 3	Apparent Power
Aggregate/ Average	Active Power
	Power Factor
	Frequency
	Power Consumption
	15-Minute kVA Demand

The 8096 processor learns of the position of the pair of rotary switches by reading address E800H. That

FIGURE 5.3: GENERAL BLOCK DIAGRAM OF THE OUTPUT BOARD

address enables a pair of 74ALS373 gate chips which place encoded values from the rotary switches onto the data bus. All of the outputs from each rotary switch are pulled high, excepting the parameter selected on the respective switch; that selected parameter is pulled low by its connection to ground. Each set of rotary switch outputs forms the inputs to a respective 74LS148 8-to-3 encoder chip. The outputs of the encoder chips, along with a series of permanently high or low lines, form the inputs to the 74ALS373 three-state gate chips. With reference to the bottom portion of Figures 5.3 and A6, the rotary switch involved with phase selection encodes to the gate chip inputs corresponding with outputs to data lines D10 and D9, and the rotary switch involved with parameter choice (V_{RMS} , etc.) encodes to the gate chip inputs corresponding with outputs to data lines D8, D7 and D6. The gate chip inputs corresponding with outputs to data lines D15 and D12 are permanently held high, while the gate chip inputs corresponding with outputs to data lines D14, D13, D11, and D5 to D0 are permanently held low. In the result, when the 8096 processor reads address D800H, it reads the following value:

1 0 0 1 0 X X X X X 0 0 0 0 0 0

where the 2 leftmost X's represent the phase selected, and the 3 rightmost X's represent the parameter selected in that phase.

On being triggered by the XF pin of the TMS320C25 processor (at approximately 2-second intervals), the 8096 processor calculates the 8 parameters for each of the three phases, and also calculates a total or average value of the three phases for each parameter. The time remaining after completion of calculations in each 2-second interval is filled by the 8096 processor cycling in an endless loop, reading address E800H; only the EXTINT or HSI.0 interrupts

can break the endless loop.

The word that goes on the data bus by accessing address E800H reflects the value on each of the two rotary switches on the output board; that word is used as an address pointer to display RAM by the 8096 processor. The display RAM is a portion of the 8096 RAM, extending from word addresses 9000H to 97FEH. For instance, the phase-1 display RAM occupies word addresses 9000H to 91FEH in the following way:

<u>Addresses</u>	<u>Memory Contents</u>
9000H to 901EH	V O L T A G E _ R M S : _ _ _ _
9020H to 903EH	(. V) _ _ _ _
9040H to 905EH	C U R R E N T _ R M S : _ _ _ _
9060H to 907EH	(. A) _ _ x y
9080H to 909EH	A P P A R E N T _ P O W E R : _
90A0H to 90BEH	(. K W) _ _ _ _
90C0H to 90DEH	A C T I V E _ P O W E R : _ _ _
90E0H to 90FEH	(. K W) _ _ x y
9100H to 911EH	P O W E R _ F A C T O R : _ _ _
9120H to 913EH	(.) _ _ _ _ _ _
9140H to 915EH	F R E Q U E N C Y : _ _ _ _ _
9160H to 917EH	(. H Z) _ _ _ _ x y
9180H to 919EH	C O N S U M P T I O N : _ _ _ _
91A0H to 91BEH	(. K W H) _ _ _ _
91C0H to 91DEH	1 5 - M I N . _ D E M A N D : _
91E0H to 91FEH	(. K W) _ _ x y

where '_' stands for a space character (ASCII 20H), 'x' stands for a linefeed control character (ASCII 0AH), and 'y' stands for a carriage return control character (ASCII 0DH).

The 8 bracketed values are inserted by the respective software routines (described in Chapter 4) that calculate those values. The surrounding memory is filled by the 8096 initialization routine with the alphabetic content

shown above to provide context for downloading to a serial RS-232 output or a modem output (software for implementing those two outputs was not written).

On the output board is a 12-character display, comprising 3 four-character Siemens DL1416B alphanumeric intelligent display units. Access to the display is at address 1110 0XXX XXXX XXXXB, with address line A5 used to activate the CU pin of all 3 display units simultaneously and with address lines A4, A3, A2, A1 used to determine which of the 12 characters in the display are addressed. A 74LS139 dual 2-to-4 decoder chip is used to decode the address lines.

The output board further has 1488 and 1489 serial driver chips and a RS-232 connector for creating a serial interface with the TXD and RXD serial output and input pins of the 8096 processor. A DS6101 modem chip and a TIP/RING phone connector were also mounted on the output board; the modem chip was accessed at address F000H. Although hardware for both the serial input/output interface and the modem interface was placed on the output board, no software was written to implement either interface.

5.3: The Wattmeter Software

The software for the wattmeter is listed in Appendices C and D. Appendix C is a listing of the software for the TMS320C25 processor, and Appendix D lists the software for the 8096 processor. The software routines are generally described in Chapter 4.

CHAPTER 6

EXPERIMENTAL RESULTS

6.1: Introduction

6.1.1: The Test Facility

Tests on the wattmeter were conducted by the writer at the National Research Council of Canada. The facilities at the Council for testing the accuracy of commercial wattmeters and watthour meters are described in [FIL, 1987] and [FIL, 1990].

The testing equipment was capable of delivering periodic voltage and current waveforms --- either sinusoidal or with harmonic content. The maximum voltage and current levels depended on the shape of the waveform. For sinusoidal waveforms 120-volt and 10-ampere RMS outputs were possible, but for some other waveforms the maximum RMS outputs were lower. Where possible, the tests on the subject wattmeter used 120-volt RMS and 5-ampere RMS waveforms. A RMS value of 5 amperes for current did not prove a problem for any waveform; however, for some waveforms a RMS value of 120 volts was not achievable; in those cases, a lower RMS value had to be used.

The testing equipment, which was operated from a computer console, allowed variation of RMS voltage and current output values between zero and the particular maximum. The phase angle between voltage and current could be varied between -180° and $+180^\circ$. For the tests, the frequency selection for the output waveforms was limited to 50 and 60 Hz. Additional equipment is available at the Council that allows continuous frequency variation on the output waveforms from the testing facility. Though that additional equipment was available during an earlier demonstration of

the wattmeter, it was not available during the tests described here. However, the earlier demonstration did show the frequency measurement capability of the wattmeter.

The test facility had a library of stored waveforms available for generation as either the voltage or current output; for instance, Waveform No. 0001 was a sinusoidal waveform. One set of waveforms in the library had precise information readily available on such factors as:

- the number of harmonics;
- whether the harmonics were odd or even, or both;
- the amplitude of the harmonics, i.e. constant, $1/n$ or $1/n^2$, where 'n' is the harmonic number;
- total harmonic distortion;
- number of zero crossing points.

The computer console was connected to a precision voltage/current generator built at the Council. Besides having voltage and current outputs that were connected to the wattmeter of this thesis, the generator produced an indicator voltage output proportional to the average active power in the voltage and current outputs. The indicator voltage output was connected to a high-precision digital voltmeter; the voltmeter readout in volts was directly proportional to the average active power represented in the voltage and current outputs of the generator. The active power produced by the generator was estimated to be accurate to within 50 parts/million (50 ppm) of the value displayed on the voltmeter.

6.1.2: The Test Procedure

After selection of a waveform for voltage and/or current, the particular waveform was called from the waveform library within the computer. Next, the RMS value of the waveform was adjusted to the desired value. The selec-

ted value and the value displayed on the computer console never exactly matched because of software factors. For instance, when 120 volts RMS was selected, the console displayed the value as anywhere between 119.993 volts RMS and 119.998 volts RMS. Once the particular waveforms for the voltage and current were selected and the RMS values for those waveforms were set, any phase angle between the two waveforms was selected.

With the testing equipment producing the desired voltage and current outputs, the wattmeter of the thesis was calibrated to match those RMS values. As set out in Chapter 4, the wattmeter creates a calibration factor for both RMS voltage and current by using a series of DIP switches. By varying those switches, the values displayed for RMS voltage and current on the meter can be made to match very closely the RMS voltage and current values on the testing equipment. For instance, in one set of tests a RMS voltage of 119.993 volts and RMS current of 4.99968 amperes on the testing equipment were matched by a RMS voltage of 119.992 volts and RMS current of 4.9996 amperes, respectively, on the wattmeter. Because of this ability to closely match initial voltage and current values in the wattmeter with those in the testing equipment, calibration was not a significant source of error in the tests.

Where possible, both asynchronous and synchronous sampling (256 samples/waveform) were taken. Synchronous sample readings were only recorded where the readings were stable and not undergoing wide fluctuation.

6.2: Results of Active Power Measurement Tests

6.2.1: Active Power Variation with Power Level

This test was conducted with 60-hertz sinusoidal

2

PM-1 3 1/2"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

PRECISIONSM RESOLUTION TARGETS

PIONEERS IN METHYLENE BLUE TESTING SINCE 1974

MicroD
RESOLUTION

1880 COUNTY ROAD 6, BURNING WOOD, OH 44027 USA
TEL: 814 485 7857 FAX: 814 485 7857 TLA 814857857

in-phase voltage and current waveforms. The RMS voltage level was nominally set at 120 volts, but appeared on the computer console screen as 119.996 volts; the wattmeter RMS voltage was matched as closely as possible (119.987 volts RMS) by adjustment of the calibration DIP switches. The RMS current was initially set at a nominal 5 amperes, which appeared on the screen of the computer console as 4.9997 amperes; the wattmeter's RMS current was set as closely as possible --- at 4.9996 amperes. The RMS current output of the testing equipment was then decremented in 0.5-ampere steps from the nominal initial value of 5 amperes to a nominal final value of 0.5 amperes. The active power displayed on the testing equipment was compared with the active power displayed on the wattmeter by both asynchronous and synchronous (256 samples/voltage waveform) sampling. The apparent power was also recorded on the wattmeter, using both asynchronous and synchronous sampling.

Table 6.1 contains the results of that test (all power values are in watts, and current is in amperes). A '5' as the fifth digit on some wattmeter values indicates that the display was oscillating between two values, i.e. 539.95 indicates an oscillation between 539.9 and 540.0. Table 6.1 includes a listing of the difference between the active power measured with asynchronous sampling and the active power measured on the testing equipment. The difference is taken as a percentage of the active power full scale range (FSR). For instance, at an active power setting on the test equipment of 599.95 watts the percentage FSR difference for the asynchronously-sampled active power is:

$$\frac{(599.95 - 599.9) \cdot (100\%)}{600} = +0.008\%$$

A large part of this percentage difference turns on the wattmeter having only 4 digits in the active power read-

out. The percentage difference is plotted in Graph 6.1.

TABLE 6.1
ACTIVE POWER VARIATION WITH POWER LEVEL

<u>Testing Equipment</u>		<u>Wattmeter</u>				<u>Wattmeter</u>	
<u>Current</u>	<u>Active Power</u>	<u>Active Power</u>				<u>Apparent Power</u>	
		<u>Asynch.</u>	<u>(% FSR Diff.)</u>	<u>Synch.</u>	<u>(% FSR Diff.)</u>	<u>Asynch.</u>	<u>Synch.</u>
4.9997	+599.95	+599.9	+0.008%	+599.8	+0.025%	599.9	599.8
4.49998	+539.98	+539.95	+0.005%	+540.0	-0.003%	539.95	540.0
3.99979	+479.96	+479.9	+0.010%	+480.0	-0.007%	479.9	480.0
3.49960	+419.94	+419.95	-0.002%	+420.0	-0.010%	419.95	420.0
2.9998	+359.97	+359.95	+0.003%	+360.0	-0.005%	359.95	360.0
2.4996	+299.95	+299.95	0.000%	+299.9	+0.008%	299.95	299.9
1.9998	+239.98	+240.0	-0.003%	+240.0	-0.003%	240.0	240.0
1.4997	+179.96	+180.0	-0.007%	+180.0	-0.007%	180.0	180.0
0.99995	+119.99	+120.0	-0.002%	+120.0	-0.002%	120.0	120.0
0.49976	+59.97	+60.0	-0.005%	+59.9	+0.012%	60.0	59.9

GRAPH 6.1

PERCENTAGE FSR DIFFERENCE BETWEEN ACTIVE POWER OF TESTING EQUIPMENT AND WATTMETER (ASYNCH. AND SYNCH. SAMPLES) VERSUS POWER LEVEL (DATA FROM TABLE 6.1)

% FSR
Diff.

6.2.2: Active Power Variation With Phase Angle

A series of tests were run in which the phase angle between the voltage waveform and the current waveform was adjusted in 10° increments from -90° to $+90^\circ$, and the Active Power displayed by the testing equipment compared with the asynchronously-measured Active Power displayed by the wattmeter (Apparent Power on the wattmeter also being recorded).

6.2.2.(a): Sinusoidal Voltage and Current Waveforms

In this test, Waveform No. 0001 (sinusoid) was used for both the voltage and current waveforms. Calibration was performed by matching a testing equipment voltage value of 119.9960 volts RMS with 119.987 volts RMS on the wattmeter, and 4.9997 amperes RMS on the testing equipment with 4.9996 amperes RMS on the wattmeter. Synchronous, as well as asynchronous, sampling was used. The results are shown in Table 6.2 and Graph 6.2.

TABLE 6.2

VARIATION OF ACTIVE POWER WITH PHASE ANGLE FOR
SINUSOIDAL VOLTAGE AND CURRENT WAVEFORMS

Testing Equipment		Wattmeter				Wattmeter	
Phase Angle	Active Power	Active Power				Apparent Power	
		Asynch.	(% FSR Diff.)	Synch.	(% FSR Diff.)	Asynch.	Synch.
-90°	+0.000241	+0.0000	0.000%	+0.0000	0.000%	599.9	599.9
-80°	+104.180	+104.1	+0.013%	+104.0	+0.030%	599.9	599.9
-70°	+205.195	+205.1	+0.016%	+205.0	+0.033%	599.9	599.9
-60°	+299.975	+299.9	+0.013%	+299.8	+0.029%	599.9	599.9
-50°	+385.640	+385.6	+0.007%	+385.5	+0.023%	599.9	599.9
-40°	+459.588	+459.5	+0.015%	+459.4	+0.031%	599.8	599.8
-30°	+519.571	+519.5	+0.012%	+519.4	+0.018%	599.9	599.8
-20°	+563.768	+563.7	+0.011%	+563.6	+0.028%	599.8	599.8
-10°	+590.835	+590.8	+0.006%	+590.7	+0.023%	599.9	599.8
0°	+599.950	+599.9	+0.008%	+599.8	+0.025%	599.9	599.8
+10°	+590.835	+590.8	+0.006%	+590.7	+0.023%	599.8	599.8
+20°	+563.768	+563.8	-0.005%	+563.8	-0.005%	599.8	599.9
+30°	+519.571	+519.6	-0.005%	+519.6	-0.005%	599.9	599.9
+40°	+459.588	+459.6	-0.002%	+459.6	-0.002%	599.9	599.9
+50°	+385.640	+385.7	-0.010%	+385.7	-0.010%	599.9	599.8
+60°	+299.975	+300.0	-0.004%	+300.0	-0.004%	599.9	599.8
+70°	+205.195	+205.2	-0.001%	+205.2	-0.001%	599.9	599.9
+80°	+104.180	+104.2	-0.003%	+104.2	-0.003%	599.9	599.8
+90°	+0.000026	+0.0001	0.000%	-0.0000	0.000%	599.9	599.9

GRAPH 6.2

PERCENTAGE FSR DIFFERENCE BETWEEN ACTIVE POWER OF TESTING
EQUIPMENT AND WATTMETER (ASYNCH. AND SYNCH. SAMPLES) VERSUS
PHASE ANGLE (DATA FROM TABLE 6.2)

% FSR
Diff.

6.2.2.(b): Periodic Nonsinusoidal Waveforms

For this test, Waveforms No. 0256 and No. 0257, illustrated in Figure 6.1, were used for voltage and current, respectively. Each contains 49 harmonics. The current was nominally 5 amperes; the highest RMS voltage that was possible with Waveform No. 0256 was 103.997 volts (corresponding wattmeter setting = 104.000 volts). Table 6.3 lists the power values (in watts) recorded as the phase angle was varied between -90° and $+90^\circ$. The percentage difference in active power is recorded in Graph 6.3. Because of large fluctuations, no synchronous values were recorded.

TABLE 6.3

VARIATION OF ACTIVE POWER WITH PHASE ANGLE FOR PERIODIC NONSINUSOIDAL VOLTAGE AND CURRENT WAVEFORMS

<u>Testing Equipment</u>		<u>Wattmeter</u>		<u>Wattmeter</u>
<u>Phase Angle</u>	<u>Active Power</u>	<u>Active Power</u>	<u>(% FSR Diff.)</u>	<u>Apparent Power</u>
		<u>Asynch.</u>		<u>Asynch.</u>
-90°	+441.406	+441.4	-0.001%	519.9
-80°	+467.897	+467.8	+0.019%	519.9
-70°	+482.037	+482.0	+0.007%	519.9
-60°	+480.376	+480.4	-0.005%	519.9
-50°	+462.819	+462.8	+0.004%	519.9
-40°	+431.072	+431.1	-0.005%	519.9
-30°	+384.478	+384.5	-0.004%	519.9
-20°	+326.567	+326.6	-0.006%	519.9
-10°	+259.349	+259.4	-0.010%	519.9
0°	+190.744	+190.8	-0.011%	519.9
$+10^\circ$	+116.893	+116.9	-0.001%	519.9
$+20^\circ$	+32.371	+32.4	-0.006%	519.9
$+30^\circ$	-53.642	-53.5	-0.027%	519.9
$+40^\circ$	-138.793	-138.7	-0.018%	519.8
$+50^\circ$	-217.863	-217.7	-0.031%	519.8
$+60^\circ$	-289.003	-288.9	-0.020%	519.8
$+70^\circ$	-351.702	-351.6	-0.020%	519.8
$+80^\circ$	-401.235	-401.1	-0.026%	519.8
$+90^\circ$	-441.195	-441.1	-0.018%	519.8

FIGURE 6.1: WAVEFORMS NO. 0256 AND NO. 0257

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WAVEFORM NRC256

VOLTAGE

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WAVEFORM NRC257

CURRENT

GRAPH 6.3

PERCENTAGE FSR DIFFERENCE BETWEEN ACTIVE POWER OF TESTING EQUIPMENT AND WATTMETER (ASYNCH. SAMPLES) VERSUS PHASE ANGLE
(DATA FROM TABLE 6.3)

% FSR
Diff.

6.2.3: Active Power Variation with Harmonic Content

Three sets of tests were run to determine the accuracy of the wattmeter in measuring the active power in waveforms with different harmonic content. A first test was run with Waveform No. 7031. All harmonics up to the 50th. were present; each of the harmonics had an amplitude 0.0014 times that of the primary waveform. A second test was run with Waveform No. 7064. All odd harmonics up to the 49th. were present; each of the harmonics had an amplitude $1/n$ times that of the primary waveform (where 'n' is the harmonic number, i.e. the amplitude of the fifth harmonic was $1/5$ the amplitude of the prime waveform). A third test was run with Waveform No. 7110. All harmonics up to the 50th. were present; each of the harmonics had an amplitude $1/n^2$ times that

of the primary waveform (where 'n' is the harmonic number, i.e. the amplitude of the fifth harmonic was 1/25 the amplitude of the prime waveform). The total harmonic distortion (THD) of Waveform Nos. 7031, 7064 and 7110 was the same --- 0.01.

6.2.3.(a): Harmonics With Constant Amplitude

For this test, Waveform No. 7031 (illustrated in Figure 6.2) was used as both the voltage and current waveform. All harmonics up to the 50th. were present, and each had an amplitude 0.0014 times the amplitude of the primary waveform. Synchronous values had large fluctuations, and were not recorded.

TABLE 6.4

VARIATION OF ACTIVE POWER WITH PHASE ANGLE:
FIRST 50 HARMONICS PRESENT, ALL OF EQUAL AMPLITUDE

<u>Testing Equipment</u>		<u>Wattmeter</u>		<u>Wattmeter</u>
<u>Phase</u>	<u>Active Power</u>	<u>Active Power</u>		<u>Apparent Power</u>
<u>Angle</u>		<u>Asynch.</u>	<u>(% FSR Diff.)</u>	<u>Asynch.</u>
-90°	-0.001465	-0.0001	0.000%	599.9
-80°	+104.166	+104.0	+0.028%	599.9
-70°	+205.1659	+205.0	+0.028%	599.9
-60°	+299.933	+299.8	+0.022%	599.9
-50°	+385.586	+385.4	+0.031%	599.9
-40°	+459.523	+459.4	+0.021%	599.9
-30°	+519.5017	+519.4	+0.017%	599.9
-20°	+563.6866	+563.6	+0.014%	599.9
-10°	+590.757	+590.7	+0.010%	599.9
0°	+599.928	+599.9	+0.005%	599.9
+10°	+590.757	+590.8	-0.007%	599.9
+20°	+563.6866	+563.65	+0.006%	599.9
+30°	+519.5016	+519.5	0.000%	599.9
+40°	+459.523	+459.5	+0.004%	599.9
+50°	+385.586	+385.6	-0.002%	599.9
+60°	+299.933	+299.9	+0.006%	599.9
+70°	+205.1648	+205.2	-0.006%	599.9
+80°	+104.1661	+104.2	-0.006%	599.9
+90°	-0.00125	+0.0000	0.000%	599.85

FIGURE 6.2: WAVEFORM NO. 7031

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WAVEFORM NRC7031

POLYMER

GRAPH 6.4

PERCENTAGE FSR DIFFERENCE BETWEEN ACTIVE POWER OF TESTING
EQUIPMENT AND WATTMETER (ASYNCH. SAMPLES) VERSUS PHASE ANGLE
(DATA FROM TABLE 6.4)

% FSR
Diff.

6.2.3.(b): Harmonics With '1/n' Amplitude

For this test, Waveform No. 7064 (illustrated in Figure 6.3) was used as both the voltage and current waveform. All odd harmonics up to the 49th. were present, and each had an amplitude $1/n$ times the amplitude of the primary waveform ('n' being the number of the harmonic). After voltage and current calibration of the wattmeter, the power values (in watts) of Table 6.5 were recorded as the phase angle was varied between -90° and $+90^\circ$. Synchronous values were not recorded.

TABLE 6.5

VARIATION OF ACTIVE POWER WITH PHASE ANGLE:
ALL ODD HARMONICS TO THE 49TH. PRESENT, ALL '1/N' AMPLITUDE

<u>Testing Equipment</u>		<u>Wattmeter</u>		<u>Wattmeter</u>
<u>Phase</u>	<u>Active Power</u>	<u>Active Power</u>		<u>Apparent Power</u>
<u>Angle</u>		<u>Asynch.</u>	<u>(% FSR Diff.)</u>	<u>Asynch.</u>
-90°	-0.000249	-0.0001	0.000%	620.3
-80°	+107.700	+107.5	+0.032%	620.3
-70°	+212.1299	+212.0	+0.021%	620.3
-60°	+310.1161	+309.95	+0.027%	620.3
-50°	+398.6830	+398.5	+0.030%	620.3
-40°	+475.1406	+475.0	+0.023%	620.3
-30°	+537.1675	+537.1	+0.011%	620.3
-20°	+582.879	+582.8	+0.013%	620.3
-10°	+610.889	+610.9	-0.002%	620.3
0°	+620.3436	+620.3	+0.007%	620.3
$+10^\circ$	+610.8893	+610.9	-0.002%	620.3
$+20^\circ$	+582.879	+582.9	-0.003%	620.3
$+30^\circ$	+537.1675	+537.2	-0.005%	620.3
$+40^\circ$	+475.1408	+475.1	+0.007%	620.3
$+50^\circ$	+398.6830	+398.7	-0.003%	620.3
$+60^\circ$	+310.116	+310.1	+0.003%	620.3
$+70^\circ$	+212.1297	+212.1	+0.005%	620.3
$+80^\circ$	+107.700	+107.7	0.000%	620.3
$+90^\circ$	-0.000027	+0.0000	0.000%	620.3

FIGURE 6.3: WAVEFORM NO. 7064

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WAVEFORM NRC7064

VOLTAGE

GRAPH 6.5

PERCENTAGE FSR DIFFERENCE BETWEEN ACTIVE POWER OF TESTING
EQUIPMENT AND WATTMETER (ASYNCH. SAMPLES) VERSUS PHASE ANGLE
(DATA FROM TABLE 6.5)

% FSR
Diff.

6.2.3.(c): Harmonics With '1/n²' Amplitude

For this test, Waveform No. 7110 (illustrated in Figure 6.4) was used as both the voltage and current waveform. All harmonics up to the 50th. were present, and each had an amplitude $1/n^2$ times the amplitude of the primary waveform ('n' being the number of the harmonic). After voltage and current calibration of the wattmeter, the power values (in watts) of Table 6.6 were recorded as the phase angle was varied between -90° and $+90^\circ$. Synchronous values were not recorded.

TABLE 6.6

**VARIATION OF ACTIVE POWER WITH PHASE ANGLE:
FIRST 50 HARMONICS PRESENT, ALL '1/N²' AMPLITUDE**

<u>Testing Equipment</u>		<u>Wattmeter</u>		<u>Wattmeter</u>
<u>Phase</u>	<u>Active Power</u>	<u>Active Power</u>		<u>Apparent Power</u>
<u>Angle</u>		<u>Asynch.</u>	<u>(% FSR Diff.)</u>	<u>Asynch.</u>
-90°	-0.043374	-0.0001	0.000%	599.9
-80°	+104.1268	+103.9	+0.038%	599.9
-70°	+205.137	+205.0	+0.023%	599.9
-60°	+299.918	+299.8	+0.020%	599.9
-50°	+385.591	+385.5	+0.015%	599.9
-40°	+459.550	+459.4	+0.025%	599.9
-30°	+519.549	+519.5	+0.008%	599.9
-20°	+563.761	+563.7	+0.010%	599.9
-10°	+590.841	+590.8	+0.007%	599.9
0°	+599.961	+600.0	-0.007%	599.9
+10°	+590.841	+590.9	+0.010%	599.9
+20°	+563.761	+563.8	-0.007%	599.9
+30°	+519.549	+519.6	-0.009%	599.9
+40°	+459.550	+459.55	0.000%	599.9
+50°	+385.591	+385.6	-0.002%	599.9
+60°	+299.918	+299.9	+0.003%	599.9
+70°	+205.137	+205.1	+0.006%	599.9
+80°	+104.127	+104.1	+0.005%	599.9
+90°	-0.04316	-0.0000	-0.007%	599.9

FIGURE 6.4: WAVEFORM NO. 7110

GRAPH 6.6

PERCENTAGE FSR DIFFERENCE BETWEEN ACTIVE POWER OF TESTING
EQUIPMENT AND WATTMETER (ASYNCH. SAMPLES) VERSUS PHASE ANGLE
(DATA FROM TABLE 6.6)

% FSR
Diff.

6.3: Results of 15-Min. kVA Demand Measurement Tests

For this set of tests the voltage on the testing equipment was set nominally at 120 volts RMS and the current was set nominally at 4 amperes RMS. The wattmeter was calibrated such that its voltage and current corresponded very closely with the testing equipment values. The Waveform No. 0001 (sinusoid) was used for both the voltage and current waveforms. The storage RAM area for the 15-min. kVA demand value was set to zero through the calibration routine.

The rotary switches on the output board were then turned to Phase 1 and 15-Min. kVA Demand, and the display observed. As soon as the calibration routine was disconnected, the 15-min. kVA demand started to increase at a steady rate, and stopped increasing 15 minutes later at a value of 0.480 kVA.

The current was then ramped as shown in Figure 6.5. For 3-minute intervals, the current was held sequentially at 4.1 amperes, 4.2 amperes, 4.3 amperes, 4.2 amperes and 4.1 amperes, finally being returned to 4.0 amperes. A stopwatch was used to time the entry of the changed current values on the console of the testing equipment. After entry of the 5 current values over the 15-minute interval, a 15-min. kVA demand value of 0.5018 kVA was displayed; this compared with the theoretical value of 0.5016 kVA. The current was then modified again, such that for 3-minute intervals it was held sequentially at 4.5 amperes, 4.7 amperes, 4.9 amperes, 4.7 amperes and 4.5 amperes, then returned to 4.0 amperes. The new 15-min. kVA demand value displayed was 0.5597 kVA; this compared with the theoretical value of 0.5592 kVA.

Apart from any inaccuracy in the meter on this set of tests, one source of error was the manual timing of the 3-minute intervals.

FIGURE 6.5: 15-MIN. KVA DEMAND TRACKING CURRENT CHANGE

6.4: Stability of the Meter

The test relating to variation of active power with phase angle for sinusoidal waveforms, for which the results are listed in Table 6.2, was repeated four hours after the initial test. There was no difference in the results between the two tests.

CHAPTER 7

CONCLUSIONS

7.1: Summary

A wattmeter/watthour meter was developed based on asynchronous sampling, and utilizing two processors working in tandem. A first processor was used for fast multiplication and summation of products, while the second performed calculation and display functions based on data passed by the first. The meter was capable of determining a series of power parameters from voltage and current waveforms, and optimized for 3-phase measurement at 60 hertz. The parameters determined were RMS voltage and RMS current, apparent and active power, power factor and frequency, power consumption and 15-min. kVA demand. A synchronous sampling capability was included in the meter to allow a comparison with asynchronous sampling.

Samples were gathered in 117-cycle intervals, each interval lasting approximately 2 seconds. At 60 hertz, 256 samples/cycle were gathered --- more at lower frequencies, less at higher frequencies. Since the spacing between samples was based on an external clock, the sample count over a 117-cycle interval was utilized to determine the frequency of the voltage and current waveforms. The meter was capable of measuring frequency between approximately 34 and 63 Hz to an accuracy better than one sample width per 117 waveform periods (approximately 1 part in 30,000 at 60 hertz).

After voltage and current RMS inputs on the meter were calibrated against corresponding outputs from testing equipment, a series of comparisons were made between active power readings on the testing equipment and active power measured by the meter. The results, which are contained in Chapter 6, indicate a maximum difference in asynchronously-

measured active power between the testing equipment and the meter of approximately 0.03%. The testing equipment had an estimated accuracy of 0.005%.

Active power measurement using synchronous sampling fluctuated widely for nonsinusoidal voltage waveforms, and values based on synchronous sampling were only recorded for sinusoidal waveforms. For sinusoidal waveforms the synchronous and asynchronous active power values on the meter were either identical --- or differed only slightly. When active power values of the testing equipment and asynchronously-measured active power values of the meter were compared for sinusoidal waveforms, the maximum difference was found to be under 0.02%. The difference was greater for negative phase angles (current leading voltage) than for positive phase angles.

Four sets of tests were run for nonsinusoidal waveforms. A first set involved voltage and current waveforms each comprising 49 harmonics and having a shape differing substantially from the sinusoidal shape. The other 3 sets of nonsinusoidal waveforms had specifically-defined harmonic content: one having all harmonics up to the 50th. (all equal in amplitude), one having odd harmonics up to the 49th. (all of amplitude ' $1/n$ '), and one having all harmonics up to the 50th. (all of amplitude ' $1/n^2$ '). Only asynchronous sampling was used for the four sets of tests, after synchronous sampling resulted in wide fluctuation at each meter setting.

When active power values of the testing equipment and asynchronously-measured active power values of the meter were compared for the four sets of tests, the maximum difference was found to be approximately 0.03%. The difference was generally higher for positive phase angles for the first set of tests, but was generally higher for negative phase angles for the three sets of tests with waveforms with known harmonic content.

Measurements were made of 15-min. kVA demand with

the meter. The measured and theoretical values differed by approximately 0.9% in each of two tests. Unfortunately, the measurement technique was rather crude.

The general sources of error with the meter were:

- (1) truncation error of approximately 0.003% from the asynchronous sampling (based on [STEN, 1984]);
- (2) A/D converter error of approximately 0.003% (based on tests showing random oscillation only in the least significant bit of the 16-bit A/D converters); and,
- (3) the limited digital readout (for instance, only four digits in the active power readout represented an error of $0.017\% \left(\frac{0.1}{600}\right)$).

7.2: Claims Of Innovation

A wattmeter/watthour meter, utilizing asynchronous sampling and employing two commercially-available general processors operating in tandem on functions for which they are most suitable, has been shown to be feasible. Although wattmeters utilizing two processors are known in the literature ([WOOD, 1985] and [MAL, 1981]), the processors of those meters were not closely matched to the particular processing functions within the meter.

The gathering of voltage and current samples asynchronously over 117 periods of the voltage waveform provided a basis for highly-accurate frequency determination. The accuracy was within one sample period over the 117 waveform periods, which at 60 hertz equated to approx. 1/30,000. The literature includes meters capable of measuring waveform frequency by counting asynchronous samples over a waveform

considerably less than that of the thesis wattmeter.

Although asynchronous sampling wattmeters have been previously built, no meter with zero-crossing detection has been located which incorporated as many samples into each sampling interval and thus into each parameter calculation as did this meter. For instance, [STEN, 1984] refers to a 35-bit accumulator and [RIAZ, 1985] refers to a 27-bit accumulator. The meter of this thesis utilized a 48-bit accumulator for each of three parameters over three phases. The accuracy obtained was in part due to large number of samples gathered during each sampling interval.

This meter combined synchronous and asynchronous sampling in a single device, which allowed a comparison of the two sampling techniques directly through the same input channels. Unfortunately, the phase-lock loop was not very stable.

7.3: Future Work

Building on the meter of this thesis, future work could be carried out in several directions.

In respect of reducing construction detail of the meter described here, the two processors used in the meter have now been available for about 5 years, and the price of them has declined since their initial availability and the design of this meter. An EPROM version of the TMS320C25 processor is now available, and the program code developed for this thesis could be incorporated into that EPROM chip. Similarly, the program code for the 8096 processor could be incorporated into its EPROM version (8796 chip).

The phase-lock loop circuit on the input board could be improved. Also, the autoranging display software for 8096 processor in the existing meter could be modified to add a fifth digit to the active power readout. Alter-

natively, the existing four-digit readout could be retained but a series of perhaps 100 readings be taken at each test setting. If then, for example, 30 of the values indicated an active power value of 457.1 W and 70 of the values indicated an active power value of 457.2 W, one might extrapolate the steady-state active power value to be 457.17 W.

In respect of possibly constructing a more powerful meter based on the general design described here, the Texas Instruments' line of fast-multiplier signal processing chips has now advanced with improved multiply/accumulate and other instructions and with reduced instruction cycle time. Using the algorithms developed for this meter, it is probably now possible to include 512 asynchronous samples or more in each period of a 60-hertz waveform. The writer, however, doubts such change would result in an improvement in accuracy.

The algorithms used in the calculation of power consumption and 15-min. kVA demand could be improved by removing their dependence on frequency. One way to do that would involve using the number of samples collected during each sampling interval to create a power consumption correction factor. The power consumption and 15-min. kVA demand values would be multiplied by the correction factor in modifications to their existing algorithms (which would maintain the basis of each hour having 1800 sampling intervals). The correction factor, applied each sampling interval, would be:

$$\frac{(117) \cdot (256)}{\text{No. of Samples/Sampling Interval}} \cdot \frac{120}{117}$$

APPENDIX A:
DETAILED SCHEMATIC DRAWINGS OF THE METER

FIG. A1: INPUT BOARD SCHEMATIC (PART 1 OF 2)

FIG. A3: MAIN BOARD SCHEMATIC (PART 1)

FIG. A4: MAIN BOARD SCHEMATIC (PART 2 OF 3)

FIG. A5: MAIN BOARD SCHEMATIC (PART 3 OF 3)

FIG. A6: OUTPUT BOARD SCHEMATIC

APPENDIX B:
PHOTOGRAPHS OF THE METER

FIGURE B1: FRONT PERSPECTIVE VIEW OF THE METER

FIGURE B2: BACK PERSPECTIVE VIEW OF THE METER

FIGURE B3: TOP PLAN VIEW OF THE TWO PARTS OF THE
MAIN BOARD OF THE METER

FIGURE B4: BOTTOM PLAN VIEW OF THE TWO PARTS OF THE
MAIN BOARD OF THE METER

APPENDIX C:
SOURCE CODE FOR THE TMS320C25 PROCESSOR

TMS320C25 PROGRAMINITIALIZATION

<u>ADDRESS</u>		<u>COMMAND</u>	<u>CYCLES</u>	<u>OBJECT CODE</u>	<u>COMMENTS</u>
0000H	RESET	B INIT1	2	FFH 80H	;branch to main program
0001H				00H 20H	
0002H	INT0	POP	1	CEH 1DH	;jump to address in accumulator
0003H		RET	1	CEH 26H	; on each INTO interrupt
0004H		NOP	1	55H 00H	
0005H		NOP	1	55H 00H	
0006H		NOP	1	55H 00H	
0007H		NOP	1	55H 00H	
0008H		NOP	1	55H 00H	
0009H		NOP	1	55H 00H	
000AH		NOP	1	55H 00H	
000BH		NOP	1	55H 00H	
000CH		NOP	1	55H 00H	
000DH		NOP	1	55H 00H	
000EH		NOP	1	55H 00H	
000FH		NOP	1	55H 00H	
0010H		NOP	1	55H 00H	
0011H		NOP	1	55H 00H	
0012H		NOP	1	55H 00H	
0013H		NOP	1	55H 00H	
0014H		NOP	1	55H 00H	
0015H		NOP	1	55H 00H	
0016H		NOP	1	55H 00H	
0017H		NOP	1	55H 00H	
0018H		POP	1	CEH 1DH	;jump to address in accumulator
0019H		RET	1	CEH 26H	; on each TINT interrupt
001AH		NOP	1	55H 00H	
001BH		NOP	1	55H 00H	
001CH		NOP	1	55H 00H	
001DH		NOP	1	55H 00H	
001EH		NOP	1	55H 00H	
001FH		NOP	1	55H 00H	
0020H	INIT1	SOVM	1	CEH 03H	;set overflow mode
0021H		LDPK 00	1	C8H 00H	;load page 0
0022H		LACK COH	1	CAH C0H	;set TINT interrupt
0023H		AND DAT04	1	4EH 04H	
0024H		SACL 0,DAT04	1	60H 04H	
0025H		LACK 08H	1	CAH 08H	
0026H		OR DAT04	1	4DH 04H	
0027H		SACL 0,DAT04	1	60H 04H	
0028H		LDPK 04	1	C8H 04H	
0029H		LACK 0A0H	1	CAH A0H	;load DAT00 with counter
002AH		SACL 0,DAT00	1	60H 00H	
002BH		LACK 01H	1	CAH 01H	;load DAT01 with 1
002CH		SACL 0,DAT01	1	60H 01H	
002DH		ZALS DAT00	1	41H 00H	;decrement counter for 1 second

002EH	SUBS DAT01	1	45H 01H	; delay
002FH	SACL 0,DAT00	1	60H 00H	.
0030H	BZ INIT2	2/3	F6H 80H	
0031H			00H 39H	
0032H	LALK 002DH	2	DOH 01H	
0033H			00H 2DH	
0034H	PUSH	1	CEH 1CH	
0035H	EINT	1	CEH 00H	
0036H	WAIT NOP	1	55H 00H	
0037H	B WAIT	3	FFH 80H	
0038H			00H 36H	
0039H	INIT2 LDPK 00	1	C8H 00H	;load TIM and PRD with 650
003AH	LALK 028AH	2	DOH 01H	
003BH			02H 8AH	
003CH	SACL 0,DAT03	1	60H 03H	
003DH	ZAC	1	CAH 00H	;put zero in all data memory
003EH	LARP 07H	1	55H 8FH	; addresses
003FH	LARK AR7,96+	1	C7H 60H	
0040H	RPTK 31	1	CBH 1FH	
0041H	SACL *+	1	60H A0H	
0042H	LRLK AR7,512+	2	D7H 00H	
0043H			02H 00H	
0044H	RPTK 255	1	CBH FFH	
0045H	SACL *+	1	60H A0H	
0046H	RPTK 255	1	CBH FFH	
0047H	SACL *+	1	60H A0H	
0048H	RSXM	1	CEH 06H	;drop sign-extension mode
0049H	LDPK 4	1	C8H 04H	;load page 4
004AH	LACK 03H	1	CAH 03H	;load 3 in DAT05
004BH	SACL 0,DAT05	1	60H 05H	
004CH	LACK 01H	1	CAH 01H	;load 1 in DAT04
004DH	SACL 0,DAT04	1	60H 04H	
004EH	LALK OFFFFH	2	DOH 01H	;load OFFFFH in DAT1F
004FH			FFH FFH	
0050H	SACL 0,DAT1F	1	60H 1FH	
0051H	LACK 78H	1	CAH 78H	;load 120 in DAT06, DAT26
0052H	SACL 0,DAT06	1	60H 06H	; and DAT46
0053H	SACL 0,DAT26	1	60H 26H	
0054H	SACL 0,DAT46	1	60H 46H	
0055H	LACK 75H	1	CAH 75H	;load 117 in DAT07, DAT27
0056H	SACL 0,DAT07	1	60H 07H	; and DAT47
0057H	SACL 0,DAT27	1	60H 27H	
0058H	SACL 0,DAT47	1	60H 47H	
0059H	LALK 120H	2	DOH 01H	;load 288 in DAT60, DAT61,
005AH			01H 20H	; DAT62, DAT63, DAT64 and
005BH	SACL 0,DAT60	1	60H 60H	; DAT65
005CH	SACL 0,DAT61	1	60H 61H	
005DH	SACL 0,DAT62	1	60H 62H	
005EH	SACL 0,DAT63	1	60H 63H	
005FH	SACL 0,DAT64	1	60H 64H	
0060H	SACL 0,DAT65	1	60H 65H	
0061H	LALK 7500H	2	DOH 01H	;load 29952 in DAT66, DAT67,

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0062H          75H 00H ; DAT68, DAT69, DAT6A and
0063H          SACL 0,DAT66 1 60H 66H ; DAT6B
0064H          SACL 0,DAT67 1 60H 67H
0065H          SACL 0,DAT68 1 60H 68H
0066H          SACL 0,DAT69 1 60H 69H
0067H          SACL 0,DAT6A 1 60H 6AH
0068H          SACL 0,DAT6B 1 60H 6BH
0069H ONE      IN 001 DAT01 2 81H 01H ;input phase-1 voltage
006AH          BIT 15,DAT01 1 90H 01H
006BH          BBNZ TWO 2/3 F9H 80H ;if negative, jump to TWO
006CH          00H 79H ; to see if goes positive
006DH          ZALS DAT60 1 41H 60H ;decrement DAT60
006EH          SUBS DAT04 1 45H 04H
006FH          SACL 0,DAT60 1 60H 60H
0070H          BZ THREE 2/3 F6H 80H ;if inputs are still positive
0071H          00H 92H ; after 288 inputs, goto THREE
0072H          LALK 0069H 2 DOH 01H ;load address of ONE, enable
0073H          00H 69H ; interrupts, and wait for
0074H          PUSH 1 CEH 1CH ; TINT interrupt
0075H          EINT 1 CEH 00H
0076H FOUR     NOP 1 55H 00H
0077H          B FOUR 3 FFH 80H
0078H          00H 76H
0079H TWO      LALK 0080H 2 DOH 01H ;load address of SIX, enable
007AH          00H 80H ; interrupts, and wait for
007BH          PUSH 1 CEH 1CH ; TINT interrupt
007CH          EINT 1 CEH 00H
007DH FIVE     NOP 1 55H 00H
007EH          B FIVE 3 FFH 80H
007FH          00H 7DH
0080H SIX      IN 001 DAT01 2 81H 01H ;input phase-1 voltage
0081H          BIT 15,DAT01 1 90H 01H
0082H          BBZ SEVEN 2/3 F8H 80H ;if goes positive, place 1 in
0083H          00H 90H ; DAT6C and go to next phase
0084H          ZALS DAT61 1 41H 61H ;decrement DAT61
0085H          SUBS DAT04 1 45H 04H
0086H          SACL 0,DAT61 1 60H 61H
0087H          BZ THREE 2/3 F6H 80H ;if inputs are still negative
0088H          00H 92H ; after 288 inputs goto THREE
0089H          LALK 0080H 2 DOH 01H ;load address of SIX, enable
008AH          00H 80H ; interrupts, and wait for
008BH          PUSH 1 CEH 1CH ; TINT interrupt
008CH          EINT 1 CEH 00H
008DH EIGHT    NOP 1 55H 00H
008EH          B EIGHT 3 FFH 80H
008FH          00H 8DH
0090H SEVEN    LACK 01H 1 CAH 01H ;load 1 in DAT6C if alternating
0091H          SACL 0,DAT6C 1 60H 6CH ; voltage present in phase-1
0092H THREE    IN 003 DAT21 2 83H 21H ;input phase-2 voltage
0093H          BIT 15,DAT21 1 90H 21H
0094H          BBNZ NINE 2/3 F9H 80H ;if negative, jump to NINE
0095H          00H A2H ; to see if goes positive

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0096H		ZALS DAT62	1	41H 62H	;decrement DAT62
0097H		SUBS DAT04	1	45H 04H	
0098H		SACL 0,DAT62	1	60H 62H	
0099H		BZ TEN	2/3	F6H 80H	;if inputs are still positive
009AH				00H BBH	; after 288 inputs, goto TEN
009BH		LALK 0092H	2	DOH 01H	;load address of THREE, enable
009CH				00H 92H	; interrupts, and wait for
009DH		PUSH	1	CEH 1CH	; TINT interrupt
009EH		EINT	1	CEH 00H	
009FH	TEEN1	NOP	1	55H 00H	
00A0H		B TEEN1	3	FFH 80H	
00A1H				00H 9FH	
00A2H	NINE	LALK 00A9H	2	DOH 01H	;load address of TEEN3, enable
00A3H				00H A9H	; interrupts, and wait for
00A4H		PUSH	1	CEH 1CH	; TINT interrupt
00A5H		EINT	1	CEH 00H	
00A6H	TEEN2	NOP	1	55H 00H	
00A7H		B TEEN2	3	FFH 80H	
00A8H				00H A6H	
00A9H	TEEN3	IN 003 DAT21	2	83H 21H	;input phase-2 voltage
00AAH		BIT 15,DAT21	1	90H 21H	
00ABH		BBZ TEEN4	2/3	F8H 80H	;if goes positive, place 1 in
00ACH				00H B9H	; DAT6D and go to next phase
00ADH		ZALS DAT63	1	41H 63H	;decrement DAT63
00AEH		SUBS DAT04	1	45H 04H	
00AFH		SACL 0,DAT63	1	60H 63H	
00B0H		BZ TEN	2/3	F6H 80H	;if inputs are still negative
00B1H				00H BBH	; after 288 inputs, goto TEN
00B2H		LALK 00A9H	2	DOH 01H	;load address of TEEN3, enable
00B3H				00H A9H	; interrupts, and wait for
00B4H		PUSH	1	CEH 1CH	; TINT interrupt
00B5H		EINT	1	CEH 00H	
00B6H	TEEN5	NOP	1	55H 00H	
00B7H		B TEEN5	3	FFH 80H	
00B8H				00H B6H	
00B9H	TEEN4	LACK 01H	1	CAH 01H	;load 1 in DAT6D if alternating
00BAH		SACL 0,DAT6D	1	60H 6DH	; voltage present in phase-2
00BBH	TEN	IN 005 DAT41	2	85H 41H	;input phase-3 voltage
00BCH		BIT 15,DAT41	1	90H 41H	
00BDH		BBNZ TEEN6	2/3	F9H 80H	;if negative, jump to TEEN6
00BEH				00H CBH	; to see if goes positive
00BFH		ZALS DAT64	1	41H 64H	;decrement DAT64
00C0H		SUBS DAT04	1	45H 04H	
00C1H		SACL 0,DAT64	1	60H 64H	
00C2H		BZ TEEN7	2/3	F6H 80H	;if inputs are still positive
00C3H				00H E4H	; after 288 inputs, goto TEEN7
00C4H		LALK 00BBH	2	DOH 01H	;load address of TEN, enable
00C5H				00H BBH	; interrupts, and wait for
00C6H		PUSH	1	CEH 1CH	; TINT interrupt
00C7H		EINT	1	CEH 00H	
00C8H	TEEN8	NOP	1	55H 00H	
00C9H		B TEEN8	3	FFH 80H	

00CAH				00H C8H	
00CBH	TEEN6	LALK 00D2H	2	DOH 01H	;load address of TWENTY, enable
00CCH				00H D2H	; interrupts, and wait for
00CDH		PUSH	1	CEH 1CH	; TINT interrupt
00CEH		EINT	1	CEH 00H	
00CFH	TEEN9	NOP	1	55H 00H	
00DOH		B TEEN9	3	FFH 80H	
00D1H				00H CFH	
00D2H	TWENTY	IN 005 DAT41	2	85H 41H	;input phase-3 voltage
00D3H		BIT 15,DAT41	1	90H 41H	
00D4H		BBZ TWENT1	2/3	F8H 80H	;if goes positive, place 1 in
00D5H				00H E2H	; DAT6E and go to next phase
00D6H		ZALS DAT65	1	41H 65H	;decrement DAT65
00D7H		SUBS DAT04	1	45H 04H	
00D8H		SACL 0,DAT65	1	60H 65H	
00D9H		BZ TEEN7	2/3	F6H 80H	;if inputs are still positive
00DAH				00H E4H	; after 288 inputs, goto TEEN7
00DBH		LALK 00D2H	2	DOH 01H	;load address of TWENTY, enable
00DCH				00H D2H	; interrupts, and wait for
00DDH		PUSH	1	CEH 1CH	; TINT interrupt
00DEH		EINT	1	CEH 00H	
00DFH	TWENT2	NOP	1	55H 00H	
00E0H		B TWENT2	3	FFH 80H	
00E1H				00H DFH	
00E2H	TWENT1	LACK 01H	1	CAH 01H	;load 1 in DAT6E if alternating
00E3H		SACL 0,DAT6E	1	60H 6EH	; voltage present in phase-3
00E4H	TEEN7	ZALS DAT6C	1	41H 6CH	;jump if non-alternating
00E5H		BZ TWENT3	2/3	F6H 80H	; phase-1 to TWENT3
00E6H				01H 2BH	
00E7H	TWENT4	LALK 00EEH	2	DOH 01H	;load address of TWENT6, enable
00E8H				00H EEH	; interrupts, and wait for
00E9H		PUSH	1	CEH 1CH	; TINT interrupt
00EAH		EINT	1	CEH 00H	
00EBH	TWENT5	NOP	1	55H 00H	
00ECH		B TWENT5	3	FFH 80H	
00EDH				00H EBH	
00EEH	TWENT6	IN 001 DAT01	2	81H 01H	;input phase-1 voltage
00EFH		BIT 15,DAT01	1	90H 01H	;check bit15
00F0H		BBNZ TWENT4	2/3	F9H 80H	;branch to TWENT4 if negative
00F1H				00H E7H	; voltage
00F2H		LALK 00F9H	2	DOH 01H	;load address of TWENT8, enable
00F3H				00H F9H	; interrupts, and wait for
00F4H		PUSH	1	CEH 1CH	; TINT interrupt
00F5H		EINT	1	CEH 00H	
00F6H	TWENT7	NOP	1	55H 00H	
00F7H		B TWENT7	3	FFH 80H	
00F8H				00H F6H	
00F9H	TWENT8	IN 001 DAT01	2	81H 01H	;input phase-1 voltage
00FAH		BIT 15,DAT01	1	90H 01H	;check bit15
00FBH		BBNZ TWENT4	2/3	F9H 80H	;branch to TWENT4 if negative
00FCH				00H E7H	; voltage
00FDH		LALK 0104H	2	DOH 01H	;load address of THIRTY, enable

00FEH			01H 04H	; interrupts, and wait for
00FFH	PUSH	1	CEH 1CH	; TINT interrupt
0100H	EINT	1	CEH 00H	
0101H	TWENT9	1	55H 00H	
0102H	B TWENT9	3	FFH 80H	
0103H			01H 01H	
0104H	THIRTY	2	81H 01H	;input phase-1 voltage
0105H	BIT 15,DAT01	1	90H 01H	;check bit15
0106H	BBNZ TWENT4	2/3	F9H 80H	;branch to TWENT4 if negative
0107H			00H E7H	; voltage
0108H	THIRT1	2	DOH 01H	;load address of THIRT3, enable
0109H			01H 0FH	; interrupts, and wait for
010AH	PUSH	1	CEH 1CH	; TINT interrupt
010BH	EINT	1	CEH 00H	
010CH	THIRT2	1	55H 00H	
010DH	B THIRT2	3	FFH 80H	
010EH			01H 0CH	
010FH	THIRT3	2	81H 01H	;input phase-1 voltage
0110H	BIT 15,DAT01	1	90H 01H	;check bit15
0111H	BBZ THIRT1	2/3	F8H 80H	;branch to THIRT1 if positive
0112H			01H 08H	; voltage
0113H	LALK 011AH	2	DOH 01H	;load address of THIRT5, enable
0114H			01H 1AH	; interrupts, and wait for
0115H	PUSH	1	CEH 1CH	; TINT interrupt
0116H	EINT	1	CEH 00H	
0117H	THIRT4	1	55H 00H	
0118H	B THIRT4	3	FFH 80H	
0119H			01H 17H	
011AH	THIRT5	2	81H 01H	;input phase-1 voltage
011BH	BIT 15,DAT01	1	90H 01H	;check bit15
011CH	BBZ THIRT1	2/3	F8H 80H	;branch to THIRT1 if positive
011DH			01H 08H	; voltage
011EH	LALK 0125H	2	DOH 01H	;load address of THIRT7, enable
011FH			01H 25H	; interrupts, and wait for
0120H	PUSH	1	CEH 1CH	; TINT interrupt
0121H	EINT	1	CEH 00H	
0122H	THIRT6	1	55H 00H	
0123H	B THIRT6	3	FFH 80H	
0124H			01H 22H	
0125H	THIRT7	2	81H 01H	;input phase-1 voltage
0126H	BIT 15,DAT01	1	90H 01H	;check bit15
0127H	BBZ THIRT1	2/3	F8H 80H	;branch to THIRT1 if positive
0128H			01H 08H	; voltage, otherwise to the
0129H	B SIXT7	3	FFH 80H	; start of phase-1
012AH			01H B7H	
012BH	TWENT3	1	41H 6DH	;jump if non-alternating
012CH	BZ THIRT8	2/3	F6H 80H	; phase-2 to THIRT8
012DH			01H 72H	
012EH	THIRT9	2	DOH 01H	;load address of FORT1, enable
012FH			01H 35H	; interrupts, and wait for
0130H	PUSH	1	CEH 1CH	; TINT interrupt
0131H	EINT	1	CEH 00H	

0132H	FORTY	NOP	1	55H 00H	
0133H		B FORTY	3	FFH 80H	
0134H				01H 32H	
0135H	FORT1	IN 003 DAT21	2	83H 21H	;input phase-2 voltage
0136H		BIT 15,DAT21	1	90H 21H	;check bit15
0137H		BBNZ THIRT9	2/3	F9H 80H	;branch to THIRT9 if negative
0138H				01H 2EH	; voltage
0139H		LALK 0140H	2	DOH 01H	;load address of FORT3, enable
013AH				01H 40H	; interrupts, and wait for
013BH		PUSH	1	CEH 1CH	; TINT interrupt
013CH		EINT	1	CEH 00H	
013DH	FORT2	NOP	1	55H 00H	
013EH		B FORT2	3	FFH 80H	
013FH				01H 3DH	
0140H	FORT3	IN 003 DAT21	2	83H 21H	;input phase-2 voltage
0141H		BIT 15,DAT21	1	90H 21H	;check bit15
0142H		BBNZ THIRT9	2/3	F9H 80H	;branch to THIRT9 if negative
0143H				01H 2EH	; voltage
0144H		LALK 014BH	2	DOH 01H	;load address of FORT5, enable
0145H				01H 4BH	; interrupts, and wait for
0146H		PUSH	1	CEH 1CH	; TINT interrupt
0147H		EINT	1	CEH 00H	
0148H	FORT4	NOP	1	55H 00H	
0149H		B FORT4	3	FFH 80H	
014AH				01H 48H	
014BH	FORT5	IN 003 DAT21	2	83H 21H	;input phase-2 voltage
014CH		BIT 15,DAT21	1	90H 21H	;check bit15
014DH		BBNZ THIRT9	2/3	F9H 80H	;branch to THIRT9 if negative
014EH				01H 2EH	; voltage
014FH	FORT6	LALK 0156H	2	DOH 01H	;load address of FORT8, enable
0150H				01H 56H	; interrupts, and wait for
0151H		PUSH	1	CEH 1CH	; TINT interrupt
0152H		EINT	1	CEH 00H	
0153H	FORT7	NOP	1	55H 00H	
0154H		B FORT7	3	FFH 80H	
0155H				01H 53H	
0156H	FORT8	IN 003 DAT21	2	83H 21H	;input phase-2 voltage
0157H		BIT 15,DAT21	1	90H 21H	;check bit15
0158H		BBZ FORT6	2/3	F8H 80H	;branch to FORT6 if positive
0159H				01H 4FH	; voltage
015AH		LALK 0161H	2	DOH 01H	;load address of FIFTY, enable
015BH				01H 61H	; interrupts, and wait for
015CH		PUSH	1	CEH 1CH	; TINT interrupt
015DH		EINT	1	CEH 00H	
015EH	FORT9	NOP	1	55H 00H	
015FH		B FORT9	3	FFH 80H	
0160H				01H 5EH	
0161H	FIFTY	IN 003 DAT21	2	83H 21H	;input phase-2 voltage
0162H		BIT 15,DAT21	1	90H 21H	;check bit15
0163H		BBZ FORT6	2/3	F8H 80H	;branch to FORT6 if positive
0164H				01H 4FH	; voltage
0165H		LALK 016CH	2	DOH 01H	;load address of FIFT2, enable

0166H			01H 6CH	; interrupts, and wait for
0167H		PUSH	1 CEH 1CH	; TINT interrupt
0168H		EINT	1 CEH 00H	
0169H	FIFT1	NOP	1 55H 00H	
016AH		B FIFT1	3 FFH 80H	
016BH			01H 69H	
016CH	FIFT2	IN 003 DAT21	2 83H 21H	;input phase-2 voltage
016DH		BIT 15,DAT21	1 90H 21H	;check bit15
016EH		BBZ FORT6	2/3 F8H 80H	;branch to FORT6 if positive
016FH			01H 4FH	; voltage, otherwise to the
0170H		B SIXT7	3 FFH 80H	; start of phase-1
0171H			01H B7H	
0172H	THIRT8	ZALS DAT6E	1 41H 6EH	;jump if non-alternating
0173H		BZ SIXT7	2/3 F6H 80H	; phase-3 to start of phase-1
0174H			01H B7H	
0175H	FIFT3	LALK 017CH	2 DOH 01H	;load address of FIFT5, enable
0176H			01H 7CH	; interrupts, and wait for
0177H		PUSH	1 CEH 1CH	; TINT interrupt
0178H		EINT	1 CEH 00H	
0179H	FIFT4	NOP	1 55H 00H	
017AH		B FIFT4	3 FFH 80H	
017BH			01H 79H	
017CH	FIFT5	IN 005 DAT41	2 85H 41H	;input phase-3 voltage
017DH		BIT 15,DAT41	1 90H 41H	;check bit15
017EH		BBNZ FIFT3	2/3 F9H 80H	;branch to FIFT3 if negative
017FH			01H 75H	; voltage
0180H		LALK 0187H	2 DOH 01H	;load address of FIFT7, enable
0181H			01H 87H	; interrupts, and wait for
0182H		PUSH	1 CEH 1CH	; TINT interrupt
0183H		EINT	1 CEH 00H	
0184H	FIFT6	NOP	1 55H 00H	
0185H		B FIFT6	3 FFH 80H	
0186H			01H 84H	
0187H	FIFT7	IN 005 DAT41	2 85H 41H	;input phase-3 voltage
0188H		BIT 15,DAT41	1 90H 41H	;check bit15
0189H		BBNZ FIFT3	2/3 F9H 80H	;branch to FIFT3 if negative
018AH			01H 75H	; voltage
018BH		LALK 0192H	2 DOH 01H	;load address of FIFT9, enable
018CH			01H 92H	; interrupts, and wait for
018DH		PUSH	1 CEH 1CH	; TINT interrupt
018EH		EINT	1 CEH 00H	
018FH	FIFT8	NOP	1 55H 00H	
0190H		B FIFT8	3 FFH 80H	
0191H			01H 8FH	
0192H	FIFT9	IN 005 DAT41	2 85H 41H	;input phase-3 voltage
0193H		BIT 15,DAT41	1 90H 41H	;check bit15
0194H		BBNZ FIFT3	2/3 F9H 80H	;branch to FIFT3 if negative
0195H			01H 75H	; voltage
0196H	SIXTY	LALK 019DH	2 DOH 01H	;load address of SIXT2, enable
0197H			01H 9DH	; interrupts, and wait for
0198H		PUSH	1 CEH 1CH	; TINT interrupt
0199H		EINT	1 CEH 00H	

019AH	SIXT1	NOP	1	55H 00H	
019BH		B SIXT1	3	FFH 80H	
019CH				01H 9AH	
019DH	SIXT2	IN 005 DAT41	2	85H 41H	;input phase-3 voltage
019EH		BIT 15,DAT41	1	90H 41H	;check bit15
019FH		BBZ SIXTY	2/3	F8H 80H	;branch to SIXTY if positive
01A0H				01H 96H	; voltage
01A1H		LALK 01A8H	2	DOH 01H	;load address of SIXT4, enable
01A2H				01H A8H	; interrupts, and wait for
01A3H		PUSH	1	CEH 1CH	; TINT interrupt
01A4H		EINT	1	CEH 00H	
01A5H	SIXT3	NOP	1	55H 00H	
01A6H		B SIXT3	3	FFH 80H	
01A7H				01H A5H	
01A8H	SIXT4	IN 005 DAT41	2	85H 41H	;input phase-3 voltage
01A9H		BIT 15,DAT41	1	90H 41H	;check bit15
01AAH		BBZ SIXTY	2/3	F8H 80H	;branch to SIXTY if positive
01ABH				01H 96H	; voltage
01ACH		LALK 01B3H	2	DOH 01H	;load address of SIXT6, enable
01ADH				01H B3H	; interrupts, and wait for
01AEH		PUSH	1	CEH 1CH	; TINT interrupt
01AFH		EINT	1	CEH 00H	
01B0H	SIXT5	NOP	1	55H 00H	
01B1H		B SIXT5	3	FFH 80H	
01B2H				01H B0H	
01B3H	SIXT6	IN 005 DAT41	2	85H 41H	;input phase-3 voltage
01B4H		BIT 15,DAT41	1	90H 41H	;check bit15
01B5H		BBZ SIXTY	2/3	F8H 80H	;branch to SIXTY if positive
01B6H				01H 96H	; voltage
01B7H	SIXT7	LDPK 00	1	C8H 00H	;load PRD register with 216
01B8H		LACK 0D8H	1	CAH D8H	
01B9H		SACL 0,DAT03	1	60H 03H	
01BAH		LDPK 04	1	C8H 04H	

PHASE 1

01BBH	START1	BIOZ SYNCH	2/3	FAH 80H	;jump to SYNCH routine if BIO
01BCH				04H 57H	; pin is zero
01BDH		ZALS DAT00	1	41H 00H	;increment count of number of
01BEH		ADDS DAT04	1	49H 04H	; samples
01BFH		SACL 0,DAT00	1	60H 00H	
01C0H		IN 001 DAT01	2	81H 01H	;input phase-1 voltage
01C1H		IN 002 DAT02	2	82H 02H	;input phase-1 current
01C2H		LT DAT01	1	3CH 01H	;multiply phase-1 voltage by
01C3H		MPY DAT02	1	38H 02H	; phase-1 current
01C4H		SPH DAT0D	1	7DH 0DH	
01C5H		SPL DAT0C	1	7CH 0CH	
01C6H		ZAC	1	CAH 00H	;sign-extend the upper word of
01C7H		SACL 0,DAT0E	1	60H 0EH	; the product to a third word
01C8H		BIT 15,DAT0D	1	90H 0DH	
01C9H		BBZ ONE1	2/3	F8H 80H	
01CAH				01H CEH	

01CBH	LALK OFFFFH	2	DOH 01H	
01CCH			FFH FFH	
01CDH	SACL 0,DAT0E	1	60H 0EH	
01CEH	ONE1 ZALS DAT0C	1	41H 0CH	;add the three-word product to
01CFH	ADDS DAT0F	1	49H 0FH	; the three-word accumulated
01DOH	SACL 0,DAT0F	1	60H 0FH	; phase-1 V.I total
01D1H	SACH 0,DAT6F	1	68H 6FH	
01D2H	ZALS DAT6F	1	41H 6FH	
01D3H	ADDS DAT0D	1	49H 0DH	
01D4H	ADDS DAT10	1	49H 10H	;the running total is at
01D5H	SACL 0,DAT10	1	60H 10H	; addresses 0FH, 10H, and
01D6H	SACH 0,DAT6F	1	68H 6FH	; 11H (MSW)
01D7H	ZALS DAT6F	1	41H 6FH	
01D8H	ADDS DAT0E	1	49H 0EH	
01D9H	ADDS DAT11	1	49H 11H	
01DAH	SACL 0,DAT11	1	60H 11H	
01DBH	SQRA DAT01	1	39H 01H	;square phase-1 voltage
01DCH	SPH DAT13	1	7DH 13H	
01DDH	SPL DAT12	1	7CH 12H	
01DEH	ZALS DAT12	1	41H 12H	;add the two-word product to
01DFH	ADDS DAT15	1	49H 15H	; the three-word accumulated
01EOH	SACL 0,DAT15	1	60H 15H	; phase-1 V.V total
01E1H	SACH 0,DAT6F	1	68H 6FH	
01F2H	ZALS DAT6F	1	41H 6FH	
01E3H	ADDS DAT13	1	49H 13H	
01E4H	ADDS DAT16	1	49H 16H	;the running total is at
01E5H	SACL 0,DAT16	1	60H 16H	; addresses 15H, 16H, and
01E6H	SACH 0,DAT6F	1	68H 6FH	; 17H (MSW)
01E7H	ZALS DAT6F	1	41H 6FH	
01E8H	ADDS DAT17	1	49H 17H	
01E9H	SACL 0,DAT17	1	60H 17H	
01EAH	SQRA DAT02	1	39H 02H	;square phase-1 current
01EBH	SPH DAT19	1	7DH 19H	
01ECH	SPL DAT18	1	7CH 18H	
01EDH	ZALS DAT18	1	41H 18H	;add the two-word product to
01EEH	ADDS DAT1B	1	49H 1BH	; the three-word accumulated
01EFH	SACL 0,DAT1B	1	60H 1BH	; phase-2 I.I total
01FOH	SACH 0,DAT6F	1	68H 6FH	
01F1H	ZALS DAT6F	1	41H 6FH	
01F2H	ADDS DAT19	1	49H 19H	
01F3H	ADDS DAT1C	1	49H 1CH	;the running total is at
01F4H	SACL 0,DAT1C	1	60H 1CH	; addresses 1BH, 1CH, and
01F5H	SACH 0,DAT6F	1	68H 6FH	; 1DH (MSW)
01F6H	ZALS DAT6F	1	41H 6FH	
01F7H	ADDS DAT1D	1	49H 1DH	
01F8H	SACL 0,DAT1D	1	60H 1DH	
01F9H	ZALS DAT6C	1	41H 6CH	;branch to TWO1 if alternating
01FAH	BNZ TWO1	2/3	F5H 80H	; voltage in phase-1
01FBH			02H 08H	
01FCH	ZALS DAT66	1	41H 66H	;decrement DAT66
01FDH	SUBS DAT04	1	45H 04H	
01FEH	SACL 0,DAT66	1	60H 66H	

01FFH	BZ WRITE1	2/3	F6H 80H	;branch to write routine after
0200H			02H 45H	; non-alternating cycles
0201H	LALK (phase 2)	2	DOH 01H	;load phase-2 starting address
0202H			02H 9BH	; into accumulator, push
0203H	PUSH	1	CEH 1CH	; accumulator onto stack,
0204H	EINT	1	CEH 00H	; enable interrupts, and wait
0205H	THREE1 NOP	1	55H 00H	; for T1NT interrupt
0206H	B THREE1	3	FFH 80H	
0207H			02H 05H	
0208H	TWO1 ZALH DAT06	1	40H 06H	;skip 240 samples
0209H	SUBH 0,DAT04	1	44H 04H	
020AH	SACH 0,DAT06	1	68H 06H	
020BH	BGZ FOUR1	2/3	F1H 80H	
020CH			02H 1EH	
020DH	BIT 15,DAT01	1	90H 01H	;branch if sampled voltage
020EH	BBNZ FIVE1	2/3	F9H 80H	; is negative
020FH			02H 1CH	
0210H	BIT 15,DAT03	1	90H 03H	;branch if previous sampled
0211H	BBZ FIVE1	2/3	F8H 80H	; voltage is positive
0212H			02H 1CH	
0213H	LACK FOH	1	CAH FOH	;load 240 in DAT06 for skipping
0214H	SACL 0,DAT06	1	60H 06H	; next 240 samples
0215H	ZALS DAT07	1	41H 07H	;check if this is 117th. cycle
0216H	SUBS DAT04	1	45H 04H	
0217H	SACL 0,DAT07	1	60H 07H	
0218H	BGZ FOUR1	2/3	F1H 80H	
0219H			02H 1EH	
021AH	B WR 'E1	3	FFH 80H	;branch to write routine if
021BH			02H 45H	; this is 117th. cycle
021CH	FIVE1 ZALS DAT01	1	41H 01H	;store present V reading in
021DH	SACL 0,DAT03	1	60H 03H	; DAT03 for next run
021EH	FOUR1 BIT 15,DAT01	1	90H 01H	;determine phase-1 peak V
021FH	BBNZ SIX1	2/3	F9H 80H	; value and position
0220H			02H 29H	
0221H	ZALS DAT01	1	41H 01H	
0222H	SUBS 0,DAT08	1	45H 08H	
0223H	BLEZ SIX1	2/3	F2H 80H	
0224H			02H 29H	
0225H	ZALS DAT01	1	41H 01H	
0226H	SACL 0,DAT08	1	60H 08H	;phase-1 peak V value
0227H	ZALS DAT00	1	41H 00H	
0228H	SACL 0,DAT09	1	60H 09H	;phase-1 peak V position
0229H	SIX1 BIT 15,DAT02	1	90H 02H	;determine phase-1 peak I
022AH	BBNZ SEVEN1	2/3	F9H 80H	; value and position
022BH			02H 34H	
022CH	ZALS DAT02	1	41H 02H	
022DH	SUBS 0,DAT0A	1	45H 0AH	
022EH	BLEZ SEVEN1	2/3	F2H 80H	
022FH			02H 34H	
0230H	ZALS DAT02	1	41H 02H	
0231H	SACL 0,DAT0A	1	60H 0AH	;phase-1 peak I value
0232H	ZALS DAT00	1	41H 00H	

0233H		SACL 0,DAT0B	1	60H 0BH	;phase-1 peak I position
0234H	SEVEN1	ZALS DAT07	1	41H 07H	;if 115th cycle, zero peak
0235H		SUBS 0,DAT04	1	45H 04H	; voltage and current
0236H		SUBS 0,DAT04	1	45H 04H	; counters
0237H		BNZ EIGHT1	2/3	F5H 80H	
0238H				02H 3EH	
0239H		ZAC	1	CAH 00H	
023AH		SACL 0,DAT08	1	60H 08H	
023BH		SACL 0,DAT09	1	60H 09H	
023CH		SACL 0,DAT0A	1	60H 0AH	
023DH		SACL 0,DAT0B	1	60H 0BH	
023EH	EIGHT1	LALK (phase 2)	2	DOH 01H	;load phase 2 starting address
023FH				02H 9BH	; into accumulator, push
0240H		PUSH	1	CEH 1CH	; accumulator onto stack,
0241H		EINT	1	CEH 00H	; enable interrupts, and wait
0242H	NINE1	NOP	1	55H 00H	; for TINT interrupt
0243H		B NINE1	3	FFH 80H	
0244H				02H 42H	
0245H	WRITE1	BIT 15,DAT11	1	90H 11H	;determine if the sum of V.I
0246H		BBZ WRITE2	2/3	F8H 80H	; is negative, and if so,
0247H				02H 56H	; transform it into the two's
0248H		ZALS DAT11	1	41H 11H	; complement
0249H		XOR DAT1F	1	4CH 1FH	
024AH		SACL 0,DAT11	1	60H 11H	
024BH		ZALS DAT0F	1	41H 0FH	
024CH		ADDH DAT10	1	48H 10H	
024DH		CMPL	1	CEH 27H	
024EH		ADDS DAT04	1	49H 04H	
024FH		SACL 0,DAT0F	1	60H 0FH	
0250H		SACH 0,DAT10	1	68H 10H	
0251H		ZAC	1	CAH 00H	
0252H		ADDC DAT11	1	43H 11H	
0253H		SACL 0,DAT11	1	60H 11H	
0254H		ZALS DAT04	1	41H 04H	
0255H		SACL 0,DAT1E	1	60H 1EH	
0256H	WRITE2	LACK 00H	1	CAH 00H	;write the number of samples
0257H		TBLW DAT00	3	59H 00H	; in phase-1 over 117 cycles
0258H		LACK 01H	1	CAH 01H	;write the sample number of the
0259H		TBLW DAT08	3	59H 08H	; peak V value in cycle 116
025AH		LACK 02H	1	CAH 02H	;write the phase-1 peak V value
025BH		TBLW DAT09	3	59H 09H	
025CH		LACK 03H	1	CAH 03H	;write the sample number of the
025DH		TBLW DAT0A	3	59H 0AH	; peak I value in cycle 116
025EH		LACK 04H	1	CAH 04H	;write the phase-1 peak I value
025FH		TBLW DAT0B	3	59H 0BH	
0260H		LACK 05H	1	CAH 05H	;write the three-word phase-1
0261H		TBLW DAT0F	3	59H 0FH	; V.I total
0262H		LACK 06H	1	CAH 06H	
0263H		TBLW DAT10	3	59H 10H	
0264H		LACK 07H	1	CAH 07H	
0265H		TBLW DAT11	3	59H 11H	

0266H	LACK 08H	1	CAH 08H	;write the three-word phase-1
0267H	TBLW DAT15	3	59H 15H	; V.V total
0268H	LACK 09H	1	CAH 09H	
0269H	TBLW DAT16	3	59H 16H	
026AH	LACK 0AH	1	CAH 0AH	
026BH	TBLW DAT17	3	59H 17H	
026CH	LACK 0BH	1	CAH 0BH	;write the three-word phase-1
026DH	TBLW DAT1B	3	59H 1BH	; I.I total
026EH	LACK 0CH	1	CAH 0CH	
026FH	TELW DAT1C	3	59H 1CH	
0270H	LACK 0DH	1	CAH 0DH	
0271H	TBLW DAT1D	3	59H 1DH	
0272H	LACK 0EH	1	CAH 0EH	;write 01 to common memory if
0273H	TBLW DAT1E	3	59H 1EH	; the sum of V.I is negative
0274H	ZALS DAT05	1	41H 05H	;decrement DAT05, and check if
0275H	SUBS DAT04	1	45H 04H	equal to zero
0276H	SACL 0,DAT05	1	60H 05H	
0277H	BNZ WRITE3	2/3	F5H 80H	
0278H			02H 7CH	
0279H	RXF	1	CEH 0CH	;reset XF output pin
027AH	LACK 03H	1	CAH 03H	;load 3 in DAT05
027BH	SACL 0,DAT05	1	60H 05H	
027CH	WRITE3 ZALS DAT00	1	41H 00H	;transfer contents of DAT00 to
027DH	SACL DAT69	1	60H 69H	; DAT69
027EH	ZAC	1	CAH 00H	;zero the data memory addresses
027FH	SACL 0,DAT00	1	60H 00H	; used in gathering data
0280H	SACL 0,DAT03	1	60H 03H	
0281H	SACL 0,DAT08	1	60H 08H	
0282H	SACL 0,DAT09	1	60H 09H	
0283H	SACL 0,DAT0A	1	60H 0AH	
0284H	SACL 0,DAT0B	1	60H 0BH	
0285H	SACL 0,DAT0F	1	60H 0FH	
0286H	SACL 0,DAT10	1	60H 10H	
0287H	SACL 0,DAT11	1	60H 11H	
0288H	SACL 0,DAT15	1	60H 15H	
0289H	SACL 0,DAT16	1	60H 16H	
028AH	SACL 0,DAT17	1	60H 17H	
028BH	SACL 0,DAT1B	1	60H 1BH	
028CH	SACL 0,DAT1C	1	60H 1CH	
028DH	SACL 0,DAT1D	1	60H 1DH	
028EH	SACL 0,DAT1E	1	60H 1EH	
028FH	LACK 75H	1	CAH 75H	;write 117 to DAT07
0290H	SACL 0,DAT07	1	60H 07H	
0291H	ZALS DAT6A	1	41H 6AH	;use phase-2 frequency for next
0292H	SACL 0,DAT66	1	60H 66H	; phase-1 non-alternating pass
0293H	LALK (phase 2)	2	40H 01H	;load phase-2 starting address
0294H			02H 9BH	; into accumulator, push
0295H	PUSH	1	CEH 1CH	; accumulator onto stack, set
0296H	SXF	1	CEH 0DH	; XF output pin, enable
0297H	EINT	1	CEH 00H	; interrupts, and wait for
0298H	WRITE4 NOP	1	55H 00H	; TINT interrupt
0299H	B WRITE4	3	FFH 80H	

029AH

02H 98H

PHASE 2

029BH	START2	ZALS DAT20	1	41H 20H	;increment count of number of
029CH		ADDS DAT04	1	49H 04H	; samples
029DH		SACL 0,DAT20	1	60H 20H	
029EH		IN 003 DAT21	2	83H 21H	;input phase-2 voltage
029FH		IN 004 DAT22	2	84H 22H	;input phase-2 current
02A0H		LT DAT21	1	3CH 21H	;multiply phase-2 voltage by
02A1H		MPY DAT22	1	38H 22H	; phase-2 current
02A2H		SPH DAT2D	1	7DH 2DH	
02A3H		SPL DAT2C	1	7CH 2CH	
02A4H		ZAC	1	CAH 00H	;sign-extend the upper word of
02A5H		SACL 0,DAT2E	1	60H 2EH	; the product to a third word
02A6H		BIT 15,DAT2D	1	90H 2DH	
02A7H		BBZ ONE2	2/3	F8H 80H	
02A8H				02H ACH	
02A9H		LALK OFFFFH	2	DOH 01H	
02AAH				FFH FFH	
02ABH		SACL 0,DAT2E	1	60H 2EH	
02ACH	ONE2	ZALS DAT2C	1	41H 2CH	;add the three-word product to
02ADH		ADDS DAT2F	1	49H 2FH	; the three-word accumulated
02AEH		SACL 0,DAT2F	1	60H 2FH	; phase-2 V.I total
02AFH		SACH 0,DAT6F	1	68H 6FH	
02B0H		ZALS DAT6F	1	41H 6FH	
02B1H		ADDS DAT2D	1	49H 2DH	
02B2H		ADDS DAT30	1	49H 30H	;the running total is at
02B3H		SACL 0,DAT30	1	60H 30H	; addresses 2FH, 30H, and
02B4H		SACH 0,DAT6F	1	68H 6FH	; 31H (MSW)
02B5H		ZALS DAT6F	1	41H 6FH	
02B6H		ADDS DAT2E	1	49H 2EH	
02B7H		ADDS DAT31	1	49H 31H	
02B8H		SACL 0,DAT31	1	60H 31H	
02B9H		SQRA DAT21	1	39H 21H	;square phase-2 voltage
02BAH		SPH DAT33	1	7DH 33H	
02BBH		SPL DAT32	1	7CH 32H	
02BCH		ZALS DAT32	1	41H 32H	;add the three-word product to
02BDH		ADDS DAT35	1	49H 35H	; the three-word accumulated
02BEH		SACL 0,DAT35	1	60H 35H	; phase-2 V.V total
02BFH		SACH 0,DAT6F	1	68H 6FH	
02COH		ZALS DAT6F	1	41H 6FH	
02C1H		ADDS DAT33	1	49H 33H	
02C2H		ADDS DAT36	1	49H 36H	;the running total is at
02C3H		SACL 0,DAT36	1	60H 36H	; addresses 35H, 36H, and
02C4H		SACH 0,DAT6F	1	68H 6FH	; 37H (MSW)
02C5H		ZALS DAT6F	1	41H 6FH	
02C6H		ADDS DAT37	1	49H 37H	
02C7H		SACL 0,DAT37	1	60H 37H	
02C8H		SQRA DAT22	1	39H 22H	;square phase-2 current
02C9H		SPH DAT39	1	7DH 39H	
02CAH		SPL DAT38	1	7CH 38H	

02CBH		ZALS DAT38	1	41H 38H	;add the three-word product to
02CCH		ADDS DAT3B	1	49H 3BH	; the three-word accumulated
02CDH		SACL O,DAT3B	1	60H 3BH	; phase-2 I.I total
02CEH		SACH O,DAT6F	1	68H 6FH	
02CFH		ZALS DAT6F	1	41H 6FH	
02D0H		ADDS DAT39	1	49H 39H	
02D1H		ADDS DAT3C	1	49H 3CH	;the running total is at
02D2H		SACL O,DAT3C	1	60H 3CH	; addresses 3BH, 3CH, and
02D3H		SACH O,DAT6F	1	68H 6FH	; 3DH (MSW)
02D4H		ZALS DAT6F	1	41H 6FH	
02D5H		ADDS DAT3D	1	49H 3DH	
02D6H		SACL O,DAT3D	1	60H 3DH	
02D7H		ZALS DAT6D	1	41H 6DH	;branch to TWO2 if alternating
02D8H		BNZ TWO2	2/3	F5H 80H	; voltage in phase-2
02D9H				02H E6H	
02DAH		ZALS DAT67	1	41H 67H	;decrement DAT67
02DBH		SUBS DAT04	1	45H 04H	
02DCH		SACL O,DAT67	1	60H 67H	
02DDH		BZ WRITE5	2/3	F6H 80H	;branch to write routine after
02DEH				03H 23H	; non-alternating cycles
02DFH		LALK (phase 3)	2	D0H 01H	;load phase-3 starting address
02EOH				03H 79H	; into accumulator, push
02E1H		PUSH	1	CEH 1CH	; accumulator onto stack,
02E2H		EINT	1	CEH 00H	; enable interrupts, and wait
02E3H	THREE2	NOP	1	55H 00H	; for TINT interrupt
02E4H		B THREE2	3	FFH 80H	
02E5H				02H E3H	
02E6H	TWO2	ZALH DAT26	1	40H 26H	;skip 240 samples
02E7H		SUBH O,DAT04	1	44H 04H	
02E8H		SACH O,DAT26	1	68H 26H	
02E9H		BGZ FOUR2	2/3	F1H 80H	
02EAH				02H FCH	
02EBH		BIT 15,DAT21	1	90H 21H	;branch if sampled voltage
02ECH		BBNZ FIVE2	2/3	F9H 80H	; is negative
02EDH				02H FAH	
02EEH		BIT 15,DAT23	1	90H 23H	;branch if previous sampled
02EFH		BBZ FIVE2	2/3	F8H 80H	; voltage is positive
02FOH				02H FAH	
02F1H		LACK FOH	1	CAH FOH	;load 240 in DAT26 for skipping
02F2H		SACL O,DAT26	1	60H 26H	; next 240 samples
02F3H		ZALS DAT27	1	41H 27H	;check if this is 117th. cycle
02F4H		SUBS DAT04	1	45H 04H	
02F5H		SACL O,DAT27	1	60H 27H	
02F6H		BGZ FOUR2	2/3	F1H 80H	
02F7H				02H FCH	
02F8H		B WRITE5	3	FFH 80H	;branch to write routine if
02F9H				03H 23H	; this is 117th. cycle
02FAH	FIVE2	ZALS DAT21	1	41H 21H	;store present V reading in
02FBH		SACL O,DAT23	1	60H 23H	; DAT23 for next run
02FCH	FOUR2	BIT 15,DAT21	1	90H 21H	;determine phase-2 peak V
02FDH		BBNZ SIX2	2/3	F9H 80H	; value and position
02FEH				03H 07H	

02FFH		ZALS DAT21	1	41H 21H	
0300H		SUBS 0,DAT28	1	45H 28H	
0301H		BLEZ SIX2	2/3	F2H 80H	
0302H				03H 07H	
0303H		ZALS DAT21	1	41H 21H	
0304H		SACL 0,DAT28	1	60H 28H	;phase-2 peak V value
0305H		ZALS DAT20	1	41H 20H	
0306H		SACL 0,DAT29	1	60H 29H	;phase-2 peak V position
0307H	SIX2	BIT 15, DAT22	1	90H 22H	;determine phase-2 peak I
0308H		BBNZ SEVEN2	2/3	F9H 80H	; value and position
0309H				03H 12H	
030AH		ZALS DAT22	1	41H 22H	
030BH		SUBS 0,DAT2A	1	45H 2AH	
030CH		BLEZ SEVEN2	2/3	F2H 80H	
030DH				03H 12H	
030EH		ZALS DAT22	1	41H 22H	
030FH		SACL 0,DAT2A	1	60H 2AH	;phase-2 peak I value
0310H		ZALS DAT20	1	41H 20H	
0311H		SACL 0,DAT2B	1	60H 2BH	;phase-2 peak I position
0312H	SEVEN2	ZALS DAT27	1	41H 27H	;if 115th cycle, zero peak
0313H		SUBS 0,DAT04	1	45H 04H	; voltage and current
0314H		SUBS 0,DAT04	1	45H 04H	; counters
0315H		BNZ EIGHT2	2/3	F5H 80H	
0316H				03H 1CH	
0317H		ZAC	1	CAH 00H	
0318H		SACL 0,DAT28	1	60H 28H	
0319H		SACL 0,DAT29	1	60H 29H	
031AH		SACL 0,DAT2A	1	60H 2AH	
031BH		SACL 0,DAT2B	1	60H 2BH	
031CH	EIGHT2	LALK (phase 3)	2	DOH 01H	;load phase 3 starting address
031DH				03H 79H	; into accumulator, push
031EH		PUSH	1	CEH 1CH	; accumulator onto stack,
031FH		EINT	1	CEH 00H	; enable interrupts, and wait
0320H	NINE2	NOP	1	55H 00H	; for TINT interrupt
0321H		B NINE2	3	FFH 80H	
0322H				03H 20H	
0323H	WRITE5	BIT 15,DAT31	1	90H 31H	;determine if the sum of V.I
0324H		BBZ WRITE6	2/3	F8H 80H	; is negative, and if so,
0325H				03H 34H	; transform it into the two's
0326H		ZALS DAT31	1	41H 31H	; complement
0327H		XOR DAT1F	1	4CH 1FH	
0328H		SACL 0,DAT31	1	60H 31H	
0329H		ZALS DAT2F	1	41H 2FH	
032AH		ADDD DAT30	1	48H 30H	
032BH		CMPL	1	CEH 27H	
032CH		ADDS DAT04	1	49H 04H	
032DH		SACL 0,DAT2F	1	60H 2FH	
032EH		SACH 0,DAT30	1	68H 30H	
032FH		ZAC	1	CAH 00H	
0330H		ADDC DAT31	1	43H 31H	
0331H		SACL 0,DAT31	1	60H 31H	

0332H	ZALS DAT04	1	41H 04H	
0333H	SACL 0,DAT3E	1	60H 3EH	
0334H	WRITE6 LACK 10H	1	CAH 10H	;write the number of samples
0335H	TBLW DAT20	3	59H 20H	; in phase-2 over 117 cycles
0336H	LACK 11H	1	CAH 11H	;write the sample number of the
0337H	TBLW DAT28	3	59H 28H	; peak V value in cycle 116
0338H	LACK 12H	1	CAH 12H	;write the phase-2 peak V value
0339H	TBLW DAT29	3	59H 29H	
033AH	LACK 13H	1	CAH 13H	;write the sample number of the
033BH	TBLW DAT2A	3	59H 2AH	; peak I value in cycle 116
033CH	LACK 14H	1	CAH 14H	;write the phase-2 peak I value
033DH	TBLW DAT2B	3	59H 2BH	
033EH	LACK 15H	1	CAH 15H	;write the three-word phase-2
033FH	TBLW DAT2F	3	59H 2FH	; V.I total
0340H	LACK 16H	1	CAH 16H	
0341H	TBLW DAT30	3	59H 30H	
0342H	LACK 17H	1	CAH 17H	
0343H	TBLW DAT31	3	59H 31H	
0344H	LACK 18H	1	CAH 18H	;write the three-word phase-2
0345H	TBLW DAT35	3	59H 35H	; V.V total
0346H	LACK 19H	1	CAH 19H	
0347H	TBLW DAT36	3	59H 36H	
0348H	LACK 1AH	1	CAH 1AH	
0349H	TBLW DAT37	3	59H 37H	
034AH	LACK 1BH	1	CAH 1BH	;write the three-word phase-2
034BH	TBLW DAT3B	3	59H 3BH	; I.I total
034CH	LACK 1CH	1	CAH 1CH	
034DH	TBLW DAT3C	3	59H 3CH	
034EH	LACK 1DH	1	CAH 1DH	
034FH	TBLW DAT3D	3	59H 3DH	
0350H	LACK 1EH	1	CAH 1EH	;write 01 to common memory if
0351H	TBLW DAT3E	3	59H 3EH	; the sum of V.I is negative
0352H	ZALS DAT05	1	41H 05H	;decrement DAT05, and check if
0353H	SUBS DAT04	1	45H 04H	; equal to zero
0354H	SACL 0,DAT05	1	60H 05H	
0355H	BNZ WRITE7	2/3	F5H 80H	
0356H			03H 5AH	
0357H	RXF	1	CEH 0CH	;reset XF output pin
0358H	LACK 03H	1	CAH 03H	;load 3 in DAT05
0359H	SACL 0,DAT05	1	60H 05H	
035AH	WRITE7 ZALS DAT20	1	41H 20H	
035BH	SACL DAT6A	1	60H 6AH	
035CH	ZAC	1	CAH 00H	;zero the data memory addresses
035DH	SACL 0,DAT20	1	60H 20H	; used in obtaining totals
035EH	SACL 0,DAT23	1	60H 23H	
035FH	SACL 0,DAT28	1	60H 28H	
0360H	SACL 0,DAT29	1	60H 29H	
0361H	SACL 0,DAT2A	1	60H 2AH	
0362H	SACL 0,DAT2B	1	60H 2BH	
0363H	SACL 0,DAT2F	1	60H 2FH	
0364H	SACL 0,DAT30	1	60H 30H	
0365H	SACL 0,DAT31	1	60H 31H	

0366H		SACL 0,DAT35	1	60H 35H	
0367H		SACL 0,DAT36	1	60H 36H	
0368H		SACL 0,DAT37	1	60H 37H	
0369H		SACL 0,DAT3B	1	60H 3BH	
036AH		SACL 0,DAT3C	1	60H 3CH	
036BH		SACL 0,DAT3D	1	60H 3DH	
036CH		SACL 0,DAT3E	1	60H 3EH	
036DH		LACK 75H	1	CAH 75H	;write 117 to DAT27
036EH		SACL 0,DAT27	1	60H 27H	
036FH		ZALS DAT6B	1	41H 6BH	;use phase-3 frequency for next
0370H		SACL 0,DAT67	1	60H 67H	; phase-2 non-alternating pass
0371H		LALK (phase 3)	2	DOH 01H	;load phase-3 starting address
0372H				03H 79H	; into accumulator, push
0373H		PUSH	1	CEH 1CH	; accumulator onto stack, set
0374H		SXF	1	CEH 0DH	; XF output pin, enable
0375H		EINT	1	CEH 00H	; interrupts, and wait for
0376H	WRITE8	NOP	1	55H 00H	; TINT interrupt
0377H		B WRITE8	3	FFH 80H	
0378H				03H 76H	

PHASE 3

0379H	START3	ZALS DAT40	1	41H 40H	;increment count of number of
037AH		ADDS DAT04	1	49H 04H	; samples
037BH		SACL 0,DAT40	1	60H 40H	
037CH		IN 005 DAT41	2	85H 41H	;input phase-3 voltage
037DH		IN 006 DAT42	2	86H 42H	;input phase-3 current
037EH		LT DAT41	1	3CH 41H	;multiply phase-3 voltage by
037FH		MPY DAT42	1	38H 42H	; phase-3 current
0380H		SPH DAT4D	1	7DH 4DH	
0381H		SPL DAT4C	1	7CH 4CH	
0382H		ZAC	1	CAH 00H	;sign-extend the upper word of
0383H		SACL 0,DAT4E	1	60H 4EH	; the product to a third word
0384H		BIT 15,DAT4D	1	90H 4DH	
0385H		BBZ ONE3	2/3	F8H 80H	
0386H				03H 8AH	
0387H		LALK OFFFFH	2	DOH 01H	
0388H				FFH FFH	
0389H		SACL 0,DAT4E	1	60H 4EH	
038AH	ONE3	ZALS DAT4C	1	41H 4CH	;add the three-word product to
038BH		ADDS DAT4F	1	49H 4FH	; the three-word accumulated
038CH		SACL 0,DAT4F	1	60H 4FH	; phase-3 V.I total
038DH		SACH 0,DAT6F	1	68H 6FH	
038EH		ZALS DAT6F	1	41H 6FH	
038FH		ADDS DAT4D	1	49H 4DH	
0390H		ADDS DAT50	1	49H 50H	;the running total is at
0391H		SACL 0,DAT50	1	60H 50H	; addresses 4FH, 50H, and
0392H		SACH 0,DAT6F	1	68H 6FH	; 51H (MSW)
0393H		ZALS DAT6F	1	41H 6FH	
0394H		ADDS DAT4E	1	49H 4EH	
0395H		ADDS DAT51	1	49H 51H	
0396H		SACL 0,DAT51	1	60H 51H	

0397H	SQRA DAT41	1	39H 41H	;square phase-3 voltage
0398H	SPH DAT53	1	7DH 53H	
0399H	SPL DAT52	1	7CH 52H	
039AH	ZALS DAT52	1	41H 52H	;add the three-word product to
039BH	ADDS DAT55	1	49H 55H	; the three-word accumulated
039CH	SACL 0,DAT55	1	60H 55H	; phase-3 V.V total
039DH	SACH 0,DAT6F	1	68H 6FH	
039EH	ZALS DAT6F	1	41H 6FH	
039FH	ADDS DAT53	1	49H 53H	
03A0H	ADDS DAT56	1	49H 56H	;the running total is at
03A1H	SACL 0,DAT56	1	60H 56H	; addresses 55H, 56H, and
03A2H	SACH 0,DAT6F	1	68H 6FH	; 57H (MSW)
03A3H	ZALS DAT6F	1	41H 6FH	
03A4H	ADDS DAT57	1	49H 57H	
03A5H	SACL 0,DAT57	1	60H 57H	
03A6H	SQRA DAT42	1	39H 42H	;square phase-3 current
03A7H	SPH DAT59	1	7DH 59H	
03A8H	SPL DAT58	1	7CH 58H	
03A9H	ZALS DAT58	1	41H 58H	;add the three-word product to
03AAH	ADDS DAT5B	1	49H 5BH	; the three-word accumulated
03ABH	SACL 0,DAT5B	1	60H 5BH	; phase-3 I.I total
03ACH	SACH 0,DAT6F	1	68H 6FH	
03ADH	ZALS DAT6F	1	41H 6FH	
03AEH	ADDS DAT59	1	49H 59H	
03AFH	ADDS DAT5C	1	49H 5CH	;the running total is at
03BOH	SACL 0,DAT5C	1	60H 5CH	; addresses 5BH, 5CH, and
03B1H	SACH 0,DAT6F	1	68H 6FH	; 5DH (MSW)
03B2H	ZALS DAT6F	1	41H 6FH	
03B3H	ADDS DAT5D	1	49H 5DH	
03B4H	SACL 0,DAT5D	1	60H 5DH	
03B5H	ZALS DAT6E	1	41H 6EH	;branch to TWO3 if alternating
03B6H	BNZ TWO3	2/3	F5H 80H	; voltage in phase-3
03B7H			03H C4H	
03B8H	ZALS DAT68	1	41H 68H	;decrement DAT68
03B9H	SUBS DAT04	1	45H 04H	
03BAH	SACL 0,DAT68	1	60H 68H	
03BBH	BZ WRITE9	2/3	F6H 80H	;branch to write routine after
03BCH			04H 01H	; non-alternating cycles
03BDH	LALK (phase 1)	2	DOH 01H	;load phase-1 starting address
03BEH			01H BBH	; into accumulator, push
03BFH	PUSH	1	CEH 1CH	; accumulator onto stack,
03COH	EINT	1	CEH 00H	; enable interrupts, and wait
03C1H	THREE3 NOP	1	55H 00H	; for TINT interrupt
03C2H	B THREE3	3	FFH 80H	
03C3H			03H C1H	
03C4H	TWO3 ZALH DAT46	1	40H 46H	;skip 240 samples
03C5H	SUBH 0,DAT04	1	44H 04H	
03C6H	SACH 0,DAT46	1	68H 46H	
03C7H	BGZ FOUR3	2/3	F1H 80H	
03C8H			03H DAH	
03C9H	BIT 15,DAT41	1	90H 41H	;branch if sampled voltage
03CAH	BBNZ FIVE3	2/3	F9H 80H	; is negative

03CBH			03H D8H	
03CCH	BIT 15,DAT43	1	90H 43H	;branch if previous sampled
03CDH	BBZ FIVE3	2/3	F8H 80H	; voltage is positive
03CEH			03H D8H	
03CFH	LACK FOH	1	CAH FOH	;load 240 in DAT46 for skipping
03DOH	SACL 0,DAT46	1	60H 46H	; next 240 samples
03D1H	ZALS DAT47	1	41H 47H	;check if this is 117th. cycle
03D2H	SUBS DAT04	1	45H 04H	
03D3H	SACL 0,DAT47	1	60H 47H	
03D4H	BGZ FOUR3	2/3	F1H 80H	
03D5H			03H DAH	
03D6H	B WRITE9	3	FFH 80H	;branch to write routine if
03D7H			04H 01H	; this is 117th. cycle
03D8H	FIVE3 ZALS DAT41	1	41H 41H	;store present V reading in
03D9H	SACL 0,DAT43	1	60H 43H	; DAT43 for next run
03DAH	FOUR3 BIT 15,DAT41	1	90H 41H	;determine phase-3 peak V
03DBH	BBNZ SIX3	2/3	F9H 80H	; value and position
03DCH			03H E5H	
03DDH	ZALS DAT41	1	41H 41H	
03DEH	SUBS 0,DAT48	1	45H 48H	
03DFH	BLEZ SIX3	2/3	F2H 80H	
03E0H			03H E5H	
03E1H	ZALS DAT41	1	41H 41H	
03E2H	SACL 0,DAT48	1	60H 48H	;phase-3 peak V value
03E3H	ZALS DAT40	1	41H 40H	
03E4H	SACL 0,DAT49	1	60H 49H	;phase-3 peak V position
03E5H	SIX3 BIT 15,DAT42	1	90H 42H	;determine phase-3 peak I
03E6H	BBNZ SEVEN3	2/3	F9H 80H	; value and position
03E7H			03H FOH	
03E8H	ZALS DAT42	1	41H 42H	
03E9H	SUBS 0,DAT4A	1	45H 4AH	
03EAH	BLEZ SEVEN3	2/3	F2H 80H	
03EBH			03H FOH	
03ECH	ZALS DAT42	1	41H 42H	
03EDH	SACL 0,DAT4A	1	60H 4AH	;phase-3 peak I value
03EEH	ZALS DAT40	1	41H 40H	
03EFH	SACL 0,DAT4B	1	60H 4BH	;phase-3 peak I position
03FOH	SEVEN3 ZALS DAT47	1	41H 47H	;if 115th. cycle, zero peak
03F1H	SUBS 0,DAT04	1	45H 04H	; voltage and current
03F2H	SUBS 0,DAT04	1	45H 04H	; counters
03F3H	BNZ EIGHT3	2/3	F5H 80H	
03F4H			03H FAH	
03F5H	ZAC	1	CAH 00H	
03F6H	SACL 0,DAT48	1	60H 48H	
03F7H	SACL 0,DAT49	1	60H 49H	
03F8H	SACL 0,DAT4A	1	60H 4AH	
03F9H	SACL 0,DAT4B	1	60H 4BH	
03FAH	EIGHT3 LALK (phase 1)	2	DOH 01H	;load phase 1 starting address
03FBH			01H BBH	; into accumulator, push
03FCH	PUSH	1	CEH 1CH	; accumulator onto stack,
03FDH	EINT	1	CEH 00H	; enable interrupts, and wait
03FEH	NINE3 NOP	1	55H 00H	; for TINT interrupt

03FFH	B NINE3	3	FFH 80H	
0400H			03H FEH	
0401H	WRITE9	1	90H 51H	;determine if the sum of V.I
0402H	BBZ WRITE10	2/3	F8H 80H	; is negative, and if so,
0403H			04H 12H	; transform it into the two's
0404H	ZALS DAT51	1	41H 51H	; complement
0405H	XOR DAT1F	1	4CH 1FH	
0406H	SACL 0,DAT51	1	60H 51H	
0407H	ZALS DAT4F	1	41H 4FH	
0408H	ADDH DAT50	1	48H 50H	
0409H	CMPL	1	CEH 27H	
040AH	ADDS DAT04	1	49H 04H	
040BH	SACL 0,DAT4F	1	60H 4FH	
040CH	SACH 0,DAT50	1	68H 50H	
040DH	ZAC	1	CAH 00H	
040EH	ADDC DAT51	1	43H 51H	
040FH	SACL 0,DAT51	1	60H 51H	
0410H	ZALS DAT04	1	41H 04H	
0411H	SACL 0,DAT5E	1	60H 5EH	
0412H	WRITE10	1	CAH 20H	;write the number of samples
0413H	TBLW DAT40	3	59H 40H	; in phase-3 over 117 cycles
0414H	LACK 21H	1	CAH 21H	;write the sample number of the
0415H	TBLW DAT48	3	59H 48H	; peak V value in cycle 116
0416H	LACK 22H	1	CAH 22H	;write the phase-3 peak V value
0417H	TBLW DAT49	3	59H 49H	
0418H	LACK 23H	1	CAH 23H	;write the sample number of the
0419H	TBLW DAT4A	3	59H 4AH	; peak I value in cycle 116
041AH	LACK 24H	1	CAH 24H	;write the phase-3 peak I value
041BH	TBLW DAT4B	3	59H 4BH	
041CH	LACK 25H	1	CAH 25H	;write the three-word phase-3
041DH	TBLW DAT4F	3	59H 4FH	; V.I total
041EH	LACK 26H	1	CAH 26H	
041FH	TBLW DAT50	3	59H 50H	
0420H	LACK 27H	1	CAH 27H	
0421H	TBLW DAT51	3	59H 51H	
0422H	LACK 28H	1	CAH 28H	;write the three-word phase-3
0423H	TBLW DAT55	3	59H 55H	V.V total
0424H	LACK 29H	1	CAH 29H	
0425H	TBLW DAT56	3	59H 56H	
0426H	LACK 2AH	1	CAH 2AH	
0427H	TBLW DAT57	3	59H 57H	
0428H	LACK 2BH	1	CAH 2BH	;write the three-word phase-3
0429H	TBLW DAT5B	3	59H 5BH	; I.I total
042AH	LACK 2CH	1	CAH 2CH	
042BH	TBLW DAT5C	3	59H 5CH	
042CH	LACK 2DH	1	CAH 2DH	
042DH	TBLW DAT5D	3	59H 5DH	
042EH	LACK 2EH	1	CAH 2EH	;write 01 to common memory if
042FH	TBLW DAT5E	3	59H 5EH	; the sum of V.I is negative
0430H	ZALS DAT05	1	41H 05H	;decrement DAT05, and check if
0431H	SUBS DAT04	1	45H 04H	; equal to zero

0432H		SACL 0,DAT05	1	60H 05H	
0433H		BNZ WRITE11	2/3	F5H 80H	
0434H				04H 38H	
0435H		RXF	1	CEH 0CH	;reset XF output pin
0436H		LACK 03H	1	CAH 03H	;load 3 in DAT05
0437H		SACL 0,DAT05	1	60H 05H	
0438H	WRITE11	ZALS DAT40	1	41H 40H	
0439H		SACL 0,DAT6B	1	60H 6BH	
043AH		ZAC	1	CAH 00H	;zero the data memory addresses
043BH		SACL 0,DAT40	1	60H 40H	; used in gathering data
043CH		SACL 0,DAT43	1	60H 43H	
043DH		SACL 0,DAT48	1	60H 48H	
043EH		SACL 0,DAT49	1	60H 49H	
043FH		SACL 0,DAT4A	1	60H 4AH	
0440H		SACL 0,DAT4B	1	60H 4BH	
0441H		SACL 0,DAT4F	1	60H 4FH	
0442H		SACL 0,DAT50	1	60H 50H	
0443H		SACL 0,DAT51	1	60H 51H	
0444H		SACL 0,DAT55	1	60H 55H	
0445H		SACL 0,DAT56	1	60H 56H	
0446H		SACL 0,DAT57	1	60H 57H	
0447H		SACL 0,DAT5B	1	60H 5BH	
0448H		SACL 0,DAT5C	1	60H 5CH	
0449H		SACL 0,DAT5D	1	60H 5DH	
044AH		SACL 0,DAT5E	1	60H 5EH	
044BH		LACK 75H	1	CAH 75H	;write 117 to DAT47
044CH		SACL 0,DAT47	1	60H 47H	
044DH		ZALS DAT69	1	41H 69H	;use phase-1 frequency for next
044EH		SACL 0,DAT68	1	60H 68H	; phase-3 non-alternating pass
044FH		LALK (phase 1)	2	00H 01H	;load phase-1 starting address
0450H				01H BBH	; into accumulator, push
0451H		PUSH	1	CEH 1CH	; accumulator onto stack, set
0452H		SXF	1	CEH 0DH	; XF output pin, enable
0453H		EINT	1	CEH 00H	; interrupts, and wait for
0454H	WRITE12	NOP	1	55H 00H	; TINT interrupt
0455H		B WRITE12	3	FFH 80H	
0456H				04H 54H	

SYNCHRONOUSINITIALIZATION

0457H	SYNCH	LDPK 00	1	C8H 00H	;reset TINT interrupt and set
0458H		LACK 00H	1	CAH 00H	; INTO interrupt
0459H		AND DAT04	1	4EH 04H	
045AH		SACL 0,DAT04	1	60H 04H	
045BH		LACK 01H	1	CAH 01H	
045CH		OR DAT04	1	4DH 04H	
045DH		SACL 0,DAT04	1	60H 04H	
045EH		LDPK 04	1	C8H 04H	
045FH		ZAC	1	CAH 00H	;zero the data memory addresses
0460H		SACL 0,DAT00	1	60H 00H	

0461H	SACL 0,DAT0F	1	60H 0FH	
0462H	SACL 0,DAT10	1	60H 10H	
0463H	SACL 0,DAT11	1	60H 11H	
0464H	SACL 0,DAT15	1	60H 15H	
0465H	SACL 0,DAT16	1	60H 16H	
0466H	SACL 0,DAT17	1	60H 17H	
0467H	SACL 0,DAT1B	1	60H 1BH	
0468H	SACL 0,DAT1C	1	60H 1CH	
0469H	SACL 0,DAT1D	1	60H 1DH	
046AH	SACL 0,DAT1E	1	60H 1EH	
046BH	SACL 0,DAT20	1	60H 20H	
046CH	SACL 0,DAT2F	1	60H 2FH	
046DH	SACL 0,DAT30	1	60H 30H	
046EH	SACL 0,DAT31	1	60H 31H	
046FH	SACL 0,DAT35	1	60H 35H	
0470H	SACL 0,DAT36	1	60H 36H	
0471H	SACL 0,DAT37	1	60H 37H	
0472H	SACL 0,DAT3B	1	60H 3BH	
0473H	SACL 0,DAT3C	1	60H 3CH	
0474H	SACL 0,DAT3D	1	60H 3DH	
0475H	SACL 0,DAT3E	1	60H 3EH	
0476H	SACL 0,DAT40	1	60H 40H	
0477H	SACL 0,DAT4F	1	60H 4FH	
0478H	SACL 0,DAT50	1	60H 50H	
0479H	SACL 0,DAT51	1	60H 51H	
047AH	SACL 0,DAT55	1	60H 55H	
047BH	SACL 0,DAT56	1	60H 56H	
047CH	SACL 0,DAT57	1	60H 57H	
047DH	SACL 0,DAT5B	1	60H 5BH	
047EH	SACL 0,DAT5C	1	60H 5CH	
047FH	SACL 0,DAT5D	1	60H 5DH	
0480H	SACL 0,DAT5E	1	60H 5EH	
0481H	LALK 0100H	2	DOH 01H	;load each first counter with
0482H			01H 00H	; 256
0483H	SACL 0,DAT66	1	60H 66H	
0484H	SACL 0,DAT67	1	60H 67H	
0485H	SACL 0,DAT68	1	60H 68H	
0486H	LACK 75H	1	CAH 75H	;load each second counter with
0487H	SACL 0,DAT07	1	60H 07H	; 117
0488H	SACL 0,DAT27	1	60H 27H	
0489H	SACL 0,DAT47	1	60H 47H	

PHASE 1

048AH	SYNCH1	BIOZ START4	2/3	FAH 80H	;jump to START4 if the BIO pin
048BH				04H 93H	; is zero
048CH		LDPK 00H	1	C8H 00H	;reset INTO interrupt, and
048DH		LACK 00H	1	CAH 00H	; jump to RESET for
048EH		AND DAT04	1	4EH 04H	; asynchronous sampling
048FH		SACL 0,DAT04	1	60H 04H	
0490H		LDPK 04H	1	C8H 04H	
0491H		B RESET	3	FFH 80H	

0492H				00H 00H	
0493H	START4	ZALS DAT00	1	41H 00H	;increment count of number of
0494H		ADDS DAT04	1	49H 04H	; samples
0495H		SACL 0,DAT00	1	60H 00H	
0496H		IN 001 DAT01	2	81H 01H	;input phase-1 voltage
0497H		IN 002 DAT02	2	82H 02H	;input phase-1 current
0498H		LT DAT01	1	3CH 01H	;multiply phase-1 voltage by
0499H		MPY DAT02	1	38H 02H	; phase-1 current
049AH		SPH DAT0D	1	7DH 0DH	
049BH		SPL DAT0C	1	7CH 0CH	
049CH		ZAC	1	CAH 00H	;sign-extend the upper word of
049DH		SACL 0,DAT0E	1	60H 0EH	; the product to a third word
049EH		BIT 15,DAT0D	1	90H 0DH	
049FH		BBZ ONE4	2/3	F8H 80H	
04A0H				04H A4H	
04A1H		LALK OFFFFH	2	DOH 01H	
04A2H				FFH FFH	
04A3H		SACL 0,DAT0E	1	60H 0EH	
04A4H	ONE4	ZALS DAT0C	1	41H 0CH	;add the three-word product to
04A5H		ADDS DAT0F	1	49H 0FH	; the three-word accumulated
04A6H		SACL 0,DAT0F	1	60H 0FH	; phase-1 V.I total
04A7H		SACH 0,DAT6F	1	68H 6FH	
04A8H		ZALS DAT6F	1	41H 6FH	
04A9H		ADDS DAT0D	1	49H 0DH	
04AAH		ADDS DAT10	1	49H 10H	
04ABH		SACL 0,DAT10	1	60H 10H	;the running total is at
04ACH		SACH 0,DAT6F	1	68H 6FH	; addresses 0FH, 10H, and
04ADH		ZALS DAT6F	1	41H 6FH	; 11H (MSW)
04AEH		ADDS DAT0E	1	49H 0EH	
04AFH		ADDS DAT11	1	49H 11H	
04B0H		SACL 0,DAT11	1	60H 11H	
04B1H		SQRA DAT01	1	39H 01H	;square phase-1 voltage
04B2H		SPH DAT13	1	7DH 13H	
04B3H		SPL DAT12	1	7CH 12H	
04B4H		ZALS DAT12	1	41H 12H	;add the three-word product to
04B5H		ADDS DAT15	1	49H 15H	; the three-word accumulated
04B6H		SACL 0,DAT15	1	60H 15H	; phase-1 V.V total
04B7H		SACH 0,DAT6F	1	68H 6FH	
04B8H		ZALS DAT6F	1	41H 6FH	
04B9H		ADDS DAT13	1	49H 13H	
04BAH		ADDS DAT16	1	49H 16H	;the running total is at
04BBH		SACL 0,DAT16	1	60H 16H	; addresses 15H, 16H, and
04BCH		SACH 0,DAT6F	1	68H 6FH	; 17H (MSW)
04BDH		ZALS DAT6F	1	41H 6FH	
04BEH		ADDS DAT17	1	49H 17H	
04BFH		SACL 0,DAT17	1	60H 17H	
04C0H		SQRA DAT02	1	39H 02H	;square phase-1 current
04C1H		SPH DAT19	1	7DH 19H	
04C2H		SPL DAT18	1	7CH 18H	
04C3H		ZALS DAT18	1	41H 18H	;add the three-word product to
04C4H		ADDS DAT18	1	49H 18H	; the three-word accumulated
04C5H		SACL 0,DAT18	1	60H 18H	; phase-2 I.I total

04C6H		SACH 0,DAT6F	1	68H 6FH	
04C7H		ZALS DAT6F	1	41H 6FH	
04C8H		ADDS DAT19	1	49H 19H	
04C9H		ADDS DAT1C	1	49H 1CH	;the running total is at
04CAH		SACL 0,DAT1C	1	60H 1CH	; addresses 1BH, 1CH, and
04CBH		SACH 0,DAT6F	1	68H 6FH	; 1DH (MSW)
04CCH		ZALS DAT6F	1	41H 6FH	
04CDH		ADDS DAT1D	1	49H 1DH	
04CEH		SACL 0,DAT1D	1	60H 1DH	
04CFH		ZALS DAT66	1	41H 66H	;decrement first counter
04DOH		SUBS DAT04	1	45H 04H	
04D1H		SACL 0,DAT66	1	60H 66H	
04D2H		BZ TWO4	2/3	F6H 80H	;if first counter is 0, branch
04D3H				04H DBH	; to second counter
04D4H		LALK (phase 2)	2	DOH 01H	;load phase 2 starting address
04D5H				05H 26H	; into accumulator, push
04D6H		PUSH	1	CEH 1CH	; accumulator onto stack,
04D7H		EINT	1	CEH 00H	; enable interrupts, and wait
04D8H	THREE4	NOP	1	55H 00H	; for INTO interrupt
04D9H		B THREE4	3	FFH 80H	
04DAH				04H D8H	
04DBH	TWO4	LALK 0100H	2	DOH 01H	;load first counter with 256
04DCH				01H 00H	
04DDH		SACL 0,DAT66	1	60H 66H	
04DEH		ZALS DAT07	1	41H 07H	;decrement second counter
04DFH		SUBS DAT04	1	45H 04H	
04E0H		SACL 0,DAT07	1	60H 07H	
04E1H		BZ WRITE13	2/3	F6H 80H	;if 117 cycles, branch to write
04E2H				04H EAH	; routine
04E3H		LALK (phase 2)	2	DOH 01H	;load phase 2 starting address
04E4H				05H 26H	; into accumulator, push
04E5H		PUSH	1	CEH 1CH	; accumulator onto stack,
04E6H		EINT	1	CEH 00H	; enable interrupts, and wait
04E7H	FOUR4	NOP	1	55H 00H	; for INTO interrupt
04E8H		B FOUR4	3	FFH 80H	
04E9H				04H E7H	
04EAH	WRITE13	BIT 15,DAT11	1	90H 11H	;determine if the sum of V.1
04EBH		BBZ WRITE14	2/3	F8H 80H	; is negative, and if so,
04ECH				04H FBH	; transform it into the two's
04EDH		ZALS DAT11	1	41H 11H	; complement
04EEH		XOR DAT1F	1	4CH 1FH	
04EFH		SACL 0,DAT11	1	60H 11H	
04FOH		ZALS DAT0F	1	41H 0FH	
04F1H		ADDS DAT10	1	48H 10H	
04F2H		CMPL	1	CEH 27H	
04F3H		ADDS DAT04	1	49H 04H	
04F4H		SACL 0,DAT0F	1	60H 0FH	
04F5H		SACH 0,DAT10	1	68H 10H	
04F6H		ZAC	1	CAH 00H	
04F7H		ADDC DAT11	1	43H 11H	
04F8H		SACL 0,DAT11	1	60H 11H	

04F9H		ZALS DAT04	1	41H 04H	
04FAH		SACL 0,DAT1E	1	60H 1EH	
04FBH	WRITE14	LACK 00H	1	CAH 00H	;write the number of samples
04FCH		TBLW DAT00	3	59H 00H	; in phase-1 over 351 cycles
04FDH		LACK 05H	1	CAH 05H	;write the three-word phase-1
04FEH		TBLW DAT0F	3	59H 0FH	; V.I total
04FFH		LACK 06H	1	CAH 06H	
0500H		TBLW DAT10	3	59H 10H	
0501H		LACK 07H	1	CAH 07H	
0502H		TBLW DAT11	3	59H 11H	
0503H		LACK 08H	1	CAH 08H	;write the three-word phase-1
0504H		TBLW DAT15	3	59H 15H	; V.V total
0505H		LACK 09H	1	CAH 09H	
0506H		TBLW DAT16	3	59H 16H	
0507H		LACK 0AH	1	CAH 0AH	
0508H		TBLW DAT17	3	59H 17H	
0509H		LACK 0BH	1	CAH 0BH	;write the three-word phase-1
050AH		TBLW DAT1B	3	59H 1BH	; I.I total
050BH		LACK 0CH	1	CAH 0CH	
050CH		TBLW DAT1C	3	59H 1CH	
050DH		LACK 0DH	1	CAH 0DH	
050EH		TBLW DAT1D	3	59H 1DH	
050FH		LACK 0EH	1	CAH 0EH	;write 01 to common memory if
0510H		TBLW DAT1E	3	59H 1EH	; the sum of V.I is negative
0511H		ZAC	1	CAH 00H	;zero the data memory addresses
0512H		SACL 0,DAT00	1	60H 00H	; used in gathering data
0513H		SACL 0,DAT0F	1	60H 0FH	
0514H		SACL 0,DAT10	1	60H 10H	
0515H		SACL 0,DAT11	1	60H 11H	
0516H		SACL 0,DAT15	1	60H 15H	
0517H		SACL 0,DAT16	1	60H 16H	
0518H		SACL 0,DAT17	1	60H 17H	
0519H		SACL 0,DAT1B	1	60H 1BH	
051AH		SACL 0,DAT1C	1	60H 1CH	
051BH		SACL 0,DAT1D	1	60H 1DH	
051CH		SACL 0,DAT1E	1	60H 1EH	
051DH		LACK 75H	1	CAH 75H	;load counter with 117 cycles
051EH		SACL 0,DAT07	1	60H 07H	; for each write
051FH		LALK (phase 2)	2	DOH 01H	;load phase-2 starting address
0520H				05H 26H	; into accumulator, push
0521H		PUSH	1	CEH 1CH	; accumulator onto stack,
0522H		EINT	1	CEH 00H	; enable interrupts, and wait
0523H	WRITE15	NOP	1	55H 00H	; for INTO interrupt
0524H		B WRITE15	3	FFH 80H	
0525H				05H 23H	

PHASE 2

0526H	START15	ZALS DAT20	1	41H 20H	;increment count of number of
0527H		ADDS DAT04	1	49H 04H	; samples
0528H		SACL 0,DAT20	1	60H 20H	
0529H		IN 003 DAT21	2	83H 21H	;input phase-1 voltage

052AH	IN 004 DAT22	2	84H 22H	;input phase-1 current
052BH	LT DAT21	1	3CH 21H	;multiply phase-2 voltage by
052CH	MPY DAT22	1	38H 22H	; phase-2 current
052DH	SPH DAT2D	1	7DH 2DH	
052EH	SPL DAT2C	1	7CH 2CH	
052FH	ZAC	1	CAH 00H	;sign-extend the upper word of
0530H	SACL 0,DAT2E	1	60H 2EH	; the product to a third word
0531H	BIT 15,DAT2D	1	90H 2DH	
0532H	BBZ ONE5	2/3	F8H 80H	
0533H			05H 37H	
0534H	LALK OFFFFH	2	DOH 01H	
0535H			FFH FFH	
0536H	SACL 0,DAT2E	1	60H 2EH	
0537H	ZALS DAT2C	1	41H 2CH	;add the three-word product to
0538H	ADDS DAT2F	1	49H 2FH	; the three-word accumulated
0539H	SACL 0,DAT2F	1	60H 2FH	; phase-2 V.I total
053AH	SACH 0,DAT6F	1	68H 6FH	
053BH	ZALS DAT6F	1	41H 6FH	
053CH	ADDS DAT2D	1	49H 2DH	
053DH	ADDS DAT30	1	49H 30H	;the running total is at
053EH	SACL 0,DAT30	1	60H 30H	; addresses 2FH, 30H, and
053FH	SACH 0,DAT6F	1	68H 6FH	; 31H (MSW)
0540H	ZALS DAT6F	1	41H 6FH	
0541H	ADDS DAT2E	1	49H 2EH	
0542H	ADDS DAT31	1	49H 31H	
0543H	SACL 0,DAT31	1	60H 31H	
0544H	SQRA DAT21	1	39H 21H	;square phase-2 voltage
0545H	SPH DAT33	1	7DH 33H	
0546H	SPL DAT32	1	7CH 32H	
0547H	ZALS DAT32	1	41H 32H	;add the three-word product to
0548H	ADDS DAT35	1	49H 35H	; the three-word accumulated
0549H	SACL 0,DAT35	1	60H 35H	; phase-2 V.V total
054AH	SACH 0,DAT6F	1	68H 6FH	
054BH	ZALS DAT6F	1	41H 6FH	
054CH	ADDS DAT33	1	49H 33H	
054DH	ADDS DAT36	1	49H 36H	;the running total is at
054EH	SACL 0,DAT36	1	60H 36H	; addresses 35H, 36H, and
054FH	SACH 0,DAT6F	1	68H 6FH	; 37H (MSW)
0550H	ZALS DAT6F	1	41H 6FH	
0551H	ADDS DAT37	1	49H 37H	
0552H	SACL 0,DAT37	1	60H 37H	
0553H	SQRA DAT22	1	39H 22H	;square phase-2 current
0554H	SPH DAT39	1	7DH 39H	
0555H	SPL DAT38	1	7CH 38H	
0556H	ZALS DAT38	1	41H 38H	;add the three word product to
0557H	ADDS DAT3B	1	49H 3BH	; the three word accumulated
0558H	SACL 0,DAT3B	1	60H 3BH	; phase-2 I.I total
0559H	SACH 0,DAT6F	1	68H 6FH	
055AH	ZALS DAT6F	1	41H 6FH	
055BH	ADDS DAT39	1	49H 39H	
055CH	ADDS DAT3C	1	49H 3CH	;the running total is at
055DH	SACL 0,DAT3C	1	60H 3CH	; addresses 3BH, 3CH, and

055EH		SACL 0,DAT6F	1	68H 6FH	; 3DH (MSW)
055FH		ZALS DAT6F	1	41H 6FH	
0560H		ADDS DAT3D	1	49H 3DH	
0561H		SACL 0,DAT3D	1	60H 3DH	
0562H		ZALS DAT67	1	41H 67H	;decrement first counter
0563H		SUBS DAT04	1	45H 04H	
0564H		SACL 0,DAT67	1	60H 67H	
0565H		BZ TWO5	2/3	F6H 80H	;if first counter is 0, branch
0566H				05H 6EH	; to second counter
0567H		LALK (phase 3)	2	DOH 01H	;load phase 3 starting address
0568H				05H B9H	; into accumulator, push
0569H		PUSH	1	CEH 1CH	; accumulator onto stack,
056AH		EINT	1	CEH 00H	; enable interrupts, and wait
056BH	THREE5	NOP	1	55H 00H	; for INTO interrupt
056CH		B THREE5	3	FFH 80H	
056DH				05H 6BH	
056EH	TWO5	LALK 0100H	2	DOH 01H	;load first counter with 256
056FH				01H 00H	
0570H		SACL 0,DAT67	1	60H 67H	
0571H		ZALS DAT27	1	41H 27H	;decrement second counter
0572H		SUBS DAT04	1	45H 04H	
0573H		SACL 0,DAT27	1	60H 27H	
0574H		BZ WRITE16	2/3	F6H 80H	;if 117 cycles, branch to write
0575H				05H 7DH	; routine
0576H		LALK (phase 3)	2	DOH 01H	;load phase 3 starting address
0577H				05H B9H	; into accumulator, push
0578H		PUSH	1	CEH 1CH	; accumulator onto stack,
0579H		EINT	1	CEH 00H	; enable interrupts, and wait
057AH	FOUR5	NOP	1	55H 00H	; for INTO interrupt
057BH		B FOUR5	3	FFH 80H	
057CH				05H 7AH	
057DH	WRITE16	BIT 15,DAT31	1	90H 31H	;determine if the sum of V.I
057EH		BBZ WRITE17	2/3	F8H 80H	; is negative, and if so,
057FH				05H 8EH	; transform it into the two's
0580H		ZALS DAT31	1	41H 31H	; complement
0581H		XOR DAT1F	1	4CH 1FH	
0582H		SACL 0,DAT31	1	60H 31H	
0583H		ZALS DAT2F	1	41H 2FH	
0584H		ADDS DAT30	1	48H 30H	
0585H		CMPL	1	CEH 27H	
0586H		ADDS DAT04	1	49H 04H	
0587H		SACL 0,DAT2F	1	60H 2FH	
0588H		SACL 0,DAT30	1	68H 30H	
0589H		ZAC	1	CAH 00H	
058AH		ADDS DAT31	1	43H 31H	
058BH		SACL 0,DAT31	1	60H 31H	
058CH		ZALS DAT04	1	41H 04H	
058DH		SACL 0,DAT3E	1	60H 3EH	
058EH	WRITE17	LACK 10H	1	CAH 10H	;write the number of samples
058FH		TRFW DAT20	3	59H 20H	; in phase-2 over 117 cycles
0590H		LACK 15H	1	CAH 15H	;write the three-word phase-2

0591H	TBLW DAT2F	3	59H 2FH	; V.I total
0592H	LACK 16H	1	CAH 16H	
0593H	TBLW DAT30	3	59H 30H	
0594H	LACK 17H	1	CAH 17H	
0595H	TBLW DAT31	3	59H 31H	
0596H	LACK 18H	1	CAH 18H	;write the three-word phase-2
0597H	TBLW DAT35	3	59H 35H	; V.V total
0598H	LACK 19H	1	CAH 19H	
0599H	TBLW DAT36	3	59H 36H	
059AH	LACK 1AH	1	CAH 1AH	
059BH	TBLW DAT37	3	59H 37H	
059CH	LACK 1BH	1	CAH 1BH	;write the three-word phase-2
059DH	TBLW DAT3B	3	59H 3BH	; I.I total
059EH	LACK 1CH	1	CAH 1CH	
059FH	TBLW DAT3C	3	59H 3CH	
05A0H	LACK 1DH	1	CAH 1DH	
05A1H	TBLW DAT3D	3	59H 3DH	
05A2H	LACK 1EH	1	CAH 1EH	;write 01 to common memory if
05A3H	TBLW DAT3E	3	59H 3EH	; the sum of V.I is negative
05A4H	ZAC	1	CAH 00H	;zero the data memory addresses
05A5H	SACL 0,DAT20	1	60H 20H	; used in gathering data
05A6H	SACL 0,DAT2F	1	60H 2FH	
05A7H	SACL 0,DAT30	1	60H 30H	
05A8H	SACL 0,DAT31	1	60H 31H	
05A9H	SACL 0,DAT35	1	60H 35H	
05AAH	SACL 0,DAT36	1	60H 36H	
05ABH	SACL 0,DAT37	1	60H 37H	
05ACH	SACL 0,DAT3B	1	60H 3BH	
05ADH	SACL 0,DAT3C	1	60H 3CH	
05AEH	SACL 0,DAT3D	1	60H 3DH	
05AFH	SACL 0,DAT3E	1	60H 3EH	
05B0H	LACK 75H	1	CAH 75H	;load counter with 117 cycles
05B1H	SACL 0,DAT27	1	60H 27H	; for each write
05B2H	LALK (phase 3)	2	DOH 01H	;load phase-3 starting address
05B3H			05H B9H	; into accumulator, push
05B4H	PUSH	1	CEH 1CH	; accumulator onto stack,
05B5H	EINT	1	CEH 006	; enable interrupts, and wait
05B6H	WRITE18 NOP	1	55H 00H	; for INTO interrupt
05B7H	B WRITE18	3	FFH 80H	
05B8H			05H B6H	

PHASE 3

05B9H	START6	ZALS DAT40	1	41H 40H	;increment count of number of
05BAH		ADDS DAT04	1	49H 04H	; samples
05BBH		SACL DAT40	1	60H 40H	
05BCH		IN 005 DAT41	2	85H 41H	;input phase 3 voltage
05BDH		IN 006 DAT42	2	86H 42H	;input phase-3 current
05BEH		LT DAT41	1	3CH 41H	;multiply phase-3 voltage by
05BFH		MPY DAT42	1	38H 42H	; phase-3 current
05C0H		SPH DAT4D	1	7DH 4DH	
05C1H		SPL DAT4C	1	7CH 4CH	

05C2H	ZAC	1	CAH 00H	;sign-extend the upper word of
05C3H	SACL 0,DAT4E	1	60H 4EH	; the product to a third word
05C4H	BIT 15,DAT4D	1	90H 4DH	
05C5H	BBZ ONE6	2/3	F8H 80H	
05C6H			05H CAH	
05C7H	LALK OFFFFH	2	D0H 01H	
05C8H			FFH FFH	
05C9H	SACL 0,DAT4E	1	60H 4EH	
05CAH	ONE6 ZALS DAT4C	1	41H 4CH	;add the three-word product to
05CBH	ADDS DAT4F	1	49H 4FH	; the three-word accumulated
05CCH	SACL 0,DAT4F	1	60H 4FH	; phase-3 V.I total
05CDH	SACH 0,DAT6F	1	68H 6FH	
05CEH	ZALS DAT6F	1	41H 6FH	
05CFH	ADDS DAT4D	1	49H 4DH	
05DOH	ADDS DAT50	1	49H 50H	;the running total is at
05D1H	SACL 0,DAT50	1	60H 50H	; addresses 4FH, 50H, and
05D2H	SACH 0,DAT6F	1	68H 6FH	; 51H (MSW)
05D3H	ZALS DAT6F	1	41H 6FH	
05D4H	ADDS DAT4E	1	49H 4EH	
05D5H	ADDS DAT51	1	49H 51H	
05D6H	SACL 0,DAT51	1	60H 51H	
05D7H	SQRA DAT41	1	39H 41H	;square phase-3 voltage
05D8H	SPH DAT53	1	7DH 53H	
05D9H	SPL DAT52	1	7CH 52H	
05DAH	ZALS DAT52	1	41H 52H	;add the three-word product to
05DBH	ADDS DAT55	1	49H 55H	; the three-word accumulated
05DCH	SACL 0,DAT55	1	60H 55H	; phase-3 V.V total
05DDH	SACH 0,DAT6F	1	68H 6FH	
05DEH	ZALS DAT6F	1	41H 6FH	
05DFH	ADDS DAT53	1	49H 53H	
05EOH	ADDS DAT56	1	49H 56H	;the running total is at
05E1H	SACL 0,DAT56	1	60H 56H	; addresses 55H, 56H, and
05E2H	SACH 0,DAT6F	1	68H 6FH	; 57H (MSW)
05E3H	ZALS DAT6F	1	41H 6FH	
05E4H	ADDS DAT57	1	49H 57H	
05E5H	SACL 0,DAT57	1	60H 57H	
05E6H	SQRA DAT42	1	39H 42H	;square phase-3 current
05E7H	SPH DAT59	1	7DH 59H	
05E8H	SPL DAT58	1	7CH 58H	
05E9H	ZALS DAT58	1	41H 58H	;add the three-word product to
05EAH	ADDS DAT5B	1	49H 5BH	; the three-word accumulated
05EBH	SACL 0,DAT5B	1	60H 5BH	; phase-3 I.I total
05ECH	SACH 0,DAT6F	1	68H 6FH	
05EDH	ZALS DAT6F	1	41H 6FH	
05EEH	ADDS DAT59	1	49H 59H	
05EFH	ADDS DAT5C	1	49H 5CH	;the running total is at
05FOH	SACL 0,DAT5C	1	60H 5CH	; addresses 5BH, 5CH, and
05F1H	SACH 0,DAT6F	1	68H 6FH	; 5DH (MSW)
05F2H	ZALS DAT6F	1	41H 6FH	
05F3H	ADDS DAT5D	1	49H 5DH	
05F4H	SACL 0,DAT5D	1	60H 5DH	
05F5H	ZALS DAT6H	1	41H 68H	;decrement first counter

05F6H		SUBS DAT04	1	45H 04H	
05F7H		SACL 0,DAT68	1	60H 68H	
05F8H		BZ TWO6	2/3	F6H 80H	;if first counter is 0, branch
05F9H				06H 01H	; to second counter
05FAH		LALK (phase 1)	2	DOH 01H	;load phase 1 starting address
05FBH				04H 8AH	; into accumulator, push
05FCH		PUSH	1	CEH 1CH	; accumulator onto stack,
05FDH		EINT	1	CEH 00H	; enable interrupts, and wait
05FEH	THREE6	NOP	1	55H 00H	; for INTO interrupt
05FFH		B THREE6	3	FFH 80H	
0600H				05H FEH	
0601H	TWO6	LALK 0100H	2	DOH 01H	;load first counter with 256
0602H				01H 00H	
0603H		SACL 0,DAT68	1	60H 68H	
0604H		ZALS DAT47	1	41H 47H	;decrement second counter
0605H		SUBS DAT04	1	45H 04H	
0606H		SACL 0,DAT47	1	60H 47H	
0607H		BZ WRITE19	2/3	F6H 80H	;if 117 cycles, branch to write
0608H				06H 10H	; routine
0609H		LALK (phase 1)	2	DOH 01H	;load phase 1 starting address
060AH				04H 8AH	; into accumulator, push
060BH		PUSH	1	CEH 1CH	; accumulator onto stack,
060CH		EINT	1	CEH 00H	; enable interrupts, and wait
060DH	FOUR6	NOP	1	55H 00H	; for INTO interrupt
060EH		B FOUR6	3	FFH 80H	
060FH				06H 0DH	
0610H	WRITE19	BIT 15,DAT51	1	90H 51H	;determine if the sum of V.I
0611H		BBZ WRITE20	2/3	F8H 80H	; is negative, and if so,
0612H				06H 21H	; transform it into the two's
0613H		ZALS DAT51	1	41H 11H	; complement
0614H		XOR DAT1F	1	4CH 1FH	
0615H		SACL 0,DAT51	1	60H 51H	
0616H		ZALS DAT4F	1	41H 4FH	
0617H		ADDH DAT50	1	48H 50H	
0618H		CMPL	1	CEH 27H	
0619H		ADDS DAT04	1	49H 04H	
061AH		SACL 0,DAT4F	1	60H 4FH	
061BH		SACH 0,DAT50	1	68H 50H	
061CH		ZAC	1	CAH 00H	
061DH		ADDC DAT51	1	43H 51H	
061EH		SACL 0,DAT51	1	60H 51H	
061FH		ZALS DAT04	1	41H 04H	
0620H		SACL 0,DAT5E	1	60H 5EH	
0621H	WRITE20	LACK 20H	1	CAH 20H	;write the number of samples
0622H		TBLW DAT40	3	59H 40H	; in phase 3 over 117 cycles
0623H		LACK 25H	1	CAH 25H	;write the three-word phase 3
0624H		TBLW DAT4F	3	59H 4FH	; V.I total
0625H		LACK 26H	1	CAH 26H	
0626H		TBLW DAT50	3	59H 50H	
0627H		LACK 27H	1	CAH 27H	
0628H		TBLW DAT51	3	59H 51H	

0629H	LACK 28H	1	CAH 28H	;write the three-word phase-3
062AH	TBLW DAT55	3	59H 55H	; V.V total
062BH	LACK 29H	1	CAH 29H	
062CH	TBLW DAT56	3	59H 56H	
062DH	LACK 2AH	1	CAH 2AH	
062EH	TBLW DAT57	3	59H 57H	
062FH	LACK 2BH	1	CAH 2BH	;write the three-word phase-3
0630H	TBLW DAT5B	3	59H 5BH	; I.I total
0631H	LACK 2CH	1	CAH 2CH	
0632H	TBLW DAT5C	3	59H 5CH	
0633H	LACK 2DH	1	CAH 2DH	
0634H	TBLW DAT5D	3	59H 5DH	
0635H	LACK 2EH	1	CAH 2EH	;write 01 to common memory if
0636H	TBLW DAT5E	3	59H 5EH	; the sum of V.I is negative
0637H	RXF	1	CEH 0CH	;reset XF output pin
0638H	ZAC	1	CAH 00H	;zero the data memory addresses
0639H	SACL 0,DAT40	1	60H 40H	; used in gathering data
063AH	SACL 0,DAT4F	1	60H 4FH	
063BH	SACL 0,DAT50	1	60H 50H	
063CH	SACL 0,DAT51	1	60H 51H	
063DH	SACL 0,DAT55	1	60H 55H	
063EH	SACL 0,DAT56	1	60H 56H	
063FH	SACL 0,DAT57	1	60H 57H	
0640H	SACL 0,DAT5B	1	60H 5BH	
0641H	SACL 0,DAT5C	1	60H 5CH	
0642H	SACL 0,DAT5D	1	60H 5DH	
0643H	SACL 0,DAT5E	1	60H 5EH	
0644H	LACK 75H	1	CAH 75H	;load counter with 117 cycles
0645H	SACL 0,DAT47	1	60H 47H	; for each write
0646H	LALK (phase 1)	2	DOH 01H	;load phase-1 starting address
0647H			04H 8AH	; into accumulator, push
0648H	PUSH	1	CEH 1CH	; accumulator onto stack, set
0649H	SXF	1	CEH 0DH	; XF output pin, enable
064AH	EINT	1	CEH 00H	; interrupts, and wait for
064BH	WRITE21 NOP	1	55H 00H	; INTO interrupt
064CH	B WRITE21	3	FFH 80H	
064DH			06H 4BH	

APPENDIX D:
SOURCE CODE FOR THE I8096 PROCESSOR

INTEL 8096 PROGRAM

INITIALIZATION

ADDRESS	COMMAND	OBJECT CODE	COMMENTS
200EH	low address	7D	;EXTINT address low byte
200FH	high address	3C	;EXTINT address high byte
2080H	COLDSTART LD SP,0F8H	A1 F8 00 18	;locate SP at 00F8H
2084H	LDB 40H,0CH	B1 0C 40	;reset the 12-character
2087H	LD 20H,E036H	A1 36 E0 20	; display by writing to
208BH	LD 30H,0000H	A1 00 00 30	; each address with CU low
208FH	BACK ST 30H,(20H)	C2 20 30	; and D0 low
2092H	SUBB 20H,02H	79 02 20	;
2095H	DECB 40H	15 40	;
2097H	CMPB 40H,00H	98 00 40	;
209AH	JCT BACK	D2 F3	;
209CH	LD 20H,9800H	A1 00 98 20	;load display RAM with spaces
20A0H	LD 30H,0020H	A1 20 00 30	;
20A4H	DISP1 SUB 20H,0002H	69 02 00 20	;
20A8H	ST 30H,(20H)	C2 20 30	;
20ABH	CMP 20H,9000H	89 00 90 20	;
20AFH	JNE DISP1	D7 F3	;
20F1H	LD 20H,987CH	A1 7C 98 20	;load display RAM with line
20B5H	LD 30H,000AH	A1 0A 00 30	; feeds
20B9H	DISP2 SUB 20H,0080H	69 80 00 20	;
20BDH	ST 30H,(20H)	C2 20 30	;
20C0H	CMP 20H,907CH	89 7C 90 20	;
20C4H	JNE DISP2	D7 F3	;
20C6H	LD 20H,987EH	A1 7E 98 20	;load display RAM with
20CAH	LD 30H,000DH	A1 0D 00 30	; carriage returns
20CEH	DISP3 SUB 20H,0080H	69 80 00 20	;
20D2H	ST 30H,(20H)	C2 20 30	;
20D5H	CMP 20H,907EH	89 7E 90 20	;
20D9H	JNE DISP3	D7 F3	;
20DBH	LD 20H,C000H	A1 00 C0 20	;load 15-Min. Demand RAM with
20DFH	LD 30H,0000H	A1 00 00 30	; zeroes
20E3H	DISP4 SUB 20H,0002H	69 02 00 20	;
20E7H	ST 30H,(20H)	C2 20 30	;
20EAH	CMP 20H,A000H	89 00 A0 20	;
20EEH	JNE DISP4	D7 F3	;
20F0H	LD 20H,A004H	A1 04 A0 20	;load four address pointers
20F4H	LD 30H,A020H	A1 20 A0 30	; for pointing to V.A
20F8H	ST 30H,(20H)	C2 20 30	; value for calculation of
20FEH	LD 20H,A804H	A1 04 A8 20	; 15-Min. Demand
20FFH	LD 30H,A820H	A1 20 A8 30	;
2103H	ST 30H,(20H)	C2 20 30	;
2106H	LD 20H,B004H	A1 04 B0 20	;
210AH	LD 30H,B020H	A1 20 B0 30	;

210EH	ST 30H,(20H)	C2 20 30	:
2111H	LD 20H,B804H	A1 04 B8 20	:
2115H	LD 30H,B820H	A1 20 B8 30	:
2119H	ST 30H,(20H)	C2 20 30	:
211CH	LD 40H,8FB EH	A1 BE 8F 40	;load display RAM with
2120H	LDB 50H,04H	B1 04 50	; descriptive statements
2123H	DISP5 LD 30H,2158H	A1 58 21 30	:
2127H	LDB 51H,08H	B1 08 51	:
212AH	DISP6 LD 20H,40H	A0 40 20	:
212DH	ADD 20H,0040H	65 40 00 20	:
2131H	LD 40H,20H	A0 20 40	:
2134H	DISP7 ADD 20H,0002H	65 02 00 20	:
2138H	ADD 30H,0002H	65 02 00 30	:
213CH	LD 70H,(30H)	A2 30 70	:
213FH	ST 70H,(20H)	C2 20 70	:
2142H	CMP 70H,003AH	89 3A 00 70	:
2146H	JNE DISP7	D7 EC	:
2148H	DECB 51H	15 51	:
214AH	CHPB 00H,51H	98 00 51	:
214DH	JNE DISP6	D7 DB	:
214FH	DECB 50H	15 50	:
2151H	CHPB 00H,50H	98 00 50	:
2154H	JNE DISP5	D7 CD	:
2156H	LJMP DISP8	E7 CD 00	:
2159H	NOP	FD	:
215AH	0056H,006FH	56 00 6F 00	;data for display RAM
215EH	006CH,0074H	6C 00 74 00	; descriptive statements:
2162H	0061H,0067H	61 00 67 00	; Voltage RMS, Current RMS,
2166H	0065H,0020H	65 00 20 00	; Applied Power, Active
216AH	0052H,004DH	52 00 4D 00	; Power, Power Factor,
216EH	0053H,003AH	53 00 3A 00	; Frequency, Consumption,
2172H	0043H,0075H	43 00 75 00	; 15-Min. Demand
2176H	0072H,0072H	72 00 72 00	:
217AH	0065H,006EH	65 00 6E 00	:
217EH	0074H,0020H	74 00 20 00	:
2182H	0052H,004DH	52 00 4D 00	:
2186H	0C53H,003AH	53 00 3A 00	:
218AH	0041H,0070H	41 00 70 00	:
218EH	0070H,0061H	70 00 61 00	:
2192H	0072H,0065H	72 00 65 00	:
2196H	006EH,0074H	6E 00 74 00	:
219AH	0020H,0050H	20 00 50 00	:
219EH	006FH,0077H	6F 00 77 00	:
21A2H	0065H,0072H	65 00 72 00	:
21A6H	003AH,0041H	3A 00 41 00	:
21AAH	0063H,0074H	63 00 74 00	:
21AEH	0069H,0076H	69 00 76 00	:
21B2H	0065H,0020H	65 00 20 00	:
21B6H	0050H,006FH	50 00 6F 00	:
21BAH	0077H,0065H	77 00 65 00	:
21BEH	0072H,003AH	72 00 3A 00	:
21C2H	0050H,006FH	50 00 6F 00	:

21C6H	0077H,0065H	77 00 65 00	:
21CAH	0072H,0020H	72 00 20 00	:
21CEH	0046H,0061H	46 00 61 00	:
21D2H	0063H,0074H	63 00 74 00	:
21D6H	006FH,0072H	6F 00 72 00	:
21DAH	003AH,0046H	3A 00 46 00	:
21DEH	0072H,0065H	72 00 65 00	:
21E2H	0071H,0075H	71 00 75 00	:
21E6H	0065H,006EH	65 00 6E 00	:
21EAH	0063H,0079H	63 00 79 00	:
21EEH	003AH,0043H	3A 00 43 00	:
21F2H	006FH,006EH	6F 00 6E 00	:
21F6H	0073H,0075H	73 00 75 00	:
21FAH	006DH,0070H	6D 00 70 00	:
21FEH	0074H,0069H	74 00 69 00	:
2202H	006FH,006EH	6F 00 6E 00	:
2206H	003AH,0031H	3A 00 31 00	:
220AH	0035H,002DH	35 00 2D 00	:
220EH	004DH,0069H	4D 00 69 00	:
2212H	006EH,002EH	6E 00 2E 00	:
2216H	0020H,0044H	20 00 44 00	:
221AH	0065H,006DH	65 00 6D 00	:
221EH	0061H,006EH	61 00 6E 00	:
2222H	0064H,003AH	64 00 3A 00	:
2226H	DISPB LD 20H,E016H	A1 16 E0 20	;load display address
222AH	LD 30H,0050H	A1 50 00 30	; with 'PLEASE WAIT!'
222EH	ST 30H,(20H)	C2 20 30	:
2231H	SUBB 20H,02H	79 02 20	:
2234H	LDB 30H,4CH	B1 4C 30	:
2237H	ST 30H,(20H)	C2 20 30	:
223AH	SUBB 20H,02H	79 02 20	:
223DH	LDB 30H,45H	B1 45 30	:
2240H	ST 30H,(20H)	C2 20 30	:
2243H	SUBB 20H,02H	79 02 20	:
2246H	LDB 30H,41H	B1 41 30	:
2249H	ST 30H,(20H)	C2 20 30	:
224CH	SUBB 20H,02H	79 02 20	:
224FH	LDB 30H,53H	B1 53 30	:
2252H	ST 30H,(20H)	C2 20 30	:
2255H	SUBB 20H,02H	79 02 20	:
2258H	LDB 30H,45H	B1 45 30	:
225BH	ST 30H,(20H)	C2 20 30	:
225EH	SUBB 20H,02H	79 02 20	:
2261H	LDB 30H,20H	B1 20 30	:
2264H	ST 30H,(20H)	C2 20 30	:
2267H	SUBB 20H,02H	79 02 20	:
226AH	LDB 30H,57H	B1 57 30	:
226DH	ST 30H,(20H)	C2 20 30	:
2270H	SUBB 20H,02H	79 02 20	:
2273H	LDB 30H,41H	B1 41 30	:
2276H	ST 30H,(20H)	C2 20 30	:

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2279H      SUBB 20H,02H      79 02 20      ;
227CH      LDB 30H,49H      B1 49 30      ;
227FH      ST 30H,(20H)     C2 20 30      ;
2282H      SUBB 20H,02H      79 02 20      ;
2285H      LDB 3CH,54H      B1 54 30      ;
2288H      ST 30H,(20H)     C2 20 30      ;
228BH      SUBB 20H,02H      79 02 20      ;
228EH      LDB 30H,21H      B1 21 30      ;
2291H      ST 30H,(20H)     C2 20 30      ;

2294H      CLRB 80H          11 80          ;one-second delay routine
2296H      LD 82H,800H       A1 00 08 82    ;
229AH      ONE              DEC 82H         05 82          ;
229CH      DJNZ 80H         EO 80 FD        ;
229FH      CMP 82H,00H      88 00 82        ;
22A2H      JGT ONE          D2 F6          ;

22A4H      ANDB PORT1,7FH    71 7F 0F      ;reset the TMS320C25
22A7H      ORB PORT1,80H     91 80 0F      ;

22AAH      ANDB INT-P,00H    71 00 09      ;reset all of INT-PEND. reg.

22ADH      ANDB IOC1,0FDH    71 FD 16      ;connect EXTINT interrupt
22BDH      ORB INT-MSK,80H    91 80 08      ;activate EXTINT interrupt
22B3H      EI                FB            ;enable interrupts

22B4H      JBC bit4,09H      34 09 FD        ;low 'C25 XF output sets bit4
; of INT-PEND. register

                                START

22B7H      REPEAT          ANDB 09H,EFH      71 EF 09      ;clear HSI.0 in interrupt
; pending register

22BAH      EXTINT          ANDB IOC1,0FDH    71 FD 16      ;connect EXTINT interrupt
22BDH      ORB INT-MSK,80H    91 80 08      ;activate EXTINT interrupt
22C0H      EI                FB            ;enable interrupts

22C1H      MEMTRANS        LDB 80H,30H      B1 30 80      ;transfer contents of common
22C4H      LD 82H,C000H      A1 00 C0 82    ; memory to the I96 RAM
22C8H      LD 84H,8000H      A1 00 80 84    ; starting at 8090H
22CCH      TWO            LD 86H,(82H)      A2 82 86      ;
22CFH      ST 86H,(84H)      C2 84 86      ;
22D2H      ADDB 82H,02H      75 02 82      ;
22D5H      ADDB 84H,02H      75 02 84      ;
22D8H      DECB 80H          15 80          ;
22DAH      CMPB 80H,00H      98 00 80      ;
22DDH      JGT TWO          D2 ED          ;

22DFH      LD 54H,80FFH      A1 FF 80 54    ;reset phase counter for
22E3H      ST 00H,(54H)     C2 54 00      ; frequency

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CALIBRATE

22E6H		LD 2CH,0008H	A1 08 00 2C	;load counter
22EAH		JBS P0-0,SECURE	38 0E 03	;jump to PHASE1 if bit0 of
22EDH		LJMP PHASE1	E7 7D 02	port0 is clear
22F0H	SECURE	JBS P0-1,THREE	39 0E 03	;jump to PHASE1 if bit1 of
22F3H		LJMP PHASE1	E7 77 02	port0 is clear
22F6H	THREE	JBS P0-2,FOUR	32 0E 03	;jump to FIVE if bit2 of port0
22F9H		LJMP FIVE	E7 D6 00	is set
22FCH	FOUR	JBS P0-3,SIX	3B 0E 03	;jump to SEVEN if bit3 of
22FFH		LJMP SEVEN	E7 68 00	port0 is clear
2302H	SIX	JBS P0-4,EIGHT	3C 0E 03	;jump to NINE if bit4 of
2305H		LJMP NINE	E7 31 00	port0 is clear
2308H	EIGHT	JBS P0-5,TEN	3D 0E 17	;jump to TEN if bit5 is set
230BH		LD 80H,6028H	A1 28 60 80	;load zero in Kwh phase-2
230FH		LD 2EH,2CH	A0 2C 2E	(6028H to 6037H)
2312H	AGAIN1	ST 00H,80H	C2 80 00	
2315H		ADDB 80H,02H	75 02 80	
2318H		DEC 2EH	05 2E	
231AH		CMP 2EH,00H	88 00 2E	
231DH		JGT AGAIN1	D2 F3	
231FH		LJMP PHASE1	E7 4B 02	
2322H	TEN	LD 80H,6038H	A1 38 60 80	;load zero in Kwh phase-3
2326H		LD 2EH,2CH	A0 2C 2E	(6038H to 6047H)
2329H	AGAIN2	ST 00H,80H	C2 80 00	
232CH		ADDB 80H,02H	75 02 80	
232FH		DEC 2EH	05 2E	
2331H		CMP 2EH,00H	88 00 2E	
2334H		JGT AGAIN2	D2 F3	
2336H		LJMP PHASE1	E7 34 02	
2339H	NINE	JBS P0-5,TEN1	3D 0E 17	;jump to TEN1 if bit5 is set
233CH		LD 80H,6048H	A1 48 60 80	;load zero in Kwh total
2340H		LD 2EH,2CH	A0 2C 2E	(6048H to 6057H)
2343H	AGAIN3	ST 00H,80H	C2 80 00	
2346H		ADDB 80H,02H	75 02 80	
2349H		DEC 2EH	05 2E	
234BH		CMP 2EH,00H	88 00 2E	
234EH		JGT AGAIN3	D2 F3	
2350H		LJMP PHASE1	E7 1A 02	
2353H	TEN1	LD 80H,6018H	A1 18 60 80	;load zero in Kwh phase-1
2357H		LD 2EH,2CH	A0 2C 2E	(6018H to 6027H)
235AH	AGAIN4	ST 00H,80H	C2 80 00	
235DH		ADDB 80H,02H	75 02 80	
2360H		DEC 2EH	05 2E	
2362H		CMP 2EH,00H	88 00 2E	
2365H		JGT AGAIN4	D2 F3	
2367H		LJMP PHASE1	E7 03 02	
236AH	SEVEN	JBS P0-4,TEN2	3C 0E 03	;jump to TEN3 if bit4 of
236DH		LJMP TEN3	E7 2F 00	port0 is clear
2370H	TEN2	JBS P0-5,TEN4	3D 0E 17	;jump to TEN4 if bit5 is set
2373H		LD 80H,6068H	A1 68 60 80	;load zero in phase-2 demand
2377H		LD 2EH,2CH	A0 2C 2E	(6068H to 6077H)

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237AH  AGAIN5  ST 00H,80H      C2 80 00      ;
237DH          ADDB 80H,02H    75 02 80      ;
2380H          DEC 2EH         05 2E         ;
2382H          CMP 2EH,00H     88 00 2E      ;
2385H          JGT AGAIN5      D2 F3         ;
2387H          LJMP PHASE1     E7 E3 01      ;
238AH  TEN4    LD 80H,6078H    A1 78 60 80    ;load zero in phase-3 demand
238EH          LD 2EH,2CH      A0 2C 2E      ; (6078H to 6087H)
2391H  AGAIN6  ST 00H,80H      C2 80 00      ;
2394H          ADDB 80H,02H    75 02 80      ;
2397H          DEC 2EH         05 2E         ;
2399H          CMP 2EH,00H     88 00 2E      ;
239CH          JGT AGAIN6      D2 F3         ;
239EH          LJMP PHASE1     E7 CC 01      ;
23A1H  TEN3    JBS PO-5,TEN5   3D 0E 17      ;jump to TEN5 if bit5 is set
23A4H          LD 80H,6088H    A1 88 60 80    ;load zero in total demand
23A8H          LD 2EH,2CH      A0 2C 2E      ; (6088H to 6097H)
23ABH  AGAIN7  ST 00H,80H      C2 80 00      ;
23AEH          ADDB 80H,02H    75 02 80      ;
23B1H          DEC 2EH         05 2E         ;
23B3H          CMP 2EH,00H     88 00 2E      ;
23B6H          JGT AGAIN7      D2 F3         ;
23B8H          LJMP PHASE1     E7 B2 01      ;
23BBH  TEN5    LD 80H,6058H    A1 58 60 80    ;load zero in phase-1 demand
23BFH          LD 2EH,2CH      A0 2C 2E      ; (6058H to 6067H)
23C2H  AGAIN8  ST 00H,80H      C2 80 00      ;
23C5H          ADDB 80H,02H    75 02 80      ;
23C8H          DEC 2EH         05 2E         ;
23CAH          CMP 2EH,00H     88 00 2E      ;
23CDH          JGT AGAIN8      D2 F3         ;
23CFH          LJMP PHASE1     E7 9B 01      ;
23D2H  FIVE    JBS PO-3,TEN6   3B 0E 03      ;jump to TEN7 if bit3 of port0
23D5H          LJMP TEN7       E7 CC 00      ; is clear
23D8H  TEN6    JBS PO-4,TEN8   3C 0E 03      ;jump to TEN9 if bit4 of port0
23DBH          LJMP TEN9       E7 83 00      ; is clear
23DEH  TEN8    JBS PO-5,TWEN   3D 0E 40      ;jump to TWEN if bit5 is set
23E1H          LD 80H,8020H    A1 20 80 80    ;determine phase-2 voltage
23E5H          LD E6H,(80H)     A2 80 E6      ; calibration factor, and
23E8H          ADDB 80H,10H     75 10 80      ; store at 6004H to 6007H
23EBH          LD E0H,(80H)     A2 80 E0      ;
23EEH          ADDB 80H,02H     75 02 80      ;
23F1H          LD E2H,(80H)     A2 80 E2      ;
23F4H          ADDB 80H,02H     75 02 80      ;
23F7H          LD E4H,(80H)     A2 80 E4      ;
23FAH          CALL DIV        EF F5 13      ;
23FDH          CALL SORT       EF 0D 14      ;
2400H          LD A0H,C800H     A1 00 C8 A0    ;
2404H          LD B0H,(A0H)     A2 A0 B0      ;
2407H          LD A0H,C400H     A1 00 C4 A0    ;
240BH          LD B2H,(A0H)     A2 A0 B2      ;
240EH          DIVU B0H,B4H     8C B4 B0      ;
2411H          LD A0H,6004H     A1 04 60 A0    ;

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2415H		ST B2H,(AOH)	C2 A0 B2	;remainder at 6004H
2418H		ADDB AOH,02H	75 02 A0	;
241BH		ST B0H,(AOH)	C2 A0 B0	;quotient at 6006H
241EH		LJMP PHASE1	E7 4C 01	;
2421H	TWEN	LD 80H,8040H	A1 20 80 80	;determine phase-3 voltage
2425H		LD E6H,(80H)	A2 80 E6	; calibration factor, and
2428H		ADDB 80H,10H	75 10 80	; store at 6008H to 600BH
242BH		LD E0H,(80H)	A2 80 E0	;
242EH		ADDB 80H,02H	75 02 80	;
2431H		LD E2H,(80H)	A2 80 E2	;
2434H		ADDB 80H,02H	75 02 80	;
2437H		LD E4H,(80H)	A2 80 E4	;
243AH		CALL DIV	EF B5 13	;
243DH		CALL SQRT	EF CD 13	;
2440H		LD AOH,C800H	A1 00 C8 A0	;
2444H		LD B0H,(AOH)	A2 A0 B0	;
2447H		LD AOH,C400H	A1 00 C4 A0	;
244BH		LD B2H,(AOH)	A2 A0 B2	;
244EH		DIVU B0H,B4H	8C B4 B0	;
2451H		LD AOH,6008H	A1 08 60 A0	;
2455H		ST B2H,(AOH)	C2 A0 B2	;remainder at 6008H
2458H		ADDB AOH,02H	75 02 A0	;
245BH		ST B0H,(AOH)	C2 A0 B0	;quotient at 600AH
245EH		LJMP PHASE1	E7 0C 01	;
2461H	TEN9	JBC PO-5,TWEN1	35 0E 3D	;jump to TWEN1 if bit5 is set
2464H		LD 80H,8000H	A1 00 80 80	;determine phase-1 voltage
2468H		LD E6H,(80H)	A2 80 E6	; calibration factor, and
246BH		ADDB 80H,10H	75 10 80	; store at 6000H to 6003H
246EH		LD E0H,(80H)	A2 80 E0	;
2471H		ADDB 80H,02H	75 02 80	;
2474H		LD E2H,(80H)	A2 80 E2	;
2477H		ADDB 80H,02H	75 02 80	;
247AH		LD E4H,(80H)	A2 80 E4	;
247DH		CALL DIV	EF 72 13	;
2480H		CALL SQRT	EF 8A 13	;
2483H		LD AOH,C800H	A1 00 C8 A0	;
2487H		LD B0H,(AOH)	A2 A0 B0	;
248AH		LD AOH,C400H	A1 00 C4 A0	;
248EH		LD B2H,(AOH)	A2 A0 B2	;
2491H		DIVU B0H,B4H	8C B4 B0	;
2494H		LD AOH,6000H	A1 00 60 A0	;
2498H		ST B2H,(AOH)	C2 A0 B2	;remainder at 6000H
249BH		ADDB AOH,02H	75 02 A0	;
249EH		ST B0H,(AOH)	C2 A0 B0	;quotient at 6002H
24A1H	TWEN1	LJMP PHASE1	E7 C9 00	;
24A4H	TEN7	JBC PO-4,TWEN2	3C 0E 03	;jump to TWEN3 if bit4 of
24A7H		LJMP TWEN3	E7 83 00	; port0 is clear
24AAH	TWEN,	JBC PO-5,TWEN4	3D 0E 40	;jump to TWEN4 if bit5 is set
24ADH		LD 80H,8020H	A1 20 80 80	;determine phase-2 current
24B1H		LD E6H,(80H)	A2 80 E6	; calibration factor, and
24B4H		ADDB 80H,16H	75 16 80	; store at 6010H to 6013H
24B7H		LD E0H,(80H)	A2 80 E0	;

24BAH		ADDB 80H,02H	75 02 80	:
24BDH		LD E2H,(80H)	A2 80 E2	:
24COH		ADDB 80H,02H	75 02 80	:
24C3H		LD E4H,(80H)	A2 80 E4	:
24C6H		CALL DIV	EF 29 13	:
24C9H		CALL SQRT	EF 41 13	:
24CCH		LD A0H,C800H	A1 00 C8 A0	:
24DOH		LD B0H,(A0H)	A2 A0 B0	:
24D3H		LD A0H,C400H	A1 00 C4 A0	:
24D7H		LD B2H,(A0H)	A2 A0 B2	:
24DAH		DIVU B0H,B4H	8C B4 B0	:
24DDH		LD A0H,6010H	A1 10 60 A0	:
24E1H		ST B2H,(A0H)	C2 A0 B2	;remainder at 6010H
24E4H		ADDB A0H,02H	75 02 A0	:
24E7H		ST B0H,(A0H)	C2 A0 B0	;quotient at 6012H
24EAH		LJMP PHASE1	E7 80 00	:
24EDH	TWEN4	LD 80H,8040H	A1 40 80 80	;determine phase-3 current
24F1H		LD E6H,(80H)	A2 80 E6	; calibration factor, and
24F4H		ADDB 80H,16H	75 16 80	; store at 6014H to 6017H
24F7H		LD E0H,(80H)	A2 80 E0	:
24FAH		ADDB 80H,02H	75 02 80	:
24FDH		LD E2H,(80H)	A2 80 E2	:
2500H		ADDB 80H,02H	75 02 80	:
2503H		LD E4H,(80H)	A2 7F E4	:
2506H		CALL DIV	EF E9 12	:
2509H		CALL SQRT	EF 01 13	:
250CH		LD A0H,C800H	A1 00 C8 A0	:
2510H		LD B0H,(A0H)	A2 A0 B0	:
2513H		LD A0H,C400H	A1 00 C4 A0	:
2517H		LD B2H,(A0H)	A2 A0 B2	:
251AH		DIVU B0H,B4H	8C B4 B0	:
251DH		LD A0H,6014H	A1 14 60 A0	:
2521H		ST B2H,(A0H)	C2 A0 B2	;remainder at 6014H
2524H		ADDB A0H,02H	75 02 A0	:
2527H		ST B0H,(A0H)	C2 A0 B0	;quotient at 6016H
252AH		LJMP PHASE1	E7 40 00	:
252DH	TWEN3	JBC P0-5,TWEN5	35 0E 3D	;jump to TWEN5 if bit5 is set
2530H		LD 80H,8000H	A1 00 80 80	;determine phase-1 current
2534H		LD E6H,(80H)	A2 80 E6	; calibration factor, and
2537H		ADDB 80H,16H	75 16 80	; store at 600CH to 600FH
253AH		LD E0H,(80H)	A2 80 E0	:
253DH		ADDB 80H,02H	75 02 80	:
2540H		LD E2H,(80H)	A2 80 E2	:
2543H		ADDB 80H,02H	75 02 80	:
2546H		LD E4H,(80H)	A2 80 E4	:
2549H		CALL DIV	EF A6 12	:
254CH		CALL SQRT	EF BE 12	:
254FH		LD A0H,C800H	A1 00 C8 A0	:
2553H		LD B0H,(A0H)	A2 A0 B0	:
2556H		LD A0H,C400H	A1 00 C4 A0	:
255AH		LD B2H,(A0H)	A2 A0 B2	:
255DH		DIVU B0H,B4H	8C B4 B0	:

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2560H      LD A0H,600CH      A1 0C 60 A0      ;
2564H      ST B2H,(A0H)      C2 A0 B2      ;remainder at 600CH
2567H      ADDB A0H,02H      75 02 A0      ;
256AH      ST B0H,(A0H)      C2 A0 B0      ;quotient at 600EH

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PHASE ONE

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256DH  VOLTAGE1  LD 20H,8000H      A1 00 80 20      ;find RMS value of voltage in
2571H      LD E6H,(20H)      A2 20 E6      ; phase 1
2574H      ADDB 20H,10H      75 10 20      ;
2577H      LD E0H,(20H)      A2 20 E0      ;
257AH      ADDB 20H,02H      75 02 20      ;
257DH      LD E2H,(20H)      A2 20 E2      ;
2580H      ADDB 20H,02H      75 02 20      ;
2583H      LD E4H,(20H)      A2 20 E4      ;
2586H      CALL DIV          EF 69 12      ;
2589H      CALL SQRT         EF 81 12      ;
258CH      LD 70H,B4H        A0 B4 70      ;store RMS value for PF value
258FH      LD 22H,6000H      A1 00 60 22      ;multiply by phase-1 voltage
2593H      LD 24H,22H        A2 22 24      ; calibration factor
2596H      MULU 24H,B4H      6C B4 24      ;
2599H      ADDB 22H,02H      75 02 22      ;
259CH      LD 28H,22H        A2 22 28      ;
259FH      MULU 28H,B4H      6C B4 28      ;
25A2H      LD 24H,26H        A0 26 24      ;
25A5H      LD 26H,00H        A0 00 26      ;
25A8H      ADD 24H,28H        64 28 24      ;integer result is in 26H, and
25ABH      ADDC 26H,2AH      A4 2A 26      ; fraction result is in 24H
25AEH      LD 20H,8060H      A1 60 80 20      ;store values for calculation
25B2H      ST 24H,(20H)      C2 20 24      ; of apparent power and
25B5H      ADDB 20H,02H      75 02 20      ; average voltage
25B8H      ST 26H,(20H)      C2 20 26      ;
25BBH      LD 80H,24H        A0 24 80      ;
25BEH      LD 82H,26H        A0 26 82      ;
25C1H      LD C2H,00H        A0 00 C2      ;
25C4H      LD C0H,26H        A0 26 C0      ;
25C7H      LD C4H,24H        A0 24 C4      ;
25CAH      LD C6H,9020H      A1 20 90 C6      ;
25CEH      LD C8H,2E56H      A1 56 2E C8      ;
25D2H      CALL DISPIN      EF 21 13      ;put voltage in display RAM
25D5H  CURRENT1  LD 20H,8000H      A1 00 80 20      ;find RMS value of current in
25D9H      LD E6H,(20H)      A2 20 E6      ; phase 2
25DCH      ADDB 20H,16H      75 16 20      ;
25DFH      LD E0H,(20H)      A2 20 E0      ;
25E2H      ADDB 20H,02H      75 02 20      ;
25E5H      LD E2H,(20H)      A2 20 E2      ;
25E8H      ADDB 20H,02H      75 02 20      ;
25FBH      LD E4H,(20H)      A2 20 E4      ;
25FEH      CALL DIV          EF 01 12      ;
25F1H      CALL SQRT         EF 19 12      ;
25F4H      LD 72H,B4H        A0 B4 72      ;store RMS value for PF value

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25F7H      LD 22H,600CH      A1 0C 60 22      ;multiply by phase-1 current
25FBH      LD 24H,22H       A2 22 24      ; calibration factor
25FEH      MULU 24H,B4H     6C B4 24      ;
2601H      ADDB 22H,02H     75 02 22      ;
2604H      LD 28H,22H       A2 22 28      ;
2607H      MULU 28H,B4H     6C B4 28      ;
260AH      LD 24H,26H       A0 26 24      ;
260DH      LD 26H,00H       A0 00 26      ;
2610H      ADD 24H,28H      64 28 24      ;integer result is in 26H, and
2613H      ADDC 26H,2AH     A4 2A 26      ; fraction result is in 24H
2616H      LD 20H,8064H     A1 64 80 20      ;store values for calculation
261AH      ST 24H,(20H)     C2 20 24      ; of apparent power and
261DH      ADDB 20H,02H     75 02 20      ; average current
2620H      ST 26H,(20H)     C2 20 26      ;
2623H      LD 86H,24H       A0 24 86      ;
2626H      LD 88H,26H       A0 26 88      ;
2629H      LD C2H,00H       A0 00 C2      ;
262CH      LD C0H,26H       A0 26 C0      ;
262FH      LD C4H,24H       A0 24 C4      ;
2632H      LD C6H,9060H     A1 60 90 C6      ;
2636H      LD C8H,2E41H     A1 41 2E C8      ;
263AH      CALL DISPIN      EF B9 12      ;put current in display RAM
263DH      APP.POW.1 LD 84H,00H     A0 00 84      ;determine apparent power =
2640H      CALL MUL         EF EC 15      ; (VRMS*IRMS)/1000 (KW)
2643H      LD E0H,B2H       A0 B2 E0      ;
2646H      LD E2H,B4H       A0 B4 E2      ;
2649H      LD E4H,B6H       A0 B6 E4      ;
264CH      LD E6H,03E8H     A1 E8 03 E6      ;
2650H      CALL DIV         EF 9F 11      ;
2653H      ADDB E8H,01H     75 01 E8      ;correct roundoff error
2656H      LD 20H,8068H     A1 68 80 20      ;store values for calculation
265AH      ST E8H,(20H)     C2 20 E8      ; of active power, 15-Min.
265DH      LD 30H,A000H     A1 00 A0 30      ; Demand, and average
2661H      ST E8H,(30H)     C2 30 E8      ; apparent power
2664H      ADDB 20H,02H     75 02 20      ;
2667H      ST EAH,(20H)     C2 20 EA      ;
266AH      ADDB 30H,02H     75 02 30      ;
266DH      ST EAH,(30H)     C2 30 EA      ;
2670H      LD 80H,E8H       A0 E8 80      ;
2673H      LD 82H,EAH       A0 EA 82      ;
2676H      LD 84H,00H       A0 00 84      ;
2679H      LD C4H,E8H       A0 E8 C4      ;
267CH      LD C0H,EAH       A0 EA C0      ;
267FH      LD C2H,00H       A0 00 C2      ;
2682H      LD C6H,90A0H     A1 A0 90 C6      ;
2686H      LD C8H,574BH     A1 4B 57 C8      ;
268AH      CALL DISPIN      EF 69 12      ;
268DH      P.FACTOR1 LD 20H,8000H     A1 00 80 20      ;determine power factor
2691H      LD E6H,(20H)     A2 20 E6      ;
2694H      ADDB 20H,0AH     75 0A 20      ;
2697H      LD E0H,(20H)     A2 20 E0      ;
269AH      ADDB 20H,02H     75 02 20      ;

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269DH	LD E2H,(20H)	A2 20 E2	:
26A0H	ADDB 20H,02H	75 02 20	:
26A3H	LD E4H,(20H)	A2 20 E4	:
26A6H	CALL DIV	EF 49 11	:
26A9H	DIVU E8H,70H	8C 70 E8	:
26ACH	LD E4H,00H	A0 00 E4	:
26AFH	LD E2H,E8H	A0 E8 E2	:
26B2H	LD E0H,EAH	A0 EA E0	:
26B5H	LD E6H,72H	A0 72 E6	:
26B8H	CALL DIV	EF 37 11	:
26BBH	CMP EAH,0001H	89 01 00 EA	;if integer value is not zero
26BFH	JE NOT10.1	DF 08	; or one, make equal to zero
26C1H	CMP EAH,00H	88 00 EA	:
26C4H	JE NOT10.1	DF 0C	:
26C6H	LD EAH,00H	A0 00 EA	:
26C9H	NOT10.1 LD 20H,806CH	A1 6C 80 20	;store values for calculation
26CDH	ST E8H,(20H)	C2 20 E8	; of active power and average
26DOH	ADDB 20H,02H	75 02 20	; power factor
26D3H	ST EAH,(20H)	C2 20 EA	:
26D6H	LD 86H,E8H	A0 E8 86	:
26D9H	LD 88H,EAH	A0 EA 88	:
26DCH	LD C2H,00H	A0 00 C2	:
26DFH	LD C0H,EAH	A0 EA C0	:
26E2H	LD C4H,E8H	A0 E8 C4	:
26E5H	LD C6H,9120H	A1 20 91 C6	:
26E9H	LD C8H,2020H	A1 20 20 C8	:
26EDH	CALL DISPIN	EF 06 12	:
26F0H	JBC PO-6,P.F.21	36 0E 7F	;for asynchronous sampling
26F3H	LD 20H,8004H	A1 04 80 20	; only: if the current is
26F7H	LD E6H,(20H)	A2 20 E6	; leading the voltage by 1
26FAH	ADDB 20H,04H	75 04 20	; to 127 samples, display
26FDH	LD E8H,(20H)	A2 20 E8	; CAP.; if the current is
2700H	CMP E6H,E8H	88 E8 E6	; lagging the voltage by 1
2703H	JE P.F.21	DF 6D	; to 127 samples, display
2705H	CLRC	F8	; IND.; if the current is
2706H	CMP E6H,E8H	88 E8 E6	; leading the voltage by 0
2709H	JC P.F.11	DB 3B	; or 128 samples, do not
270BH	CLRC	F8	; display CAP. or IND.
270CH	SUB E8H,E6H	68 E6 E8	:
270FH	CMP E8H,0080H	89 80 00 E8	:
2713H	JE P.F.21	DF 5D	:
2715H	JC P.F.11	DB 2F	:
2717H	LD 20H,9130H	A1 30 91 20	:
271RH	LD 30H,0049H	A1 49 00 30	:
271FH	ST 30H,(20H)	C2 20 30	:
2722H	LD 20H,9132H	A1 32 91 20	:
2726H	LD 30H,004EH	A1 4E 00 30	:
272AH	ST 30H,(20H)	C2 20 30	:
272DH	LD 20H,9134H	A1 34 91 20	:
2731H	LD 30H,0044H	A1 44 00 30	:
2735H	ST 30H,(20H)	C2 20 30	:
2738H	LD 20H,9136H	A1 36 91 20	:

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273CH      LD 30H,002EH      A1 2E 00 30      :
2740H      ST 30H,(20H)      C2 20 30      :
2743H      LJMP P.F.21      E7 2C 00      :
2746H      P.F.11      LD 20H,9130H      A1 30 91 20      :
274AH      LD 30H,0043H      A1 43 00 30      :
274EH      ST 30H,(20H)      C2 20 30      :
2751H      LD 20H,9132H      A1 32 91 20      :
2755H      LD 30H,0041H      A1 41 00 30      :
2759H      ST 30H,(20H)      C2 20 30      :
275CH      LD 20H,9134H      A1 34 91 20      :
276CH      LD 30H,0050H      A1 50 00 30      :
2764H      ST 30H,(20H)      C2 20 30      :
2767H      LD 20H,9136H      A1 36 91 20      :
276BH      LD 30H,002EH      A1 2E 00 30      :
276FH      ST 30H,(20H)      C2 20 30      :
2772H      P.F.21      LD 20H,801CH      A1 1C 80 20      :if active power is positive,
2776H      LD E6H,(20H)      A2 20 E6      : add '+' to power factor; if
2779H      CLRC      F8      : active power is negative,
277AH      CMP 00H,E6H      88 E6 00      : add '-' to power factor
277DH      JC P.F.31      DB 0E      :
277FH      LD 20H,9120H      A1 20 91 20      :
2783H      LD 30H,002DH      A1 2D 00 30      :
2787H      ST 30H,(20H)      C2 20 30      :
278AH      LJMP ACT.POW.1      E7 0B 00      :
278DH      P.F.31      LD 20H,9120H      A1 20 91 20      :
2791H      LD 30H,002BH      A1 2B 00 30      :
2795H      ST 30H,(20H)      C2 20 30      :
2798H      ACT.POW.1      CALL MUL      EF 94 14      :determine active power =
279BH      LD 20H,8070H      A1 70 80 20      : (P.FACTOR)*(APP.POW.)
279FH      ST B2H,(20H)      C2 20 B2      :store values for calculation
27A2H      ADDB 20H,02H      75 02 20      : of power consumption and
27A5H      ST B4H,(20H)      C2 20 B4      : average active power
27A8H      LD 30H,B2H      A0 B2 30      :
27ABH      LD 32H,B4H      A0 B4 32      :
27AEH      LD 34H,00H      A0 00 34      :
27B1H      LD C4H,B2H      A0 B2 C4      :
27B4H      LD C0H,B4H      A0 B4 C0      :
27B7H      LD C2H,B6H      A0 B6 C2      :
27BAH      LD C6H,90E0H      A1 E0 90 C6      :
27BEH      LD C8H,574BH      A1 4B 57 C8      :
27C2H      CALL DISPIN      EF 31 11      :
27C5H      LD 20H,801CH      A1 1C 80 20      :if active power is positive,
27C9H      LD E6H,(20H)      A2 20 E6      : add '+' to display; if
27CCH      CLRC      F8      : active power is negative,
27CDH      CMP 00H,E6H      88 E6 00      : add '-' to display
27D0H      JC A.P.11      DB 0E      :
27D2H      LD 20H,90E0H      A1 E0 90 20      :
27D6H      LD 30H,002DH      A1 2D 00 30      :
27DAH      ST 30H,(20H)      C2 20 30      :
27DDH      LJMP FREQ.1      E7 0B 00      :
27E0H      A.P.11      LD 20H,90E0H      A1 E0 90 20      :
27E4H      LD 30H,002BH      A1 2B 00 30      :

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27FBH      ST 30H,(20H)      C2 20 30      ;
27EBH  FREQ.1  LD 20H,8002H    A1 02 80 20    ;determine input frequency
27EFH      CMP 20H,00H      8A 20 00      ;
27F2H      JE TWEN71        DF 69        ;
27F4H      JBS PO-6,FREQ.21 3E 0E 1B      ;if pin 6 of PORT0 (connected
27F7H      LDB 40H,0CH      B1 0C 40      ; to SYNCH/ASYNCH switch) is
27FAH      LD 20H,9160H     A1 60 91 20    ; set, jump to FREQ.21; else,
27FEH      LD 30H,0020H     A1 20 00 30    ; load FREQ. memory addresses
2802H  FREQ.11 ST 30H,(20H)    C2 20 30    ; with 20H (blank)
2805H      ADDB 20H,02H     75 02 20      ;
2808H      DECB 40H        15 40         ;
280AH      CMPB 40H,00H     98 00 40      ;
280DH      JGT FREQ.11      D2 F3        ;
280FH      LJMP POW.CON.1   E7 6C 00      ;
2812H  FREQ.21 LD E0H,7502H    A1 02 75 E0  ;if alternating input,
2816H      MULU E0H,3CH     6D 3C 00 E0    ; determine input frequency
281AH      LD 24H,8000H     A1 00 80 24    ;
281EH      LD E6H,(24H)     A2 24 E6      ;
2821H      LD E4H,E2H       A0 E2 E4      ;
2824H      LD E2H,E0H       A0 E0 E2      ;
2827H      LD E0H,00H       A0 00 E0      ;
282AH      CALL DIV         EF C5 0F      ;
282DH      LD 50H,8074H     A1 74 80 50    ;store values for calculation
2831H      ST E8H,(50H)     C2 50 E8      ; of average frequency
2834H      ADDB 50H,02H     75 02 50      ;
2837H      ST EAH,(50H)     C2 50 EA      ;
283AH      LD 54H,80FEH     A1 FE 80 54    ;
283EH      LD 52H,(54H)     A2 54 52      ;
2841H      INCB 52H         17 52         ;
2843H      ST 52H,(54H)     C2 54 52      ;
2846H      LD C4H,E8H       A0 E8 C4      ;
2849H      LD C0H,EAH       A0 EA C0      ;
284CH      LD C2H,00H       A0 00 C2      ;
284FH      LD C6H,9160H     A1 60 91 C6    ;
2853H      LD C8H,5A48H     A1 48 5A C8    ;
2857H      CALL DISPIN      EF 9C 10      ;
285AH      LJMP POW.CON.1   E7 21 00      ;
285DH  TWEN71 LD 50H,8074H     A1 74 80 50  ;if non-alternating input
2861H      ST 00H,(50H)     C2 50 00      ;
2864H      ADDB 50H,02H     75 02 50      ;
2867H      ST 00H,(50H)     C2 50 00      ;
286AH      LD C2H,00H       A0 00 C0      ;
286DH      LD C0H,00H       A0 00 C2      ;
2870H      LD C4H,00H       A0 00 C4      ;
2873H      LD C6H,9160H     A1 60 91 C6    ;
2877H      LD C8H,5A48H     A1 48 5A C8    ;
287BH      CALL DISPIN      EF 78 10      ;
287EH  POW.CON.1 LD 20H,601AH  A1 1A 60 20  ;add active power of this
2882H      LD 86H,(20H)     A2 20 86      ; cycle to running hourly
2885H      ADDB 20H,02H     75 02 20      ; total for phase 1 at
2888H      LD 88H,(20H)     A2 20 88      ; 601AH to 601FH
288BH      ADDB 20H,02H     75 02 20      ;

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288EH	LD 8AH,(20H)	A2 20 8A	:
2891H	ADD 86H,30H	64 30 86	:
2894H	ADDC 88H,32H	A4 32 88	:
2897H	ADDC 8AH,34H	A4 34 8A	:
289AH	ST 8AH,(20H)	C2 20 8A	:
289DH	SUBB 20H,02H	79 02 20	:
28A0H	ST 88H,(20H)	C2 20 88	:
28A3H	SUBB 20H,02H	79 02 20	:
28A6H	ST 86H,(20H)	C2 20 86	:
28A9H	SUBB 20H,02H	79 02 20	:
28ACH	LD 8EH,(20H)	A2 20 8E	:
28AFH	INC 8EH	07 8E	;increment counter at 6018H
28B1H	ST 8EH,(20H)	C2 20 8E	:
28B4H	CMP 8EH,0708H	89 08 07 8E	;compare counter to 1800D, and
28B8H	JNE NONSTORE1	D7 5B	; if equal, go to STORE
28BAH	STORE1 LD E6H,(20H)	A2 20 E6	;divide power stored over the
28BDH	ADDB 20H,02H	75 02 20	; last hour by 1800D to
28COH	LD E0H,(20H)	A2 20 E0	; obtain average value
28C3H	ADDB 20H,02H	75 02 20	:
28C6H	LD E2H,(20H)	A2 20 E2	:
28C9H	ADDB 20H,02H	75 02 20	:
28CCH	LD E4H,(20H)	A2 20 E4	:
28CFH	CALL DIV	EF 20 0F	:
28D2H	ADDB E8H,01H	75 01 E8	;correct roundoff error
28D5H	LD 30H,6020H	A1 20 60 30	;load previous value of power
28D9H	LD 70H,(30H)	A2 30 70	; consumed
28DCH	ADDB 30H,02H	75 02 30	:
28DFH	LD 72H,(30H)	A2 30 72	:
28E2H	ADDB 30H,02H	75 02 30	:
28E5H	LD 74H,(30H)	A2 30 74	:
28E8H	ADD 70H,E8H	64 E8 70	;add total power over last
28EBH	ADDC 72H,EAH	A4 EA 72	; hour to total power
28EEH	ADDC 74H,00H	A4 00 74	; consumption
28F1H	ST 74H,(30H)	C2 30 74	;store total power consumption
28F4H	SUBB 30H,02H	79 02 30	:
28F7H	ST 72H,(30H)	C2 30 72	:
28FAH	SUBB 30H,02H	79 02 30	:
28FDH	ST 70H,(30H)	C2 30 70	:
2900H	ST 00H,(20H)	C2 20 00	;zero running hourly total and
2903H	SUBB 20H,02H	79 02 20	; counter
2906H	ST 00H,(20H)	C2 20 00	:
2909H	SUBB 20H,02H	79 02 20	:
290CH	ST 00H,(20H)	C2 20 00	:
290FH	SUBB 20H,02H	79 02 20	:
2912H	ST 00H,(20H)	C2 20 00	:
2915H	NONSTORE1 LD 30H,6020H	A1 20 60 30	;load previous value of power
2919H	LD C4H,(30H)	A2 30 C4	; consumed
291CH	ADDB 30H,02H	75 02 30	:
291FH	LD C0H,(30H)	A2 30 C0	:
2922H	ADDB 30H,02H	75 02 30	:
2925H	LD C2H,(30H)	A2 30 C2	:
2928H	LD 20H,601AH	A1 1A 60 20	;load running total of power

292CH	LD E0H,(20H)	A2 20 E0	; consumption
292FH	ADDB 20H,02H	75 02 20	;
2932H	LD E2H,(20H)	A2 20 E2	;
2935H	ADDB 20H,02H	75 02 20	;
2938H	LD E4H,(20H)	A2 20 E4	;
293BH	LD E6H,0708H	A1 08 07 E6	;
293FH	CALL DIV	EF 80 0E	;divide running total by 1800D
2942H	ADDB E8H,01H	75 01 E8	;correct roundoff error
2945H	ADD C4H,E8H	64 E8 C4	;add running value of power
2948H	ADDC C0H,EAH	A4 EA C0	; consumed to previous total
294BH	ADDC C2H,00H	A4 00 C2	;
294EH	LD 20H,8078H	A1 78 80 20	;store values for calculation
2952H	ST C4H,20H	C2 20 C4	; of total power consumption
2955H	ADDB 20H,02H	75 02 20	;
2958H	ST C0H,20H	C2 20 C0	;
295BH	ADDB 20H,02H	75 02 20	;
295EH	ST C2H,20H	C2 20 C2	;
2961H	LD C6H,91A0H	A1 A0 91 C6	;
2965H	LD C8H,484BH	A1 4B 48 C8	;
2969H	CALL DISPIN	EF 8A 0F	;
296CH	KW.DEM.1 LD 20H,A000H	A1 00 A0 20	;load registers from 15-Min.
2970H	LD 30H,(20H)	A2 20 30	; Demand RAM for calculation
2973H	LD 50H,(20H)	A2 20 50	; of 15-Min. Demand. Current
2976H	ADDB 20H,02H	75 02 20	; V.I value is in registers
2979H	LD 32H,(20H)	A2 20 32	; 30H,32H and 50H,52H
297CH	LD 52H,(20H)	A2 20 52	;
297FH	ADDB 20H,02H	75 02 20	;
2982H	LD 34H,(20H)	A2 20 34	;15-Min. Demand addr. register
2985H	ADDB 20H,02H	75 02 20	; is in register 34H
2988H	LD 36H,(20H)	A2 20 36	;current 15-Min. Demand total
298BH	ADDB 20H,02H	75 02 20	; V.I is in registers 36H,
298EH	LD 38H,(20H)	A2 20 38	; 38H,3AH
2991H	ADDB 20H,02H	75 02 20	;
2994H	LD 3AH,(20H)	A2 20 3A	;
2997H	LD 40H,(34H)	A2 34 40	;oldest V.I value is in
299AH	ADDB 34H,02H	75 02 34	; registers 40H,42H
299DH	LD 42H,(34H)	A2 34 42	;
29A0H	ADD 36H,30H	64 30 36	;calculate new 15-Min. Demand
29A3H	ADDC 38H,32H	A4 32 38	; total V.I by subtracting
29A6H	ADDC 3AH,00H	A4 00 3A	; oldest V.I value and adding
29A9H	SUB 36H,40H	68 40 36	; current V.I value
29ACH	SUBC 38H,42H	A8 42 38	;
29AFH	SUBC 3AH,00H	A8 00 3A	;
29B2H	ST 3AH,(20H)	C2 20 3A	;store new 15-Min. Demand
29B5H	SUBB 20H,02H	79 02 20	; total
29B8H	ST 38H,(20H)	C2 20 38	;
29BBH	SUBB 20H,02H	79 02 20	;
29BEH	ST 36H,(20H)	C2 20 36	;
29C1H	SUBB 20H,02H	79 02 20	;
29C4H	ST 52H,(34H)	C2 34 52	;replace oldest V.I value with
29C7H	SUBB 34H,02H	79 02 34	; current V.I value
29CAH	ST 50H,(34H)	C2 34 50	;

29CDH		LD 56H,36H	A0 36 56	;compare new 15-Min. Demand
29DOH		LD 58H,38H	A0 38 58	; total with maximum 15-Min.
29D3H		LD 5AH,3AH	A0 3A 5A	; Demand total, and store the
29D6H		LD 20H,6058H	A1 58 60 20	; larger value as the new
29DAH		LD 40H,(20H)	A2 20 40	; maximum 15-Min. Demand
29DDH		LD 50H,(20H)	A2 20 50	; total
29EOH		ADDB 20H,02H	75 02 20	;
29E3H		LD 42H,(20H)	A2 20 42	;
29E6H		LD 52H,(20H)	A2 20 52	;
29E9H		ADDB 20H,02H	75 02 20	;
29ECH		LD 44H,(20H)	A2 20 44	;
29EFH		LD 54H,(20H)	A2 20 54	;
29F2H		SUB 36H,40H	68 40 36	;
29F5H		SUBC 38H,42H	A8 42 38	;
29F8H		SUBC 3AH,44H	A8 44 3A	;
29FBH		JC KW.DEM.11	DB 12	;
29FDH		ST 54H,(20H)	C2 20 54	;
2A00H		SUBB 20H,02H	79 02 20	;
2A03H		ST 52H,(20H)	C2 20 52	;
2A06H		SUBB 20H,02H	79 02 20	;
2A09H		ST 50H,(20H)	C2 20 50	;
2A0CH		LJMP KW.DEM.21	E7 0F 00	;
2AOFH	KW.DEM.11	ST 5AH,(20H)	C2 20 5A	;
2A12H		SUBB 20H,02H	79 02 20	;
2A15H		ST 58H,(20H)	C2 20 58	;
2A18H		SUBB 20H,02H	79 02 20	;
2A1BH		ST 56H,(20H)	C2 20 56	;
2A1EH	KW.DEM.21	LD E0H,(20H)	A2 20 E0	;divide maximum 15-Min. Demand
2A21H		ADDB 20H,02H	75 02 20	; total by 450 to obtain
2A24H		LD E2H,(20H)	A2 20 E2	; value for 15-Min. Demand
2A27H		ADDB 20H,02H	75 02 20	; display
2A2AH		LD E4H,(20H)	A2 20 E4	;
2A2DH		LD E6H,01C2H	A1 C2 01 r6	;
2A31H		CALL DIV	EF BE 0D	;
2A34H		ADD 34H,0004H	65 04 00 34	;increment address pointer to
2A38H		CHP 34H,A728H	89 28 A7 34	; next oldest V.I value
2A3CH		JNE KW.DEM.31	D7 04	;
2A3EH		SUB 34H,0708H	69 08 07 34	;
2A42H	KW.DEM.31	LD 20H,A004H	A1 04 A0 20	;
2A46H		ST 34H,(20H)	C2 20 34	;
2A49H		LD C2H,00H	A0 00 C2	;display 15-Min. Demand value
2A4CH		LD C0H,EAH	A0 EA C0	;
2A4FH		LD C4H,E8H	A0 E8 C4	;
2A52H		LD C6H,91E0H	A1 E0 91 C6	;
2A56H		LD C8H,574BH	A1 4B 57 C8	;
2A5AH		CALL DISPIN	EF 99 0E	;

PHASE TWO

2A5DH	VOLTAGE2	LD 20H,8020H	A1 20 80 20	;find RMS value of voltage in
2A61H		LD E6H,(20H)	A2 20 E6	; phase 2
2A64H		ADDB 20H,10H	75 10 20	;

2A67H	LD E0H,(20H)	A2 20 E0	:
2A6AH	ADDB 20H,02H	75 02 20	:
2A6DH	LD E2H,(20H)	A2 20 E2	:
2A70H	ADDB 20H,02H	75 02 20	:
2A73H	LD E4H,(20H)	A2 20 E4	:
2A76H	CALL DIV	EF 79 0D	:
2A79H	CALL SQRT	EF 91 0D	:
2A7CH	LD 70H,B4H	A0 B4 70	;store RMS value for PF value
2A7FH	LD 22H,6004H	A1 04 60 22	;multiply by phase-2 voltage
2A83H	LD 24H,22H	A2 22 24	; calibration factor
2A86H	MULU 24H,B4H	6C B4 24	:
2A89H	ADDB 22H,02H	75 02 22	:
2A8CH	LD 28H,22H	A2 22 28	:
2A8FH	MULU 28H,B4H	6C B4 28	:
2A92H	LD 24H,26H	A0 26 24	:
2A95H	LD 26H,00H	A0 00 26	:
2A98H	ADD 24H,28H	64 28 24	;integer result is in 26H, and
2A9BH	ADDC 26H,2AH	A4 2A 26	; fraction result is in 24H
2A9EH	LD 20H,8080H	A1 80 80 20	;store values for calculation
2AA2H	ST 24H,(20H)	C2 20 24	; of apparent power and
2AA5H	ADDB 20H,02H	75 02 20	; average voltage
2AA8H	ST 26H,(20H)	C2 20 26	:
2AABH	LD 80H,24H	A0 24 80	:
2AAEH	LD 82H,26H	A0 26 82	:
2AB1H	LD C2H,00H	A0 00 C2	:
2AB4H	LD C0H,26H	A0 26 C0	:
2AB7H	LD C4H,24H	A0 24 C4	:
2ABAH	LD C6H,9220H	A1 20 92 C6	:
2ABEH	LD C8H,2E56H	A1 56 2E C8	:
2AC2H	CALL DISPIN	EF 31 0E	;put voltage in display RAM
2AC5H	CURRENT2 LD 20H,8020H	A1 20 80 20	;find RMS value of current in
2AC9H	LD E6H,(20H)	A2 20 E6	; phase 2
2ACC	ADDB 20H,16H	75 16 20	:
2ACFH	LD E0H,(20H)	A2 20 E0	:
2AD2H	ADDB 20H,02H	75 02 20	:
2AD5H	LD E2H,(20H)	A2 20 E2	:
2AD8H	ADDB 20H,02H	75 02 20	:
2ADB	LD E4H,(20H)	A2 20 E4	:
2ADEH	CALL DIV	EF 11 0D	:
2AE1H	CALL SQRT	EF 29 0D	:
2AE4H	LD 72H,B4H	A0 B4 72	;store RMS value for PF value
2AE7H	LD 22H,6010H	A1 10 60 22	;multiply by phase-2 current
2AE9H	LD 24H,22H	A2 22 24	; calibration factor
2AECH	MULU 24H,B4H	6C B4 24	:
2AF1H	ADDB 22H,02H	75 02 22	:
2AF4H	LD 28H,22H	A2 22 28	:
2AF7H	MULU 28H,B4H	6C B4 28	:
2AF9H	LD 24H,26H	A0 26 24	:
2AFDH	LD 26H,00H	A0 00 26	:
2B00H	ADD 24H,28H	64 28 24	;integer result is in 26H, and
2B03H	ADDC 26H,2AH	A4 2A 26	; fraction result is in 24H
2B06H	LD 20H,8084H	A1 84 80 20	;store values for calculation

2B0AH	ST 24H,(20H)	C2 20 24	; of apparent power and
2B0DH	ADDB 20H,02H	75 02 20	; average current
2B10H	ST 26H,(20H)	C2 20 26	;
2B13H	LD 86H,24H	A0 24 86	;
2B16H	LD 88H,26H	A0 26 88	;
2B19H	LD C2H,00H	A0 00 C2	;
2B1CH	LD C0H,26H	A0 26 C0	;
2B1FH	LD C4H,24H	A0 24 C4	;
2B22H	LD C6H,9260H	A1 60 92 C6	;
2B26H	LD C8H,2E41H	A1 41 2E C8	;
2B2AH	CALL DISPIN	EF C9 0D	;put current in display RAM
2B2DH	APP.POW.2 LD 84H,00H	A0 00 84	;determine apparent power
2B30H	CALL MUL	EF FC 10	; (VRMS*IRMS)/1000 (KW)
2B33H	LD E0H,B2H	A0 B2 E0	;
2B36H	LD E2H,B4H	A0 B4 E2	;
2B39H	LD E4H,B6H	A0 B6 E4	;
2B3CH	LD E6H,03E8H	A1 E8 03 E6	;
2B40H	CALL DIV	EF AF 0C	;
2B43H	ADDB E8H,01H	75 01 E8	;correct roundoff error
2B46H	LD 20H,8088H	A1 88 80 20	;store values for calculation
2B4AH	ST E8H,(20H)	C2 20 E8	; of active power, 15-Min.
2B4DH	LD 30H,A800H	A1 00 A8 30	; Demand, and average
2B51H	ST E8H,(30H)	C2 30 E8	; apparent power
2B54H	ADDB 20H,02H	75 02 20	;
2B57H	ST EAH,(20H)	C2 20 EA	;
2B5AH	ADDB 30H,02H	75 02 30	;
2B5DH	ST EAH,(30H)	C2 30 EA	;
2B60H	LD 80H,E8H	A0 E8 80	;
2B63H	LD 82H,EAH	A0 EA 82	;
2B66H	LD 84H,00H	A0 00 84	;
2B69H	LD C4H,E8H	A0 E8 C4	;
2B6CH	LD C0H,EAH	A0 EA C0	;
2B6FH	LD C2H,00H	A0 00 C2	;
2B72H	LD C6H,92A0H	A1 A0 92 C6	;
2B76H	LD C8H,574BH	A1 4B 57 C8	;
2B7AH	CALL DISPIN	EF 79 0D	;
2B7DH	P.FACTOR2 LD 20H,8020H	A1 20 80 20	;determine power factor
2B81H	LD E6H,(20H)	A2 20 E6	;
2B84H	ADDB 20H,0AH	75 0A 20	;
2B87H	LD E0H,(20H)	A2 20 E0	;
2B8AH	ADDB 20H,02H	75 02 20	;
2B8DH	LD E2H,(20H)	A2 20 E2	;
2B90H	ADDB 20H,02H	75 02 20	;
2B93H	LD E4H,(20H)	A2 20 E4	;
2B96H	CALL DIV	EF 59 0C	;
2B99H	DIVU E8H,70H	8C 70 E8	;
2B9CH	LD E4H,00H	A0 00 E4	;
2B9FH	LD E2H,E8H	A0 E8 E2	;
2BA2H	LD E0H,EAH	A0 EA E0	;
2BA5H	LD E6H,72H	A0 72 E6	;
2BA8H	CALL DIV	EF 47 0C	;
2BABH	CMP EAH,0001H	89 01 00 EA	;if integer value is not zero

2BAFH	JE NOT10.2	DF 08	; or one, make equal to zero
2BB1H	CMP EAH,00H	88 00 EA	;
2BB4H	JE NOT10.2	DF 03	;
2BB6H	LD EAH,00H	A0 00 EA	;
2BB9H	NOT10.2 LD 20H,808CH	A1 8C 80 20	;store values for calculation
2BBDH	ST E8H,(20H)	C2 20 E8	; of active power and average
2BC0H	ADDB 20H,02H	75 02 20	; power factor
2BC3H	ST EAH,(20H)	C2 20 EA	;
2BC6H	LD 86H,E8H	A0 E8 86	;
2BC9H	LD 88H,EAH	A0 EA 88	;
2BCCH	LD C2H,00H	A0 00 C2	;
2BCFH	LD C0H,EAH	A0 EA C0	;
2BD2H	LD C4H,E8H	A0 E8 C4	;
2BD5H	LD C6H,9320H	A1 20 93 C6	;
2BD9H	LD C8H,2020H	A1 20 20 C8	;
2BDDH	CALL DISPIN	EF 16 0D	;for asynchronous sampling
2BE0H	JBC P0-6,P.F.22	36 0E 7F	; only: if the current is
2BE3H	LD 20H,8024H	A1 24 80 20	; leading the voltage by 1
2BE7H	LD E6H,(20H)	A2 20 E6	; to 127 samples, display
2BEAH	ADDB 20H,04H	75 04 20	; CAP.; if the current is
2BEDH	LD E8H,(20H)	A2 20 E8	; lagging the voltage by 1
2BFOH	CMP E6H,E8H	88 E8 E6	; to 127 samples, display
2BF3H	JE P.F.22	DF 6D	; IND.; if the current is
2BF5H	CLRC	F8	; leading the voltage by 0
2BF6H	CMP E6H,E8H	88 E8 E6	; or 128 samples, do not
2BF9H	JC P.F.12	DB 3B	; display CAP. or IND.
2BFBH	CLRC	F8	;
2BFCH	SUB E8H,E6H	68 E6 E8	;
2BFFH	CMP E8H,0080H	89 80 00 E8	;
2C03H	JE P.F.22	DF 5D	;
2C05H	JC P.F.12	DB 2F	;
2C07H	LD 20H,9330H	A1 30 93 20	;
2C08H	LD 30H,0049H	A1 49 00 30	;
2C0FH	ST 30H,(20H)	C2 20 30	;
2C12H	LD 20H,9332H	A1 32 93 20	;
2C16H	LD 30H,004EH	A1 4E 00 30	;
2C1AH	ST 30H,(20H)	C2 20 30	;
2C1DH	LD 20H,9334H	A1 34 93 20	;
2C21H	LD 30H,0044H	A1 44 00 30	;
2C25H	ST 30H,(20H)	C2 20 30	;
2C28H	LD 20H,9336H	A1 36 93 20	;
2C2CH	LD 30H,002EH	A1 2E 00 30	;
2C30H	ST 30H,(20H)	C2 20 30	;
2C33H	LJMP P.F.22	E7 2C 00	;
2C36H	P.F.12 LD 20H,9330H	A1 30 93 20	;
2C3AH	LD 30H,0043H	A1 43 00 30	;
2C3FH	ST 30H,(20H)	C2 20 30	;
2C41H	LD 20H,9332H	A1 32 93 20	;
2C45H	LD 30H,0041H	A1 41 00 30	;
2C49H	ST 30H,(20H)	C2 20 30	;
2C4CH	LD 20H,9334H	A1 34 93 20	;
2C50H	LD 30H,0050H	A1 50 00 30	;

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2C54H      ST 30H,(20H)      C2 20 30      ;
2C57H      LD 20H,9336H      A1 36 93 20      ;
2C5BH      LD 30H,002EH      A1 2E 00 30      ;
2C5FH      ST 30H,(20H)      C2 20 30      ;
2C62H      P.F.22      LD 20H,803CH      A1 3C 80 20      ;if active power is positive,
2C66H      LD E6H,(20H)      A2 20 E6      ; add '+' to power factor; if
2C69H      CLRC              F8              ; active power is negative,
2C6AH      CMP 00H,E6H        88 E6 00      ; add '-' to power factor
2C6DH      JC P.F.32          DB 0E          ;
2C6FH      LD 20H,9320H      A1 20 93 20      ;
2C73H      LD 30H,002DH      A1 2D 00 30      ;
2C77H      ST 30H,(20H)      C2 20 30      ;
2C7AH      LJMP ACT.POW.2     E7 0B 00      ;
2C7DH      P.F.32      LD 20H,9320H      A1 20 93 20      ;
2C81H      LD 30H,002BH      A1 2B 00 30      ;
2C85H      ST 30H,(20H)      C2 20 30      ;
2C88H      ACT.POW.2      CALL MUL        EF A4 0F      ;determine active power =
2C8BH      LD 20H,8090H      A1 90 80 20      ; (t.FACTOR)*(APP.POW.)
2C8FH      ST B2H,(20H)      C2 20 B2      ;store values for calculation
2C92H      ADDB 20H,02H      75 02 20      ; of power consumption and
2C95H      ST B4H,(20H)      C2 20 B4      ; average active power
2C98H      LD 30H,B2H        A0 B2 30      ;
2C9BH      LD 32H,B4H        A0 B4 32      ;
2C9EH      LD 34H,00H        A0 00 34      ;
2CA1H      LD C4H,B2H        A0 B2 C4      ;
2CA4H      LD C0H,B4H        A0 B4 C0      ;
2CA7H      LD C2H,B6H        A0 B6 C2      ;
2CAAH      LD C6H,92E0H      A1 E0 92 C6      ;
2CAEH      LD C8H,574BH      A1 4B 57 C8      ;
2CB2H      CALL DISPIN       EF 41 0C      ;
2CB5H      LD 20H,803CH      A1 3C 80 20      ;if active power is positive,
2CB9H      LD E6H,(20H)      A2 20 E6      ; add '+' to display; if
2CBCH      CLRC              F8              ; active power is negative,
2CBDH      CMP 00H,E6H        88 E6 00      ; add '-' to display
2CC0H      JC A.P.12          DB 0E          ;
2CC2H      LD 20H,92E0H      A1 E0 92 20      ;
2CC6H      LD 30H,002DH      A1 2D 00 30      ;
2CCA      ST 30H,(20H)      C2 20 30      ;
2CCDH      LJMP FREQ.2       E7 0B 00      ;
2CDOH      A.P.12      LD 20H,92E0H      A1 E0 92 20      ;
2CD4H      LD 30H,002BH      A1 2B 00 30      ;
2CD8H      ST 30H,(20H)      C2 20 30      ;
2CDBH      FREQ.2      LD 20H,8027H      A1 22 80 20      ;determine input frequency
2CDFH      CMP 20H,00H        8A 20 00      ;
2CE2H      JE TWEN72         DF 69          ;
2CE4H      JBS P0-6,FREQ.22  3E 0E 1B      ;if pin 6 of PORT0 (connected
2CE7H      LDB 40H,0CH        B1 0C 40      ; to SYNCH/ASYNCH switch) is
2CEAH      LD 20H,9360H      A1 60 93 20      ; set, jump to FREQ.22; else,
2CEEH      LD 30H,0020H      A1 20 00 30      ; load FREQ. memory addresses
2CF2H      FREQ.12      ST 30H,(20H)      C2 20 30      ; with 20H (blank)
2CF5H      ADDB 20H,02H      75 02 20      ;
2CF8H      DECB 40H          15 40          ;

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2CFAH		CMPB 40H,00H	98 00 40	:	
2CFDH		JGT FREQ.12	D2 F3	:	
2CFFH		LJMP POW.CON.2	E7 6C 00	:	
2D02H	FREQ.22	LD E0H,7502H	A1 02 75 E0	:	;if alternating input,
2D06H		MULU E0H,3CH	6D 3C 00 E0	:	; determine input frequency
2D0AH		LD 24H,8020H	A1 20 80 24	:	
2D0EH		LD E6H,(24H)	A2 24 E6	:	
2D11H		LD E4H,E2H	A0 E2 E4	:	
2D14H		LD E2H,E0H	A0 E0 E2	:	
2D17H		LD E0H,00H	A0 00 E0	:	
2D1AH		CALI DIV	EF D5 0A	:	
2D1DH		LD 50H,8094H	A1 94 80 50	:	;store values for calculation
2D21H		ST E8H,(50H)	C2 50 E8	:	; of average frequency
2D24H		ADDB 50H,02H	75 02 50	:	
2D27H		ST EAH,(50H)	C2 50 EA	:	
2D2AH		LD 54H,80FEH	A1 FE 80 54	:	
2D2EH		LD 52H,(54H)	A2 54 52	:	
2D31H		INCB 52H	17 52	:	
2D33H		ST 52H,(54H)	C2 54 52	:	
2D36H		LD C4H,E8H	A0 E8 C4	:	
2D39H		LD C0H,EAH	A0 EA C0	:	
2D3CH		LD C2H,00H	A0 00 C2	:	
2D3FH		LD C6H,9360H	A1 60 93 C6	:	
2D43H		LD C8H,5A48H	A1 48 5A C8	:	
2D47H		CALL DISPIN	EF AC 0B	:	
2D4AH		LJMP POW.CON.2	E7 21 00	:	
2D4DH	TWEN72	LD 50H,8094H	A1 94 80 50	:	;if non-alternating input
2D51H		ST 00H,(50H)	C2 50 00	:	
2D54H		ADDB 50H,02H	75 02 50	:	
2D57H		ST 00H,(50H)	C2 50 00	:	
2D5AH		LD C2H,00H	A0 00 C0	:	
2D5DH		LD C0H,00H	A0 00 C2	:	
2D60H		LD C4H,00H	A0 00 C4	:	
2D63H		LD C6H,9360H	A1 60 93 C6	:	
2D67H		LD C8H,5A48H	A1 48 5A C8	:	
2D6BH		CALL DISPIN	EF 88 0B	:	
2D6EH	POW.CON.2	LD 20H,602AH	A1 2A 60 20	:	;add active power of this
2D72H		LD 86H,(20H)	A2 20 86	:	; cycle to running hourly
2D75H		ADDB 20H,02H	75 02 20	:	; total for phase 2 at
2D78H		LD 88H,(20H)	A2 20 88	:	; 602AH to 602FH
2D7BH		ADDB 20H,02H	75 02 20	:	
2D7EH		LD 8AH,(20H)	A2 20 8A	:	
2D81H		ADD 86H,30H	64 30 86	:	
2D84H		ADDC 88H,32H	A4 32 88	:	
2D87H		ADDC 8AH,34H	A4 34 8A	:	
2D8AH		ST 8AH,(20H)	C2 20 8A	:	
2D8DH		SUBB 20H,02H	79 02 20	:	
2D90H		ST 88H,(20H)	C2 20 88	:	
2D93H		SUBB 20H,02H	79 02 20	:	
2D96H		ST 86H,(20H)	C2 20 86	:	
2D99H		SUBB 20H,02H	79 02 20	:	
2D9CH		LD 8EH,(20H)	A2 20 8E	:	

2D9FH	INC 8EH	07 8E	;increment counter at 6028H
2DA1H	ST 8EH,(20H)	C2 20 8E	;
2DA4H	CMP 8EH,0708H	89 08 07 8E	;compare counter to 1800D, and
2DA8H	JNE NONSTORE2	D7 5B	; if equal, go to STORE
2DAAH	LD E6H,(20H)	A2 20 E6	;divide power stored over the
2DADH	ADDB 20H,02H	75 02 20	; last hour by 1800D to
2DB0H	LD E0H,(20H)	A2 20 E0	; obtain average value
2DB3H	ADDB 20H,02H	75 02 20	;
2DB6H	LD E2H,(20H)	A2 20 E2	;
2DB9H	ADDB 20H,02H	75 02 20	;
2DBCH	LD E4H,(20H)	A2 20 E4	;
2DBFH	CALL DIV	EF 30 0A	;
2DC2H	ADDB E8H,01H	75 01 E8	;correct roundoff error
2DC5H	LD 30H,6030H	A1 30 60 30	;load previous value of power
2DC9H	LD 70H,(30H)	A2 30 70	; consumed
2DCCH	ADDB 30H,02H	75 02 30	;
2DCFH	LD 72H,(30H)	A2 30 72	;
2DD2H	ADDB 30H,02H	75 02 30	;
2DD5H	LD 74H,(30H)	A2 30 74	;
2DD8H	ADD 70H,E8H	64 E8 70	;add total power over last
2DDBH	ADDC 72H,EAH	A4 EA 72	; hour to total power
2DDEH	ADDC 74H,00H	A4 00 74	; consumption
2DE1H	ST 74H,(30H)	C2 30 74	;store total power consumption
2DE4H	SUBB 30H,02H	79 02 30	;
2DE7H	ST 72H,(30H)	C2 30 72	;
2DEAH	SUBB 30H,02H	79 02 30	;
2DEDH	ST 70H,(30H)	C2 30 70	;
2DF0H	ST 00H,(20H)	C2 20 00	;zero running hourly total and
2DF3H	SUBB 20H,02H	79 02 20	; counter
2DF6H	ST 00H,(20H)	C2 20 00	;
2DF9H	SUBB 20H,02H	79 02 20	;
2DFCH	ST 00H,(20H)	C2 20 00	;
2DFFH	SUBB 20H,02H	79 02 20	;
2E02H	ST 00H,(20H)	C2 20 00	;
2E05H	LD 30H,6030H	A1 30 60 30	;load previous value of power
2E09H	LD C4H,(30H)	A2 30 C4	; consumed
2E0CH	ADDB 30H,02H	75 02 30	;
2E0FH	LD C0H,(30H)	A2 30 C0	;
2E12H	ADDB 30H,02H	75 02 30	;
2E15H	LD C2H,(30H)	A2 30 C2	;
2E18H	LD 20H,602AH	A1 2A 60 20	;load running total of power
2E1CH	LD E0H,(20H)	A2 20 E0	; consumption
2E1FH	ADDB 20H,02H	75 02 20	;
2E22H	LD E2H,(20H)	A2 20 E2	;
2E25H	ADDB 20H,02H	75 02 20	;
2E28H	LD E4H,(20H)	A2 20 E4	;
2E2BH	LD E6H,0708H	A1 08 07 E6	;
2E2FH	CALL DIV	EF C0 09	;divide running total by 1800D
2E32H	ADDB E8H,01H	75 01 E8	;correct roundoff error
2E35H	ADD C4H,E8H	64 E8 C4	;add running value of power
2E38H	ADDC C0H,EAH	A4 EA C0	; consumed to previous total
2E3BH	ADDC C2H,00H	A4 00 C2	;

2E4EH	LD 20H,8098H	A1 98 80 20	;store values for calculation
2E4ZH	ST C4H,20H	C2 20 C4	; of total power consumption
2E45H	ADDB 20H,02H	75 02 20	;
2E48H	ST C0H,20H	C2 20 C0	;
2E4BH	ADDB 20H,02H	75 02 20	;
2E4EH	ST C2H,20H	C2 20 C2	;
2E51H	LD C6H,93A0H	A1 A0 93 C6	;
2E55H	LD C8H,484BH	A1 4B 48 C8	;
2E59H	CALL DISPIN	EF 9A 0A	;
2E5CH	KW.DEM.2 LD 20H,A800H	A1 00 A8 20	;load registers from 15-Min.
2E60H	LD 30H,(20H)	A2 20 30	; Demand RAM for calculation
2E63H	LD 50H,(20H)	A2 20 50	; of 15-Min. Demand. Current
2E66H	ADDB 20H,02H	75 02 20	; V.I value is in registers
2E69H	LD 32H,(20H)	A2 20 32	; 30H,32H and 50H,52H
2E6CH	LD 52H,(20H)	A2 20 52	;
2E6FH	ADDB 20H,02H	75 02 20	;
2E72H	LD 34H,(20H)	A2 20 34	;15-Min. Demand addr. register
2E75H	ADDB 20H,02H	75 02 20	; is in register 34H
2E78H	LD 36H,(20H)	A2 20 36	;current 15-Min. Demand total
2E7BH	ADDB 20H,02H	75 02 20	; V.I is in registers 36H,
2E7EH	LD 38H,(20H)	A2 20 38	; 38H,3AH
2E81H	ADDB 20H,02H	75 02 20	;
2E84H	LD 3AH,(20H)	A2 20 3A	;
2E87H	LD 40H,(34H)	A2 34 40	;oldest V.I value is in
2E8AH	ADDB 34H,02H	75 02 34	; registers 40H,42H
2E8DH	LD 42H,(34H)	A2 34 42	;
2E90H	ADD 36H,30H	64 30 36	;calculate new 15-Min. Demand
2E93H	ADDC 38H,32H	A4 32 38	; total V.I by subtracting
2E96H	ADDC 3AH,00H	A4 00 3A	; oldest V.I value and adding
2E99H	SUB 36H,40H	68 40 36	; current V.I value
2E9CH	SUBC 38H,42H	A8 42 38	;
2E9FH	SUBC 3AH,00H	A8 00 3A	;
2EA2H	ST 3AH,(20H)	C2 20 3A	;store new 15-Min. Demand
2EA5H	SUBB 20H,02H	79 02 20	; total
2EA8H	ST 38H,(20H)	C2 20 38	;
2EABH	SUBB 20H,02H	79 02 20	;
2EAEH	ST 36H,(20H)	C2 20 36	;
2EB1H	SUBB 20H,02H	79 02 20	;
2EB4H	ST 52H,(34H)	C2 34 52	;replace oldest V.I value with
2EB7H	SUBB 34H,02H	79 02 34	; current V.I value
2EBAH	ST 50H,(34H)	C2 34 50	;
2EBDH	LD 56H,36H	A0 36 56	;compare new 15-Min. Demand
2EC0H	LD 58H,38H	A0 38 58	; total with maximum 15-Min.
2EC3H	LD 5AH,3AH	A0 3A 5A	; Demand total, and store the
2EC6H	LD 20H,6068H	A1 68 60 20	; larger value as the new
2ECAH	LD 40H,(20H)	A2 20 40	; maximum 15-Min. Demand
2ECIH	LD 50H,(20H)	A2 20 50	; total
2ED0H	ADDB 20H,02H	75 02 20	;
2ED3H	LD 42H,(20H)	A2 20 42	;
2ED6H	LD 52H,(20H)	A2 20 52	;
2ED9H	ADDB 20H,02H	75 02 20	;
2EDCH	LD 44H,(20H)	A2 20 44	;

2EDFH		LD 54H,(20H)	A2 20 54	:	
2EE2H		SUB 36H,40H	68 40 36	:	
2EE5H		SUBC 38H,42H	A8 42 38	:	
2EE8H		SUBC 3AH,44H	A8 44 3A	:	
2EEBH		JC KW.DEM.12	DB 12	:	
2EEDH		ST 54H,(20H)	C2 20 54	:	
2EFOH		SUBB 20H,02H	79 02 20	:	
2EF3H		ST 52H,(20H)	C2 20 52	:	
2EF6H		SUBB 20H,02H	79 02 20	:	
2EF9H		ST 50H,(20H)	C2 20 50	:	
2EFCH		LJMP KW.DEM.22	E7 0F 00	:	
2EFFH	KW.DEM.12	ST 5AH,(20H)	C2 20 5A	:	
2F02H		SUBB 20H,02H	79 02 20	:	
2F05H		ST 58H,(20H)	C2 20 58	:	
2F08H		SUBB 20H,02H	79 02 20	:	
2F0BH		ST 56H,(20H)	C2 20 56	:	
2F0EH	KW.DEM.22	LD E0H,(20H)	A2 20 E0	:	;divide maximum 15-Min. Demand
2F11H		ADDB 20H,02H	75 02 20	:	; total by 450 to obtain
2F14H		LD E2H,(20H)	A2 20 E2	:	; value for 15-Min. Demand
2F17H		ADDB 20H,02H	75 02 20	:	; display
2F1AH		LD E4H,(20H)	A2 20 E4	:	
2F1DH		LD E6H,01C2H	A1 C2 01 E6	:	
2F21H		CALL DIV	EF CE 08	:	
2F24H		ADD 34H,0004H	65 04 00 34	:	;increment address pointer to
2F28H		CMP 34H,AF28H	89 28 AF 34	:	; next oldest V.I value
2F2CH		JNE KW.DEM.32	D7 04	:	
2F2EH		SUB 34H,0708H	69 08 07 34	:	
2F32H	KW.DEM.32	LD 20H,A804H	A1 04 A8 20	:	
2F36H		ST 34H,(20H)	C2 20 34	:	
2F39H		LD C2H,00H	A0 00 C2	:	;display 15-Min. Demand value
2F3CH		LD C0H,EAH	A0 EA C0	:	
2F3FH		LD C4H,E8H	A0 E8 C4	:	
2F42H		LD C6H,93E0H	A1 E0 93 C6	:	
2F46H		LD C8H,574BH	A1 4B 57 C8	:	
2F4AH		CALL DISPIN	EF A9 09	:	

PHASE THREE

2F4DH	VOLTAGE3	LD 20H,8040H	A1 40 80 20	:	;find RMS value of voltage in
2F51H		LD E6H,(20H)	A2 20 E6	:	; phase 3
2F54H		ADDB 20H,10H	75 10 20	:	
2F57H		LD E0H,(20H)	A2 20 E0	:	
2F5AH		ADDB 20H,02H	75 02 20	:	
2F5DH		LD E2H,(20H)	A2 20 E2	:	
2F60H		ADDB 20H,02H	75 02 20	:	
2F63H		LD E4H,(20H)	A2 20 E4	:	
2F66H		CALL DIV	EF 89 08	:	
2F69H		CALL SQRT	EF A1 08	:	
2F6CH		LD 70H,B4H	A0 B4 70	:	;store RMS value for PF value
2F6FH		LD 22H,6008H	A1 08 60 22	:	;multiply by phase-2 voltage
2F73H		LD 24H,22H	A2 22 24	:	; calibration factor
2F76H		MULU 24H,B4H	6C B4 24	:	

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2F79H      ADDB 22H,02H      75 02 22      ;
2F7CH      LD 28H,22H      A2 22 28      ;
2F7FH      MULU 28H,B4H     6C B4 28      ;
2F82H      LD 24H,26H      A0 26 24      ;
2F85H      LD 26H,00H      A0 00 26      ;
2F88H      ADD 24H,28H      64 28 24      ;integer result is in 26H, and
2F8BH      ADDC 26H,2AH     A4 2A 26      ; fraction result is in 24H
2F8EH      LD 20H,80A0H     A1 A0 80 20    ;store values for calculation
2F92H      ST 24H,(20H)     C2 20 24      ; of apparent power and
2F95H      ADDB 20H,02H     75 02 20      ; average voltage
2F98H      ST 26H,(20H)     C2 20 26      ;
2F9BH      LD 80H,24H      A0 24 80      ;
2F9EH      LD 82H,26H      A0 26 82      ;
2FA1H      LD C2H,00H      A0 00 C2      ;
2FA4H      LD C0H,26H      A0 26 C0      ;
2FA7H      LD C4H,24H      A0 24 C4      ;
2FAAH      LD C6H,9420H     A1 20 94 C6      ;
2FAEH      LD C8H,2E56H     A1 56 2E C8      ;
2FB2H      CALL DISPIN     EF 41 09      ;put voltage in display RAM
2FB5H      CURRENT3 LD 20H,8040H A1 40 80 20    ;find RMS value of current in
2FB9H      LD E6H,(20H)     A2 20 E6      ; phase 3
2FBCB      ADDB 20H,16H     75 16 20      ;
2FBFH      LD E0H,(20H)     A2 20 E0      ;
2FC2H      ADDB 20H,02H     75 02 20      ;
2FC5H      LD E2H,(20H)     A2 20 E2      ;
2FC8H      ADDB 20H,02H     75 02 20      ;
2FCBH      LD E4H,(20H)     A2 20 E4      ;
2FCEH      CALL DIV        EF 21 08      ;
2FD1H      CALL SQRT       EF 39 08      ;
2FD4H      LD 72H,B4H      A0 B4 72      ;store RMS value for PF value
2FD7H      LD 22H,6014H     A1 14 60 22    ;multiply by phase-3 current
2FDBH      LD 24H,22H      A2 22 24      ; calibration factor
2FDEH      MULU 24H,B4H     6C B4 24      ;
2FE1H      ADDB 22H,02H     75 02 22      ;
2FE4H      LD 28H,22H      A2 22 28      ;
2FE7H      MULU 28H,B4H     6C B4 28      ;
2FEAH      LD 24H,26H      A0 26 24      ;
2FEDH      LD 26H,00H      A0 00 26      ;
2FF0H      ADD 24H,28H      64 28 24      ;integer result is in 26H, and
2FF3H      ADDC 26H,2AH     A4 2A 26      ; fraction result is in 24H
2FF6H      LD 20H,80A4H     A1 A4 80 20    ;store values for calculation
2FFAH      ST 24H,(20H)     C2 20 24      ; of apparent power and
2FFDH      ADDB 20H,02H     75 02 20      ; average current
3000H      ST 26H,(20H)     C2 20 26      ;
3003H      LD 86H,24H      A0 24 86      ;
3006H      LD 88H,26H      A0 26 88      ;
3009H      LD C2H,00H      A0 00 C2      ;
300CH      LD C0H,26H      A0 26 C0      ;
300FH      LD C4H,24H      A0 24 C4      ;
3012H      LD C6H,9460H     A1 60 94 C6      ;
3016H      LD C8H,2E41H     A1 41 2E C8      ;
301AH      CALL DISPIN     EF D9 08      ;put current in display RAM

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301DH APP.POW.3 LD 84H,00H A0 00 84 ;determine apparent power -
3020H CALL MUL EF 0C 0C ; (VRMS*IRMS)/1000 (KW)
3023H LD E0H,B2H A0 B2 E0 ;
3026H LD E2H,B4H A0 B4 E2 ;
3029H LD E4H,B6H A0 B6 E4 ;
302CH LD E6H,03E8H A1 E8 03 E6 ;
3030H CALL DIV EF BF 07 ;
3033H ADDB E8H,01H 75 01 E8 ;correct roundoff error
3036H LD 20H,80A8H A1 A8 80 20 ;store values for calculation
303AH ST E8H,(20H) C2 20 E8 ; of active power, 15-Min.
303DH LD 30H,B000H A1 00 B0 30 ; Demand, and average
3041H ST E8H,(30H) C2 30 E8 ; apparent power
3044H ADDB 20H,02H 75 02 20 ;
3047H ST EAH,(20H) C2 20 EA ;
304AH ADDB 30H,02H 75 02 30 ;
304DH ST EAH,(30H) C2 30 EA ;
3050H LD 80H,E8H A0 E8 80 ;
3053H LD 82H,EAH A0 EA 82 ;
3056H LD 84H,00H A0 00 84 ;
3059H LD C4H,E8H A0 E8 C4 ;
305CH LD C0H,EAH A0 EA C0 ;
305FH LD C2H,00H A0 00 C2 ;
3062H LD C6H,94A0H A1 A0 94 C6 ;
3066H LD C8H,574BH A1 4B 57 C8 ;
306AH CALL DISPIN EF 89 08 ;
306DH P.FACTOR3 LD 20H,8040H A1 40 80 20 ;determine power factor
3071H LD E6H,(20H) A2 20 E6 ;
3074H ADDB 20H,0AH 75 0A 20 ;
3077H LD E0H,(20H) A2 20 E0 ;
307AH ADDB 20H,02H 75 02 20 ;
307DH LD E2H,(20H) A2 20 E2 ;
3080H ADDB 20H,02H 75 02 20 ;
3083H LD E4H,(20H) A2 20 E4 ;
3086H CALL DIV EF 69 07 ;
3089H DIVU E8H,70H 8C 70 E8 ;
308CH LD E4H,00H A0 00 E4 ;
308FH LD E2H,E8H A0 E8 E2 ;
3092H LD E0H,EAH A0 EA E0 ;
3095H LD E6H,72H A0 72 E6 ;
3098H CALL DIV EF 57 07 ;
309BH CMP EAH,01H 89 01 00 EA ;if integer value is not zero
309FH JE NOT10.3 DF 08 ; or one, make equal to zero
30A1H CMP EAH,00H 88 00 EA ;
30A4H JE NOT10.3 DF 03 ;
30A6H LD EAH,00H A0 00 EA ;
30A9H NOT10.3 LD 20H,80ACH A1 AC 80 20 ;store values for calculation
30ADH ST E8H,(20H) C2 20 E8 ; of active power and average
30B0H ADDB 20H,02H 75 02 20 ; power factor
30B3H ST EAH,(20H) C2 20 EA ;
30B6H LD 86H,E8H A0 E8 86 ;
30B9H LD 88H,FAH A0 EA 88 ;
30BCH LD C2H,00H A0 00 C2 ;

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30BFH	LD C0H,EAH	A0 EA C0	:
30C2H	LD C4H,E8H	A0 E8 C4	:
30C5H	LD C6H,9520H	A1 20 95 C6	:
30C9H	LD C8H,2020H	A1 20 20 C8	:
30CDH	CALL DISPIN	EF 26 08	;for asynchronous sampling
30D0H	JBC P0-6,P.F.23	36 0E 7F	; only: if the current is
30D3H	LD 20H,8044H	A1 44 80 20	; leading the voltage by 1
30D7H	LD E6H,(20H)	A2 20 E6	; to 127 samples, display
30DAH	ADDB 20H,04H	75 04 20	; CAP.; if the current is
30DDH	LD E8H,(20H)	A2 20 E8	; lagging the voltage by 1
30E0H	CMP E6H,E8H	88 E8 E6	; to 127 samples, display
30E3H	JE P.F.23	DF 6D	; IND.; if the current is
30E5H	CLRC	F8	; leading the voltage by 0
30E6H	CMP E6H,E8H	88 E8 E6	; or 128 samples, do not
30E9H	JC P.F.13	DB 3B	; display CAP. or IND.
30EBH	CLRC	F8	:
30ECH	SUB E8H,E6H	68 E6 E8	:
30EFH	CMP E8H,0080H	89 80 00 E8	:
30F3H	JE P.F.23	DF 5D	:
30F5H	JC P.F.13	DB 2F	:
30F7H	LD 20H,9530H	A1 30 95 20	:
30FBH	LD 30H,0049H	A1 49 00 30	:
30FFH	ST 30H,(20H)	C2 20 30	:
3102H	LD 20H,9532H	A1 32 95 20	:
3106H	LD 30H,004EH	A1 4E 00 30	:
310AH	ST 30H,(20H)	C2 20 30	:
310DH	LD 20H,9534H	A1 34 95 20	:
3111H	LD 30H,0044H	A1 44 00 30	:
3115H	ST 30H,(20H)	C2 20 30	:
3118H	LD 20H,9536H	A1 36 95 20	:
311CH	LD 30H,002EH	A1 2E 00 30	:
3120H	ST 30H,(20H)	C2 20 30	:
3123H	LJMP P.F.23	E7 2C 00	:
3126H	P.F.13 LD 20H,9530H	A1 30 95 20	:
312AH	LD 30H,0043H	A1 43 00 30	:
312EH	ST 30H,(20H)	C2 20 30	:
3131H	LD 20H,9532H	A1 32 95 20	:
3135H	LD 30H,0041H	A1 41 00 30	:
3139H	ST 30H,(20H)	C2 20 30	:
313CH	LD 20H,9534H	A1 34 95 20	:
3140H	LD 30H,0050H	A1 50 00 30	:
3144H	ST 30H,(20H)	C2 20 30	:
3147H	LD 20H,9536H	A1 36 95 20	:
314BH	LD 30H,002EH	A1 2E 00 30	:
314FH	ST 30H,(20H)	C2 20 30	:
3152H	P.F.23 LD 20H,805CH	A1 5C 80 20	;if active power is positive,
3156H	LD E6H,(20H)	A2 20 E6	; add '+' to power factor; if
3159H	CLRC	F8	; active power is negative,
315AH	CMP 00H,E6H	88 E6 00	; add '-' to power factor
315DH	JC P.F.33	DB 0E	:
315FH	LD 20H,9520H	A1 20 95 20	:
3163H	LD 30H,002DH	A1 2D 00 30	:

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3167H      ST 30H,(20H)      C2 20 30      ;
316AH      LJMP ACT.POW.3    E7 0B 00      ;
316DH      P.F.33          LD 20H,9520H      A1 20 95 20      ;
3171H      LD 30H,002BH      A1 2B 00 30      ;
3175H      ST 30H,(20H)      C2 20 30      ;
3178H      ACT.POW.3        CALL MUL          EF B4 0A      ;determine active power *
317BH      LD 20H,80B0H      A1 B0 80 20      ; (P.FACTOR)*(APP.POW.)
317FH      ST B2H,(20H)      C2 20 B2      ;store values for calculation
3182H      ADDB 20H,02H      75 02 20      ; of power consumption and
3185H      ST B4H,(20H)      C2 20 B4      ; average active power
3188H      LD 30H,B2H        A0 B2 30      ;
318BH      LD 32H,B4H        A0 B4 32      ;
318EH      LD 34H,00H        A0 00 34      ;
3191H      LD C4H,B2H        A0 B2 C4      ;
3194H      LD C0H,B4H        A0 B4 C0      ;
3197H      LD C2H,B6H        A0 B6 C2      ;
319AH      LD C6H,94E0H      A1 E0 94 C6      ;
319EH      LD C8H,574BH      A1 4B 57 C8      ;
31A2H      CALL DISPIN      EF 54 07      ;
31A5H      LD 20H,805CH      A1 5C 80 20      ;if active power is positive,
31A9H      LD E6H,(20H)      A2 20 E6      ; add '+' to display; if
31ACH      CLRC              F8              ; active power is negative,
31ADH      CMP 00H,E6H       88 E6 00      ; add '-' to display
31B0H      JC A.P.13         DB 0E          ;
31B2H      LD 20H,94E0H      A1 E0 94 20      ;
31B6H      LD 30H,002DH      A1 2D 00 30      ;
31BAH      ST 30H,(20H)      C2 20 30      ;
31BDH      LJMP FREQ.3       E7 0B 00      ;
31C0H      A.P.13          LD 20H,94E0H      A1 E0 94 20      ;
31C4H      LD 30H,002BH      A1 2B 00 30      ;
31C8H      ST 30H,(20H)      C2 20 30      ;
31CBH      FREQ.3          LD 20H,8042H      A1 42 80 20      ;determine input frequency
31CFH      CMP 20H,00H       8A 20 00      ;
31D2H      JE TWEN73         DF 69          ;
31D4H      JBS PO-6,FREQ.23 3E 0E 1B      ;if pin 6 of PORT0 (connected
31D7H      LDB 40H,0CH       B1 0C 40      ; to SYNCH/ASYNCH switch) is
31DAH      LD 20H,9560H      A1 60 95 20      ; set, jump to FREQ.23; else,
31DEH      LD 30H,0020H      A1 20 00 30      ; load FREQ. memory addresses
31E2H      FREQ.1          ST 30H,(20H)      C2 20 30      ; with 20H (blank)
31E5H      ADDB 20H,02H      75 02 20      ;
31E8H      DECB 40H          15 40          ;
31EAH      CMPB 40H,00H      98 00 40      ;
31EDH      JGT FREQ.13       D2 F3          ;
31EPH      LJMP POW.CON.3    E7 6C 00      ;
31F2H      FREQ.23         LD E0H,7502H      A1 02 75 E0      ;if alternating input,
31F6H      MULU E0H,3CH      6D 3C 00 E0      ; determine input frequency
31FAH      LD 24H,8040H      A1 40 80 24      ;
31FEH      LD E6H,(24H)      A2 24 E6      ;
3201H      LD E4H,E2H        00 E2 E4      ;
3204H      LD E2H,E0H        A0 E0 E2      ;
3207H      LD E0H,00H        A0 00 E0      ;
320AH      CALL DIV          EF E5 05      ;

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3200H	LD 50H,80B4H	A1 B4 80 50	;store values for calculation
3211H	ST E8H,(50H)	C2 50 E8	; of average frequency
3214H	ADDB 50H,02H	75 02 50	;
3217H	ST EAH,(50H)	C2 50 EA	;
321AH	LD 54H,80FEH	A1 FE 80 54	;
321EH	LD 52H,(54H)	A2 54 52	;
3221H	INCB 52H	17 52	;
3223H	ST 52H,(54H)	C2 54 52	;
3226H	LD C4H,E8H	A0 E8 C4	;
3229H	LD C0H,EAH	A0 EA C0	;
322CH	LD C2H,00H	A0 00 C2	;
322FH	LD C6H,9560H	A1 60 95 C6	;
3233H	LD C8H,5A48H	A1 48 5A C8	;
3237H	CALL DISPIN	EF BC 06	;
323AH	LJMP POW.CON.3	E7 21 00	;
323DH	TWEN73 LD 50H,80B4H	A1 B4 80 50	;if non-alternating input
3241H	ST 00H,(50H)	C2 50 00	;
3244H	ADDB 50H,02H	75 02 50	;
3247H	ST 00H,(50H)	C2 50 00	;
324AH	LD C2H,00H	A0 00 C0	;
324DH	LD C0H,00H	A0 00 C2	;
3250H	LD C4H,00H	A0 00 C4	;
3253H	LD C6H,9560H	A1 60 95 C6	;
3257H	LD C8H,5A48H	A1 48 5A C8	;
325BH	CALL DISPIN	EF 98 06	;
325EH	POW.CON.3 LD 20H,603AH	A1 3A 60 20	;add active power of this
3262H	LD 86H,(20H)	A2 20 86	; cycle to running hourly
3265H	ADDB 20H,02H	75 02 20	; total for phase 3 at
3268H	LD 88H,(20H)	A2 20 88	; 603AH to 603FH
326BH	ADDB 20H,02H	75 02 20	;
326EH	LD 8AH,(20H)	A2 20 8A	;
3271H	ADD 86H,30H	64 30 86	;
3274H	ADDC 88H,32H	A4 32 88	;
3277H	ADDC 8AH,34H	A4 34 8A	;
327AH	ST 8AH,(20H)	C2 20 8A	;
327DH	SUBB 20H,02H	79 02 20	;
3280H	ST 88H,(20H)	C2 20 88	;
3283H	SUBB 20H,02H	79 02 20	;
3286H	ST 86H,(20H)	C2 20 86	;
3289H	SUBB 20H,02H	79 02 20	;
328CH	LD 8EH,(20H)	A2 20 8E	;
328FH	INC 8EH	07 8E	;increment counter at 6038H
3291H	ST 8EH,(20H)	C2 20 8E	;
3294H	CMP 8EH,0708H	89 08 07 8E	;compare counter to 1800D, and
3298H	JNE NONSTORE3	D7 5B	; if equal, go to STORE
329AH	STORE3 LD E6H,(20H)	A2 20 E6	;divide power stored over the
329DH	ADDB 20H,02H	75 02 20	; last hour by 1800D to
32A0H	LD E0H,(20H)	A2 20 E0	; obtain average value
32A3H	ADDB 20H,02H	75 02 20	;
32A6H	LD E2H,(20H)	A2 20 E2	;
32A9H	ADDB 20H,02H	75 02 20	;
32ACH	LD E4H,(20H)	A2 20 E4	;

32AFH	CALL DIV	EF 40 05	;
32B2H	ADDB E8H,01H	75 01 E8	;correct roundoff error
32B5H	LD 30H,6040H	A1 40 60 30	;load previous value of power
32B9H	LD 70H,(30H)	A2 30 70	; consumed
32BCH	ADDB 30H,02H	75 02 30	;
32BFH	LD 72H,(30H)	A2 30 72	;
32C2H	ADDB 30H,02H	75 02 30	;
32C5H	LD 74H,(30H)	A2 30 74	;
32C8H	ADD 70H,E8H	64 E8 70	;add total power over last
32CBH	ADDC 72H,EAH	A4 EA 72	; hour to total power
32CEH	ADDC 74H,00H	A4 00 74	; consumption
32D1H	ST 74H,(30H)	C2 30 74	;store total power consumption
32D4H	SUBB 30H,02H	79 02 30	;
32D7H	ST 72H,(30H)	C2 30 72	;
32DAH	SUBB 30H,02H	79 02 30	;
32DDH	ST 70H,(30H)	C2 30 70	;
32E0H	ST 00H,(20H)	C2 20 00	;zero running hourly total and
32E3H	SUBB 20H,02H	79 02 20	; counter
32E6H	ST 00H,(20H)	C2 20 00	;
32E9H	SUBB 20H,02H	79 02 20	;
32ECH	ST 00H,(20H)	C2 20 00	;
32EFH	SUBB 20H,02H	79 02 20	;
32F2H	ST 00H,(20H)	C2 20 00	;
32F5H	NONSTORE3 LD 30H,6040H	A1 40 60 30	;load previous value of power
32F9H	LD C4H,(30H)	A2 30 C4	; consumed
32FCH	ADDB 30H,02H	75 02 30	;
32FFH	LD C0H,(30H)	A2 30 C0	;
3302H	ADDB 30H,02H	75 02 30	;
3305H	LD C2H,(30H)	A2 30 C2	;
3308H	LD 20H,603AH	A1 3A 60 20	;load running total of power
330CH	LD E0H,(20H)	A2 20 E0	; consumption
330FH	ADDB 20H,02H	75 02 20	;
3312H	LD E2H,(20H)	A2 20 E2	;
3315H	ADDB 20H,02H	75 02 20	;
3318H	LD E4H,(20H)	A2 20 E4	;
331BH	LD E6H,0708H	A1 08 07 E6	;
331FH	CALL DIV	EF D0 04	;divide running total by 18000
3322H	ADDB E8H,01H	75 01 E8	;correct roundoff error
3325H	ADD C4H,E8H	64 E8 C4	;add running value of power
3328H	ADDC C0H,EAH	A4 EA C0	; consumed to previous total
332BH	ADDC C2H,00H	A4 00 C2	;
332EH	LD 20H,80B8H	A1 B8 80 20	;store values for calculation
3332H	ST C4H,20H	C2 20 C4	; of total power consumption
3335H	ADDB 20H,02H	75 02 20	;
3338H	ST C0H,20H	C2 20 C0	;
333BH	ADDB 20H,02H	75 02 20	;
333EH	ST C2H,20H	C2 20 C2	;
3341H	LD C6H,95A0H	A1 A0 95 C6	;
3345H	LD C8H,484BH	A1 4B 48 C8	;
3349H	CALL DISPIN	EF AA 05	;
334CH	KW.DEM.3 LD 20H,B000H	A1 00 B0 20	;load registers from 15-Min.
3350H	LD 30H,(20H)	A2 20 30	; Demand RAM for calculation

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3353H	LD 50H,(20H)	A2 20 50	; of 15-Min. Demand. Current
3356H	ADDB 20H,02H	75 02 20	; V.I value is in registers
3359H	LD 32H,(20H)	A2 20 32	; 30H,32H and 50H,52H
335CH	LD 52H,(20H)	A2 20 52	;
335FH	ADDB 20H,02H	75 02 20	;
3362H	LD 34H,(20H)	A2 20 34	;15-Min. Demand addr. register
3365H	ADDB 20H,02H	75 02 20	; is in register 34H
3368H	LD 36H,(20H)	A2 20 36	;current 15-Min. Demand total
336BH	ADDB 20H,02H	75 02 20	; V.I is in registers 36H,
336EH	LD 38H,(20H)	A2 20 38	; 38H,3AH
3371H	ADDB 20H,02H	75 02 20	;
3374H	LD 3AH,(20H)	A2 20 3A	;
3377H	LD 40H,(34H)	A2 34 40	;oldest V.I value is in
337AH	ADDB 34H,02H	75 02 34	; registers 40H,42H
337DH	LD 42H,(34H)	A2 34 42	;
3380H	ADD 36H,30H	64 30 36	;calculate new 15-Min. Demand
3383H	ADDC 38H,32H	A4 32 38	; total V.I by subtracting
3386H	ADDC 3AH,00H	A4 00 3A	; oldest V.I value and adding
3389H	SUB 36H,40H	68 40 36	; current V.I value
338CH	SUBC 38H,42H	A8 42 38	;
338FH	SUBC 3AH,00H	A8 00 3A	;
3392H	ST 3AH,(20H)	C2 20 3A	;store new 15-Min. Demand
3395H	SUBB 20H,02H	79 02 20	; total
3398H	ST 38H,(20H)	C2 20 38	;
339BH	SUBB 20H,02H	79 02 20	;
339EH	ST 36H,(20H)	C2 20 36	;
33A1H	SUBB 20H,02H	79 02 20	;
33A4H	ST 52H,(34H)	C2 34 52	;replace oldest V.I value with
33A7H	SUBB 34H,02H	79 02 34	; current V.I value
33AAH	ST 50H,(34H)	C2 34 50	;
33ADH	LD 56H,36H	A0 36 56	;compare new 15-Min. Demand
33BOH	LD 58H,38H	A0 38 58	; total with maximum 15-Min.
33B3H	LD 5AH,3AH	A0 3A 5A	; Demand total, and store the
33B6H	LD 20H,6078H	A1 78 60 20	; larger value as the new
33BAH	LD 40H,(20H)	A2 20 40	; maximum 15-Min. Demand
33BDH	LD 50H,(20H)	A2 20 50	; total
33COH	ADDB 20H,02H	75 02 20	;
33C3H	LD 42H,(20H)	A2 20 42	;
33C6H	LD 52H,(20H)	A2 20 52	;
33C9H	ADDB 20H,02H	75 02 20	;
33CCH	LD 44H,(20H)	A2 20 44	;
33CFH	LD 54H,(20H)	A2 20 54	;
33D2H	SUB 36H,40H	68 40 36	;
33D5H	SUBC 38H,42H	A8 42 38	;
33D8H	SUBC 3AH,44H	A8 44 3A	;
33DBH	JC KW.DEM.13	DB 12	;
33DDH	ST 54H,(20H)	C2 20 54	;
33EOH	SUBB 20H,02H	79 02 20	;
33E3H	ST 52H,(20H)	C2 20 52	;
33E6H	SUBB 20H,02H	79 02 20	;
33E9H	ST 50H,(20H)	C2 20 50	;
33ECH	LJMP KW.DEM.23	E7 0F 00	;

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33EFH KW.DEM.13 ST 5AH,(20H) C2 20 5A ;
33F2H SUBB 20H,02H 79 02 20 ;
33F5H ST 58H,(20H) C2 20 58 ;
33F8H SUBB 20H,02H 79 02 20 ;
33FBH ST 56H,(20H) C2 20 56 ;
33FEH KW.DEM.23 LD E0H,(20H) A2 20 E0 ;divide maximum 15-Min. Demand
3401H ADDB 20H,02H 75 02 20 ; total by 450 to obtain
3404H LD E2H,(20H) A2 20 E2 ; value for 15-Min. Demand
3407H ADDB 20H,02H 75 02 20 ; display
340AH LD E4H,(20H) A2 20 E4 ;
340DH LD E6H,01C2H A1 C2 01 E6 ;
3411H CALL DIV EF DE 03 ;
3414H ADD 34H,0004H 65 04 00 34 ;increment address pointer to
3418H CMP 34H,B728H 89 28 B7 34 ; next oldest V.I value
341CH JNE KW.DEM.33 D7 04 ;
341EH SUB 34H,0708H 69 08 07 34 ;
3422H KW.DEM.33 LD 20H,8004H A1 04 B0 20 ;
3426H ST 34H,(20H) C2 20 34 ;
3429H LD C2H,00H A0 00 C2 ;display 15-Min. Demand value
342CH LD C0H,EAH A0 EA C0 ;
342FH LD C4H,E8H A0 E8 C4 ;
3432H LD C6H,95E0H A1 E0 95 C6 ;
3436H LD C8H,574BH A1 4B 57 C8 ;
343AH CALL DISPIN EF B9 04 ;

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TOTAL OF PHASES

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343DH VOLTAVGE LD 20H,8060H A1 60 80 20 ;find average voltage value
3441H LD E0H,(20H) A2 20 E0 ;
3444H ADDB 20H,02H 75 02 20 ;
3447H LD E2H,(20H) A2 20 E2 ;
344AH LD E4H,00H A0 00 E4 ;
344DH LD 20H,8080H A1 80 80 20 ;
3451H LD 40H,(20H) A2 20 40 ;
3454H ADDB 20H,02H 75 02 20 ;
3457H LD 42H,(20H) A2 20 42 ;
345AH LD 20H,80A0H A1 A0 80 20 ;
345EH LD 50H,(20H) A2 20 50 ;
3461H ADDB 20H,02H 75 02 20 ;
3464H LD 52H,(20H) A2 20 52 ;
3467H ADD E0H,40H 64 40 E0 ;
346AH ADDC E2H,42H A4 42 E2 ;
346DH ADDC E4H,00H A4 00 E4 ;
3470H ADD E0H,50H 64 50 E0 ;
3473H ADDC E2H,52H A4 52 E2 ;
3476H ADDC E4H,00H A4 00 E4 ;
3479H LD E6H,0003H A1 03 00 E6 ;
347DH CALL DIV EF 72 03 ;
3480H LD C2H,00H A0 00 C2 ;
3483H LD C0H,EAH A0 EA C0 ;
3486H LD C4H,E8H A0 E8 C4 ;
3489H LD C6H,9620H A1 20 96 C6 ;

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348DH	LD C8H,2E56H	A1 56 2E C8	;
3491H	CALL DISPIN	EF 62 04	;
3494H	CURRAVGE LD 20H,8064H	A1 64 80 20	;find average current value
3498H	LD E0H,(20H)	A2 20 E0	;
349BH	ADDB 20H,02H	75 02 20	;
349EH	LD E2H,(20H)	A2 20 E2	;
34A1H	LD E4H,00H	A0 00 E4	;
34A4H	LD 20H,8084H	A1 84 80 20	;
34A8H	LD 40H,(20H)	A2 20 40	;
34ABH	ADDB 20H,02H	75 02 20	;
34AEH	LD 42H,(20H)	A2 20 42	;
34B1H	LD 20H,80A4H	A1 A4 80 20	;
34B5H	LD 50H,(20H)	A2 20 50	;
34B8H	ADDB 20H,02H	75 02 20	;
34BBH	LD 52H,(20H)	A2 20 52	;
34BEH	ADD E0H,40H	64 40 E0	;
34C1H	ADDC E2H,42H	A4 42 E2	;
34C4H	ADDC E4H,00H	A4 00 E4	;
34C7H	ADD E0H,50H	64 50 E0	;
34CAH	ADDC E2H,52H	A4 52 E2	;
34CDH	ADDC E4H,00H	A4 00 E4	;
34D0H	LD E6H,0003H	A1 03 00 E6	;
34D4H	CALL DIV	EF 1B 03	;
34D7H	LD C2H,00H	A0 00 C2	;
34DAH	LD C0H,EAH	A0 EA C0	;
34DDH	LD C4H,E8H	A0 E8 C4	;
34E0H	LD C6H,9660H	A1 60 96 C6	;
34E4H	LD C8H,2E41H	A1 41 2E C8	;
34E8H	CALL DISPIN	EF 0B 04	;
34EBH	TOTAPPOW LD 20H,8068H	A1 68 80 20	;determine total apparent
34EFH	LD E0H,(20H)	A2 20 E0	power in KW
34F2H	ADDB 20H,02H	75 02 20	;
34F5H	LD E2H,(20H)	A2 20 E2	;
34F8H	LD E4H,00H	A0 00 E4	;
34FBH	LD 20H,8088H	A1 88 80 20	;
34FFH	LD 40H,(20H)	A2 20 40	;
3502H	ADDB 20H,02H	75 02 20	;
3505H	LD 42H,(20H)	A2 20 42	;
3508H	LD 20H,80A8H	A1 A8 80 20	;
350CH	LD 50H,(20H)	A2 20 50	;
350FH	ADDB 20H,02H	75 02 20	;
3512H	LD 52H,(20H)	A2 20 52	;
3515H	ADD E0H,40H	64 40 E0	;
3518H	ADDC E2H,42H	A4 42 E2	;
351BH	ADDC E4H,00H	A4 00 E4	;
351EH	ADD E0H,50H	64 50 E0	;
3521H	ADDC E2H,52H	A4 52 E2	;
3524H	ADDC E4H,00H	A4 00 E4	;
3527H	LD 20H,B800H	A1 00 B8 20	;
352BH	ST E0H,(20H)	C2 20 E0	;
352EH	ADDB 20H,02H	75 02 20	;
3531H	ST E2H,(20H)	C2 20 E2	;

3534H	LD C4H,E0H	A0 E0 C4	;
3537H	LD C0H,E2H	A0 E2 C0	;
353AH	LD C2H,E4H	A0 E4 C2	;
353DH	LD C6H,96A0H	A1 A0 96 C6	;
3541H	LD C8H,574BH	A1 4B 57 C8	;
3545H	CALL DISPIN	EF AE 03	;
3548H	P.F.AVGE LD 20H,806CH	A1 6C 80 20	;determine average value of
354CH	LD E0H,(20H)	A2 20 E0	; the power factor
354FH	ADDB 20H,02H	75 02 20	;
3552H	LD E2H,(20H)	A2 20 E2	;
3555H	LD 20H,808CH	A1 8C 80 20	;
3559H	LD 40H,(20H)	A2 20 40	;
355CH	ADDB 20H,02H	75 02 20	;
355FH	LD 42H,(20H)	A2 20 42	;
3562H	LD 20H,80ACH	A1 AC 80 20	;
3566H	LD 50H,(20H)	A2 20 50	;
3569H	ADDB 20H,02H	75 02 20	;
356CH	LD 52H,(20H)	A2 20 52	;
356FH	ADD E0H,40H	64 40 E0	;
3572H	ADDC E2H,42H	A4 42 E2	;
3575H	ADD E0H,50H	64 50 E0	;
3578H	ADDC E2H,52H	A4 52 E2	;
357BH	LD E4H,00H	A0 00 E4	;
357EH	LD E6H,0003H	A1 03 00 E6	;
3582H	CALL DIV	EF 6D 02	;
3585H	LD C2H,00H	A0 00 C2	;
3588H	LD C0H,EAH	A0 EA C0	;
358BH	LD C4H,E8H	A0 E8 C4	;
358EH	LD C6H,9720H	A1 20 97 C6	;
3592H	LD C8H,2020H	A1 20 20 C8	;
3596H	CALL DISPIN	EF 5D 03	;
3599H	TOTACPOW LD 20H,8070H	A1 70 80 20	;determine average active
359DH	LD E0H,(20H)	A2 20 E0	; power
35A0H	ADDB 20H,02H	75 02 20	;
35A3H	LD E2H,(20H)	A2 20 E2	;
35A6H	LD 20H,8090H	A1 90 80 20	;
35AAH	LD 40H,(20H)	A2 20 40	;
35ADH	ADDB 20H,02H	75 02 20	;
35BOH	LD 42H,(20H)	A2 20 42	;
35B3H	LD 20H,80B0H	A1 B0 80 20	;
35B7H	LD 50H,(20H)	A2 20 50	;
35BAH	ADDB 20H,02H	75 02 20	;
35BDH	LD 52H,(20H)	A2 20 52	;
35C0H	LD E4H,00H	A0 00 E4	;
35C3H	ADD E0H,40H	64 40 E0	;
35C6H	ADDC E2H,42H	A4 42 E2	;
35C9H	ADDC E4H,00H	A4 00 E4	;
35CCH	ADD E0H,50H	64 50 E0	;
35CFH	ADDC E2H,52H	A4 52 E2	;
35D2H	ADDC E4H,00H	A4 00 E4	;
35D5H	LD C4H,E0H	A0 E0 C4	;
35D8H	LD C0H,E2H	A0 E2 C0	;

35DBH	LD C2H,E4H	A0 E4 C2	;
35DEH	LD C6H,96E0H	A1 E0 96 C6	;
35E2H	LD C8H,574BH	A1 4B 57 C8	;
35E6H	CALL DISPIN	EF 0D 03	;
35E9H	FREQAVGE LD 20H,80FEH	A1 FE 80 20	;determine average frequency
35EDH	CMP 00H,(20H)	8A 20 00	;
35FOH	JE NONALT4	DF 6F	;
35F2H	LD E0H,00H	A0 00 E0	;
35F5H	LD E2H,00H	A0 00 E2	;
35F8H	LD 20H,8002H	A1 02 80 20	;
35FCH	CMP 00H,(20H)	8A 20 00	;
35FFH	JE NONALT1	DF 13	;
3601H	LD 20H,8074H	A1 74 80 20	;
3605H	LD 30H,(20H)	A2 20 30	;
3608H	ADDB 20H,02H	75 02 20	;
360BH	LD 32H,(20H)	A2 20 32	;
360EH	ADD E0H,30H	64 30 E0	;
3611H	ADDC E2H,32H	A4 32 E2	;
3614H	NONALT1 LD 20H,8022H	A1 22 80 20	;
3618H	CMP 00H,(20H)	8A 20 00	;
361BH	JE NONALT2	DF 13	;
361DH	LD 20H,8094H	A1 94 80 20	;
3621H	LD 30H,(20H)	A2 20 30	;
3624H	ADDB 20H,02H	75 02 20	;
3627H	LD 32H,(20H)	A2 20 32	;
362AH	ADD E0H,30H	64 30 E0	;
362DH	ADDC E2H,32H	A4 32 E2	;
3630H	NONALT2 LD 20H,8042H	A1 42 80 20	;
3634H	CMP 00H,(20H)	8A 20 00	;
3637H	JE NONALT3	DF 13	;
3639H	LD 20H,80B4H	A1 B4 80 20	;
363DH	LD 30H,(20H)	A2 20 30	;
3640H	ADDB 20H,02H	75 02 20	;
3643H	LD 32H,(20H)	A2 20 32	;
3646H	ADD E0H,30H	64 30 E0	;
3649H	ADDC E2H,32H	A4 32 E2	;
364CH	NONALT3 LD E4H,00H	A0 00 E4	;
364FH	LD E6H,52H	A0 52 E6	;
3652H	CALL DIV	EF 9D 01	;
3655H	LD C2H,00H	A0 00 C2	;
3658H	LD C0H,EAH	A0 EA C0	;
365BH	LD C4H,E8H	A0 E8 C4	;
365EH	LJMP NONALT5	E7 09 00	;
3661H	NONALT4 LD C2H,00H	A0 00 C2	;
3664H	LD C0H,00H	A0 00 C0	;
3667H	LD C4H,00H	A0 00 C4	;
366AH	NONALT5 LD C6H,9760H	A1 60 97 C6	;
366EH	LD C8H,5A48H	A1 48 5A C8	;
3672H	CALL DISPIN	EF 81 02	;
3675H	TOTCONS LD 30H,8078H	A1 78 80 30	;determine total power
3679H	LD E0H,(30H)	A2 30 E0	; consumption
367CH	ADDB 30H,02H	75 02 30	;

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367FH      LD E2H,(30H)      A2 30 E2      ;
3682H      ADDB 30H,02H      75 02 30      ;
3685H      LD E4H,(30H)      A2 30 E4      ;
3688H      LD 50H,8098H      A1 98 80 50    ;
368CH      LD 60H,(50H)      A2 50 60      ;
368FH      ADDB 50H,02H      75 02 50      ;
3692H      LD 62H,(50H)      A2 50 62      ;
3695H      ADDB 50H,02H      75 02 50      ;
3698H      LD 64H,(50H)      A2 50 64      ;
369BH      LD 70H,80B8H      A1 B8 80 70    ;
369FH      LD 80H,(70H)      A2 70 80      ;
36A2H      ADDB 70H,02H      75 02 70      ;
36A5H      LD 82H,(70H)      A2 70 82      ;
36A8H      ADDB 70H,02H      75 02 70      ;
36ABH      LD 84H,(70H)      A2 70 84      ;
36AEH      ADD E0H,60H       64 60 E0      ;
36B1H      ADDC E2H,62H      A4 62 E2      ;
36B4H      ADDC E4H,64H      A4 64 E4      ;
36B7H      ADD E0H,80H       64 80 E0      ;
36BAH      ADDC E2H,82H      A4 82 E2      ;
36BDH      ADDC E4H,84H      A4 84 E4      ;
36C0H      LD C4H,E0H        A0 E0 C4      ;
36C3H      LD C0H,E2H        A0 E2 C0      ;
36C6H      LD C2H,E4H        A0 E4 C2      ;
36C9H      LD C6H,97A0H      A1 A0 97 C6    ;
36CDH      LD C8H,484BH      A1 4B 48 C8    ;
36D1H      CALL DISPIN      EF 22 02      ;
36D4H      TOTDEMAND LD 20H,D800H      A1 00 B8 20    ;determine maximum 15-Min.
36D8H      LD 30H,(20H)      A2 20 30      ; Demand aggregate
36DBH      LD 50H,(20H)      A2 20 50      ;
36DEH      ADDB 20H,02H      75 02 20      ;
36E1H      LD 32H,(20H)      A2 20 32      ;
36E4H      LD 52H,(20H)      A2 20 52      ;
36E7H      ADDB 20H,02H      75 02 20      ;
36EAH      LD 34H,(20H)      A2 20 34      ;15-Min. Demand addr. register
36EDH      ADDB 20H,02H      75 02 20      ; is in register 34H
36F0H      LD 36H,(20H)      A2 20 36      ;current 15-Min. Demand total
36F3H      ADDB 20H,02H      75 02 20      ; V.I is in registers 36H,
36F6H      LD 38H,(20H)      A2 20 38      ; 38H,3AH
36F9H      ADDB 20H,02H      75 02 20      ;
36FCH      LD 3AH,(20H)      A2 20 3A      ;
36FFH      LD 40H,(34H)      A2 34 40      ;oldest V.I value is in
3702H      ADDB 34H,02H      75 02 34      ; registers 40H,42H
3705H      LD 42H,(34H)      A2 34 42      ;
3708H      ADD 36H,30H       64 30 36      ;calculate new 15-Min. Demand
370BH      ADDC 38H,32H      A4 32 38      ; total V.I by subtracting
370EH      ADDC 3AH,00H      A4 00 3A      ; oldest V.I value and adding
3711H      SUB 36H,40H       68 40 36      ; current V.I value
3714H      SUBC 38H,42H      A8 42 38      ;
3717H      SUBC 3AH,00H      A8 00 3A      ;
371AH      ST 3AH,(20H)      C2 20 3A      ;store new 15-Min. Demand
371DH      SUBB 20H,02H      79 02 20      ; total

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3720H      ST 38H,(20H)      C2 20 38      ;
3723H      SUBB 20H,02H      79 02 20      ;
3726H      ST 36H,(20H)      C2 20 36      ;
3729H      SUBB 20H,02H      79 02 20      ;
372CH      ST 52H,(34H)      C2 34 52      ;replace oldest V.I value with
372FH      SUBB 34H,02H      79 02 34      ; current V.I value
3732H      ST 50H,(34H)      C2 34 50      ;
3735H      LD 56H,36H        A0 36 56      ;compare new 15-Min. Demand
3738H      LD 58H,38H        A0 38 58      ; total with maximum 15-Min.
373BH      LD 5AH,3AH        A0 3A 5A      ; Demand total, and store the
373EH      LD 20H,6088H      A1 88 60 20  ; larger value as the new
3742H      LD 40H,(20H)      A2 20 40      ; maximum 15-Min. Demand
3745H      LD 50H,(20H)      A2 20 50      ; aggregate total
3748H      ADDB 20H,02H      75 02 20      ;
374BH      LD 42H,(20H)      A2 20 42      ;
374EH      LD 52H,(20H)      A2 20 52      ;
3751H      ADDB 20H,02H      75 02 20      ;
3754H      LD 44H,(20H)      A2 20 44      ;
3757H      LD 54H,(20H)      A2 20 54      ;
375AH      SUB 36H,40H        68 40 36      ;
375DH      SUBC 38H,42H      A8 42 38      ;
3760H      SUBC 3AH,44H      A8 44 3A      ;
3763H      JC KW.DEM.14      DB 14         ;
3765H      ST 54H,(20H)      C2 20 54      ;
3768H      SUBB 20H,02H      79 02 20      ;
376BH      ST 52H,(20H)      C2 20 52      ;
376EH      SUBB 20H,02H      79 02 20      ;
3771H      ST 50H,(20H)      C2 20 50      ;
3774H      LJMP KW.DEM.24     E7 0F 00      ;
3777H      KW.DEM.14 ST 5AH,(20H) C2 20 5A      ;
377AH      SUBB 20H,02H      79 02 20      ;
377DH      ST 58H,(20H)      C2 20 58      ;
3780H      SUBB 20H,02H      79 02 20      ;
3783H      ST 56H,(20H)      C2 20 56      ;
3786H      KW.DEM.24 LD E0H,(20H) A2 20 E0      ;divide maximum 15-Min. Demand
3789H      ADDB 20H,02H      75 02 20      ; aggregate total by 450 to
378CH      LD E2H,(20H)      A2 20 E2      ; obtain value for 15-Min.
378FH      ADDB 20H,02H      75 02 20      ; Demand display
3792H      LD E4H,(20H)      A2 20 E4      ;
3795H      LD E6H,01C2H      A1 C2 01 E6      ;
3799H      CALL DIV          EF 56 00      ;
379CH      ADD 34H,0004H      65 04 00 34      ;increment address pointer to
37A0H      CMP 34H,BF28H      89 28 BF 34      ; next oldest aggregate V.I
37A4H      JNE KW.DEM.34      D7 04         ; value
37A6H      SUB 34H,0708H      69 08 07 34      ;
37AAH      KW.DEM.34 LD 20H,B804H A1 04 B8 20      ;
37AEH      ST 34H,(20H)      C2 20 34      ;
37B1H      LD C2H,00H        A0 00 C2      ;display 15-Min. Demand
37B4H      LD C0H,EAH        A0 EA C0      ; aggregate value
37B7H      LD C4H,E8H        A0 E8 C4      ;
37BAH      LD C6H,97E0H      A1 E0 97 C6      ;
37BEH      LD C8H,574BH      A1 4B 57 C8      ;

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37C2H          CALL DISPIN      EF 31 01      ;

                                     DISPLAY

37C5H  DISPLAY  LD A8H,E800H      A1 00 E8 A8      ;continuously output display
37C9H          LD AAH,(A8H)      A2 A8 AA          ; RAM until 'C25 interrupts
37CCH          ADD AAH,20H      65 20 00 AA      ;
37D0H          LDB ACH,0CH      B1 0C AC          ;
37D3H          LD AEH,E016H     A1 16 E0 AE      ;
37D7H  DISPLAY1 LD B0H,(AAH)     A2 AA B0          ;
37DAH          ST B0H,(AEH)     C2 AE B0          ;
37DDH          DCRB (ACH)      15 AC          ;
37DFH          JE DISPLAY2     DF 0B          ;
37E1H          DCR AEH         05 AE          ;
37E3H          DCR AEH         05 AE          ;
37E5H          INC AAH         07 AA          ;
37E7H          INC AAH         07 AA          ;
37E9H          LJMP DISPLAY1    E7 EB FF          ;
37ECH  DISPLAY2 JBC bit4,09H     34 09 D6      ;jump to REPEAT if HSI.0 goes
37EFH          LJMP REPEAT      E7 C5 EA      ; high; otherwise to DISPLAY
37F2H          DIV
380DH          Sqrt
38F6H          DISPIN
3C2FH          MUL

3C7DH  POWEROFF PUSHF           F2              ;EXTINT interrupt routine
3C7EH          LD 20H,6000H     A1 00 60 20      ; for storing calibration
3C82H          LD 22H,(20H)     A2 20 22          ; values in EEPROM when
3C85H          ANDB PORT1,0BFH  71 BF 0F          ; power goes off
3C88H          NOP,NOP,NOP     FD FD FD
3C8BH          ST 22H,(20H)     C2 20 22
3C8EH          NOP,NOP,NOP     FD FD FD
3C91H          ORB PORT1,40H    91 40 0F
3C94H          POP 20H         CC 20
3C96H          POP 20H         CC 20
3C98H  ENDLESS  JUMP ENDLESS    E7 FD FF

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DIV SubroutineInputs

Dividend in (E0)-(E5)

Divisor in (E6)-(E7)

Outputs

Quotient in (E8)-(EB)

<u>Address</u>		<u>Mnemonic</u>	<u>Object Code</u>	<u>Comments</u>
0000H	DIV:	PUSHF	F2	;push flag register
0001H		LD (E4),(DA)	A0 E4 DA	;move (E4) to (DA)
0004H		LD (E2),(D8)	A0 E2 D8	;move (E2) to (D8)
0007H		LD (E6),(DC)	A0 E6 DC	;move (E6) to (DC)
000AH		DIV (DC),(D8)	8C DC D8	;divide (D8) by (DC)
000DH		LD (D8),(EA)	A0 D8 EA	;put quotient in (EA)
0010H		LD (E0),(D8)	A0 E0 D8	;move (E0) to (D8)
0013H		DIV (DC),(D8)	8C DC D8	;divide (D8) by (DC)
0016H		LD (D8),(E8)	A0 D8 E8	;put quotient in (E8)
0019H		POPF	F3	;pop flag register
001AH		RET	F0	;return to main routine

MUL SubroutineInputs

Multiplicand in (80)-(85)

Multiplier in (86)-(89)

Outputs

Product in (B0)-(B9)

<u>Address</u>		<u>Mnemonic</u>	<u>Object Code</u>	<u>Comments</u>
0000H	MUL:	PUSHF	F2	;push flag register
0001H		LD B0H,00H	A0 00 B0	;clear (B0) to (B9)
0004H		LD B2H,00H	A0 00 B2	;
0007H		LD B4H,00H	A0 00 B4	;
000AH		LD B6H,00H	A0 00 B6	;
000DH		LD B8H,00H	A0 00 B8	;
0010H		MULU 90H,86H,80H	4C 80 86 90	;create partial products
0014H		MULU 94H,86H,82H	4C 82 86 94	;
0018H		MULU 98H,88H,80H	4C 80 88 98	;
001CH		MULU 9CH,88H,82H	4C 82 88 9C	;
0020H		MULU A0H,86H,84H	4C 84 86 A0	;
0024H		MULU A4H,88H,84H	4C 84 88 A4	;
0028H		LD B0H,90H	A0 90 B0	;add the partial products
002BH		LD B2H,92H	A0 92 B2	;
002EH		ADD B2H,94H	64 94 B2	;
0031H		ADDC B4H,96H	A4 96 B4	;
0034H		ADD B2H,98H	64 98 B2	;
0037H		ADDC B4H,9AH	A4 9A B4	;
003AH		ADD B4H,9CH	64 9C B4	;
003DH		ADDC B6H,9EH	A4 9E B6	;
0040H		ADD B4H,A0H	64 A0 B4	;
0043H		ADDC B6H,A2H	A4 A2 B6	;
0046H		ADD B6H,A4H	64 A4 B6	;
0049H		ADDC B8H,A6H	A4 A6 B8	;
004CH		POPF	F3	;pop flag register
004DH		RET	F0	;return to main routine

SQRT SubroutineInput

(E8)-(EB) = 32-bit integer input

Output

(B4)-(B5) = 16-bit square root of input

<u>Address</u>		<u>Mnemonic</u>	<u>Object Code</u>	<u>Comments</u>
0000H	SQRT:	PUSHF	F2	;push flag register
0001H		CLR B4	01 B4	;clear (B4)
0003H		CLR B6	01 B6	;clear (B6)
0005H		CLR B8	01 B8	;clear (B8)
0007H		CLR BA	01 BA	;clear (BA)
0009H		CLR BC	01 BC	;clear (BC)
000BH		LDB (AE),(EB)	B0 EB AE	;move (EB) to (AE)
000EH		SHRB (AE),04H	18 04 AE	;shift (AE) 4 bits right
0011H		SETC	F9	;set carry bit
0012H		CMPB (AE),09H	99 09 AE	;compare (AE) with 09H
0015H		JNC ONE	D3 06	;jump if borrow to ONE
0017H		LDB (B4),03H	B1 03 B4	;put 03H in (B4)
001AH		LJMP TWO	E7 15 00	;jump to TWO
001DH	ONE:	SETC	F9	;set carry bit
001EH		CMPB (AE),04H	99 04 AE	;compare (AE) with 04H
0021H		JNC THREE	D3 06	;jump if borrow to THREE
0023H		LDB (B4),02H	B1 02 B4	;put 02H in (B4)
0026H		LJMP TWO	E7 09 00	;jump to TWO
0029H	THREE:	SETC	F9	;set carry bit
002AH		CMPB (AE),01H	99 01 AE	;compare (AE) with 01H
002DH		JNC TWO	D3 03	;jump if borrow to TWO
002FH		LDB (B4),01H	B1 01 B4	;put 01H in (B4)
0032H	TWO:	LDB (BC),(B4)	B0 B4 BC	;move (B4) to (BC)
0035H		LDB (CO),(B4)	B0 B4 CO	;move (B4) to (CO)
0038H		MULUB (CO).(BC)	7C CO BC	;mulub (CO).(BC)=(BC)
003BH		SUBB (AE)-(BC)	58 BC AE B8	;subb (AE)-(BC)=(B8)
003FH		LDB (AF),07H	B1 07 AF	;put 07H in (AF)
0042H	FIVE:	SHLL (E8),04H	0D 04 E8	;shift (E8)-(EB) 4 bits left
0045H		SHLL (B8),04H	0D 04 B8	;shift (B8)-(BB) 4 bits left
0048H		LDB (AE),(EB)	B0 EB AE	;move (EB) to (AE)
004BH		SHRB (AE),04H	18 04 AE	;shift (AE) 4 bits right
004EH		ORB (B8),(AE)	90 AE B8	;ORB (B8) with (AE)
0051H		SHLL (B4),03H	0D 03 B4	;shift (B4)-(B7) 3 bits left
0054H		ADD (B4),03H	75 03 B4	;add 03H to (B4)
0057H		LDB (BC),03H	B1 03 BC	;put 03H in (BC)
005AH		LD (C4),(B4)	A0 B4 C4	;move (B4) to (C4)
005DH		LD (CC),(B4)	A0 B4 CC	;move (B4) to (CC)
0060H		LD (C6),(B6)	A0 B6 C6	;move (B6) to (C6)
0063H		LD (CE),(B6)	A0 B6 CE	;move (B6) to (CE)
0066H		LD (C8),(B8)	A0 B8 C8	;move (B8) to (C8)

0069H	LD (CA),(BA)	A0 BA CA	;move (BA) to (CA)
006CH	SHLL (C4),01H	0D 01 C4	;shift (C4)-(C7) 1 bit left
006FH	ADD (CC),(C4)	64 CC C4	;(CC)+(C4)=(C4)
0072H	ADDC (CE),(C6)	A4 CE C6	;(CE)+(C6)+C=(C6)
0075H	LD (CC),(C4)	A0 C4 CC	;move (C4) to (CC)
0078H	LD (CE),(C6)	A0 C6 CE	;move (C6) to (CE)
007BH	SETC	F9	;set carry bit
007CH	SUB (C8)-(C4)	68 C4 C8	;(C8)-(C4)=(C8)
007FH	SUBC (CA)-(C6)	A8 C6 CA	;(CA)-(C6)-B=(CA)
0082H	JC FOUR	DB 4D	;jump if borrow to FOUR
0084H	DCRB (B4)	15 B4	;decrement (B4)
0086H	DCRB (BC)	15 BC	;decrement (BC)
0088H	LD (C4),(B4)	A0 B4 C4	;move (B4) to (C4)
008BH	LD (C6),(B6)	A0 B6 C6	;move (B6) to (C6)
008EH	LD (C8),(B8)	A0 B8 C8	;move (B8) to (C8)
0091H	LD (CA),(BA)	A0 BA CA	;move (BA) to (CA)
0094H	SHLL (C4),01H	0D 01 C4	;shift (C4) 1 bit left
0097H	LD (CC),(C4)	A0 C4 CC	;move (C4) to (CC)
009AH	LD (CE),(C6)	A0 C6 CE	;move (C6) to (CE)
009DH	SETC	F9	;set carry bit
009EH	SUB (C8)-(C4)	68 C4 C8	;(C8)-(C4)=(C8)
00A1H	SUBC (CA)-(C6)	A8 C6 CA	;(CA)-(C6)-B=(CA)
00A4H	JC FOUR	DB 2B	;jump if borrow to FOUR
00A6H	DCRB (B4)	15 B4	;decrement (B4)
00A8H	DCRB (BC)	15 BC	;decrement (BC)
00AAH	LD (C4),(B4)	A0 B4 C4	;move (B4) to (C4)
00ADH	LD (CC),(B4)	A0 B4 CC	;move (B4) to (CC)
00BOH	LD (C6),(B6)	A0 B6 C6	;move (B6) to (C6)
00B3H	LD (CE),(B6)	A0 B6 CE	;move (B6) to (CE)
00B6H	LD (C8),(B8)	A0 B8 C8	;move (B8) to (C8)
00B9H	LD (CA),(BA)	A0 BA CA	;move (BA) to (CA)
00BCH	SETC	F9	;set carry bit
00BDH	SUB (C8)-(C4)	68 C4 C8	;(C8)-(C4)=(C8)
00COH	SUBC (CA)-(C6)	A8 C6 CA	;(CA)-(C6)-B=(CA)
00C3H	JC FOUR	DB 0C	;jump if borrow to FOUR
00C5H	LD (CC),0000H	A1 00 00 CC	;load (CC) with 0000H
00C9H	LD (CE),0000H	A1 00 00 CE	;load (CE) with 0000H
00CDH	DCRB (B4)	15 34	;decrement (B4)
00CFH	DCRB (BC)	15 BC	;decrement (BC)
00D1H	FOUR: SUB (B8)-(CC)	68 CC B8	;(B8)-(CC)=(B8)
00D4H	SUBC (BA)-(CE)	A8 CE BA	;(BA)-(CE)-B=(BA)
00D7H	SHRL (B4),03H	0C 03 B4	;shift (B4)-(B7) 3 bits right
00DAH	SHLL (B4),02H	0D 02 B4	;shift (B4)-(B7) 2 bits left
00DDH	ORB (B4),(BC)	90 BC B4	;ORB (B4) with (BC)
00E0H	DCRB (AF)	15 AF	;decrement (AF)
00E2H	JE SIX	DF 03	;jump to SIX if (AF)=0
00E4H	LJMP FIVE	E7 5B FF	;jump to FIVE
00E7H	SIX: POPF	F3	;pop flag register
00E8H	RET	F0	;return to main routine

DISPIN Subroutine

Autoranging 12-character display RAM loader for Intel 8096

Inputs

(C0)-(C3) = 32-bit integer input
 (C4)-(C5) = 16-bit fraction input
 (C6)-(C7) = RAM address in which first character is to be loaded
 (C8) = ASCII character to go in (RAM address+11)
 (C9) = ASCII character to go in (RAM address+12)

<u>Address</u>	<u>Mnemonic</u>	<u>Object Code</u>	<u>Comments</u>
0000H	PUSHF	F2	;push flag register
0001H	LD (CF),0000H	A1 00 00 CF	;put 0000H in (CF)
0005H	LD (D0),0030H	A1 30 00 D0	;put 0030H in (D0)
0009H	LD (D2),0030H	A1 30 00 D2	;put 0030H in (D2)
000DH	LD (D4),0030H	A1 30 00 D4	;put 0030H in (D4)
0011H	LD (D6),0030H	A1 30 00 D6	;put 0030H in (D6)
0015H	LD (D8),0030H	A1 30 00 D8	;put 0030H in (D8)
0019H	LD (DA),0030H	A1 30 00 DA	;put 0030H in (DA)
001DH	LD (DC),0030H	A1 30 00 DC	;put 0030H in (DC)
0021H	LD (DE),0030H	A1 30 00 DE	;put 0030H in (DE)
0025H	LD (E0),0030H	A1 30 00 E0	;put 0030H in (E0)
0029H	LD (E2),0030H	A1 30 00 E2	;put 0030H in (E2)
002DH	LD (E4),002EH	A1 2E 00 E4	;put 002EH in (E4)
0031H	LD (E6),0030H	A1 30 00 E6	;put 0030H in (E6)
0035H	LD (E8),0030H	A1 30 00 E8	;put 0030H in (E8)
0039H	LD (EA),0030H	A1 30 00 EA	;put 0030H in (EA)
003DH	LD (EC),0030H	A1 30 00 EC	;put 0030H in (EC)
0041H	LD (EE),0020H	A1 20 00 EE	;put 0020H in (EE)
0045H	LD (F0),0020H	A1 20 00 F0	;put 0020H in (F0)
0049H	LD (F2),0020H	A1 20 00 F2	;put 0020H in (F2)

Load (D0) to (E2) with the decimal equivalent of the contents of (C0)-(C3).
 The least significant digit is in (E2). Make any left-hand zeroes invisible.

004DH	START:	LD (A0),(C0)	A0 C0 A0	;load (A0) from (C0)
0050H		LD (A2),(C2)	A0 C2 A2	;load (A2) from (C2)
0053H	ONE:	SETC	F9	;set carry
0054H		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
0057H		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
005AH		SUB (A0),CA00H	69 00 CA A0	;subt. (A0)-CA00H
005EH		SUBC (A2),3B9AH	A9 9A 3B A2	;subt. (A2)-3B9AH-C
0062H		JNC TWO	D3 05	;jump if borrow to TWO
0064H		INCB (D0)	17 D0	;increment (D0)
0066H		LJMP ONE	E7 EA FF	;jump to ONE
0069H	TWO:	CMPB (D0),30H	99 30 D0	;compare (D0) with 30H
006CH		JNE THREE	D7 06	;if (D0)=30H, jump to THREE
006EH		SUBB (D0),10H	79 10 D0	;change (D0) to 20H
0071H		LJMP FOUR	E7 03 00	;jump to FOUR

0074H	THRE.:	ADDB (CF),01H	75 01 CF	;put 01H in (CF) if not 30H
0077H	FOUR:	LD (A0),(A4)	A0 A4 A0	;load (A4) from (A0)
007AH		LD (A2),(A6)	A0 A6 A2	;load (A6) from (A2)
007DH	FIVE:	SETC	F9	;set carry
007EH		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
0081H		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
0084H		SUB (A0),E100H	69 00 E1 A0	;subt. (A0)-E100H
0088H		SUBC (A2),05F5H	A9 F5 05 A2	;subt. (A2)-05F5H-C
008CH		JNC SIX	D3 05	;jump if borrow to SIX
008EH		INCB (D2)	17 D2	;increment (D2)
0090H		LJMP FIVE	E7 EA FF	;jump to FIVE
0093H	SIX:	CMPB (CF),00H	99 00 CF	;compare (CF) with 00H
0096H		JNE EIGHT	D7 0E	;if (CF)=00H, jump to EIGHT
0098H		CMPB (D2),30H	99 30 D2	;compare (D2) with 30H
009BH		JNE SEVEN	D7 06	;if (D2)=30H, jump to SEVEN
009DH		SUBB (D2),10H	79 10 D2	;change (D2) to 20H
00A0H		LJMP EIGHT	E7 03 00	;jump to EIGHT
00A3H	SEVEN:	ADDB (CF),01H	75 01 CF	;put 01H in (CF) if not 30H
00A6H	EIGHT:	LD (A0),(A4)	A0 A4 A0	;load (A4) from (A0)
00A9H		LD (A2),(A6)	A0 A6 A2	;load (A6) from (A2)
00ACH	NINE:	SETC	F9	;set carry
00ADH		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
00BOH		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
00B3H		SUB (A0),9680H	69 80 96 A0	;subt. (A0)-9680H
00B7H		SUBC (A2),0098H	A9 98 00 A2	;subt. (A2)-0098H-C
00BBH		JNC TEN	D3 05	;jump if borrow to TEN
00BDH		INCB (D4)	17 D4	;increment (D4)
00BFH		LJMP NINE	E7 EA FF	;jump to NINE
00C2H	TEN:	CMPB (CF),00H	99 00 CF	;compare (CF) with 00H
00C5H		JNE TEEN2	D7 0E	;if (CF)=00H, jump to TEEN2
00C7H		CMPB (D4),30H	99 30 D4	;compare (D4) with 30H
00CAH		JNE TEEN1	D7 06	;if (D4)=30H, jump to TEEN1
00CCH		SUBB (D4),10H	79 10 D4	;change (D4) to 20H
00CFH		LJMP TEEN2	E7 03 00	;jump to TEEN2
00D2H	TEEN1:	ADDB (CF),01H	75 01 CF	;put 01H in (CF) if not 30H
00D5H	TEEN2:	LD (A0),(A4)	A0 A4 A0	;load (A4) from (A0)
00D8H		LD (A2),(A6)	A0 A6 A2	;load (A6) from (A2)
00DBH	TEEN3:	SETC	F9	;set carry
00DCH		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
00DFH		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
00E2H		SUB (A0),4240H	69 40 42 A0	;subt. (A0)-4240H
00E6H		SUBC (A2),000FH	A9 0F 00 A2	;subt. (A2)-000FH-C
00EAH		JNC TEEN4	D3 05	;jump if borrow to TEEN4
00ECH		INCB (D6)	17 D6	;increment (D6)
00EEH		LJMP TEEN3	E7 EA FF	;jump to TEEN3
00F1H	TEEN4:	CMPB (CF),00H	99 00 CF	;compare (CF) with 00H
00F4H		JNE TEEN6	D7 0E	;if (CF)=00H, jump to TEEN6
00F6H		CMPB (D6),30H	99 30 D6	;compare (D6) with 30H
00F9H		JNE TEEN5	D7 06	;if (D6)=30H, jump to TEEN5
00FBH		SUBB (D6),10H	79 10 D6	;change (D6) to 20H
00FEH		LJMP TEEN6	E7 03 00	;jump to TEEN6
0101H	TEEN5:	ADDB (CF),01H	75 01 CF	;put 01H in (CF) if not 30H

0104H	TEEN6:	LD (A0),(A4)	A0 A4 A0	;load (A4) from (A0)
0107H		LD (A2),(A6)	A0 A6 A2	;load (A6) from (A2)
010AH	TEEN7:	SETC	F9	;set carry
010BH		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
010EH		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
0111H		SUB (A0),86A0H	69 A0 86 A0	;subt. (A0)-86A0H
0115H		SUBC (A2),0001H	A9 01 00 A2	;subt. (A2)-0001H-C
0119H		JNC TEEN8	D3 05	;jump if borrow to TEEN8
011BH		INCB (D8)	17 D8	;increment (D8)
011DH		LJMP TEEN7	E7 EA FF	;jump to TEEN7
0120H	TEEN8:	CMPB (CF),00H	99 00 CF	;compare (CF) with 00H
0123H		JNE TWENTY	D7 0E	;if (CF)=00H, jump to TWENTY
0125H		CMPB (D8),30H	99 30 D8	;compare (D8) with 30H
0128H		JNE TEEN9	D7 06	;if (D8)=30H, jump to TEEN9
012AH		SUBB (D8),10H	79 10 D8	;change (D8) to 20H
012DH		LJMP TWENTY	E7 03 00	;jump to TWENTY
0130H	TEEN9:	ADDB (CF),01H	75 01 CF	;put 01H in (CF) if not 30H
0133H	TWENTY:	LD (A0),(A4)	A0 A4 A0	;load (A4) from (A0)
0136H		LD (A2),(A6)	A0 A6 A2	;load (A6) from (A2)
0139H	TWENTY1:	SETC	F9	;set carry
013AH		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
013DH		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
0140H		SUB (A0),2710H	69 10 27 A0	;subt. (A0)-2710H
0144H		SUBC (A2),0000H	A9 00 00 A2	;subt. (A2)-0000H-C
0148H		JNC TWENTY2	D3 05	;jump if borrow to TWENTY2
014AH		INCB (DA)	17 DA	;increment (DA)
014CH		LJMP TWENTY1	E7 EA FF	;jump to TWENTY1
014FH	TWENTY2:	CMPB (CF),00H	99 00 CF	;compare (CF) with 00H
0152H		JNE TWENTY4	D7 0E	;if (CF)=00H, jump to TWENTY4
0154H		CMPB (DA),30H	99 30 DA	;compare (DA) with 30H
0157H		JNE TWENTY3	D7 06	;if (DA)=30H, jump to TWENTY3
0159H		SUBB (DA),10H	79 10 DA	;change (DA) to 20H
015CH		LJMP TWENTY4	E7 03 00	;jump to TWENTY4
015FH	TWENTY3:	ADDB (CF),01H	75 01 CF	;put 01H in (CF) if not 30H
0162H	TWENTY4:	LD (A0),(A4)	A0 A4 A0	;load (A4) from (A0)
0165H		LD (A2),(A6)	A0 A6 A2	;load (A6) from (A2)
0168H	TWENTY5:	SETC	F9	;set carry
0169H		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
016CH		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
016FH		SUB (A0),03E8H	69 E8 03 A0	;subt. (A0)-03E8H
0173H		SUBC (A2),0000H	A9 00 00 A2	;subt. (A2)-0000H-C
0177H		JNC TWENTY6	D3 05	;jump if borrow to TWENTY6
0179H		INCB (DC)	17 DC	;increment (DC)
017BH		LJMP TWENTY5	E7 EA FF	;jump to TWENTY5
017EH	TWENTY6:	CMPB (CF),00H	99 00 CF	;compare (CF) with 00H
0181H		JNE TWENTY8	D7 0E	;if (CF)=00H, jump to TWENTY8
0183H		CMPB (DC),30H	99 30 DC	;compare (DC) with 30H
0186H		JNE TWENTY7	D7 06	;if (DC)=30H, jump to TWENTY7
0188H		SUBB (DC),10H	79 10 DC	;change (DC) to 20H
018BH		LJMP TWENTY8	E7 03 00	;jump to TWENTY8
018EH	TWENTY7:	ADDB (CF),01H	75 01 CF	;put 01H in (CF) if not 30H
0191H	TWENTY8:	LD (A0),(A4)	A0 A4 A0	;load (A4) from (A0)

0194H		LD (A2),(A6)	A0 A6 A2	;load (A6) from (A2)
0197H	TWENTY9:	SETC	F9	;set carry
0198H		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
019BH		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
019EH		SUB (A0),0064H	69 64 00 A0	;subt. (A0)-0064H
01A2H		SUBC (A2),0000H	A9 00 00 A2	;subt. (A2)-0000H-C
01A6H		JNC THIRTY	D3 05	;jump if borrow to THIRTY
01A8H		INCB (DE)	17 DE	;increment (DE)
01AAH		LJMP TWENTY9	E7 EA FF	;jump to TWENTY9
01ADH	THIRTY:	CMPB (CF),00H	99 00 CF	;compare (CF) with 00H
01BOH		JNE THIRTY2	D7 0E	;if (CF)=00H, jump to THIRTY2
01B2H		CMPB (DE),30H	99 30 DE	;compare (DE) with 30H
01B5H		JNE THIRTY1	D7 06	;if (DE)=30H, jump to THIRTY1
01B7H		SUBB (DE),10H	79 10 DE	;change (DE) to 20H
01BAH		LJMP THIRTY2	E7 03 00	;jump to THIRTY2
01BDH	THIRTY1:	ADDB (CF),01H	75 01 CF	;put 01H in (CF) if not 30H
01COH	THIRTY2:	LD (A0),(A4)	A0 A4 A0	;load (A4) from (A0)
01C3H		LD (A2),(A6)	A0 A6 A2	;load (A6) from (A2)
01C6H	THIRTY3:	SETC	F9	;set carry
01C7H		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
01CAH		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
01CDH		SUB (A0),000AH	69 0A 00 A0	;subt. (A0)-000AH
01D1H		SUBC (A2),0000H	A9 00 00 A2	;subt. (A2)-0000H-C
01D5H		JNC THIRTY4	D3 05	;jump if borrow to THIRTY4
01D7H		INCB (E0)	17 E0	;increment (E0)
01D9H		LJMP THIRTY3	E7 EA FF	;jump to THIRTY3
01DCH	THIRTY4:	CMPB (CF),00H	99 00 CF	;compare (CF) with 00H
01DFH		JNE THIRTY5	D7 08	;if (CF)=00H, jump to THIRTY5
01E1H		CMPB (E0),30H	99 30 E0	;compare (E0) with 30H
01E4H		JNE THIRTY5	D7 03	;if (E0)=30H, jump to THIRTY5
01E6H		SUBB (E0),10H	79 10 E0	;change (E0) to 20H
01E9H	THIRTY5:	LD (A0),(A4)	A0 A4 A0	;load (A4) from (A0)
01ECH		LD (A2),(A6)	A0 A6 A2	;load (A6) from (A2)
01EFH	THIRTY6:	SETC	F9	;set carry
01F0H		SUB (A0),0001H	69 01 00 A0	;subt. (A0)-0001H
01F4H		SUBC (A2),0000H	A9 00 00 A2	;subt. (A2)-0000H-C
01F8H		JNC THIRTY7	D3 05	;jump if borrow to THIRTY7
01FAH		INCB (E2)	17 E2	;increment (E2)
01FCH		LJMP THIRTY6	E7 EA FF	;jump to THIRTY6

Load (E6) to (EA) with the decimal equivalent of the contents of (C4)-(C5).

01FFH	THIRTY7:	LD (A2),(C4)	A0 C4 A2	;load (A2) with (C4)
0202H		LD (A0),0000H	A1 00 00 A0	;load (A0) with 0000H
0206H	THIRTY8:	SETC	F9	;set carry
0207H		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
020AH		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
020DH		SUB (A0),9999H	69 99 99 A0	;subt. (A0)-9999H
0211H		SUBC (A2),1999H	A9 99 19 A2	;subt. (A2)-1999H-C
0215H		JNC THIRTY9	D3 05	;jump if borrow to THIRTY9
0217H		INCB (E6)	17 E6	;increment (E6)
0219H		LJMP THIRTY8	E7 EA FF	;jump to THIRTY8

021CH	THIRTY9:	LD (A0),(A4)	A0 A4 A0	;load (A0) with (A4)
021FH		LD (A2),(A6)	A0 A6 A2	;load (A2) with (A6)
0222H	FORTY:	SETC	F9	;set carry
0223H		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
0226H		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
0229H		SUB (A0),5C28H	69 28 5C A0	;subt. (A0)-5C28H
022DH		SUBC (A2),028FH	A9 8F 02 A2	;subt. (A2)-028FH-C
0231H		JNC FORTY1	D3 05	;jump if borrow to FORTY1
0233H		INCB (E8)	17 E8	;increment (E8)
0235H		LJMP FORTY	E7 EA FF	;jump to FORTY
0238H	FORTY1:	LD (A0),(A4)	A0 A4 A0	;load (A0) with (A4)
023BH		LD (A2),(A6)	A0 A6 A2	;load (A2) with (A6)
023EH	FORTY2:	SETC	F9	;set carry
023FH		ST (A0),(A4)	C0 A4 A0	;store (A0) at (A4)
0242H		ST (A2),(A6)	C0 A6 A2	;store (A2) at (A6)
0245H		SUB (A0),8937H	69 37 89 A0	;subt. (A0)-8937H
0249H		SUBC (A2),0041H	A9 41 00 A2	;subt. (A2)-0041H-C
024DH		JNC FORTY3	D3 05	;jump if borrow to FORTY3
024FH		INCB (EA)	17 EA	;increment (EA)
0251H		LJMP FORTY2	E7 EA FF	;jump to FORTY2
0254H	FORTY3:	LD (A0),(A4)	A0 A4 A0	;load (A0) with (A4)
0257H		LD (A2),(A6)	A0 A6 A2	;load (A2) with (A6)
025AH	FORTY4:	SETC	F9	;set carry
025BH		SUB (A0),8DB8H	69 B8 8D A0	;subt. (A0)-8DB8H
025FH		SUBC (A2),0006H	A9 06 00 A2	;subt. (A2)-0006H-C
0263H		JNC FORTY5	D3 05	;jump if borrow to FORTY5
0265H		INCB (EC)	17 EC	;increment (EC)
0267H		LJMP FORTY4	E7 F0 FF	;jump to FORTY4

Count the number of decimal integers, and store the result in (A3).

026AH	FORTY5:	LDB (A3),01H	B1 01 A3	;load (A3) with 01H
026DH		CMPB (E0),20H	99 20 E0	;compare (E0) with 20H
0270H		JNE FORTY6	D7 03	;if not 20H, jump to FORTY6
0272H		LJMP FIFTY5	E7 52 00	;jump to FIFTY5
0275H	FORTY6:	INCB (A3)	17 A3	;increment (A3)
0277H		CMPB (DE),20H	99 20 DE	;compare (DE) with 20H
027AH		JNE FORTY7	D7 03	;if not 20H, jump to FORTY7
027CH		LJMP FIFTY5	E7 48 00	;jump to FIFTY5
027FH	FORTY7:	INCB (A3)	17 A3	;increment (A3)
0281H		CMPB (DC),20H	99 20 DC	;compare (DC) with 20H
0284H		JNE FORTY8	D7 03	;if not 20H, jump to FORTY8
0286H		LJMP FIFTY5	E7 3E 00	;jump to FIFTY5
0289H	FORTY8:	INCB (A3)	17 A3	;increment (A3)
028BH		CMPB (DA),20H	99 20 DA	;compare (DA) with 20H
028EH		JNE FORTY9	D7 03	;if not 20H, jump to FORTY9
0290H		LJMP FIFTY5	E7 34 00	;jump to FIFTY5
0293H	FORTY9:	INCB (A3)	17 A3	;increment (A3)
0295H		CMPB (D8),20H	99 20 D8	;compare (D8) with 20H
0298H		JNE FIFTY	D7 03	;if not 20H, jump to FIFTY
029AH		LJMP FIFTY5	E7 2A 00	;jump to FIFTY5
029DH	FIFTY:	INCB (A3)	17 A3	;increment (A3)

029FH		CMPB (D6),20H	99 20 D6	;compare (D6) with 20H
02A2H		JNE FIFTY1	D7 03	;if not 20H, jump to FIFTY1
02A4H		LJMP FIFTY5	E7 20 00	;jump to FIFTY5
02A7H	FIFTY1:	INCB (A3)	17 A3	;increment (A3)
02A9H		CMPB (D4),20H	99 20 D4	;compare (D4) with 20H
02ACH		JNE FIFTY2	D7 03	;if not 20H, jump to FIFTY2
02AEH		LJMP FIFTY5	E7 16 00	;jump to FIFTY5
02B1H	FIFTY2:	INCB (A3)	17 A3	;increment (A3)
02B3H		CMPB (D2),20H	99 20 D2	;compare (D2) with 20H
02B6H		JNE FIFTY3	D7 03	;if not 20H, jump to FIFTY3
02B8H		LJMP FIFTY5	E7 0C 00	;jump to FIFTY5
02BBH	FIFTY3:	INCB (A3)	17 A3	;increment (A3)
02BDH		CMPB (D0),20H	99 20 D0	;compare (D0) with 20H
02COH		JNE FIFTY4	D7 03	;if not 20H, jump to FIFTY4
02C2H		LJMP FIFTY5	E7 02 00	;jump to FIFTY5
02C5H	FIFTY4:	INCB (A3)	17 A3	;increment (A3)

Drop some of the stored fraction values if the integer value is large.

02C7H	FIFTY5:	CLRC	F8	;clear carry
02C8H		CMPB (A3),09H	99 09 A3	;compare (A3) with 09H
02CBH		JC SIXTY	DB 02	;if above 08H, jump to FIFTY6
02CDH		INCB (A3)	17 A3	;increment (A3)
02CFH	FIFTY6:	SETC	F9	;set carry
02D0H		CMPB (A3),04H	99 04 A3	;compare (A3) with 04H
02D3H		JNC FIFTY7	D3 1E	;if below 04H, jump to FIFTY7
02D5H		LDB (EC),20H	B1 20 EC	;put 20H in (EC)
02D8H		SETC	F9	;set carry
02D9H		CMPB (A3),05H	99 05 A3	;compare (A3) with 05H
02DCH		JNC FIFTY7	D3 15	;if below 05H, jump to FIFTY7
02DEH		LDB (EA),20H	B1 20 EA	;put 20H in (EA)
02E1H		SETC	F9	;set carry
02E2H		CMPB (A3),06H	99 06 A3	;compare (A3) with 06H
02E5H		JNC FIFTY7	D3 0C	;if below 06H, jump to FIFTY7
02E7H		LDB (E8),20H	B1 20 E8	;put 20H in (E8)
02EAH		SETC	F9	;set carry
02EBH		CMPB (A3),07H	99 07 A3	;compare (A3) with 07H
02EEH		JNC FIFTY7	D3 03	;if below 07H, jump to FIFTY7
02FOH		LDB (E6),20H	B1 20 E6	;put 20H in (E6)

Load display RAM with the contents of ten of the registers (D0) to (F2).
The contents of register (A3) indicate where the registers are stored in the display RAM.

02F3H	FIFTY7:	LDB (A2),0AH	B1 0A A2	;put 0AH in (A2)
02F6H		LD (A0),(C6)	A0 C6 A0	;load (A0) with (C6)
02F9H		LDB (A5),00H	B1 00 A5	;put 00H in (A5)
02FCH		LDB (A4),0AH	B1 0A A4	;put 0AH in (A4)
02FFH		SUBB (A4)-(A3)	78 A3 A4	;subt. (A4)-(A3)
0302H		SHL (A4),01H	09 01 A4	;double (A4)
0305H		ADDB (A4),DOH	75 D0 A4	;add DOH to (A4)
0308H	FIFTY8:	LD (A8),((A4))	A2 A4 A8	;load (A8) with ((A4))

030BH	ST (A8),((A0))	C2 A0 A8	;store (A8) at ((A0))
030EH	DCRB (A2)	15 A2	;decrement (A2)
0310H	JE FIFTY9	DF 0B	;jump if 10 characters stored
0312H	INC (A4)	07 A4	;increment (A4)
0314H	INC (A4)	07 A4	;increment (A4)
0316H	INC (A0)	07 A0	;increment (A0)
0318H	INC (A0)	07 A0	;increment (A0)
031AH	LJMP FIFTY8	E7 EB FF	;jump to FIFTY8

Load positions 11 and 12 of display RAM with two ASCII characters.

031DH	FIFTY9:	INC (A0)	07 A0	;increment (A0)
031FH		INC (A0)	07 A0	;increment (A0)
0321H		LDB (A3),00H	B1 00 A3	;put 00H in (A3)
0324H		LDB (A5),00H	B1 00 A5	;put 00H in (A5)
0327H		LDB (A2),(C8)	B0 C8 A2	;load (A2) with (C8)
032AH		LDB (A4),(C9)	B0 C9 A4	;load (A4) with (C9)
032DH		ST (A2),((A0))	C2 A0 A2	;store (A2) at ((A0))
0330H		INC (A0)	07 A0	;increment (A0)
0332H		INC (A0)	07 A0	;increment (A0)
0334H		ST (A4),((A0))	C2 A0 A4	;store (A4) at ((A0))
0337H		POPF	F3	;pop flag register
0338H		RET	F0	;return to main routine

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