A 0.78mm^2 Co-Channel Interference Canceller in 130nm SOI RF CMOS with Novel Passive Phase Shifters and Combiner Circuitry

by

Mackenzie Brian Cook, B.Eng.

A thesis submitted to the Faculty of Graduate and Postdoctoral Affairs in partial fulfillment of the requirements for the degree of

Master of Applied Science

in

Electrical and Computer Engineering

Ottawa-Carleton Institute for Electrical and Computer Engineering
Carleton University
Ottawa, Ontario

Abstract

An increasingly congested frequency spectrum has presented an unfortunate opportunity for two independent radios on the same device to exist co-channel. Currently, co-channel coexistence requires temporal scheduling to prevent co-channel interference from disrupting downlink communications. This work develops a method of front end co-channel cancellation within the receive chain of a co-channel transceiver to allow for simultaneous operation.

An extremely compact co-channel interference canceller (CCIC) is presented. A polar modulator in a feed-forward path creates an inverted copy of the on-board interference signal at RF and recombines in the front end LNA for cancellation. The system contains novel phase shifters and digital capacitor architectures and a novel front end combination circuit. The system provides 6 bits of phase control and 5 bits of amplitude control and 25dB of cancellation is demonstrated. The measured IIP3 was +7dBm and the measured noise figure was 1.5dB with 14dB of LNA gain at 2.2GHz.

Acknowledgements

I would like to thank Skyworks Solutions Inc. in Kanata, Ontario for their extremely generous support of my work. Skyworks provided all of the design tools I needed and, in addition to the expertise I had at my disposal, they also fabricated my chips (two tape outs, nearly fifty variants) and provided custom testing and demonstration boards for my final design. I am also pleased to acknowledge the support of the National Science and Engineering Research Council (NSERC) for their support in the form of a Canada Graduate Scholarship (CGS-M).

This work would not have been possible without the support of my supervisor John Rogers. In addition to facilitating my partnership with Skyworks, he provided essential oversight and support for me, inside and outside of the context of my thesis. Furthermore, I doubt I would have been enrolled in a graduate program if it weren't for his involvement in my work at the bachelor's level since 2012.

Many people at Skyworks were essential to my success. In particular I want to thank John Nisbet and Steve Kovacic for their unwavering support of my work. Steve was the one who made this partnership happened and I simply could not be here without his efforts and support. John Nisbet was my project manager and his assistance and trust in my abilities really shaped my development over the more than 16 months I have worked with him. John Nisbet encouraged and supported my outside-the-box ideas, which ended up being essential to my thesis and led to four provisional patent filings at the time of writing. I would also like to thank Jam Zhou for being there for me inside and outside of work, and also to Abdulkareem Karar for his efforts in the fabrication of my evaluation boards. Skyworks was an incredible place for me to be and I am very grateful.

Table of Contents

List of Tables

List of Figures

List of Appendices

Chapter 1: Introduction

As technology continues to improve and provide faster communication services, the demand for said services rapidly grows. With staggering increases in data consuming applications such as YouTube and Netflix, accessible on mobile devices, the demand on the mobile network is unwavering. Mobile providers have access to a fixed frequency band on which to operate, and high demand inevitably leads to a crowded frequency spectrum. Therefore, spectral and temporal efficiency is of pivotal importance to both network providers and handset designers. Spectral efficiency refers to how much information can be conveyed in a period of time for a given bandwidth. The higher the efficiency, the more paying users can occupy a cell in the network. Temporal efficiency in this context refers to a handset's ability to utilize different radio standards simultaneously.

RF systems rely on the ability to isolate a desired received signal amongst energy generated by hundreds of sources. It is the job of the receiver to detect their signal of interest while rejecting all others. Modern RF circuits can tolerate blockers when they are sufficiently out of band by using filters. A bandpass filter at the front end of a superheterodyne receiver can mitigate the out of band blockers. For signals adjacent to the target band however, the filter will not sufficiently diminish the interference. Due to spectrum congestion, it is now possible for a blocker to be sufficiently close in frequency and space to overload the receiver and decrease the signal to noise ratio to zero. In other words, the ability to receive is greatly limited when there is a strong near-band interferer. A signal that occupies the adjacent band is called co-channel, and the act of hindering its operation is called co-channel interference, or CCI. This issue typically was not as

common when the frequency spectrum was less crowded. Today, nearly every person above the age of 16 owns and uses a mobile device and the spectrum is filled by different providers, cellular or otherwise. It is possible to operate at one frequency, and have a strong signal in the adjacent band nearby generating CCI. Fortunately, spatial attenuation increases by the square of the distance, so cellular devices can often tolerate external co-channel interferers due to their distance providing sufficient attenuation.

This problem became worse when multiple standards and radios began integrating onto a single mobile device. In modern telecommunication devices, a high powered transmitter of one radio is usually located within millimeters or centimeters of another radio's receiver. With the adoption of LTE (Long Term Evolution), or "4G" cellular, there is greater opportunity for a cellular device to self-interfere. Both Bluetooth and Wi-Fi operate at 2.4GHz. The LTE bands relevant to this discussion from the 3GPP Standards Update [1] are shown in Table I.

TABLE I: LTE BANDS NEAR 2.4GHZ

Band Number	Freq. Band (MHz)	Uplink (MHz)	Downlink (MHz)	Channel Bandwidth (MHz)
7	2600	2500 – 2570	2620 – 2690	5, 10, 15, 20
30	2300	2305 – 2315	2350 – 2360	5, 10
40	2300	2300 – 2400		5, 10, 15, 20
41	2500	2496 – 2690		5, 10, 15, 20

For this discussion, LTE will be the desired received signal, and Wi-Fi will be transmitting in the 2.4GHz band. At the output of the Wi-Fi transmitter, the transmitted energy will not only radiate outward from the antenna, but will also be picked up by the LTE receiver. If two radios are co-channel, it may be economical for a handset designer

to design the radios to share the same antenna, and therefore the leakage wouldn't need to radiate from the antenna to be picked up by the receiver.

If a Wi-Fi transmission (uplink) occurs at the same time as an LTE downlink, the Wi-Fi transmission's spectral leakage will raise the noise floor in the LTE band well above a weak desired signal, effectively reducing its Signal to Noise Ratio (SNR) to zero and blocking the LTE downlink. High powered signals may still be received, but the dynamic range – the difference between the minimum power received signal and maximum power – of the system will be severely degraded.

This thesis will explore a method of allowing simultaneous transmit and receive for two co-channel radios on the same device. There is a crucial difference between co-channel interference on board, and externally generated blockers: the offending signal is available. This makes signal cancellation a possibility; external signals are unknown and thus a copy cannot be created in order to facilitate cancellation. This work presents the design, fabrication, and testing of a Co-Channel Interference Canceller, or CCIC.

1.1 Thesis Outline

Chapter 2 will discuss the background literature of the topic and illustrate the different methods of addressing co-channel or self- interference, including a discussion of the research being done on full duplex radio – the simultaneous transmit and receive on the same frequency. Chapter 3 will describe the system level design including the system specifications provided and the circuit level specifications required for successful operation. Chapter 4 provides the circuit level design of the blocks of the system. Chapter 5 provides implementation and layout details system and sub-circuits. Chapter 6 provides the simulation results and Chapter 7 provides the measured results of the two prototype chips designed and outlines their testing. Chapter 8 will conclude the thesis, discuss the contributions this work has made, and discuss future work on the topic.

Chapter 2: Background

The issue of co-channel or self- interference in mobile systems has been known for a long time, and there have been a number of different approaches to attempt to mitigate it. This chapter will outline the different approaches taken to address co-channel interference (CCI).

The two main schools of thought on mitigating CCI are to reduce the antenna spatial coupling that causes the interference, or to accept its presence and eliminate it within the receiver. Antenna coupling reduction has been attempted by use of null-beam steering, or spatial filtering between systems; this attempts to direct an antenna null at the interferer's location in space. In the front end, signal conditioning of a sample of the transmit energy can be used to cancel the signal in hardware, but only if you have access to the interferer source.

2.1 Null-Beam Steering

Null-beam steering is used to direct a null of the receive antenna array in the direction from which an interferer is coming from. A null is a direction in space to which an antenna does not direct energy towards or receive energy from. This concept is known as spatial filtering and has long been known as an effective means to reduce CCI [2]. Briefly, beam steering requires an array of antennas. The direction in which the overall array propagates in the far field is determined by the summation of EM fields from each antenna. Due to the spatial separation, the phase of the signals from each antenna is not equal. At a single point in space, the net EM propagation will range from all in phase to anti-phase. Anti-phased signals sum to zero, producing a null, and in-phase produces "lobes" or beams. By controlling the phase of one or all of the branches in the antenna

array, the location of the lobes and/or nulls can be directed as desired. Beam steering is the act of directing the maximum of the lobe in a desired direction to maximize reception in that direction. Spatial filtering, or null-beam steering, is the act of positioning the null in the direction from which reception is undesirable. For CCI, a receive antenna array would position a null in the direction of the co-channel source, preventing its reception.

An implementation example in [3] demonstrates different algorithms to steer the null to the desired location. This concept is also found in [4] where they implement two modes in a diversity receiver: a maximize signal-to-noise ratio (normal diversity) mode, and a cancellation (spatial filter) mode. When CCI is an issue, they sacrifice the diversity gain in order to negate the interferer. A visual representation of this concept is shown in Fig. 1. The goal is to spatially null or filter the co-channel signal while maintaining the beam formation in the direction of the basestation.

This filtering in space is ideal for MIMO systems where the CCI is external. Unfortunately this method does not lend itself well to intra-device CCI, where the interferer is located on the same board. If two of the device's radios are co-channel, it is also likely that a mobile phone will make use of the same antenna for cost and space reduction measures. In this case, beam steering will not remove energy already within the system.

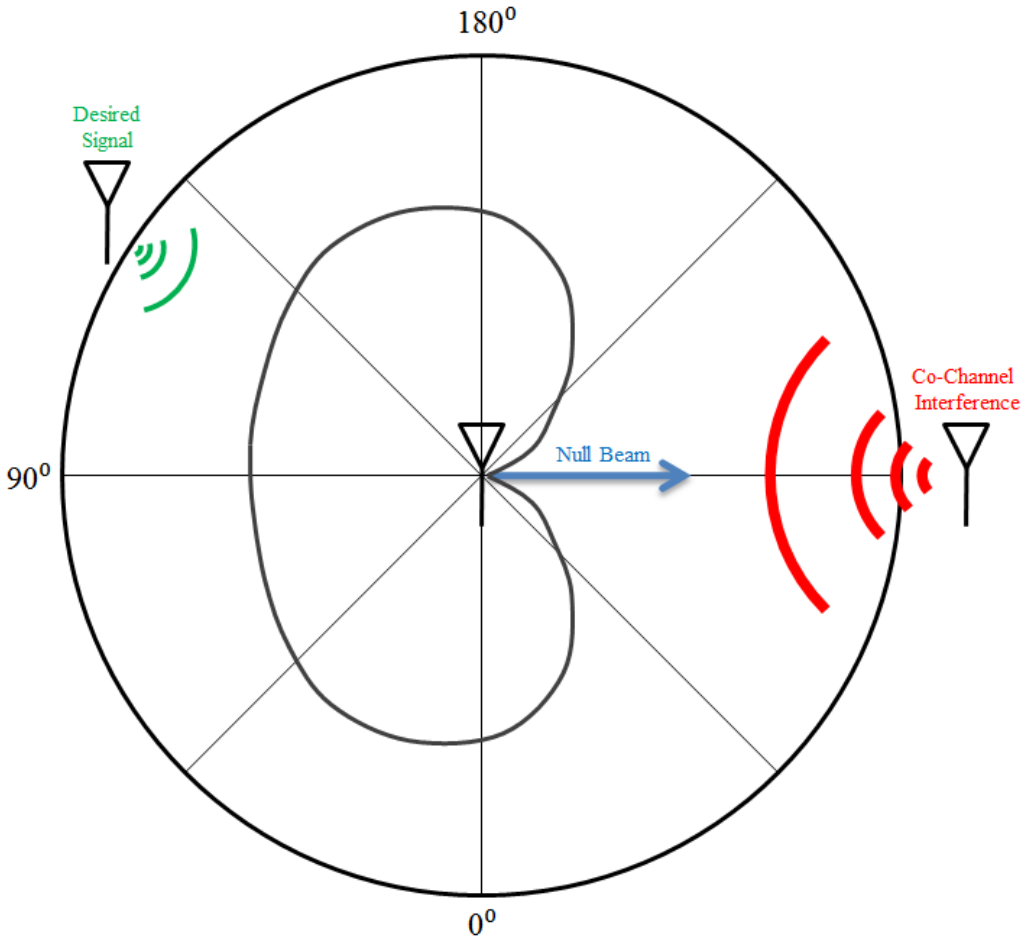

Fig. 1. Visual representation of antenna null-beam steering

For separate antennas, which are tightly packed onto a handset, there are significant challenges. In order to change the propagation direction of an antenna, you need a physically separated array of antennas with phase shifting elements. Directing the beam is extremely challenging within a mobile phone because the element-to-element separation required is difficult to attain [5]. In [5], they were able to reliably direct the main beam in 3 different angles, however for null-beam steering, high precision would be required. In addition, if a mobile designer were able to have sufficient array sizing, the transmit antenna would be extremely close to the receive array, comparable to the element-to-element spacing within the array itself. Although one could argue that the

direction of CCI is known in this case, the transmit antenna would fall well within the near-field of the beam-steering array; the design of which assumes far field propagation which is predictable. It is due to these factors that null beam steering within a handheld is infeasible to achieve. Furthermore, the cost of adding numerous antennas and phase shifters and increasing the complexity of the mechanical and electrical design of the device would outweigh any gains made by its successful operation. Transmit and receive scheduling would remain the preferred method of addressing CCI in this case.

2.2 Front-End Hardware Cancellation, Co-channel

The disadvantage faced by a handset subject to co-channel self-interference is that the proximity of the interferer prohibits spatial filtering to address it. There is an upside however: the offending signal is known and available on the device. It cannot be filtered spatially or electrically, however it can be cancelled through the polar modulation of a sample of the offending signal.

Self-CCI in radios isn't strictly new to the 4G LTE generation of mobile phones. In [6], the invention describes a circumstance of interference between a WiMAX and Wi-Fi transceiver on the same device. It is from this work that this research continued. The solution in [6] presents a Wi-Fi transceiver operating in the range of 2400–2485 MHz, and a WiMAX transceiver operating in the range of 2300–2690 MHz. Fig. 2, taken with permission from [6], shows a WiMAX signal to be received at 2.35GHz (4300), however it is coexisting with a very large Wi-Fi signal in the 2.4GHz band (4400), whose leakage significantly overlaps with the receive signal. The desired system response is indicated by (4600) where the cancellation circuitry produces a large null at the interferer.

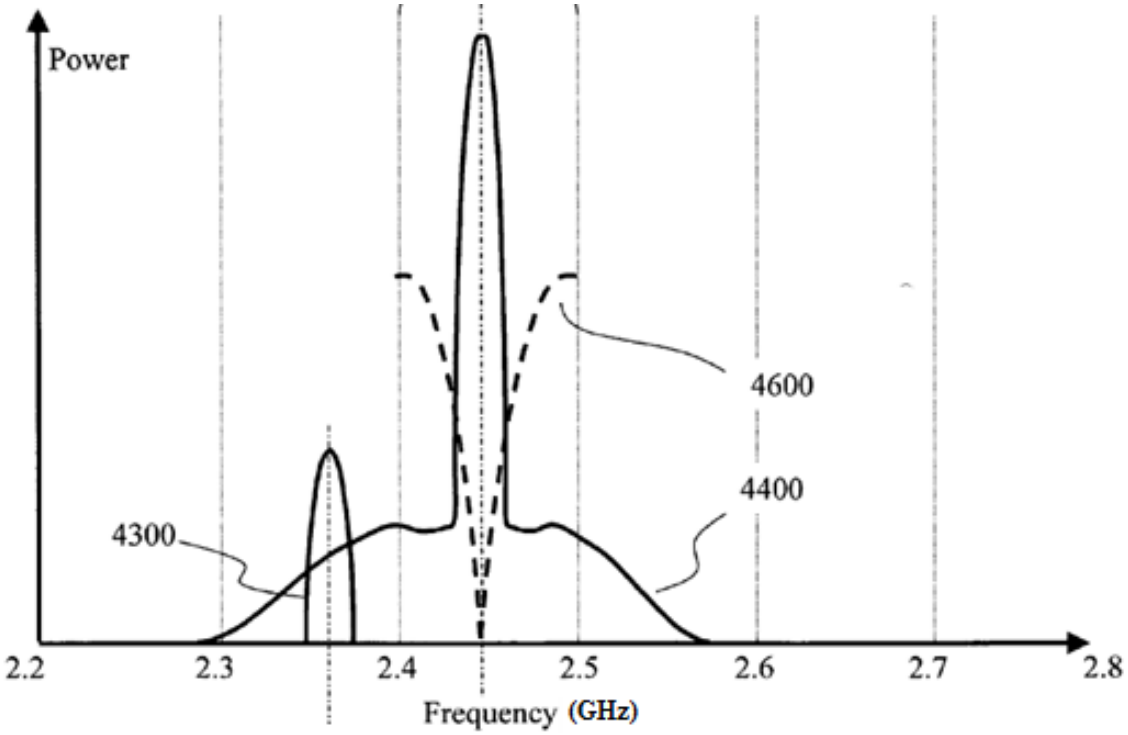

Fig. 2. Frequency spectrum showing coexistence of WiMAX (4300) and Wi-Fi (4400) on the same device, along with desired nullification of Wi-Fi leakage (4600)

Without cancellation, the SNR will be significantly reduced. The resulting spectrum post cancellation is shown in Figure 5 in [6]. The invention, found in Figure 8 in [6], presents a copy of the transmission signal to cancellation circuits composed of polar modulators, which are controlled via feedback from the output. The feedback path features a power detector (note 835) which is used to measure the power and control the polar modulators to minimize received power from 845. The broadened approach of multiple cancellation circuits is to provide either A) a wider bandwidth of cancellation, or B) the ability to expand to attack multiple sources of interference. In its simplest form, the invention extracts a copy of the Tx signal, polar modulates it, and recombines in the receiver before the first amplification stage, the LNA, in order to protect it from overload. Any signal attenuation occurring before the gain stage in a receiver shall degrade the noise figure of

the receiver by a factor of the loss. Therefore, the cancellation mechanism is ideal; however the architecture poses some challenges at a system level on noise figure and gain, for example.

2.3 Full Duplex RF Cancellation

The search for work relevant to CCI can be made broader by expanding to any situation where an interferer is on-board, or generated on the same device as the receiver, generating self-interference. There has been a lot of recent investigation into the feasibility of a full-duplex radio – a prime example of self-interference. Full duplex is the holy grail of spectrally efficient communications; it is transmit and receive on the same channel at the same time. This is not possible without extremely robust transmit cancellation within the receiver, and is one step above the problem of co-channel interference. With CCI, the interference is band adjacent with spectral leakage swamping the received signal. In full-duplex, the full power of the transmitter coexists with the received signal at the same frequency. The goal and methods are the same in both problems; however the cancellation requirements are far steeper for full duplex solutions. A CCI cancellation of 20dB will not be complete, but it will greatly reduce the complexity of Surface Acoustic Wave (SAW) or Bulk Acoustic Wave (BAW) filters at the front end. A completely robust full-duplex solution requires 110dB of linear cancellation to bring the main signal to the noise floor [7], and you cannot filter any remaining energy. Any full-duplex techniques providing cancellation at RF should lend themselves to self-CCI generating devices as well.

Adaptive RF cancellation for full-duplex radio is described and demonstrated at a basic level in [8]. The design features a polar (vector) modulator tapped from the transmitter output, seen in Figure 1 in [8]. While the authors lacked IC prototyping capabilities, they demonstrate that polar modulation of the interference signal at the PCB level will cancel out interference to a reasonable degree, up to 60dB with 20MHz bandwidth in their design.

In [7], the authors demonstrate the required cancellation schemes for a completely robust fully duplex Wi-Fi radio with 110dB of cancellation at the PCB level, similar to [8]. The solution assumes moderate circulator isolation (15dB), and provides a reported 60dB of RF front end cancellation and 50dB of digital cancellation at baseband, totaling 110dB. Focusing on the RF cancellation, they implement a multi-tap solution with varying delay. To quote the paper, they pass the signal through a circuit "which consists of parallel fixed lines of varying delays (essentially wires of different lengths)" before passing through attenuators to control the amplitude. They claim that this variable delay line addresses the problem that "precise programmable delays with resolution as precise as 10 picoseconds" are required but extremely hard to attain. The design in [9], which authors Bharadia and Katti from [7] also authored, had the best programmable delays they could find at the time of publication of 100-1000 picoseconds.

The delay mechanism in [7] is feasible and extremely effective at the PCB level but is infeasible for integration due to high area use to implement on an IC, and the wire coupling that would arise due to extremely close proximity. This concern is noted by the authors of [10] when comparing [7] to their proposed technology. The circuit in [10] follows the same basic methodology: polar modulate a copy of the Tx signal for

recombination in the receive chain, however they use a vector modulating downconverter in a zero-IF transceiver. In contrast to other RF cancellations, the cancellation operation occurs after the downconversion, as seen in Figure 19.2.1 in [10]. The authors' downconvert the RF signal and downconvert the copy signal separately in a vector modulated downconverter which can control the output phase and amplitude, and then combine to cancel the Tx leakage. The vector modulator covers a square constellation of 32x32 phase/amplitude points, allowing for a claimed 28.5dB self-interference cancellation. The authors combine this with a digital cancellation at baseband to improve their full-duplex performance to a peak 69.5dB. While this implementation is integrated, it is not compatible with the desired superheterodyne radio architecture. In this work, cancellation is to occur completely at RF.

Chapter 3: System Level Design and Specifications

This chapter will outline the system level design of the CCIC, the system specifications, and finally determine the circuit parameters required to meet the system specifications.

3.1 System Level Considerations and Architecture

A simplified multi-radio system is shown in Fig. 3. The module contains multiple radios and in this case, Radio A transmit frequency is band-adjacent to the Radio B receive signal and will leak into the receive path of Radio B due to their proximity in space. This is co-channel interference and typically prevents simultaneous transmit/receive with these two radios.

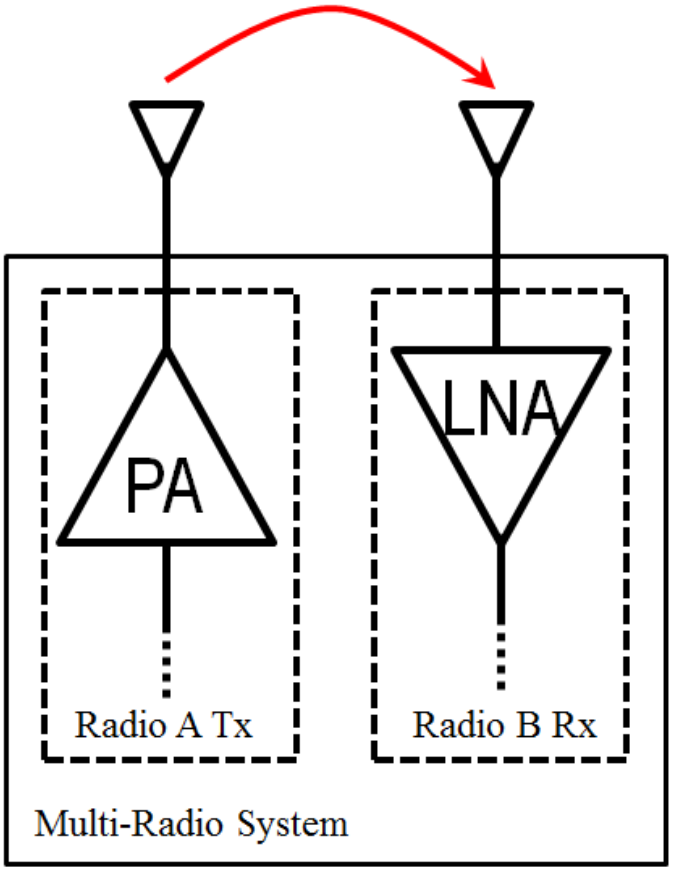

Fig. 3. Typical system architecture with co-channel interference

In order to cancel the interferer, a copy of the signal needs to be taken from the transmitter. The PA introduces many nonlinearities to the transmit signal, therefore the copy must be taken at the output of the PA to ensure all signal components found in the receiver are accurately replicated. The copy can be obtained by using a directional coupler to siphon a small portion of the transmit power from the output of the PA. Consequently, the PA design would need to factor in the coupler to compensate for the output power loss; a -10dB coupler would cause a forward attenuation of 0.9, or 0.46dB.

The copy needs to be subtracted at the input of the receiver to cancel the undesired signal. For cancellation to occur, the phase and amplitude of the signal must match the phase and amplitude of the signal received. There is no control over the interferer once it leaves the PA, and the propagation properties will be affected by objects in proximity to the telecommunication device. Therefore, the phase and amplitude must be adjustable on chip using a phase shifter and amplitude shifter.

The proposed design is a fully integrated feed-forward system that can be controlled on-chip in a fully integrated solution. A calibration period is required in order to determine the ideal phase and amplitude to nullify the offending signal. A relative signal strength indicator, or RSSI, can be used in combination with digital logic to algorithmically determine and set the ideal phase and amplitude setting. As an example, the RSSI could measure the signal strength at the output of the LNA, which would take advantage of the LNA's typical bandpass response to isolate the undesired signal. The undesired signal is in the adjacent band and therefore would be minimally affected by the LNA's frequency response. To algorithmically control the phase and amplitude shifting,

they will need to be digitally controlled. The full system diagram with RSSI and control logic is shown in Fig. 4.

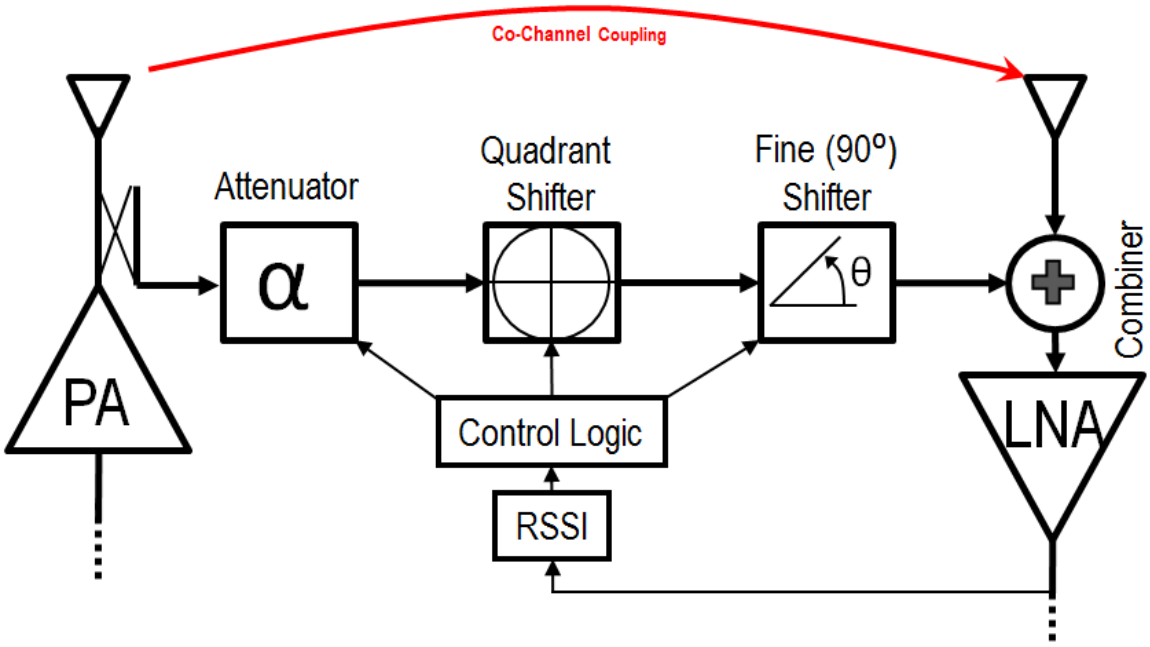

Fig. 4. Proposed system architecture including control logic for calibration

3.2 System Specifications

The basic specifications given at the beginning of this project are as follows:

- Greater than 20dB of co-channel interference cancellation
    - Passive signal manipulation in a feed-forward system
- Low area usage (therefore low cost)
- LNA for Band 40 LTE Specification – covering 2.3-2.4GHz
- Interferer is Wi-Fi at 2.4GHz
- Input power level to CCIC is +5dBm

The scope of this project will include the system level and hardware level design and fabrication of:

- 2.35GHz LNA
- 2.4GHz Passive Phase Shifter
    - 360^0 of phase shift
- Passive Attenuator
    - 20dB of attenuation range
- Signal combination circuit within receiver
- Control algorithm and logic
    - Demonstration: Can be done off-chip/board in order to abstract the logic design to code (no hardware logic design or required) RSSI = Spectrum Analyzer

The following is not being designed in this project:

- Power Amplifier in transmitter
- Directional Coupler to siphon PA power
- Other transmit or receiver circuits such as mixers or filters

The specifications for the receiver from antenna to the output of the LNA were given as follows:

- Gain = 14dB
- Noise Figure = 1.5dB
- Input Referred 3^{rd} order Intercept Point (IIP3) = +5dBm
- System impedance = 50Ω
- Minimize power consumption (no specific specification)

As this chip is intended as a proof of concept of the system, the current consumption of the LNA was not a large concern; as a result, there isn't an explicit specification on its value.

In order to determine the specifications for the phase shifter and attenuator, the phase and amplitude resolution, minimum CCIC path loss, and expected power levels need to be determined.

3.3 Phase and Amplitude Resolution

Two sinusoidal signals added together will produce a cancellation if they are properly matched in anti-phase. This can be expressed as the difference between a normalized cosine, cos(ωt), and a cosine with amplitude, phase, and delay errors, i.e. $a \cdot \cos(\omega t + b + xd)$; where $x = \omega - \omega_o$ or the distance from the center frequency, a is the amplitude relative to interferer, b is the phase error, and d is the delay error which will be discussed in Section 3.4. Using trigonometric identities, this can be simplified as:

$$Cancellation = 10\log(1 + a^2 - 2a\cos(b + xd)) \quad (1)$$

Amplitude and phase are essential to cancellation; both must be close to the original signal or the sine waves will not sum to zero. Amplitude and phase error must be considered together in order to obtain a desired cancellation. The amplitude could be matched perfectly but the cancellation will then be limited by the phase error. Both must be sufficiently low to obtain high cancellation. A contour plot in Fig. 5 illustrates attained cancellation versus the phase and amplitude errors with contours showing 15dB, 20dB, 25dB and 30dB cancellation. The 20dB region shown illustrates the outermost boundaries where the CCIC can operate within requirements. In order to obtain circuit specifications, it is important to understand that neither phase nor amplitude can have a

resolution that places it at the edge of the 20dB contour along the axis, because if one variable is at the boundary, an imperfect cancellation with regards to the other variable will cause the cancellation to fall outside of the 20dB region. Therefore, although the problem is circular, the design approach must be rectangular to guarantee compliance in all conditions. To achieve greater than 20dB of signal cancellation, the phase shifter and attenuator step specifications must form a rectangle that resides completely within a circle defined by Phase Error = $\pm 6^0$ and Relative Amplitude = ±10% or 0.85dB.

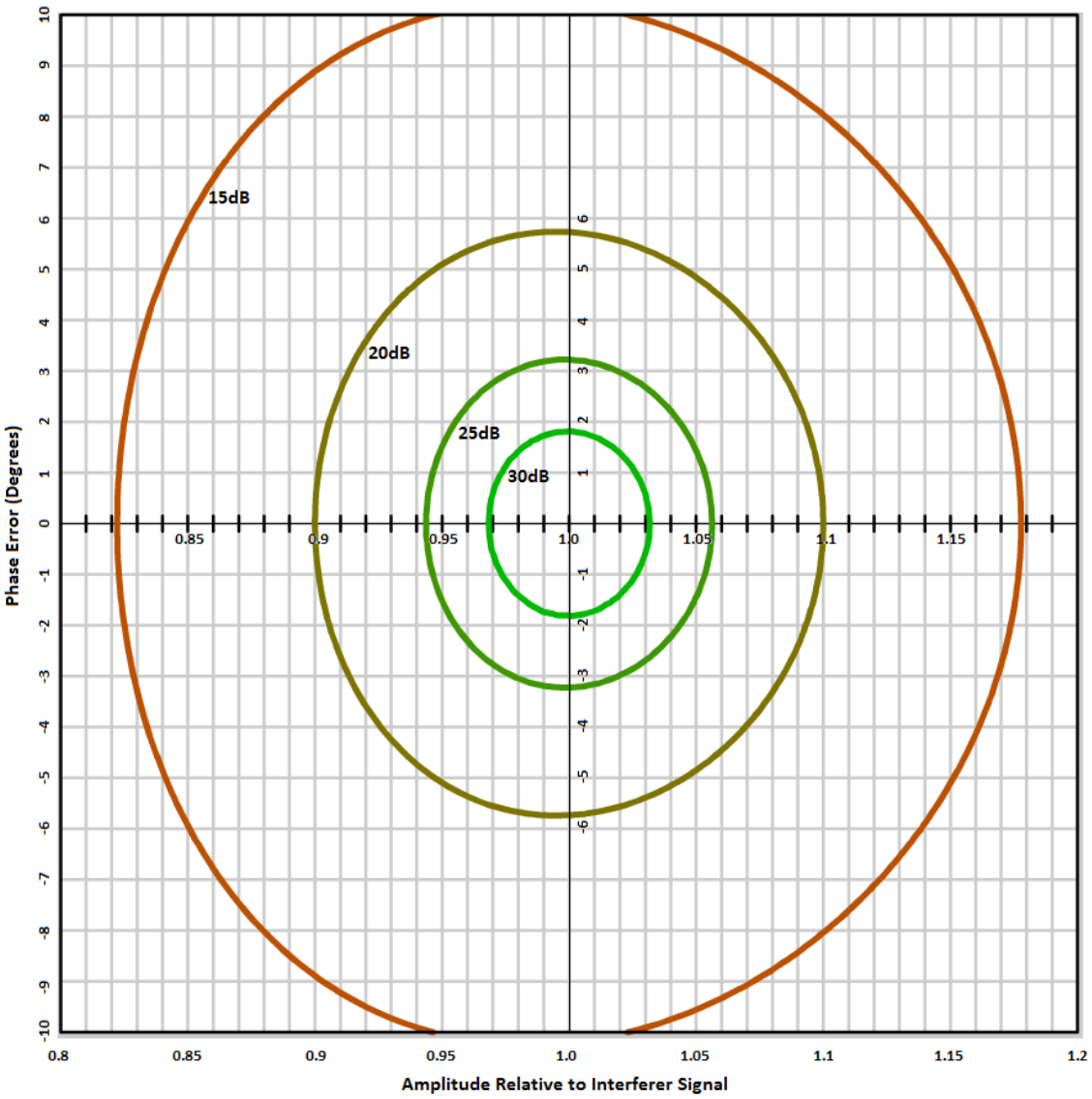

Fig. 5. Cancellation contours versus phase error and relative amplitude

.

For a given phase step and amplitude step, the worst case cancellation error occurs when the phase and amplitude are exactly between two steps. For amplitude, "halfway" means halfway logarithmically in a linear sense; 1dB is halfway between 0.5dB and 1.5dB proportionally. Using the previous values, a maximum error of 6^0 and 0.85dB translates to a phase step of 12^0 and amplitude step of 1.7dB. As mentioned, these values are not the required resolutions; they form the circle within which the circuit specifications rectangle must reside. A contour plot showing minimum (worst case) cancellation vs. phase and amplitude step is shown in Fig. 6.

To begin determining hardware performance requirements, basic circuit specifications can be established immediately. Regarding the phase shifter, the phase range is known as 360^0. The circuit is to be passive and digitally controlled, therefore the range and resolution will be related by the number of bits. The resolution and range are related by:

$$Resolution = \frac{Range}{2^N} \tag{2}$$

where N is the number of bits in the system. Using this equation, the resolution for a 4-bit system is:

$$Resolution(4b) = \frac{360^0}{2^4} = \frac{360^0}{16} = 22.5^0 \tag{3}$$

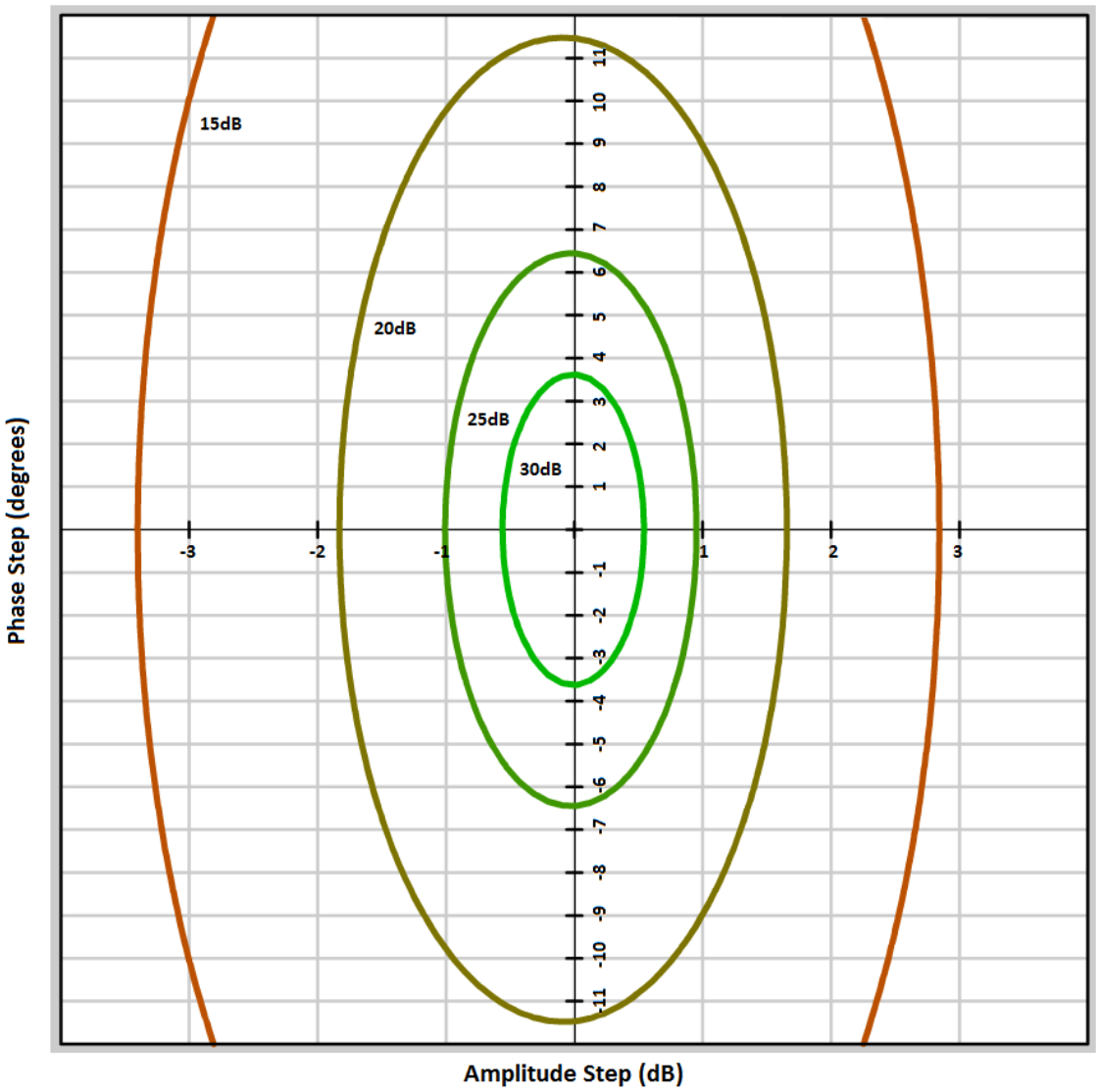

Fig. 6. Minimum cancellation contours vs. phase and amplitude steps

A 5-bit, 6-bit and 7-bit phase resolution is calculated in (4), (5), and (6) respectfully.

$$Resolution(5b) = \frac{360^0}{2^5} = \frac{360^0}{32} = 11.25^0 \tag{4}$$

$$Resolution(6b) = \frac{360^0}{2^6} = \frac{360^0}{64} = 5.625^0 \tag{5}$$

$$Resolution(7b) = \frac{360^0}{2^7} = \frac{360^0}{128} = 2.8125^0 \tag{6}$$

A 22.5^0 phase step isn't reflected on the contour map and is far too coarse for this application. Referring to Fig. 6, a 5-bit phase shifter, with 11.25^0 resolution, would exist at the edge of the 20dB contour. As discussed, this is not acceptable because variation in amplitude will push the cancellation outside of the 20dB region. The resulting requirements on the attenuator would be very stringent. Therefore, the lowest number of bits that would work with margin is 6 bits. 6 bits will have a 5.6^0 resolution, placing it inside of the 25dB cancellation region. 7 bits with 2.8^0 resolution begins inside the 30dB+ cancellation region and is not required for this design.

The specification given for the attenuation is that it has at least 20dB of range to accommodate changes in co-channel coupling as well as variations in transmit power. A similar approach as the phase shifter can be taken with this information to determine the number of bits and resolution that would satisfy the minimum cancellation specification. Assuming a 20dB attenuation range, a 4-bit, 5-bit, and 6-bit attenuator resolutions are found in (7), (8), and (9) respectfully.

$$Resolution(4b) = \frac{20dB}{2^4} = \frac{20}{16} = 1.25\ dB \tag{7}$$

$$Resolution(5b) = \frac{20dB}{2^5} = \frac{20}{32} = 0.625\ dB \tag{8}$$

$$Resolution(6b) = \frac{20dB}{2^6} = \frac{20}{64} = 0.3125\ dB \tag{9}$$

The 4-bit attenuator lies within the 20dB region, and the 5-bit and 6-bit lie within the 30dB+ cancellation region.

At this point, it was decided to aim for near 25dB cancellation. This provides some margin, and given that the coarsest acceptable phase resolution lies within the 25dB region, the only design factor to accomplish 25dB is the attenuation resolution. By

increasing by one bit, to 5 bits in total, the rectangle that defines the cancellation region mostly presides within the 25dB contour, which is shown in Fig. 7.

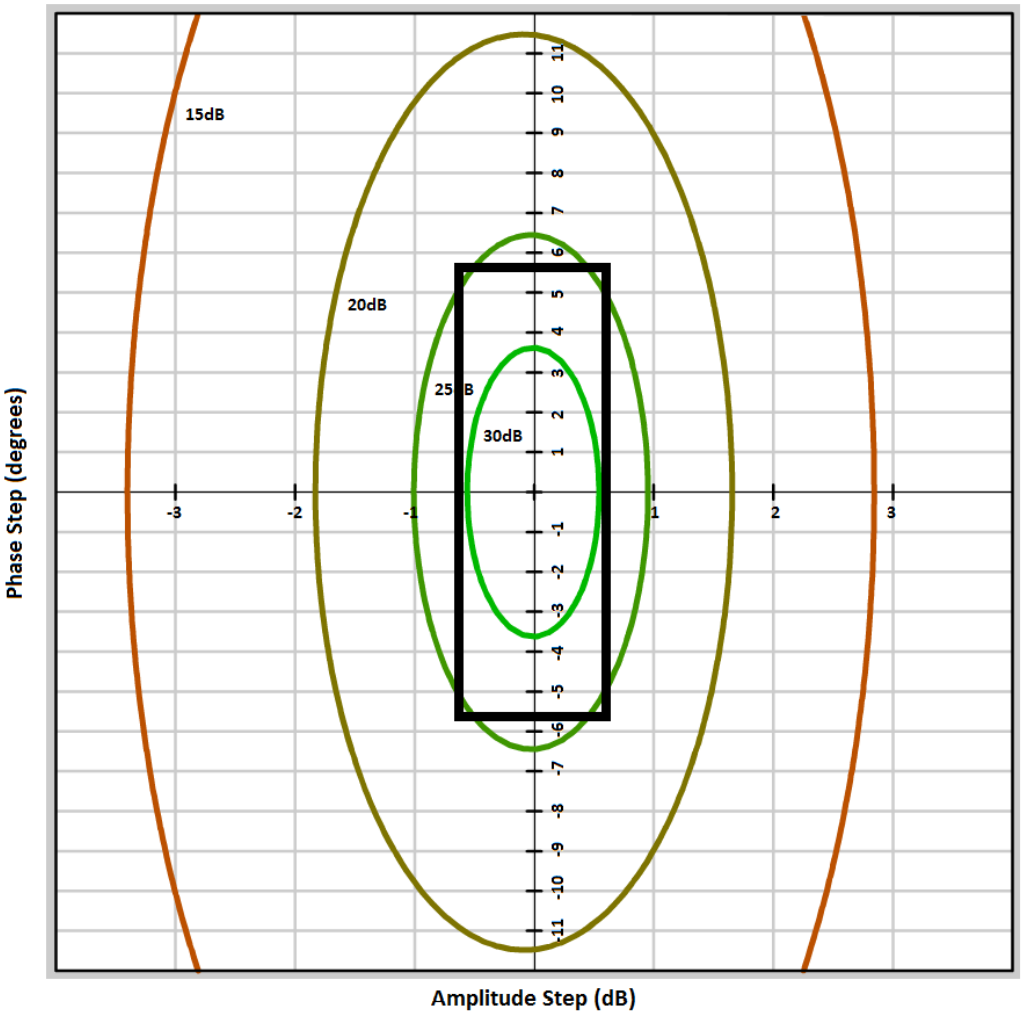

Fig. 7. Theoretical region of cancellation based on 5.6^0 and 0.625dB resolution

The phase and attenuation will be designed with margin on the range specification, to ensure that there is at minimum 360^0 and 20dB coverage. As a result, an attenuation resolution of 0.7dB and phase resolution of 6^0 is selected as a starting point for design at the schematic level. This will give a theoretical phase shift of 384^0 and an attenuation range of 22.4dB, or 24^0 and 2.4dB of margin respectfully. This will extend the corners of the circuit cancellation rectangle further from the 25dB region; however it

is still considerably within the target 20dB cancellation. Using (1), a phase step of 6^0 and attenuation step of 0.7dB, with 3^0 and 0.35dB maximum error respectfully, will lead to a minimum cancellation of 23.74dB. This will provide 3.74dB of margin over the specification.

The summarized phase shifter and attenuator performance parameters are shown in Table II along with the specification provided.

TABLE II: SPECIFICATIONS FOR THE PHASE SHIFTER AND ATTENUATOR

Parameter	**Phase Shifter**		**Attenuator**	
	Specification	*Design*	*Specification*	*Design*
Number of Bits	*	6	*	5
Range	360^0	384^0	20dB	22.4dB
Resolution	*	6^0	*	0.7dB

***Specification provided only on final cancellation coefficient**

3.4 Delay Matching

Up to this point the discussion has been regarding worst case peak cancellation at one frequency, however it is necessary to consider the bandwidth of cancellation which is determined primarily by the delay error. Delay is a less intuitive cancellation requirement; delay affects the phase differently for each frequency. As a result, the larger the delay error or difference in delay between the two paths, the harder it will be to cancel a broad band of frequencies. It will not affect cancellation at the desired frequency but must be considered in order to have meaningful cancellation over the channel of interest. It can be seen in (1) that *x*, the frequency difference, mathematically carries a larger impact when the delay error is larger. As the cosine term approaches zero with phase and delay errors approaching zero, it disappears from the equation, leaving only the

amplitude. If the delay error is large, the cosine term will diverge from zero quickly as the frequency difference increases, resulting in a lower bandwidth of cancellation.

The 20dB bandwidth of cancellation is logarithmically related to the delay error. Wi-Fi 802.11b/g/n has a maximum bandwidth of 40MHz [11], and as shown in TABLE I, the relevant LTE bands have a maximum bandwidth of 20MHz, therefore the system ideally would need to have 40MHz bandwidth or greater with these standards. An illustration of 20dB cancellation bandwidth versus delay error is found in Fig. 8.

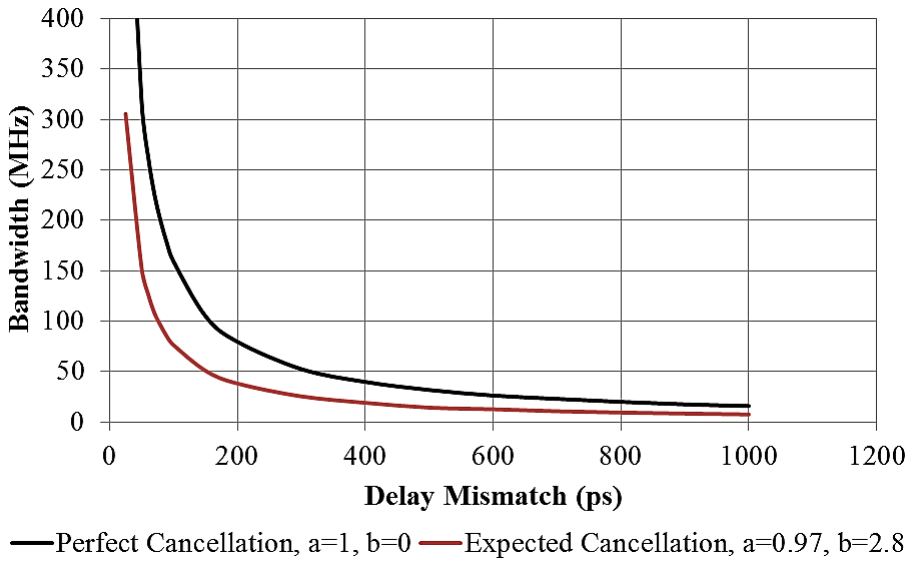

Fig. 8. 20dB cancellation bandwidth versus delay mismatch

In this instance, in order to have a 20dB cancellation bandwidth of 40MHz for the worst case bandwidth, an ideal system (perfect cancellation) would require a maximum of 400ps of delay error. A more realistic system with 2.8^{0} of phase error and 3% amplitude error would require less than 200ps of delay error to cancel over 40MHz. The difference in requirement is due to the depth of cancellation. With perfect cancellation there is more margin over 20dB, resulting in a larger 20dB cancellation bandwidth.

3.5 Power Levels and Maximum Loss

The minimum loss of the passive section is determined by the known power levels and coupling factors in the system. The following specification regarding Tx-Rx leakage is provided for the design: The maximum and minimum expected Tx to Rx leakage is −25dB to −35dB respectfully.

In order to cancel the signal, the maximum power level seen at the receiver must be equal to the power level of the copy in the minimum loss state. Therefore the total loss in the CCIC path from the PA must be equal to 25dB. If 20dB of total coupling loss is assumed from the couplers, then the minimum loss of the phase shifter and attenuator combined is 5dB. The assumed input power level for the CCIC is given as +5dBm.

Chapter 4: Circuit Level Design

This chapter will outline the design of the phase shifter, attenuator, low noise amplifier and the LNA combiner hybrid circuit at the transistor level. Section 4.1 will outline the fine phase shifter and ambidextrous quadrant selector design, Section 4.2 will describe the design of the 5-bit attenuator, and Section 4.3 will describe the LNA and combiner circuitry. Four provisional patent applications have come about from these designs.

4.1 Phase Shifter

Phase shifting is an important operation in many RF applications. Phase Shifters are commonly used in signal cancellers and equalizers [12]. Phase shifters are also used in beam steering, where a phased antenna array directs the antenna energy in a desired direction, which is commonly used in radar and non-line-of-sight (NLOS) operations [13]. In dynamic gain equalizers, phase shifters are used to fit the attenuation profile of the equalizer to a desired one to compensate for non-flat gain responses across a communication band [12].

This chapter outlines the design of a highly compact phase shifter comprised of a digitally tuned transmission line and an ambidextrous quadrant selector. The basic theory surrounding lumped element transmission lines will be highlighted, and the architectures for a novel quadrant selector and a fine tuning phase shifter are explained. The fine shifter, ambidextrous quadrant selector, and cross biased symmetrical digital capacitor have all been filed as provision patents through Skyworks to the United States Patent and Trademark Office. The application information is considered trade secret until non-provisional filing in June 2016.

4.1.1 Basic Theory

A lumped element quarter wave transmission line, shown in Fig. 9, has a characteristic impedance, Z_0, given by

$$Z_0 = \sqrt{\frac{L}{C}}, \tag{10}$$

and a corner frequency, ω_o, given by

$$\omega_O = \frac{1}{\sqrt{LC}}. \tag{11}$$

A change in inductance or capacitance will change the corner frequency of the system, and thus the phase of the signal at the output will change as well. Inductance is not easily altered; however, capacitance is variable with an appropriate device, such as a MOS varactor. Therefore, in a lumped element transmission line, utilizing a variable capacitance will alter the phase of the signal at the output.

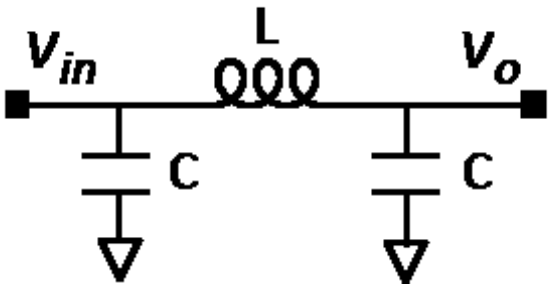

Fig. 9. A lumped element transmission line

A lumped element circuit from Fig. 9 will have a low pass response up to the corner frequency response indicated in (11). Prior to this frequency the gain response is fairly flat, but phase will be changing. As a result, the phase can be altered while the gain of the system remains relatively flat by changing the corner frequency of the system within the pass band region close to the corner frequency.

Using a fine tuning system by altering the corner frequency of a circuit similar to Fig. 9 will enable fine tuning. In order to cover 360°, a coarse tuning will be needed as well. A logical choice for coarse phase shifting is 90^0. With a fixed L, C and Z_0, the electrical length of a lumped transmission line will be constant at a given frequency. Using several fixed quarter wave transmission lines, different quadrants (0°, 90°, 180°, 270°) can be selected using switches to obtain the coarse phase shift. This would yield 360° total range when paired together with a variable capacitor loaded transmission line.

4.1.2 Ambidextrous Quadrant Shifter

A simple way to design a quadrant shifter is to construct it using fixed quarter wave transmission lines can be switched in or out to select the quadrant desired. To select the four quadrants, one would need three quarter wave sections selectable by switches. With three sections, there would be three inductors which are the main area consumer in this circuit.

The architecture shown in Fig. 10 employs inductor reuse in combination with switches to accomplish the same goal with two inductors instead of three. It does so by electrically reconfiguring the circuit's inductors between series and parallel connections to make use of left handed lumped transmission lines, which provide the opposite phase shift of the right handed version shown in Fig. 9. The architecture selects between bypass, single right handed quarter wave, double right handed quarter wave, and single *left handed* quarter wave states, which provides 0°, –90°, –180°, and +90° of phase shift respectively. The architecture is shown in Fig. 10, followed by a description of each quadrant state.

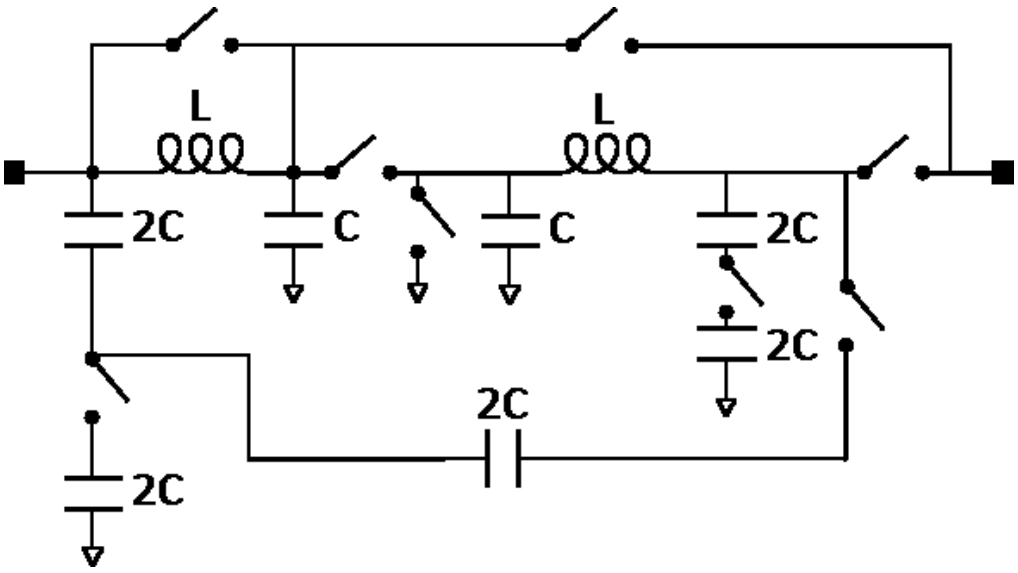

Fig. 10. An ambidextrous quadrant selector. L=3.32nH, C=1.32pF

4.1.2.1 Bypass Quadrant State, 0° Phase Shift

In the bypass state, both bypass switches are on, and all others are opened. Note that one shunt capacitor C to ground could also be removed with another switch, but in practice this proved to be unnecessary.

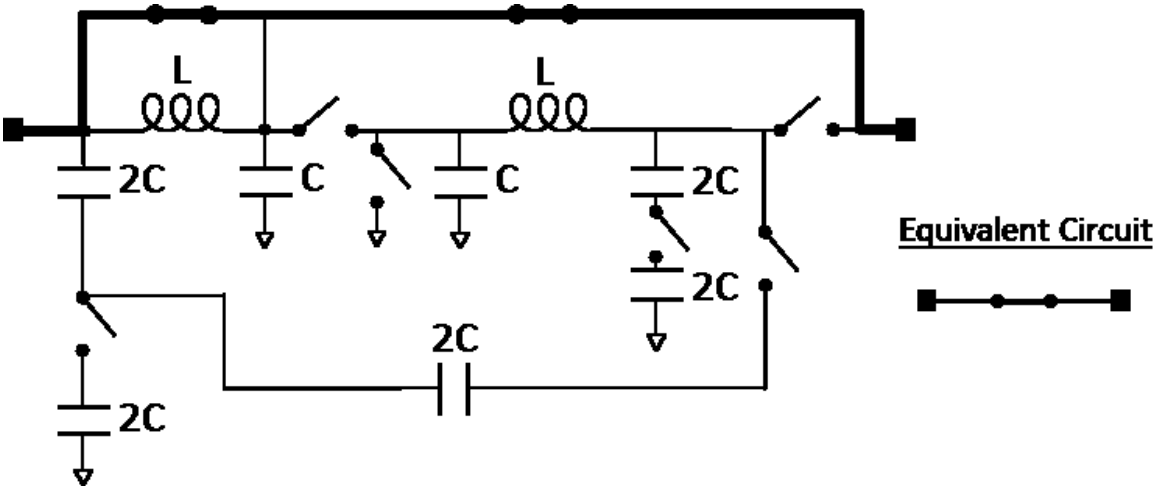

Fig. 11. Bypass state of quadrant selector and equivalent circuit

4.1.2.2 Single Quarter Wave Transmission Line Quadrant State,–90°

A single right handed transmission line is formed by creating a shunt C at the input, and activating the bypass switch at the output.

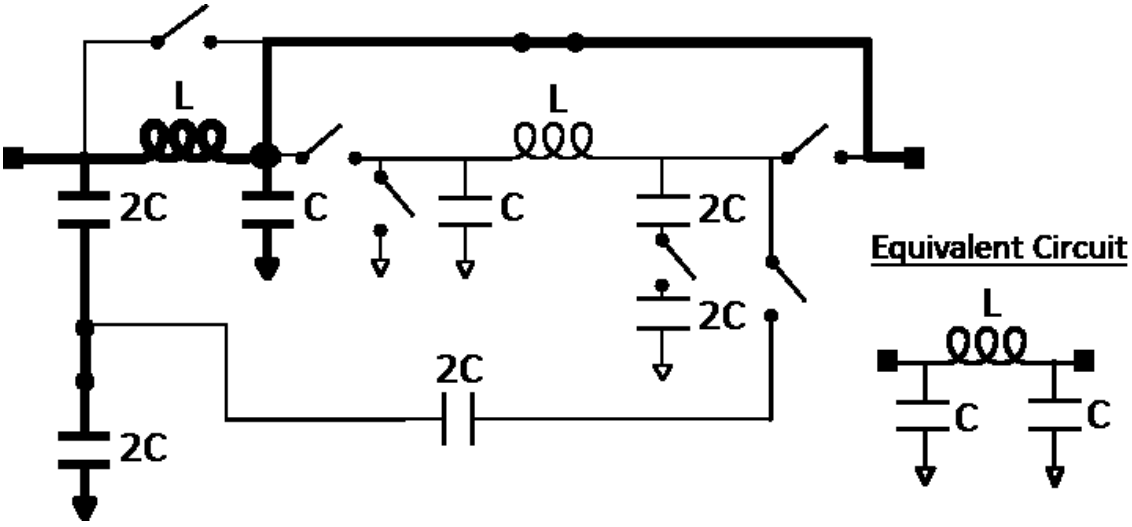

Fig. 12. –90° state of quadrant selector and equivalent circuit

4.1.2.3 Double Quarter Wave Transmission Line, –180°

Both bypass switches are opened and two series quarter wave transmission lines are formed to produce a 180^0 phase shift.

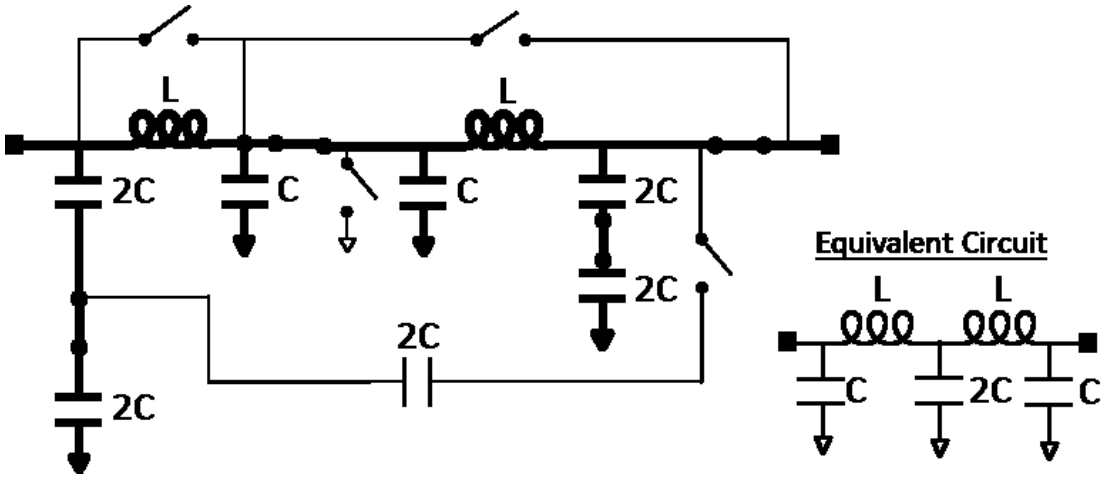

Fig. 13. –180° state of quadrant selector and equivalent circuit

4.1.2.4 Left-Handed Quarter Wave Transmission Line, +90°

Both inductors are shunted to ground from the input and output using a switch to ground in the middle of the circuit. A series capacitance C is created using the series combination of the capacitance 2C at the input and 2C connecting to the output through a closed switch. The previously shunted capacitance 2C to ground is disconnected by opening the shunt switch at the input. This creates a left handed transmission line with two series capacitors of 2C, creating C, and two shunt inductors to ground. This is shown in Fig. 14.

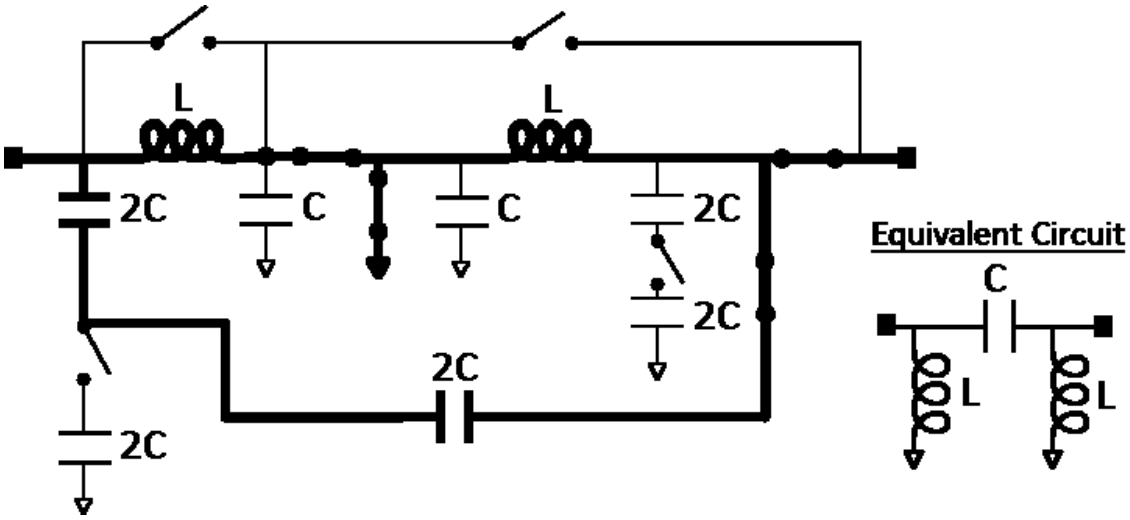

Fig. 14. +90° state of quadrant selector and equivalent circuit

In addition to a significant area reduction, this design will also provide a more consistent loss between states and a lower maximum loss than the simple method of three quarter wave transmission lines. This architecture would have the most loss in the double transmission line state, rather than triple in the other method.

4.1.3 Fine Phase Shifter

The fine tuning phase shifter is comprised of two series lumped element transmission lines from Fig. 9, where the capacitors are replaced with variable capacitors to enable tuning. This is shown in Fig. 15.

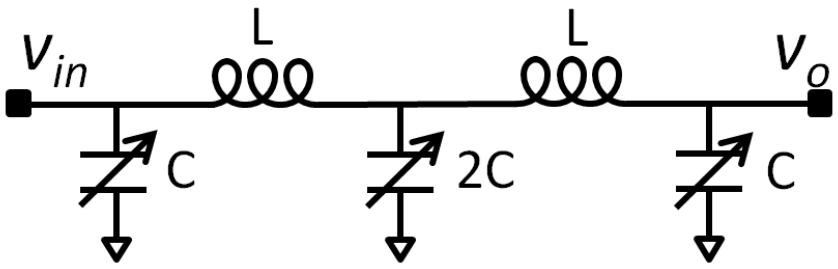

Fig. 15. Fine Shifter architecture composed of dual tuned transmission lines

The architecture makes use of high-ratio variable capacitors described in the next section in order to achieve 90° of total phase shift while maintaining a 50Ω match with only two inductors. The capacitors are 4-bit, enabling approximately 6° resolution for 90° of total phase shift.

The theoretical phase shift vs. capacitance can be derived from Fig. 15 using Kirchoff's Voltage Law. Assuming a 50Ω voltage source at V_{in} and 50Ω load at V_0, the transfer function V_{out}/V_{source} can be expressed in terms of impedances in (12). When substituting $Z_C = (sC)^{-1}$ and $Z_L = sL$ into (12), the Laplace transfer function in (13) is obtained. Finally, substituting $s = j\omega$ and factoring into Cartesian form in the denominator, (14) is obtained.

Using (10) and (11), and assuming a 50Ω transmission line at 2.4GHz, will yield L = 3.32nH and C = 1.32pF for a fixed quarter wave transmission line. Using this inductance value at 2.4GHz, the phase shift is found by solving (14) for the angle of

V_{OUT}/V_{IN} at various capacitances. This is illustrated in Fig. 16. Note that the angle values have been artificially constrained to ±180 degrees; the circuit does not advance the phase.

The resulting phase shift is quite linear with respect to capacitance over a large range, which will allow for a binary weighted digital capacitor to control the phase shift in a linear fashion.

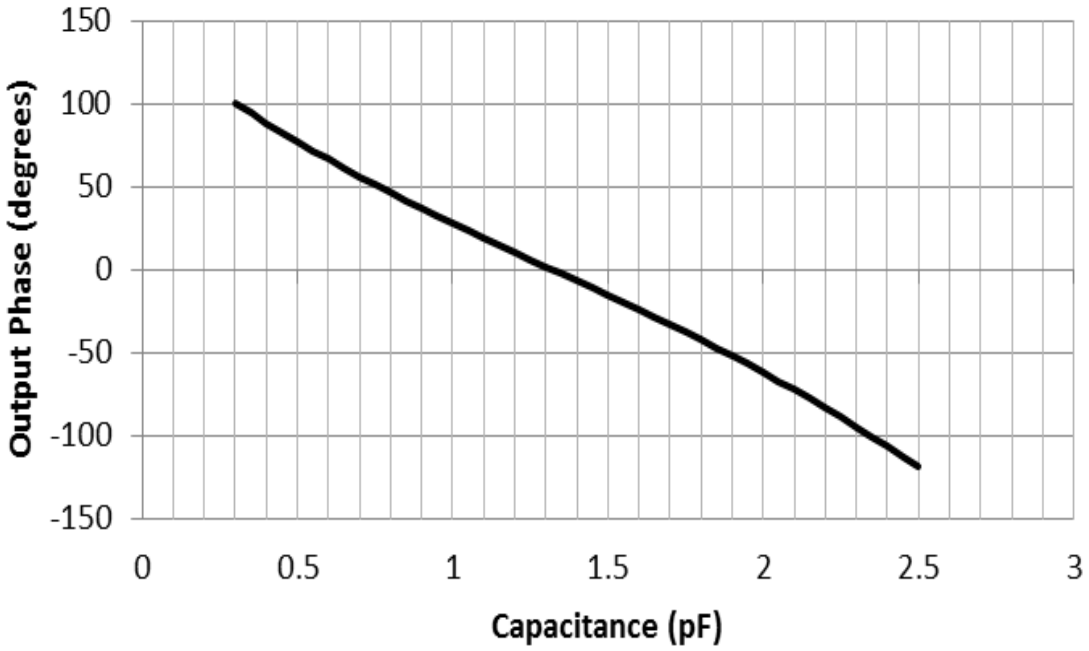

Fig. 16. Theoretical phase shift versus capacitance

As an example, using ideal devices in Fig. 16, 90° of phase occurs between 0.5pF and 1.5pF, for a C_{MAX}:C_{MIN} of 3:1, similar to MOS varactors [14]. For a 360° application

$$\frac{V_{out}}{V_{in}} = \left(\frac{Z_C \| 50}{Z_L + Z_C \| 50}\right)\left(\frac{\frac{Z_C}{2} \| (Z_L + (Z_C \| 50))}{Z_L + \left(\frac{Z_C}{2} \| (Z_L + (Z_C \| 50))\right)}\right)\left(\frac{Z_C \| \left(Z_L + \left(\frac{Z_C}{2} \| (Z_L + (Z_C \| 50))\right)\right)}{50 + Z_C \| \left(Z_L + \left(\frac{Z_C}{2} \| (Z_L + (Z_C \| 50))\right)\right)}\right) \tag{12}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{25}{2500C^3L^2s^5 + 100C^2L^2s^4 + (7500C^2L + CL^2)s^3 + 200CLs^2 + 5000Cs + Ls + 50} \tag{13}$$

$$\frac{V_{out}}{V_{in}} = \frac{25}{100C^2L^2\omega^4 - 200CL\omega^2 + 50 + j(2500C^3L^2\omega^5 - (7500C^2L + CL^2)\omega^3 + (5000C + L)\omega)} \tag{14}$$

paired with a quadrant selector, some margin would be needed to ensure no gaps occur from using real components and due to process variation, so a target starting design of at least 100 degrees is selected. In addition, on chip devices are far from ideal, therefore a variable capacitance with a ratio larger than 3:1 will be needed to reach 90° with two transmission line segments.

The input match is extremely important for RF applications. Using Fig. 15, Z_{IN}, which is equal to Z_{OUT}, can be found as:

$$Z_{IN} = Z_C \parallel \left(Z_L + \left(\frac{Z_C}{2} \parallel \left(Z_L + (Z_C \parallel 50) \right) \right) \right) \tag{15}$$

When (15) is simplified into Cartesian form and solved for magnitude, the input impedance for the 2.4GHz phase shifter is shown in Fig. 17.

For RF applications this design is advantageous due to a consistent 50Ω match over a large range of capacitance values.

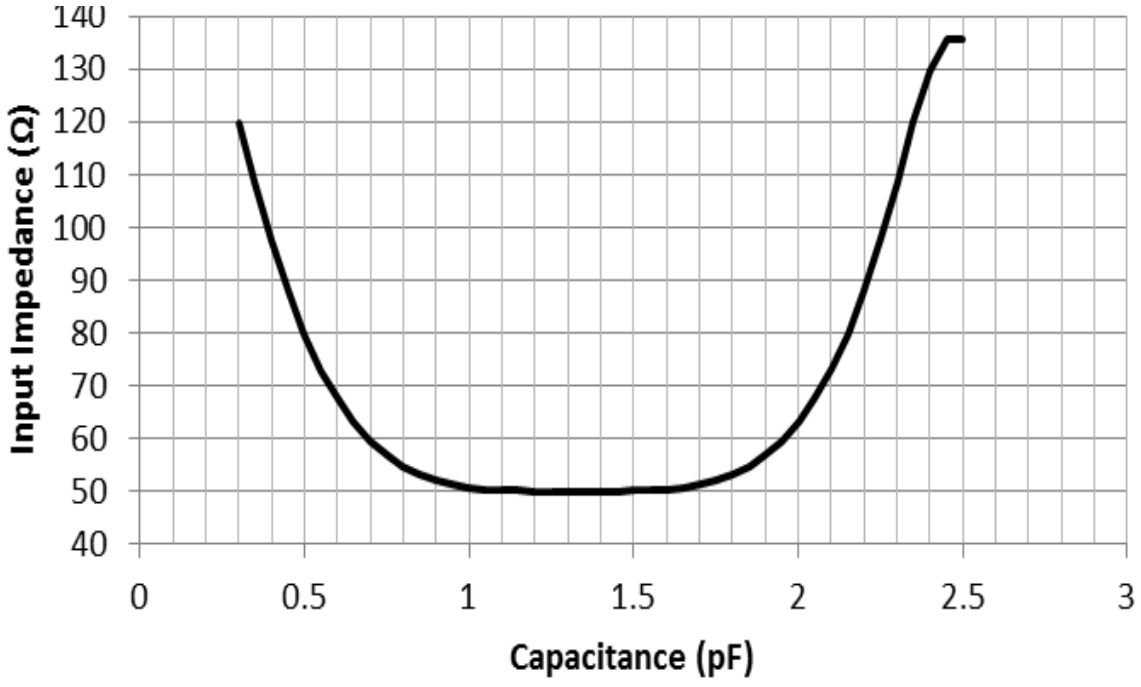

Fig. 17. The input impedance of the fine shifter versus capacitance

4.1.4 High Ratio Switched Variable Capacitors

This design aimed to have a very low area use. Traditional MOS varactors typically have a C_{MAX}:C_{MIN} near 3:1 [14]. By using real components with MOS varactors instead of ideal components as previously explored, the capacitance ratio would be insufficient to achieve greater than 90° of phase shift with two transmission line segments. Such a design would therefore require three series transmission lines to reach 90° of phase shift. However, if there were a variable capacitance with a higher ratio, a larger phase shift would be attainable and using two sections would become feasible. This would reduce the area considerably by being able to use two sections instead of three as compared to using MOS varactors.

A switchable capacitance is shown in Fig. 18. By using switches which are DC decoupled with fixed capacitors in parallel, capacitance can be added or removed digitally. Cross biasing the switches as seen in in grey in Fig. 18, where the channel and gate are biased to opposite potentials using an inverter [15], has three distinct benefits.

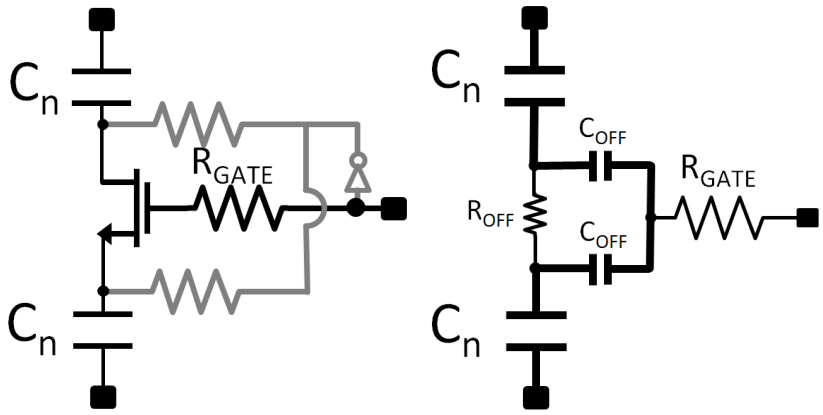

Fig. 18. A cross-biased switch, left, where gate and channel are inversely biased via an inverter, and equivalent circuit when gate is low (off), right. R_{GATE}=10kΩ

The first benefit is that the switch will not turn on or turn off easily due to a high powered RF signal. The second advantage is that by splitting the desired capacitance into two series capacitors, they also act to block DC. This means that traditionally large (RF short) DC blocking capacitors are not required, which will reduce area consumption. The third benefit to the design, specifically for a differential application, is that the capacitance will be symmetrical because a switch's source and drain are symmetrical, and the isolating capacitors can be the same value if desired. In this application, although not differential, requires the capacitor to ground in order to properly bias the channel as shown in Fig. 18. If cross biasing were not pursued, the circuit could be a set of capacitors with switches to ground as is done in [16], where this topology is used to improve VCO tuning compared to MOS varactors.

The architecture of a 4-bit variable capacitor is shown in Fig. 19.

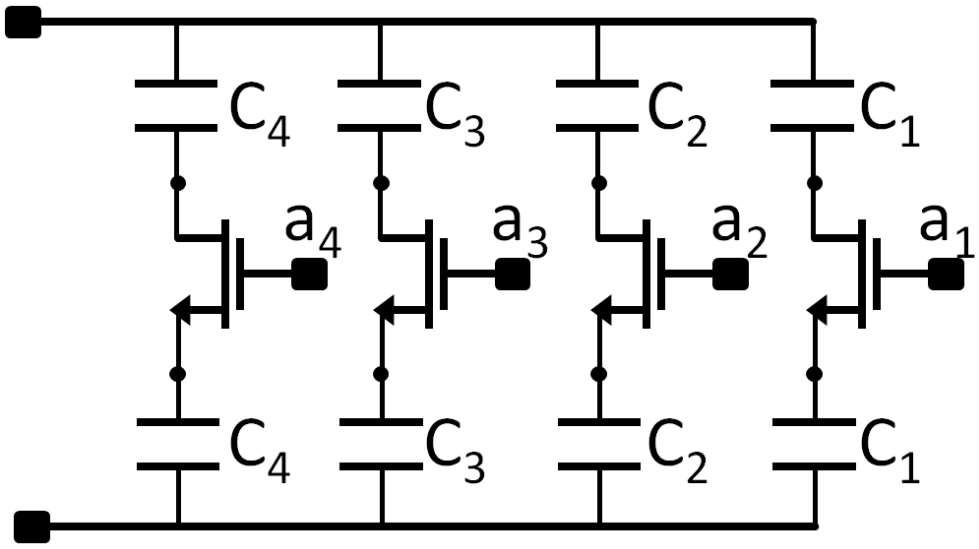

Fig. 19. A 4-bit symmetric digitally variable capacitor. C_1=200fF, C_2=350fF, C_3=730fF, C_4=1.35pF. L=120nm, $W_{1,2}$=100µm, $W_{3,4}$=300µm

In Fig. 19, a change in capacitance, ΔC_n, is toggled using the control signal a_n at the gate of a respective switch. The desired capacitance step is the difference between

two C_n in series with the R_{ON} of the switch, and two C_n and two C_{OFF} in series as seen in Fig. 18. The latter assumes a large R_{GATE} resistor and a large R_{OFF} of the switch. C_{OFF} is the capacitance between source/drain and gate when the switch is off as shown in Fig. 18. The difference ΔC_n can be expressed as:

$$\Delta C_n = \frac{C_n}{2} - \frac{C_n C_{OFF}}{2(C_n + C_{OFF})} \tag{16}$$

C_n can be chosen to provide the desired capacitance steps, and the number of bits is fully expandable. This design would have a C_{MAX}:C_{MIN} dependent of the selected C_n and only limited at the low end by C_{OFF}. Therefore, a large highly-linear capacitance ratio can be achieved using this architecture.

4.1.5 Complete Phase Shifter

The complete phase shifter is comprised of the Fine Shifter with high-ratio variable capacitors in series with the Ambidextrous Quadrant Selector. The design is 6-bit for a total of 64 phases across 360°. The circuit is entirely passive and only draws current when changing states. The full circuit is shown in Fig. 20

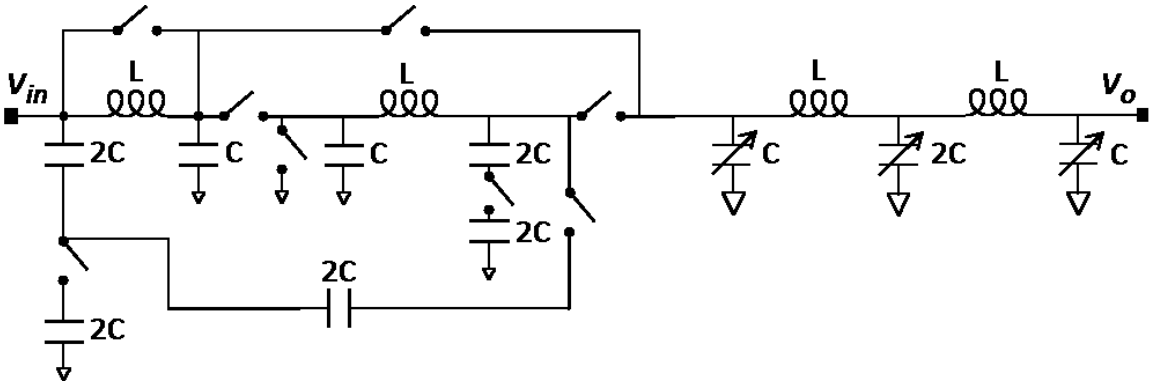

Fig. 20. Full 6-bit phase shifter architecture

4.2 Attenuator

4.2.1 Attenuator Theory

Attenuators are used in RF and Analog systems to adjust signal levels, control impedance mismatch, and to isolate circuit stages [17]. Digital attenuators use a control word to dictate the level of attenuation achieved. Within the CCIC, the attenuator is used to control the signal amplitude in order to match the interferer signal strength to that of the copy signal. In combination with an inverted phase of the signal, correct signal strength will lead to cancellation of the undesired signal. The attenuator, like the phase shifter, is to be passive, consuming energy only when switching states.

Passive attenuators have a core which commonly uses one of three structures or "pads", the *pi*-pad, *T*-pad, or *bridged-T* attenuator, shown in Fig. 21 and Fig. 22 respectfully. The pi-pad and T-pad circuits can be used to match unequal impedances; however the bridged-T, given the bridged resistance, cannot be used to match unequal impedances [18]. For this design, the pi-pad was chosen due to its simplicity; it also utilized larger series resistors at low attenuation compared to the T-pad core which would make it easier to accurately produce in layout.

The CCIC exists within a 50Ω system, and for the sake of simplicity, 50Ω is maintained throughout the system unless it is otherwise required, such as within the LNA combiner. Therefore, the attenuator design only needs to consider one system impedance, i.e. $Z_{IN} = Z_{OUT} = Z$.

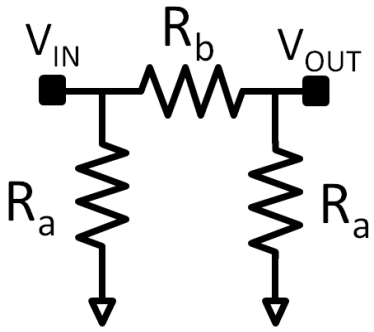

Fig. 21. A pi-pad attenuator core

For all circuit configurations, a K-factor representing the attenuation is equal to:

$$K = 10^{\frac{Attenuation(dB)}{20}} \tag{17}$$

For *pi*-pad circuits, the shunt resistor R_a can be found as:

$$R_a = \frac{Z(K+1)}{K-1} \tag{18}$$

The series resistor R_b can be found as:

$$R_b = Z\left(\frac{K^2-1}{2K}\right) \tag{19}$$

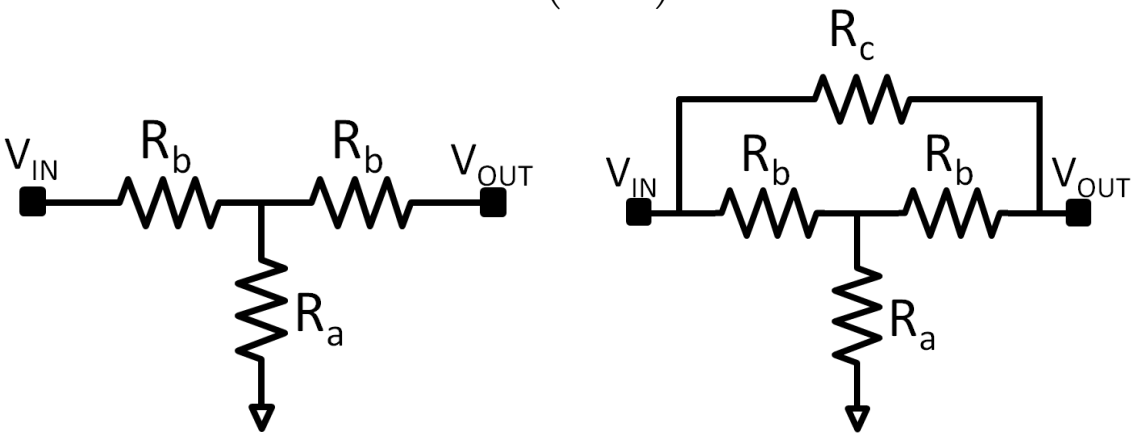

Fig. 22. A T-pad attenuator core, left, and Bridged-T attenuator core, right.

4.2.2 Attenuator Architecture

In order to select the desired attenuation with equal attenuation steps throughout the entire range, binary weighted sections will be needed. In this case, binary weighting occurs logarithmically, e.g. 0.7dB, 1.4dB, 2.8dB etc. The block diagram of the attenuator is shown in Fig. 23.

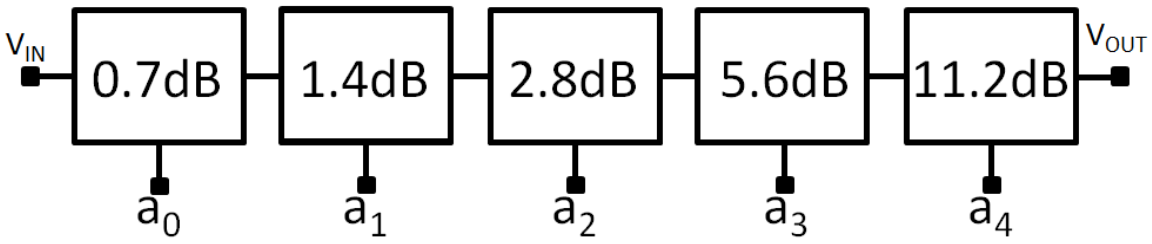

Fig. 23. Basic attenuator block diagram

When the control bit a_x is low, the attenuator core in the respective stage is bypassed. When a_x is high, the core is active and the attenuation increases by $0.7(2^x)$ dB. The order of the stages can be altered to suit different design needs such as linearity or input/output impedance.

The order presented in Fig. 23 was chosen for the following reasons. When the bypass switch is closed, the core will create a voltage difference across the switch, and the voltage difference will be larger for higher attenuation. The 11.2dB stage will have the greatest voltage across its bypass switch, which could cause it to unintentionally exit the cutoff state and turn on partially or fully, introducing distortion and changing the attenuation. Therefore, for linearity and attenuation level concerns, the highest attenuation is placed last to minimize the signal power that is applied to it. The low attenuation core will have the lowest voltage difference across the switch and, for equal switch sizing, will have higher linearity due to lower peak V_{DS}.

Each binary stage will need to be bypassed if the stage is not selected by the attenuation control word. As switches have non-zero attenuation themselves, the attenuator core needs to be designed so that the *difference* between the bypass attenuation and thru attenuation is equal to the desired step size. For example, if the bypass state has an insertion loss of 0.3dB, then a 0.7dB stage will require a core whose attenuation is 1dB. This will yield an attenuation step of 0.7dB as desired.

To properly bypass the attenuation core, the shunt components need to be opened to prevent current from continuing to flow to ground. Switches in series with these components are shown in Fig. 24. The example shunt switches are driven by control bit a_0, and the bypass switch is controlled inversely.

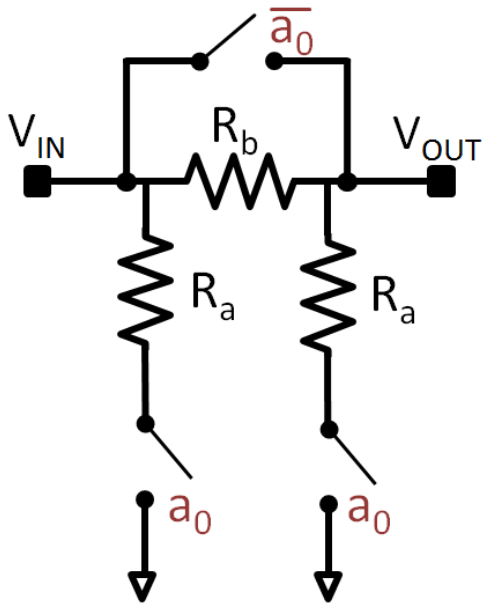

Fig. 24. Attenuator core example with switches to disconnect shunt components

By placing the switches in series with the shunt components instead of in series with the core, it will allow for a lower minimum attenuation as there are fewer series components. Additionally, the resistance of the shunt components can be compensated to adjust for the R_{ON} of the switch. When the shunt switches are off and the bypass switch is

on, the net circuit is approximately R_{ON} of the bypass switch in parallel with R_b in the case of a pi-pad circuit. When the shunt resistor switches are on and the bypass switch is off, the effective circuit is the attenuator core, adjusted for R_{ON}, whose shunt resistors are in series with R_{ON}, yielding $R_{SHUNT} = R_a' + R_{ON} = R_a$, the original required resistance.

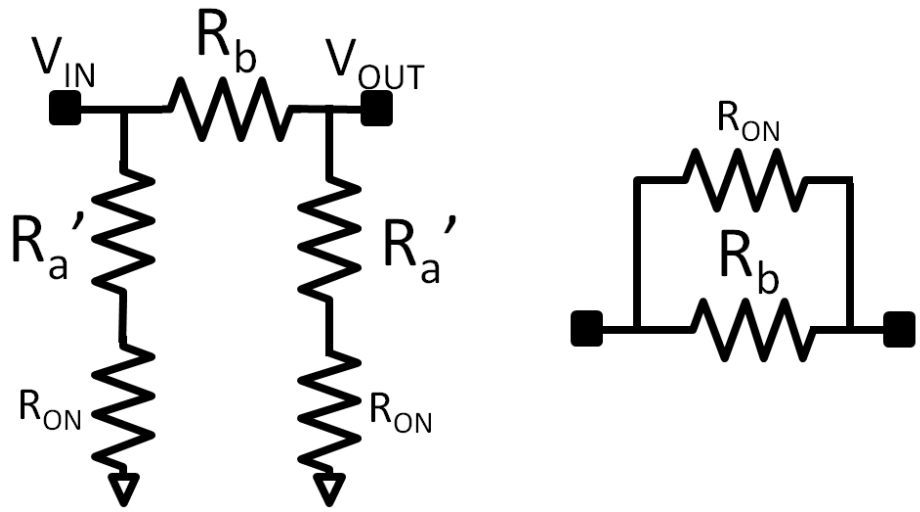

Fig. 25. Active (left) and bypass (right) effective circuits for attenuator stage states

In the bypass state, R_{ON} will often dominate and the bypass loss will be the insertion loss of the switch. In low-attenuation pi-pads where R_b is small, the total bypass resistance will be lower than the switch alone and therefore the bypass loss will be less than a switch alone. This is advantageous because the circuit is passive and a low minimum loss is a desirable quality due to the loss constraints on the system.

4.2.3 Attenuator Circuit Design

The resistance values required for the pi-pad core versus attenuation from (18) and (19) are shown in Fig. 26.

For low attenuation, high resistance to ground and low resistance in series are required. As attenuation increases, the resistance to ground decreases and the series resistor increases to dissipate more energy.

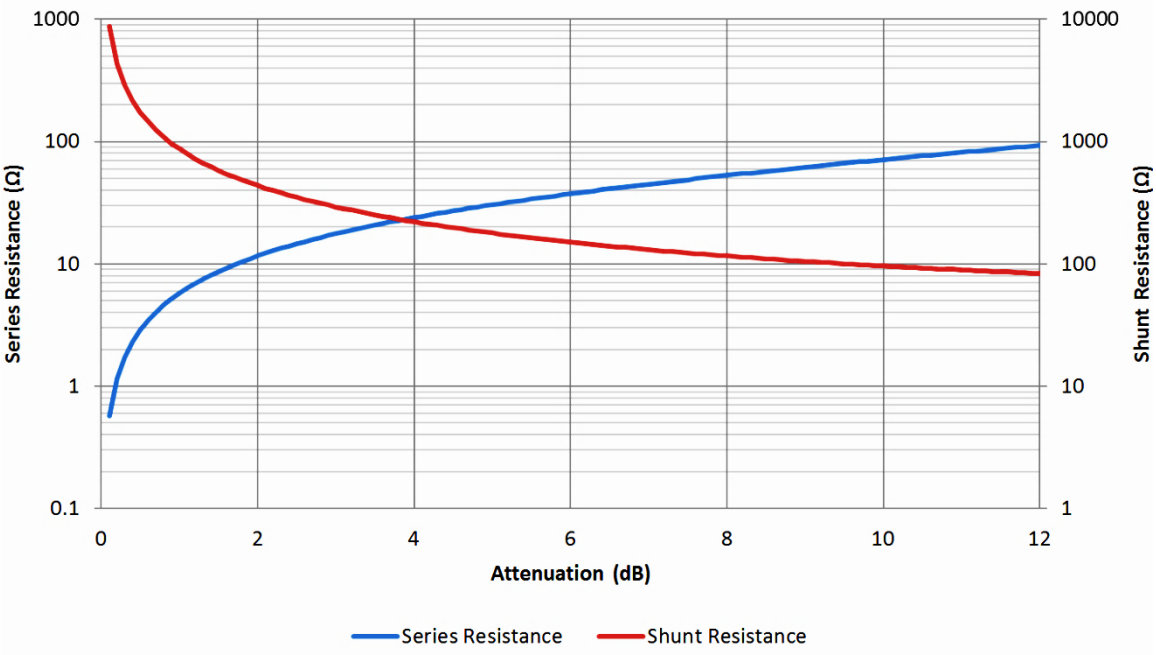

Fig. 26. Resistance values required for pi-pad core versus attenuation (dB)

The 5-bit schematic design which uses pi-pad attenuator cores is shown in Fig. 27. The bypass and shunt switches are oppositely driven via an inverter on the control bit.

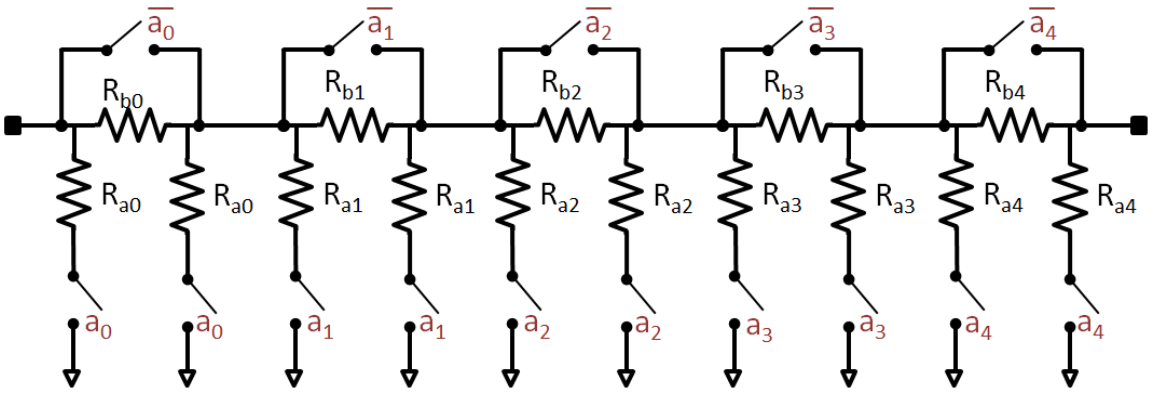

Fig. 27. Switch level schematic diagram for 5-bit passive attenuator

As discussed earlier, the switches have a non-zero ON resistance, therefore $R_{aX} = R_a – R_{ON}$, where R_{aX} is the shunt resistor and R_a is the total required shunt resistance including the switch found in (18).

The switches in this section are each two NMOS transistors in series. The larger the attenuation factor, the larger required switch to prevent the transistor from turning on unexpectedly. As will be discussed in the implementation chapter, it is desirable to have interchangeable stages for post-extraction tweaking, therefore all but the 11.2dB stage were made the same size. The bypass FETs were all the same but the shunt FETs differed in the 5^{th} stage. The first 4 stages were kept the size for the 4^{th} stage for interchangeability ease in layout, but the fifth stage required larger FETs which exceeded the footprint established for the first four.

4.3 Low Noise Amplifier Combiner Hybrid

A front end with a passive combiner before the LNA will increase the noise figure of the system by the forward loss of the combiner. This means that the NF specification for the LNA becomes more stringent because the specification is for the whole front end. Another concern is that a passive combiner is made from lumped elements; for example a 3-port device such as a Wilkinson combiner contains two inductors and a number of capacitors. One of the biggest factors in IC design is cost, and area consumption directly translates to cost. Therefore, an architecture that would forgo additional lumped elements, inductors in particular, is desirable from an economical point of view. The LNA combiner hybrid circuit has been filed as a provisional patent application through Skyworks with the United States Patent and Trademark Office.

4.3.1 Low Noise Amplifier Design

The LNA combiner hybrid design was conceived after an LNA had already been designed to the schematic level. The LNA at this point was then modified to have 3 ports and adjusted to attain the front end performance specifications. The LNA design was a traditional two-port simultaneous noise and power matched cascode LNA. The schematic for the cascode LNA is shown in Fig. 28.

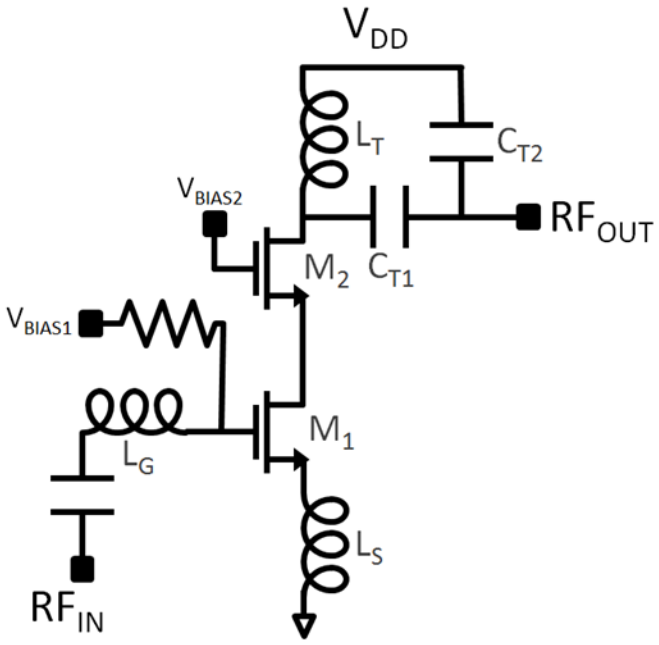

Fig. 28. A cascode LNA schematic

The LNA was designed by sizing the common source transistor M_1 and current density to have a minimum NF_{MIN} at a 50Ω input impedance, or G_{OPT} = 50Ω. L_S is sized to set the real part of the input impedance to 50Ω, and L_G is sized to cancel out the remaining imaginary part of the input impedance. The advantage to this method is that the LNA is now power matched but also matched for an optimum noise figure [14].

4.3.2 Combiner Hybridization

This goal of this circuit is to add two signals whose sum is amplified by the LNA, which traditionally would be achieved by a directional coupler. A directional combiner will ideally have minimal impact on the forward (received) signal, while superimposing the second signal on top of it at a desired attenuation, i.e. 10dB. Directivity cannot be achieved by a simple short; therefore the second signal needs to be injected into a different node than the original signal. Normally this would be where a discrete combiner would come into play in order to allow a gain path through the LNA for both signals as shown in Fig. 29.

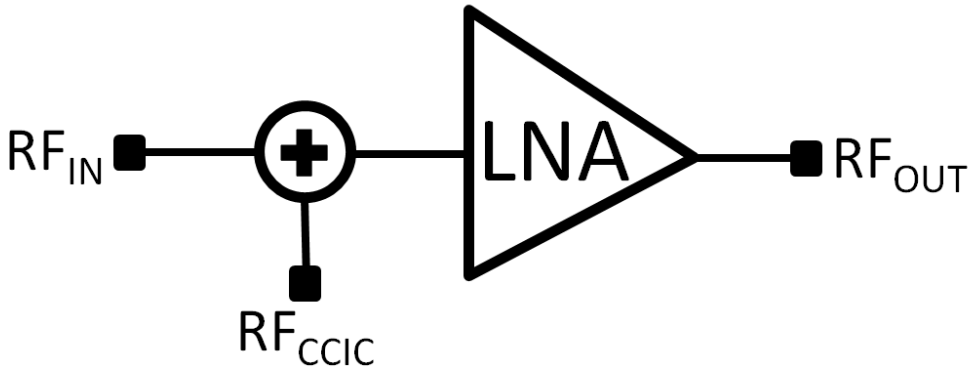

Fig. 29. System level diagram for front-end cancellation operation

The LNA combiner hybrid takes a 2 port amplifier and modifies it into a 3 port LNA where two signals are simultaneously applied to the LNA, one at the gate and one in the source. The reduced gain from injecting into the source doubles as the desired attenuation factor from a coupler. The circuit is shown in Fig. 30.

This circuit injects the copy (CCIC) signal into the source node of the common source transistor M_1 through an impedance buffer to perform the summation operation via the V_{GS} of M_1 as illustrated by superposition in Fig. 31. The combination produces a net V_{GS} equal to $V_{GS1} - V_{GS2}$. If V_{GS2} is made to be equal to V_{GS1} by properly sizing and

phase shifting V_2, then the net V_{GS} will be zero and the undesired portion of V_1 will be cancelled out. To illustrate this with regards to co-channel interference cancellation, V_{GS1} and V_{GS2} are assumed to be:

$$V_{GS1} = Asin(j\omega_o) + B_1 sin(j\omega_x + \theta_1) \quad (20)$$

$$V_{GS2} = B_2 \sin(j\omega_x + \theta_2) \quad (21)$$

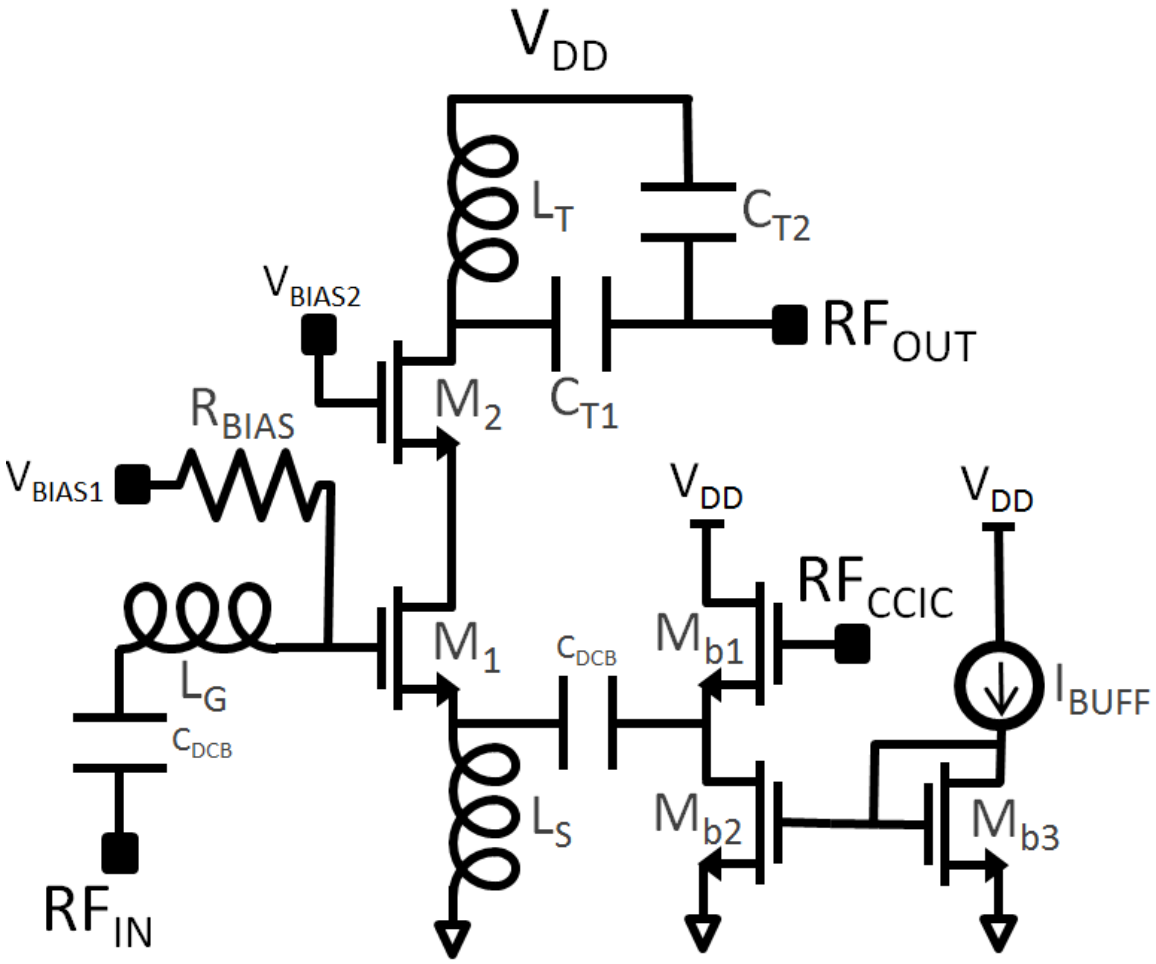

Fig. 30. A 3-port LNA combiner hybrid circuit

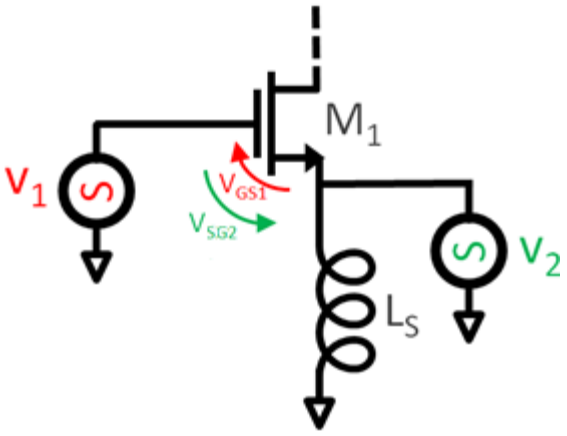

Fig. 31. Sum operation performed on the gate of common source transistor M_1

Signal V_1 contains a desired received signal and a co-channel interference term whose presence disrupts normal operation, generating V_{GS1}. The CCIC will create a copy of this interference and inject it as V_2, generating V_{GS2}. If V_2 is modulated such that the V_{GS2} amplitude $B_2 = B_1 = B$ and phase $\theta_2 = \theta_1 = \theta$, then the total LNA V_{GS} will become:

$$\begin{aligned} V_{GS} &= V_{GS1} - V_{GS2} \\ &= Asin(j\omega_o) + B_1 sin(j\omega_x + \theta_1) - B_2 \sin(j\omega_x + \theta_2) \\ &= Asin(j\omega_0) + (B - B)\sin(j\omega_x + \theta) \\ &= Asin(j\omega_o) \end{aligned} \tag{22}$$

Proper polar modulation of V_2, when injected into the source of the LNA combiner hybrid circuit, will cancel the co-channel interference component of the incoming signal V_1.

The load as seen from the impedance buffer of RF_{CCIC} is the parallel combination of the source inductor and the LNA impedance looking into the source. Usually the source inductor is quite small, in the area of 5Ω to 10Ω. This will likely result in a non-ideal (e.g. unmatched or high-loss) voltage divider, however, the application calls for 10dB coupling factor at the LNA, therefore this poor voltage divider limitation is not a disadvantage.

The LNA combiner hybrid circuit acts as the superposition of a common source amplifier (from RF_{IN}) and a common gate amplifier (from RF_{CCIC}) to a common output RF_{OUT}. The difference in gain between RF_{IN} and RF_{CCIC} inputs to RF_{OUT} forms the effective coupling coefficient. The benefit gained over a discrete passive combiner is the removal of pre-LNA loss as well as a significant area reduction. The benefit of using a buffer instead of a direct connection or transformation network connection is front end performance metric stability which will be discussed below. The trade-off penalty incurred in both cases is additional current consumption within the LNA combiner hybrid.

The purpose of the source follower in Fig. 30 is to act as an impedance buffer. Although the polar modulator is designed to maintain an acceptable output match to 50Ω over all phase and amplitude shifts (e.g. $S_{22} < -10$dB), in non-logarithmic values this represents a wide range of impedances. Limiting the discussion to real values for simplicity, −10dB corresponds to the range of impedance calculated below in (23).

$$\begin{aligned} S_{22} &= \pm 10^{-\frac{10}{20}} \\ &= \pm 0.316 = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{Z_{OUT} - 50}{Z_{OUT} + 50} \\ \pm 0.316 Z_{OUT} - Z_{OUT} &= -50 - (\pm 15.81) \\ Z_{OUT}(+0.316 - 1) = -65.81 \quad &OR \quad Z_{OUT}(-0.316 - 1) = -34.19 \\ Z_{OUT} = \frac{65.81}{0.684} = 96.21\,\Omega \quad &OR \quad Z_{OUT} = \frac{-34.19}{-1.316} = 25.98\,\Omega \end{aligned} \tag{23}$$

To facilitate the correct and consistent coupling coefficient, the impedance seen by the voltage divider would need to be controlled to a tight range. 26Ω to 96Ω, conversely, is an extremely wide range. In addition, the source node is low impedance

and the LNA is sensitive to the impedance in this node. The input match, noise figure, gain, linearity and stability would all be in flux if the source impedance were subject to large variations. A source inductance is typically small, in the range of a few hundred picohenries to a nanohenry. At 2.4GHz, this would range from approximately 4Ω to 10Ω. Worst case variation would occur at the high end of this range because the injected signal circuitry would form a parallel connection and 10Ω will be less dominant than 4Ω. The effective circuit from the LNA is shown in Fig. 32.

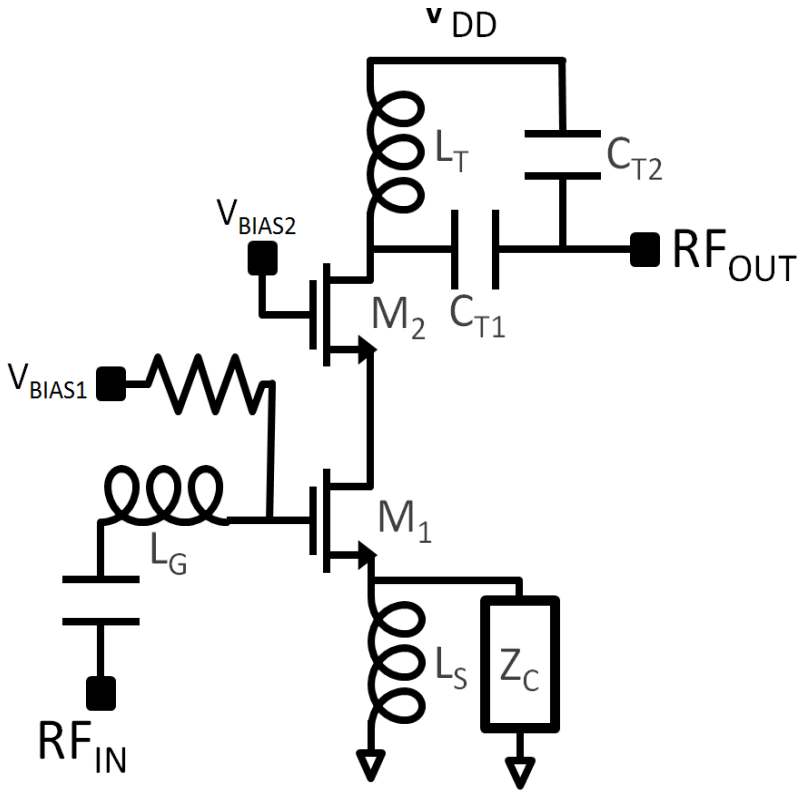

Fig. 32. Effective circuit seen by the cascode LNA RF_{IN} input

To demonstrate the mathematical variation using real impedances for simplicity, the effective source impedance becomes:

$$LOW:\ Z_S = 26\Omega||10\Omega = 7.2\Omega \tag{24}$$

$$HIGH: Z_S = 96\Omega||10\Omega = 9\Omega \tag{25}$$

This variation in the source would cause sizable variation to the LNA performance metrics discussed above. The polar modulator output impedance variation would cause substantially more variation to the coupling coefficient due to the voltage divider between the output impedance (26Ω to 96Ω) and input impedance looking into the source ($(4\Omega \leq Z_{OUT} \leq 10\Omega) \parallel Z_{SOURCE}$). A quick example shows this variation for a 5Ω source input impedance, disregarding the additional gain terms from a common gate amplifier.

$$Coup_{HIGH} = 20\log\left(\frac{5\Omega}{25+5}\right) = 20\log\left(\frac{1}{6}\right) = -15.6dB \tag{26}$$

$$Coup_{LOW} = 20\log\left(\frac{5\Omega}{95+5}\right) = 20\log\left(\frac{1}{20}\right) = -26dB \tag{27}$$

For a 5Ω source input impedance, the coupling factor varies by >10dB which is not acceptable; therefore, an alternative solution is required.

An impedance buffer can maintain fairly constant output impedance over changing input conditions. The output impedance of the buffer can also be designed to provide the desired coupling factor, which eliminates the need for an area intensive matching network. Therefore, in exchange for current, a buffer can ensure coupling and LNA performance consistency.

The buffer was designed with an approximate current of 12mA which produced a 20Ω output impedance. In the system level this equated to an approximate 10dB coupling factor when comparing the common source gain to the common gate path gain.

Chapter 5: Layout and Implementation

This chapter will outline the layouts of all of the designed circuits, followed by an overview of the chips designed. There were two tape outs completed and 48 total variants taped out, however, this chapter will discuss the primary variants designed and any major layout considerations for the design of the sub-circuits.

5.1 Layout Design

5.1.1 Phase Shifter

The phase shifter had two different layouts in two different tape outs. The primary chip did not have any restraints on the architecture of the phase shifter so it was able to be a simpler linear layout. The final tape out required a change to the positioning of the inductors in the design. In addition, the use of a planar EM simulator became available therefore some additional changes were made to metallization and inductor sizing. Fig. 33 shows the final layout for the full CCIC system tape out, and the prototype layout from the original tape out is shown in Fig. 43.

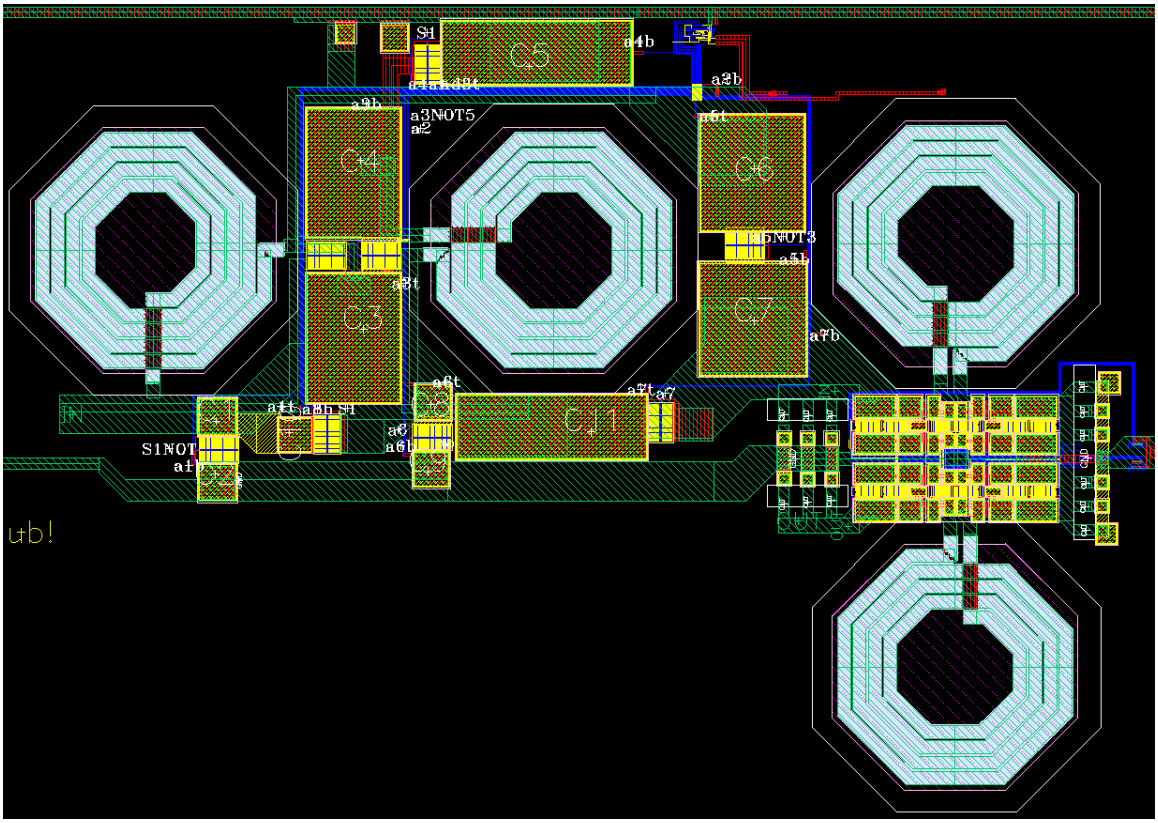

Fig. 33. Phase shifter layout from final CCIC tape out

The layout of the fine shifter is shown in Fig. 34. To maximize the area efficiency with two identical inductors and a symmetrical design, the four variable capacitor banks were placed symmetrically along both center axes between the inductors to minimize area. Laser trim-able tuning capacitors were placed on each RF net in the circuit to enable laser trimming. The variable capacitor bank layout is shown in Fig. 35. The quadrant shifter layout in Fig. 36 remains the same in both tape outs with the exception of the inductor dimensions. The quadrant shifter logic design and layout can be found in Appendix A.2.

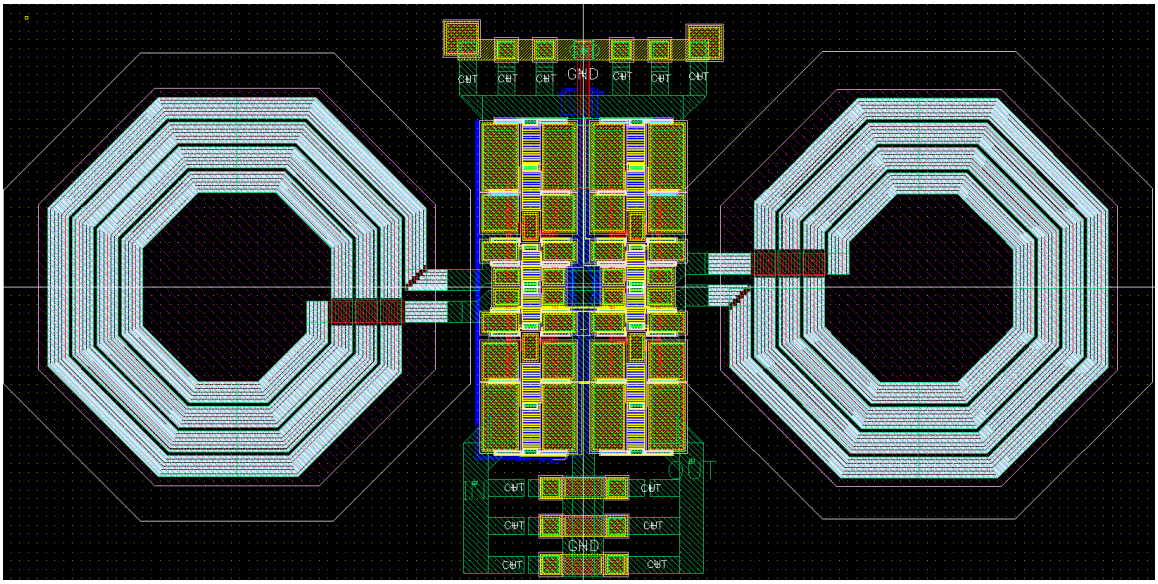

Fig. 34. Fine shifter layout

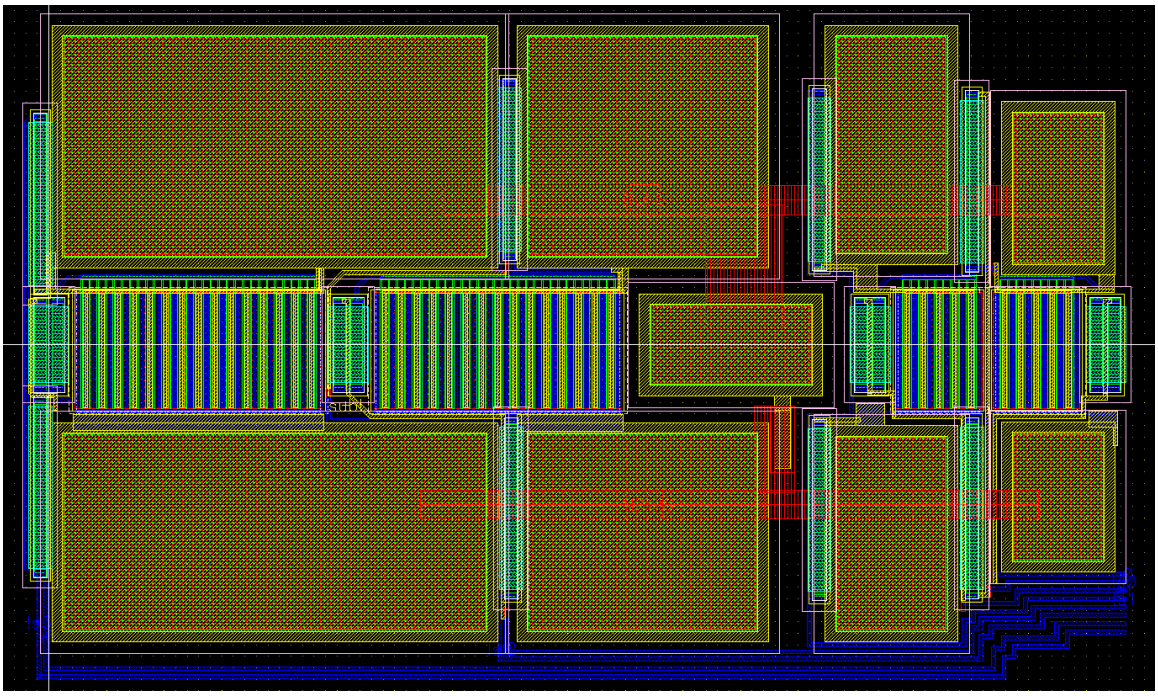

Fig. 35. High-ratio variable capacitor bank layout

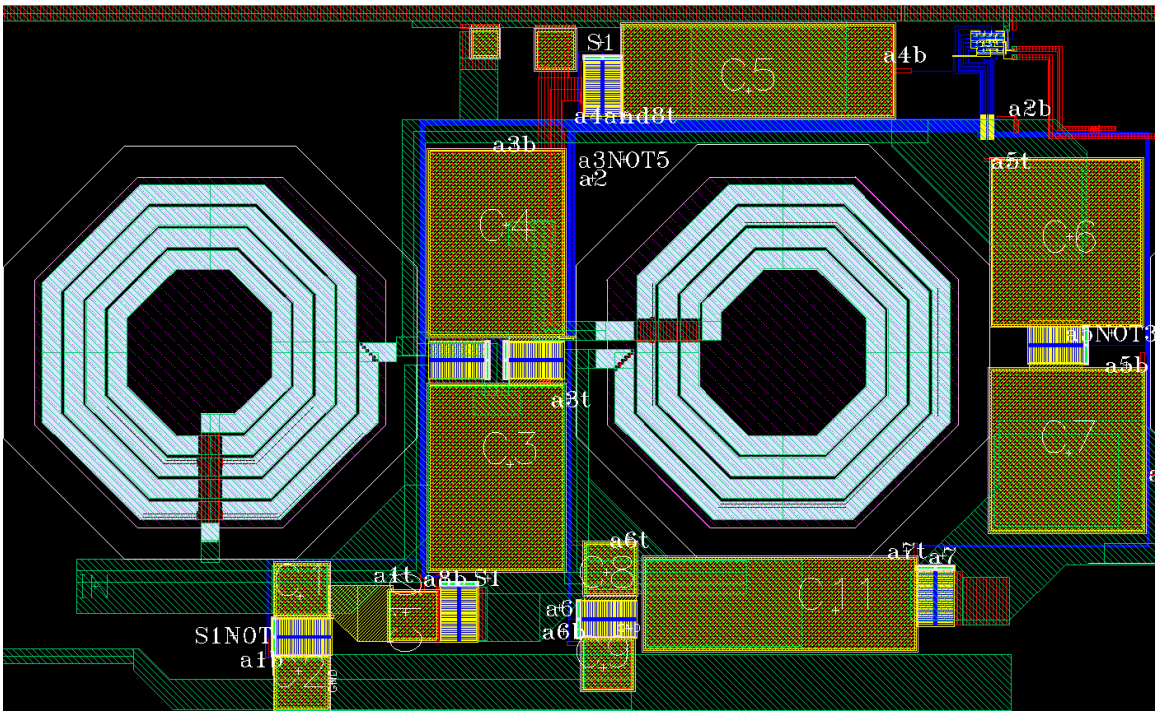

Fig. 36. Quadrant shifter layout

The complex schematic of the quadrant shifter required ground connections to occur at both the top and bottom of the circuit, with the upper boundary of the chip providing one ground connection, and the center of the chip (bottom of Fig. 36) having a ground connection come from the left border of the chip, and sharing the ground connection of the fine shifter seen in Fig. 33 which originates from the right side of the chip. There is a break in the metal at the top of the chip to prevent a loop antenna from being formed in the ground ring.

5.1.2 Attenuator

When designing the attenuator cores with layout in mind, there were three primary concerns:

- Resistance Process Variation: As seen previously, the required series resistance becomes very small as the required attenuation becomes small. At these physical

sizes – for a single resistor, ΔL and ΔW become more dominant, however this is addressable with design choices. Using larger resistances in parallel will reduce this effect at the expense of area. In some cases, the resistance may not be buildable with a single resistor without breaking minimum dimension design rules.

- Power Handling: The maximum current density in each resistor needs to be considered. The power level will be fairly high (0-5dBm) at the attenuator, therefore the devices current handling capability needs to be taken into account.
- Interchangeability of the attenuator stages: in order to facilitate ease of adjustability in post-layout simulations, it was decided that it was important to be able to change the order of the attenuator stages easily.

These three concerns have mutually beneficial solutions. In order to construct accurate low-ohm resistors, many resistors will be placed in parallel. The parallel resistor configurations will ensure that the minimum current density specifications are met. In order to aid process variation resistor-to-resistor, unit resistors will be placed in a grid structure so that they are self-dummying and area efficient. Self-dummying refers to each resistor having an identical resistor on all sides but the resisters aren't exclusively dummy resistors. The outer ring will be dummy resistors; however, the inner active resistors can be seen as dummies of each other. In other words, the resistor grid is self-dummying. These actions enable each stage to conform to the same grid structure, differing only in metallization, and enable ease of interchangeability.

For brevity, the 0.7dB section will be discussed here, followed by the final resulting layout of the complete attenuator. The 0.9dB core has resistances of 5.2Ω and

952.5Ω. The resistor networks using a unit 404Ω (2µm width) resistor are 78 in parallel for 5.2Ω and 3 series resistors in parallel with 11 series resistors for 952.5Ω. The shunt resistor differs from the required R_a value because it takes into account the series resistance of the switch used as mentioned in chapter 3.

The unit resistors are arranged in a grid and connected to form these resistors, with dummies filling out the rest of the core. The 0.9dB core is shown below in Fig. 37. The entire stage, when combined with the bypass and shunt switches, is shown in Fig. 38.

The total layout of the attenuator is shown in Fig. 39. The original design was rectangular, but spacing constraints on the chip required a different architecture.

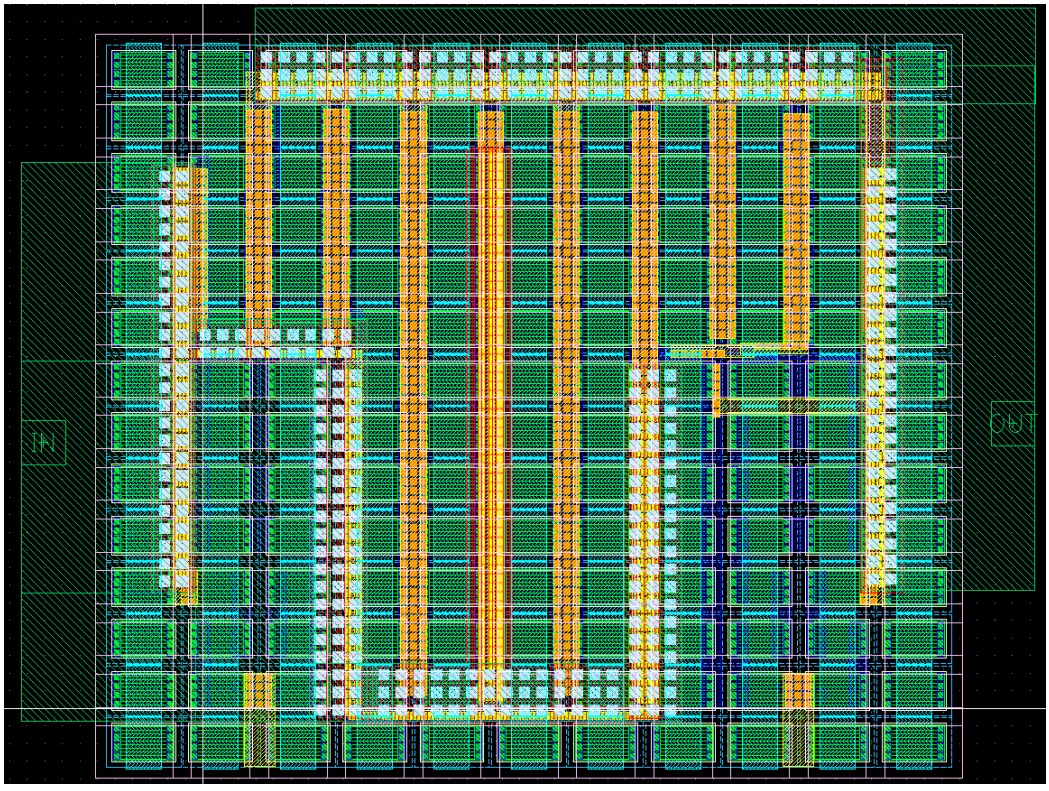

Fig. 37. Layout of 0.9dB attenuator core composed of self-dummying resistor grids

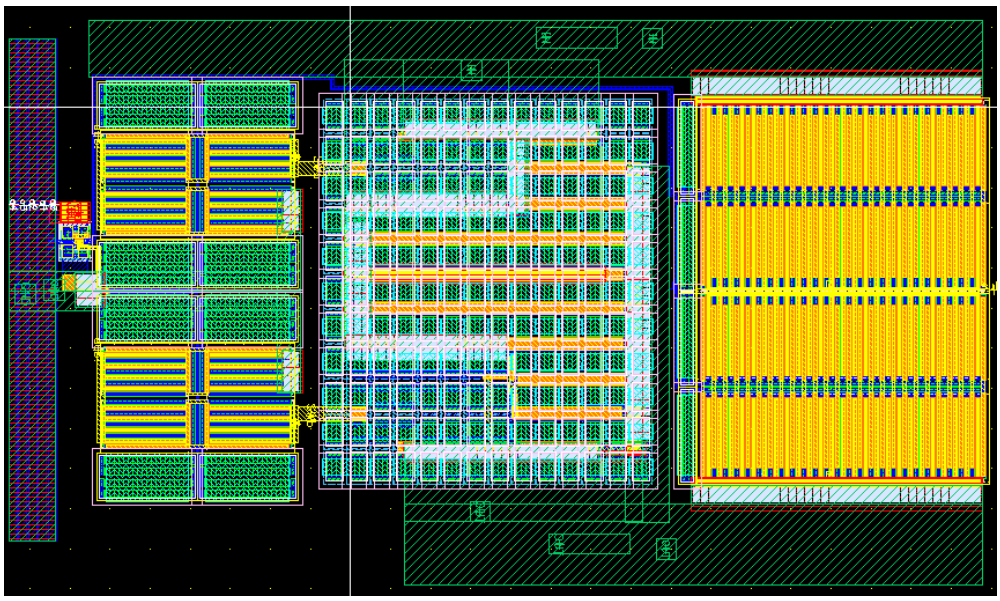

Fig. 38. Layout of complete 0.7dB attenuation stage

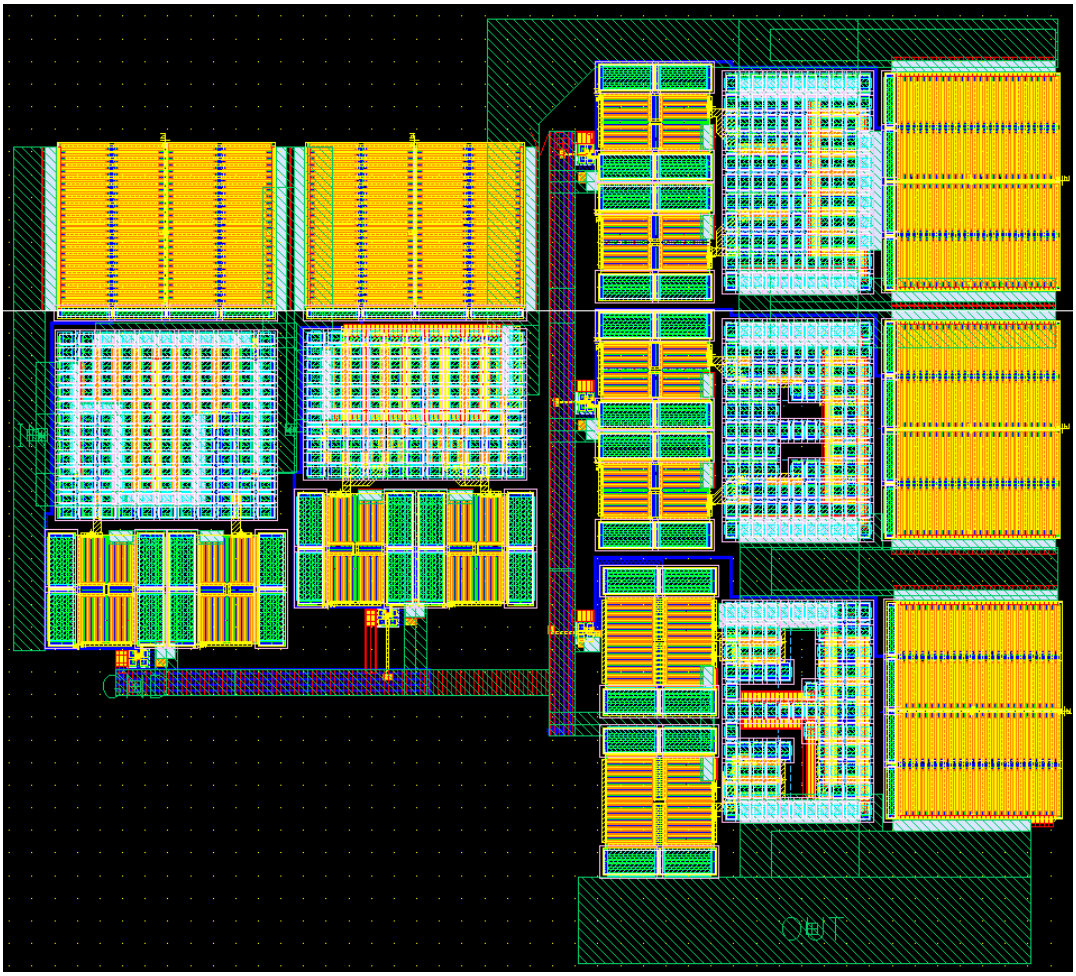

Fig. 39. Layout of 5-bit passive attenuator

5.1.3 LNA Combiner Hybrid

The LNA combiner hybrid is composed of the impedance buffer source injection circuit and the LNA. The LNA layout is shown in Fig. 40 and the impedance buffer is shown in Fig. 41. The LNA source inductor is composed of the bond wire to ground, allowing for maximum Q and maximum tunability. The impedance buffer, which injects the CCIC copy signal, also connects to this node, denoted with L_SOURCE in Fig. 40. The complete circuit is shown in Fig. 42.

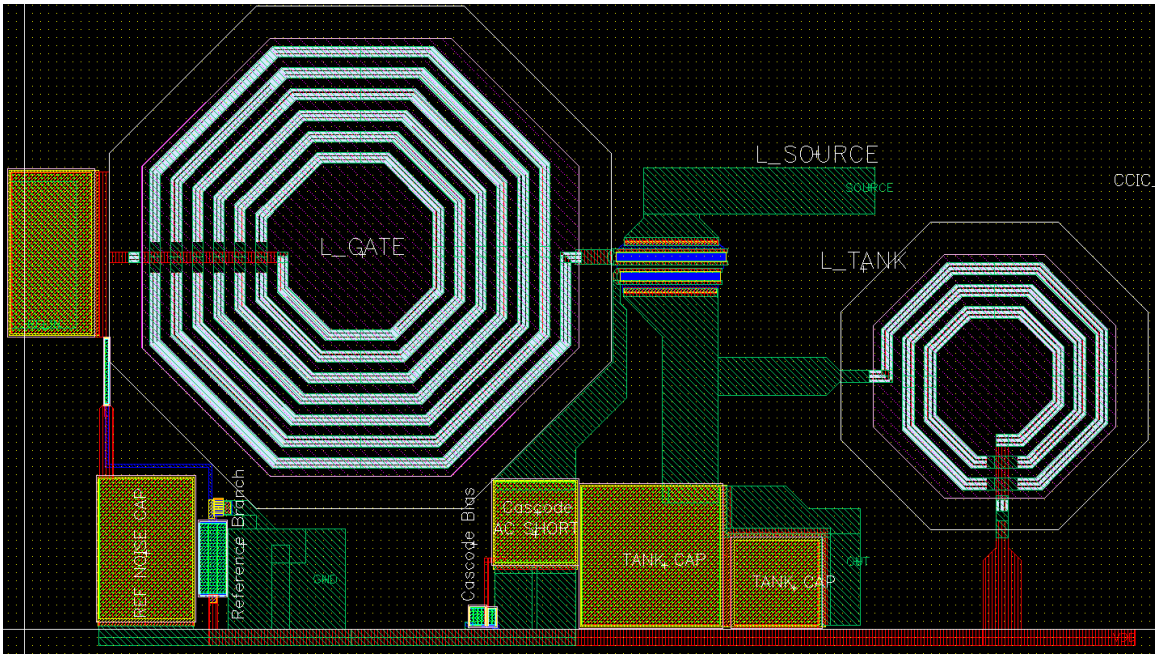

Fig. 40. LNA layout

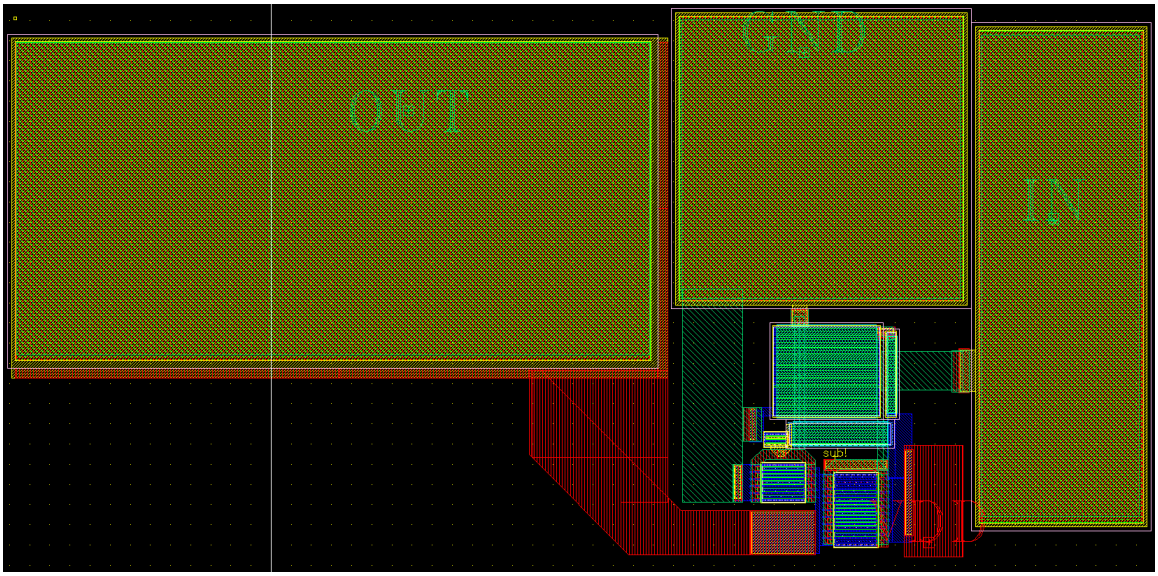

Fig. 41. Impedance buffer layout

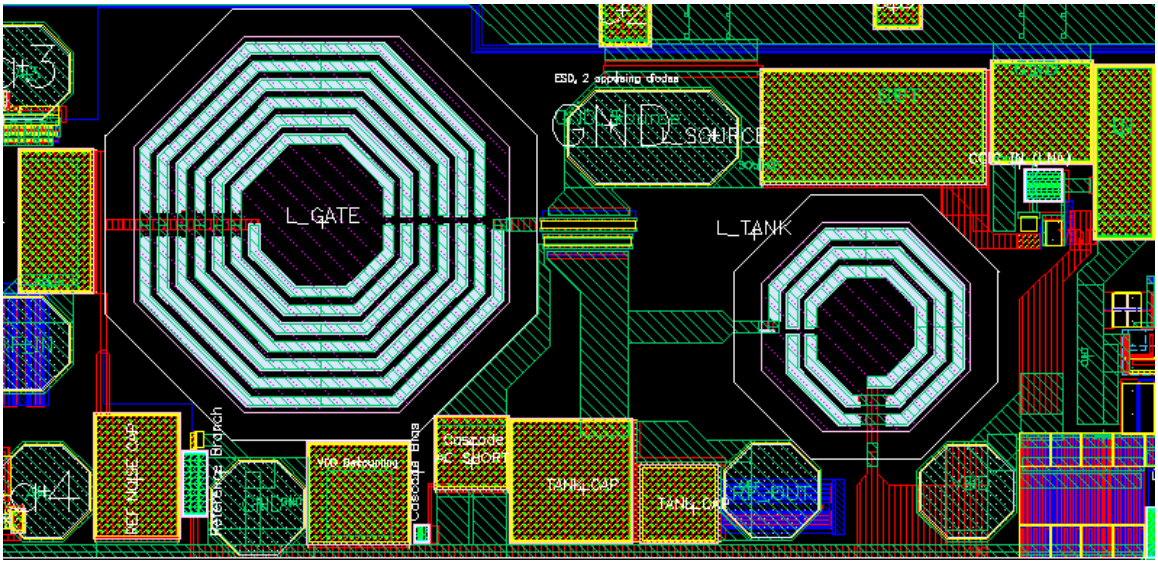

Fig. 42. LNA combiner hybrid layout

5.2 Chip Design Overview

The two tape outs that occurred were completed in a commercial 130nm Silicon-on-Insulator (SOI) RF CMOS process. The process has 4 metal layers comprising of 2 thick and 2 thin layers. The first chip designed was to test the phase shifter prototype. The second was the final design containing the entire CCIC system.

5.2.1 Phase Shifter Chip

The ambidextrous quadrant selector and fine phase shifter test chip measured 1400µm x 600µm and had a total die area of 0.84 mm^2. This area included unused space, bond pads, and ESD structures. The circuit utilized an on-chip area of approximately 0.47 mm^2. There are two RF pins, 6 control pins, 3 ground pins, and one voltage supply pin. The layout is shown in Fig. 43. The photomicrograph is shown in Fig. 44. The chip is shown bonded in an open face package in Fig. 45. The bonding diagram can be found in Appendix A.1.

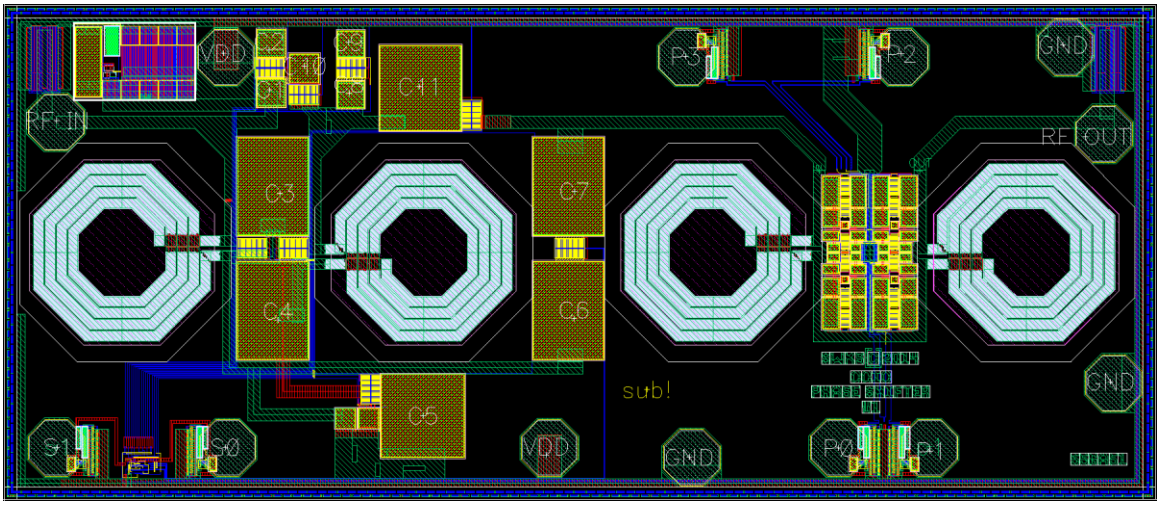

Fig. 43. Phase shifter test die, 1400µm x 600µm

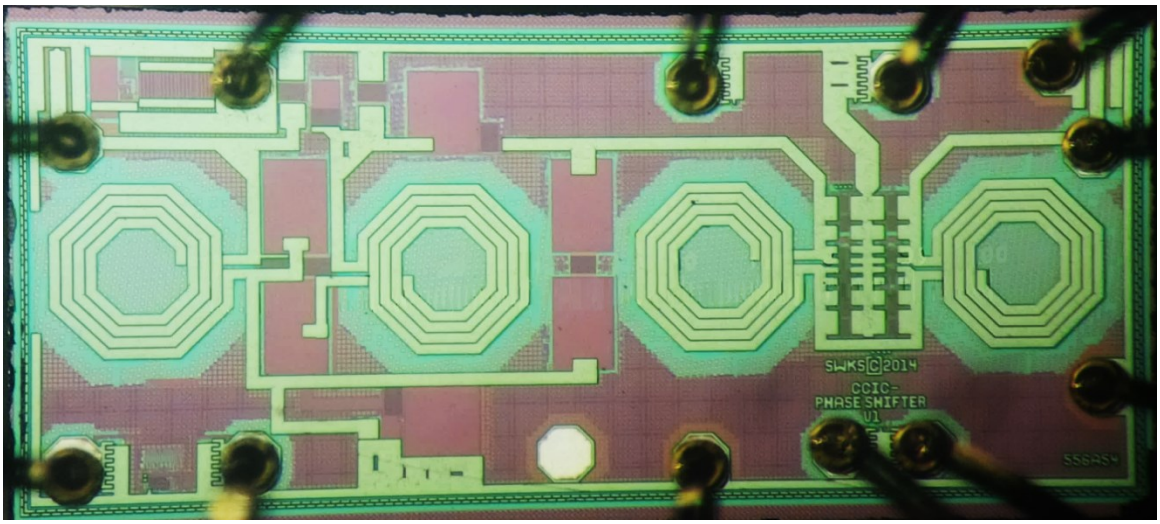

Fig. 44. Phase shifter photomicrograph

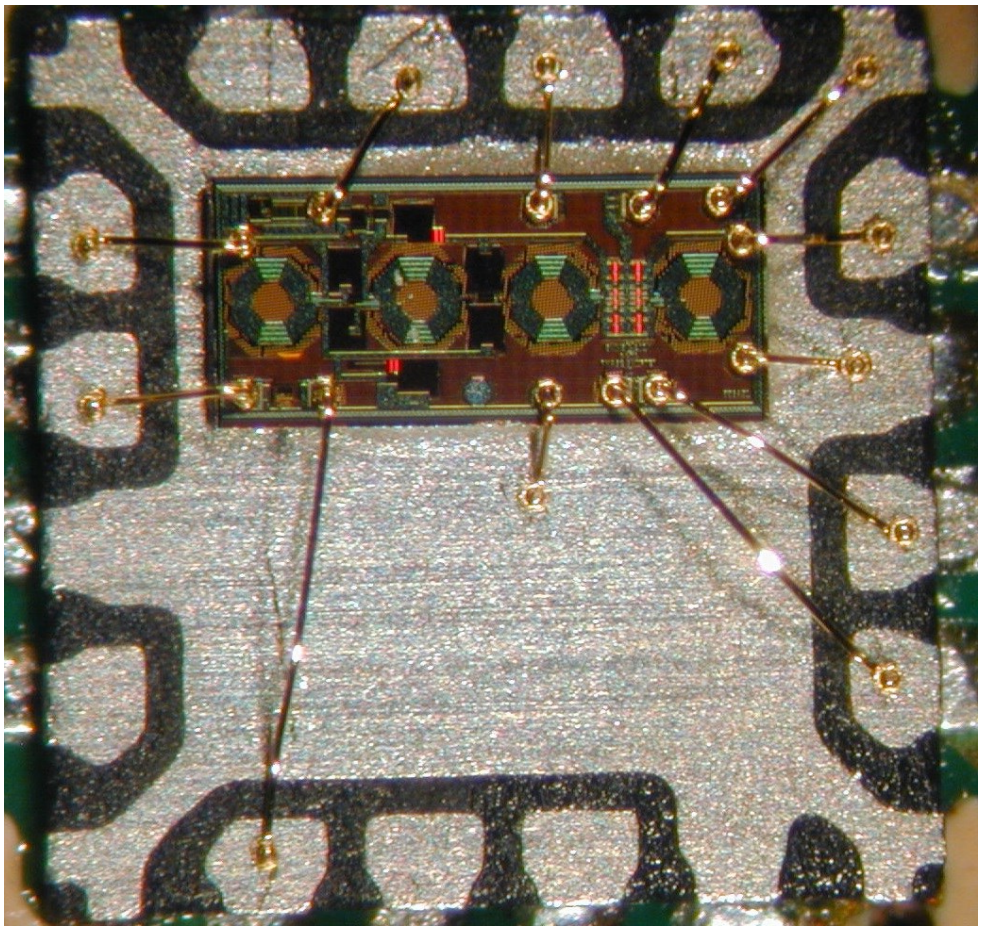

Fig. 45. Phase shifter die bonded in open faced 16 pin package

5.2.2 CCIC Chip

The full CCIC design utilized an on-chip area of approximately 0.78mm^2 on a chip measuring 1400µm x 850µm, for a total test die area of 1.19mm^2. There are 3 RF pins, 11 control pins, 3 voltage supply pins (2 for V_{DD_LOW}, 1 for V_{DD}), and 4 ground pins. The layout is shown in Fig. 46, and the photomicrograph is shown in Fig. 47. The chip is shown bonded into an open face package in Fig. 48. The bonding diagram can be found in Appendix A.1

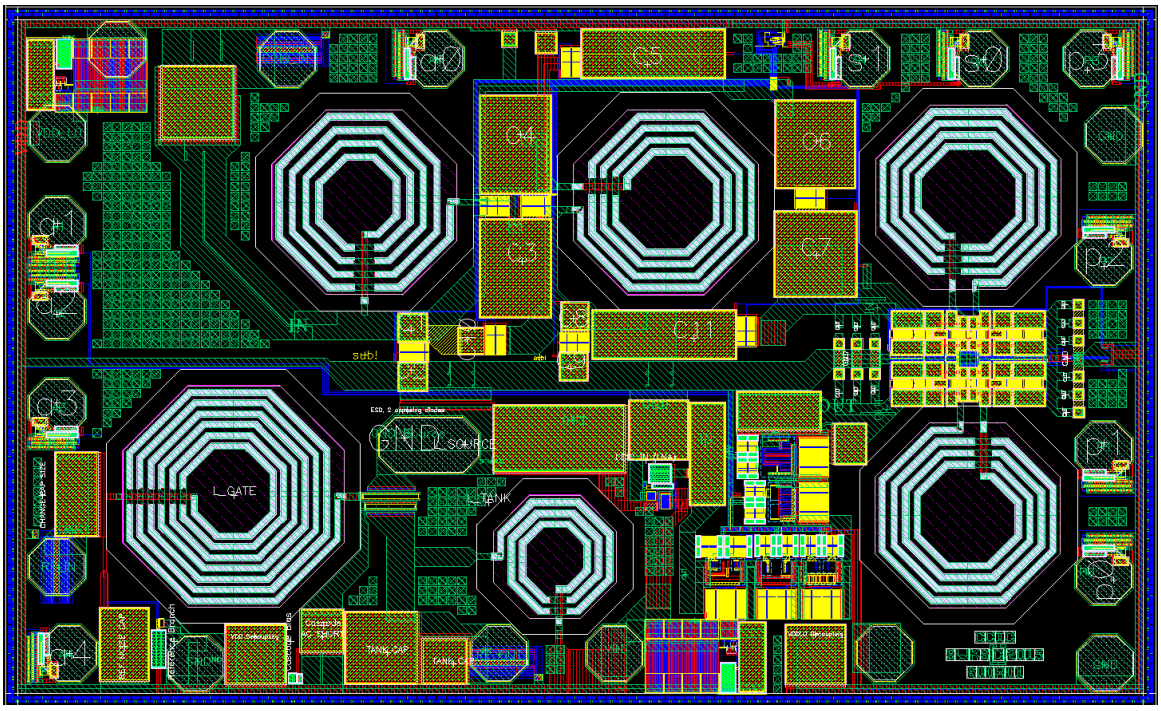

Fig. 46. Full co-channel interference canceller (CCIC) layout, 1400µm x 850µm

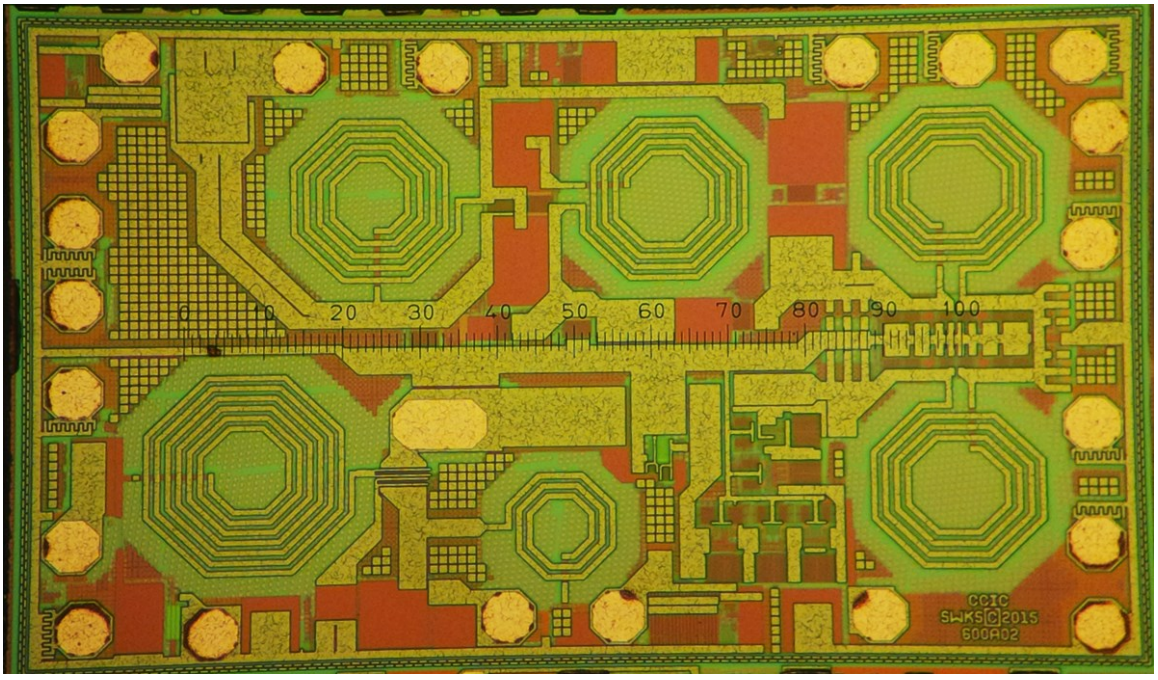

Fig. 47. Co-channel interference canceller photomicrograph

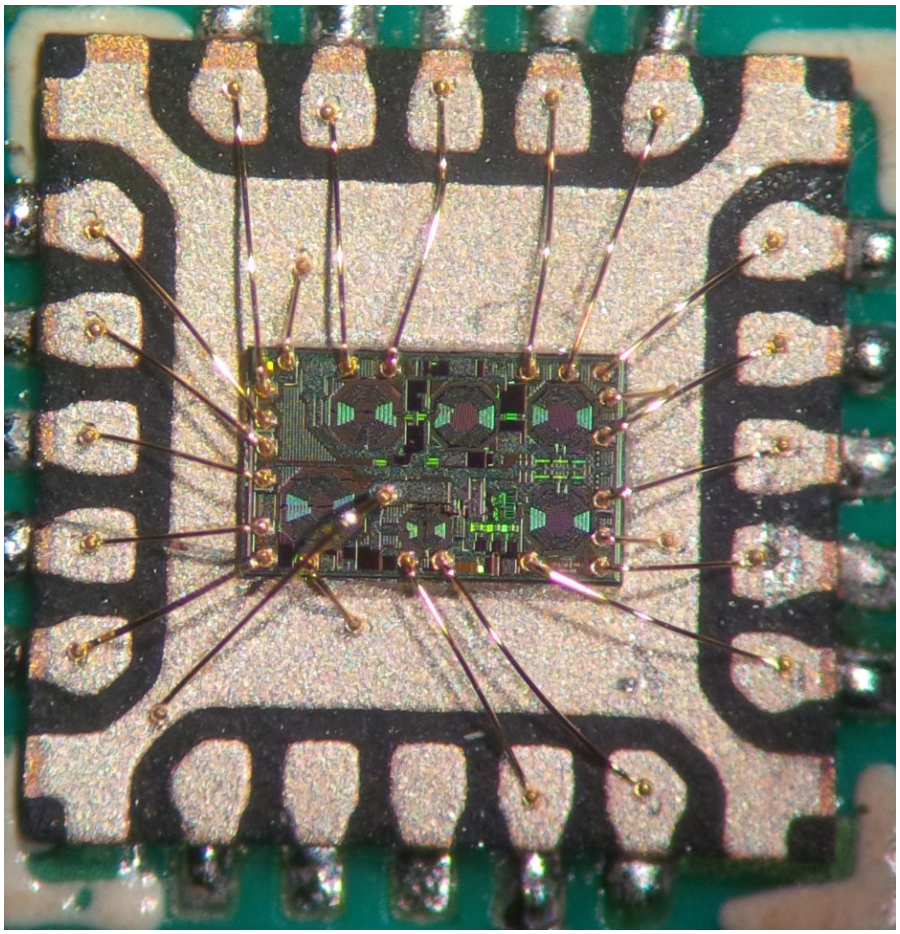

Fig. 48. Co-channel interference canceller die bonded in open faced 20 pin package

5.3 Printed Circuit Boards

There were two evaluation boards designed for the CCIC, a measurement board and a demonstration board. The phase shifter chip re-used a Skyworks evaluation board for simplicity and will not be included in this section. The demo board was 4-port and contained a 10dB coupler to simulate the transmit side coupling into the CCIC input. The measurement board was 3-port and was used to measure the performance parameters such as s-parameters, linearity, and noise figure. Both boards contain the same control/indicator circuitry which has LEDs to indicate the phase and amplitude state, along with mechanical DIP switches to manually control the state. The state can be

controlled externally via the header on the right side of the board. The bare boards (demonstration on the left and testing on the right) are shown in Fig. 49, and the 3-port board without package and chip is shown in Fig. 50. The long vertical track in the demonstration board between coupler and CCIC chip was to minimize any coupling between the two horizontal tracks which contain the coupling signal.

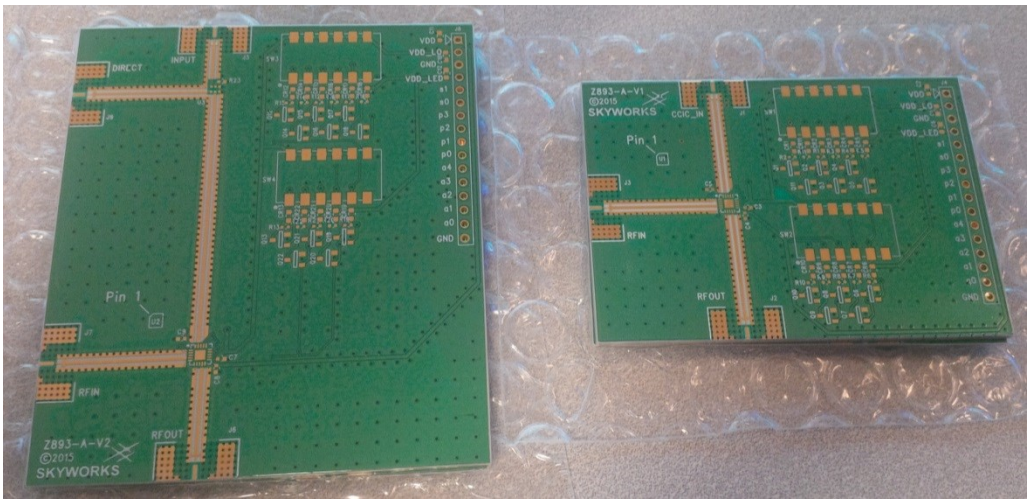

Fig. 49. Bare CCIC demonstration (left) and test (right) boards

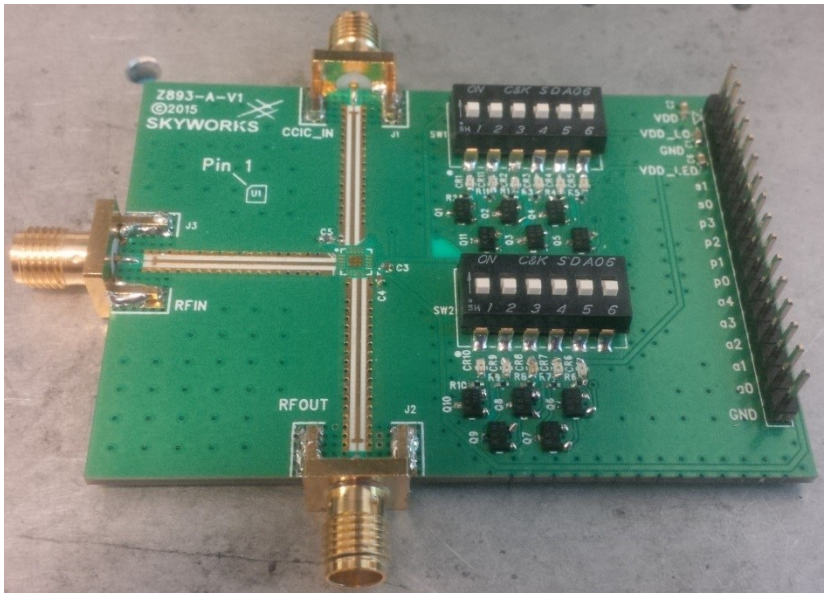

Fig. 50. CCIC Test Board

Chapter 6: Simulation Results

This chapter will present the relevant extracted simulated results of the CCIC and sub-circuits. Section 6.1 will show the polar modulator and buffer chain simulation results, and section 6.2 will discuss the full system (polar modulator, buffer, LNA combiner) simulations.

6.1 CCIC Polar Modulator and Buffer

The polar modulator was buffered in order to present more constant output impedance to the LNA combiner hybrid, as discussed in Chapter 4. The function of this circuit is to enable access to 2048 points in the polar constellation. Each quadrant has 4 bits of phase shift and 5 bits of attenuation for 512 points per quadrant. The passive polar modulation network (attenuator and phase shifters) in series with the buffer circuit was extracted and simulated and a polar plot showing magnitude and phase at the output of the buffer is shown in Fig. 51. The complete circuit will also include common gate amplification from the LNA. Note that each quadrant was designed to overlap slightly to ensure no large gaps occur after fabrication – this can be seen by the 4 groupings of tight points in the phase axis. All angles are covered and it can be seen that the attenuator covers greater than 20dB of amplitude range.

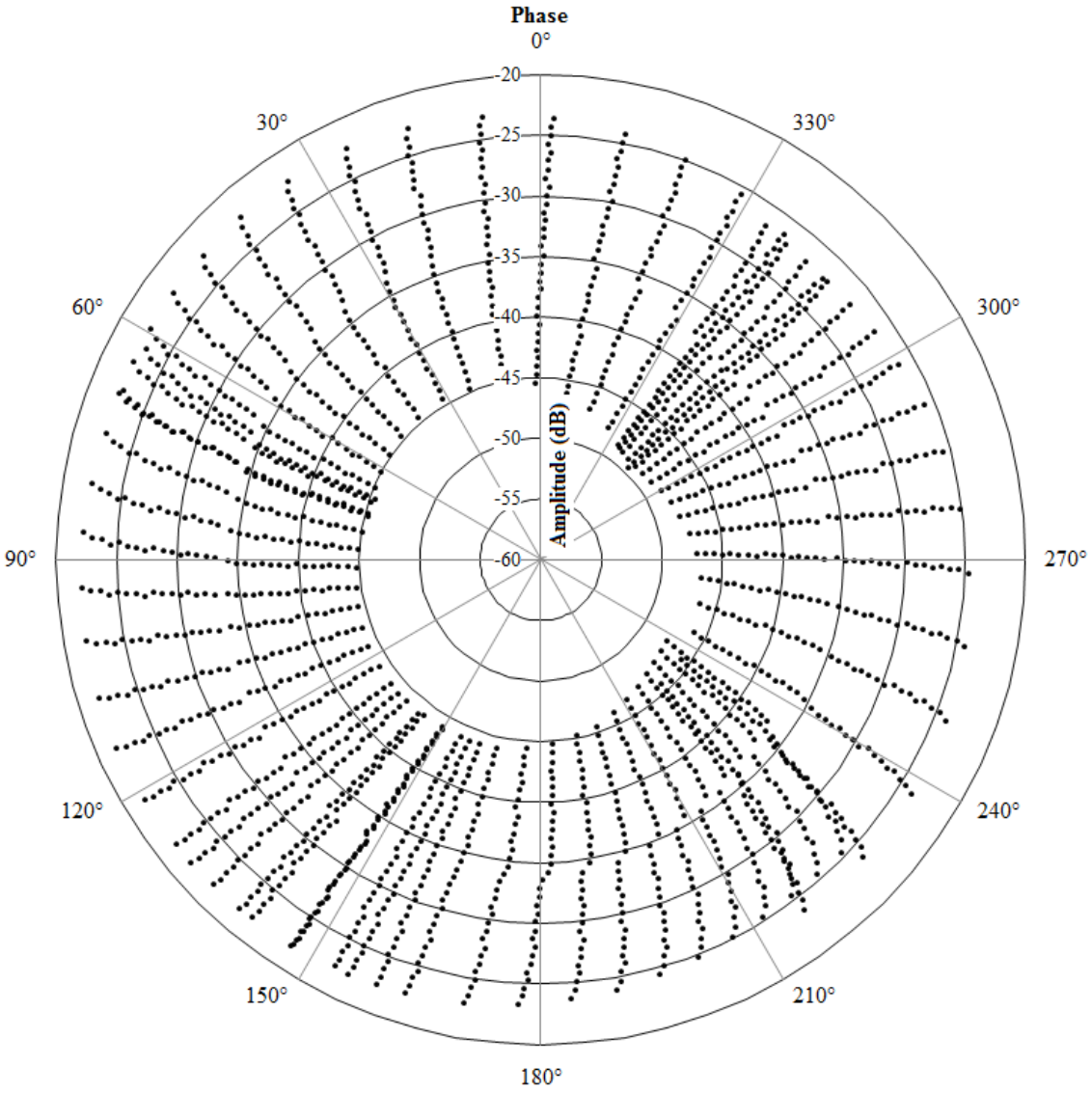

Fig. 51. 2048 polar states at the output of the impedance buffer

6.2 Full System Simulations

The full system was extracted and simulated, including the expected bond wire inductances and resistances. The simulated DC current consumption was 32mA total for the LNA and impedance buffer, with 18mA consumed by the LNA and 14mA consumed by the buffer. The assumed inductance and resistance for a 1mm bond wire was 1nH and 0.25Ω respectively based on models provided. The test bench is shown below in Fig. 52.

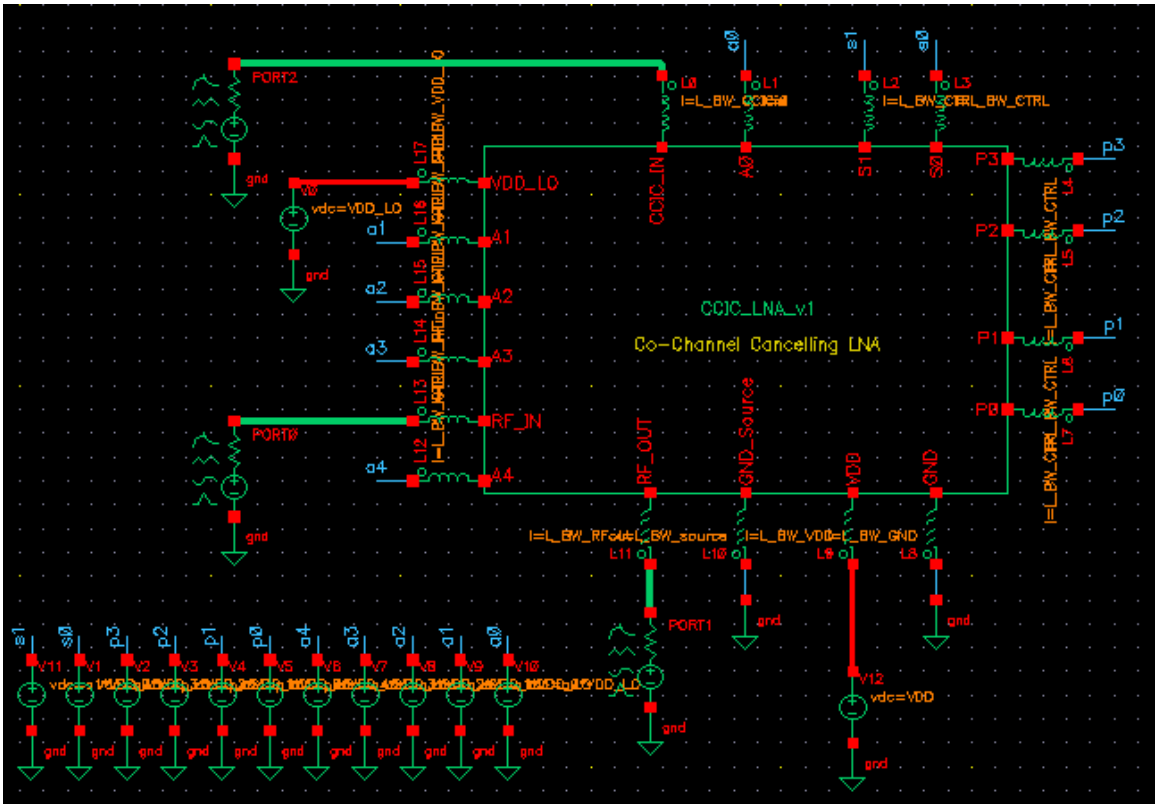

Fig. 52. Full CCIC testbench in Cadence

In Fig. 52, the thick green nets are RF nets and the red nets are power lines. All ground pins are down bonds to the package; however GND_Source on the bottom is the bond wire from the source of the LNA; this is tunable by modifying its length and height from the fabricated chip. All other blue nets are the control pins. The system is simulated assuming 1nH inductance on the RF lines and control lines. The other ground down-bonds are assumed to be 400pH. The source bond wire is varied to observe its effect. VDD is the high power supply at 2.5V and VDD_LO is the lower power supply for the passive devices and is 1.5V.

The input referred third order intercept point (IIP3) was simulated over 2048 control states in steps of 4 (512 total simulations). The interpolation point in all simulations was −50dBm and is shown in Fig. 53.

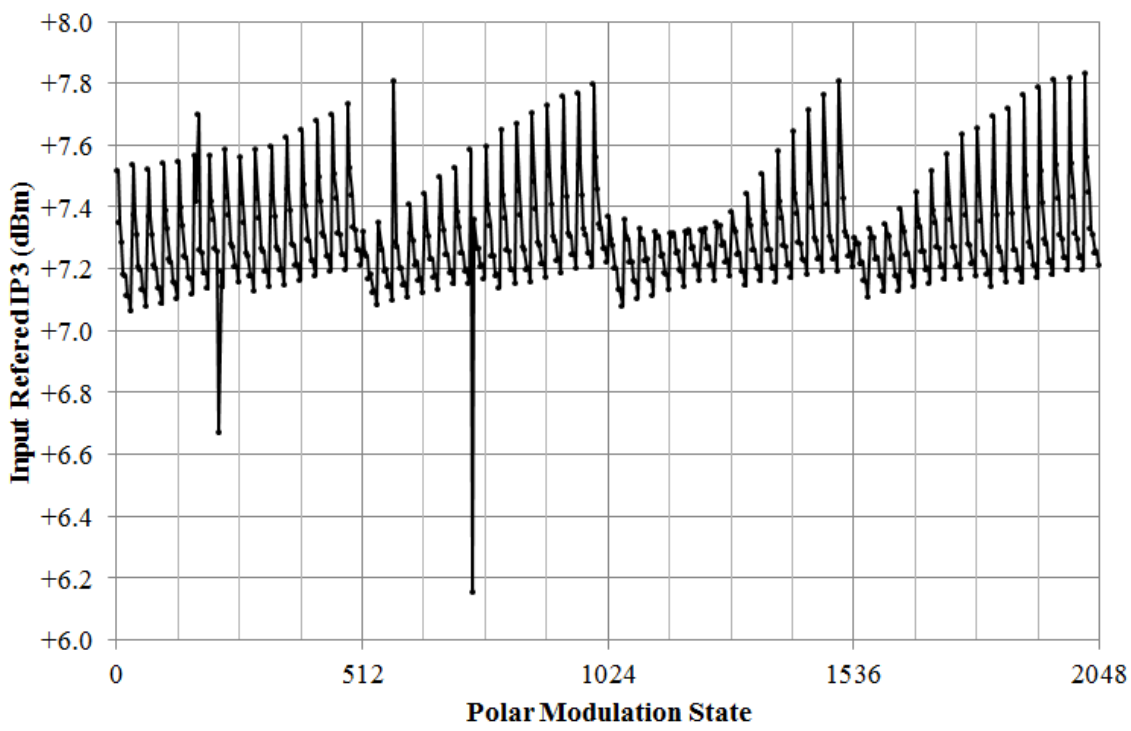

Fig. 53. Simulated IIP3 vs. polar modulation state

The simulated linearity of the CCIC exceeds the required +5dBm across all polar modulation states. The simulated 2-port s-parameters versus control state at 2.35GHz is shown in Fig. 56. The simulated 2- and 3-port s-parameter data over frequency are shown in Fig. **54** and Fig. 55 respectfully. The simulated noise figure (NF) and minimum noise figure (NF_{MIN}) at 2.35GHz is shown in Fig. 57. The CCIC Attenuation – or the difference in gain from the CCIC input to the output compared to the forward gain is shown in Fig. 58, and the simulated phase shift performance ($S_{32(deg)}$) is shown in Fig. 59. The important phase shift parameter is the difference between the CCIC applied phase shift (S_{32}) and the phase shift change occurring in the LNA (S_{21}) due to the polar modulator change. Ideally, the change in phase in the LNA over polar states will be zero. The phase shift of the LNA is shown in Fig. 60, and the complete CCIC polar coverage, factoring in the LNA phase shift is shown in Fig. 61.

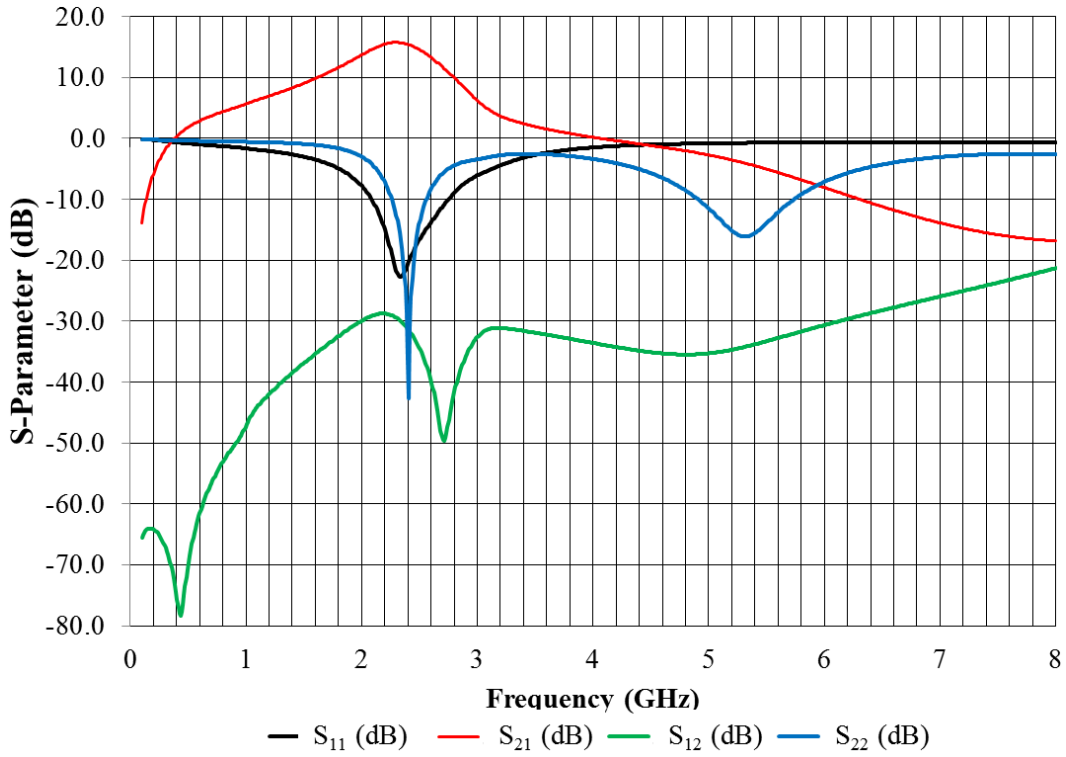

Fig. 54. Simulated CCIC s-parameter performance versus frequency (2-port)

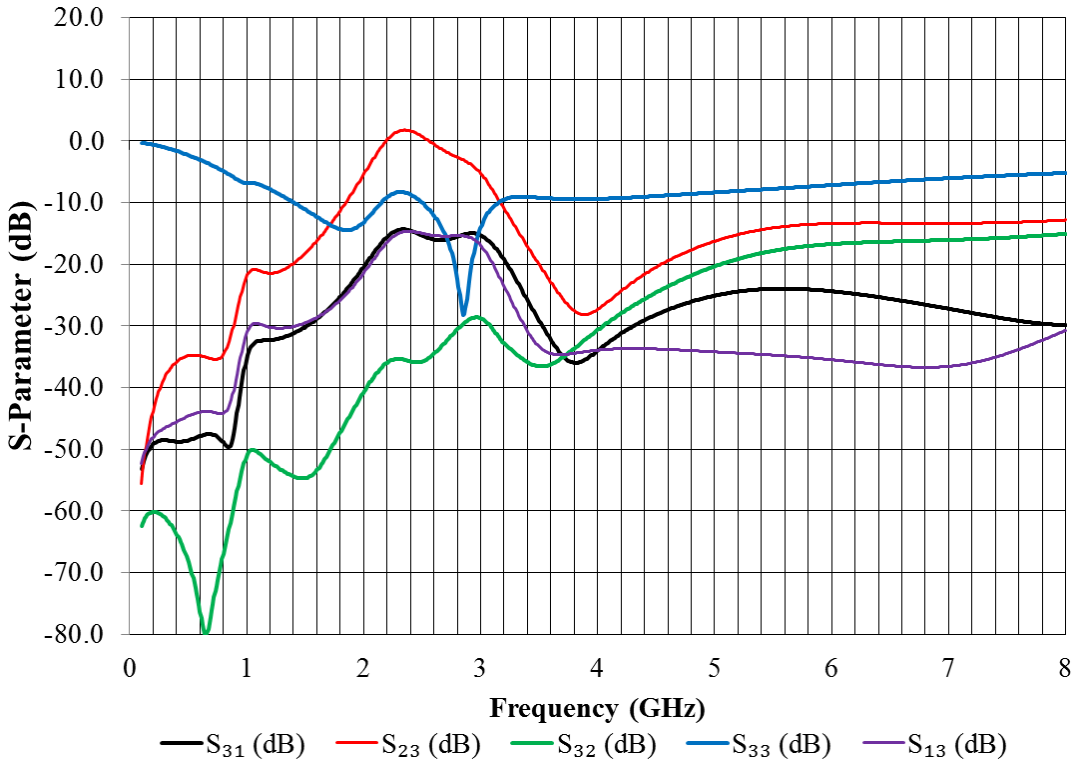

Fig. 55. Simulated CCIC s-parameter performance versus frequency (3-port)

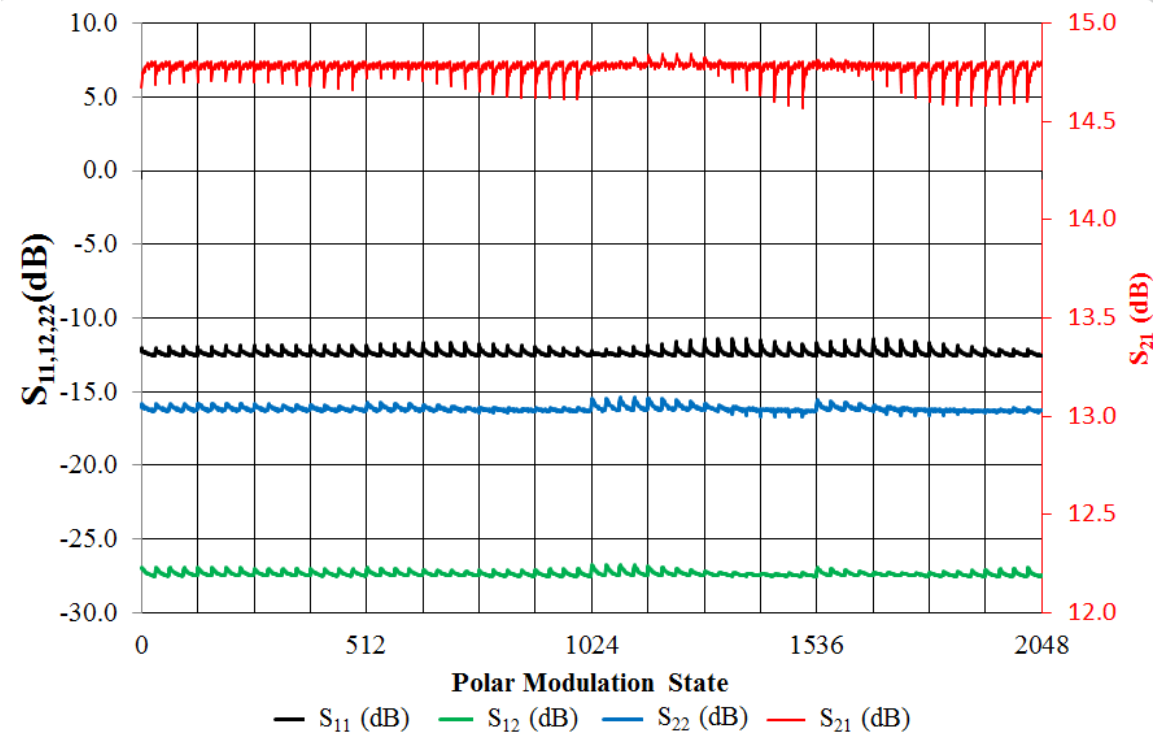

Fig. 56. Simulated CCIC s-parameter performance versus polar modulation state

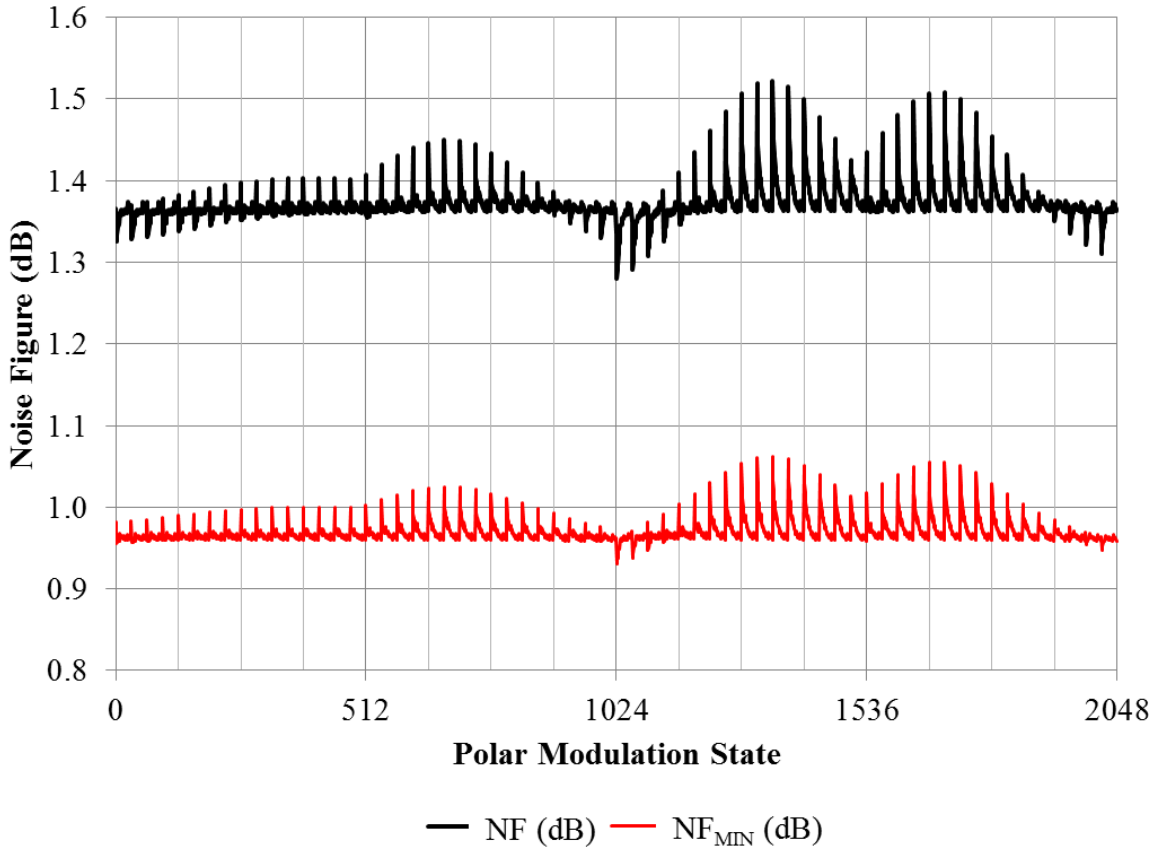

Fig. 57. Simulated CCIC noise performance versus polar modulation state

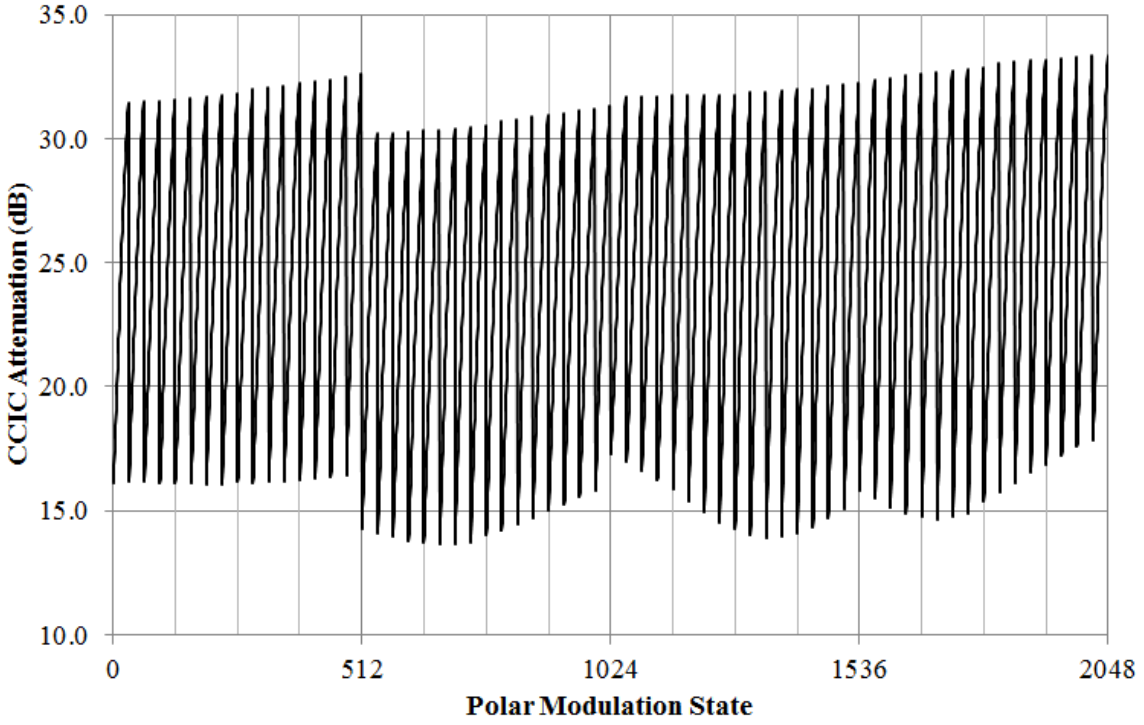

Fig. 58. Simulated CCIC Attenuation versus polar modulation step

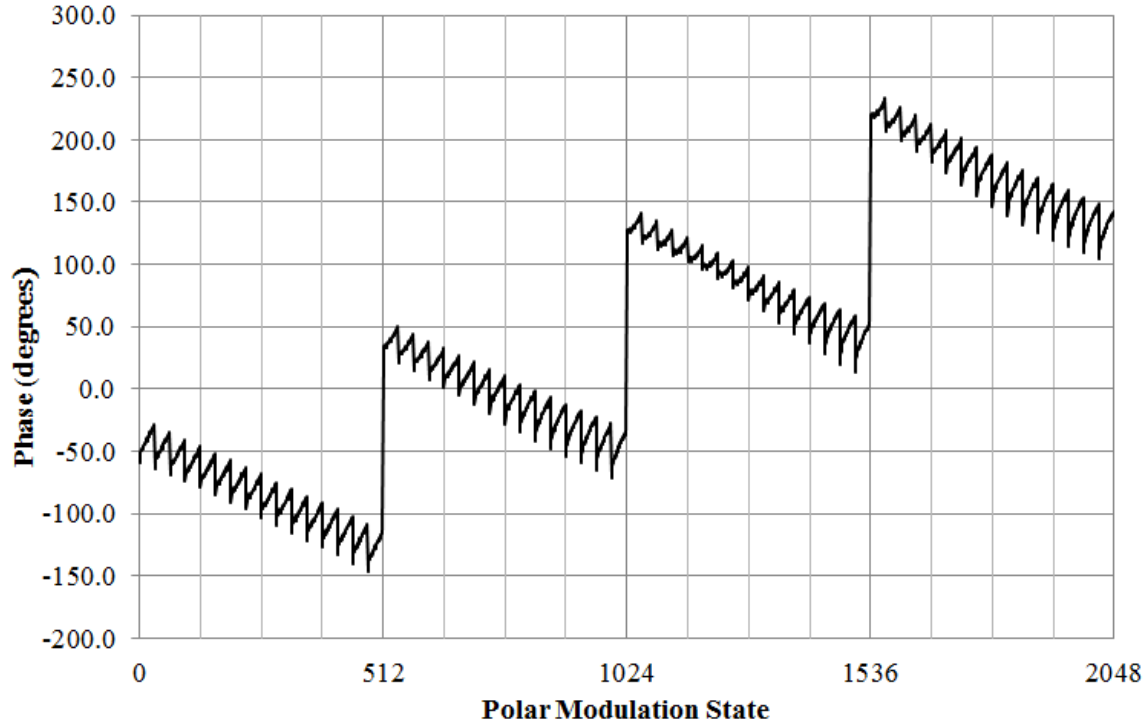

Fig. 59. Simulated CCIC phase shift performance over control state

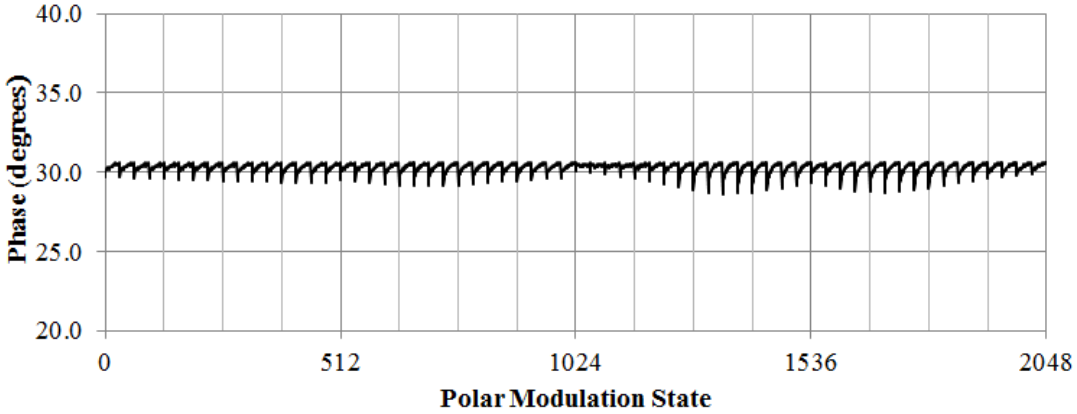

Fig. 60. Simulated LNA phase shift ($S_{21(deg)}$) versus polar modulator setting

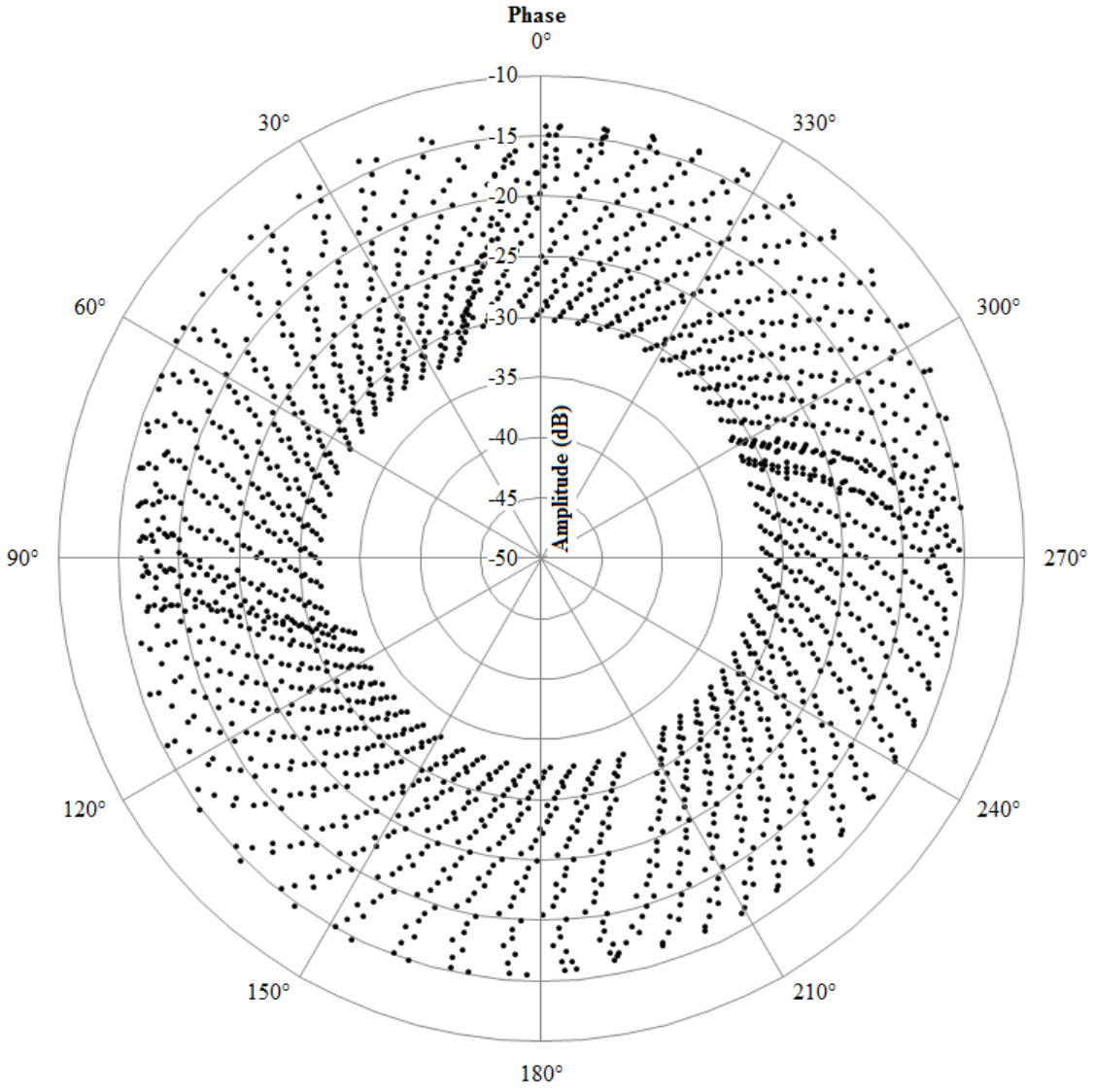

Fig. 61. Simulated CCIC polar coverage

In Fig. 57, the average noise figure at 2.35GHz is 1.37dB, with a minimum of 1.28dB and maximum of 1.52dB, meeting the 1.5dB NF specification. The NF_{MIN} averaged 0.97dB. The maximum variation between highest and lowest noise figure was 0.24dB.

The voltage gain (S_{21}) shown in Fig. 56 varied between 14.56dB and 14.84dB, for a variation of 0.28dB, with an average value of 14.77dB. The input return loss (S_{11}) varied between -1.39dB and -12.59dB, with an average value of -12.37dB. The output return loss (S_{22}) varied between -15.4dB and -16.75dB, with an average value of -16.16dB. The reverse isolation (S_{12}) varied between -26.71dB and -27.52dB, with an average value of -27.35dB. Overall, the results are consistent over all polar modulation states.

The CCIC attenuation in Fig. 58, which aims to be around -15dB at a minimum to total 25dB with a 10dB coupler, is almost achieved, with an average minimum value in each phase state of approximately 16dB. Unfortunately, the attenuation range when the system was assembled has been reduced from 22dB to an average of 16dB. At the time of tape out a solution had not been determined and it was decided to proceed with the reduced cancellation range. The tradeoff of range vs. resolution means that although the cancellation range has decreased, the amplitude resolution has improved, meaning the minimum cancellation will increase as a result.

The output phase shift has also changed after being assembled into the system, specifically in that the phase shifter over attenuation steps has increased. Ideally this value is zero. This will translate into twisting of the points in a polar plot, seen in Fig. 61. This is not a significant problem, as an algorithm can account for this when searching for

the ideal control word. The LNA phase shift in Fig. 60 is extremely consistent, varying only 2 degrees in its extremes.

The polar coverage of the CCIC is extensive, with the exception of the reduced amplitude range described above. There is overlap in phase, which is expected, and there are no large gaps in phase or amplitude. Therefore, it can be expected that signal cancellation will be comparable to the expected 24dB or better.

Chapter 7: Measured Results

This chapter will outline the measurement results obtained from the integrated circuits outlined in chapter 5. The measured results of the phase shifter prototype will be presented in section 7.1, followed by the results chip of the full CCIC system in section 7.2.

7.1 Phase Shifter Measured Results

The measured performance of the phase shifter chip in Fig. 45 was obtained with a vector network analyzer (VNA), signal generators, and power meters. The phase shift performance at 2.4GHz is shown in Fig. 62. The phase shifter achieves linear monotonic phase shift with an average phase step of 5.84° and a total phase range of 372°. S_{21}(dB) performance is shown in Fig. 63. S_{21} is fairly consistent, varying between -3.5 and -7.1dB at its extremes, or 5.3±1.8dB. The return loss performance is shown in Fig. 64. The phase shifter remains well matched at 2.4GHz over all phases at both the input and the output terminals. The frequency response for STEP=0 is shown in Fig. 65.

The phase shifter is well matched (< −10dB) in this state from 1.7GHz to 2.8GHz and has a pass band of 400MHz – 2.8GHz. The revised circuit in the CCIC tape out features wider RF lines in the top metal layer and higher Q inductors, obtained through EM planar simulation (EMX). The existance of this tool was unknown at the time of the design of the phase shifter. This alteration is aimed at improving the insertion loss of the phase shifter.

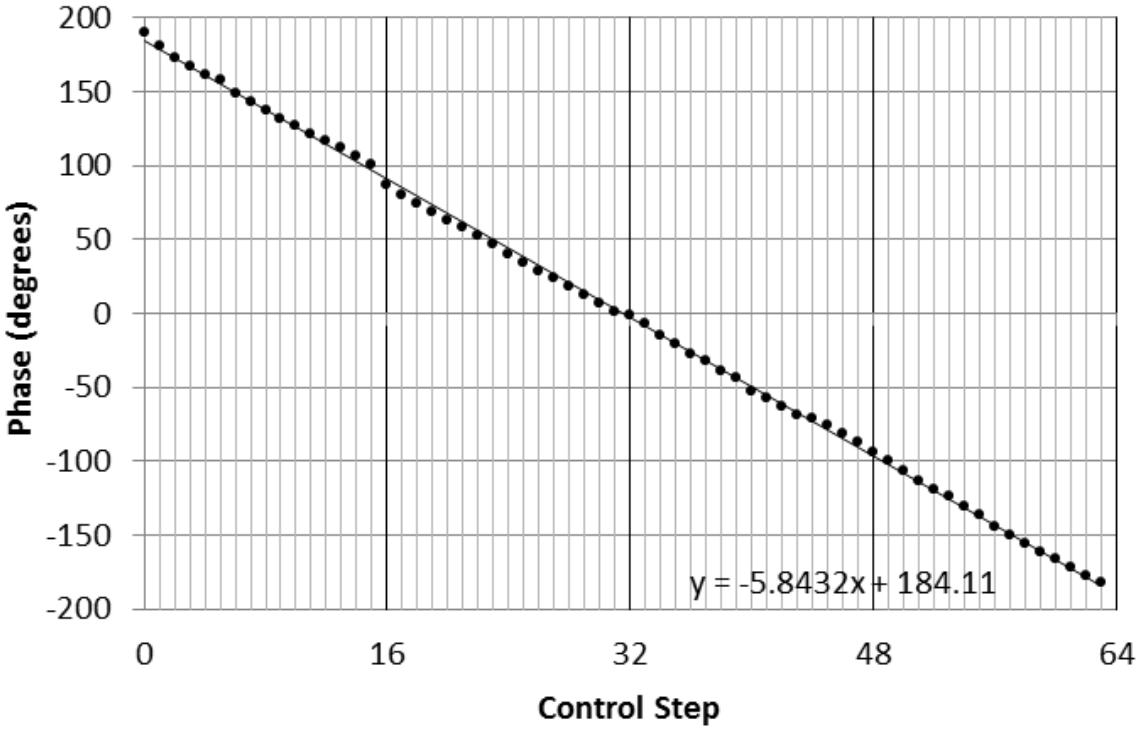

Fig. 62. The measured phase shift (S_{21} phase) vs. control step with trend-line

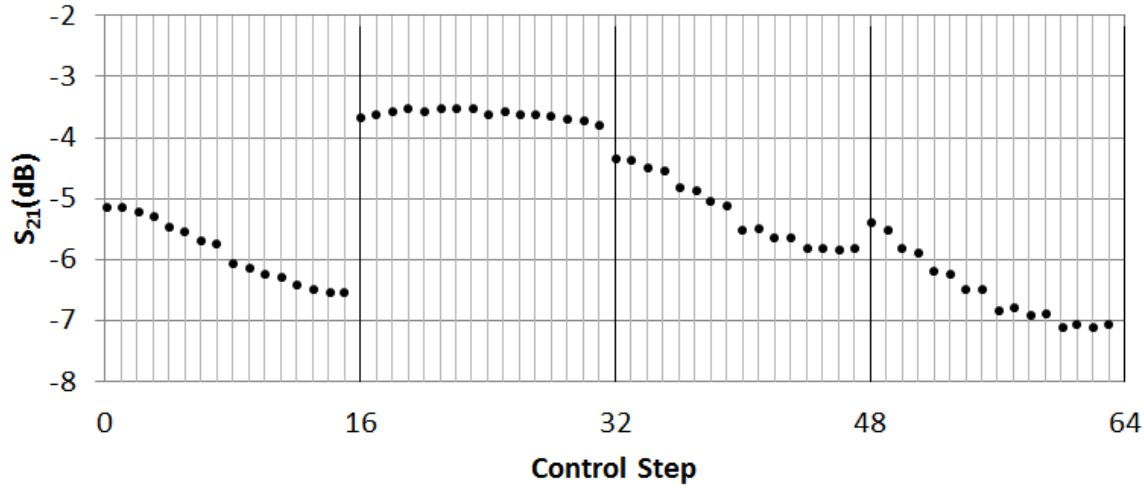

Fig. 63. The measured S_{21}(dB) performance vs. control step

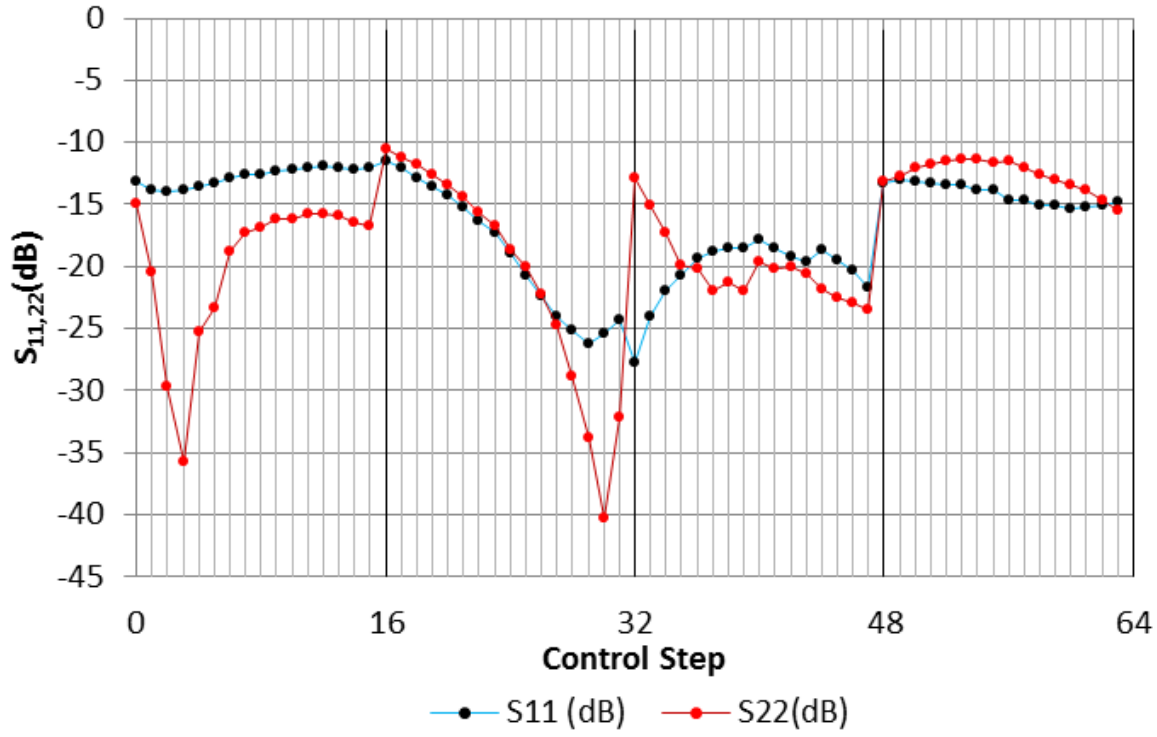

Fig. 64. The measured phase shifter return loss (dB) vs. control step

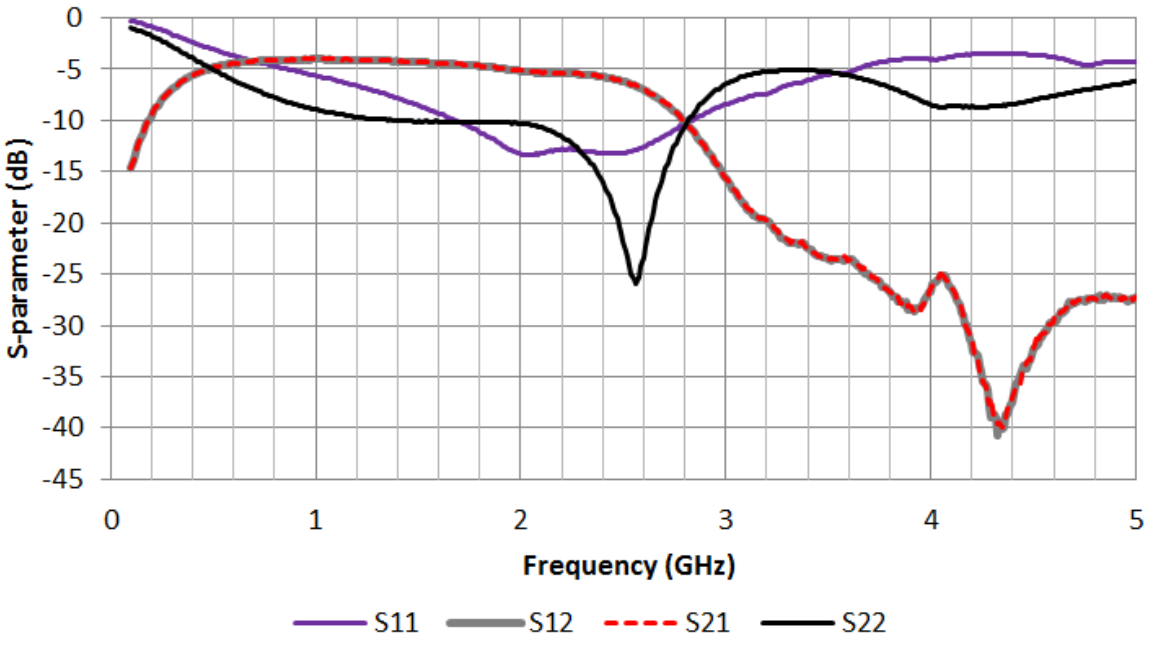

Fig. 65. The measured frequency response from 100MHz to 5GHz

The RMS phase error is shown in Fig. 66. This phase shifter was designed for accurate quadrants with less importance on quadrant to quadrant accuracy. As a result, the quadrant RMS phase error is also included. The RMS error of each quadrant ranges from 0.5^0 to 1.7^0 in each quadrant at 2.4GHz, with the full range having 3.6^0 RMS phase error at 2.5GHz. The phase shifter is effective over a range of 2.3-2.6GHz. Although the quadrant error remains low at 2.2GHz, the quadrants diverge significantly, contributing to a higher total RMS error.

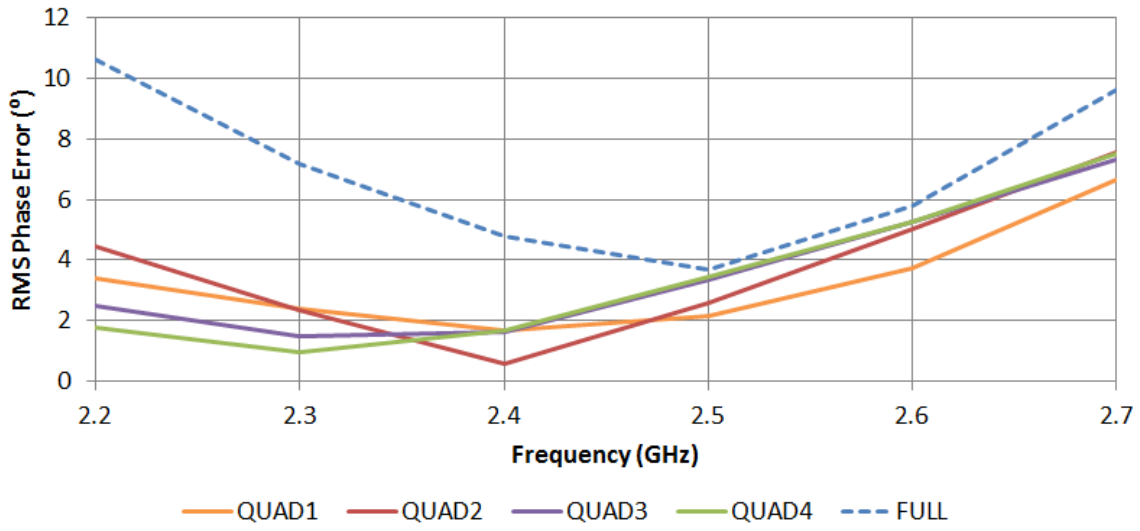

Fig. 66. The measured RMS phase error of each quadrant and over the full range

The power handling capability is shown in Fig. 67. The 1-dB compression point was measured with a signal generator and two power meters. The measured single tone 1-dB compression point is +23dBm.

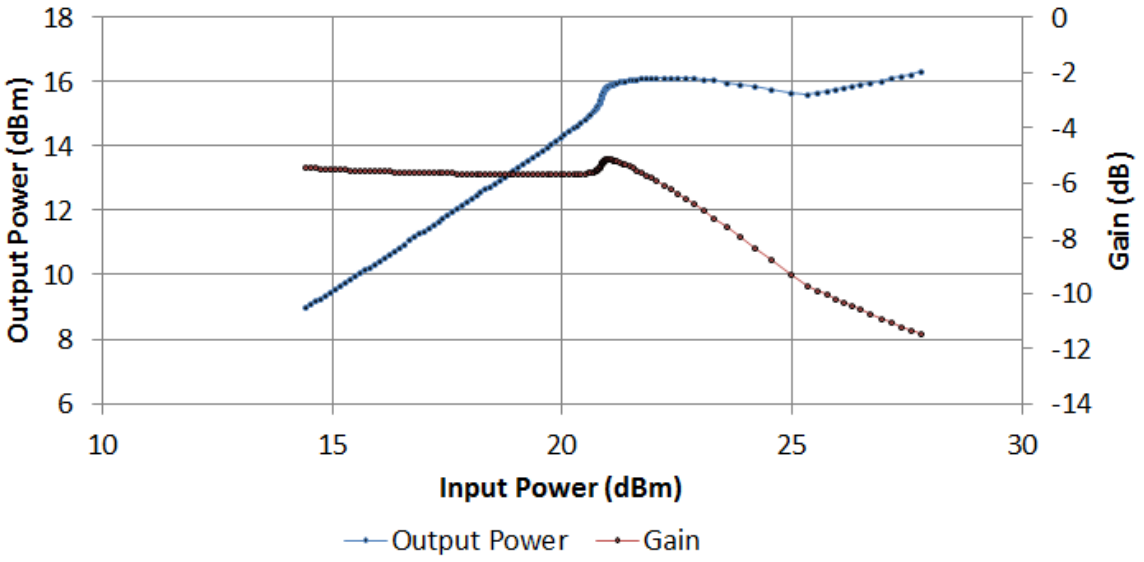

Fig. 67. Output power and gain versus input power at 2.4GHz

A comparison of this work to state of the art published works is found in TABLE III. The presented phase shifter has competitive but not state-of-the-art insertion loss. However, for all compared digital phase shifters, this work occupies nearly six times less area than the best of all works found and presents a significant advancement in area efficiency for passive digital phase shifters at 2.4GHz. When comparing to the most area efficient work in similar frequency ranges of at least 6 bits, [19] occupies the least area at 3.1mm^2. This is an approximate 600% improvement in area efficiency.

An extremely compact yet high performance 6-bit phase shifter has been designed. It offers performance comparable to other state of the art phase shifters yet occupies less than 20% of the area. This work presents a significant advancement in area efficiency while providing excellent matching and low insertion loss.

TABLE III: PHASE SHIFTER PERFORMANCE COMPARISON

	Freq. (GHz)	No. of Bits	Insertion Loss (dB)	Area (mm^2)	Technology
---	**2.4**	**6**	**5.3±1.8**	**0.47**	**130nm SOI CMOS**
[17]	2.5-3.2	6	13*	3.1*	180nm CMOS
[22]	1.4-2.4	6	3.8±0.4	3.8	0.5µm GaAs pHEMT
[21]	1.4-2.4	4	3.8±0.4	2.6	400nm GaAs
[20]	1.4-1.7	9	9.3±3.3	5.94	250nm SOS
[20]	1.8-2.4	10	5.1±2.2	3.4	250nm SOS

*Estimate taken from [18] based on die photograph in [17]

SOS = Silicon on Sapphire, pHEMT = p-High Electron Mobility Transistor

7.2 CCIC Measured Results

This section will outline the CCIC measured results obtained and compare them to simulation. For initial power-on comparison, on a 2.5V supply the measured current consumption was approximately 29.5mA. The simulated current consumption was 32mA, which is within a 10% difference and reasonable. The active components on the die are the LNA and the impedance buffer.

7.2.1 CCIC S-Parameter Performance

The small signal performance was measured using an Agilent N5230A vector network analyzer (VNA) and a custom Labview program written for this thesis. The Labview program was designed to automate the process of measuring 2048 control states. In short, the program measures the 3-port SP (Log magnitude and phase) data from the VNA, writes it to a Comma Separated Value (.csv), and then increment the hardware state. The Labview program writes the desired state to a National Instruments USB-6501 control box which then produces the 11-bit parallel output. The modified NI USB-6501

produced 3.3V, and a breadboard voltage divider circuit stepped down the voltage on each pin to 1.5V. An Agilent E3646 Dual Output DC power supply and an Agilent 33250A Function/Arbitrary waveform generator produced the 3.3V, 2.5V and 1.5V supply voltages required for the USB-6501 and CCIC respectively. The board set up is shown in Fig. 68. Each state took 13.7 seconds to measure, or approximately 8 hours for the full range.

The 2-port SP data over frequency are shown in Fig. 69, and the remaining five 3rd port SP data are shown in Fig. 70.

The measured 2-port SP data versus control state at the center frequency is shown in Fig. 71. This data is compared to the simulated SP data at the simulated center frequency (2.35GHz). The bold lines in Fig. 71 are measured data and the fine lines are the simulated data. The 3rd-port return loss (S_{33}) is shown in Fig. 72.

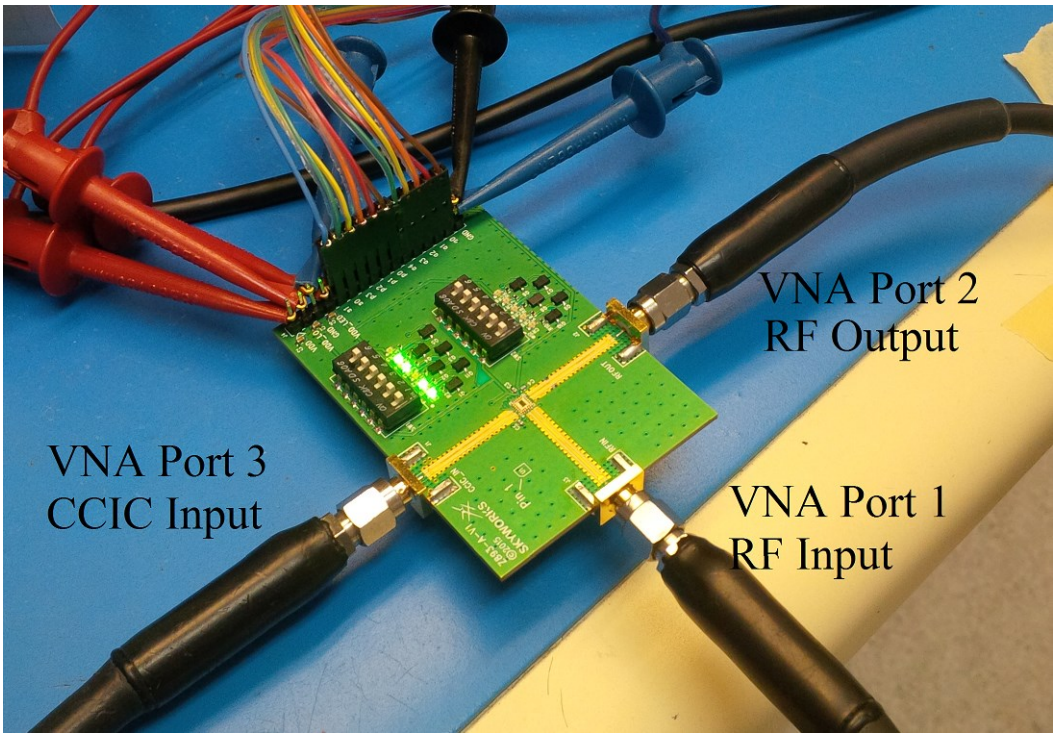

Fig. 68. S-Parameter measurement test board setup

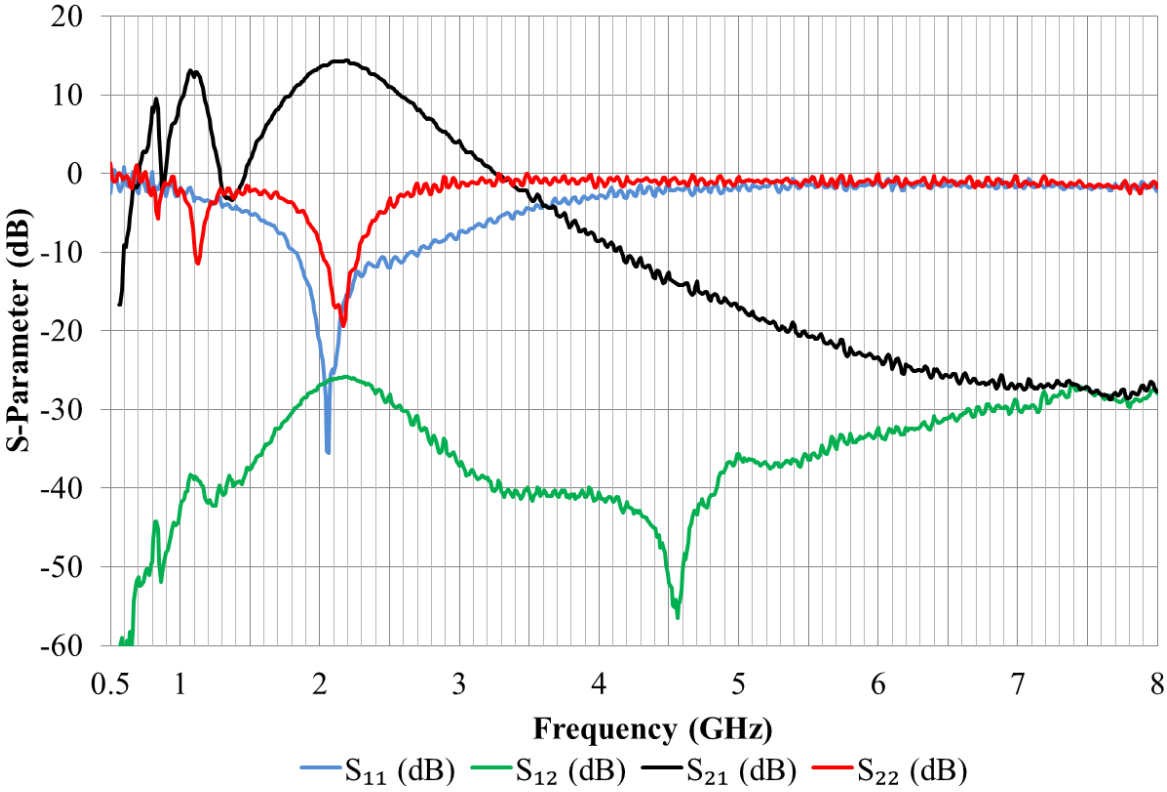

Fig. 69. Measured CCIC 2-port s-parameter results versus frequency

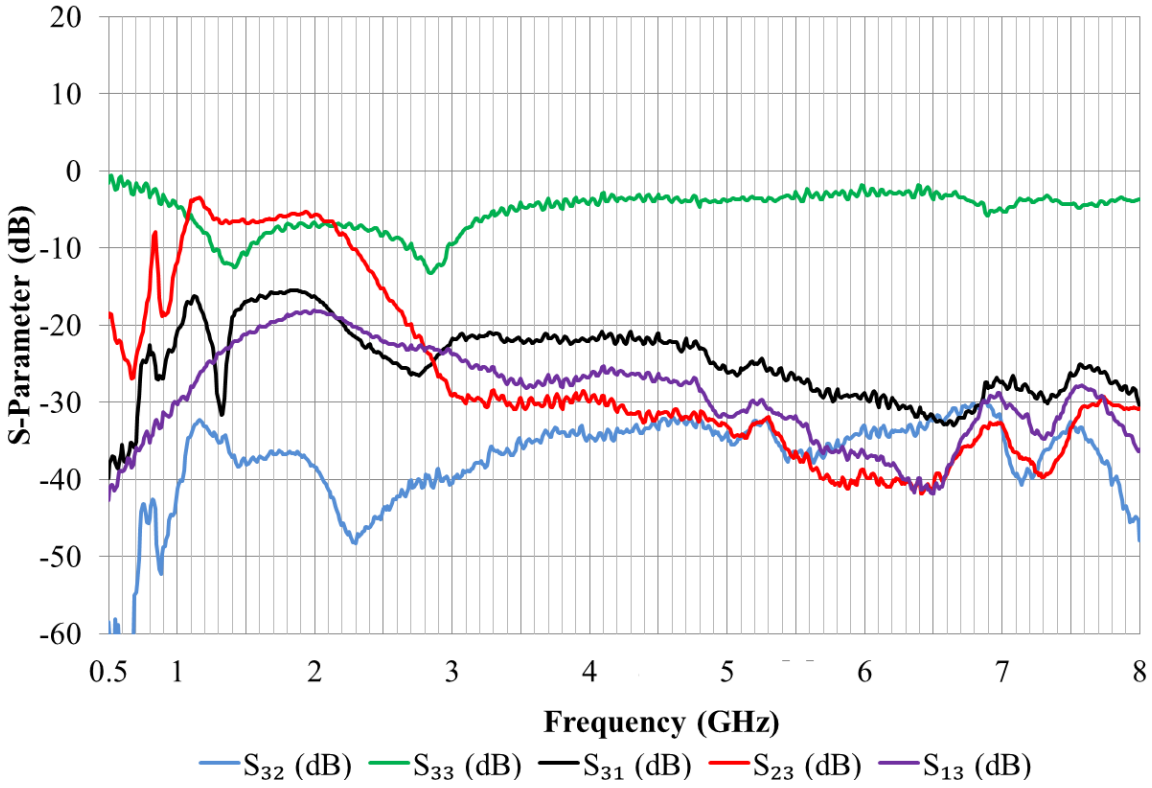

Fig. 70. Measured CCIC 3-port s-parameter results versus frequency

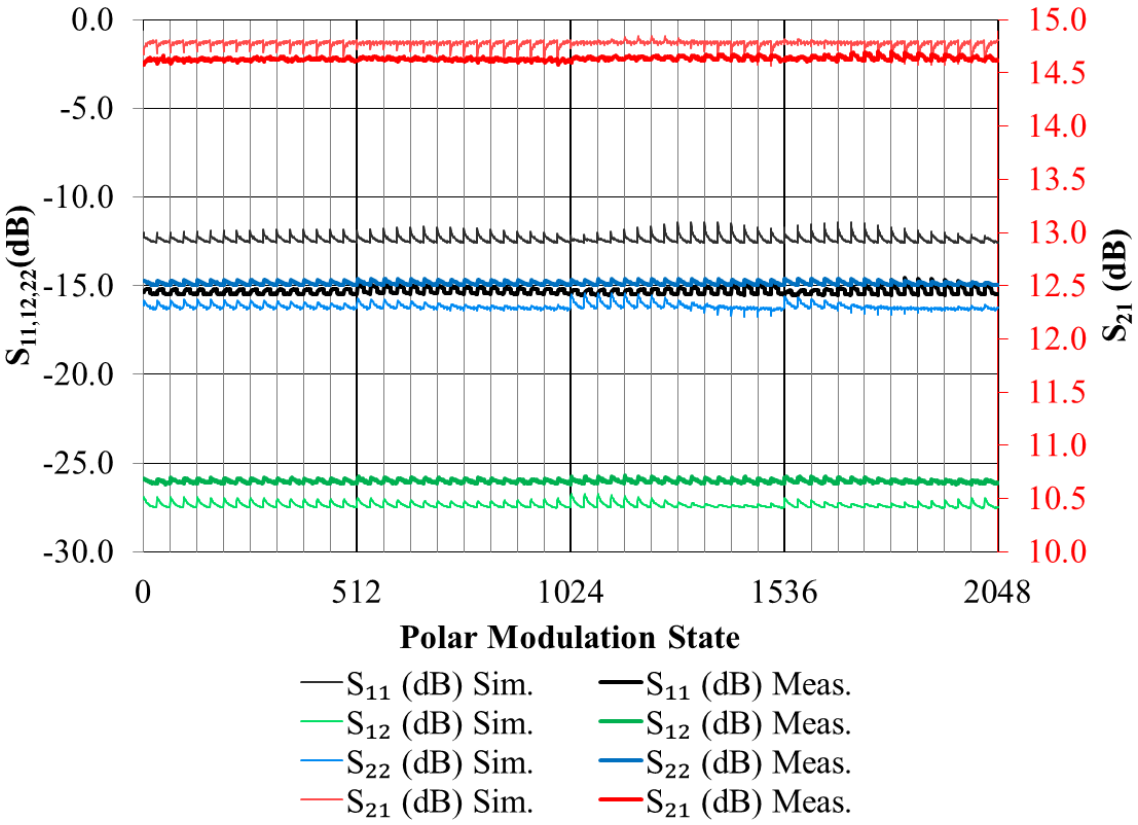

Fig. 71. Comparison of measured and simulated CCIC 2-port s-parameters

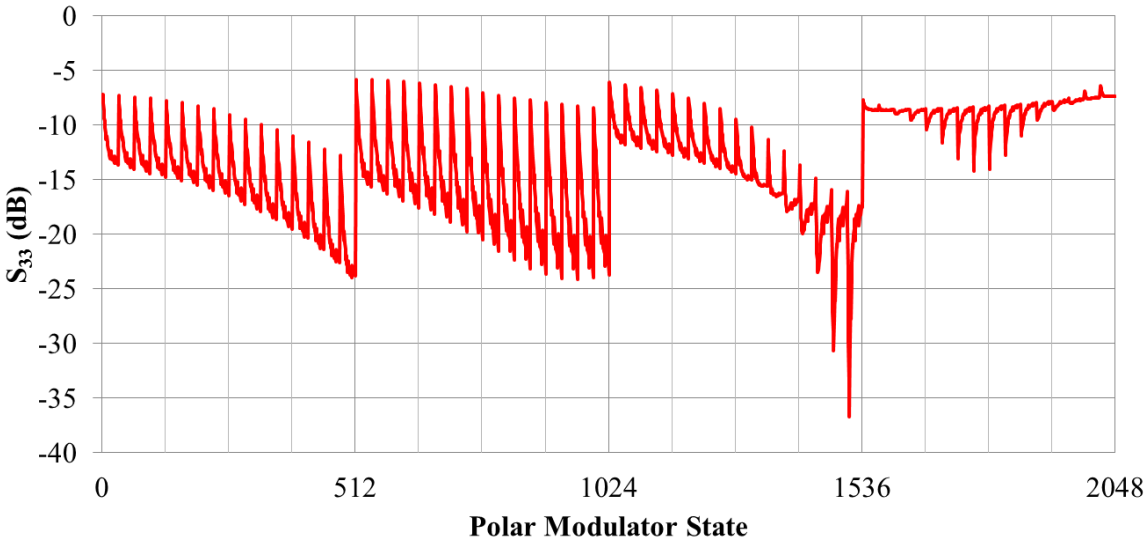

Fig. 72. Measured CCIC 3rd port return loss (S_{33})

The s-parameter performance holds up very well when accounting for the shifted 2.2GHz center frequency. The gain (S_{21}) had an average value of 14.61dB, varying from 14.53dB to 14.68dB at its extremes. The average simulated gain of 14.77dB is extremely

close to measured results. The reverse isolation (S_{12}) was also well predicted, yielding a measured -26.21dB average value compared to a simulated average of -27.35dB. The isolation varied from -25.23dB and -27.23dB. The input and output match were both acceptable at center frequency; S_{22} had an average value of -14.86dB compared to -16.16dB in simulation. S_{11} had an average value of -14.63dB compared to -12.37dB in simulation. Comparing the input and output return losses at the same frequency (2.35GHz), S_{11} had an average value of -11dB and S_{22} had an average value of -7.45dB. This is consistent with the shift down in frequency observed in S_{21}.

One issue that was not expected was gain produced near the subharmonic of the center frequency around 1.1GHz seen in Fig. 69. At the time of writing and after consultation with other designers, there was no immediate explanation for this gain. It is possible that the frequency is coincidental, but the most promising suggestion mentioned possible issues with RF decoupling. This issue was not replicated in simulation nor were there any simulated instability issues. Further exploration on this issue is required; however in a typical system filtering would eliminate any incoming signals near this frequency.

One other concern on the circuit performance was the poor third port match (S_{33}). In simulation over polar states the S_{33} match was not stellar; it reached −9dB at the maximum, however the measured match is further degraded with a maximum value of −6dB. The average value, however, was −13.54dB and minimum value was −36.7dB. The S_{33} match at low attenuation states was very poor, and the best matching occurred at the highest attenuation state, therefore in further designs the input circuitry (input to the quadrant shifter) could be better selected to provide for a better match as long as the

phase performance did not suffer. In this design, the match was sacrificed slightly in order to give preference to the quadrant phase performance.

The polar performance measurement of the full CCIC chip was made possible by a Labview program written to automate the 2048 VNA SP measurements. The measured coverage is found in Fig. 73 and a comparison to simulation is found in Fig. 74.

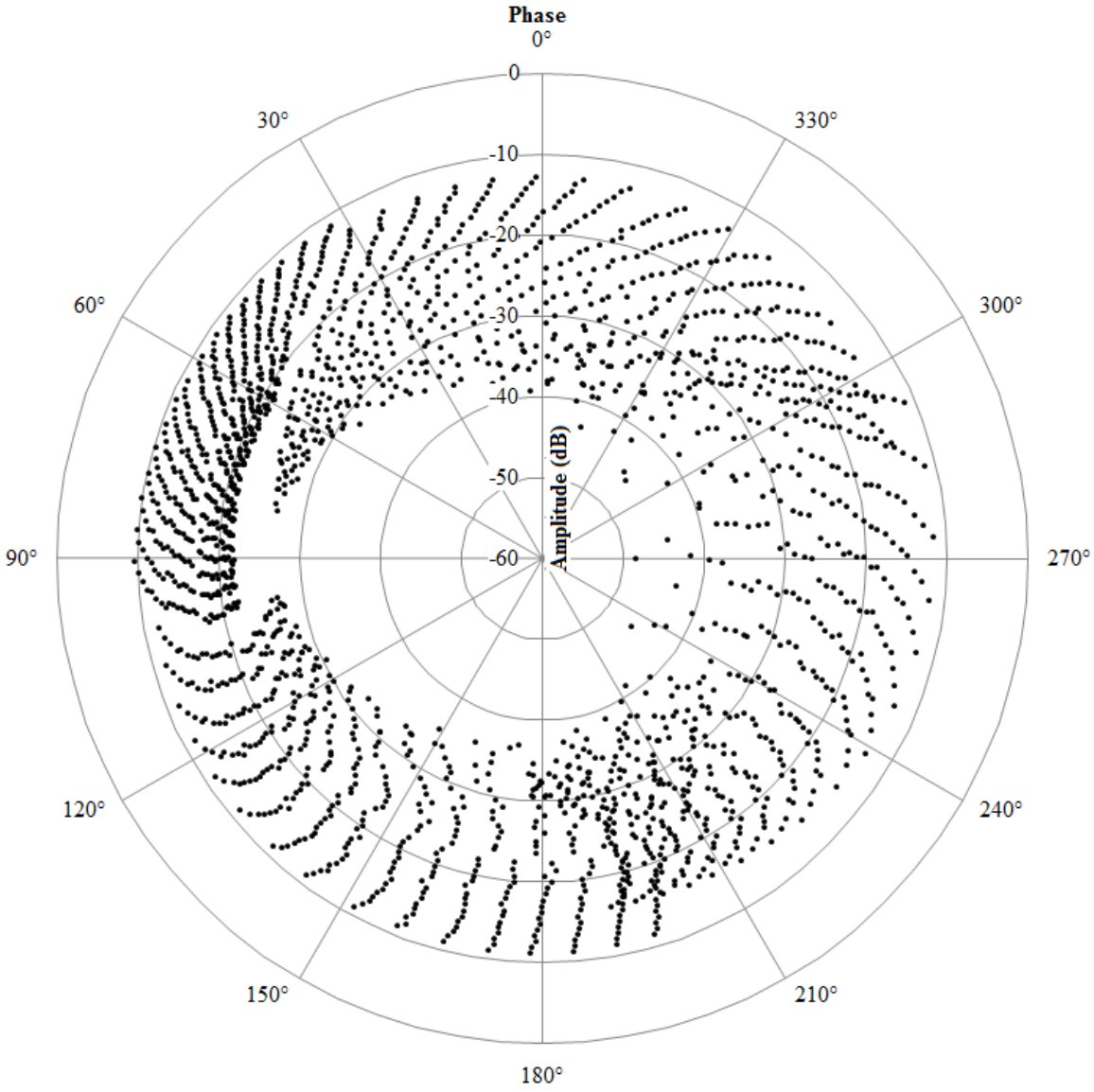

Fig. 73. Measured CCIC polar coverage at 2.4GHz

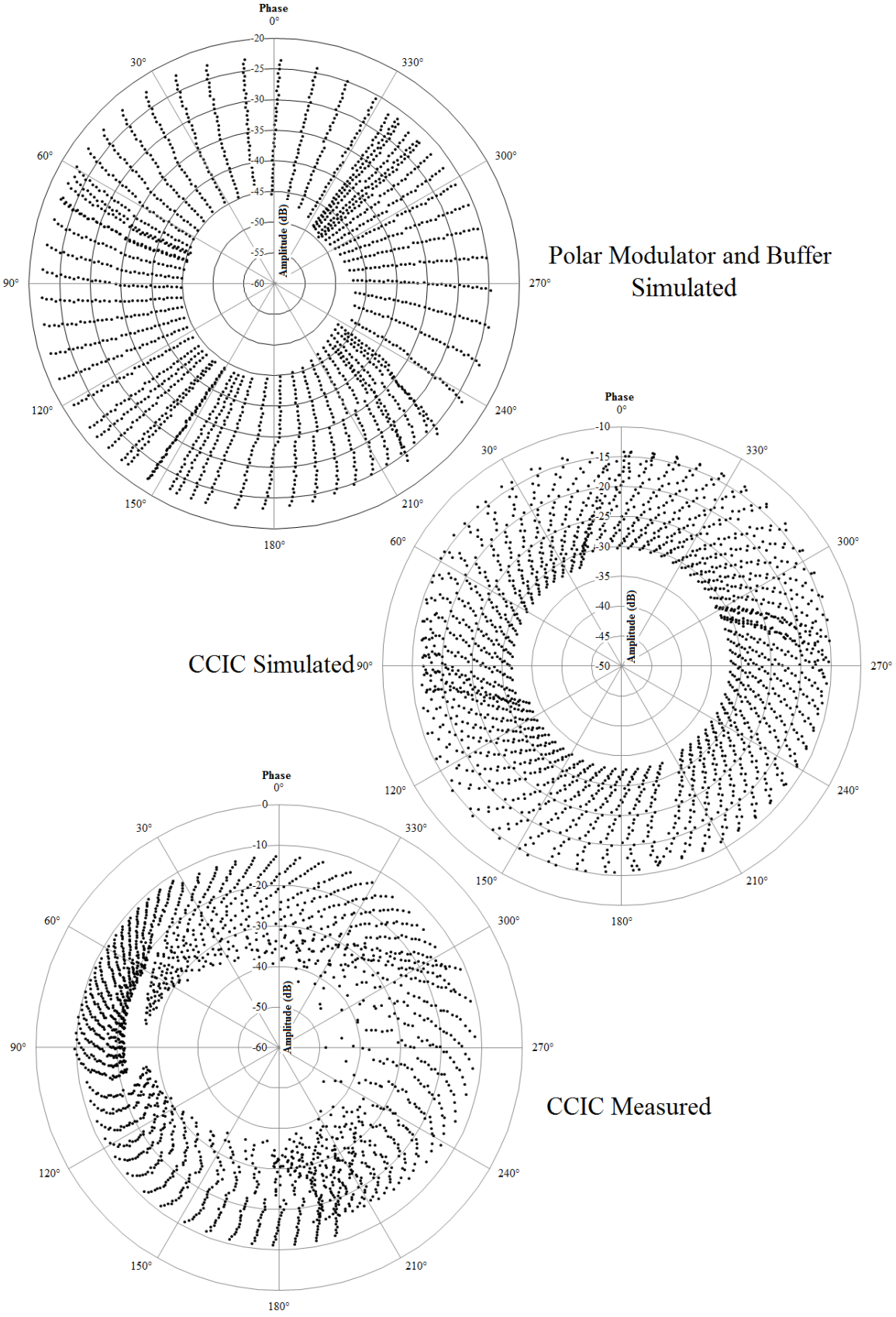

Fig. 74. Comparison of simulated and measured polar coverage

The polar coverage suffers in measurement slightly with an increased twist in the upper quadrant, increased attenuation range and high attenuation phase twist in the right quadrant, and a decreased attenuation range in the left quadrant. Given the complexity and ultra-compact nature of this device, however, the coverage is quite good. When comparing the system to the same chips as the phase shifter, the whole system, including phase shifter, at 0.78mm^2 is four times smaller than the smallest comparable phase shifter found (3.1mm^2).

There aren't significant disruptions to the pattern which a search algorithm cannot compensate for. The coverage discrepancies are notably quadrant based; therefore it is reasonable to suspect that the impedance interaction between the phase shifter and attenuator is affecting the attenuation range and attenuation based phase shift. A colour coded polar plot is shown in Fig. 75 to more clearly distinguish the quadrant performance.

The bypass state has the least twisting, which is understandable due to having the least reactive circuitry to be affected by a changing load. The left handed transmission line suffers from the most twist and largest attenuation range – it is possible that it could be tuned too close to the corner of its high pass response. The increased attenuation state may be pushing the response over the corner, thus increasing the attenuation from entering the stop band of the left handed transmission line.

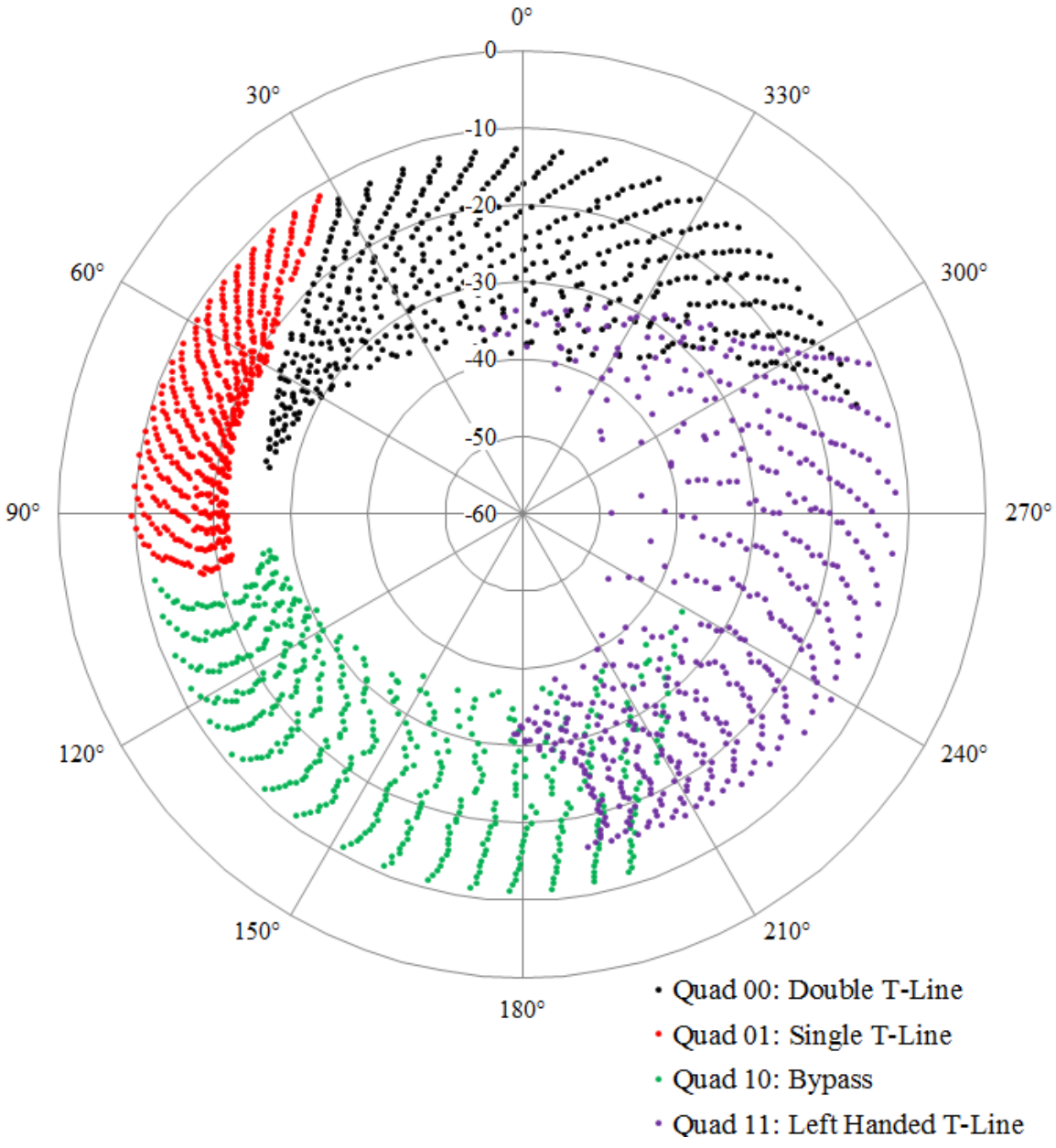

Fig. 75. Quadrant color coded polar coverage of measured CCIC

7.2.2 Noise Performance

The noise figure was measured using an HP Noise Figure Analyzer inside of a shielded enclosure to block exterior noise sources. The noise figure was measured for each state where one bit is high, and measured between 2.1GHz and 2.4GHz. The CCIC input port was terminated with a 50Ω load and the noise figure was measured from the LNA input to the output.

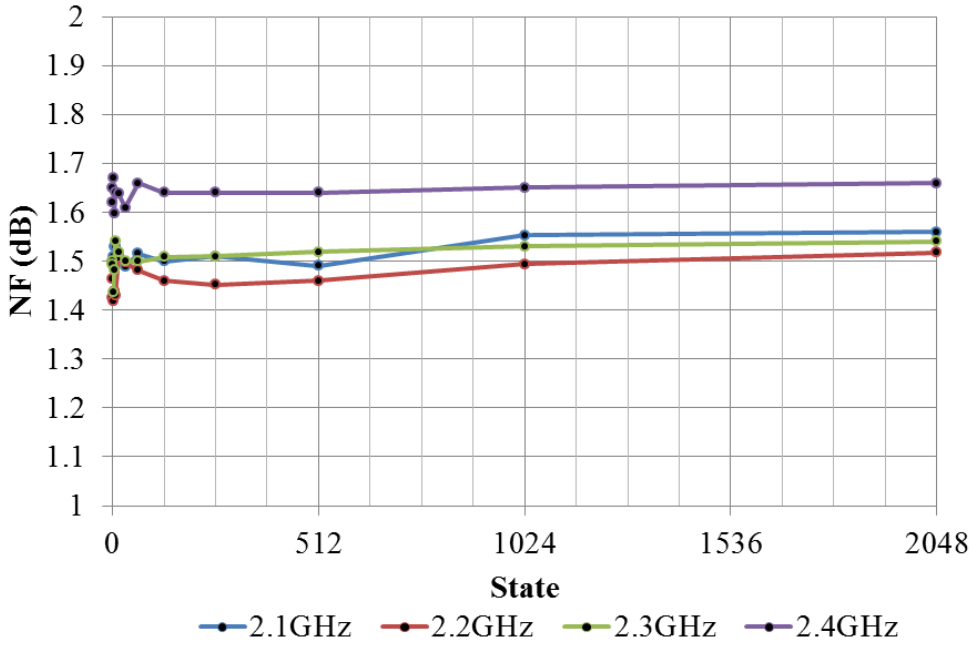

Fig. 76. Measured noise figure at 2.1GHz – 2.4GHz

The measured noise figure at 2.2GHz, near the measured center frequency, was between 1.42 and 1.52dB over the 12 states measured. These values are similar to simulated values, which has noise figures on average of 1.37dB. The noise figure tests were not automated so it was impractical to obtain the same thoroughness as the SP data. The measured noise figure states at 2.2GHz in Fig. 77 are compared directly to their simulated counterpart. For ease of comparison, the noise figure is shown versus the control bit that is currently high (or base-2 logarithmically) instead of raw state number.

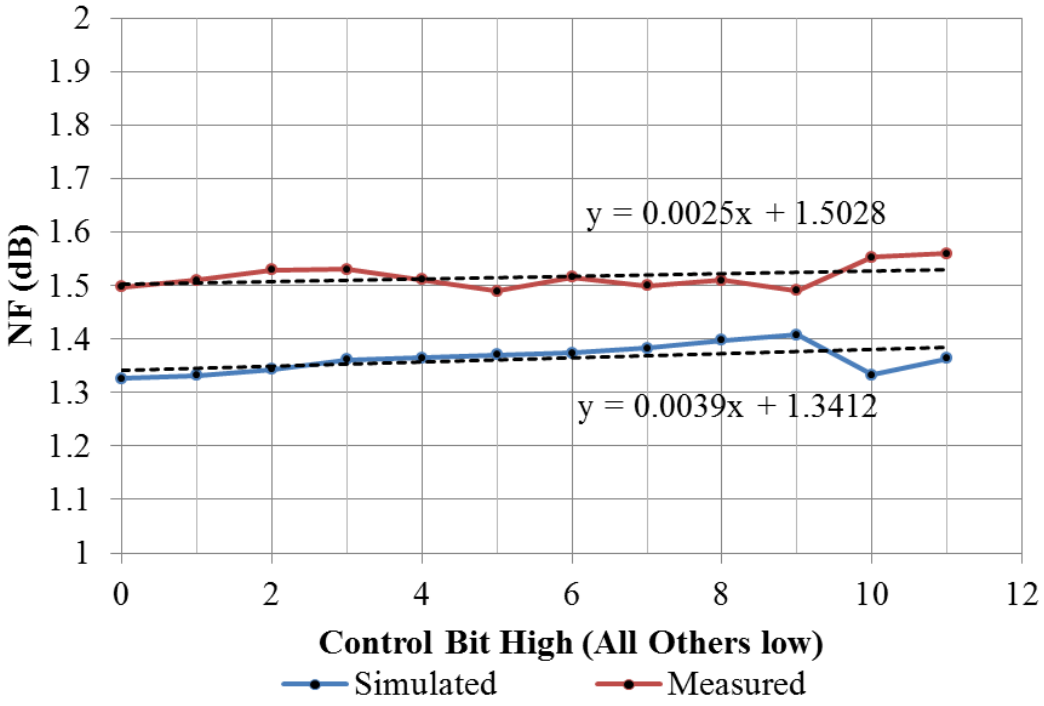

Fig. 77. Comparison of measured and simulated noise figure

On average, the measured noise figure is 0.15dB higher than in simulation but is a reasonably close comparison. Based on observations conducted at Skyworks using this technology, 0.15dB is a typical noise figure discrepancy compared to simulation. The average noise figure at 2.2GHz on is approximately 1.5dB.

7.2.3 CCIC Linearity

The 1-dB compression point (P_{1dB}) and input-referred third-order intercept point (IIP3) were measured using two Agilent signal generators (N5182A and E4438C), and two Rohde and Schwarz NRP power meters. The signal generators generated two tones for the IIP3 test, while a single tone was used to measure P_{1dB}. The power meter measured the input and output power levels at both the fundamental and IM3 frequencies. The linearity was measured in the same direction as the noise figure. The IIP3 was extrapolated from a -20dBm input power with a 2MHz delta frequency; this was also

compared to an extrapolation from each power level as well as the gain vs. input power to verify a 3:1 IM3 slope and a lack of gain compression. The fundamental and 3rd order intermodulation product (IM3) power for 2.2GHz is shown in Fig. 78 along with the extrapolated IP3 values. The IIP3 versus extrapolation point is shown in Fig. 79, and the IIP3 is compared to simulation for a number of control states in Fig. 80. The output power and gain versus input power to calculate the 1dB compression point at 2.2GHz is shown in Fig. 81.

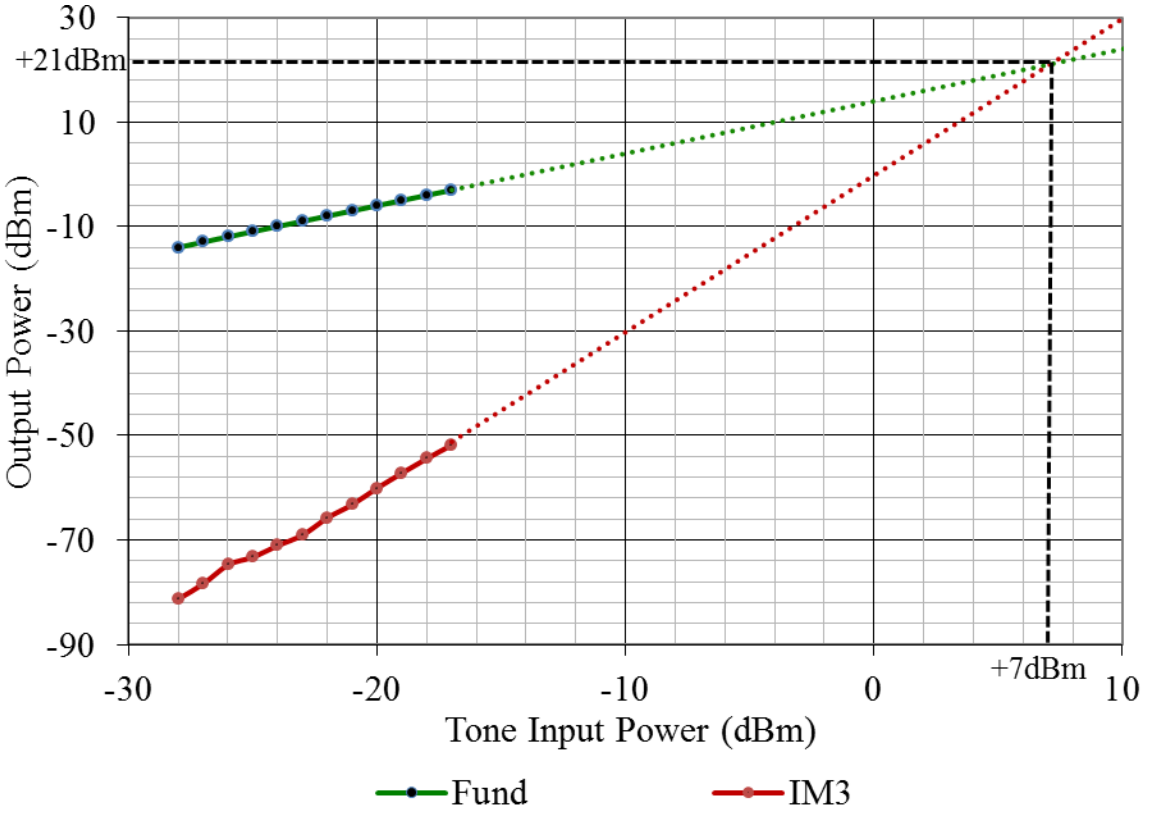

Fig. 78. Measured first and third order power levels versus P_{IN} with extrapolated IIP3

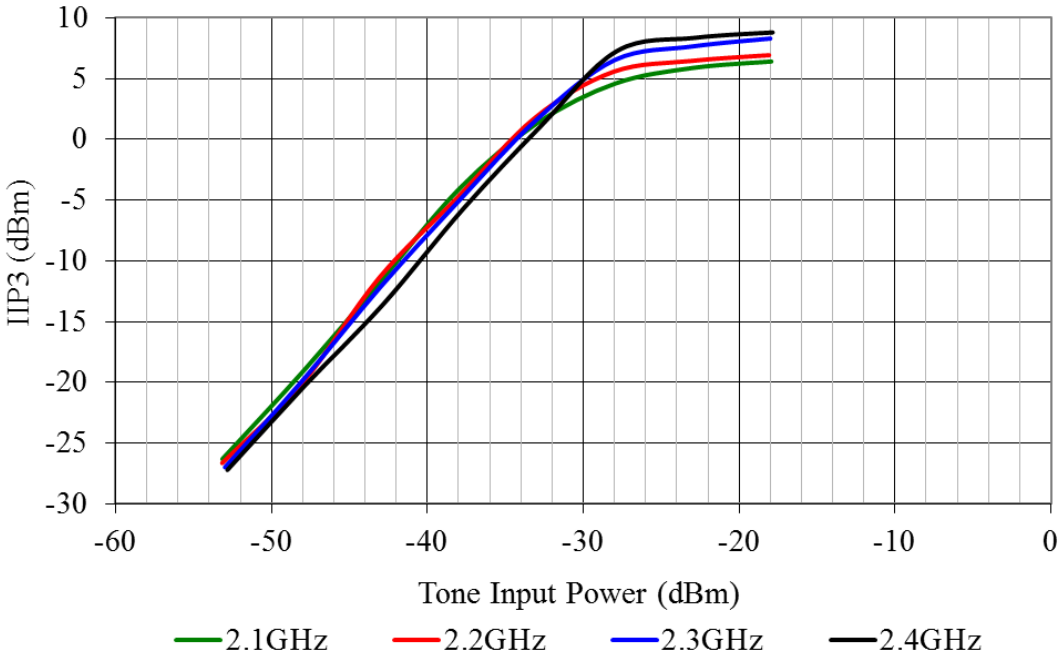

Fig. 79. IIP3 calculation versus input power extrapolation point at 2.1GHz – 2.4GHz

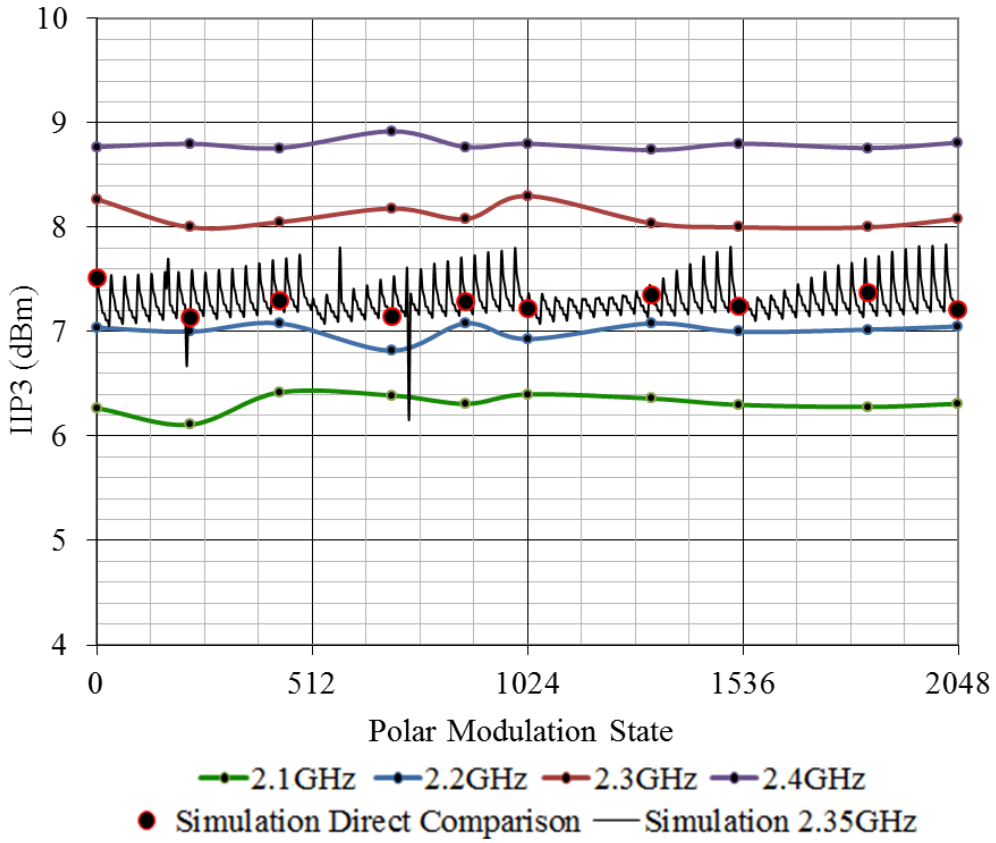

Fig. 80. Measured IIP3 versus control state compared to simulation

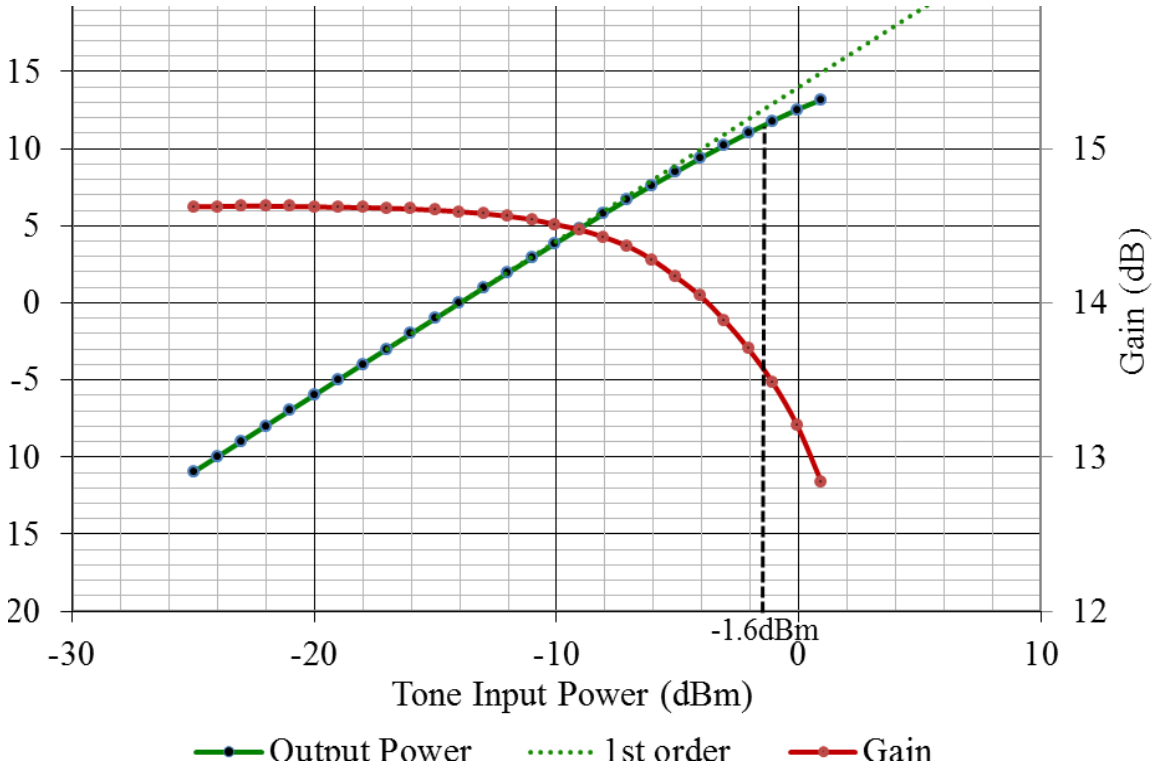

Fig. 81. Measured output power and gain with measured 1-dB compression point

The measured IIP3 at 2.2GHz was +7dBm as shown in Fig. 78, exceeding the +5dBm specification by 2dB. The extrapolation point used was −20dBm, and to demonstrate the appropriateness of this choice, Fig. 79 shows the IIP3 vs. extrapolation point. Before −30dBm input power, it can be seen that the calculated IIP3 decreases at nearly 20dB/decade, which is evidence for the IM3 product being near or below the noise floor of the measurement device. As the power level increases from −50dBm, the fundamental tone increases linearly, however the IM3 tone is being measured at the same value, with the difference in tones decreasing 10dB/decade instead of 30dB/decade as expected, resulting in a 20dB/decade increase in the calculated IIP3 until the IM3 tone fully emerges from the noise floor at approximately −25dBm.

The linearity of the CCIC agrees quite well with simulation. When comparing center frequency in simulation (2.35GHz) to center frequency in measurements

(2.2GHz), the agreement shown in Fig. 80 is considerable: measured results differ only by 0.27dB on average. The difference increases to an average 0.82dB and 1.51dB for 2.3GHz and 2.4GHz respectfully, however the decreased gain at those frequencies compared to simulation would account for an increased IP3.

The 1dB compression point in Fig. 81 was -1.6dB. The gain remains steady at approximately 14.6dB, with 0.1dB compression occurring at approximately −11.4dBm followed by 1dB compression at -1.6dB. The average 1dB compression point over the same control states from Fig. 80 at 2.2GHz was −1.97dBm. The average value at 2.1GHz was −2.1dBm, and at 2.3GHz and 2.4GHz the average values were −1dBm and −0.48dBm respectfully.

7.2.4 CCIC Cancellation Demonstration

To demonstrate signal cancellation, the CCIC demonstration board was connected with attenuation between the PA coupling port and the RF input to simulate air coupling. The PA output port on the board is an input from the Tx PA; in this test a signal generator is used. A power splitter was used to combine the coupled co-channel signal and the desired signal at the input of the CCIC. Two signal generators were used to create the co-channel (PA) and desired (Rx) signal, and a spectrum analyzer was connected to the output of the CCIC. The configuration is shown in Fig. 82.

For this test, a desired signal and co-channel signal co-exist at 2.412GHz and 2.392GHz respectfully. The output of the CCIC, uncalibrated, is shown in Fig. 83. The calibrated output is shown in Fig. 84. The uncalibrated phase shifter state is approximately 180^0 from the calibrated signal to facilitate easy demonstration. As a

result, the difference in amplitude is the cancellation + 6dB due to constructive voltage addition.

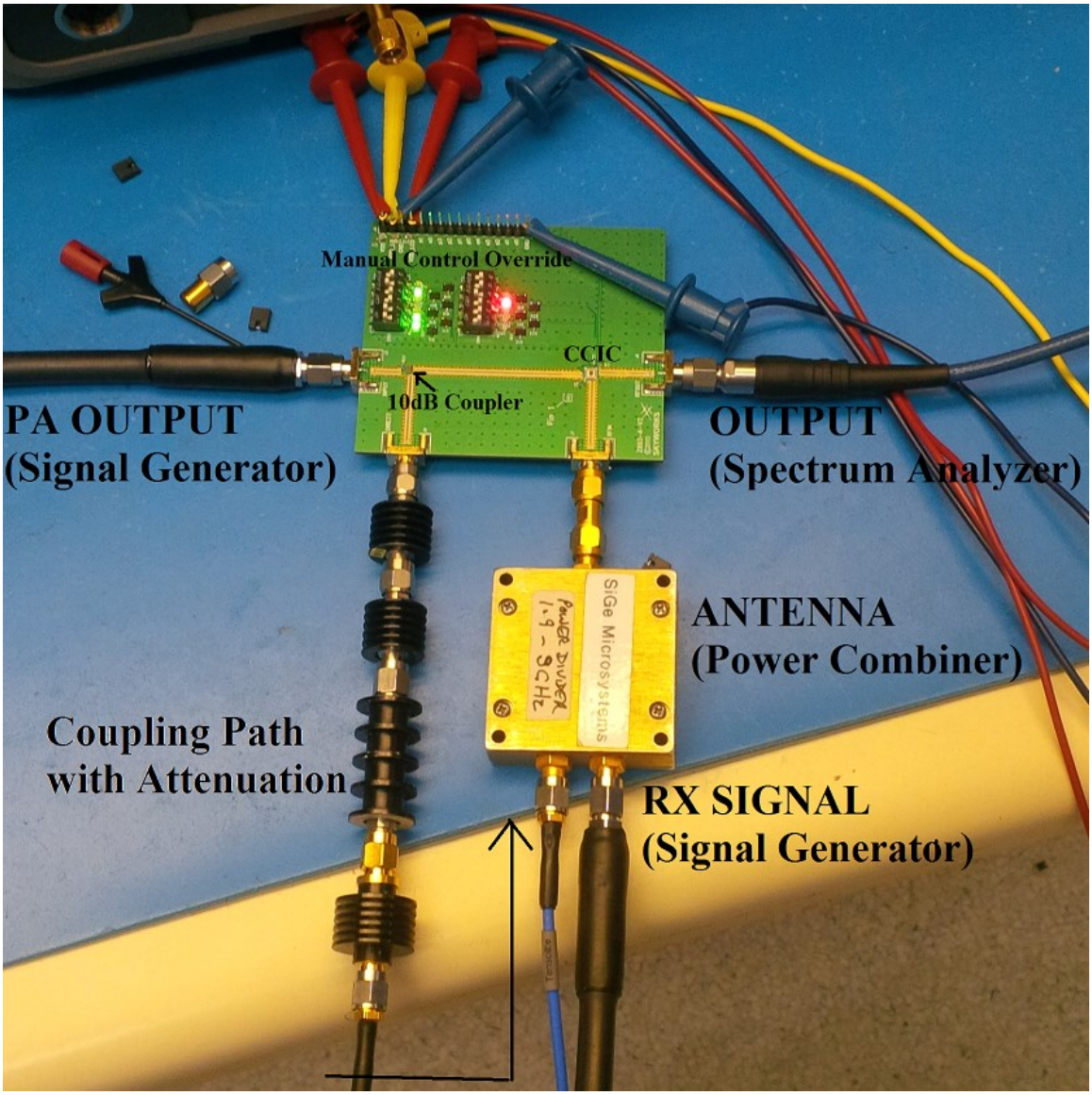

Fig. 82. Evaluation board test configuration for cancellation measurement

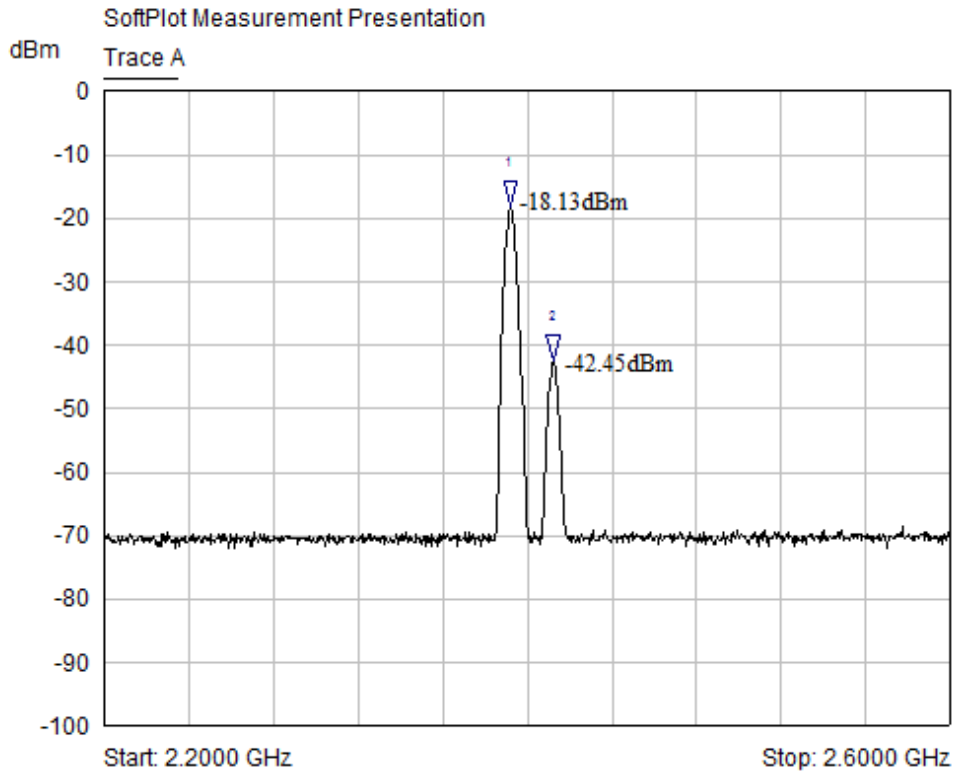

Fig. 83. CCIC measured output before calibration with strong blocking signal

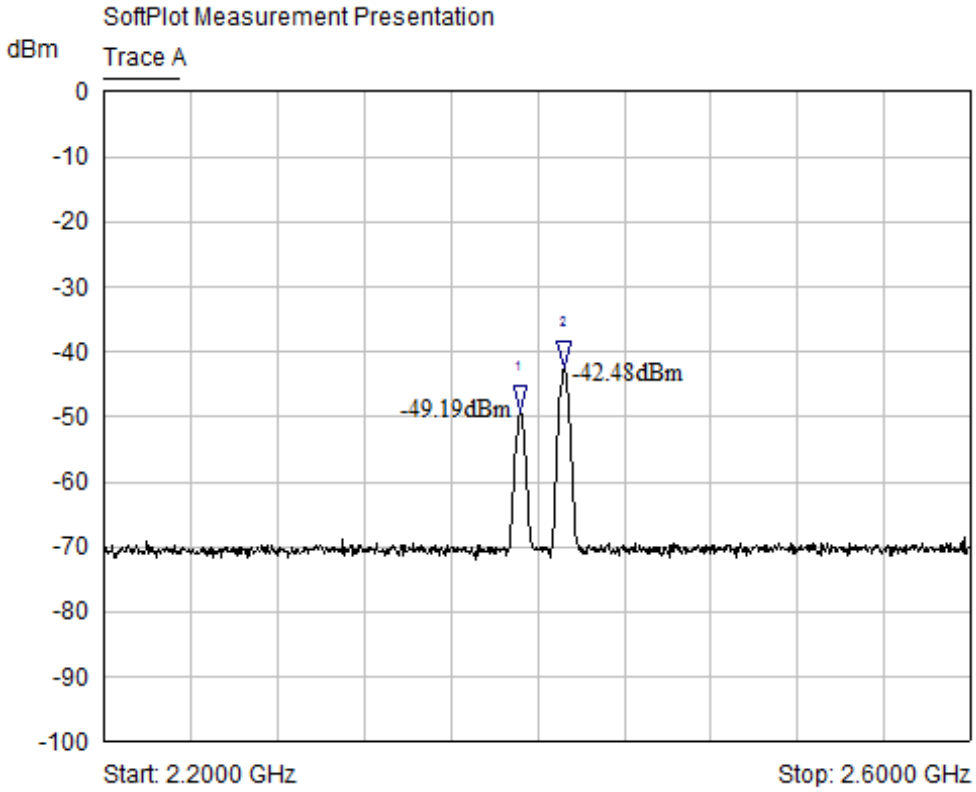

Fig. 84. CCIC measured output after calibration

The co-channel signal drops from -18.13dBm to -49.19dB after the system is calibrated for nullification. This produces a difference of 31dB or at least 25dB of cancellation assuming 6dB in-phase constructive addition. Additionally, the desired signal remains unchanged regardless of the frequency of the interferer. The system has successfully cancelled the co-channel interference to the degree expected.

The usefulness of any cancellation system in practice depends on the bandwidth over which cancellation meets the specification. Channel bandwidths can range from 5MHz – 20MHz in the LTE bands discussed in [1], and Wi-Fi 802.11b/g/n bands at 2.4GHz can be up to 40MHz wide [11]. The newest 802.11ac standard at 5GHz approved for use by the IEEE in 2014 can occupy bandwidths of up to 160MHz [20]. Therefore, the system must be capable of a cancellation bandwidth meeting the standard on which it will operate.

Two things are required for cancellation bandwidth: delay matching and circuit bandwidth. Delay, as discussed in Section 3.4, is required to ensure that different frequencies experience the same phase shift in both paths. If the delay error is zero, the only limitation is the circuit bandwidth. The evaluation set up from Fig. 82 was tested for cancellation over frequency with two different SMA cable lengths between the attenuators and power combiner to compare the 20dB cancellation bandwidth. The two shortest cables available were used, one approximately 20cm and one approximately 60cm. The measured group delays through these cables were 1.37ns and 4.42ns respectfully, a difference of 3.05ns. The delay was flat across the band.

In this test, a 2.25GHz interference signal was injected into the system. The system was calibrated to produce maximum cancellation for this signal and then the

interference frequency was swept to observe the change in amplitude over frequency. The resulting cancellation is shown in Fig. 85 with the longer cable on the left subplot and shorter cable on the right.

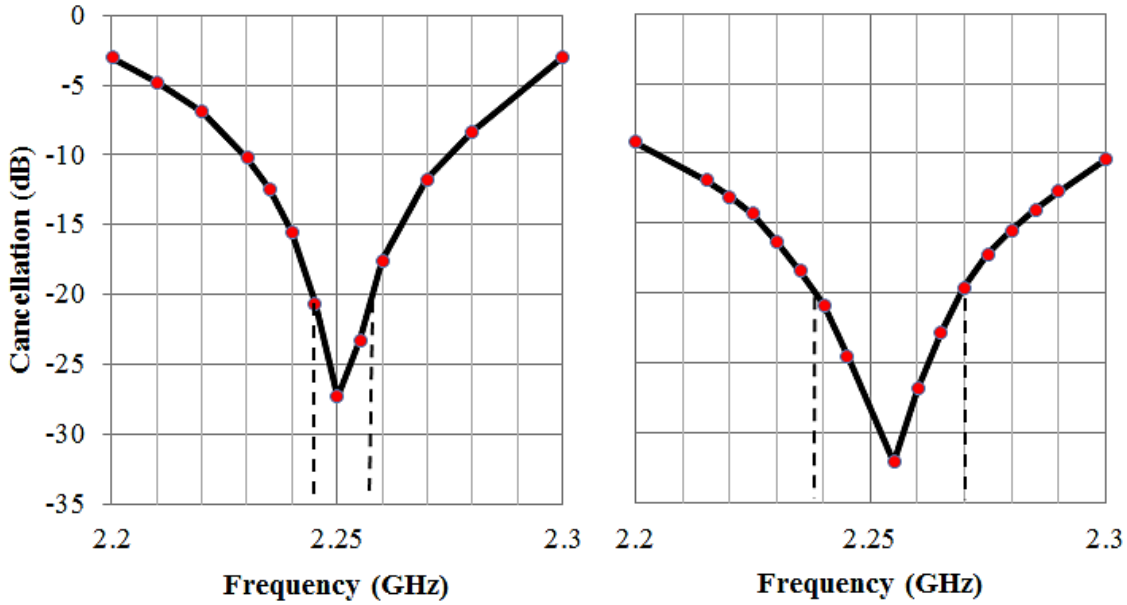

Fig. 85. Measured cancellation bandwidth with two simulated antenna delays

With only two short SMA cables available, the delays cannot be precisely matched, however the change in bandwidth with a change in delay can be observed with these two tests. Using the longer SMA cable, which simulates a larger delay through the antenna coupling path, the 20dB cancellation bandwidth was approximately 14MHz. The shorter SMA cable, conversely, had approximately 31MHz of cancellation bandwidth. Therefore, it can be concluded at this point that the measured circuit 20dB cancellation bandwidth is at least 31MHz. In a real product, extensive effort would be undertaken to match the delays as closely as possible with adjustability in order to counteract environmental delay changes; however this was not a focus in this experiment.

In order to infer the circuit bandwidth to determine its suitability for the Wi-Fi and LTE standards chosen, the group delays between the three ports can be calculated from existing SP data. This can be done using the slope of the phase over frequency:

$$Group\ Delay = -\frac{\Delta\theta}{\Delta\omega} \tag{28}$$

The phase response was measured on the 3-port test board in order to isolate the response of the chip from the system which includes a coupler in the 4-port board. The group delays of the Rx path (S_{21}) and the CCIC path (S_{23}) are shown below in Fig. 86.

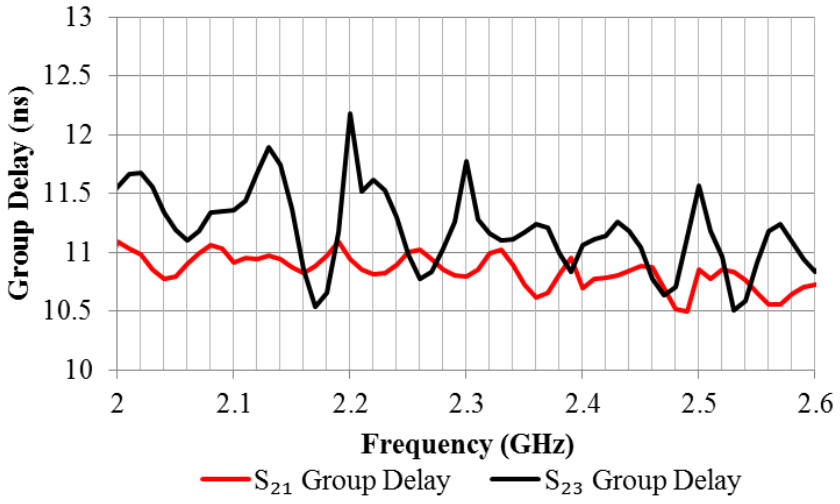

Fig. 86. Measured group delays of the R_X and CCIC paths

The delays differ quite a bit from each other; in order to observe meaningful delay information, the difference between the two, $d_\Delta(f)$, is shown in Fig. 87.

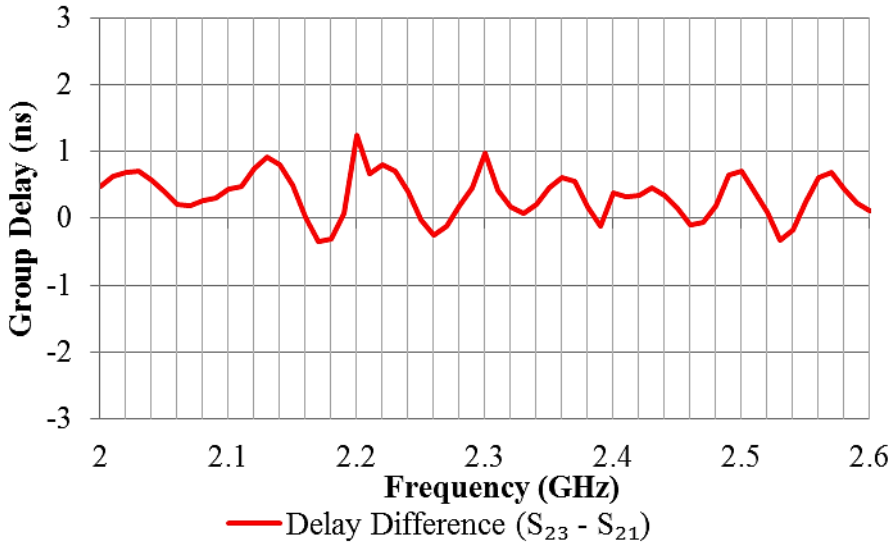

Fig. 87. Measured group delay difference ($d_\Delta(f)$) between R_x and CCIC paths

The group delay difference over frequency is a characteristic which represents the CCIC ability to cancel over frequency. This information can be used with (1) to infer the cancellation versus frequency with matched delays. The group delay variation over frequency in Fig. 87 illustrates why the total delay error cannot truly be made zero: the path delay error can be made near zero; however the circuit's frequency response dominates by introducing group delay variations. If the path delay error were zero, then d in (1) could be replaced with the group delay difference $d_\Delta(f)$ found in Fig. 87 in order to observe the path delay matched CCIC cancellation bandwidth. This is shown in Fig. 88.

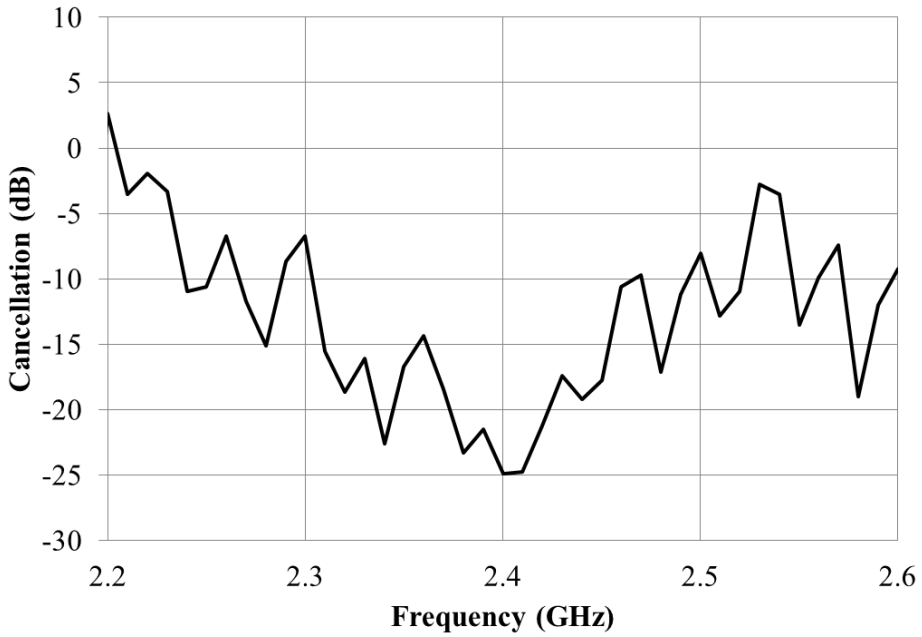

Fig. 88. Inferred delay matched cancellation versus frequency (a=0.97, b=2.8)

With delay error originating from the circuit group delay characteristics alone, the 20dB cancellation bandwidth when tuned at 2.4GHz is approximately 50MHz. The 15dB cancellation bandwidth is approximately 150MHz. It would be useful for future work to obtain higher resolution SP data to more precisely determine group delay and projected cancellation. Based on the above tests, however, the system would be suitable for greater than 20dB of cancellation for Wi-Fi (802.11b/g/n) and LTE (bands 7, 30, 40, and 41) if the system delays were reasonably matched. These standards have maximum bandwidths of 40MHz and 20MHz respectfully.

The delay and polar errors can be inferred by comparing the measured cancellation from Fig. 85 to the cancellation characteristic in Fig. 88 with an additional path loss added. By matching the measured response to the inferred response, the delay and polar errors can be estimated. The shorter path delay results from Fig. 85 were

matched to the inferred cancellation in Fig. 89 and the longer path delay results are matched in Fig. 90.

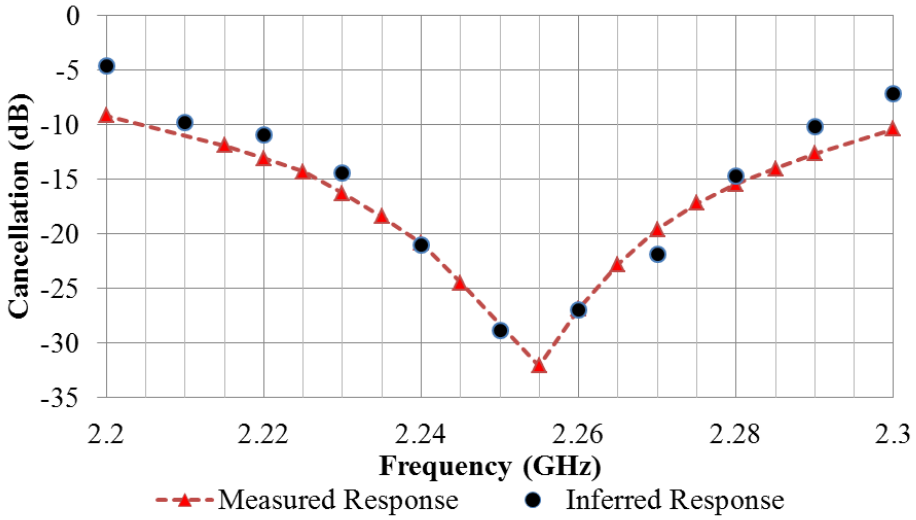

Fig. 89. Measured and inferred cancellation response for shorter path delay

The parameters from (1) used in Fig. 89 are: $a = 0.99$; $b = 2^0$; $d_p = -0.1$ns where d_p is the path delay error added to the group delay difference $d_\Delta(f)$, and where delay error $d = d_p + d_\Delta(f)$.

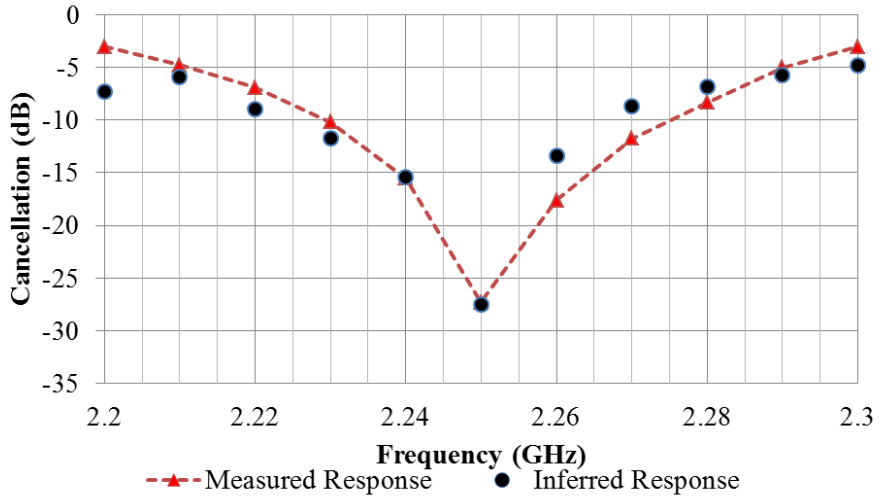

Fig. 90. Measured and inferred cancellation response for longer path delay

The parameters from (1) used in Fig. 90 are: $a = 0.97$; $b = 1.7$; $d_p = 2.9$ns

Note that the phase and amplitude error is underdetermined; the response can be replicated by improving one variable and degrading the other as cancellation is a 2 dimensional balance of both phase and amplitude as discussed in Section 3.3. As a result, the amplitude error *a* and phase error *b* from Fig. 89 and Fig. 90 are only one solution.

An interesting result from Fig. 89 and Fig. 90 is the difference in delay errors needed to replicate the measured results. The difference in delay errors used in Fig. 89 and Fig. 90 was 3ns. This compares extremely closely to the measured delay difference between the cables of 3.05ns. Therefore this serves as a verification of results given that the prediction difference aligned with the measured delay difference. There is more work to be done assessing the bandwidth potential of the CCIC, however the circuit would be extremely capable with narrowband channels (5, 10, 20MHz), and if delay matching were accomplished the circuit should be suitable for 40MHz 802.11b/g/n operation.

The CCIC has successfully achieved most of its specifications; it has achieved a 1.5dB NF, greater than +5dBm IIP3, 14dB gain LNA with greater than 25dB of co-channel interference cancellation capability. The receive chain is well matched at the input and output, however the center frequency was slightly lower than expected at 2.2GHz instead of 2.35GHz. The circuit was extremely compact at 0.78mm^2 due to novel circuit architectures.

Chapter 8: Future Work and Conclusion

8.1 Future Work: Current Hardware

There has been a lot of effort exploring the viability of this chip, however there is still more to be done to better understand the system and its limitations. The system cancellation on the 4-port testing board proved that the system can cancel co-channel interference regardless of its frequency; however the coupling is simulated with attenuators and SMA cables. To take it a step further, antennas could be used, or optionally an SMA cable cut in half with stripped insulation would simulate leakage coupling. Further to the delay discussion from the previous section, it would be very useful to measure the exact cancellation bandwidth from the circuit without delay error, but this would require an external tunable delay. It has been inferred that the 20dB cancellation bandwidth should be able to reach 50MHz from the measured group delay characteristic, and this was corroborated by comparing the prediction to two sets of measured results by comparing the required delay to match them. However, this has not been measured due to lack of equipment. Future work would be well spent here.

The polar constellation concerns from Chapter 7 should be further examined as well. The tradeoff to the ultra-compact nature of the quadrant shifter is that it utilized the opposite handed transmission line for one of the states. As a result, any shift in component parameter will have the right and left handed states shift in opposite directions. Therefore, additional study needs to be done here to determine if there is a way to mitigate this effectively to ensure proper tuning relative to each other.

The gain at 1.1GHz does not have a concrete explanation at this time, therefore this also needs further investigating to determine if this is related to a PCB issue or if it is

an issue on the chip itself. There is no semblance of this gain in simulation; therefore experimentation on the current hardware could shed more light on this issue.

8.2 Future Work: Future Hardware

This proof of concept has been a success; however there are many avenues one could pursue to improve performance with future revisions on the design. One avenue that has been pursued is the feasibility of a higher resolution phase shifter. By expanding on the high-ratio capacitors, it may be possible to reliably generate smaller capacitance steps while maintaining a passive architecture. This can be possibly achieved by stacking unit capacitors in series to divide down the capacitance at the expense of area. The caveat here is that while a finer phase resolution may be possible, smaller passive attenuation steps becomes exceedingly more challenging below 0.7dB. Doubling the resolution to 0.35dB may be achievable using traditional means pursued in this thesis, but beyond would be extremely challenging due to the precise ohm-resistances required. Further innovations may be required to reliably create centibel resolution attenuation steps.

Should this be achievable, however, these techniques could lend themselves to full duplex operation. It was demonstrated that this technology is unaffected by the relation of receive frequency to interferer frequency; if one has access to the signal, it can be cancelled while leaving the desired signal alone. As the research in Chapter 2 shows, however, RF cancellation alone may only go so far in achieving perfect full duplex operation on chip.

In addition to resolution enhancement, on-chip delay matching would be needed for any commercial CCIC application. The co-channel delay between Tx and Rx depends on the environment which can change. As a result, the bandwidth of cancellation will be

inconsistent. To maintain satisfactory cancellation bandwidth, a delay calibration circuit will be required. As found with the cancellation bandwidth experiments in Chapter 7, the current implementation would be suitable for 802.11b/g/n Wi-Fi and LTE co-channel applications whose maximum bandwidth is 40MHz. Future hardware should pay particular focus to the delay characteristic of the circuit to attempt to keep as flat as possible to maximize bandwidth even amongst path delay variation. This will help keep the bandwidth reasonably predictable as well.

The ultimate in demonstrations for this device would be implementation into an actual mobile device with the standards mentioned. This would be an immense undertaking and would have to be done at the company level, but would be the next step in proving its real world viability.

8.3 Contributions and Conclusions

The phase shifter design and results were submitted to and reviewed by the IEEE journal Transactions in Circuits and Systems (TCAS-II) in September 2015. The phase shifter paper is currently being reviewed for acceptability following revisions at the suggestion of the reviewers, which were submitted in November 2015. The phase shifter achieved comparable performance to state of the art 2.4GHz passive digital phase shifters, however, attained state of the art area efficiency with a 600% improvement in area over the smallest comparable shifter.

The full results of this work are in the process of being compiled for submission to the IEEE Journal of Solid State Circuits (JSSC). While some concerns and future work pursuits have been noted in this thesis, the ultra-compact nature of the design will have tradeoffs in accuracy, bandwidth, and performance in exchange for area.

This work has been very successful in terms of intellectual property development. Four provisional patents have been filed by Skyworks, with non-provisional filing being pursued in May 2015 before this document becomes public domain. A novel ambidextrous quadrant phase shifter and novel fine shifter with high ratio digital capacitors have been designed, in addition to a novel 3-port LNA combiner hybrid device.

An extremely compact co-channel interference canceller (CCIC) was designed in 130nm SOI RF CMOS at 2.4GHz. The system contained four novel circuits which have been provisionally filed with the US Patent and Trademark office. The 0.47mm^2 phase shifter designed for the CCIC improved area efficiency over comparable state of the art passive digital phase shifters by more than 600% while maintaining similar performance. The entire system took less than 25% of the area of the smallest phase shifter compared to. The CCIC was successfully able to cancel a self-generated co-channel signal by at least 25dB with no impact on the receive channel. The system would be suitable for use in current 802.11b/g/n and LTE near 2.4GHz with an inferred delay matched 20dB cancellation bandwidth of 50MHz. With limited delay matching capability, a 31MHz cancellation bandwidth was measured which is suitable for all but the 40MHz 802.11b/g/n channel. The overall utilized area on chip was extremely compact at 0.78mm^2. The receive device was highly linear with +7dBm IIP3, with a 1.5dB noise figure with 14dB of gain.

Appendices

A.1 Bonding Diagrams

The phase shifter chip bonding diagram is shown in Fig. 91 and the CCIC bonding diagram is shown in Fig. 92. Control bits S_X control the quadrant shifter, P_X controls the fine phase shifter, and a_X controls the attenuator.

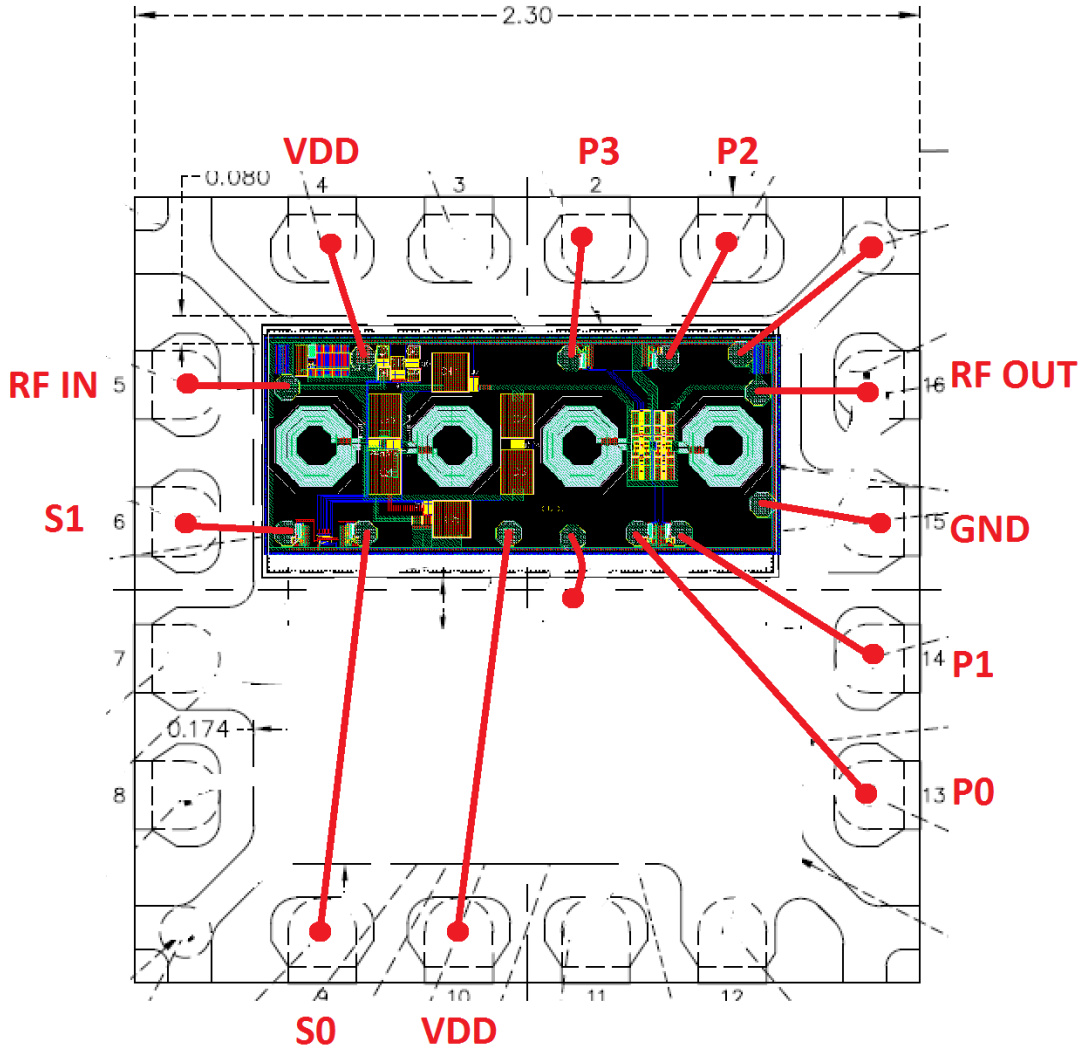

Fig. 91. Phase Shifter Bonding Diagram

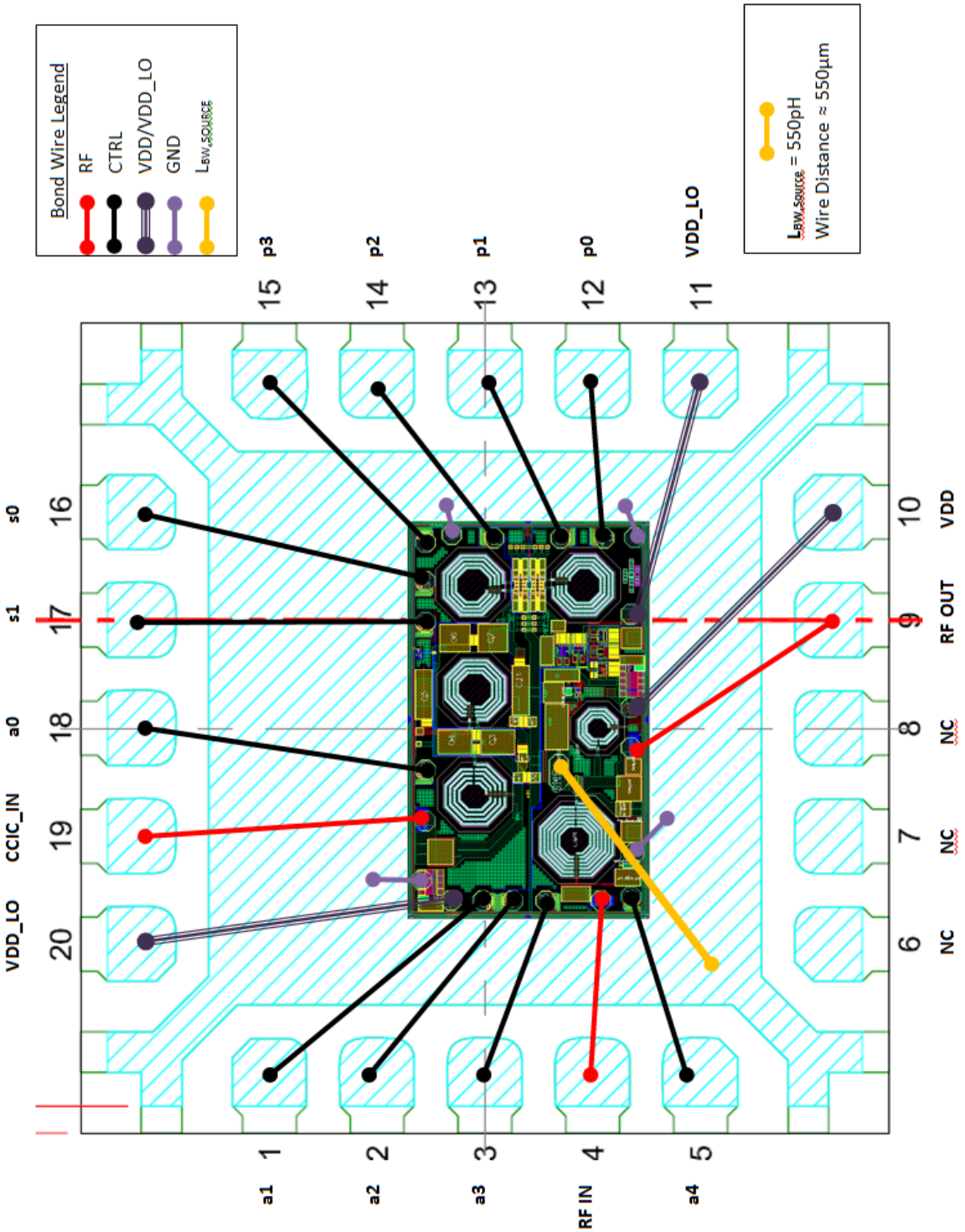

Fig. 92. CCIC Bonding Diagram

A.2 Quadrant Shifter Logic

The quadrant shifter logic design is shown in Fig. 93 with the corresponding schematic in Fig. 94. The layout is shown in Fig. 95.

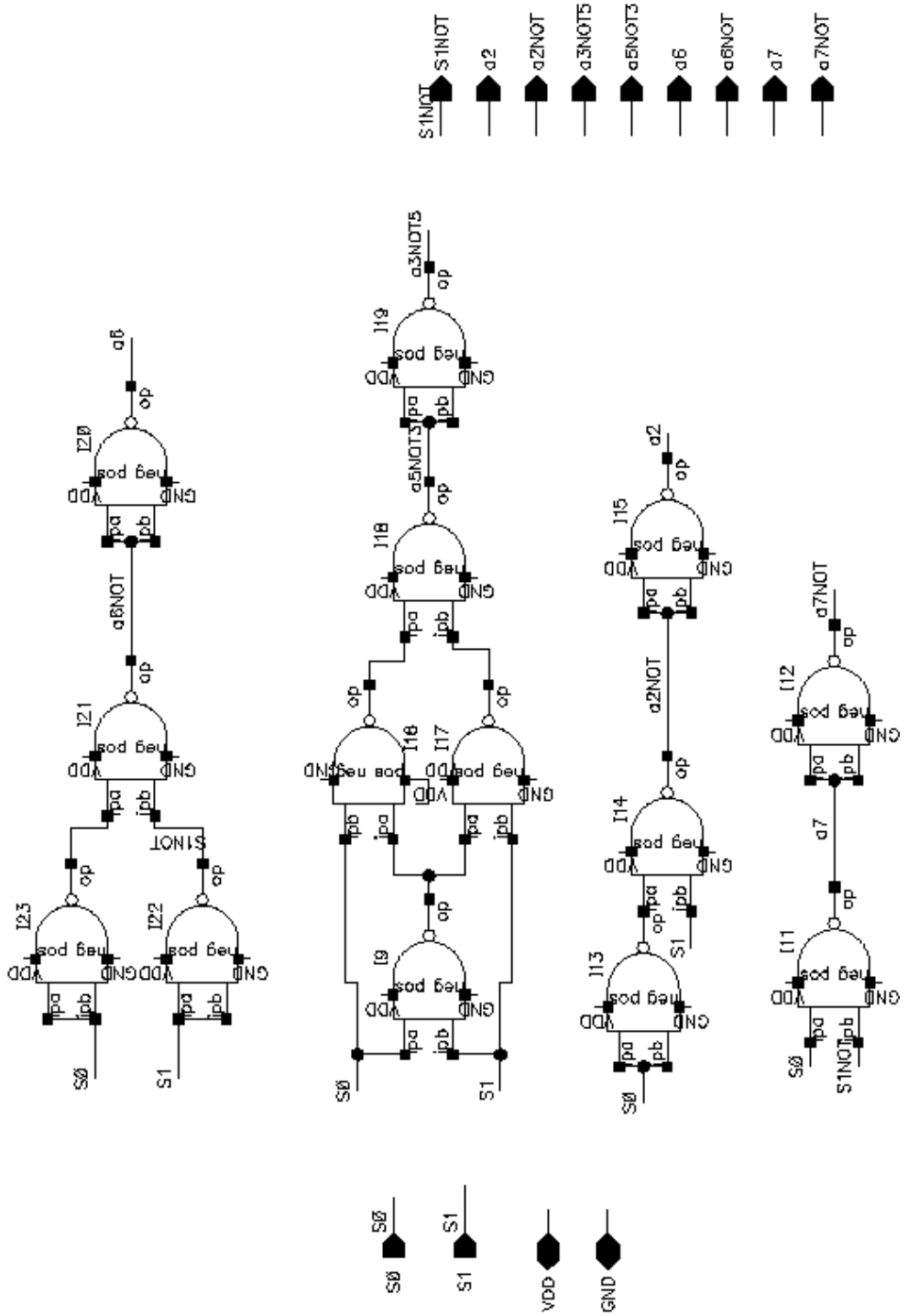

Fig. 93. Quadrant shifter logic design

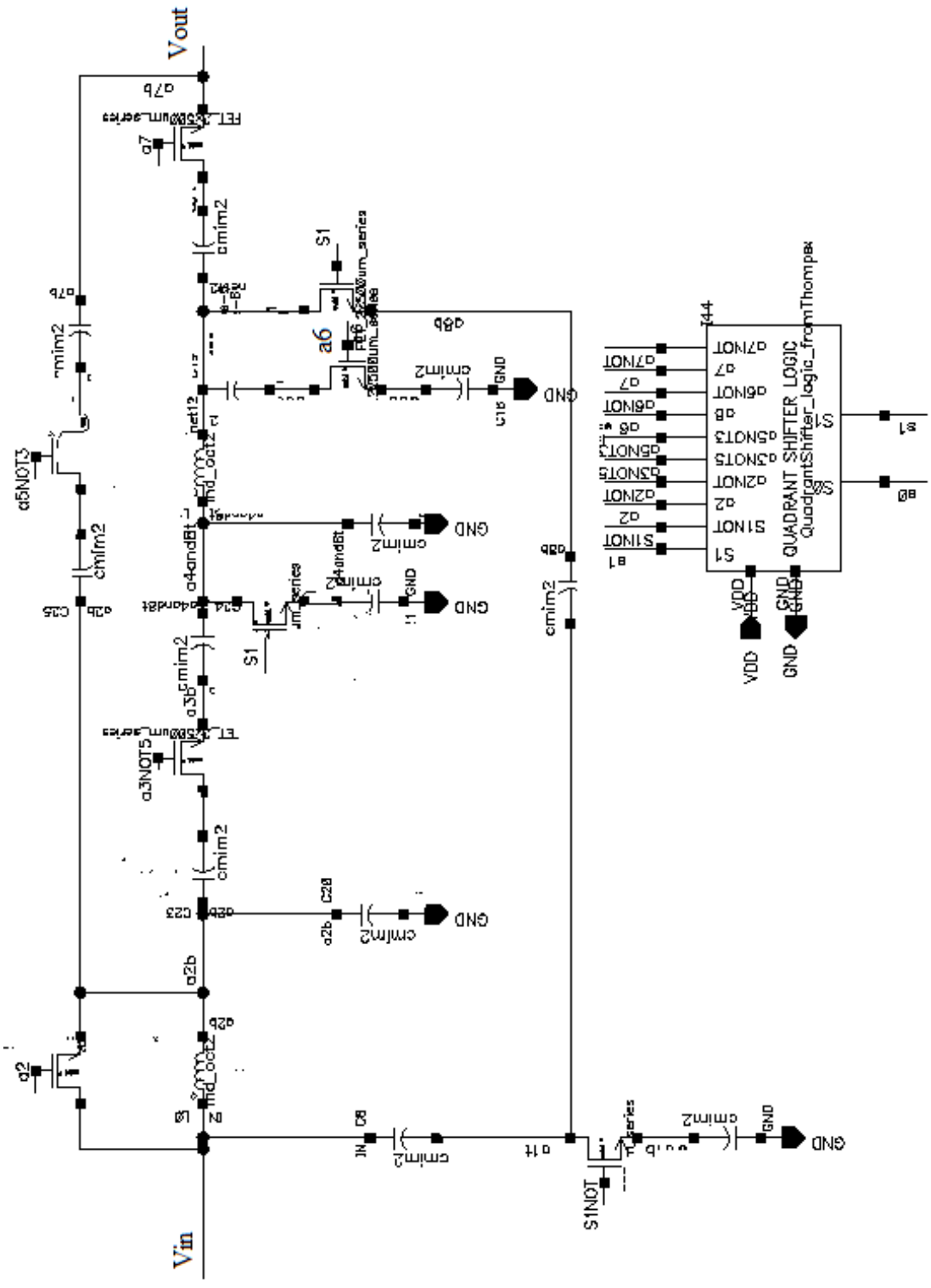

Fig. 94. Quadrant shifter logic signals on schematic

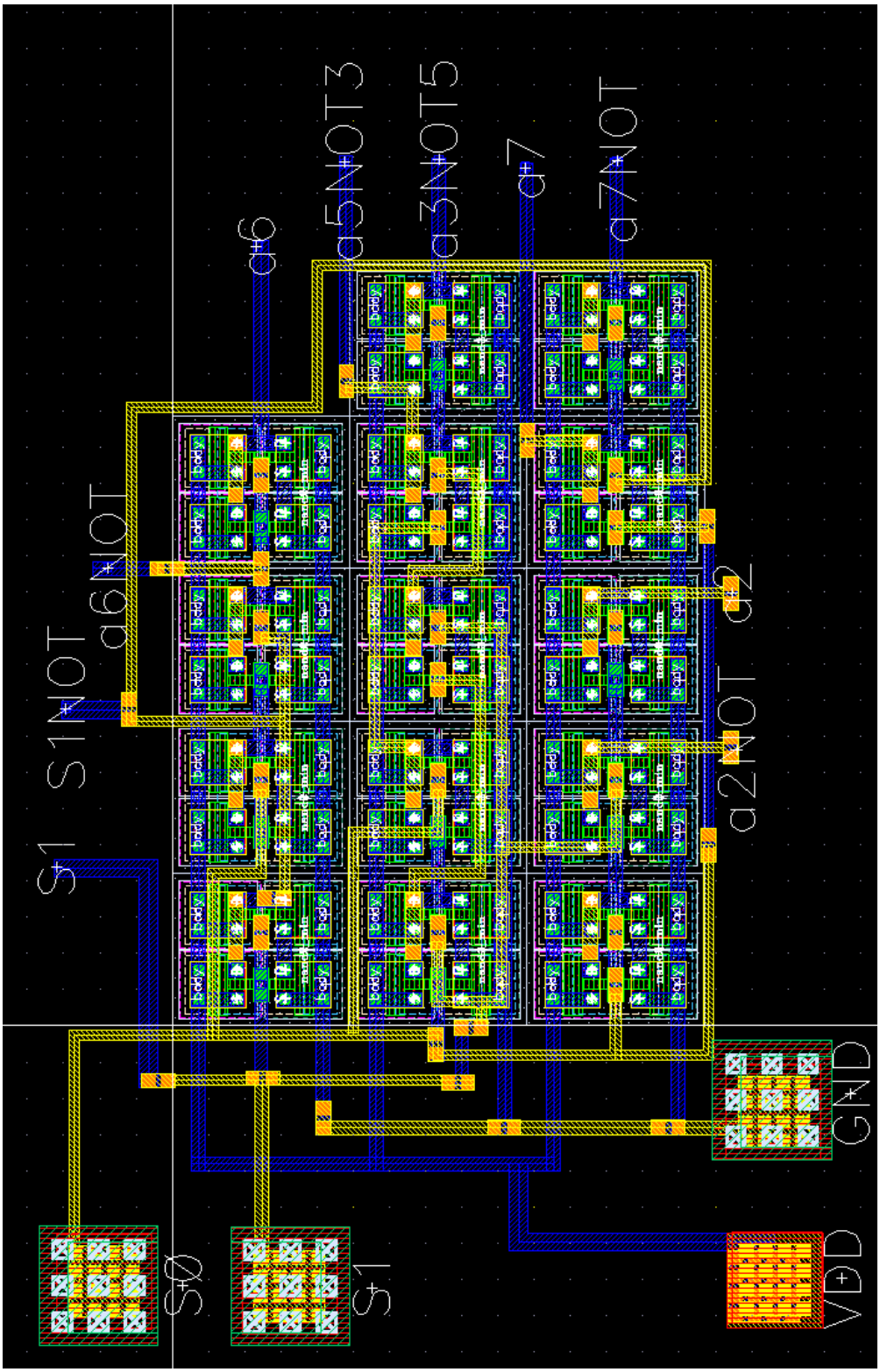

Fig. 95. Quadrant shifter logic layout

A.3 Warp Capable Silicon

One of the variants designed had additional area for "extra credit" to be pursued. The author intended to design IC's where no one has gone before. At 150µm in length, this Enterprise-D represents a 1/4,283,400 scale model and possibly the smallest ever created. The layout design followed by the photomicrograph is shown in Fig. 96.

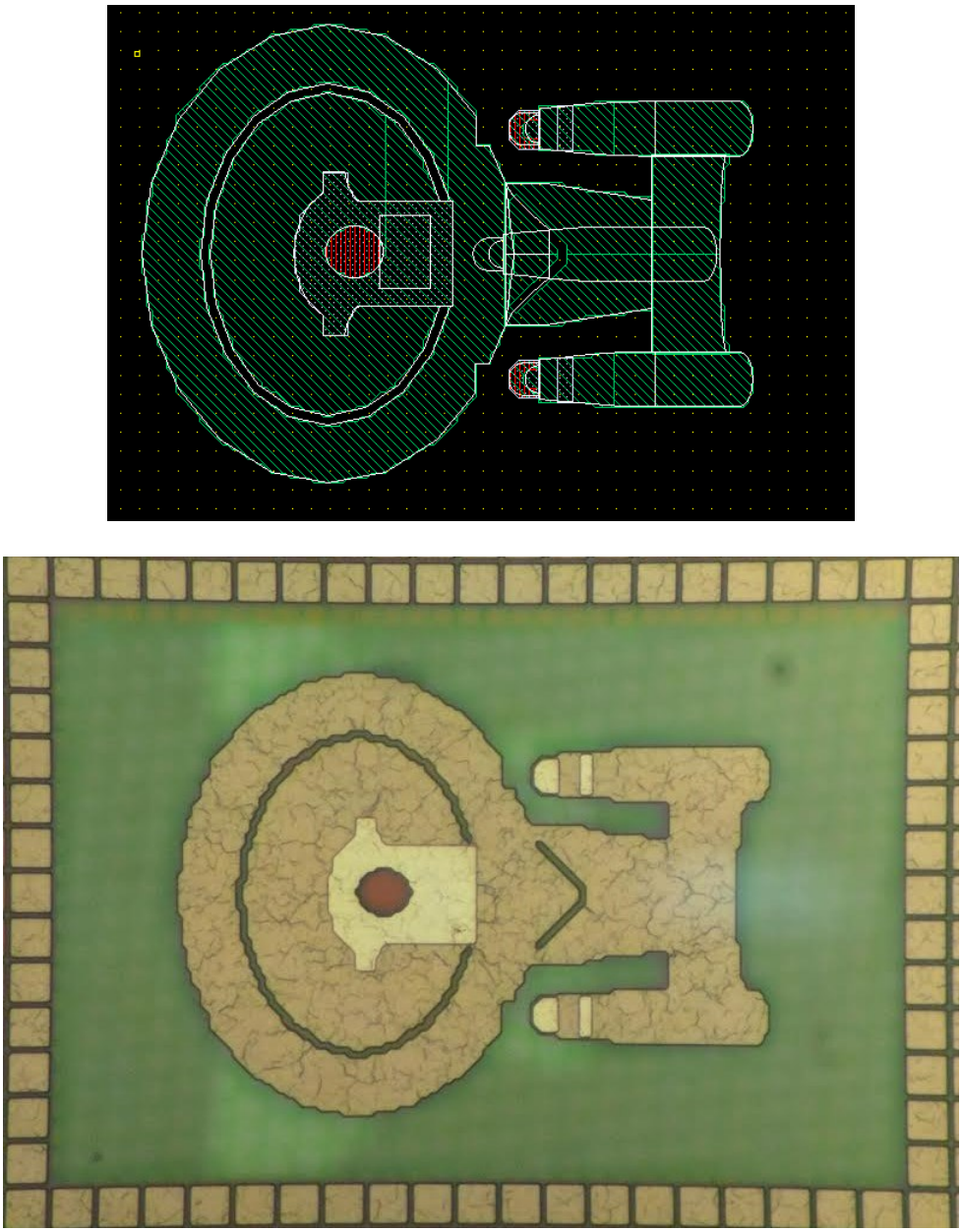

Fig. 96. Final Frontier in Silicon

References

[1] M. Rumney, "Keysight Technologies," 25 October 2012. [Online]. Available: http://www.keysight.com/upload/cmc_upload/All/25Oct12LTE.pdf. [Accessed August 2015].

[2] J.H.Winters, "Smart Antennas for Wireless Systems," *IEEE Personal Commun.,* vol. 5, no. 1, pp. 23-27, 1998.

[3] M. R. R. Khan and V. Tuzlukov, "Null-steering Beamforming for Cancellation of Co-channel Interference in CDMA Wireless Communication System," in *ICSPCS*, Gold Coast, Australia, 2010.

[4] T. Ishimoto and S. Hara, "A Simple Co-Channel Interference Cancellation for OFDM Diversity Receivers," in *Vehicle Technology Conference*, Barcelona, 2009.

[5] M. R. Islam and M. Ali, "A multi-element enhanced bandwidth PIFA for beam steering in a mobile phone at 1900 MHz," in *APSURSI*, Charleston, SC, 2009.

[6] J. Nisbet, "Feed-Forward Cancellation in Wireless Receivers". United States of America Patent US200802119389, 11 September 2008.

[7] D. Bharadia, E. Mcmilin and S. Katti, "Full Duplex Radios," in *SIGCOMM*, Hong Kong, 2013.

[8] T. Huusari, Y.-S. Choi, P. Liikkanen, D. Korpi, S. Talwar and M. Valkama, "Wideband Self-Adaptive RF Cancellation Circuit for Full-Duplex Radio: Operating Principle and Measurements," in *IEEE Vehicular Technology Conference (VTC)*, Glasgow, 2015.

[9] M. Jain, J. I. Choi, T. Kim, D. Bharadia, S. Seth, K. Srinivasan, P. Levis, S. Katt and P. Sinha, "Practical, real-time, full duplex wireless," in *MobiCom*, New York, NY, USA, 2011.

[10] D.-J. van den Broek, E. Klumperink and B. Nauta, "A Self-Interference-Cancelling Receiver for In-Band Full-Duplex Wireless with Low Distortion Under Cancellation of Strong TX Leakage," in *ISSCC*, San Francisco, CA, USA, 2015.

[11] IEEE Computer Society, "IEEE Standards Association," 2012. [Online]. Available: http://standards.ieee.org/about/get/802/802.11.html. [Accessed Nov. 2015].

[12] K. Maru, T. Chiba, K. Tanaka, S. Himi and H. Uetsuka, "Dynamic Gain Equalizer Using Hybrid Integrated Silica-Based Planar Lightwave Circuits With LiNbO3 Phase Shifter Array," *Jour. Of Lightwave Techn.,* vol. 24, no. 1, Jan. 2006.

[13] S. Voinigescu, High Frequency Integrated Circuits, New York, NY: Cambridge University Press, 2013.

[14] J. W. M. Rogers and C. Plett, Radio Frequency Integrated Circuit Design, 2nd ed., Norwood, MA, United States: Artech House, 2010.

[15] J. Nisbet, M. McPartlin and C.-W. P. Huang, "Switching Circuit". United States Patent US 8,451,044 B2, 28 May 2013.

[16] H. Sjoland, "Improved Switched Tuning of Differential CMOS VCOs," *IEEE Trans. Circ. Syst.,* vol. 49, no. 5, pp. 352-355, May 2002.

[17] P. Vizmuller, RF Design Guide: Systems, Circuits, and Equations, Norwood, MA, United States: Artech House, 1995.

[18] "Electronics Tutorials: Bridged-T Attenuator," [Online]. Available: http://www.electronics-tutorials.ws/attenuators/bridged-t-attenuator.html. [Accessed 25 January 2015].

[19] M. Meghdadi, M. Azizi, M. Kian, A. Med and M. Atarodi, "A 6-bit CMOS phase shifter for -band," *IEEE Trans. Microw. Theory Techn.,* vol. 58, no. 12, pp. 3519-3526, Dec. 2010.

[20] IEEE Computer Society, "IEEE Standards Association," 2013. [Online]. Available: http://standards.ieee.org/getieee802/download/802.11ac-2013.pdf. [Accessed Nov. 2015].

[21] R. Amirkhanzadeh, H. Sjöland, J. Redouté, D. Nobbe and M. Faulkner, "High-Resolution Passive Phase Shifters for Adaptive Duplexing Applications in SOS Process," *IEEE Trans. Microw. Theory Techn.,* vol. 62, no. 8, pp. 1678-1685, Aug. 2014.

[22] I. Bahl and D.Conway, "L- and S-band compact octave bandwidth 4-bit MMIC phase shifters," *IEEE Trans. Microw. Theory Techn.,* vol. 56, no. 2, pp. 293-299, Feb. 2008.

[23] Q. Xiao, "A compact -band broadband 6-bit MMIC phase shifter with low phase error," in *Proc. Eur. Microw. Integr. Circuits Conf.*, Oct. 2011.