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***In-Situ* Doped p^+ Polysilicon as a MOS Gate
Material**

by

Srilakshmi V. Dantu

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfilment of the requirements
for the degree of

Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering,
Department of Electronics,
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Ottawa, Ontario, Canada

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submitted by
Srilakshmi V. Dantu, M.Sc.,

in partial fulfilment of the requirements
for the degree of Master of Engineering.

Acting Chair, Department of Electronics

Thesis Supervisor

Carleton University

September 1994

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Abstract

In this thesis we examine the stability of heavily in-situ doped p^+ gates over thin gate oxide when subjected to rapid thermal anneal cycles of the kind that might be required to remove damage from the source/drain implants in a MOSFET.

p^+ gated MOS capacitors with oxide thicknesses ranging from 11 to 18 nm were fabricated on lightly-doped p-type silicon substrates. High-frequency C-V curves were recorded for the capacitors and the flatband voltage (V_{fb}) was computed following conventional analysis. No evidence of a decrease in capacitance at large negative gate voltage was seen, confirming that the gate is so heavily doped that polysilicon depletion is not a problem. No large shift in V_{fb} for RTA thermal budgets as high as 1050°C for 30 seconds was seen, even for 11 nm gate oxides.

D_{it} was computed by comparison of quasi-static and high frequency C-V curves. D_{it} values for the boron-doped gates were always higher than for phosphorus-doped control samples. However, no significant dependence of D_{it} on RTA thermal budget was found.

The strength of the gate dielectric was tested by slowly sweeping V_G from 0 to large negative values for 300 micron square capacitors using an HP4145A semiconductor Parameter Analyzer until destructive breakdown was observed. Average breakdown fields were found to be significantly lower for p^+ poly gate capacitors ($\approx 12 \text{ MVcm}^{-1}$) than for n^+ gates ($\approx 14 \text{ MVcm}^{-1}$). p^+ gated capacitors also showed hysteresis in gate I-V characteristics, presumably as the result of charge trapping in the oxide.

Time-dependent dielectric breakdown (TDDB) of the gate oxide was studied

by stressing to breakdown at high field. The time to breakdown at 4.5 MVcm^{-1} was then extrapolated. Once again the n^+ poly gated capacitors performed significantly better than devices with p^+ gates. However even the p^+ gated capacitors with the thinnest gate oxides had acceptable TDDB for circuit applications.

In conclusion, degenerate in-situ boron-doped polysilicon gates appear sufficiently stable over 10 nm gate oxide to support their use in CMOS processes with gate dimensions near 0.5 micron.

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Chapter 1

Introduction

Scaling down CMOS devices has been carried out to achieve higher packing density and better performance. However, when channel length decreases to deep submicron values, short channel effects for PMOSFETs and hot carrier effects for NMOSFETs become severe problems. The choice of gate electrode material for CMOS technologies has a direct impact on determining whether the NMOS or PMOS transistor will be a buried or surface channel device [1]. Conventional CMOS process that use n^+ poly silicon gates require p-type channel implants to adjust for the correct threshold voltage. This creates a channel p-n junction in the PMOS surface region (buried channel structure), resulting in surface channel NMOS and buried channel PMOS devices. Such buried channel devices exhibit enhanced short channel effects such as threshold voltage lowering and punchthrough leakage as compared to surface channel devices [2]. The punchthrough resistance of buried channel devices can be considerably improved by creating shallow channel p-n junctions and shallow

source/drain junctions. Techniques to produce shallow channel junctions include retrograde wells [3] [4] and punchthrough stopper implants placed just below the compensating channel implant [5] [6].

One approach that eliminates the need for compensated surface layers for the threshold voltage adjustment of either type of device, allowing both surface channel NMOS and PMOS devices, is the use of n-type and p-type polysilicon for the gates of NMOS and PMOS devices respectively. In this thesis technologies of this kind will be referred to as " n^+/μ^+ gate" processes. Several other approaches have been proposed to allow both surface channel NMOS and PMOS devices such as midgap refractory metal gates [7] and work-function-controlled silicide gates [4] or silicon/germanium alloy gates. However, these approaches risk gate oxide contamination from impurities in the gate electrode, and so have not been widely adopted.

Thus in most CMOS processes with gate length, L_g , less than approximately $0.6 \mu\text{m}$, the polysilicon gates are doped with the source/drain implants, providing n^+ poly gates for the n-channel transistors and p^+ poly gates for the p-channel transistors. Although this approach helps control short channel effects in the p-channel MOSFETs, it introduces several process complexities which are discussed by Wylie *et al* [8]. First, using different gate workfunctions for the two transistor types necessitates different threshold adjust implants, requiring that at least one (and possibly both) implants be masked. Second, doping the gate with the source/drain implant is not conducive to producing a high doping level at the polysilicon/gate oxide interface, which is in turn essential to avoid polysilicon depletion and consequent reduced

current sourcing [6]. The conflict between the need to preserve shallow source/drain junctions by minimizing implant dose, energy and anneal thermal budget while at the same time establishing uniformly heavy doping in the polysilicon gate becomes more acute as the gate length is reduced. Typically, this conflict is dealt with by reducing the gate polysilicon thickness, but this limits the width of any sidewall spacer attached to the gate, which in turn compromises the design of lightly doped drain (LDD) structures required to avoid hot carrier effects.

In an n^+/p^+ gate process, it is normal practice to use salicidation to ensure that any pn junction formed in the polysilicon between the two types of MOSFET is shorted out. But in this approach, it has been found that [4] the impurities which are used to dope the underlying polysilicon (arsenic, phosphorous and boron) may diffuse laterally through the silicide layer at such enormous rates that conversion of the type of the underlying polysilicon in the neighbouring gate can occur. Such conversion of the gate type causes large variations in the threshold voltages of NMOS and PMOS devices that share the common polycide gate.

Taking above issues into consideration, Wylie *et al* [9] suggested an alternative approach to sub half-micron CMOS, in which both n- and p- channel devices have p^+ poly gates. This approach provides the advantages of surface p-channel transistors while avoiding the problems encountered when the source/drain implant is used to dope the gate. Use of a p^+ poly gate gives a buried n-channel MOSFET, which is susceptible to short channel effects. However it is found that these are more easily controlled than in the case of buried p-channel device, since it is easier to form

source/drain junctions and threshold adjust implants with arsenic or antimony than with boron. Although the buried-channel NMOS transistor can be more prone to short channel effects than a surface-channel NMOS device, the performance of the buried-channel NMOS device benefits from the enhanced electron channel mobility that results from the buried channel structure (resulting from reduced surface scattering), and from improved hot-carrier life time due to the displacement of the region of hot electron generation from the sensitive Si/SiO_2 interface.

So far, blanket p^+ poly gate CMOS has received very little attention. A $1.2\ \mu\text{m}$ channel length process with blanket p^+ poly gates was reported by Parillo *et al* in 1984 [4], with emphasis on avoiding lateral diffusion effects in the polysilicon during salicidation. A CMOS process using p-type polysilicon gates for both n- and p- channel devices was reported by Pfeister *et al* in 1988 [10], but this process used a lightly doped p^- gate for the n-channel transistor, forming a surface channel device. Some data on p^+ polysilicon gated n channel transistors with gate lengths near $1\ \mu\text{m}$ was provided by Noguchi *et al* [7] in conjunction with a study of refractory metal gates. Wylie *et al* [8] emphasis on the advantages offered by the blanket p^+ poly flow in providing sub half-micron gate devices capable of reliable operation from 5 V supplies.

The blanket p^+ poly gate approach lends itself to heavy *in-situ* doping of the gate with boron during deposition. This avoids the need to compromise between the formation of very shallow source and drain junctions and the establishment of degenerate doping at the polysilicon/gate oxide interface.

Eguchi *et al* [17] recently proposed an alternative use of *in-situ* gate doping with boron in a submicron CMOS technology. In their approach, an *in-situ* boron-doped polysilicon film was used to form the gates of both types of transistors. The n-channel gates were then converted to n^+ doping by a heavy phosphorus implant.

Whether *in-situ* boron doped gates are used in a blanket p^+ gate technology as suggested by Wylie *et al*, or in this compensated gate approach of Eguchi *et al*, it is necessary to demonstrate that a heavily *in-situ* doped gate formed over very thin gate oxide can withstand the thermal budget required to anneal the source/drain implants in a CMOS process. The penetration of boron from the degenerate p^+ poly gate through thin gate oxide into the channel region is a major concern even for implanted gates [11-13]. The problem is likely to be considerably worse for *in-situ* doped gates, since in this structure there is no "lag time" while boron diffuses from the heavily implanted region near the surface of the polysilicon to the polysilicon/gate oxide interface. Instead, with an *in-situ* doped gate boron is present in extremely high concentration immediately adjacent to the gate oxide through the source/drain anneal cycle.

The suppression of boron diffusion through thin gate dielectrics by the use of an oxynitride in place of pure thermal oxide has been studied [13]. However, oxynitride dielectrics have been linked to reduced hole mobility in the surface channel. So, that pure oxide dielectrics are generally preferred. Rapid thermal annealing, which is commonly used to anneal source/drain implants while preserving shallow junctions, should also be of assistance in minimizing boron diffusion through the gate oxide.

This thesis examines the stability of heavily *in-situ* boron doped polysilicon gates over thin thermal gate oxide when subjected to rapid thermal anneal cycles of the kind that might be required to remove damage from source/drain implants. Aspects of stability investigated include flatband and threshold voltage shift, interface state density, dielectric strength and time dependent dielectric breakdown.

This thesis is organized in the following way. In the next chapter, a brief review of the previous work done on p^+ gated devices is given. Other related issues are also briefly reviewed in this chapter. In the third chapter, the different experimental methods and characterization techniques used in this work are described. In the fourth chapter, the experimental results are presented and analyzed and finally we conclude the experimental results in the fifth chapter.

Chapter 2

Background

In this chapter, we present a brief review of the previous work done on p^+ polysilicon gates in regard to the dopant diffusion from the gate and other issues related to their reliability.

2.1 Diffusion of boron through the gate in p^+ gate MOS devices

p^+ polysilicon gate MOS devices under positive bias temperature stress have exhibited large degradation of electrical characteristics. The degradation involves shift in threshold and flat band voltages or increases in interface-state density at the SiO_2/Si interface [16] [13]. The boron used to dope these p^+ polysilicon gate electrodes can diffuse through the thin gate oxide and into the underlying silicon channel region

causing an instability in the threshold voltage [16]. Thus although p^+ gates provided improvements in short channel behaviour in PMOS devices, boron penetration from p^+ polysilicon gates has become a critical issue for surface channel submicrometer PMOS/buried channel NMOS design.

2.1.1 Boron Penetration Models

Since boron penetration is dominated by diffusion through the thin gate oxide, the flatband voltage/threshold voltage shift is increased by either decreasing the gate oxide thickness or increasing the thermal anneal budget [16]. Previous studies have shown that these threshold shifts due to boron penetration become more severe with annealing in the presence of hydrogen. For example, Sun *et al* [11] studied the temperature and ambient effects on boron penetration from an ion implanted gate electrode through very thin oxides. Figure 2.1 summarizes their results in the above aspect. From the figure, it is very clear that the thermal cycle should be optimized to minimize boron penetration and also care must be taken to minimize hydrogen or moisture in the annealing ambient after poly gate formation.

The boron penetration phenomenon may be modeled by a very thin sheet of charge at the Si/SiO_2 interface [15]. This negative charge may be represented by either a fixed charge in the oxide which resides close to the oxide/silicon interface or by a p-type layer in the silicon substrate [Figure 2.2]. Previous studies have also linked boron penetration with both a shallow p-type layer in the silicon and water related traps in the SiO_2 .

Figure 2.1: Flatband voltage versus anneal temperature for different ambients [11]

Figure 2.2: Models for boron penetration [15]

Pfiester *et al* [19], used device and process simulation to determine the shape of the boron profile in the silicon substrate which results from boron penetration from the p^+ polysilicon gate. A consistent result was reported from both process and device simulation which indicated a very shallow exponential profile for the boron p-type layer. In this paper the authors assumed an exponential characteristic decay length of $70\text{\AA}$ and used SEDAN simulation to predict the change in PMOS threshold voltage as a function of different surface concentration values. A near-linear relationship was obtained for the dependence of threshold voltage shift on the p-type surface concentration (see Figure 2.3). Corresponding two-dimensional simulation using PISCES indicates complete depletion of this shallow p-type layer even for surface concentrations as high as $5 \times 10^{19} \text{ cm}^{-3}$. The authors also measured subthreshold I-V curves for 0.8 micron channel-length PMOS devices which exhibit threshold voltage shifts as high as 2 V but with complete turn-off in the subthreshold regime. Additional device measurements including carrier, freeze-out effects at 77 K, threshold voltage sensitivity to operating temperature, and change in subthreshold slope have been used to substantiate the shallowness of the p-type layer.

The effective boron diffusivity in the gate oxide for the BF_3 implanted samples was determined using estimated values of the p-type surface concentration and the anneal time. A consistent boron diffusivity of $0.1 \text{ cm}^2/\text{s}$ was obtained for the 12.5 nm gate oxide samples. The SUPREM3 default diffusivity value of $3.5 \times 10^{-4} \text{ cm}^2/\text{s}$ predicted no significant penetration of boron into the underlying n-type substrate, as shown in Figure 2.1. It was also shown that the boron flux is dominated by

Figure 2.3: SEDAN simulation results for PMOS capacitor threshold voltage as a function of the p-type surface concentration for both 8 nm and 12.5 nm gate oxides. The assumed exponential p-type profile has a vertical characteristic length of 7 nm. Taken from [19]

diffusion across the thin gate oxide region. Since the enhanced boron diffusivity in the gate oxide is comparable to that in silicon, the resulting boron profile in the silicon substrate is very shallow to satisfy the steady-state segregation at the oxide/silicon interface.

2.1.2 Effect of Flourine in p^+ Gate Devices

Although some studies [20] indicate that flourine can be beneficial in phosphorous doped NMOS polysilicon gates, it is reported recently that flourine and boron, when implanted into polysilicon, readily segregate into the underlying SiO_2 layer [15] [16]. Flourine incorporation into the gate oxide which results from BF_2 implantation, can jeopardize the p^+ gate devices even under moderate annealing temperatures. It enhances the boron penetration problem resulting in PMOS devices with positive threshold voltage shifts (V_t), and an increase in the electron trapping rate in the gate oxide. It has been shown that the resulting boron distribution in the substrate can explain the experimentally observed changes in the device behaviour.

The flourine influence on the device characteristics particularly on the gate oxide quality of the n^+ poly MOS structure, had been studied quite extensively in the literature, because flourine can be inadvertently introduced into the gate in processes such as tungsten silicidation, BF_2 source/drain and/or gate implantation during the MOSFET fabrication. In the n^+ gate MOS devices, the incorporation of flourine into gate oxide was found to be advantageous in terms of fixed charge reduction, interface state reduction and hot electron hardness. The associated physical

Figure 2.4: SUPREM4 simulation results for the 12.5 nm gate oxide PMOS capacitor. Thermal anneal times of 15, 30, 60 min at 900°C were simulated corresponding to the threshold voltage. Taken from [19]

mechanisms accounting for the observed advantages by fluorine pointed to the reduction of unsaturated Si bonds, and/or additional oxide grown in the SiO_2 network [21] [22], which resulted from fluorine incorporated in the bulk of oxide.

The detail interaction of B/F with SiO_2 network results in the observed fluorine effect in the p^+ gate devices is not very clearly understood yet. Sung et al, [15] proposed a hypothetical explanation regarding the role of fluorine in SiO_2 : when the fluorine is activated, fluorine-boron complexes then bind the dangling bonds in the SiO_2 , producing the negative charge states near/at the SiO_2/Si interface. In addition fluorine is probably able to prevent the formation of B_2O_3 or related complexes. Thus boron can easily diffuse through the thin SiO_2 layer and penetrate into the silicon substrate.

Thus the common practice to help minimize the boron penetration is to keep the hydrogen content in the annealing furnaces as low as possible. Also, it is widely agreed that fluorine should be avoided in p^+ gate devices and B^+ implantation or *in-situ* doping is preferable for the gate formation.

In the case of p^+ polysilicon, a gettering effect for mobile ions was studied also [23]. It is reported that boron has less gettering effect than phosphorous in n^+ polysilicon. Consequently in p^+ polysilicon gates, Na^+ ions diffuse laterally from the capacitor edge into the gate oxide. This lateral diffusion may effect device reliability more seriously than vertical diffusion through polysilicon. Since it is an important and more serious problem in p^+ gate devices, a brief review is needed regarding the role of mobile ionic impurities in SiO_2 dielectric and their effect on MOS devices.

2.2 Mobile ionic impurities in MOS devices

Thermally grown SiO_2 layers are excellent insulators for the gate, field and interlevel dielectrics in silicon circuitry. However, the electronic behaviour of silicon devices is degraded by the action of mobile ionic impurities drifting and diffusing through these oxides. This ionic charge induces a charge of opposite polarity in the substrate. The amount of induced charge relates inversely to the distance of the oxide charge from the substrate. In MOS devices, the induced charge causes shifts in the flatband voltage and therefore the threshold voltage. The most common mobile impurities are small, light, alkali ions. Na^+ is the most common one, and moves freely above 110°C . It can be detected by the bias temperature stress test discussed below. The presence of Na^+ in the oxide also strongly influences the radiation sensitivity of these devices. To retain satisfactory performance for most silicon devices, mobile charge concentrations must be kept near or below $10^{10} \text{ ions/cm}^2$.

Many of the substances used in the fabrication of MOS devices are sources of Na^+ contamination. Alkali ions do get into the wafers through furnace tubes and boats, fixtures in metal deposition systems, gaseous ambients and reactants, chemical etchants and solvents, beakers, tweezers and human handling. Sodium contamination is usually kept in the $10^9 - 10^{10} \text{ ions/cm}^2$ range in modern fabrication lines, but can vary from $10^8 - 10^{12} \text{ ions/cm}^2$.

The chief means of reducing the effect of mobile alkali ions is to minimize their quantity through clean fabrication material and equipment. As an adjunct,

gettering of the impurities can be accomplished through the introduction of chlorine anions or cations in doped glasses. A mixture of O_2 and HCl is often introduced into quartz furnace tubes used for processing. This " HCl clean" works by reacting Cl^- with Na^+ to form a volatile $NaCl$ complex which evaporates during heating, or inactive salts upon cooling. This reduces the mobile ion concentration by more than an order of magnitude with no change in other characteristics.

The most widely used non-destructive measurement technique to check for mobile ion contamination is the Temperature Bias Stress Test (TBST), which is explained below. In this test, a voltage is applied between the gate and substrate of the device while temperature is elevated for a given duration and then returned to the start temperature. The flatband voltage changes due to shift of mobile ionic impurities and polarization of the dielectric. Figure 2.5 [24] depicts a cross-sectional view of the MOS capacitor and illustrates alkali ion movement during negative and positive-bias stressing.

The test conditions should be chosen such that virtually all of the mobile oxide charge is shifted from one oxide boundary to the other. The charge magnitude can then be determined by multiplying the flatband voltage shift by the oxide capacitance per unit area, and dividing by the electron charge. The stress parameters (electric field, temperature, time) strongly influence the amount of shift. The positive features of the TBST are that it is non-destructive, simple, relatively quick, and can resolve charged impurities at less than 10^9 ions/cm² concentrations. The negatives include the need for correction for polarization of the oxide and the fact

Figure 2.5: Ionic movement during electrothermal stress

that any change in interface state density during stress affects the results.

2.3 I-V characteristics of a MOS device

The I-V characteristics for MOS diodes have a number of distinct regimes. Normally, we assume the insulating material to have a band structure analogous to a semiconductor with a very wide band-gap (approximately 9 eV for SiO_2). The large effective band-gap difference between the oxide and the silicon results in a large barriers to electrons in the conduction band (3.2 eV) and holes in the valence band (4.7 eV) at both the polysilicon-to-oxide and the silicon-to-oxide interfaces. Due to the height of the potential barriers, the amount of thermionic emission is completely negligible at normal operating temperatures and for potential drops across the insulator less than the barrier height, the current through the capacitor structure is dominated by parasitic parallel leakage paths.

Once the potential drop across the gate insulator becomes comparable to the barrier height, the width of the barrier is effectively modulated. Figure 2.6 shows the band structure of the n-channel device biased so high into inversion that the effective barrier to electrons has been reduced to half its low field width. In such a situation, carriers may be able to tunnel from the conduction band of the gate electrode into the conduction band of the oxide where they are swept out by the high electric field. Since the probability of tunneling through a barrier is strongly related to the width of the barrier, once this width starts narrowing, the current

through the structure rises dramatically. This conduction mechanism, known as Fowler-Nordheim tunneling, is typically the dominant conduction process for MOS diodes with SiO_2 thinner dielectrics. A simplified equation which describes Fowler-Nordheim tunneling is:

$$J \propto E^2 \exp(-k_2/E) \quad (2.1)$$

where J is the current density through the structure, E is the electric field in the insulator and k_2 is a constant which depends on the barrier height, ϕ_B , and on the effective mass of the carrier in the insulator, m_{eff} .

Fowler-Nordheim conduction is usually accompanied by a polarization effect where some of the charges injected into the dielectric become trapped. This effect is readily observed as a change (reduction in the currents) in the I-V characteristic as subsequent sweeps of voltage are applied since the trapped charge distorts the electric field within the dielectric to the extent that current injection is suppressed. The polarization effect may also be seen as a change of current with time for a fixed bias voltage. The charge trapping ability of the structure should be minimized as it leads to instabilities in device parameters such as the threshold voltage.

The tunneling current through the device rises slightly less than exponentially with increasing bias until, eventually, the insulating layer suffers a catastrophic breakdown and the current level is limited only by parasitic resistances. This is known as dielectric breakdown and, unlike avalanche breakdown in semiconductors,

Figure 2.6: Band diagram of an n-channel device at the onset of Fowler-Nordheim tunneling

tends to be permanent for SiO_2 layers. As SiO_2 layers become thinner, the breakdown fields on single crystal silicon have been found to increase substantially and, as the thickness tends to zero, they approach the maximum Si-O bond strength of 30 MV/cm. For dielectric thickness between 15 and 17.5 nm, breakdown fields on the order of 15-16 MV/cm are the expected upper limit.

As with tunneling characteristics, breakdown field measurements provide a means of measuring the quality of both the dielectric and the injecting interface. If the interface has many asperities, or the asperities which it has are substantial, localized electric field enhancement will reduce the overall measured breakdown field. Also, low field and infant failures may occur due to pin-holes or other defects in the film.

Chapter 3

Experiments

In this chapter, the experimental method utilized will be described. First, the process involved in fabricating the test device structures is described and then different tests done for their characterization are explained.

The experiments in this study attempted to disclose the following concerns:

1. To find out the maximum thermal budget that can be used in in-situ doped p^+ gate devices.
2. To see if there is a difference in device reliability under these conditions between n^+ gate and p^+ gate devices.
3. To identify the device reliability properties, if any influenced by the thermal anneal.

3.1 Device Fabrication

The complete process specification for the device fabrication is given in Appendix I. Each sample wafer began as 2 Ω cm p-type (100) silicon. The wafers were given an "RCA" clean and 1 μ m thick field oxide was grown using an dry O_2 / O_2 +pyrogenic H_2O / O_2 +2.5% HCl sequence for 10/180/30 minutes respectively (2.5% HCl in O_2 was used to restrict Na^+ content). This was followed by a 40 minute anneal in N_2 . Device wells were opened using *BHF* ("Buffered HydroFlouric Acid"- 9:1, NH_4F : HF) etch until the Si surface was exposed. Following an RCA clean, the wafers were divided into different sets to grow 10 nm, 11 nm, 12.5 nm and 17 nm gate oxides. These four different thicknesses of gate oxides were thermally grown in dry O_2 at 900°C using a conventional horizontal quartz tube furnace. At this point, half the number of wafers in each thickness range were rapid thermal annealed at 1000°C for 10 seconds. *In-situ* boron and phosphorous doped gate polysilicon of 0.4 μ m and 0.15 μ m thickness respectively was deposited on to the gate oxide using LPCVD deposition. Deposition was done at 560°C temperature and the pressure was maintained at 0.4 Torr for p^+ gate deposition. The experimental procedure used for this is explained below.

3.1.1 LPCVD deposition of in-situ boron doped gate polysilicon

The LPCVD system employed in this study consisted of a horizontal quartz tube reactor in a conventional three zone furnace [25]. Wafers were loaded back-to-back vertically in a quartz boat so that the wafers were perpendicular to the tube axis, as shown in Figure 3.1. Earlier work [25] indicated that in order to obtain acceptable load uniformity, it was necessary to use a gas injector tube, a 1cm diameter quartz tube that lies along the bottom of the reactor and which carries the reactant gases from the gas inlet to just below the wafer boats where small carefully placed holes in the injector allow the gases to enter the reactor. The use of an injector tube allows more even distribution of the reactant gases among the wafers and reduces gas depletion effects. In addition, covered boats and wafer spacing of approximately 9 mm, both of which are also used for phosphorous-doped polysilicon, were required to achieve across wafer uniformity.

Source gases were supplied to the reactor as silane and 30% diborane diluted in silane. The flow of each source gas was controlled independently by a mass flow controller. For all experimental runs, fixed flows for each source gas (SiH_4 and B_2H_6) were maintained. Since the system was not equipped with a throttle valve to control pressure, pressure was determined by the pumping speed of the vacuum pump and therefore was affected by temperature, total gas flow, and reaction rate. Pressure during deposition ranged from 0.35 to 0.4 Torr for different experimental runs

Figure 3.1: LPCVD system [25]

depending on the deposition parameters (with temperature having the strongest effect). The deposition temperature was monitored by a thermocouple which extended into the reactor just below the wafers. Since the crystal structure of the deposited silicon is critically dependent on the deposition temperature, particularly at temperatures close to the amorphous/polycrystalline transition, the temperature profile was maintained as flat as possible ($\pm 2^\circ\text{C}$) over the length of the wafer load. The injector tube described earlier was therefore required to obtain across load uniformity due to the lack of a temperature ramp which is commonly used to compensate for gas depletion effects. The temperature was maintained at 560°C . The test slices were placed in representative locations throughout the load while dummy wafers filled the remaining slots.

After the gate polysilicon was deposited, gate patterns were formed by wet etching in polyetch at room temperature for about 50 seconds using a photoresist mask. The wafers were all RCA cleaned with no HF. After this step, the wafers of each thickness were separated into various sets and annealed in the RTA for various times and at various temperatures to observe boron diffusion effects. After the polysilicon films were patterned the resistivity was determined using a Van der Pauw cross technique.

The gate dopant activation was carried out in an A. G. Associate Heat Pulse Model 210 rapid thermal annealer. The set-up and the procedure are explained below.

3.1.2 Rapid thermal annealing

A cross section of the Heatpulse 210 rapid thermal processing system is shown in Figure 3.2. It consists of quartz tube chamber which is heated by two rows of tungsten halogen lamps, one at the top and the other at the bottom. The wafer is transported to the chamber through a flat quartz stand attached to the chamber door. The wafers are heated by the radiant energy of the lamps. The wafer temperature is monitored through a chromel alumel thermocouple embedded in a T-shaped silicon piece and pre-calibrated to represent the temperature of the wafer being processed. The operating temperature range is 300-1150° C with an accuracy of $\pm 7^{\circ}\text{C}$. The heating rate is quite fast, of the order of 100-150° C per second. A maximum annealing time of 300 seconds can be attained with this system. Before loading each wafer, the chamber was purged with N_2 to expel any air present, the constituents of which are likely to contaminate the wafer and cause unwanted oxidation. The wafer is then loaded and heated.

Following the rapid thermal anneal cycle, aluminum was electron-beam evaporated onto the top-side of the wafers, to a thickness of 1 μm . Just prior to loading the wafers into the evaporator for aluminum deposition, they were given a ten minute DI water rinse. A photoresist mask was then formed, and the metal was patterned using phosphoric acid etchant. Next, 0.5 μm of aluminum was electron-beam evaporated onto the back of the wafers for good electrical contact to the substrate during probing.

Figure 3.2: Thermal processing system

Later, all the wafers are annealed in H_2 for 20 minutes at 400°C . Figure 3.3 depicts a MOS capacitor formed using the above procedure.

3.2 Characterization of the devices

3.2.1 Physical characterization

Ellipsometry

Ellipsometry is a technique which allows the measurement of optical properties of material systems composed of various layers. If each layer of structure may be considered to be homogeneous and uniform with respect to the parameters index of refraction, n , extinction coefficient, k , and thickness, then fixed-wavelength ellipsometry provides a method of determining any single parameter or pair of parameters of the structure provided all others are known. The technique measures the change in phase difference, Δ , and the change in amplitude ratio, of polarized light beam upon reflection off the surface of the structure. The ellipsometry readings, Δ , and Ψ , are related to the complex reflection coefficients R^P and R^S , for light polarized parallel and perpendicular to the plane of incidence respectively by

$$\tan(\Psi)\exp(i\Delta) = \frac{R^P}{R^S} \quad (3.1)$$

From basic optics theory, formulae may be developed which express R^P and R^S , and therefore Ψ , and Δ , as a function of the unknown parameters in a given

Figure 3.3: Basic MOS capacitor test structure

structure. An iterative numerical technique, such as Newton's method, may then be used to solve for the unknown parameters, from measured ψ , and Δ values.

The most common use for ellipsometry, by far, is the measurements of the thickness of oxide layers on silicon. For improved accuracy, it is desirable for the substrate material to be absorbing strongly at the measurement wavelength.

Ellipsometry handles intermediate film thicknesses (≈ 20 nm) well and is the industry standard method for measuring oxide thickness. For very thin films, however, errors may result from the non-uniform refractive index caused by thin film stresses. There is disagreement, in this regime, as to whether the thin film's refractive index should be considered fixed or variable to gain accuracy in the thickness calculation. For these reasons, one must assume a possible error of at least ± 5 -10% on film thickness measurements below 20 nm obtained by ellipsometry.

Though most initial work relied on ellipsometry to measure oxide thickness, second and third round experimentation favoured the use of capacitance as an indication of oxide thickness. The bulk of the characterization performed in this work was electrical in nature. Capacitor structures of various sizes were used to characterize the dielectrics, the interfaces and the overall process.

Secondary ion mass spectroscopy (SIMS)

To establish the boron content in the poly gate, SIMS analysis was done on representative samples. Energetic ion bombardment of a surface causes atoms to be

ejected from the sample by the sputtering process. A fraction of the ejected species are either positive or negative ions. This fraction is mass analyzed in a mass spectrometer to determine the elemental composition of the material from the sample surface. Because of the high sensitivity of the mass spectrometer, small traces of an element can be detected. All elements, even hydrogen, can be detected with SIMS. Because of the sputtering nature of the technique, measurements of the ion currents as a function of time provides a depth-composition profile, from the original surface into the bulk of the material.

3.2.2 Electrical characterization

MOS capacitor structures of various sizes were used to measure capacitance-voltage (C-V) and current-voltage (I-V) characteristics. The analysis of MOS C-V curves to determine oxide thickness, effective uniform substrate doping density, flat-band voltage and oxide fixed charge was performed in the standard first-order manner as described by Nicollian and Brews [26].

C-V Technique

A description of the laboratory apparatus and measurement automation program is given in this section. The equipment used to execute the C-V tests is illustrated in figure 3.4 [24]. To contact the MOS capacitors two probes in a small probe station were used. The station had a chuck equipped with a vacuum port in the centre. The probe station was enclosed in a lidded black box to shield the wafers from airborne

Figure 3.3: C-V measurement equipment [24]

debris and ambient light. The attached vacuum pump holds the wafers firmly to the chuck during probing. To aid placement of the probe tips, a monoscope was used. The probes and chuck were connected to an HP4280A C-V meter for data acquisition, with the C-V meter controlled by an HP9816 microcomputer via HPIB bus. The computer had hard and soft disk drives for data storage. An HP7475A plotter was connected so that hard copies of the C-V plots could be made.

For the TBS tests, a heating coil which was externally controlled, plumbing for cooling water, a thermocouple for temperature sensing and a connector for electrical contact to the wafer substrate are attached to the probe station.

Sheet Resistance measurements

Polysilicon sheet resistance is measured a Van der Pauw cross structure, which is shown in Figure 3.5. The resistivity of a sample of this type can be determined by passing a known current through two adjacent terminals and measuring the voltage developed across the other two terminals. Then the sheet resistance is given by the following equation:

$$R_s = (\pi/\ln 2) \frac{V}{I} \quad (3.2)$$

Figure 3.5: Van der Pauw cross structure

I-V measurements

I-V characteristics of the MOS capacitors were recorded using an HP4145 Semiconductor Parameter Analyzer which is connected to a probe station similar to the one used for C-V measurements. The HP4145A is connected to an IBM personal computer for data storage. Finally data was transferred to a network of SUN workstations for further analysis and plotting.

Chapter 4

Results and Discussion

Section 4.1 concentrates on the optimum thermal budget that can be used without diffusing the boron in p^+ gate MOS devices and the limit on the gate oxide thickness in this respect. In section 4.2, we mainly look into the reliability of these devices. Time dependent dielectric breakdown analysis is done for p^+ gate capacitors and compared with those of the control devices (n^+ gated MOS capacitors).

4.1 C-V analysis

4.1.1 High-frequency C-V analysis

The penetration of boron impurity from the degenerate p^+ poly through thin gate oxide into the channel region of the MOSFET causes changes in device flatband and threshold voltage. So, boron penetration through thin gate oxides is most easily

studied by fabricating p^+ poly gate MOS capacitors on p- type silicon substrates and monitoring the C-V shifts. For this purpose, high-frequency C-V analysis was performed on the MOS capacitors. p^+ polysilicon gated MOS capacitors were formed with gate oxide thicknesses varying from 10 - 17 nm as discussed in section 3.1. MOS capacitors with n^+ doped poly silicon gates were also made as the control capacitors. The measurement frequency was 1 MHz and large area capacitors ($(300\mu m)^2$) were used. The procedure used for measurement was explained in the previous chapter. Flat-band voltage was computed following conventional analysis [26]. To study the boron penetration phenomenon, several process parameters were varied, including gate oxide thickness, rapid thermal anneal time and temperature.

Oxide thickness and substrate doping density measurements

Through the high-frequency C-V analysis, the gate oxide thickness was calculated from accumulation capacitance of a number of devices from each wafer. For n^+ poly gate capacitors, the average gate oxide thickness was 11 nm, and the average gate oxide thickness for both n^+ and p^+ poly gate capacitors are close to the values measured by ellipsometry within the error limit. The equivalent uniform doping density in the substrate, as determined from the minimum high frequency capacitance value in inversion was $4 \times 10^{15} \text{ cm}^{-3}$.

Mobile ion contamination

Since the presence of mobile ion impurities (e.g. Na^+) also causes flatband shifts, the mobile charge concentration must be kept below $10^{10} \text{ ions/cm}^2$. In order to make sure that the observed changes in the flatband voltage are not due to the mobile ions in the oxide, a few devices on each wafer were tested with temperature bias stress (TBS). Temperature bias stresses were performed at 200°C for 10 minutes at an approximate field of 9 MVcm^{-1} on these field oxide isolated MOS capacitors. As explained in the previous chapter, the electric field was applied before the ramp to the stress temperature and was not removed until the device had cooled to room temperature after the stress. The samples that showed no significant changes in any of the high frequency capacitance analysis results after the stresses, implying that the mobile ion concentration in these oxides is quite low, were taken for further analysis. On the other hand, the samples which showed significant changes in V_{fb} and V_t after stressing under the same conditions were eliminated from analysis.

Polysilicon depletion

Another issue which is very important in sub-micron CMOS devices is the uniform and heavy doping of gate polysilicon. So, below we explain briefly how this affects the device and present a one-dimensional model to study polysilicon depletion effects as a function of carrier density at the gate and oxide interface and oxide thickness suggested by Wong et al. [6]. For a MOSFET in which the gate doping is of opposite

type to the substrate, insufficient doping at the poly gate oxide interface results in depletion of the poly when the MOSFET channel is biased into inversion. It is important in polysilicon doping to minimize the depletion in polysilicon near the gate oxide interface. The space charge layer in the polysilicon effectively enlarges the insulator thickness i.e., it results in an increased "equivalent" gate oxide thickness and reduces the current drive. It can be quantified by measuring the ratio of the inversion to accumulation capacitance under quasi-static C-V conditions.

When the silicon substrate surface (MOSFET channel) is inverted,

$$\frac{C_{inv}}{C_{ox}} = \frac{1}{1 + (W_p \epsilon_{ox} / t_{ox} \epsilon_{Si})} \quad (4.1)$$

where W_p is the depletion-layer width in polysilicon. W_p can be approximated as

$$W_p \approx \frac{Q_p}{n} \quad (4.2)$$

where n is the active dopant (free carrier) concentration at the polysilicon/oxide interface and Q_p is the charge induced in the polysilicon gate electrode. Charge neutrality requires that

$$Q_p = Q_{inv} + qN_b W_{max} \quad (4.3)$$

where N_b is the substrate doping density, W_{max} is the maximum depletion-layer width in substrate, and the inversion layer charge Q_{inv} can be approximated by

$$Q_{inv} \approx C_{ox}(V_G - V_T) \quad (4.4)$$

C_{inv}/C_{ox} as a function of carrier concentration at the polysilicon/ SiO_2 was calculated from this model with $N_b = 4 \times 10^{15} \text{ cm}^{-3}$ and $V_G - V_T = 1 \text{ V}$ for 11

nm thick gate oxide. As the gate oxide thickness is scaled down, increased carrier density is required to limit the current loss due to polysilicon depletion effects. Taking into account grain-boundary and interfacial segregation where the dopants are generally considered to be electrically inactive, chemical concentrations of these dopants, as measured by SIMS, should be even higher than the indicated carrier density. According to the model, the carrier concentration at the polysilicon/ SiO_2 interface, for 11 nm gate oxide should be higher than 10^{20} cm^{-3} .

In Figure 4.1 we show quasi-static and high frequency C-V curves of boron-doped polysilicon on 11 nm gate oxide with a rapid thermal anneal cycle of 1050°C for 10 seconds. From the figure, no evidence of a decrease in capacitance at large negative gate voltages was seen. In other words, it is evident that there is no dopant depletion in the polysilicon, indicating sufficient doping at the polysilicon/gate oxide interface. This is reconfirmed by the SIMS data, which indicates that the chemical concentration of boron at the polysilicon/oxide interface is approximately $4 \times 10^{20} \text{ cm}^{-3}$. The SIMS profile of an unannealed *in-situ* boron doped, 400 nm polysilicon film is shown in figure 3. It indicates the polysilicon film has a high degree of doping uniformity. The gate oxide thickness for this device is 11 nm. Thus these *in-situ* doped gates are so heavily doped that polysilicon depletion is not a problem.

Flatband Voltage

The theoretical flatband voltage for a 10 nm gate oxide p^+ capacitor on a p-type substrate is calculated below. The band diagram for this capacitor is shown in

Figure 4.1: High frequency and quasi-static C-V curves for 11 nm thick p^+ poly gate capacitor annealed at 1050 °C for 10 seconds

Figure 4.2.

$$\text{With } N_b = 1\text{E}15 \text{ cm}^{-3}$$

$$C_{ox} = 296.7 \text{ pF}$$

$$\text{Assumed fixed oxide charge, } Q_{of} = 2\text{E}10 \text{ cm}^{-3}$$

$$\text{Thus, } V_{of} \text{ due to fixed oxide charge} = \frac{-Q_{of} A q}{C_{ox}}$$

$$V_{of} = -0.01 \text{ V}$$

Workfunction difference between gate and substrate,

$$\phi_{ms} = (E_F - E_V) \text{ in the substrate}$$

$$= \frac{E_G}{2q} - \frac{\phi_{b2} q}{q}$$

$$\phi_{b2} = \frac{KT}{q} \ln \frac{N_b}{n_i}$$

$$\text{Thus, } \phi_{ms} = 0.28 \text{ V}$$

$$V_{fb} = \frac{q\phi_{ms}}{q} + V_{of} = 0.275 \text{ V}$$

Thus, for p^+ gate with 10 nm oxide p-substrate MOS capacitor,

$$V_{fb} = 0.275 \text{ V.}$$

Similar calculations were done for an n^+ gated MOS capacitor.

In the case of 10 nm oxide p^+ gated capacitors, high-frequency C-V curves are shown in figure 4.3. These capacitors are subjected to rapid thermal anneals at different temperatures after the p^+ poly formation. The curves are presented for an as-made sample, and after 900°C, 10 second anneal.

These C-V measurements are done on a number of capacitors for each wafer. Presented V_{fb} values are the average values calculated from these measurements. As

Figure 4.2: Band diagram for a MOS capacitor with p^+ polysilicon gate and p -type Si substrate

Figure 4.3: High frequency C-V curves of 10 nm thick p^+ poly gate capacitor. The curves are shown for an as-made sample and after 900°C, 10 second anneal

can be seen in the figures, flatband voltages of the devices are still less than the expected theoretical values for initial low temperature anneals. Thus it is very clear that the initial shift in the flat band voltage in the positive direction of ≈ 0.1 V is because of the boron activation in the gate poly due to the thermal anneal, which increases the gate work function, and in turn causes V_{fb} to increase in the positive direction.

For the devices with 11 nm gate oxide, similar activation of boron in gate polysilicon causes the positive shift in V_{fb} which can be seen in Figure 4.4. No change in the flatband voltage is seen between the devices which were annealed for 20 seconds at 1100°C, and 30 seconds at the same temperature (see Figure 4.5), indicating that there is no boron diffusion and that the degenerate V_{fb} is reached.

Capacitors with 12.5 nm gate oxides were also given anneals after gate poly deposition, including RTA at 900°C and 1050°C for 10 seconds or furnace annealing at 950°C for 30 minutes in an N_2 ambient. RTA anneals at low temperatures show only activation of boron in gate polysilicon and no significant boron diffusion is apparent. But the furnace annealed sample showed a V_{fb} shift of 0.1 V from the theoretical value, which can be attributed to the boron diffusion (see Figure 4.6).

From the independent nature of flatband voltage shift at the same anneal temperature, which can be seen from Table 4.1, with the gate oxide thickness, it is evident that there is no significant boron diffusion through the gate oxide, even at the maximum rapid thermal anneal budget used here, which is 1100°C for 30 seconds.

Figure 4.4: High frequency C-V curves of 11 nm thick p^+ poly gate capacitor. The curves are shown for an as-made sample and after 900°C , 1050°C , 10 second anneals

Figure 4.5: High frequency C-V curves of 11 nm thick p^+ poly gate capacitor. The curves are shown after 20 second and 30 second anneals at 1100°C

Figure 4.6: High frequency C-V curves of 12.5 nm thick p^+ poly gate capacitor. The curves are shown for an as-made sample and after 950°C, 30 minute furnace anneal in an N_2 ambient

RTA	GATE OXIDE			
	10 nm	11 nm	12.5 nm	17 nm
900°C 10 s	0.09 V	0.13 V	0.13 V	0.08 V
1050°C 10 s		0.25	0.15	0.17
1100°C 10 s	0.18	0.31		
1100°C 20 s		0.31		
1100°C 30 s		0.31		

Table 4.1: Flatband voltage shifts for different RTA temperatures. Time is kept 10 Sec.

Similar V_{fb} shifts are seen for the capacitors with the thickest oxide in this work i.e., 17 nm, for similar anneals, which is shown in Figure 4.7. This reconfirms that one of the possible sources of the initial V_{fb} shifts could be the activation of boron in the polysilicon gate but not the diffusion of boron from the gate into the oxide.

Figure 4.8 shows flatband voltage versus anneal temperature for 10 nm and 17 nm gate oxide devices. Anneal time is 10 seconds.

poly sheet resistance values for p^+ gate capacitors before and after anneal are given in Table 4.2. Assuming active doping concentration (n) in p^+ gate changes from 10^{19} to $10^{20} /cm^3$, the possible V_{fb} shift from the dopant activation in poly is estimated as 0.18 V.

$$n = N_c 2/\pi^{0.5} F_{1/2} \frac{E_c - E_f}{KT} \quad (4.5)$$

Where N_c is the effective density of conduction band states. Thus the change in sheet resistance value after the anneal reflects the observed V_{fb} shifts.

In Figure 4.9, C-V curves are plotted for n^+ poly gated PMOS capacitors with no anneal and after annealing at 1050°C for 10 seconds. Small V_{fb} shift is seen for that high thermal budget anneal. This small positive V_{fb} shift seen in n^+ gate capacitors suggests another possible source of observed V_{fb} shifts in p^+ gate capacitors, which is annealing of oxide fixed positive charge. Since the presence of fixed positive charge in the oxide gives rise to a negative shift in the C-V characteristics.

Figure 4.7: High frequency C-V curves of 17 nm thick p^+ poly gate capacitor. The curves are shown for an as-made sample and after 900°C, 1050°C, 10 second anneals

Figure 4.8: Flatband voltage shifts are shown for 10 nm and 17 nm thick p^+ gate capacitor at different RTA anneals. Anneal time is 10 seconds.

	Sheet resistance $\Omega/\square$	
	no RTA	RTA = 1100C, 10Sec
$t_{ox} = 10nm$	253.7	94.2
$t_{ox} = 10nm$	240.5	69.5

Table 4.2: Poly sheet resistance values for p^+ gate capacitors before and after RTA.

Figure 4.9: High frequency C-V curves of 11 nm thick n^+ poly gate capacitor. The curves are shown for an as-made sample and after 1050°C, 10 second anneal

Thus, first set of experiments, which were devoted to the characterization of the maximum thermal budget that a thin (10 nm) p^+ gate thermal oxide can withstand, show no significant flatband voltage shifts even at the maximum thermal budget (RTA, at 1100°C for 30 seconds) used in this work, which might be required to remove damage from the source/drain implants in a typical CMOS process, thus indicating no significant boron diffusion.

4.1.2 Quasi-static C-V analysis

In the first set of experiments, the flatband voltage (V_{fb}) determined by the high frequency C-V technique is used to provide an initial measure of the maximum allowable thermal budget. To investigate the boron penetration phenomenon further, quasi-static C-V analysis was performed on all of the above samples to measure the interface state density, D_{it} . Boron diffusion from the gate electrode through thin gate oxide during furnace annealing has been associated with increases in fast surface state density [27] [18] [13].

Interface Trap Density

Figure 4.10 show the quasistatic C-V curves of 12.5 nm gate oxide p^+ capacitors after different anneal cycles. They show no signs of poly depletion in the gate electrode. By comparison of quasi-static and high-frequency C-V curves, the interface state densities (D_{it}) are computed [26] for all the capacitors and typical curves are plotted in Figure 4.11.

Figure 4.10: High frequency and quasi-static C-V curves for 12.5 nm thick p^+ poly gate capacitor annealed at 1050°C for 10 seconds

Figure 4.11: Interface trap densities(D_{it}) versus position in the bandgap calculated from high frequency and quasi-static C-V curves for 11 nm thick p^+ poly gate capacitor annealed at 1050°C for 10 seconds

Mid gap interface state density does not reveal any strong degradation associated with boron diffusion. It remains nearly constant (5 to $7 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$) over all the range of rapid thermal anneal cycles used in this work. Mid-gap interface state density vs. RTA temperature for 10 seconds anneal is plotted in the case of an 11 nm oxide p^+ capacitor in Figure 4.12. On the other hand, mid-gap D_{it} shows a slight decrease in the case of 12.5 nm gate oxide p^+ capacitor when it is given a 950°C , 30 minute furnace anneal in N_2 . This could be because of the generation of interface traps by the following mechanism proposed in [28].

The activated boron in the electrode can be negatively charged by accepting an electron from a hydrogen atom which is contained in the polysilicon electrode by some means, and the hydrogen atom becomes positively charged. Accordingly, the hydrogen ion combines with the activated boron ion through coulombic attraction instead of covalent bonds. Under positive bias temperature stressing, the hydrogen is separated from the boron ion, and moves toward the SiO_2/Si interface. The hydrogen ion at the SiO_2/Si interface reacts with $O=Si-H$ or $Si=Si-H$ bonds, and generates $=Si^+$. The $=Si^+$ captures an electron injected from the Si substrate and an interface trap (Si) is generated. This model also explains our observation that n^+ gated capacitor showing lower midgap D_{it} values than p^+ gated capacitors, which is also observed by previous researchers in ion implanted gate MOS devices. Thus higher D_{it} values for the p^+ gate devices, can be attributed to hydrogen (H) atoms [2,3].

By annealing in dry N_2 , the concentration of the H atoms is reduced, thus

Figure 4.12: Mid-gap interface trap densities(D_{it}) versus RTA temperature. 10 second anneal. 11nm oxide

lower values of D_{it} should be obtained.

4.2 Reliability of thin gate oxides with p^+ polysilicon gates

In this section, the reliability of pure gate oxide in boron in-situ doped p^+ polysilicon gate MOS capacitors is investigated. The dependence of gate oxide reliability on the boron penetration degree and the gate oxide thickness (t_{ox}) is presented. The first part of this section concentrates on the time zero dielectric breakdown characteristics and the latter part presents the time dependent dielectric breakdown characteristics.

4.2.1 Time zero dielectric breakdown characteristics

The initial measurements performed in this aspect were to determine whether the basic quality of the grown interfaces and dielectrics was acceptable. That is, the gate dielectric must have suitably high breakdown fields and suitably low leakage currents. For this purpose n^+ polysilicon gated p-substrate MOS capacitors with 11 nm thick gate oxide were examined. Also, grown interface quality can be measured by the effective barrier height at the oxide to silicon interface to electrons in the conduction band of the substrate. The barrier height can be determined from the Fowler-Nordheim tunneling regime of the I-V curves.

Current-voltage (I-V) curves of both n^+ polysilicon gated and p^+ polysilicon

gated capacitors were measured by slowly sweeping gate voltage from 0 to large negative values for $(300\mu m)^2$ capacitors using an HP4145A Semiconductor Parametric Analyzer until destructive breakdown was observed. The top plate of the capacitor was biased negatively to place the p-type substrate in accumulation.

A typical gate oxide I-V curve for an n^+ polysilicon gated capacitor is shown in Figure 4.13. A breakdown field of 14 MVcm^{-1} can be inferred from this figure. This was typical of the n^+ devices measured. Furthermore, since the gate oxide yield and the time dependent reliability of an integrated circuit is defect related, statistical analysis is necessary in order to predict the yield and lifetime of actual oxide devices in a integrated circuit. Thus for estimating the defect related breakdown in gate oxide, breakdown characteristics were measured using samples with large gate area $((300\mu m)^2)$. The distribution of the gate oxide breakdown fields for the n^+ poly gate MOS capacitors is shown in Figure 4.14.

The lower field mode of the distribution is caused by small defects in the film such as pin holes, inclusions and particulates. Since the electric effect of the defect is strongly dependent on its extent (size and/or location), the large standard deviation of the low-field mode of the distribution is explained. These low field failures accounted for approximately less than 20% of the n^+ poly gate capacitors tested on the same wafer.

The main mode of the distribution is a result of the intrinsic failure of the dielectric. If we define the intrinsic breakdown regime as being from 14.5 MVcm^{-1} to 15.5 MVcm^{-1} , the mean intrinsic breakdown field is found to be approximately

Figure 4.13: Current-voltage characteristics for 11 nm thick n^+ gate oxide subjected to 1050°C 10s RTA

Figure 4.14: Breakdown voltage distribution for 11 nm thick n^+ gate oxide subjected to 1050°C 10 s RTA

15 MVcm^{-1} (See Figure 4.14). The dominant factor in the variance of the intrinsic regime breakdown field is the use of a fixed oxide thickness for each wafer in the calculation of breakdown fields. The actual variation of thickness over a wafer results in an effective variation in calculated breakdown field.

Figures 4.15 and 4.16 show the corresponding typical I-V and breakdown field distribution curves for p^+ poly gate capacitors.

The number of low field failures, however, appears to be higher than for an n^+ poly gate accounting for more than 40% of the total number of devices tested on the same wafer. The mean intrinsic breakdown field for these p^+ capacitors was 12 MVcm^{-1} . The higher number of low field failures for the p^+ gated capacitors compared to the n^+ gated ones, is perhaps due to the diffusion of boron into the gate oxide.

Average breakdown fields were found to be significantly lower for p^+ polygate capacitors (12 MVcm^{-1}) than for n^+ gates (15 MVcm^{-1}). p^+ gated capacitors also showed hysteresis in gate I-V characteristics compared to n^+ gated ones, presumably as the result of charge trapping in the oxide (see Figure 4.17 and Figure 4.18).

4.2.2 Time Dependent Dielectric Breakdown Characteristics

This section deals with the time dependent dielectric breakdown (TDDB) characteristics of the p^+ polysilicon gate MOS capacitors. TDDB has been reported as the

Figure 4.15: Current-voltage characteristics for 11 nm thick p^+ gate oxide subjected to 1050°C 10s RTA

Figure 4.16: Breakdown voltage distribution for 11 nm thick p^+ gate oxide subjected to 1050°C 10 s RTA

Figure 4.17: Hysteresis in I-V characteristics for p^+ gate capacitor. 11 nm oxide, 1050°C 10 s RTA

Figure 18: I-V characteristics for n^+ gate capacitor. 11 nm oxide, 1050°C 10 s RTA

primary failure mode of today's MOS devices.

Gate oxide lifetime (τ) was determined from time to breakdown (T_{bd}) at a particular electric field for oxide (E_{ox}) by measuring the time dependent dielectric characteristics. Since in intrinsic breakdown time-lifetime measurements, very small area capacitors are used ($(20\mu m)^2$), very little statistical variation of T_{bd} at any one applied electric field was observed. Hence, only a few measurements at each electric field are sufficient.

In order to project the lifetime of oxides under low operating fields, the concept of an "electric field acceleration factor" β is widely used [29]. This extrapolation scheme assumes a linear relationship between log of time to breakdown, $\log(T_{bd})$ and the inverse of applied stress field, E_{ox}^{-1} ; the tangential slope of $\log(T_{bd})$ vs E_{ox} curve is defined as β [30] [18] [31]. Thus from the extrapolation of the $\log(T_{bd})$ vs. $1/E_{ox}$ relationship, T_{bd} at an oxide field of 4.5 MVcm^{-1} , was determined. In Figure 4.19, current vs. time is plotted at a constant voltage. The decrease in the current is because of the charge trapping in the oxide causing eventual breakdown. The dependence of time to failure on the effective electric field in TDDB of gate oxides for p^+ and n^+ gate capacitors are shown in Table 4.3.

Figure 4.20 shows the dependence of gate oxide lifetime (τ) on T_{ox} . From Figure 4.20, it is very clear that though the boron penetration is not obvious through V_{fb} and D_{it} values, it does appear in the degradation in the reliability of the gate oxide.

Figure 4.19: Current versus time for 12.5 nm thick p^+ gate oxide subjected to a constant voltage stress

	E_{ox} MV/cm	$\log(t_{bd})$ Sec
n^+ gate $t_{ox} = 11nm$	12.7	8×10^3
	13.2	1×10^3
	14.1	3×10^1
p^+ gate $t_{ox} = 11nm$	9.6	6.2×10^3
	12.3	3×10^1
	12.7	1.3×10^1
p^+ gate $t_{ox} = 12.5nm$	13.6	9.3×10^1
	14	3×10^1
	14.4	1.2×10^1

Table 4.3: The dependence of time to failure on the effective electric field in TDDB.

Figure 4.20: Extrapolated time-to-breakdown for 4.5 MVcm^{-1} field for p^+ and n^+ gate capacitors, as a function of oxide thickness

The lifetimes (τ) of the p^+ polysilicon gated capacitors are many orders of magnitude less than those of n^+ conventional polysilicon gate capacitors. In Figure 4.20, gate oxide lifetimes (τ) are shown for two different gate oxide thicknesses, T_{ox} , with the same RTA anneal cycle of 1050° C for 10 seconds, together with the lifetime of the n^+ control gate oxide.

Also, the gate oxide degradation due to boron penetration, besides breakdown characteristics were investigated. Leakage current in the low gate voltage region was compared for capacitors with different T_{ox} , which had undergone the same anneal cycles. Thin gate oxides show significant leakage current at low gate voltages compared to the thick oxides, see Figure 4.21. When all three gate oxides were subjected to the same anneal cycle, though they show approximately the same amount of shift in the flatband voltage, the reliability of thinner oxides shows larger degradation. This can be explained by the mechanism suggested by Ken-ichi et. al. [31]. The gate oxide contains a large amount of strained Si-O bonds near the oxide/silicon interface. When even a small amount of boron is incorporated into this strained layer, it degrades the reliability of the oxide by forming charge trapping centers. This is more severe in the thinner oxide since this strained layer occupies a larger part of the oxide.

However, even in the case of highest anneal cycle, no significant degradation of early stage breakdown characteristics was seen for the thinnest oxide, used in this work (10 nm), even at RTA temperatures up to 1050°C, for times up to 10 seconds. Thus we can conclude that the early stages of boron diffusion into SiO_2 do not lead

Figure 4.21. Current-voltage characteristics for gate oxides subjected to 1050°C 10 s RTA- for p^+ polygate capacitors

to clear interfacial modifications such as the appearance of negative fixed charges or interface states, but dielectric strength and TDDB were lower for the p^+ gated devices than for the n^+ gated controls. However, they should still be acceptable for circuit applications.

Chapter 5

Conclusions

MOS capacitors with n^+ - and p^+ - doped polysilicon gates were fabricated on p-type (100) silicon substrates, with gate oxide thicknesses ranging from 10 nm to 17 nm. For the formation of p-type gate electrodes, *in-situ* doped p-poly was deposited at 560°C by LPCVD. The capacitors were then subjected to various annealing conditions. The first part of this work concentrates on the analysis of flatband voltage shifts and interface state densities, which can be viewed as primary measures of boron penetration. The second part is concerned mainly with the reliability of gate oxides with p^+ polysilicon gates i.e. more subtle effects of boron penetration.

In the first set of experiments, the flatband voltage (V_{fb}) determined by the high-frequency C-V technique is used to evaluate the boron penetration, which is measured by the shift of V_{fb} from the initial value V_{fb0} . For initial RTA anneals, flatband voltages are still less than the theoretical values for all the p^+ gate ca-

capacitors. This indicates that the V_{fb} shifts after these anneals could be because of the activation of boron in gate polysilicon. Another possible source of V_{fb} shifts is annealing of oxide fixed positive charge. Even after an anneal cycle of 1050°C, 10 seconds, 10 nm - gate oxide capacitors did not show any significant boron diffusion. Flatband voltage shows no dependence on the gate oxide thickness.

To investigate the boron penetration phenomenon further, the interface state densities (D_{it}) are measured from the comparison of quasi-static and high frequency C-V curves for all the capacitors. Midgap interface state densities do not reveal any strong degradation associated with boron diffusion. They remain nearly constant even at the highest anneal cycle used in this work (1050°C, 10 seconds). On the other hand, for 12.5 nm - gate oxide, midgap D_{it} shows a slight decrease following a 950°C, 30 minute furnace anneal in N_2 . This can be attributed to hydrogen atoms, contained in the gate. This also can explain our observation that n^+ gate capacitors consistently show lower D_{it} values than p^+ gate capacitors. Thus early stages of boron diffusion into the gate oxide do not lead to clear interfacial modifications such as the appearance of negative fixed charges or interface states.

The strength of the gate dielectric was tested by slowly sweeping V_G from 0 to large negative values using an HP4145A Semiconductor Parameter Analyzer until destructive breakdown was observed. These breakdown measurements were done on large area capacitors. p^+ gate capacitors with 10 nm- thick gate oxide show lower breakdown field (12 MVcm^{-1}) than that of n^+ gates (15 MVcm^{-1}). p^+ gated capacitors also showed hysteresis in gate I-V characteristics which can be attributed

to the charge trapped in the oxide.

The time to breakdown at 4.5 MV/cm was extrapolated from time-dependent dielectric breakdown measurements done at high fields. p^+ gate devices show lower gate oxide lifetimes when compared to n^+ gate devices. It is observed that gate oxide reliability is degraded in p^+ poly gate capacitors when the oxide thickness is reduced. However, even the p^+ gated capacitors with the thinnest gate oxides had acceptable TDDB for circuit applications.

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PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
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Appendix I

P+ POLY GATE CAPACITORS

STARTING MATERIAL: 24 wafers 1.8-2.5 Ω cm p (100)

1. FIELD OXIDATION

include test wafer #: _____

a) RCA clean

b) Oxidation tube temperature 1100°C

	5 min preheat	O ₂
2" every	6 sec push	O ₂
	10 min oxidation	dry O ₂
	180 min oxidation	O ₂ + pyrogenic H ₂ O
	30 min oxidation	O ₂ + 2.5% HCl
	40 min anneal	N ₂
2" every	15 sec pull	N ₂
	10 min cool	N ₂

target thickness: 1.0 μ m

thickness measured on test wafer # _____: _____ μ m

2. DEVICE WELL P.E. mask CU-060-01

a) apply, prebake, expose, develop, postbake NEGATIVE PR

b) etch in buffered HF until hydrophobic

3 GATE OXIDATION (wafers 5,6,7,8,9,10)

include one test wafer #_____

a) RCA clean

b) Oxidation tube temperature 900°C

	5 min preheat	N ₂
2" every	6 sec push	N ₂
	10 min pre-heat	N ₂
	20 min oxidation	O ₂
	10 min anneal	N ₂
2" every	15 sec pull	N ₂
	10 min cool	N ₂

target thickness: 10 nm

thickness measured on test wafer #_____: _____ nm

thickness measured on test wafer #_____: _____ nm

4 BORON DOPED POLYSILICON DEPOSITION (wafers 5,6,7,8)

temperature: 560°C
 B₂H₂/SiH₄ flow ratio: 12 x 10⁻³
 B₂H₂ flow: 0.877 sccm (29.2%)
 SiH₄ flow: 73.122 sccm (35.5%)
 time: 70 min
 target thickness: 350 nm

5 PHOSPHOROUS DOPED POLYSILICON DEPOSITION (wafers 9,10)

temperature: 625°C
 SiH₄: 35.0%
 SiH₄/PH₃: 26.9%
 time : 60 min
 target thickness: 150 nm

6 GATE P.E. mask CU-060-02

a) apply, prebake, expose, develop, postbake POSITIVE PR

b) wet etch in poly etch

estimated etch time: 50 sec

actual etch times:

c) strip PR in Caro's acid

7. POLYSILICON RTA

a) RCA clean (no HF)

b) RTA-

END

31-05-95

FIN