PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

National Library
of Canada

Acquisitions and
Bibliographic Services Branch

395 Wellington Street
Ottawa, Ontario
K1A 0N4

Bibliothèque nationale
du Canada

Direction des acquisitions et
des services bibliographiques

395, rue Wellington
Ottawa (Ontario)
K1A 0N4

Your file Votre référence

Our file Notre référence

NOTICE

The quality of this microform is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Reproduction in full or in part of this microform is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30, and subsequent amendments.

AVIS

La qualité de cette microforme dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

La reproduction, même partielle, de cette microforme est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30, et ses amendements subséquents.

Heterostructure Varactors on *InP* and *GaAs* for Millimeter-Wave Frequency Triplers

by

Kathiravan Krishnamurthi

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements
for the degree of
Doctor of Philosophy

Ottawa-Carleton Institute for Electrical Engineering,
Department of Electronics,
Carleton University,
Ottawa, Ontario, Canada

January 6, 1995

© Kathiravan Krishnamurthi 1994

National Library
of Canada

Acquisitions and
Bibliographic Services Branch

395 Wellington Street
Ottawa, Ontario
K1A 0N4

Bibliothèque nationale
du Canada

Direction des acquisitions et
des services bibliographiques

395, rue Wellington
Ottawa (Ontario)
K1A 0N4

Your file Votre référence

Our file Notre référence

**THE AUTHOR HAS GRANTED AN
IRREVOCABLE NON-EXCLUSIVE
LICENCE ALLOWING THE NATIONAL
LIBRARY OF CANADA TO
REPRODUCE, LOAN, DISTRIBUTE OR
SELL COPIES OF HIS/HER THESIS BY
ANY MEANS AND IN ANY FORM OR
FORMAT, MAKING THIS THESIS
AVAILABLE TO INTERESTED
PERSONS.**

**L'AUTEUR A ACCORDE UNE LICENCE
IRREVOCABLE ET NON EXCLUSIVE
PERMETTANT A LA BIBLIOTHEQUE
NATIONALE DU CANADA DE
REPRODUIRE, PRETER, DISTRIBUER
OU VENDRE DES COPIES DE SA
THESE DE QUELQUE MANIERE ET
SOUS QUELQUE FORME QUE CE SOIT
POUR METTRE DES EXEMPLAIRES DE
CETTE THESE A LA DISPOSITION DES
PERSONNE INTERESSEES.**

**THE AUTHOR RETAINS OWNERSHIP
OF THE COPYRIGHT IN HIS/HER
THESIS. NEITHER THE THESIS NOR
SUBSTANTIAL EXTRACTS FROM IT
MAY BE PRINTED OR OTHERWISE
REPRODUCED WITHOUT HIS/HER
PERMISSION.**

**L'AUTEUR CONSERVE LA PROPRIETE
DU DROIT D'AUTEUR QUI PROTEGE
SA THESE. NI LA THESE NI DES
EXTRAITS SUBSTANTIELS DE CELLE-
CI NE DOIVENT ETRE IMPRIMES OU
AUTREMENT REPRODUITS SANS SON
AUTORISATION.**

ISBN 0-315-98478-3

Name Kathiravan Krishnamurthi

Dissertation Abstracts International is arranged by broad, general subject categories. Please select the one subject which most nearly describes the content of your dissertation. Enter the corresponding four-digit code in the spaces provided.

Electronics and Electrical

SUBJECT TERM

0544

U·M·I

SUBJECT CODE

Subject Categories

THE HUMANITIES AND SOCIAL SCIENCES

COMMUNICATIONS AND THE ARTS

Architecture 0729
Art History 0377
Cinema 0900
Dance 0378
Fine Arts 0357
Information Science 0723
Journalism 0391
Library Science 0399
Mass Communications 0708
Music 0413
Speech Communication 0459
Theater 0465

EDUCATION

General 0515
Administration 0514
Adult and Continuing 0516
Agricultural 0517
Art 0273
Bilingual and Multicultural 0282
Business 0688
Community College 0275
Curriculum and Instruction 0727
Early Childhood 0518
Elementary 0524
Finance 0277
Guidance and Counseling 0519
Health 0680
Higher 0745
History of 0520
Home Economics 0278
Industrial 0521
Language and Literature 0279
Mathematics 0280
Music 0522
Philosophy of 0998
Physical 0523

Psychology 0525
Reading 0535
Religious 0527
Sciences 0714
Secondary 0533
Social Sciences 0534
Sociology of 0340
Special 0529
Teacher Training 0530
Technology 0710
Tests and Measurements 0288
Vocational 0747

LANGUAGE, LITERATURE AND LINGUISTICS

Language
 General 0679
 Ancient 0289
 Linguistics 0290
 Modern 0291
Literature
 General 0401
 Classical 0294
 Comparative 0295
 Medieval 0297
 Modern 0298
 African 0316
 American 0591
 Asian 0305
 Canadian (English) 0352
 Canadian (French) 0355
 English 0593
 Germanic 0311
 Latin American 0312
 Middle Eastern 0315
 Romance 0313
 Slavic and East European 0314

PHILOSOPHY, RELIGION AND THEOLOGY

Philosophy 0422
Religion
 General 0318
 Biblical Studies 0321
 Clergy 0319
 History of 0320
 Philosophy of 0322
 Theology 0469

SOCIAL SCIENCES

American Studies 0323
Anthropology
 Archaeology 0324
 Cultural 0326
 Physical 0327
Business Administration
 General 0310
 Accounting 0272
 Banking 0770
 Management 0454
 Marketing 0338
Canadian Studies 0385
Economics
 General 0501
 Agricultural 0503
 Commerce-Business 0505
 Finance 0508
 History 0509
 Labor 0510
 Theory 0511
Folklore 0358
Geography 0366
Gerontology 0351
History
 General 0578

Ancient 0579
Medieval 0581
Modern 0582
Black 0328
African 0331
Asia, Australia and Oceania 0332
Canadian 0334
European 0335
Latin American 0336
Middle Eastern 0333
United States 0337
History of Science 0585
Law 0398
Political Science
 General 0615
 International Law and Relations 0616
 Public Administration 0617
Recreation 0814
Social Work 0452
Sociology
 General 0626
 Criminology and Penology 0627
 Demography 0938
 Ethnic and Racial Studies 0631
 Individual and Family Studies 0628
 Industrial and Labor Relations 0629
 Public and Social Welfare 0630
 Social Structure and Development 0700
 Theory and Methods 0344
Transportation 0709
Urban and Regional Planning 0999
Women's Studies 0453

THE SCIENCES AND ENGINEERING

BIOLOGICAL SCIENCES

Agriculture
 General 0473
 Agronomy 0285
 Animal Culture and Nutrition 0475
 Animal Pathology 0476
 Food Science and Technology 0359
 Forestry and Wildlife 0478
 Plant Culture 0479
 Plant Pathology 0480
 Plant Physiology 0817
 Range Management 0777
 Wood Technology 0746
Biology
 General 0306
 Anatomy 0287
 Biostatistics 0308
 Botany 0309
 Cell 0379
 Ecology 0329
 Entomology 0353
 Genetics 0369
 Limnology 0793
 Microbiology 0410
 Molecular 0307
 Neuroscience 0317
 Oceanography 0416
 Physiology 0433
 Radiation 0821
 Veterinary Science 0778
 Zoology 0472
Biophysics
 General 0786
 Medical 0760

EARTH SCIENCES

Biogeochemistry 0425
Geochemistry 0996

Geodesy 0370
Geology 0372
Geophysics 0373
Hydrology 0388
Mineralogy 0411
Paleobotany 0345
Paleoecology 0426
Paleontology 0418
Paleozoology 0985
Palynology 0427
Physical Geography 0368
Physical Oceanography 0415

HEALTH AND ENVIRONMENTAL SCIENCES

Environmental Sciences 0768
Health Sciences
 General 0566
 Audiology 0300
 Chemotherapy 0992
 Dentistry 0567
 Education 0350
 Hospital Management 0769
 Human Development 0758
 Immunology 0982
 Medicine and Surgery 0564
 Mental Health 0347
 Nursing 0569
 Nutrition 0570
 Obstetrics and Gynecology 0380
 Occupational Health and Therapy 0354
 Ophthalmology 0381
 Pathology 0571
 Pharmacology 0419
 Pharmacy 0572
 Physical Therapy 0382
 Public Health 0573
 Radiology 0574
 Recreation 0575

Speech Pathology 0460
Toxicology 0383
Home Economics 0386

PHYSICAL SCIENCES

Pure Sciences
 Chemistry
 General 0485
 Agricultural 0749
 Analytical 0486
 Biochemistry 0487
 Inorganic 0488
 Nuclear 0738
 Organic 0490
 Pharmaceutical 0491
 Physical 0494
 Polymer 0495
 Radiation 0734
 Mathematics 0405
 Physics
 General 0605
 Acoustics 0986
 Astronomy and Astrophysics 0606
 Atmospheric Science 0608
 Atomic 0748
 Electronics and Electricity 0607
 Elementary Particles and High Energy 0798
 Fluid and Plasma 0759
 Molecular 0609
 Nuclear 0610
 Optics 0752
 Radiation 0756
 Solid State 0611
 Statistics 0463
Applied Sciences
 Applied Mechanics 0346
 Computer Science 0984

Engineering
 General 0537
 Aerospace 0538
 Agricultural 0539
 Automotive 0540
 Biomedical 0541
 Chemical 0542
 Civil 0543
 Electronics and Electrical 0544
 Heat and Thermodynamics 0348
 Hydraulic 0545
 Industrial 0546
 Marine 0547
 Materials Science 0794
 Mechanical 0548
 Metallurgy 0743
 Mining 0551
 Nuclear 0552
 Packaging 0549
 Petroleum 0765
 Sanitary and Municipal 0554
 System Science 0790
 Geotechnology 0428
 Operations Research 0796
 Plastics Technology 0795
 Textile Technology 0994

PSYCHOLOGY

General 0621
Behavioral 0384
Clinical 0622
Developmental 0620
Experimental 0623
Industrial 0624
Personality 0625
Physiological 0989
Psychobiology 0349
Psychometrics 0632
Social 0451

Carleton University
Ottawa, Canada K1S 5J7

1912-1913

Thesis contains black and white and/or coloured graphs/tables/photographs which when microfilmed may lose their significance. The hardcopy of the thesis is available upon request from Carleton University Library.

The undersigned recommend to the Faculty of Graduate Studies and Research
acceptance of the thesis

**"Heterostructure Varactors on InP and GaAs for Millimeter-Wave
Triplers"**

submitted by Kathiravan Krishnamurthi, B.E. (Hons), M.Sc.,
in partial fulfillment of the requirements for the
degree of Doctor of Philosophy.

Prof. R.G. Harrison
Thesis Supervisor

Prof. C.H. Chan
Chairman,
Department of Electronics

Dr. P.L. Ntaky
Harris Farinon Canada
External Examiner

Ottawa-Carleton Institute for Electrical Engineering,
Department of Electronics
Faculty of Engineering
Carleton University
December 21, 1994

Acknowledgements

I gratefully acknowledge the immense investment of time and patience by my supervisor, Professor Robert G. Harrison during the course of my doctoral research work. It was characteristically done with a friendly attitude, helpful suggestions and very supportive words of encouragement, particularly at the most difficult of times. The assistance with a myriad of problems at the outset of my thesis by Dr. H.C. Liu is also acknowledged accordingly. His advice in the matter of heterostructure barriers and provision of facilities for the temperature measurements on *GaAs* devices was indispensable to the ultimate success of my research work. My thanks are also extended to Mr. Jim Thompson of NRC for his assistance in wire bonding devices. Dr. Margaret Buchanan of NRC is thanked for help with *GaAs* device processing. Dr. Anthony SpringThorpe of BNR grew the *GaAs* wafers 1205 and 1206. Dr. Z. Wasilewski of NRC grew the wafers 1411 and 1412. I am grateful to Dr. M. Cuhaci and Mr. Hien DoKy of CRC for providing measurement facilities and help with *GaAs* device characterization.

Further thanks go to Mr. John Ovey, Manager of Philips Microwave for all the assistance extended to me when I approached him in 1992 for some help with processing microwave devices at Philips in Hazelgrove, UK. John applied for a grant

from Defence Research Establishment, Malvern, UK and secured money for the InP device work. Dr. Chris Rogers at Philips and Mr Gary Smith helped with the device processing and mounting samples into packages. I thank them also for their warm hospitality when I visited them in March 1993 and December 1993. I wish to also express my appreciation to Prof. Erik Kollberg of Chalmers University for affording me the opportunity to visit Gotenberg, Sweden where I spent 45 days during which time I had the opportunity to interact with Dr. Svein M. Nilsen. I shared my research results with Svein and he kindly assisted me with the multiplier analysis program. Prof. Kollberg paid for my accommodation in Gothenberg.

I wish to thank Mr. Erik Boch, Senior Design Engineer with Lockheed Canada, Kanata for sharing his experience in designing planar triplers. The tripler was tested at Lockheed.

To my parents, N. Krishnamurthi and G. Packiam and grandfather, V.R. Govindasamy go my deepest gratitude for their financial and moral support. My brother Ilango's words of encouragement were likewise of significant assistance. To them, I dedicate this thesis.

Abstract

A recently proposed device for frequency multiplication called a single barrier varactor (SBV) is the research focus of this thesis. The device has attractive features such as frequency tripling without second harmonic idler and bias circuits. But early SBVs suffered from excessive leakage currents and the triplers based on SBVs had reduced efficiencies. Various structures on *GaAs* and *InP* are grown by molecular beam epitaxy and characterized by microwave measurements. A simple large signal model for the device yields closed form results for tripler efficiency and terminations. The devices proposed and implemented in this thesis are shown to overcome the problems of leakage currents, output power saturation due to resistive multiplication and low power output of the earlier reports. A 40 GHz planar tripler has been designed on a stacked heterostructure varactor and tested successfully to prove the usefulness of the improved devices in a millimeter-wave source.

Contents

1	Introduction	1
1.1	Motivation	1
1.2	Objectives	3
1.3	Outline of the Thesis	4
2	Heterostructure-Barrier Varactors for Frequency Tripling	6
2.1	Introduction	6
2.2	Heterojunction Device Fundamentals	8
2.2.1	Materials for Heterojunctions	8
2.2.2	Lattice Match	9
2.2.3	MBE Growth	10
2.2.4	Direct and Indirect Band Offsets	12
2.3	Varactors: A General Description and Review	14
2.3.1	Electrical Equivalence of Depletion Varactors	18

2.3.2	Large Signal Cut-Off Frequency	18
2.4	Principles of a Single-Barrier Varactor	19
2.4.1	Electrostatics of a Single Barrier Varactor	20
2.5	Single Barrier Varactors: Problems and Solutions	23
2.5.1	Reasons for High Leakage Currents	23
2.5.2	Proposed New Structures and Preliminary Results	25
2.5.3	Other Approaches and Shortcomings	28
2.6	Heterostructure Varactors on <i>InP</i>	31
2.6.1	Output Saturation and Stacked Devices	31
2.6.2	Stacked Varactors: Advantages	32
2.6.3	Previous Studies and the Current Approach	33
2.6.4	Conclusion	36
2.7	Summary	37
3	Growth and Processing of the Varactor Devices	38
3.1	MBE Growth of Varactors	38
3.2	Processing of the Wafers	40
4	Tripler Analysis and Design	42
4.1	Cubic Model (CM) for SBVs	43

4.1.1	Analysis of Triplers	43
4.2	Computer-Based Multiplier Analysis	47
4.2.1	General problem	48
4.2.2	Reflection Algorithm and Multiplier Analysis	49
4.2.3	Input Impedance	54
4.2.4	Absorbed Power	54
4.2.5	Output Power	54
4.2.6	Conversion Efficiency	54
4.3	Illustrative Example: Comparing HB and CM	55
4.4	A 39 GHz Planar Tripler Design	56
4.4.1	Conceptual Design of a Planar Z Multiplier	57
4.4.2	Design Steps and Details	59
4.5	Summary	62
5	Experimental Results and Discussions	65
5.1	Barrier Height Measurements of <i>GaAs</i> Varactors	66
5.1.1	Barrier Height and Activation Energy	66
5.1.2	Measurement Technique	66
5.1.3	Measurement Results	69

5.1.4	Discussion	70
5.2	Device Characterization	72
5.2.1	Microwave Measurement of <i>GaAs</i> Devices	73
5.2.2	Characterization of Packaged Devices on <i>InP</i>	76
5.3	Effective Barrier Width and $C(v)$ Measurements	85
5.4	<i>GaAs</i> Varactors: Some Guidelines	88
5.5	Large-Signal Tripler Simulations	89
5.5.1	Output Power Saturation in Leaky SBVs	90
5.6	Single and Stacked-Varactor Triplers on <i>InP</i>	97
5.7	Ka Band Planar Tripler Experiment	103
5.7.1	Experimental Results	104
5.7.2	Discussion	105
6	Summary of Contributions and Recommendations	108
6.1	Summary	108
6.2	Recommendations	109
A	SIMS Measurement on <i>GaAs</i> Wafers	121
B	Series Resistance of Upright Devices	124

C Touchstone File-Passive Circuit Design for a 39 GHz Planar Tripler 127

D Determination of S4 Package Parasitics 136

List of Figures

2.1	Compilation of minimum bandgap versus lattice constant data [Swa92].	9
2.2	Lattice mismatch and critical thickness for dislocation.	10
2.3	A schematic diagram to show an MBE set up.	11
2.4	$E - k$ diagram of $GaAs$ [Pie87].	13
2.5	Schematic diagram of a generic semiconductor varactor [FE92].	16
2.6	Schematic diagram of SBV.	17
2.7	Schematic diagram of bbBNN [FE92].	17
2.8	Equivalent circuit of a generalized varactor.	19
2.9	Energy band diagram of a single barrier varactor showing, accumulation, barrier and depletion potentials.	20
2.10	The calculated $C(v)$ curve of a QBV with $N_d = 10^{17} \text{ cm}^{-3}$, $w = 200 \text{ \AA}$ and $A = \pi \times 10\mu m \times 10\mu m$	22

2.11	Energy band profile of $Al_{0.7}Ga_{0.3}As/GaAs$ heterojunction barrier indicating competing $\Gamma - \Gamma$ and $\Gamma - X$ channels for electronic transport.	24
2.12	$GaAs$ varactor MBE layers. Four variants differ in the barrier and spacer design as outlined in Table 2.1.	26
2.13	Conduction band energy profile of various structures. 1206 has $InGaAs$ spacer-wells while the 1411/1412 Γ profile shows a chair-like profile. . . .	27
2.14	Measured current densities of the four varactors 1205, 1206, 1411, and 1412. The layers are indicated in Table 2.1 and Figure 2.12.	30
2.15	MBE layers of stacked InP varactor. The single barrier varactor has the same barrier and spacer layers and the depletion layer is $1\ \mu m$ thick. . . .	34
2.16	$I(v)$ curves of single and stacked varactor on InP . (a) A $61\ \mu m$ diameter single barrier device (b) A $40\ \mu m$ diameter stacked varactor device. Scale: Y axis- $100\ \mu A/div$, X axis- $2\ V/div$	35
2.17	Schematic diagram of a p^+n junction varactor diode stack [CCC+86]. . .	36
3.1	Photomicrograph of processed $GaAs$ varactor showing the device ($120\ \mu m$ by $120\ \mu m$ square mesa).	40

3.2	Photomicrograph of processed <i>InP</i> stacked varactor with the integral heat sink. Device wafers were processed by Philips Microwave, Hazelgrove, UK (42 μm diameter circular mesa).	41
4.1	Our proposed cubic charge-voltage model for symmetric varactors. The charge for zero bias is zero and the function is chosen to represent the depletion charge in the varactor. See Equation (4.1).	44
4.2	The $C(v)$ generated from the charge-voltage model. Note the symmetric $C(v)$ characteristics. For a given zero-bias capacitance, the $C_{\text{max}}/C_{\text{min}}$ ratio is varied by varying the parameter β . The maximum device voltage can be varied by choosing the appropriate value of α . See Equation(4.3). .	45
4.3	Shunt Z tripler circuit model for analysis.	46
4.4	Circuit for large signal harmonic balance analysis.	48
4.5	Illustration of multiple reflection technique. A long transmission line having an arbitrary characteristic impedance Z_0 is inserted between the nonlinear and linear subcircuits of the frequency multiplier.	50

4.6	The circuits which must be solved in the time domain to find the voltage and current at the diode terminals, (a) at time $t = 0$ when the right propagating wave contains components only at DC and the LO frequency and (b) for all successive iterations. The voltage sources together with Z_0 make up the equivalent circuit of the transmission line, which is in steady state with the diode.	52
4.7	Measured $C(v)$ of one of the devices in this thesis and the fit using our cubic model (CM). See Equations (4.3)-(4.5). $\alpha = 0.98$ $\beta = 3.2$	55
4.8	Mount design for a planar SBV tripler	58
4.9	Conceptualized tripler indicating the geometry of the circuit and the mount.	58
4.10	Simulated performance of the lowpass filter.	60
4.11	Input circuit of the planar 13 to 39 GHz tripler.	60
4.12	Simulated performance of the bandpass filter.	61
4.13	Output circuit of the planar 13-39 tripler.	62
4.14	Design diagram indicating the design objectives and the various circuit blocks.	63

5.1	Diagram indicating ΔE_C and activation energy, ϕ_e . The activation energy as a function of bias is found from the measurements. The discontinuity can be evaluated from the zero bias (extrapolated) activation energy and the term η_F that is determined from the Joyce-Dixon approximation. . .	67
5.2	Experimental set up to measure $I(v)$ characteristics of chip <i>GaAs</i> devices at various temperatures. The data is used to extract the barrier height of the various structures.	68
5.3	Plot of I/T^2 (log scale) versus $1000/T$ for a $120 \times 120 \mu m^2$ 1205 device that has a thick barrier ($250 \text{ \AA}$). The bias voltage is 0.2 V. The straight line portion indicates the validity of the thermionic emission theory to calculate ΔE_c	69
5.4	Plot of I/T^2 (log scale) versus $1000/T$ for a $120 \times 120 \mu m^2$ 1411 device that has a thinner chair barrier ($125 \text{ \AA}$). The bias voltage is 0.2 V. The straight line portion indicates the validity of thermionic emission theory to calculate ΔE_c	70
5.5	Plot of activation energy versus bias voltage for various <i>GaAs</i> devices. The activation energy at each bias point is determined from the slope of the plot $\ln I/T^2$ versus $1/T$ as indicated in Figure 5.4 and 5.3.	71

5.6	A mount for measurement of <i>GaAs</i> chip devices. The chip devices are connected to the end of a 50- Ω microstripline.	75
5.7	Network analyser displays showing the input vector reflection coefficient at various bias points. The device and the embedding can be thought of as a lossy series resonance circuit whose resonance varies with bias voltage. (a) S_{11} trace for $v_d = 0$ V. (b) S_{11} trace for $v_d = 1.0$ V.	77
5.8	S_{11} of device 1206 measured using the special mount: (a) $v_d = 2.0$ V (b) $v_d = 3.0$ V. A C_{max}/C_{min} ratio of 4 is deduced from the graphs by measuring the resonance frequency. Accurate de-embedding also reveals the same C_{max}/C_{min} ratio.	78
5.9	The $C(v)$ characteristics of two 1206 varactors having different areas. The $C(v)$ curves are obtained from microwave reflection measurements using a special mount.	79
5.10	The $C(v)$ characteristics of two 1411 chair-barrier varactors having different areas. The specific capacitance (mF/m^2) is plotted. The device capacitances are found to scale with area.	80
5.11	The coaxial mount used to characterize high- Q packaged <i>InP</i> varactors. The sketch also outlines the S4 package with the equivalent circuit elements relating to the physical package.	82

5.12	A plot of real impedance of a packaged <i>InP</i> stacked varactor as a function of frequency. Resonance occurs close to 6.0 GHz and $R_S = \text{Re}[Z_{11}] _{v_d=0V} = 0.28 \Omega$	83
5.13	A plot of imaginary impedance of a packaged stacked <i>InP</i> varactor as a function of frequency. Resonance occurs close to 6.0 GHz and $R_S = \text{Re}[Z_{11}] _{v_d=0V} = 0.28 \Omega$	84
5.14	A plot of imaginary impedance of a packaged single barrier <i>InP</i> varactor as a function of frequency. Good capacitance modulation is indicated by the change in the resonance frequency with bias.	85
5.15	A plot of real impedance of a packaged stacked <i>InP</i> varactor as a function of frequency. $R_S = 0.37 \Omega$	86
5.16	Capacitance versus voltage plot of 62 μm diameter single barrier <i>InP</i> device.	87
5.17	Capacitance versus voltage plot of a 42 μm diameter stacked <i>InP</i> device. .	87
5.18	Comparison of measured $C(v)$ with the simple model. Device type 1206 has dimensions $240 \times 240 \mu m^2$ and Device type 1411 $120 \times 120 \mu m^2$	88
5.19	A comparison of the dynamic quality factor $Q(v)$ of a thick-barrier (274 Å) type 1206 varactor with that of a thin-barrier (142 Å) type 1411.	90

- 5.20 Simulated efficiency versus absorbed power for an SBV tripler from 64 GHz to 192 GHz, based on the use of a scaled 1206 device. The device area is $(5 \times 5) \mu m^2$ and $R_S = 5 \Omega$. (-o-): using measured data for SBV 1206. (..◆...): assuming zero leakage current. (-◆-): assuming leakage current is 100× the measured value. 92
- 5.21 Simulated output power versus absorbed power for an SBV tripler from 64 GHz to 192 GHz, based on the use of a scaled 1206 device. The device area is $(5 \times 5) \mu m^2$ and $R_S = 5 \Omega$. (-o-): using measured data for SBV 1206. (..◆...): assuming zero leakage current. (-◆-): assuming leakage current is 100× the measured value. 93
- 5.22 Simulated output power versus absorbed power for a tripler from 64 GHz to 192 GHz, using a scaled 1206 device of area $(5 \times 5) \mu m^2$, showing the effect of increasing R_S from 5 Ω to 10 Ω . The 10 Ω value is typical of a small device. $R_S = 5 \Omega$ (-o-): using measured data for SBV 1206 (-◆-), assuming the leakage current is 100× the measured value. $R_S = 10 \Omega$ (...□..): using measured data for SBV 1206. (..■....), assuming the leakage current is 100× the measured value. 94

5.23	Simulated voltage and current waveforms of a frequency tripler from 64 GHz to 192 GHz, assuming a 1206 type device. The circuit conditions are: Absorbed power $P_{abs} = 5.12$ mW, output power $P_{out} = 2.56$ mW, maximum SBV voltage $v_{dmax}=4.58$ V.	95
5.24	Simulated voltage and current waveforms of a leaky -barrier frequency tripler from 64 GHz to 192 GHz, assuming a 1206-type device, but with the leakage current artificially increased to 100 times the measured value. The circuit conditions are: Absorbed power $P_{abs} = 9.29$ mW, output power $P_{out} = 1.85$ mW, maximum SBV voltage $v_{dmax} = 4.58$ V.	96
5.25	Simulation results of efficiency versus absorbed power for single barrier <i>InP</i> varactor frequency tripler from 13 to 39 GHz. The device has a $C(0)$ of 0.6 pF. Tripler simulations were terminated when v_{dmax} reached V_{br}	98
5.26	Simulation results of efficiency versus absorbed power for a stacked <i>InP</i> varactor device tripler from 13 to 39 GHz. The device has a $C(0)$ of 0.6 pF. Tripler simulations were terminated when v_{dmax} reached V_{br}	99
5.27	Simulated voltage and current waveforms of a triple stacked device in a frequency tripler from 13-39 GHz. The total device current i_d is indistinguishable from the displacement current i_C because the leakage current is very low.	100

5.28	Simulated efficiency and output power of frequency triplers from 62 to 186 GHz, as functions of absorbed input power. Single barrier and stacked devices have a zero-bias capacitance $C(0)=40.0$ fF.	101
5.29	Photomicrograph of the Ka band planar tripler. The bias circuit is designed to monitor the self-bias dc current. No appreciable amount of dc current is detected.	103
5.30	Experimental set up to measure tripler performance.	104
5.31	Frequency response of the tripler shown at $P_{in} = 18$ dBm and $P_{in} = 22$ dBm.	105
5.32	P_{in} versus P_{out} of the tripler at the center frequency 13.45 GHz.	106
6.1	Flow chart depicting the problem of early <i>GaAs</i> SBVs and the thesis contribution towards solving the problem.	110
6.2	Flow chart depicting the limitations of basic SBVs and the thesis contribution towards improving the state of the art in symmetric $C(v)$ device by stacked approach.	111
A.1	SIMS profile for the SBV device 1206.	122
A.2	SIMS profile for the SBV device 1411.	123
B.1	Series resistance model.	126

D.1	Dimensions of S4 package in cms.	136
D.2	Equivalent circuit of open and short circuit packages.	137
D.3	A plot of fitted and measured admittance of a short circuit package as a function of frequency.	138
D.4	A plot of fitted and measured admittance of an open circuit package as a function of frequency.	139

List of Tables

2.1	Proposed <i>GaAs</i> varactor structures.	28
2.2	Comparison of measured current density J of various varactors.	29
4.1	Comparison of the 10-30 GHz tripler analyses: Harmonic Balance versus Cubic Model.	56
4.2	Input matching circuit performance when loaded with output matching and filter.	64
4.3	Output matching circuit performance when loaded with input matching and filter.	64
5.1	Measured barrier heights of the various varactors.	71
5.2	Effective barrier widths from capacitance measurements.	89
5.3	Simulated performance of stacked varactor triplers.	98

Symbols

$C(v)$ Nonlinear capacitance function.

E_F Fermi energy level.

E_C Energy of the conduction band-edge.

$\mathcal{F}$ large signal cut-off frequency of a varactor.

$\mathcal{F}_{1/2}(\eta)$ Fermi-Dirac integral.

ΔE_c Conduction band discontinuity or barrier.

ϕ_e Activation energy.

η Efficiency of the frequency multiplier.

k_B Boltzmann's constant.

N_d Concentration of the dopant in cm^{-3} .

q_e Electron charge.

Q Dynamic quality factor of the varactor.

R_S Series resistance of the device due to contact, undepleted epitaxy and substrate.

Z_0 Characteristic impedance of the system.

Glossary

CM Cubic model for symmetric varactors developed in this thesis.

DRO Dielectric resonator oscillator.

GaAs Gallium arsenide.

HB Harmonic balance.

HBV Heterostructure barrier varactor.

HEMT High electron mobility transistor.

InP Indium phosphide.

MBE Molecular beam epitaxy.

MOCVD Metal organic chemical vapor deposition.

MESFET Metal semiconductor field effect transistor.

QBV Quantum barrier varactor.

RHEED Reflection high energy electron diffraction.

SBV Single barrier varactor.

SIMS Secondary ion mass spectroscopy.

TEM Transmission electron microscopy.

Chapter 1

Introduction

1.1 Motivation

Commercial and military equipment use signals at ever higher frequencies, with a lot of new activity occurring in the radio frequency band, 30-40 GHz. A high quality tunable oscillator capable of operation over this frequency range would be expensive and limited to frequencies less than 30 GHz because of the losses in the dielectric material and the oscillator circuitry used at the higher frequencies. Coverage of this frequency range can be accomplished by extending the frequency of operation of existing oscillators that work up to 18 GHz. A popular and viable means of realizing a source is to follow a highly-stable DRO (Dielectric Resonator Oscillator) with a frequency multiplier. This approach avoids direct phase locking that would require a millimeter-wave divider (or prescalers). These components are not readily available above ~ 18 GHz. The DRO can be further stabilized/tuned with a varactor and a crystal reference.

Space-borne radiotelescopes for radio astronomy and remote sensing of the atmosphere in the frequency range 150-500 GHz are receiving more and more interest. An all solid-state local oscillator consisting of a Gunn oscillator (50-100 mW) at around 100 GHz pumping a multiplier seems to be the most promising local oscillator source

[Räi92].

Diode frequency multipliers have traditionally used *pn*-junction or Schottky varactors. These devices have mostly been used to realize doublers. Higher-order multiplication using these devices requires idler circuitry that limits the efficiency, power output (~ 4 mW for a 200-GHz tripler [Räi92]) and also the bandwidth of the multipliers. A multiplier without an idler is mechanically less cumbersome and easier to design. Recent advancements in semiconductor growth have made it possible to fabricate new varactors that have characteristics suitable for designing triplers without second harmonic idlers. One such device, called the single barrier varactor (SBV), has exhibited performance comparable with the Schottky Barrier tripler at 200 GHz, with the advantage of much simpler circuitry [RGK90].

The early SBV devices had high leakage currents. The apparent height of the current-blocking barrier was found to be only 180 meV as opposed to the expected value of 680 meV [RGK90]. An explanation for this discrepancy is sought in this thesis.

The authors of [RGK90] obtained an output power and efficiency of more than 1 mW and 5% efficiency (at 210 GHz) , respectively, despite the SBV's excess current density. Further, output power saturation was observed at low input power levels. It was also pointed out that the device leakage current density played an important part in the function of the tripler. It was expected that if leakage currents could be reduced, improved tripler efficiencies would be obtained.

The zero-bias capacitance of the first SBV was 50 fF for a device area of $30 \mu\text{m}^2$ [RGK90]. A series resistance of 9Ω was reported. This series resistance is comparable with the state-of-the art Schottky varactor such as the University of Virginia 6P4 (area= $32 \mu\text{m}^2$) [Räi92]. The breakdown voltage of the UVA 6P4 is 20 V. Early SBVs broke down at 6 V. The zero bias capacitance of the Schottky varactor is 21 fF, a factor of 2.5 lower than the SBV. Lower capacitance for the same area with the same series resistance would imply better coupling to the mount at higher frequencies [RGK90]. It is necessary to find a way of obtaining lower capacitance per unit area

and higher breakdown voltages with novel structures that have the same favourable symmetric capacitance as the SBV.

The theory of abrupt junction and Schottky varactor multipliers has been addressed comprehensively by many authors; the main theories being those of Penfield and Rafuse [PR62] and a general approach by Burckhardt [Bur65]. The SBV tripler has been modeled by a measured $C(v)$ and analyzed using a computer-based algorithm [SKH84] [Räi92]. A simple large-signal model and tripler analysis is needed.

Most of the successful Schottky varactors reported so far have been on *GaAs*. Experiments have shown that at high frequencies and high power levels the multipliers employing *GaAs* Schottky barriers saturate before they are driven to breakdown or conduction [Eri90]. This has been identified as a problem with limited electron velocity in *GaAs* [KTFE92]. However the electrons can travel faster in *InGaAs* and a varactor using *InGaAs* depletion layer would have higher immunity to the problem of velocity limited saturation. This motivated the author to explore SBVs on *InP* that is lattice matched to *InGaAs*.

The attractive features of not requiring a second harmonic idler and bias circuit and new tripler requirements in the millimeter-wave band motivated the author to investigate the possible ways of improving the SBV devices and increasing the power output capability of triplers based on these devices. This thesis deals with the improved design of symmetric varactors on gallium arsenide and indium phosphide, the theory of symmetric varactor triplers, the characterization of the devices by microwave measurements and the demonstration of an idler-free, bias-free millimeter-wave tripler using such a symmetric varactor.

1.2 Objectives

The objectives of this thesis are the following.

1. To identify the causes for excessive leakage currents and low- Q of single barrier varactors. A study of the effect of leakage currents on tripler performance

will lead to an understanding of the poor performance of earlier single barrier varactors.

2. To demonstrate low-leakage varactor structures on *GaAs* by exploiting molecular beam epitaxy growth techniques.
3. To demonstrate by measurement and simulation that higher power output and lower capacitance per unit area can be obtained with novel stacked varactor structures on *InP*.
4. To develop a simple model to analyze triplers based on the single barrier varactor. This is motivated by the non-availability of a simple model or an analysis of a tripler based on such a device.
5. To actually demonstrate a planar tripler capable of working without an idler and able to give enough power output to drive a double balanced mixer.

1.3 Outline of the Thesis

Chapter 1 describes the motivation for the thesis and outlines its objectives. Chapter 2 describes the various issues and technological advances related to the development of the new device. It takes the reader through the problems with the early single barrier varactors and proposes solutions. Growth and processing are described briefly in Chapter 3. Chapter 4 briefly describes a new large-signal symmetric varactor model, proposed in the thesis for the first time, that makes possible a closed-form analysis of SBV triplers. The analysis is compared with a computer-based harmonic balance simulation, showing very good agreement. All the experimental results are described in Chapter 5. Device characterizations using RF measurements are done by employing a planar microstrip mount and a classical coaxial mount. Very high Q devices are demonstrated for the first time. Simulations of stacked devices and single SBVs are carried out and compared with the leaky varactors investigated by other

authors, thus bringing out the potential improvements realized by the work in the thesis. Experimental work on a planar SBV tripler is also reported. The final chapter summarizes the work and suggests directions for future work with the device.

Chapter 2

Heterostructure-Barrier Varactors for Frequency Tripling

2.1 Introduction

Frequency multiplication occurs whenever a nonlinear impedance is driven by a periodic source. Two types of millimeter-wave harmonic generators are in general use; one is based on the nonlinear resistance of the forward-biased Schottky barrier diode, the other makes use of the nonlinear capacitance variation of a reverse-biased diode.

The forward-biased Schottky varactor exhibits an exponential $I(v)$ characteristic which, when pumped by a periodic source, yields both odd and even harmonics. A balanced diode configuration has been used to selectively extract the even or odd harmonic. Very wideband triplers and doublers using balanced resistive diodes have been demonstrated [Hu86] [Boc89]. The ultimate conversion performance of a positive nonlinear resistance multiplier is given by the Page-Pantell inequality [Pag58] [Pan58]. This expresses the limiting efficiency of a positive nonlinear resistance multiplier as

$$\eta \leq \frac{100}{n^2} \% \quad (2.1)$$

where n =order of multiplication.

In practice the circuit losses and nonideal diodes increase the conversion loss to realistic values of 12 dB for an R-band (26.5-40 GHz) balanced doubler and 19 dB for a W band tripler (75-110 GHz) with output power in the range of a few milliwatts (< 10 mW) [SA91].

Multipliers with efficiencies of 100% are theoretically possible with a "variable reactance device" termed as a varactor. They continue to be important devices for applications that require millimeter-wave power. Additionally, these components are quiet in that they generally contribute no excess phase noise above the fundamental enhancement of $20\log_{10}n$ in the noise-to-carrier ratio at the output of a times- n multiplier. Combining high power and acceptable conversion loss with this low phase noise enhancement makes the multiplier using varactor devices a key component for millimeter-wave radar and communications applications [Pet90].

Frequency-multiplier varactors are often realized as p^+ structures on n substrates in both *GaAs* and silicon. Because the diodes' p^+ regions are difficult to fabricate uniformly in the small anode sizes necessary for high-frequency operation, these diodes are limited to the lower microwave and millimeter-wave regions [Maa88]. Frequency multipliers having input frequencies above approximately 50 GHz usually employ Schottky barrier varactors. Often such multipliers are used to generate output frequencies up to 750 GHz [Räi92].

We shall call the p^+n varactor and the Schottky varactor "conventional" devices in this thesis. The unsymmetric capacitance versus bias voltage characteristic of these conventional varactors results in the generation of both even and odd harmonics. For harmonics above the second, these multipliers require idler circuits that are lossy and difficult to implement mechanically at millimeter-wave frequencies. A device with a symmetric $C(v)$ characteristic would yield only odd harmonics and hence an idler would not be required at the second harmonic.

Capacitance-voltage characteristics with even symmetry have been realized by using opposingly biased Schottky diodes connected in anti-parallel [Ave64] [Fik64]. This set-up would require two bias circuits and depends on using two diodes with exactly

similar characteristics. Now with the advancement of device growth techniques, it is possible to grow a current-blocking barrier of large-bandgap material in between the lightly doped regions of smaller-band-gap semiconductors. This device, termed a Quantum Barrier Varactor (QBV) or a Single Barrier Varactor (SBV) has a symmetric $C(v)$ with maximum capacitance at zero bias. Multipliers designed using SBVs do not require idlers or bias circuits. This makes the realization of the tripler circuits very compact and efficient.

I shall first deal with the heterostructure fundamentals required for the study of SBV heterojunction device structures, develop the concept of a heterostructure single barrier varactor deriving its $C(v)$ characteristic, investigate the problems of early SBV's and propose solutions for realizing low-leakage SBV's on *GaAs* and *InP*.

2.2 Heterojunction Device Fundamentals

The interface between two different semiconductors, epitaxially grown on top of each other, is called an heterojunction. The complete semiconductor crystal with one or more heterojunctions is called a heterostructure. The two different semiconductors can have different bandgaps and the heterojunction can be used to provide spatial control of bandgap through the device. A heterojunction can be used to produce potential barriers which restrict charge flow to certain layers, to tailor contact injection or extraction properties, to tailor the internal electrostatic profile, or to realize optical and quantum effect devices.

2.2.1 Materials for Heterojunctions

Figure 2.1 represents the III-V semiconductor family tree. The vertical axis is the crystalline lattice constant expressed in Angstroms ($\text{\AA}$) The horizontal axis shows the minimum bandgap in electron volts. If different III-V materials can be combined as an alloy, the points are connected by lines indicating the bandgap of the alloy. The

Figure 2.1: Compilation of minimum bandgap versus lattice constant data [Swa92].

compounds lattice-matched to *GaAs* and *InP* substrates are also indicated. When growing heterostructures epitaxially, it is important to maintain the quality of the interface. Ideally the lattice constant (a_1) of the substrate and that of the epitaxial material (a_2) should be the same. The strain in % is defined as $\frac{|a_1 - a_2|}{a_1} \times 100$ %.

2.2.2 Lattice Match

There has been success in controlled growth of lattice-mismatched compounds referred to as pseudomorphic materials. In a pseudomorphic structure, a thin lattice-mismatched semiconductor takes on the lattice constant of the host semiconductor substrate. (Figure 2.2) The pseudomorphic layer is under both tensile and compressive stress, but is sufficiently thin ($t < t_{dis}$) that the strain energy is not enough to create dislocations (Figure 2.2 (b)). Figure 2.2 (c) indicates dislocations created

Figure 2.2: Lattice mismatch and critical thickness for dislocation.

by strain for an epitaxial thickness $t > t_{dis}$. These structures offer the possibility of incorporating thin layers with special electrostatic and transport properties on the host semiconductor substrate. An example is a strained layer of $In_xGa_{1-x}As$ grown on $GaAs$ to take advantage of the low bandgap and high mobility of $In_xGa_{1-x}As$. In this thesis we will use the current-blocking characteristics of the pseudomorphic structures to realize high Q varactors.

2.2.3 MBE Growth

Among the numerous different crystal growth techniques available today molecular beam epitaxy (MBE) has distinguished itself as one of the more successful ones in terms of electrical, structural and optical properties of the grown layers. The driving force in the development of MBE was and still is the possibility of growing high quality crystals suitable for basic research purposes and for the device industry. The technique has evolved to the point that it offers many attributes such as atomically smooth

Figure 2.3: A schematic diagram to show an MBE set up.

interfaces, abrupt compositional changes, sharp doping profiles and low growth rates.

The concept of molecular beam epitaxy is simple: an atomic or molecular beam of lattice constituents (*Ga*, *As*, *Al*) produced by heating high-purity, solid sources of these elements in a high vacuum ($\sim 10^{-10}$ torr) chamber are directed onto a heated substrate. The substrate is rotated to obtain uniform and reproducible layer properties. The group III atoms have a high sticking coefficient on the substrate at the growth temperature (typically $\sim 550^\circ\text{C}$). Shutters, in front of the small ovens that heat the source chemicals, allow switching in of *Al* beams for the growth of *AlGaAs*, or dopant beams; typically *Si* for *n*-type doping and *Be* for *p*-type doping.

Growth mode and kinetics on the substrate surface can readily be observed during growth by the in-situ UHV technique of reflection high energy electron diffraction (RHEED). The RHEED system is indicated in Figure 2.3 and it consists of an electron gun and a fluorescent screen. The versatility and ease of use make RHEED an important analysis instrument in many MBE-chambers. Most calibrations of growth rate and thereby alloy concentrations are made by observing the intensity oscillations

in the RHEED pattern.

2.2.4 Direct and Indirect Band Offsets

In the heterojunction there normally exists a discontinuity in the position of the valence and conduction band edges due to the different band gap of the materials. This discontinuity is often referred to as band offset. The value of the offset is of high importance for the electronic properties of the heterostructure. In particular it determines confinement energies and barrier heights in quantum structures.

There are several theories for calculating the offsets in heterostructures. The simplest are probably the affinity rule and the common anion rule. In the former the offset is obtained from the difference in the electron affinity (or the ionization potential) of the two materials and the latter states that the valence band offsets in polar semiconductors are determined solely by the anions. Unfortunately these simple rules fail to predict the offsets for many of the common heterostructures and more elaborate methods are needed. An excellent review of various theoretical approaches to this problem has been given in [CM87].

The band gap data in Figure 2.1 represents the direct bandgap of the semiconductors, i.e. the minimum difference in valence band maximum and conduction band minimum occurs at the same value of wave number k . Most of the binaries are direct at room temperature. Figure 2.4 shows the $E - k$ diagram of $GaAs$. The direct bandgap of 1.42 eV occurs at the zone center ($k = 0$). The indirect gap associated with the valence band maximum at the zone center (Γ) and the conduction band minimum at X denoting the zone end along a $\langle 100 \rangle$ direction is 1.90 eV and the one associated with the conduction band minimum L denoting the zone end along $\langle 111 \rangle$ and Γ valence band maximum is 1.71 eV. When the binaries or elemental semiconductors are mixed to form compound semiconductors the indirect bandgap, which is the difference in energy between the valence band minimum and the conduction band minimum, at different values of k , is smaller than the direct bandgap.

Figure 2.4: $E - k$ diagram of $GaAs$ [Pie87].

In these compounds the transport properties are determined by both the direct and indirect bandgaps.

When a semiconductor A is grown on top of another semiconductor B and if the fundamental energy gaps of both A and B are at the same point of the Brillouin zone, e.g., Γ , the potential barrier for the electron is the energy difference $E_{\Gamma A} - E_{\Gamma B}$. When the semiconductor B is an indirect gap semiconductor, other band offsets have to be considered as well.

$GaAs/Al_xGa_{1-x}As$ heterojunctions have been thoroughly studied and band offsets (ΔE_g) are summarized in [CM87]. For $x < 0.4$, $AlGaAs$ is a direct semiconductor and the various reports seem to converge on a relative conduction band offset of around $\Delta E_c \approx 0.65\Delta E_g$, i.e. 65 % of the total band gap difference takes places at the conduction-band edge. For higher x values $Al_xGa_{1-x}As$ becomes indirect, resulting in different values for $\Gamma - \Gamma$ and $\Gamma - X$ offsets. The valence band offset on the other hand is single valued for all x . Batey and Wight [BW86] reported the valence band offset to be a linear function of aluminium concentration x : $\Delta E_v = 0.55x$ (eV) for all

x values. For x values > 0.4 the conduction band offset is obtained from the relation $\Delta E_c = \Delta E_g - \Delta E_v$ where ΔE_g , is either the $\Gamma - \Gamma$ or the $\Gamma - X$ band gap depending on which offset is desired.

In the case of the $GaAs/Al_xGa_{1-x}As$ hetero-interface the conduction band offsets are derived from Batey's valence band results and the bandgap data are derived from [CM87]. They are given by [MCW86] as

$$\Delta_\Gamma = 0.7x \quad (0 \leq x \leq 0.45) \quad (2.2)$$

$$= 0.7x + 1.15(x - 0.45)^2 \quad (0.45 < x \leq 1), \quad (2.3)$$

$$\Delta_L = 0.30 + 0.092x \quad (0 \leq x \leq 1), \quad (2.4)$$

$$\Delta_X = 0.44 - 0.42x + 0.14x^2 \quad (0 \leq x \leq 1). \quad (2.5)$$

Other heterointerfaces of interest in the case of heterostructure barriers are:

- (a) $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ direct barrier lattice matched to InP with $\Delta E_c \approx 0.55$ eV [PWAC83].
- (b) $AlAs/In_{0.53}Ga_{0.47}As$ with $\Gamma - \Gamma$ offset of 1.2 eV and $\Gamma - X$ offset of 0.65 eV [IMN+87].
- (c) $AlSb/InAs$ with $\Gamma - \Gamma$ offset of 1.8 eV and $\Gamma - X$ offset of 1.2 eV [CMM+93].

In the structures (b) and (c) above it is very important to include the effects of strain on the energy levels. The band offset depends on the strain and hence the thickness of the strained layers [Swa92]. This overview of the heterostructure semiconductor technology and its capabilities form the basis for the design of the heterostructure varactor design work carried out in this thesis.

2.3 Varactors: A General Description and Review

Before we delve into the details of the single barrier varactor it is instructive to lay out the general features of a depletion varactor and some of the terminology and circuit

representations used. A generic varactor is shown in Figure 2.5. It consists of a contact on the top, a barrier that (a) prevents carrier flow through the structure, and (b) changes the charge density away from the equilibrium value set by the doping, a region of semiconductor where charge can be depleted or accumulated, and a bottom contact. In a conventional Schottky barrier varactor, the top contact and the barrier are combined in the metal-semiconductor junction. The barrier height is determined by the interface physics and is of the order of 1 eV for most metals on *GaAs* [FE92]. The semiconductor under the contact is depleted, with the depletion layer width and the resulting capacitance being controlled by the combination of the barrier height, the applied voltage and the doping profile in the semiconductor. Most of the high-frequency harmonic multipliers demonstrated to date are based on this Schottky structure [Räi92].

The dependence of the junction capacitance on reverse bias v of a Schottky barrier varactor is given by a relation that can be worked out from simple electrostatics [Pie87]

$$C_j(v) = C_j(0) (1 - v/\phi)^{-1/2} \quad (2.6)$$

where ϕ is the barrier potential and $C_j(0)$ is the zero-bias capacitance given by (neglecting fringing effects)

$$C_j(0) = A\sqrt{q_e N_d \epsilon / (2\phi)} \quad (2.7)$$

where N_d =donor doping density, A =diode area, ϵ =permittivity of the epi material. The unsymmetrical capacitance-versus-bias voltage ($C(v)$) when pumped with an RF signal generates both even and odd harmonics.

A symmetric $C(v)$ characteristic that has potential advantages in tripler implementations can be realized if the general structure in Figure 2.5 is altered as shown in Figure 2.6. The structure has an ohmic contact at each end and a heterojunction barrier in the middle. There are n -type regions on both sides between the contacts and the barrier. This structure is the single barrier varactor SBV, first proposed by Kollberg and Rydberg[KR89]. When a bias is applied across this structure, one side of the barrier is depleted and the other side is accumulated. The resulting capacitance

Figure 2.5: Schematic diagram of a generic semiconductor varactor [FE92].

is the series combination of the capacitance of the barrier region and the two semiconductor regions, with most of the capacitance change occurring on the depletion side of the barrier. Since the structure is symmetrical about the centre, the resulting capacitance versus bias voltage will also be symmetrical about zero bias.

In the SBV, the barrier is in the middle of the structure and the two depletion layers extend towards the ends. A structure that has two heterojunction-Schottky barriers at the ends and depletion layers extending into the middle with forward or reverse bias also has symmetric $C(v)$ characteristics [LHM87]. A team at Jet Propulsion Lab in Pasadena, USA has been working on this device which is named the bbBNN¹. The device structure as shown in Figure 2.7, is inherently planar.

All the above devices have current flow perpendicular to the semiconductor layers. In the two-dimensional-electron-gas diode proposed by Peatman of the University of Virginia, Charlottesville, the current flow is parallel to the epitaxial layers [PC90].

¹"Back-to-back barrier-n-n⁺"

Figure 2.6: Schematic diagram of SBV.

Figure 2.7: Schematic diagram of bbBNN [FE92].

The structures discussed in this section are very general structures possessing nonlinear $C(v)$ characteristics; they are being intensively researched for application in high frequency generation.

2.3.1 Electrical Equivalence of Depletion Varactors

A generalized model for the unpackaged varactor, based on electrical lumped elements, that is quite accurate and has been widely used in predicting the performance of the devices in multiplier circuits, is shown in the equivalent circuit of Figure 2.8. It consists of a resistance R_S in series with a parallel combination of a nonlinear device capacitance $C_j(v)$ and a leakage conductance $G_j(v)$. The nonlinear capacitance is due to the voltage-dependent width of the depletion layer. The nonlinear conductance is due to the $I(v)$ curve of the diode. The series resistance is due to the finite loss in the ohmic contacts, undepleted epitaxial layers and the substrate.

The best multiplier efficiency occurs when the multiplication is purely reactive, i.e. R_S and $G_j(v)$ are zero. But in practice these parasitic elements cannot be ignored. The deviation from an ideal varactor can be quantitatively represented by a quality factor. A high value of the dynamic quality factor $Q(v)$, derived from Figure 2.8, means low loss due to R_S and $G_j(v)$:

$$Q(v) = \frac{\omega C_j(v)}{R_S [G_j^2(v) + \omega^2 C_j^2(v)] + G_j(v)}. \quad (2.8)$$

This factor will be used to compare the various devices, based on an equivalent circuit that can be extracted by microwave measurements.

2.3.2 Large Signal Cut-Off Frequency

A very commonly used figure of merit for a varactor, the large signal cut-off frequency $\mathcal{F}$, can be used to compare various devices based on their $C(v)$ characteristics. The figure of merit $\mathcal{F}$ depends on the series resistance, maximum capacitance and

Figure 2.8: Equivalent circuit of a generalized varactor.

C_{max}/C_{min} ratio:

$$\mathcal{F} = \frac{1}{2\pi R_S} \left[\frac{1}{C_{jmin}} - \frac{1}{C_{jmax}} \right]. \quad (2.9)$$

Penfield and Rafuse [PR62] have pointed out that the maximum possible efficiency of multipliers depends on $\mathcal{F}$. Their result was derived for varactors with zero conduction current.

2.4 Principles of a Single-Barrier Varactor

The energy-band diagram or potential profile of a biased single-barrier varactor is shown in Figure 2.9. When the diode is biased in the forward direction, the depletion region will appear on one side of the barrier, and accumulation on the other side. The depletion capacitance of the device will decrease with increasing voltage. Since the diode is essentially symmetric, a reverse bias will also cause a decrease in the capacitance of the device. Hence the maximum capacitance is obtained for zero voltage and is determined by the thickness of the *AlGaAs* barrier. The minimum capacitance, which occurs for the maximum bias voltage, is determined by the doping concentration of the low-doped region as will be discussed later in this section. In fact, a similar capacitance swing with voltage as for a Schottky varactor is expected.

Figure 2.9: Energy band diagram of a single barrier varactor showing, accumulation, barrier and depletion potentials.

2.4.1 Electrostatics of a Single Barrier Varactor

The following are the assumptions made:

- The depletion approximation is employed. It assumes that the electrons are small in number compared to the donor ions in the depletion region on the anode side of the barrier, i.e. $\rho = q_e N_d$ in the depletion region.
- The quantum barrier is assumed uncharged. This leads to a constant electric field, $\mathcal{E} = F$ [V/m] across the barrier. The uncharged-barrier assumption is valid as long as the current J through the device is such that the mobile charge density under bias (J/v_d) is far less than the background doping concentration, N_d . Confidence in the validity of this assumption is provided by the fact that a thick barrier does not support electron transport. This assumption greatly simplifies the capacitance calculation.
- It is assumed that the charge accumulation in the cathode side of the barrier is taken into account.

The energy diagram of the biased QBV in Figure 2.9 indicates the potentials V_d , V_b and V_a . Solving Poisson's equation in the depletion region, using the depletion approximation, and using the continuity of $\mathcal{E}$ at the barrier-depletion interface, we have, for the depletion width

$$d = \sqrt{\frac{2\epsilon_s\epsilon_0 V_d}{q_e N_d}} \quad (2.10)$$

and depletion voltage

$$V_d = \frac{\epsilon_s\epsilon_0}{2q_e N_D} \left(\frac{V_b}{w} \right)^2. \quad (2.11)$$

Vakshoori and Wang [VW87] have calculated the accumulation potential by assuming a triangular potential well. Their result is

$$V_a = 2.65 \times 10^{-4} \left(\frac{V_b^2}{w} \right)^{2/5} \quad (2.12)$$

where w is the barrier width in meters and V_a , V_b are in volts. The applied bias V is the sum total of the drop in the accumulation, barrier and depletion regions:

$$V = V_a + V_b + V_d. \quad (2.13)$$

For each value of bias voltage, V , we solve Equations 2.11, 2.12 and 2.13. Knowing V_d , we can calculate the depletion width, d from Equation 2.10 and hence the depletion capacitance,

$$C_d = \frac{\epsilon_s\epsilon_0 A}{d}. \quad (2.14)$$

The barrier capacitance is given by

$$C_b = \frac{\epsilon_b\epsilon_0 A}{w}, \quad (2.15)$$

where A is the device area.

The accumulation capacitance is large compared to the barrier and the depletion capacitance. This is because the accumulation occurs over a small length (tens of $\text{\AA}$) as opposed to depletion over 100's of $\text{\AA}$. The device capacitance C , is therefore approximated by the series combination of the barrier capacitance C_b and the depletion

Figure 2.10: The calculated $C(v)$ curve of a QBV with $N_d = 10^{17} \text{ cm}^{-3}$, $w = 200 \text{ \AA}$ and $A = \pi \times 10 \mu\text{m} \times 10 \mu\text{m}$.

capacitance C_d :

$$C = \frac{C_b C_d}{C_b + C_d}. \quad (2.16)$$

The calculated $C(v)$ characteristic of the varactor with $w = 200 \text{ \AA}$ and $N_d = 10^{17} \text{ cm}^{-3}$ is shown in Figure 2.10.

If we assume that the relative permittivity of the barrier (ϵ_b) and depletion material (ϵ_s) to be the same then we can simplify $C(v)$ to a neat close form expression

$$C(v) = \frac{\epsilon_s \epsilon_0 A}{w + \sqrt{\frac{2\epsilon_s \epsilon_0 V_d}{q_0 N_d}}} \quad (2.17)$$

The above equation can be simplified if we express the voltage dependence of the device capacitance in terms of the zero bias capacitance, $C(0)$

$$C(v) = \frac{C(0)}{1 + \sqrt{\frac{2\epsilon_s \epsilon_0 V_d}{q_0 N_d w^2}}} \quad (2.18)$$

We will find later that in practical single-barrier devices the measured $C(0)$ is smaller than the calculated $C(0)$ based on the metallurgical barrier thickness. This can be accommodated by an effective barrier thickness at zero bias, w_{eff} .

2.5 Single Barrier Varactors: Problems and Solutions

As pointed out in previous sections, SBVs with symmetric $C(v)$ characteristics, and maximum capacitance at zero bias have potential advantages for designing triplers without idlers and bias circuits. These devices simplify the tripler circuitry by obviating the need for second harmonic idlers and bias circuits. The tripler can yield good efficiencies if the dynamic Q of the device is high.

The first single-barrier varactors, also known as quantum barrier varactors, were made on *GaAs* and were limited in their power output [RGK90]. An efficiency of 5% with a power output of 2 mW was measured experimentally for the output frequency range of 210-280 GHz. The device was leaky and output saturation occurred at low input power levels. A closer investigation led the author to identify the problem to be the type of barrier used for current blocking [KH92]. The reasons for leakage currents are pointed out in this thesis and solutions for reducing the leakage currents will be proposed based on the understanding of the *GaAs/AlGaAs* interface transport.

2.5.1 Reasons for High Leakage Currents

The authors of [RGK90] used a 200Å-wide $Al_{0.7}Ga_{0.3}As$ barrier. As discussed in the Section 2.2 on heterostructure fundamentals, in the $Al_xGa_{1-x}As/GaAs$ system, $Al_xGa_{1-x}As$ is an indirect bandgap semiconductor for *Al* concentrations $x > 0.41$. Using the equations given by [MCW86] and quoted in Section 2.2, the $\Gamma \rightarrow \Gamma$ barrier energy for $Al_{0.7}Ga_{0.3}As/GaAs$ is approximately equal to 560 meV and the $\Gamma \rightarrow X$ barrier is only 254 meV. This is indicated in Figure 2.11, which depicts the energy

Figure 2.11: Energy band profile of $Al_{0.7}Ga_{0.3}As/GaAs$ heterojunction barrier indicating competing $\Gamma - \Gamma$ and $\Gamma - X$ channels for electronic transport.

band profile including the $\Gamma - X$ discontinuity.

Thus the electron transport is not the simple $\Gamma - \Gamma$ tunnelling observed in direct semiconductor barriers. Elastic intervalley scatterings are possible between the Γ minimum and one of three X minima in the k_z direction in k -space for an incident Γ electron. The lateral ($k_x - k_y$) momentum conservation forbids transfers to the two lateral X minima in the k_x and k_y directions and to all L minima, while the momentum in the k_z direction is not conserved because of the potential discontinuities. The other X minima become important when scattering by, e.g., phonons, random alloys, and interface roughness are involved [Liu87].

Liu [Liu87] has treated this problem of $\Gamma - X$ transfer current theoretically by using a mixing factor for the Γ and X wavefunctions at the $AlAs - GaAs$ inter-

face, neglecting the effects of phonon and interface roughness scattering. The theory was later confirmed experimentally by Landheer et al [LLBS89], whose experimental results at 20 K agree with the theoretical model when the mixing factor is varied. Their experimental observations reveal that $\Gamma \rightarrow X$ tunneling becomes a significant contributor to the electron transport for $AlAs$ barrier thicker than $\sim 20\text{\AA}$.

Some convincing experimental measurements of barrier heights of $AlAs/GaAs$ heterostructures of different barrier widths ranging from $14\text{\AA}$ - $150\text{\AA}$ were made by Kyono et al. [KKN⁺89]. Their results suggest a significant contribution to conduction from the $\Gamma_{GaAs} - X_{AlAs}$ tunneling which occurs for $AlAs$ barriers as thin as $31.1\text{\AA}$ and the conduction is well described at room temperatures by thermionic emission over a 0.2 eV barrier. An attempt was made recently by Rossmanith et al. [RLK91] to explain the experimental activation energy measurements on thick $Al_xGa_{1-x}As$ barriers. They explained the measured activation energy by using a competing $\Gamma \rightarrow X$ transmission model and associating a 'prefactor' to represent a changing ordinate intercept for different barrier compositions.

2.5.2 Proposed New Structures and Preliminary Results

The above study convinced the author that in SBVs where thicker barriers of the order of $200\text{\AA}$ are needed for effective current blocking, one should use a direct $Al_xGa_{1-x}As$ barrier that can offer a $\Gamma \rightarrow \Gamma$ barrier height of 280 meV for $x = 0.4$ [KH92]. Further attention has to be paid to the spacer layers grown between the depletion layers and the barrier. Apart from the purpose of preventing migration of the dopants into the barrier regions during the MBE growth, the spacer regions also serve to increase the effective heights of barriers [DLBH⁺89].

Pseudomorphic layers of $In_xGa_{1-x}As$ spacers have been used to increase the conduction band discontinuity with increased sheet concentrations and electron mobilities [UM88]. However care has to be taken since only thin films of dislocation-free $InGaAs$ can be grown due to a lattice mismatch of 6.7% between $GaAs$ and $InAs$ [Sze91].

Figure 2.12: *GaAs* varactor MBE layers. Four variants differ in the barrier and spacer design as outlined in Table 2.1.

Figure 2.13: Conduction band energy profile of various structures. 1206 has *InGaAs* spacer-wells while the 1411/1412 Γ profile shows a chair-like profile.

We propose to use $50\text{\AA}$ spacers of $In_{0.2}Ga_{0.8}As$ on either side of the barrier. The total $In_{0.2}Ga_{0.8}As$ thickness of $100\text{\AA}$ is less than the experimentally reported critical thickness of $165\text{\AA}$ [ACK⁺87]. The $InGaAs$ spacer-well is shown in the conduction band profile of Figure 2.13. This figure also shows a chair-like structure. The proposed SBV structures have depletion layers $3500\text{\AA}$ thick on both sides. The depletion doping is fixed at $N_d = 10^{17}cm^{-3}$. Contact layers $0.3\mu m$ thick on the top and $0.8\mu m$ thick on the bottom are doped to $3.5 - 4.0 \times 10^{18}cm^{-3}$. The depletion thickness is sufficient to accomodate a bias voltage of 7 V before the device can punch through. Four combinations of barrier and spacer layers were implemented, as shown in Figure 2.12 and Table 2.1.

Device	Spacers	Barrier Thickness and Composition
1205	$50\text{\AA} GaAs$	$250\text{\AA} Al_{0.4}Ga_{0.6}As$
1206	$50\text{\AA} In_{0.2}Ga_{0.8}As$	$250\text{\AA} Al_{0.4}Ga_{0.6}As$
1411	$50\text{\AA} In_{0.2}Ga_{0.8}As$	$60\text{\AA}/18\text{\AA}/60\text{\AA} - Al_{0.4}Ga_{0.6}As/AlAs/Al_{0.4}Ga_{0.6}As$
1412	$50\text{\AA} In_{0.2}Ga_{0.8}As$	$60\text{\AA}/40\text{\AA}/60\text{\AA} - Al_{0.4}Ga_{0.6}As/AlAs/Al_{0.4}Ga_{0.6}As$

Table 2.1: Proposed $GaAs$ varactor structures.

The wafer numbers 1411 and 1412 have a chair barrier profile in their conduction band diagram as indicated in Figure 2.13. Wafer 1411 has an $AlAs$ layer whose thickness is about the critical limit above which $\Gamma \rightarrow X$ tunneling starts to dominate the electronic transport. The measured current densities of the various $GaAs$ varactors is plotted in Figure 2.14. The proposed structures will be shown to have greater barrier heights than the early SBVs.

2.5.3 Other Approaches and Shortcomings

While improvements to the device's first structure were proposed by the author [KH92] and implemented [KHL⁺92] [KHL⁺94] there were reports of SBVs made on

Barrier and spacer	J (A/cm^2) at 0.4 V
(a) $Al_{0.7}Ga_{0.3}$ barrier, $GaAs$ spacer [RGK90]	10.4
(b) $AlAs/GaAs$ superlattice barrier $GaAs$ spacer [RSC ⁺ 92]	16.5
(c) $Al_4Ga_{0.6}As$ barrier and $In_{0.2}Ga_{0.8}As$ spacer [this thesis]	0.513

Table 2.2: Comparison of measured current density J of various varactors.

$GaAs$ by the University of Michigan group [RSC⁺92] and the University of California, Los Angeles group [LSD⁺93]. The UCLA group reported stacked heterostructure varactors on $GaAs$ but with no significant improvement in the current blocking capability. They used the same barrier $Al_{0.7}Ga_{0.3}As$ as used by the Chalmers team who proposed the first SBV. In their paper published in EDL the devices were leaky and the triplers were very inefficient as a result. The Michigan team used a superlattice barrier of 10 periods using $AlAs/GaAs$ $20\text{\AA}/20\text{\AA}$ with an idea of increasing the effective barrier height.

Again a closer look at the electronic character of the $AlAs/GaAs$ superlattice is essential. The effective barrier height of a superlattice is a function of the thickness of $AlAs$ and $GaAs$ layers. Ihm's tight band calculations [Ihm87] reveal that for a $20\text{\AA}/20\text{\AA}$ $AlAs/GaAs$ superlattice, the lowest conduction band state has an $AlAs$ X character, i.e. it supports inelastic tunneling from the $GaAs$ Γ band through the lower $AlAs$ X states. Thus the improvements in current blocking observed by the authors were not significant and incurred the expense of an effectively thick ($400\text{\AA}$) barrier and lower doping ($N_d = 2 \times 10^{16} \text{ cm}^{-3}$) as opposed to the $\sim 210\text{\AA}$ thick barriers and the $N_d = 10^{17} \text{ cm}^{-3}$ doping used in the first SBVs.

The authors also observed that the superlattice barrier varactor did not show capacitance variation C_{max}/C_{min} sufficient for any significant harmonic generation. Attempts to increase the capacitance swing by delta doping increased the leakage currents. A comparison of the current densities of the various varactors is given in Table 2.2. This demonstrates the effectiveness in current blocking of our structures.

Figure 2.14: Measured current densities of the four varactors 1205, 1206, 1411, and 1412. The layers are indicated in Table 2.1 and Figure 2.12.

Convincing microwave S_{11} measurements in Chapter 5 will reveal that the *GaAs* SBVs designed in this thesis exhibit a C_{max}/C_{min} ratio as high as 4.

2.6 Heterostructure Varactors on *InP*

The maximum barrier height realizable in the *AlGaAs/GaAs* system is limited to ~ 350 meV. The current blocking and breakdown voltage of the varactors can be improved by designing varactors with higher blocking barriers. In *InP*, the lattice matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ barrier of height ≈ 550 meV [PWAC83] is achieved with no limitations on the barrier widths. Higher $\Gamma - \Gamma$ (1.2 eV) and $\Gamma - X$ (0.64 eV) barrier height can be achieved with a pseudomorphic *AlAs* barrier. But the 3.7 % strain of *AlAs* limits the maximum thickness of the barriers to $\approx 100\text{\AA}$ [MH90]. A chair barrier of *InAlAs/AlAs/InAlAs* yields a high effective barrier and the strain can be accommodated in the system. This has been demonstrated by Reddy and Neikirk [RN93]. In addition to effective current blocking achieved using the *InGaAs/InAlAs* system, *InGaAs* cap layer makes possible a lower contact resistance than can be obtained on *GaAs*. We discuss the shortcomings of a SBV and propose a stacked SBV on *InP* for higher multiplier power outputs.

2.6.1 Output Saturation and Stacked Devices

Classical predictions of efficiency in a depletion-type Schottky varactor frequency multiplier indicates that the conversion efficiency increases up to the reverse breakdown limit. This prediction is violated in high frequency ($> 100\text{GHz}$) multipliers [Eri93] and saturation phenomena are observed at power levels lower than those needed for forward conduction or reverse breakdown [Eri90].

A closer look at this phenomenon by Kollberg et al. [KTFE92] revealed a basic limitation in *GaAs* Schottky varactors. These authors noted that the displacement current through the varactor depletion region is a direct function of frequency and

the power level of the input signal as given by

$$i_d(t) = C_d(t) \frac{dV_d}{dt} \quad (2.19)$$

where $C_d(t)$ is the depletion capacitance and $V_d(t)$ is the voltage across the depletion region. In a varactor diode the displacement current has to equal the electron conduction current $i_e = A_d n_e v_e(t) q_e$ through the undepleted semiconductor, where A_d is the diode area, the electron density $n_e \approx N_d$ the doping density, v_e is the electron velocity, and q_e is the charge of the electron. Since the electron velocity reaches a maximum v_{emax} at a given applied electric field, a saturation phenomenon is expected when $i_d \sim i_{sat} = i_{emax} = N_d v_{emax} q_e A_d$. This saturation carrier velocity is not easily increased and the only alternative is to decrease the current density. This can be done by using several diodes in series [Eri93] or by using diodes with larger areas.

2.6.2 Stacked Varactors: Advantages

The capacitance per unit area of the single barrier devices is typically high (2 – 4 mF/m²) [KHL⁺94]. To achieve realizable circuit-impedance levels at higher millimeter-wave frequencies, the device capacitance has to be small which in turn requires small areas. Smaller devices makes contacting to external circuits very difficult. Reducing the area also increases the contact resistance of the device. The increased value of R_s for small capacitance devices reduces the $\mathcal{F}$ and hence lowers the multiplier efficiency. The power output of single-barrier varactor triplers is limited to a couple of milliwatts at 200 GHz [RGK90].

The breakdown voltage can be increased by a factor of n , power output can be increased by a factor of n^2 and capacitance can be decreased by a factor of n by using n stacks of the single heterostructure barrier varactor. This has been demonstrated previously for a classical abrupt-junction varactor [SHOC87]. Equivalently a stacked device of larger area and power output capability can be realized for a given $R_s C(0)$ product.

We have made use of the MBE growth technique to grow stacked varactors that have lower R_S , higher V_b , and less susceptibility to current saturation. At higher millimeter-wave frequencies these varactors are potentially better than the Schottky varactors that are fabricated on *GaAs* and power-output constrained by velocity limited current saturation. Figure 2.15 shows the MBE layers of the stacked varactor concept developed in this work. It is the first demonstration of the stacked varactor concept using the heterostructure barriers on *InP* [KHR⁺94].

The velocity of electrons in *In_{0.53}Ga_{0.47}As* is higher than in *GaAs* and the current density per diode is lower in stacked varactors than single-barrier varactors having the same capacitance level. This reduces the effect of current saturation in high-power, high-frequency varactors.

The $I(v)$ characteristics of stacked and single barrier varactors on *InP* are obtained by probing the mesa devices and using a Tektronix $I(v)$ tracer. The single barrier devices were destroyed when the device voltage exceeded 5 V; the voltage across the stacked devices was not allowed to exceed 12 V. The current densities observed were lower than in *GaAs* varactors, as expected. The $I(v)$ traces are shown in Figure 2.16.

2.6.3 Previous Studies and the Current Approach

Increasing the power handling capability of varactors by series connection or stacking has been attempted by many authors. It was proposed by Uhler [Uhl58] as a means of building up the impedance of large junction structures to a more convenient level. *GaAs* monolithic frequency doublers using series connected varactor diodes were demonstrated by Chu et al. [CCC⁺86]. A power output of 150 mW at 36.9 GHz with 24 % efficiency was obtained.

The first attempt to make stacked varactors epitaxially was done by T.B. Ramachandran of M/A-COM in the early '80s. The structure is shown in Figure 2.17. The basic structure is a p^+n varactor structure with an n^+ layer separating each individual varactor. The devices being abrupt-junction type varactors, are basically

Figure 2.15: MBE layers of stacked *InP* varactor. The single barrier varactor has the same barrier and spacer layers and the depletion layer is $1 \mu\text{m}$ thick.

(a)

(b)

Figure 2.16: $I(v)$ curves of single and stacked varactor on InP . (a) A $61\ \mu m$ diameter single barrier device (b) A $40\ \mu m$ diameter stacked varactor device. Scale: Y axis- $100\ \mu A/div$, X axis- $2\ V/div$.

Figure 2.17: Schematic diagram of a p^+n junction varactor diode stack [CCC⁺86].

limited to useful operations below 100 GHz output frequency. Remarkable power outputs of 5.5 W at 35 GHz (60%), 5 W at 44 GHz (50%) and 0.28 W at 88 GHz (14%) were obtained with doubler circuits.

The M/A-COM device operates like a conventional varactor requiring bias and a second-harmonic idler for tripler circuits. In contrast, the stacked varactor tripler using the SBV concept does not require an idler or bias circuit. Intervening n^+ layers are not required in between the various varactor SBV layers. The additional parasitic resistance caused by the degenerate diodes, R_D is avoided. Further, the stacked SBV device is not limited by diffusion capacitance like the p^+n stacked varactor. Useful devices can be made to work in tripler circuits at frequencies where the p^+n stacked varactors have shown to exhibit performance limitations.

2.6.4 Conclusion

Stacked SBV structures with lower series resistance, lower specific capacitance and higher breakdown voltage are proposed. Low leakage is achieved by proper choice of the barrier.

The stacked SBV devices with the described structure are characterized (see Chap-

ter 5) by microwave S_{11} measurements in order to extract the model. The results of modeling and simulations in Chapter 4 show that very low series resistance and high unsaturated output power can be achieved using these devices.

2.7 Summary

The design of heterostructure barrier varactors has been developed at a conceptual level. The basic heterostructure fundamentals are laid out. This enables one to understand the issues of lattice matching, indirect tunneling and barrier heights essential for the heterostructure varactor design. Terminology of varactors are introduced so that the figures of merit can be invoked later to compare the various varactors. The problem of leakage currents in early single barrier varactors and reduced efficiencies resulting from lower quality factor are pointed out. New varactor layer design based on heterostructure fundamentals is carried out and the proposals detailed. Four new improved structures on *GaAs* and one novel stacked device on *InP* are proposed. The device characterization and tripler simulation and experimental results are detailed later in Chapter 5.

Chapter 3

Growth and Processing of the Varactor Devices

The varactor layers on *GaAs* and *InP* are designed to achieve improved current blocking compared to the early SBVs. Four *GaAs* varactor layers are designed. The four varactor layers and the design rationale are discussed in Chapter 2. Two wafers on *InP* are designed. The single barrier structure and the triple stacked varactor have the same barrier and spacer design as explained in Chapter 2.

3.1 MBE Growth of Varactors

The *GaAs* devices were grown by Dr. A. SpringThorpe, Bell Northern Research, Ottawa and Dr. Z. B. Wasilewski, National Research Council, Ottawa. The MBE system was a V80H system modified so as to achieve a thickness uniformity better than 1% over a 2 inch wafer. With the exception of the region containing the *InGaAs* wells all the rest was grown at a substrate temperature of 600°C. The *InGaAs* wells and the *AlGaAs/AlAs/AlGaAs* layers between them were grown at 500°C. This has been achieved in the following way: after finishing the 3500Å $N_d = 10^{17} \text{ cm}^{-3}$, layer the growth was suspended and the temperature ramped to 500 °C over 300 s. The

InGaAs/AlGaAs/AlAs/AlGaAs/InGaAs layers were grown next and an additional 200 Å cap of undoped *GaAs* was grown on the top before the temperature was ramped up to 600 °C again. This prevents the excess *In* in the top well from evaporating while the temperature is increased, which would alter the effective composition of the top *InGaAs* well.

The growth rate of *GaAs* was 2 Å/sec. *InGaAs*, *AlGaAs* and *AlAs* growth rates can be calculated from the compositions quoted. All layers were grown in the conditions where there is no re-evaporation of the group-III elements from the surface, so the growth rate of *AlGaAs* is the sum of the growth rates for the *GaAs* and *AlAs* (same for *InGaAs*). The growth rates were estimated first from the ongoing growth rate calibrations and then confirmed for *GaAs* and *AlAs* with the X-ray double crystal rocking curve measurement using as a reference the *GaAs/AlAs* multiple quantum well placed at the bottom of each layer. There was no independent confirmation of the *InGaAs* growth rate or composition, but *Ga* and *In* fluxes were found to be quite stable and the composition quoted is believed to be accurate to within 1%. Arsenic tetramer (As_4) was used as the group V element. The arsenic overpressure used was only slightly higher than that necessary to sustain *As* stabilized reconstruction for *GaAs* and *AlGaAs* layers.

The *InP* varactors layers were grown by Dr. M. Missous of the University of Manchester Institute of Science and Technology, UK. All the epitaxial layers were grown in a solid source VG V90H MBE machine. n^+ sulphur doped (100) *InP* substrates were used. The compositional accuracy of the *InGaAs* and *InAlAs* ternaries and the thickness of the *AlAs* barrier were determined from both in-situ Reflection High Energy Electron Diffraction oscillations and ex-situ double crystal X-ray crystallography. The growth conditions were those determined for best electrical properties of bulk, *InGaAs* and *InAlAs*, namely growth temperature of around 500°C and arsenic-to-group -III flux ratios of greater than 5. The *n*-type dopant used was silicon throughout.

Figure 3.1: Photomicrograph of processed *GaAs* varactor showing the device (120 μm by 120 μm square mesa).

3.2 Processing of the Wafers

The *GaAs* devices were processed by Dr. M. Buchanan of National Research Council, Ottawa. Square mesas 60, 120 and 240 μm on a side were defined with Shipley 1400-26 photoresist and then wet etched down to the back contact using 1:8:160 mix of $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$. Top and bottom contacts were then defined (with Shipley 1400-26 resist and a chlorobenzene soak after exposure to give an undercut profile. *NiGeAu* (250 Å / 550 Å / 800 Å) was evaporated by E beam, and the unwanted metal lifted away by immersion in a suitable solvent. The contact metal was then annealed at 415 °C for 15 sec in flowing H_2/N_2 using an AG Heat pulse 410 rapid thermal annealer [HCS80].

The single and stacked *InP* varactors were processed under the auspices of Dr. C. Rogers and Mr. G. Smith of Philips Microwave, Hazel Grove, UK. The active parts of the structures were grown with highly doped *InGaAs* contact layers on either side. *TiPtAu* ohmic contact layers were manufactured by pre-etch, sputter deposition

Figure 3.2: Photomicrograph of processed *InP* stacked varactor with the integral heat sink. Device wafers were processed by Philips Microwave, Hazelgrove, UK (42 μm diameter circular mesa).

and lift-off. This contact has been shown to have a specific contact resistance of approximately $5 \times 10^{-7} \Omega\text{cm}^2$. The mesas were wet etched with an etchant which etches *InGaAs*, *InAlAs* and *InP* at the same rate in all crystallographic directions.

It is possible to passivate the device by coating it with plasma-deposited silicon nitride. Connection may be made to the contacts by opening windows by wet or dry etching. The *InP* substrate was removed by selective etching. The back contact was plated to give a thickness of 50 microns of gold all over the wafer. The slice was alloyed in an inert atmosphere to bring the resistance of the contacts down to its lowest value. The gold heat sinks were wet etched using a cyanide-based etchant to give individual devices with a heat sink diameter of 300 μm and 50 μm thickness.

The devices were mounted into SOD-31 or MO-68 packages with *Au - Ge* and *Au - Sn* preforms in a forming gas atmosphere. Contact was by thermocompression bonding with gold wire. The top caps were attached by soldering for MO-68 and by welding for SOD-31.

Chapter 4

Tripler Analysis and Design

Linear or small-signal analysis can be done using constant capacitances and resistances. The frequency multiplier, being a highly nonlinear circuit, can be analyzed only by using large signal models. Large signal models have been defined for many active devices. The drain current in a MESFET is modeled as a voltage-dependent current source and many models have been used successfully to predict the performance of MESFET mixers and multipliers [Maa86]. These models are of the quasi-analytical type. The nonlinearity is expressed as a function of the dependent voltages and some empirical parameters are chosen to fit the model to the measured device nonlinear characteristics.

Traditional varactors such as abrupt-junction varactors and Schottky varactors have been modelled by simple charge-voltage or capacitance-voltage relationships. These relations stem from the physical picture of the voltage-dependent charge variation in the device. The symmetric varactor in general and the SBV in particular can be represented by a nice empirical $q - v$ relation that models the electrical measurement of the device capacitance. This relation can be conveniently used to predict the device performance in a highly non-linear circuit such as a frequency tripler.

4.1 Cubic Model (CM) for SBVs

The model was proposed in [KH93]. A charge-voltage relation for a symmetric SBV can be represented as

$$\alpha v = \frac{q}{q_0} + \beta \left(\frac{q}{q_0} \right)^3 \quad (4.1)$$

where v is the potential across the varactor (excluding R_s) and q is the charge associated with the varactor depletion region. In terms of normalized variables, Equation (4.1) becomes simply

$$y = z + \beta z^3 \quad (4.2)$$

where $y = \alpha v$, $z = \frac{q}{q_0}$. The parameters α and β can be adjusted to fit the $q-v$ relation (4.1) to the measured characteristics of an arbitrary symmetrical $C(v)$ varactor. From (4.1) we find the $C(v)$ relation that can be used to fit a measured $C(v)$. This is done by differentiating 4.1. If we introduce the definition of $C(v) = \frac{dq}{dv}$, we have

$$y = \alpha v = \pm \Psi^{1/2} [1 + \beta \Psi] \quad (4.3)$$

where

$$\Psi = \frac{1}{3\beta} \left(\frac{C(0)}{C(v)} - 1 \right). \quad (4.4)$$

and

$$q_0 = \frac{C(0)}{\alpha}. \quad (4.5)$$

A plot of the charge-voltage relationship, Equation (4.1) and the capacitance-voltage relation from Equation (4.3) are shown in Figures 4.1 and 4.2 respectively.

4.1.1 Analysis of Triplers

Tripler simulations using SBV and bbBNN⁺ varactors have been reported [PC90] [LHM87]. They were analyzed numerically using the Harmonic Balance (HB) technique. A small series resistance (or very high Q) varactor causes some numerical

Figure 4.1: Our proposed cubic charge-voltage model for symmetric varactors. The charge for zero bias is zero and the function is chosen to represent the depletion charge in the varactor. See Equation (4.1).

instability in harmonic balance simulations. Furthermore, harmonic balance simulations are computer intensive and do not offer an insight into the performance of the device in a tripler circuit.

A simple large-signal analysis of classical abrupt-junction pn-junction varactors in terms of a $q - v$ model has been given by Tang [Tan66]. The analysis given here follows Tang's approach. The device equivalent circuit consists of a series $C(v)$ and R_S . The circuit model shown in Figure 4.3 consists of ideal filters at ω and 3ω with source and load impedances Z_S and Z_L . The total current i flowing through the varactor diode is

$$i = I_1 \cos(\omega t) + I_3 \cos(3\omega t + \theta) \quad (4.6)$$

where θ is a phase angle to be determined. The normalized charge associated with

Figure 4.2: The $C(v)$ generated from the charge-voltage model. Note the symmetric $C(v)$ characteristics. For a given zero-bias capacitance, the C_{max}/C_{min} ratio is varied by varying the parameter β . The maximum device voltage can be varied by choosing the appropriate value of α . See Equation(4.3).

the depletion layer is

$$z = \frac{q}{q_0} = \frac{I_1}{q_0 \omega} \sin \omega t + \frac{I_3}{q_0 3\omega} \sin(3\omega t + \theta) \quad (4.7)$$

In the ideal case of perfect $q - v$ antisymmetry described by equation 4.1 the average charge is zero. The input power at ω is assumed to be sufficiently low that the diode is not driven to its breakdown voltage V_B . Substituting 4.7 into 4.2 the normalized voltage, y across the lossless ideal $C(v)$ element can be found. This voltage has third, fifth, seventh and ninth harmonics (but no higher-order terms):

$$y(\tau = \omega t) = \alpha v = Y_1 \cos(\tau - \zeta_1) + Y_3 \cos(3\tau - \zeta_3) + \dots \quad (4.8)$$

where Y_n and ζ_n are amplitudes and phases to be determined. Imposing the circuit

Figure 4.3: Shunt Z tripler circuit model for analysis.

conditions one finds the following equations:

$$Y_1 \cos \zeta_1 = -\frac{3}{4}\beta Z_1^2 Z_3 \sin \theta \quad (4.9)$$

$$Y_1 \sin \zeta_1 = Z_1 \left[1 + \frac{3}{2}\beta \left(\frac{1}{2}Z_1^2 + Z_3^2 \right) \right] - \frac{3}{4}\beta Z_1^2 Z_3 \cos \theta \quad (4.10)$$

$$Y_3 \cos \zeta_3 = Z_3 \left[1 + \frac{3}{2}\beta \left(Z_1^2 + \frac{1}{2}Z_3^2 \right) \right] \sin \theta \quad (4.11)$$

$$Y_3 \sin \zeta_3 = Z_3 \left[1 + \frac{3}{2}\beta \left(Z_1^2 + \frac{1}{2}Z_3^2 \right) \right] \cos \theta - \frac{1}{4}Z_1^3 \quad (4.12)$$

where Z_1 and Z_3 are the amplitudes of the normalized fundamental and third-harmonic charge components.

Defining the constraints to be (a) fixed input power $\mathcal{P}$ supplied to the nonlinear $C(v)$ element (i.e. not including R_s), and (b) minimum dissipation with respect to I_1 , the optimization condition is found to be

$$I_1 = (12)^{1/8} \left(\frac{\mathcal{P}}{M \sin \theta} \right)^{1/4} = \sqrt{3} I_3 \quad (4.13)$$

where

$$M = \frac{\beta}{4\omega^3 \alpha q_0^3}. \quad (4.14)$$

The tripler efficiency is

$$\eta = \frac{\text{power output}}{\text{power input}} = \frac{\mathcal{P} - \frac{1}{2}I_3^2 R_s}{\mathcal{P} + \frac{1}{2}I_1^2 R_s}. \quad (4.15)$$

Substituting the optimization condition, Equation (4.13) into Equation (4.15) the efficiency is

$$\eta = \frac{\sqrt{6\sqrt{3}\mathcal{P}M \sin \theta} - R_S}{\sqrt{6\sqrt{3}(\mathcal{P}M \sin \theta) + 3R_S}}. \quad (4.16)$$

The maximum efficiency occurs for a phase angle $\theta = 90^\circ$. This is also the condition for minimum dissipation.

The input and load impedances can be found as

$$Z_{in} = \left(\frac{V_1}{I_1} \cos \zeta_1 + R_S \right) + j \left(\frac{V_1}{I_1} \sin \zeta_1 \right) \quad (4.17)$$

$$Z_L = \left[\frac{V_3}{-I_3} \cos(\zeta_3 - \theta) - R_S \right] + j \left[\frac{V_3}{-I_3} \sin(\zeta_3 - \theta) \right]. \quad (4.18)$$

An interesting result that can be deduced from the above equations is

$$\frac{R_{in}}{R_L} = \frac{1}{3\eta}. \quad (4.19)$$

A design procedure for a tripler design would start with a fixed input power $\mathcal{P}$, diode parameters, α and β and frequency ω . Applying equation (4.13) I_1 , I_3 and hence Z_1 and Z_3 are found. With θ as 90° equations (4.9), (4.10), (4.11) and (4.12) can be solved for the unknown phase and amplitudes, ζ_1 , ζ_3 and Y_1 , Y_3 . Efficiency (η), Z_{in} and Z_L follow from equations (4.16), (4.17) and (4.18) respectively. A simple model like the above is very useful and will be shown to give results that agree qualitatively with a full-fledged computer-based harmonic balance simulation.

4.2 Computer-Based Multiplier Analysis

In practical single-barrier varactor devices the multiplication is not purely reactive. This is because of the device leakage currents. The multiplication process could be a hybrid of resistive and reactive multiplication. The classical theories of Penfield & Rafuse [PR62] and Burckhardt [Bur65] do not address the general multiplier problem of arbitrary nonlinearity, embedding impedances, drive levels or bias voltage. Using

Figure 4.4: Circuit for large signal harmonic balance analysis.

the Kerr's reflection algorithm [Ker75] in a computer program [SKH84] a general multiplier analysis can be performed [RGK90] [CFB93] [Nil94].

4.2.1 General problem

Figure 4.4 shows a general equivalent circuit of a multiplier circuit under large-signal excitation. The diode is represented by a large -signal equivalent circuit consisting of a nonlinear C and G in parallel along with a R_S in series. The embedding network is equivalent to a set of individual impedances ($Z_e(nf_p)$), each in series with an ideal filter. Thus the diode is terminated in a single impedance at each harmonic. The problem is to obtain the voltage waveform $v_d(t)$ given the embeddings, input power and the diode characteristics.

4.2.2 Reflection Algorithm and Multiplier Analysis

In Kerr's multiple-reflection technique the nonlinear multiplier circuit is divided into linear and nonlinear subcircuits and a long transmission line of arbitrary characteristic impedance Z_0 is inserted between these subcircuits. Choosing the length L of the transmission line to be an integral number of wavelengths at the fundamental frequency f_p (and hence also its harmonics) does not affect the circuit's steady-state response. However, the use of the transmission line allows one to treat the linear part in the frequency domain and the nonlinear part in the time domain.

The equivalent circuit of the multiplier is illustrated in Figure 4.5. The nonlinear subcircuit consists of the nonlinear conductance and capacitance of the varactor, and the linear subcircuit consists of the embedding network, bias and pumping sources and the diode series resistance.

After each of what will be termed a reflection cycle the terminal voltage and current in the linear and nonlinear subcircuits are compared. If the waveforms are the same then the large signal problem is solved, that is we have v_d and i_d equal to v_e and i_e in Figure 4.5. On the other hand, if the terminal conditions in the two networks differ, then the waveforms on the transmission line are changed in a predetermined fashion and the circuit analysis is repeated.

Consider the circuit of Figure 4.5. In general there will be a set of right- and left-traveling waves ($v_R(x, t)$, $v_L(x, t)$) on the transmission line. These waves are related to the voltage and current $[v(x), i(x)]$ at point x on the line by:

$$v(x, t) = v_R(x, t) + v_L(x, t), \quad (4.20)$$

and

$$i(x) = i_R(x, t) - i_L(x, t). \quad (4.21)$$

At the right-hand end of the transmission line these waves must conform to the boundary conditions imposed by the nonlinearities $C(v)$ and $G(v)$.

$$v_d(t) = v_R(L, t) + v_L(L, t) \quad (4.22)$$

Figure 4.5: Illustration of multiple reflection technique. A long transmission line having an arbitrary characteristic impedance Z_0 is inserted between the nonlinear and linear subcircuits of the frequency multiplier.

and

$$i_d(t) = i_R(L, t) - i_L(L, t) = \frac{v_R(L, t) - v_L(L, t)}{Z_0}. \quad (4.23)$$

At the left-hand end of the transmission line the voltage and current are

$$v_e(t) = v_L(0, t) + v_R(0, t) \quad (4.24)$$

and

$$i_e(t) = \frac{v_L(0, t) - v_R(0, t)}{Z_0} \quad (4.25)$$

respectively. However, this end is treated in the frequency domain, where it is convenient to express v_e and i_e as single-ended Fourier series.

$$v_e(t) = \sum_{n=-\infty}^{\infty} V_{en} \exp(j2\pi n f_p t), \quad (4.26)$$

$$i_e(t) = \sum_{n=-\infty}^{\infty} I_{en} \exp(j2\pi n f_p t), \quad (4.27)$$

where the Fourier series coefficients V_{en} and I_{en} related to harmonic n are, in general, complex.

Assume that the transmission line in Figure 4.5 is terminated in an impedance Z_0 until time $t = 0$ when the diode is first connected to the circuit. At time $t = 0^+$

a right propagating wave will exist on the transmission line (V_R , I_R) made up of components at DC and at the pump frequency. At the diode ($x = L$):

$$V_{R0}(x = L) = I_{R0}Z_0 = \frac{V_B Z_0}{Z_0 + R_S(0) + Z_e(0)} \equiv V_0, \quad (4.28)$$

for the DC component and

$$V_{R1}(x = L) = I_{R1}(x = 0)Z_0 = \frac{V_p Z_0}{Z_0 + R_S(f_p) + Z_e(1)} \equiv V_1 \quad (4.29)$$

at the input pump frequency. V_{Rn} and I_{Rn} are the Fourier coefficients of v_r and i_r .

In the time domain, the transmission line and diode can be replaced by the equivalent circuit of Figure 4.6 where the voltage components, V_{R0} and V_{R1} , are given by 4.28 and 4.29. The state equation for this circuit is:

$$\frac{dv_d}{dt} = \frac{\left\{ \frac{v_s(t) - v_d(t)}{Z_0} - i_{Gj}(t) \right\}}{C_j(t)}, \quad (4.30)$$

where $v_s(t)$ represents the sum of voltage sources in the equivalent circuit of the transmission line. Given an initial value of $v_d(t = 0)$ and the $I(v)$, $C(v)$ characteristics of the device, (4.30) can be solved numerically for $v_d(t)$ over a pump cycle, i.e. from $t = 2\pi m/\omega_p$ to $2\pi(m + 1)/\omega_p$. The Seigel and Kerr program uses the Runge-Kutta method to solve the differential equation.

Since the diode is nonlinear, the resulting steady state voltage waveform $v_d(t)$ will contain components at all the pump harmonic frequencies. This gives rise to a new left traveling wave on the transmission line of Figure 4.6. The amplitude of this wave is found from Equations (4.20) and (4.21)

$$v_L(x = L) = [v_d(t) - i_d(t)Z_0]/2. \quad (4.31)$$

In steady state since the transmission line is an integral number of wavelength long, $v_L(x = L) = v_L(x = 0)$, this wave is incident on the embedding network and in the frequency domain:

$$V_{Ln} = [V_{dn} - I_{dn}Z_0]/2, \quad n = 0, 1, 2, \dots, \infty, \quad (4.32)$$

Figure 4.6: The circuits which must be solved in the time domain to find the voltage and current at the diode terminals, (a) at time $t = 0$ when the right propagating wave contains components only at DC and the LO frequency and (b) for all successive iterations. The voltage sources together with Z_0 make up the equivalent circuit of the transmission line, which is in steady state with the diode.

where V_{dn} and I_{dn} are the Fourier series coefficients of the diode voltage and current over one pump cycle.

At the embedding network, part of this wave will be reflected. The reflected components are calculated at each pump harmonic frequency from the voltage reflection coefficient, ρ_n :

$$\rho_n = \frac{Z_e(n f_p) + R_S(n f_p) - Z_0}{Z_e(n f_p) + R_S(n f_p) + Z_0}. \quad (4.33)$$

The component reflected from the embedding network becomes the new right propagating wave on the transmission line of Figure 4.5 and can be expressed as:

$$V_{Rn} = \rho_n V_{Ln}, \text{ for } n > 1, \quad (4.34)$$

$$V_{R1} = \rho_1 V_{L1} + V_1, \text{ for } n = 1 \text{ and} \quad (4.35)$$

$$V_{R0} = \rho_0 V_{L0} + V_0, \text{ for } n = 0. \quad (4.36)$$

When this wave reaches the diode, the circuit of Figure 4.6b applies, where the additional voltage components produced by the diode on the previous cycle have now been included. The network state equation can be solved again for $v_d(t)$ over a pump cycle. The procedure is repeated until the absolute values of the voltage divided by the current at the two ends of the transmission line are identical at all the pump harmonic frequencies. Mathematically,

$$-\frac{V_{dn}}{I_{dn}} = \frac{V_{en}}{I_{dn}} = [Z_e(n f_p) + R_S(n f_p)] \text{ for } n > 1 \quad (4.37)$$

and

$$\frac{(V_p - V_{d1})}{I_{d1}} = [Z_e(f_p) + R_S(f_p)] \text{ for } n = 1. \quad (4.38)$$

Once the waveforms are obtained all other quantities follow:

4.2.3 Input Impedance

The input impedance of the multiplier at any port n is simply:

$$Z_{in\ n} = R_S + \frac{V_{dn}}{I_{dn}}. \quad (4.39)$$

4.2.4 Absorbed Power

Since the source impedance is not in general matched to the input impedance, only a portion of the available power will be absorbed:

$$P_{abs} = \frac{1}{2} Re[Z_{in1}] |I_{d1}|^2 \quad (4.40)$$

where the series resistance has been included in the input impedance term.

4.2.5 Output Power

The power delivered to the output port n with impedance Z_{en} is simply

$$P_{out} = 0.5 |I_{dn}|^2 Re[Z_{en}]. \quad (4.41)$$

4.2.6 Conversion Efficiency

The conversion efficiency will be defined here as the ratio of output power to the input power. If we assume perfect input matching then $P_{in} = P_{abs}$. In all our calculations perfect matching is assumed. Hence the efficiency in converting from input port 1 to output port n is:

$$\eta\% = \frac{P_{out}}{P_{abs}} \quad (4.42)$$

The Seigel and Kerr computer program [SKH84] is written in FORTRAN 77 and performs a full nonlinear analysis of a varactor diode that has frequency-dependent series resistance and arbitrary $I(v)$, $C(v)$ characteristics. It has been modified by Rydberg [RGK90] to accommodate the SBV tripler. The input file consists of $C'(v)$ and $I(v)$ data at various bias voltages. The embedding impedances at the harmonics

can be set arbitrarily. The input power, frequency, number of power steps, step size and series resistance are also input to the program during the run.

Figure 4.7: Measured $C(v)$ of one of the devices in this thesis and the fit using our cubic model (CM). See Equations (4.3)-(4.5). $\alpha = 0.98$ $\beta = 3.2$.

4.3 Illustrative Example: Comparing HB and CM

To demonstrate the validity of the cubic model (CM) we perform a computer-based harmonic balance (HB) analysis of the symmetric varactor tripler. The efficiency of the tripler and the embedding impedances at the fundamental and third harmonic at a given absorbed power are the sought after quantities. One of the varactors fabricated in this investigation is chosen. The varactor is characterized in Chapter 5 with the aid of RF measurements.

The parameters α and β are chosen so that the maximum and minimum ca-

Method	P_{in} [mW]	P_{out} [mW]	η %	R_1 Ω	X_1 Ω	R_3 Ω	X_3 Ω
HB	10.2	7.4	72.62	4.67	-52.69	11.23	24.67
CM	10.5	7.6	71.66	4.70	-47.19	10.13	21.90

Table 4.1: Comparison of the 10-30 GHz tripler analyses: Harmonic Balance versus Cubic Model.

capacitance described by Equation 4.3 and the measured $C(v)$ are the same and the breakdown voltage or maximum voltage are the same for both the capacitance fit and the measured device.

Figure 4.7 shows the measured RF capacitance and the capacitance given by the cubic model with $\alpha = 0.98$ and $\beta = 0.32$. Table 4.1 compares the numbers derived from the simple model and the algebraic analysis with the harmonic balance simulation of a 10-30 GHz tripler with measured $I(v)$, $C(v)$ and $R_S = 1 \Omega$. The agreement is remarkable considering the fact that the model is simple and does not need a computer to arrive at the efficiency and embedding impedances.

4.4 A 39 GHz Planar Tripler Design

The SBV tripler circuit theory and cubic model provide useful design information that can be translated into practical design. Designs for waveguide millimeter-wave triplers/doublers using packaged and whisker contacted varactors have been reported [Räi92] [Pet90]. But these multipliers do not exhibit mechanical characteristics which would allow them to survive harsh thermal or vibrational environments. In addition, they are costly to machine and require considerable assembly/tuning effort in order to achieve repeatability. They have demonstrated low conversion loss and broadband performance in relatively undemanding environments [Boc88]. But on the other hand planar technology can provide a mechanically rugged realization of the multiplier. The

previous results using SBV diodes were achieved in a whisker contacted waveguide technology. To the best knowledge of the author this thesis is the first to describe a planar SBV tripler at Ka band. The experimental results are reported in Chapter 5. This section describes a simple design procedure to realize a shunt Z multiplier of the kind illustrated in Figure 4.3.

4.4.1 Conceptual Design of a Planar Z Multiplier

The shunt mounted Z multiplier configuration of Figure 4.3 is very suitable for planar microstrip realization of an SBV tripler. The mesa device is mounted so that the heat is well sunk and the mesa tape-bonded both to the input and output side.

With the device mounted in a shunt configuration, the filters at ω and 3ω can be realized in microstrip. The complete circuit is fabricated on a 5-mil alumina substrate ($\epsilon = 9.9$) for a conceptual 39-GHz output tripler. The mount design is indicated in Figure 4.8. The tripler embedding impedance at the harmonics and fundamental frequency discussed in the previous sections can be realized by combinations of filters and matching circuits. The matching circuits at the input and output side of the device plane transform the device impedances to the nominal source and load impedance of $50\ \Omega$.

The planar tripler is detailed in Figure 4.9. The modules that make up the design are the input low-pass filter, input matching, output bandpass filter and output matching. Further, the input circuit should produce an open circuit to the output at the device plane and vice-versa. This is done by electrically moving the filter to the device plane by using phase-adjust $50\ \Omega$ lines that do not disturb the matching accomplished by the input and output matching circuits [IMATCH and OMATCH]. The equivalent circuit of the pumped device at the input and output frequencies determined from the cubic model or by harmonic balance is represented by R_1 and C_1 at the input and R_3 , C_3 at the output frequency.

Figure 4.8: Mount design for a planar SBV tripler .

Figure 4.9: Conceptualized tripler indicating the geometry of the circuit and the mount.

4.4.2 Design Steps and Details

The device chosen in the tripler design is a triple-stack symmetric SBV fabricated in this investigation. A zero-bias capacitance of 0.6 pF, series resistance of 0.3Ω and a break-down voltage of 14 V is achieved. The device is characterized by *S*-parameter measurements, the details of which can be found in Chapter 5. An HB analysis is performed to estimate the device impedance under full drive conditions.

The circuit design is broken down conveniently into input and output circuit designs. The input consists of a low-pass filter that passes the fundamental and rejects the third harmonic, together with a matching circuit that is used to realize the required impedance for the diode. The input low-pass filter is a high-low type of structure. The high impedance lines are chosen to be 1.9 mil thick, thicker than the minimum realizable width of $1 \tau^1$. The low-impedance section has a width 26.5τ . The length of the high- and low-impedance sections were chosen as optimization variables, with a specification of 20-dB attenuation for the second harmonic and 30 dB for the third harmonic. A TOUCHSTONE simulation (Appendix C) indicates less than 1 dB attenuation in the pass band, about 15 dB attenuation for the second harmonic and 23 dB for the third harmonic. The pass-band attenuation and return loss characteristics are shown in Figure 4.10.

The matching circuit design is a bit tricky. Stub matching is avoided due to frequency-sensitivity of the stubs and T junctions involved with them. A simple matching technique is used here. The $\lambda/8$ transmission line resonates the device to give a real impedance that is transformed to 50Ω to be connected to the low pass filter output. The impedance of the $\lambda/8$ transmission line is derived from Steinbrecher's work [Ste67]. The real impedance after the $\lambda/8$ transformation is of the order of 2Ω and a very low-impedance (wide) quarter-wave line is needed to match this to 50Ω . Return loss greater than 15 dB can be achieved over a 400 MHz bandwidth. The filter and matching circuit dimensions are indicated, in Figure 4.11.

¹1 mil = 1τ .

Figure 4.10: Simulated performance of the lowpass filter.

Figure 4.11: Input circuit of the planar 13 to 39 GHz tripler.

The length of the bondtape is about $260\text{ }\mu\text{m}$, that is $\lambda/30$ at 39 GHz. The tape can be regarded as a microstrip line with an air dielectric. The average height above the ground plane is used in the calculation. The output filter is designed as a three-section coupled line filter. Each section is electrically 90° long at the centre frequency. The coupling is varied so as to achieve minimum attenuation in the pass band and high attenuation for the second and fundamental frequencies. The output matching is very similar to the input matching. The results of the output bandpass filter design are shown in Figure 4.12. The output filter and matching circuit dimensions are indicated in Figure 4.13.

Figure 4.12: Simulated performance of the bandpass filter.

After the filters and matching networks are designed the final step is to move the input and output filters electrically to the device plane. This is done without perturbing the matching circuit by extending the filter with a $50\text{-}\Omega$ line and by varying the line length so that the output circuit, when loaded with the input, produces an open at the device plane and vice versa. Table 4.2 and Table 4.3 summarize the results. Figure 4.14 indicates the various design blocks involved and it relates to the blocks defined in the TOUCHSTONE (Appendix C) program.

Figure 4.13: Output circuit of the planar 13-39 tripler.

4.5 Summary

A new large-signal model for symmetric $C(v)$ devices has been proposed. This model is very general and is used in a large signal tripler analysis to yield closed form results for tripler efficiency and impedances. The numerical harmonic balance technique is explained and it is used to compare the results of a fully-driven SBV tripler with the cubic model results. A close agreement between the simple model and the computer analysis is found. A practical 39-GHz tripler design is outlined. The next chapter will compare the results of detailed tripler analyses with data published elsewhere.

Tripler Input Circuit Design

Tripler Output Circuit Design

Figure 4.14: Design diagram indicating the design objectives and the various circuit blocks.

Freq (GHz)	TRIPIN dB[S ₁₁]	INLOAD Re[Z ₁₁]	INLOAD Im[Z ₁₁]
12.6	-3.844	206.894	449.839
12.7	-5.067	925.483	522.487
12.8	-7.009	565.480	-622.517
12.9	-10.331	143.653	-403.257
13.0	-16.993	59.949	-272.070
13.1	-21.643	32.355	-203.142
13.2	-12.454	20.173	-161.598
13.3	-8.285	13.782	-133.931

Table 4.2: Input matching circuit performance when loaded with output matching and filter.

Freq (GHz)	TRIPOP dB[S ₁₁]	OPLOAD Re[Z ₁₁]	OPLOAD Im[Z ₁₁]
38.0	-13.55	632.44	30.10
38.2	-16.45	220.98	-378.11
38.4	-21.12	63.48	-256.57
38.6	-28.22	20.20	-167.70
38.8	-24.87	15.33	-150.88
39.0	-19.69	9.71	-126.11
39.4	-14.79	4.99	-95.19
39.8	-12.38	3.14	-75.87

Table 4.3: Output matching circuit performance when loaded with input matching and filter.

Chapter 5

Experimental Results and Discussions

The advantages of symmetric varactors were pointed out in Chapter 1. The problem of leakage currents with the early single-barrier varactors was pointed out and solutions were proposed in Chapter 2. This chapter deals with the experimental setup, theory and results to establish the potential and capabilities of newly proposed structures. The device improvements are pointed out and established by cryogenic measurements. High-frequency measurement techniques are used to accurately characterize the diodes. Large signal simulations using the measured results confirm the potential improvements possible with the new structures. A proof-of-concept planar tripler design is evaluated at Ka band to establish the usefulness of the new stacked *InP* varactor demonstrated for the first time.

5.1 Barrier Height Measurements of *GaAs* Varactors

The efficiency of varactor frequency triplers is a direct function of the quality factor (Q) of the devices. This Q factor defined in Chapter 2 deteriorates with increasing leakage conductance G through the barrier. The barrier height represents the ability of the varactor to block the deleterious conduction current. A higher barrier height would mean less G and higher Q . The improvement of device Q by using low-leakage barriers has to be substantiated by barrier height measurements. The theoretical basis of such a measurement is explained along with the experimental setup and results. The barrier heights of varactor devices are improved by a factor of 2, resulting in reduced device conduction currents.

5.1.1 Barrier Height and Activation Energy

We have to identify the difference between the conduction band discontinuity or the barrier height, ΔE_c and the activation energy ϕ_e . A portion V_a of the total bias voltage is accounted for by the accumulation of electrons in front of the barrier. The conduction band discontinuity ΔE_c is independent of applied voltage. Because of the accumulation of electrons in front of the barrier, the activation energy is a function of applied voltage V . The conduction band offset is the sum of the zero-bias activation energy ϕ_e and $\eta_F = \frac{E_F - E_c}{k_B T}$. The various energies are indicated in Figure 5.1.

5.1.2 Measurement Technique

The activation energy can be measured on the basis of thermionic emission theory. This theory relates the flux of carriers incident upon the interfacial barrier, with sufficient energy to overcome it, to the temperature T and the activation energy ϕ_e . The current density is given by the expression

Figure 5.1: Diagram indicating ΔE_C and activation energy, ϕ_c . The activation energy as a function of bias is found from the measurements. The discontinuity can be evaluated from the zero bias (extrapolated) activation energy and the term η_F that is determined from the Joyce-Dixon approximation.

$$J \approx A^* T^2 \exp(-\phi_c/k_B T), \quad (5.1)$$

where A^* is the effective Richardson constant and k_B is Boltzmann's constant. The activation energy is a complicated function of the bias voltage, although at low bias it is approximately equal to $\Delta E_c + \eta$ [BW86].

Rearranging Equation (5.1) yields

$$\ln(J/T^2) \approx \ln(A^*) - \phi_c/k_B T = \ln(A^*) - \Delta E_c/k_B T - \eta_F/k_B T \quad (5.2)$$

Assuming that ΔE_c is not temperature dependent, then the activation energy obtained from a plot of the function $\ln(J/T^2)$ against $1/T$ is approximately the conduction band discontinuity ΔE_c .

Figure 5.2: Experimental set up to measure $I(v)$ characteristics of chip *GaAs* devices at various temperatures. The data is used to extract the barrier height of the various structures.

The experimental setup for measuring ϕ_e is shown in Figure 5.2. The sample is mounted at the tip of the APD Cryogenics expander. The expander is connected to an APD compressor connected to a water cooler. The expander acts as the system refrigerator. The Scientific Instruments 5500 temperature controller is connected to the resistance heater in the expander near the sample. The sample is wire bonded to a dual-in-line package before it is mounted. The sample is connected to a Keithley 236 source measure unit controlled by a computer via an IEEE 488 bus. Before the APD compressor is turned on, the expander is brought to vacuum pressure (≈ 2 Torr) using a pump.

The $I(v)$ characteristics of the devices are all recorded at various temperatures from 77 K to 300 K. Plots of $\ln(I/T^2)$ versus $1/T$ at $V=0.2$ volts are shown for 1205 (Figure 5.3) and 1411 (Figure 5.4) devices. A straight line with constant slope is observed in the plots. This is to illustrate that the $I(v)$ curves display thermionic-emission characteristics at low bias voltages and temperatures between 200 K and 300

2 of/de 2

PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

K. This assumption of thermionic emission explains the electron conduction behaviour in thin ($\sim 125\text{\AA}$ in 1411 and 1412 devices) as well as thick ($\sim 250\text{\AA}$ in 1205 and 1206 devices) barriers. Figures 5.3 and 5.4 substantiate the thermionic emission hypothesis. At lower temperatures and higher voltages tunneling contribution to the electron transport becomes more significant.

Figure 5.3: Plot of I/T^2 (log scale) versus $1000/T$ for a $120 \times 120 \mu\text{m}^2$ 1205 device that has a thick barrier ($250 \text{\AA}$). The bias voltage is 0.2 V. The straight line portion indicates the validity of the thermionic emission theory to calculate ΔE_c .

5.1.3 Measurement Results

The activation energy determined by the procedure described above is plotted in Figure 5.5 for the various devices as a function of bias voltage. The zero bias activation energy is found by linear extrapolation. The conduction band discontinuity, ΔE_c is found from the measured zero-bias activation energy by knowing the Fermi level. The Fermi level is a strong function of doping adjacent to the barrier. Though

Figure 5.4: Plot of I/T^2 (log scale) versus $1000/T$ for a $120 \times 120 \mu m^2$ 1411 device that has a thinner chair barrier ($125\text{\AA}$). The bias voltage is 0.2 V. The straight line portion indicates the validity of thermionic emission theory to calculate ΔE_c .

the design value of the doping density is $N_d = 10^{17} \text{ cm}^{-3}$, the measured values from SIMS analysis indicate the actual doping in the wafer. We find from SIMS measurement (Appendix A) that in the 1205/1206 devices N_d is $8 \times 10^{16} \text{ cm}^{-3}$ and in 1411/1412 devices the doping concentration is $2 \times 10^{17} \text{ cm}^{-3}$. The position of Fermi level relative to the conduction band edge is found to be $\eta_F = -13 \text{ meV}$ for 1411/1412 and $\eta_F = -41.6 \text{ meV}$ for 1205/1206 devices using the Joyce-Dixon approximation [Bla82]. The conduction band discontinuities ΔE_c are shown for the various barrier-spacer combinations in Table 5.1.

5.1.4 Discussion

The results are consistent with improvements suggested in reference [KH92]. The first reported varactors were lossy, as explained in Chapter 2, with a barrier height

Barrier	Spacer	Barrier Height ΔE_C (meV)
$Al_{0.4}Ga_{0.6}As$	$GaAs$	249
$Al_{0.4}Ga_{0.6}As$	$In_{0.2}Ga_{0.8}As$	322
$Al_{0.4}Ga_{0.6}As/18\text{\AA}AlAs/Al_{0.4}Ga_{0.6}As$	$In_{0.2}Ga_{0.8}As$	372
$Al_{0.4}Ga_{0.6}As/45\text{\AA}AlAs/Al_{0.4}Ga_{0.6}As$	$In_{0.2}Ga_{0.8}As$	337

Table 5.1: Measured barrier heights of the various varactors.

Figure 5.5: Plot of activation energy versus bias voltage for various $GaAs$ devices. The activation energy at each bias point is determined from the slope of the plot $\ln I/T^2$ versus $1/T$ as indicated in Figure 5.4 and 5.3.

of 180 meV [RGK90]. The barrier height of the varactors can be improved by using an $Al_{0.4}Ga_{0.6}As$ barrier and $GaAs$ spacers yielding improvement $\Delta E_c = 249.4$ meV. Further improvements are realized by using $In_{0.2}Ga_{0.8}As$ spacers resulting in $\Delta E_c = 322.2$ meV.

A chair-barrier design, consisting of $Al_{0.4}Ga_{0.6}As$ with a small ($\approx 20 \text{ \AA}$) central $AlAs$ layer and pseudomorphic $In_{0.2}Ga_{0.8}As$ spacers, is seen to provide the highest barrier of height 372 meV. Increasing the indirect $AlAs$ thickness to 45 $\text{\AA}$ reduces the barrier height to 337 meV. This result reinforces the finding [KKN⁺89] that for single $AlAs$ barriers, the barrier height ΔE_c decreases as barrier thickness increases beyond $\sim 20 \text{ \AA}$.

This study of methods for reducing the leakage current has implications on the design of heterojunction field effect transistors (HFETs) that use undoped $Al_xGa_{1-x}As$ as a gate insulator. There is no doped $AlGaAs$ layer that would have a trapping behavior, moreover the threshold voltage of the device is governed by the material and its composition, not by its thickness and doping, as in the case of MODFETs.

In the design and development of insulated-gate FETs the gate leakage currents have to be minimized. The results obtained for ΔE_c should also provide some guidelines for reducing the gate current of the insulated-gate field effect transistors.

5.2 Device Characterization

An accurate equivalent circuit model is the basis for any non-linear circuit analysis. This model can be extracted from microwave measurements made on a mounted device. At microwave frequencies, terms such as "impedance" and "network" have meaning only with reference to specific transmission-line modes at physically localized terminal planes. Thus, the modeling and analysis of a mounted microwave diode, using the equivalent circuit of the diode and of the mount, requires that the interface between the two circuits be defined for a single mode at a specific reference plane [Get66].

In the case of a single-barrier varactor device appreciable leakage currents can flow through the device and conventional capacitance bridges cannot be used to measure the $C(v)$ characteristics. However, by measuring device S parameters in a special mount it is possible to deduce the conductance and capacitance from the reflection coefficient [TNB⁺91].

5.2.1 Microwave Measurement of *GaAs* Devices

The mounting and characterization of the diode depend on the size and type of the diode. Accurate characterization of these devices with coplanar wafer probes is possible if the devices are planar and the device mask is designed for the purpose. Standard available masks for upright¹ diodes were used both for *GaAs* and *InP* devices. The *GaAs* devices were fabricated from the following four wafers and the dimensions of the layers were determined by transmission electron microscopy (TEM).

1. 1205: a 262-Å $Al_{0.4}Ga_{0.6}As$ barrier with 50-Å *GaAs* spacers,
2. 1206: a 274-Å $Al_{0.4}Ga_{0.6}As$ barrier with 58-Å $In_{0.2}Ga_{0.8}As$ spacers,
3. 1411: a 62-Å/18-Å/62-Å $Al_{0.4}Ga_{0.6}As/AlAs/Al_{0.4}Ga_{0.6}As$ chair barrier with 58-Å $In_{0.2}Ga_{0.8}As$ spacers,
4. 1412: a 63-Å/45-Å/63-Å $Al_{0.4}Ga_{0.6}As/AlAs/Al_{0.4}Ga_{0.6}As$ chair barrier with 46-Å $In_{0.2}Ga_{0.8}As$ spacers.

Devices with areas $60 \times 60 \mu m^2$, $120 \times 120 \mu m^2$ and $240 \times 240 \mu m^2$ were made from all the four wafers. These devices were primarily made to do some DC $I(v)$ measurements to determine barrier heights. Since we know that capacitance is proportional to area, and that the device capacitance is an important parameter relating to the performance of these devices in tripler circuits, great insight can be obtained by accurate characterisation of these devices. Many a paper has been published in this area

¹Upright devices are non-planar mesa devices that are contacted from the top.

without the device being characterized accurately. Low-frequency capacitance-bridge measurements have been made [LSD⁺93] [RSC⁺92] but these investigations were not able to predict the capacitance when the leakage currents increase.

When leakage currents are present, true $C(v)$ characteristics and other model parameters can be extracted by measuring small-signal S parameters at various bias points and fitting an equivalent circuit that represents the fixture and mount. We decided to characterize the devices from wafers 1411 and 1206 that had good low-leakage characteristics.

The devices were diced and mounted on a sample holder shown in Figure 5.6 at the end of a 25-mil 50- Ω line on an alumina substate that is epoxied to a gold-coated Kovar carrier. A GE varnish is used to glue the chips to the carrier (ground). The chips have the ground on the SI *GaAs* substrate. A wirebond is used to connect the top mesa to the end of the line and another from the bottom of the diode to the ground.

A number of these sample holders (mounts) were made. They fit into the Wiltron Universal Test fixture that comes with a standard microstrip calibration kit to calibrate out the effect of coax-microstrip transition. The sample holders can be inserted and removed from the jaws of the test fixture and repeatable connection and calibration is possible. A standard one-port calibration with an open, short and load is done.

The de-embedding of the transmission lines together with bond wires is done using the EEsof TOUCHSTONE software². The device zero-bias capacitance deduced from low-frequency bridge measurements ranged from 100 pf to 10 pf. The inductance of bond wires was of the order of ~ 1 nH and the series resonance was observed in the 100 MHz -1 GHz range.

The 1206 devices with less current were characterized from -3 to 3 V and the 1411 devices were characterized in the range ± 2.5 V. Devices with different areas were characterized to observe whether they scale with area. Most of the nonlinearity of

²TOUCHSTONE is Trademark of EEsof, Lindero Canyon Rd., Westlake Village, CA 91362.

CHARACTERIZATION OF GaAs CHIP DEVICES

Figure 5.6: A mount for measurement of *GaAs* chip devices. The chip devices are connected to the end of a 50- Ω microstripline.

the $C(v)$ lies in the measurement range and the devices tend to be lossy beyond the range of normal bias voltages. This is observed from the reflection measurement plots in Figure 5.7 and 5.8 taken on a 1206 device connected to the transmission line at four different voltages.

Excellent $C(v)$ modulation, $\frac{C_{max}}{C_{min}}$ can be deduced by observing the change in resonant frequency as the bias is varied. If the diode is thought of as a series resonant circuit transformed by a transmission line it is not difficult to notice a variation of resonant frequency by a factor of 2, i.e. capacitance changing by a factor of 4. The $C(v)$ plots of 1206 and 1411 devices are shown in Figure 5.9 and Figure 5.10 respectively. The $In_{0.2}Ga_{0.8}As$ spacers combine the advantage of good current blocking with capacitance modulation. Incidentally, the work in this thesis is the first report on $C(v)$ measurements of heterostructure barrier varactors with $In_{0.2}Ga_{0.8}As$ spacers.

Some attempts by other researchers to achieve good current blocking resulted in no significant capacitance modulation [Nil94]. But devices from the 1206 wafer exhibited both current blocking and capacitance modulation.

The high values of series resistance observed are due to the poor ohmic contacts. These measurements have been successful as proof-of-concept for smaller microwave devices. The microwave measurements along with barrier-height measurements can be used as a guide to design single-barrier heterostructure varactors. The $C(v)$ model extracted along with the $I(v)$ characteristics will be used later to simulate triplers. It will be shown that the excessive leakage currents of earlier devices result in saturation effects of output power whereas a device with good $C(v)$ modulation and small leakage such as 1206 can be used to design triplers without output power saturation at low input power levels.

5.2.2 Characterization of Packaged Devices on InP

Microwave characterization of two-terminal reactive devices differs substantially from that of three-terminal devices. Three-terminal devices such as MESFETs and HEMTs

S11 FORWARD REFLECTION
IMPEDANCE

CH 3 - S11
REF. PLANE
0.0000 mm

MARKER 1
0.3538 GHz
2.628 Ω
279.371 $\mu\Omega$

MARKER TO MAX
MARKER TO MIN

$V=0$ V, $J=2.83 \times 10^{-7}$ A/cm², $f_{res}=353.8$ MHz, $C=27.39$ pF.

(a)

S11 FORWARD REFLECTION
IMPEDANCE

CH 3 - S11
REF. PLANE
0.0000 mm

MARKER 1
0.5644 GHz
2.789 Ω
311.233 $\mu\Omega$

MARKER TO MAX
MARKER TO MIN

$R_S+R_G=2.789 \Omega$

$V=1$ V, $J=2.69$ A/cm², $f_{res}=564.4$ MHz, $C=10.5$ pF.

(b)

Figure 5.7: Network analyser displays showing the input vector reflection coefficient at various bias points. The device and the embedding can be thought of as a lossy series resonance circuit whose resonance varies with bias voltage. (a) S_{11} trace for $v_d = 0$ V. (b) S_{11} trace for $v_d = 1.0$ V.

S11 FORWARD REFLECTION
IMPEDANCE

CH 3 - S11
REF. PLANE
0.0000 mm

MARKER 1
0.6508 GHz
3.547 Ω
28.361 $j\Omega$

MARKER TO MAX
MARKER TO MIN

$$R_S + R_G = 3.547 \Omega$$

$$V = 2 \text{ V}, J = 11.2 \text{ A/cm}^2, f_{\text{res}} = 650.8 \text{ MHz}, C = 7.7 \text{ pF}$$

(a)

S11 FORWARD REFLECTION
IMPEDANCE

CH 3 - S11
REF. PLANE
0.0000 mm

MARKER 1
0.6994 GHz
8.456 Ω
2.037 $j\Omega$

MARKER TO MAX
MARKER TO MIN

$$R_S + R_G = 8.456 \Omega$$

$$V = 3 \text{ V}, J = 31 \text{ A/cm}^2, f_{\text{res}} = 699.4 \text{ MHz}, C = 6.36 \text{ pF}$$

(b)

Figure 5.8: S_{11} of device 1206 measured using the special mount: (a) $v_d = 2.0 \text{ V}$ (b) $v_d = 3.0 \text{ V}$. A $C_{\text{max}}/C_{\text{min}}$ ratio of 4 is deduced from the graphs by measuring the resonance frequency. Accurate de-embedding also reveals the same $C_{\text{max}}/C_{\text{min}}$ ratio.

Figure 5.9: The $C(v)$ characteristics of two 1206 varactors having different areas. The $C(v)$ curves are obtained from microwave reflection measurements using a special mount.

have input and output impedances comparable to the characteristic impedance of the measurement system so that the device can be embedded in a $50\text{-}\Omega$ microstrip line and details of the device characteristics can be conveniently found following de-embedding. With three terminal devices the transfer characteristic is of major importance and this too can be conveniently and accurately obtained. The impedance of high- Q varactors differs significantly from the characteristic impedance and is closer to the unit circle in the Smith chart.

The Q of a microstrip transmission line is lower than that of a coaxial transmission line of the same Z_0 . Further, the microstrip standards used for calibration are not available for all substrates. Our mounts were made on 25-mil alumina but calibration

Figure 5.10: The $C(v)$ characteristics of two 1411 chair-barrier varactors having different areas. The specific capacitance (mF/m^2) is plotted. The device capacitances are found to scale with area.

standards were available on a 10-mil substrate. This might affect the accuracy of measurement when characterizing high Q devices. Further, calibration up to the device plane needs a 2-port TRL calibration.

Coaxial one-port techniques for packaged devices allow repeatable and accurate measurement of device impedance [SCST93]. The measurement set up consisted of a APC-7mm line connected to the measurement port of HP 8510 Network Analyzer. A very accurate one-port calibration can be made to the end of the line using standard open, short, fixed load and broadband sliding load.

Figure 5.11 shows the set up used for coaxial one-port measurement. The chip is

mounted on the inner post of a standard S4 package with a layer of conducting epoxy, which is cured for 2 hrs at 200 °C. Wiring with V-bond using 17 μm wire is carried out with a work table temperature of 175 °C and a hot bonding tip temperature of 210-230 °C. The bonding wedge was Microswiss type 5006. The top cap is welded and sealed after bonding.

The S4 package fits into the coaxial APC-7 mm line to form an uniform coaxial system, as shown in Figure 5.11 . The top cap end of the package comes in contact with a back-short. The equivalent circuit of the package and the chip are also indicated. C_p is the capacitance between the lower portion of the post through an air gap and ceramic ring to the top cap, and C_1 is the capacitance from the top portion of the post, through an air gap and the ceramic ring to the top cap. L_p is mainly due to the inner post and assumed to be coaxial [OC70].

CAD software can be used to extract the intrinsic device characteristics from the measured S parameters. But one has to know the intervening embedding well enough to determine the package equivalent circuit values that accord with reality. We can use the equivalent circuit of Figure 5.11 and use the initial estimates of equivalent circuit elements in a fitting program to match the measured response of the package. This is done using a linear microwave circuit analysis and optimization software TOUCHSTONE as was done for chip devices on the microstrip mount. The package parameters are determined as outlined in Appendix D.

Once the package is characterized and understood we are in a position to characterize the varactor devices in a package. The bias voltage across the device is applied via the internal bias T of the HP8510 Network Analyzer. The S parameters are measured at discrete bias voltages -5 V to 5 V for the single barrier device and -12 V to 12 V for the stacked device. The real part of the device impedance plotted in Figures 5.12 and 5.15 reveals that the device conductance is very low even at high bias voltages, 4 V for the single barrier and 12 V for the stacked device. The real impedance also is quite invariant with bias whereas the reactance plots in Figures 5.13 and 5.14 indicate that the capacitance changes with device bias. The fitted $C(v)$

CHARACTERISATION OF VARACTORS USING A COAXIAL MOUNT

Figure 5.11: The coaxial mount used to characterize high- Q packaged *InP* varactors. The sketch also outlines the S4 package with the equivalent circuit elements relating to the physical package.

Figure 5.12: A plot of real impedance of a packaged *InP* stacked varactor as a function of frequency. Resonance occurs close to 6.0 GHz and $R_S = \text{Re}[Z_{11}]|_{v_d=0V} = 0.28 \Omega$.

for the single and stacked *InP* varactor devices are shown in Figure 5.16 and 5.17 respectively. The $62\text{-}\mu\text{m}$ diameter with a single barrier of *InAlAs/AlAs/InAlAs* is found to have a zero-bias capacitance of $C(0) = 4.1 \text{ pF}$, $R_S = 0.376 \Omega$ and $C_{\text{max}}/C_{\text{min}}$ ratio of 4. The device broke down at 5.78 V and has a $C_{\text{max}}/C_{\text{min}}$ ratio of 4. A $41.7\text{-}\mu\text{m}$ diameter type triple-stacked varactor using the same barrier has a $C(0) = 0.6 \text{ pF}$, $R_S = 0.28 \Omega$ and $C_{\text{max}}/C_{\text{min}}$ ratio of 3. The stacked varactor broke down at 14.25 V. The breakdown in both the devices was destructive, i.e. they behave as short circuits after breakdown. It is believed that the barrier is destroyed. While the zero-bias capacitance of the stacked varactor scales by a factor of three, the breakdown voltage does not scale by the same factor. Furthermore $C_{\text{max}}/C_{\text{min}}$ of the stacked device is 3 as opposed to expected value of 4 as in a single barrier case. The author believes the lowering in the $C_{\text{max}}/C_{\text{min}}$ ratio of the stacked varactor is due to insufficient depletion

Figure 5.13: A plot of imaginary impedance of a packaged stacked *InP* varactor as a function of frequency. Resonance occurs close to 6.0 GHz and $R_S = \text{Re}[Z_{11}]|_{v_d=0V} = 0.28 \Omega$.

layer thickness. The single barrier varactor has depletion regions $1 \mu\text{m}$ long on both sides of the barrier; these layers are not depleted at breakdown. The depletion regions of the stacked varactor are thinner ($3500 \text{ \AA}$), so punch through occurs at 14.25 V.

The series resistance is accurately determined by noting that at zero bias, the real part of the device impedance when resonated gives the series resistance, R_S . Measured series resistance for the single barrier device is 0.37Ω and for the stacked device $R_S = 0.32 \Omega$. This agrees qualitatively with a calculation based on a simple model for R_S taking into account the contact, spreading resistance of the substrate (heat sink in the case of a stacked varactor), resistance of the contact, and undepleted active layer. Details of the model can be found in Appendix B. The calculated value of R_S is 0.26Ω for the single barrier device and 0.33Ω for the stacked device. The impedance measurement and modeling demonstrates a very accurate method of characterizing

Figure 5.14: A plot of imaginary impedance of a packaged single barrier *InP* varactor as a function of frequency. Good capacitance modulation is indicated by the change in the resonance frequency with bias.

two-terminal devices in general and high- Q varactors in particular.

5.3 Effective Barrier Width and $C(v)$ Measurements

In a single-barrier varactor the current blocking is achieved by an undoped barrier in the center of the structure. In the epitaxial growth process the doping has to be changed from the N_d value of the depletion region to a very low value for the barrier regions. The barrier layer being thin takes a very small time to grow. The abruptness in the various device layers is also a function of the growth rate. In practice spacer layers are grown and they help the growth, i.e. they prevent the diffusion of impurities into the barrier during dopant switching. The SIMS measurement described in

Figure 5.15: A plot of real impedance of a packaged stacked *InP* varactor as a function of frequency. $R_S = 0.37 \Omega$.

Appendix A reveals the doping profile in the depletion region. The observed profile is not a perfectly uniform profile. There is also a change in N_d to $8 \times 10^{16} \text{ cm}^{-3}$ (in the case of 1206) and $2 \times 10^{17} \text{ cm}^{-3}$ (in the case of 1411) from the design value of 10^{17} cm^{-3} .

Ideally, the zero-bias capacitance depends on the metallurgical barrier width. But in practice it is a complex function of barrier width, growth rate, dopant density and spacer dimensions. The effective width of the barrier can be found from the capacitance measurements. It represents the effective charge-separation distance in the barrier-region at zero bias. The Table 5.2 shows the characterized effective widths of the various device structures.

Figure 5.18 shows a plot of theoretical $C(v)$ from the Equation 2.18 in Chapter 2 and compares with measurements. The agreement is good in the qualitative sense since the $C(v)$ model is ideal. The ideal model ignores the charge that could have

Figure 5.16: Capacitance versus voltage plot of 62 μm diameter single barrier *InP* device.

Figure 5.17: Capacitance versus voltage plot of a 42 μm diameter stacked *InP* device.

Figure 5.18: Comparison of measured $C(v)$ with the simple model. Device type 1206 has dimensions $240 \times 240 \mu\text{m}^2$ and Device type 1411 $120 \times 120 \mu\text{m}^2$.

leaked into the intrinsic regions close to the barrier. This kind of discrepancy between the measured and modeled $C(v)$ was noted by [Nil94]. A measured effective width, w_{eff} is used in place of metallurgical width, w .

5.4 GaAs Varactors: Some Guidelines

The characterization of *GaAs* devices provides us with useful information. We find that the C_{max}/C_{min} ratio is ~ 4 for the *GaAs* devices and both the thick-barrier devices (1206) and thin-barrier devices (1411) have the same C_{max}/C_{min} ratio, while the thicker barriers block current better. Another advantage is that the thicker barrier results in lower specific capacitance and hence higher cutoff frequency. This can be explained by using the previously defined quality factor and comparing 1411 and 1206 devices.

Device	C(0)	Area (μm^2)	w_{eff}
1206	110 pF	57600	556 Å
1411	54 pF	14400	285 Å
459	4.0 pF	2789	741 Å

Table 5.2: Effective barrier widths from capacitance measurements.

Devices of area $(5 \times 5) \mu m^2$ are chosen. A series resistance of $R_S = 5.0 \Omega$ is assumed. A 1206 device yielded a dynamic cutoff frequency, $\mathcal{F}$ of 2.002 THz, while a 1411 device has an $\mathcal{F}$ of 1.206 THz. This dynamic cutoff frequency assumes that there is no leakage conductance G shunting the capacitance C . To have a more realistic comparison we use the dynamic quality factor $Q(v)$, derived from the measured $C(v)$, and $G(v)$ data derived from the $I(v)$ characteristics [KHL⁺94].

Figure 5.19 shows that device 1206, which has a thick barrier (274 Å) and the smaller barrier height (322 meV) has a larger Q than 1411, which has a thin barrier (142 Å) and the greater barrier height (372 meV). A device fabricated with a thick (~ 250 Å) $Al_{0.4}Ga_{0.6}As$, in the center of which is a thin $AlAs$ layer, would exhibit increased barrier height and enhanced Q simultaneously.

5.5 Large-Signal Tripler Simulations

In the previous sections we have proposed and demonstrated single-barrier varactors that have high effective barrier heights accompanied by low current densities and reduced $G(v)$ s. The problem of power output saturation of the early SBVs can be investigated with the aid of large signal tripler simulations. In this section the performance of the stacked varactor on InP is studied and compared with that of a single SBV. The SBV model resulting from the experimental characterization of the previous section is used as an input to the large signal analysis of Seigel and Kerr

Figure 5.19: A comparison of the dynamic quality factor $Q(v)$ of a thick-barrier ($274 \text{ \AA}$) type 1206 varactor with that of a thin-barrier ($142 \text{ \AA}$) type 1411.

[SKH84], which is used to predict the tripler performance.

5.5.1 Output Power Saturation in Leaky SBVs

The first experimental SBV tripler reported by the Chalmers team [RGK90] suffered from power output saturation at low input power levels. A recent 192 GHz tripler experiment by the JPL team [CFB93] also shows efficiency degradation above a certain input power level.

Power output saturation can occur in frequency multipliers when frequencies and power levels are high, if the RF current through the varactor device exceeds the velocity limited saturation current I_{sat} [KTFE92]. But the output power saturation reported in the two papers occurs at lower input power levels than the input power levels for which the diode current reaches I_{sat} due to velocity saturation. It will be

established in this thesis that this saturation phenomenon is due to resistive multiplication becoming the dominant nonlinear harmonic generating process in the device.

For the investigation of the output power saturation phenomenon a scaled type-1206 device of area $(5 \times 5) \mu m^2$ and $R_S = 5 \Omega$ was used in the simulation of a tripler from 64 GHz to 192 GHz. The simulated efficiency is plotted as a function of absorbed power in Figure 5.20. The low leakage current of the 1206 device results in nearly purely-reactive multiplication. This can be seen from the fact that the corresponding curve coincides with the simulated result for the case of zero leakage current. The output power saturation curve of Figure 5.21 was simulated for a leakage current artificially set to 100 times the measured current. This curve is in qualitative agreement with simulations performed for an SBV of the type reported in [RGK90], with the same area $(5 \times 5) \mu m^2$ and the same R_S (5Ω), as shown in Figure 5.21. These results demonstrate that the low-leakage (almost purely reactive) SBV is twice as efficient as the leaky SBV, when the dynamic device voltages v_{dmax} are driven to 4.6 V in each case.

The simulations shown in Figure 5.22 compare the power-transfer characteristics of a tripler from 64 GHz to 192 GHz, using the leaky varactor, with the results obtained when the measured $I(v)$ is used. Characteristics are shown for two different values of R_S . It is seen that the power saturation occurs for the leaky device in both values of R_S , but not for the measured device.

Figure 5.23 shows that when the measured $I(v)$ and $C(v)$ characteristics are used in the simulation, the waveforms are those of an almost purely reactive device, since the total device current i_d equals the displacement current i_{Cj} . Figure 5.24, on the other hand, depicts the corresponding waveforms when the leakage current is artificially set to 100 times the measured value. In this case significant conduction current i_{Gj} is flowing in phase with the applied voltage, leading to degraded multiplier efficiency. To achieve the same capacitance modulation (i.e. swing of v_d as in the low-loss case), considerably more absorbed input power is needed.

It is noted that the peak RF current of 40 mA is much smaller than the value

Figure 5.20: Simulated efficiency versus absorbed power for an SBV tripler from 64 GHz to 192 GHz, based on the use of a scaled 1206 device. The device area is $(5 \times 5) \mu m^2$ and $R_S = 5 \Omega$. (-o-): using measured data for SBV 1206. (..♦...): assuming zero leakage current. (-●-): assuming leakage current is $100 \times$ the measured value.

Figure 5.21: Simulated output power versus absorbed power for an SBV tripler from 64 GHz to 192 GHz, based on the use of a scaled 1206 device. The device area is $(5 \times 5) \mu m^2$ and $R_S = 5 \Omega$. (-o-): using measured data for SBV 1206. (..♦..): assuming zero leakage current. (-•-): assuming leakage current is 100× the measured value.

Figure 5.22: Simulated output power versus absorbed power for a tripler from 64 GHz to 192 GHz, using a scaled 1206 device of area $(5 \times 5) \mu m^2$, showing the effect of increasing R_S from 5Ω to 10Ω . The 10Ω value is typical of a small device. $R_S = 5\Omega$ ($- \circ -$): using measured data for SBV 1206 ($- \bullet -$), assuming the leakage current is $100\times$ the measured value. $R_S = 10\Omega$ ($\dots \square \dots$): using measured data for SBV 1206. ($\dots \blacksquare \dots$), assuming the leakage current is $100\times$ the measured value.

Figure 5.23: Simulated voltage and current waveforms of a frequency tripler from 64 GHz to 192 GHz, assuming a 1206 type device. The circuit conditions are: Absorbed power $P_{abs} = 5.12$ mW, output power $P_{out} = 2.56$ mW, maximum SBV voltage $v_{dmax} = 4.58$ V.

Figure 5.24: Simulated voltage and current waveforms of a leaky-barrier frequency tripler from 64 GHz to 192 GHz, assuming a 1206-type device, but with the leakage current artificially increased to 100 times the measured value. The circuit conditions are: Absorbed power $P_{abs} = 9.29$ mW, output power $P_{out} = 1.85$ mW, maximum SBV voltage $v_{dmax} = 4.58$ V.

of 96 mA which is calculated assuming a saturated carrier velocity of 2.4×10^5 m/s in *GaAs*. This establishes that the output power saturation observed in earlier SBV tripler is due to a leaky barrier and it occurs at lower power levels than needed to cause velocity limited current saturation in varactor devices. From the above simulations I conclude that the structures investigated in this thesis and the recommendations based on barrier height and capacitance measurements will lead to enhanced tripler performance at millimeter-wave frequencies.

5.6 Single and Stacked-Varactor Triplers on *InP*

Ultra-low current densities of SBVs on *InP* substrates have been demonstrated in this thesis. A symmetric stacked varactor on an *InP* substrate was demonstrated for the first time [KHR⁺94]. The simulations presented here outline the advantages of stacked varactor triplers and compare the single versus stacked approach. Previous tripler simulations and experiments, using leaky varactors fabricated on *InP* [TRB⁺94], showed output saturation at low input powers as explained in the previous section i.e. decrease in efficiency with increase of input swing v_{dmax} less than the breakdown voltage ($v_{dmax} < V_{br}$). Figures 5.25 and 5.26 show tripler simulations (13-39 GHz) using measured $C(v)$ and $I(v)$. Both the single and stacked devices do show increasing efficiency with input power to breakdown voltage. The peak efficiency occurs when the peak v_{dmax} of the voltage waveform across the device $v_d(t)$ equals the device breakdown voltage V_{br} .

The tripler waveforms of Figure 5.27 device reveals that the total-device current waveform $i_d(t)$ is indistinguishable from the displacement-current waveform $i_{Cj}(t)$ since the conduction current i_{Gj} is negligible.

The advantage of a stacked varactor device over a single-barrier varactor is best explained by an example. Figure 5.28 shows a plot of output power and efficiency as a function of input power for a single and a stacked varactor tripler. Both the single and stacked varactors are scaled to have a zero bias $C(0)$ of 40 fF. The area of the stacked

Figure 5.25: Simulation results of efficiency versus absorbed power for single barrier *InP* varactor frequency tripler from 13 to 39 GHz. The device has a $C(0)$ of 0.6 pF. Tripler simulations were terminated when v_{dmax} reached V_{br} .

A (μm^2)	η %	R_S Ω	$C(0)$ (pF)	f_{out} (GHz)	P_{out} (mW)	v_{dmax} (V)	i_{dmax} (mA)
1257	49.14	1	0.600	39	52.00	14.1	359
314	50.8	2	0.150	90	39.67	14.5	239
88	46.43	4	0.042	186	19.95	13.6	136

Table 5.3: Simulated performance of stacked varactor triplers.

Figure 5.26: Simulation results of efficiency versus absorbed power for a stacked *InP* varactor device tripler from 13 to 39 GHz. The device has a $C(0)$ of 0.6 pF. Tripler simulations were terminated when v_{dmax} reached V_{br} .

Figure 5.27: Simulated voltage and current waveforms of a triple stacked device in a frequency tripler from 13-39 GHz. The total device current i_d is indistinguishable from the displacement current i_{Cj} because the leakage current is very low.

Figure 5.28: Simulated efficiency and output power of frequency triplers from 62 to 186 GHz, as functions of absorbed input power. Single barrier and stacked devices have a zero-bias capacitance $C(0)=40.0$ fF.

varactor is $87.96 \mu\text{m}^2$ and that of the single barrier device is $30.68 \mu\text{m}^2$. The series resistances of the devices, taking into account the contact and epitaxial resistances, are 4Ω and 10Ω respectively. The 62-to-186 GHz tripler is analyzed using the scaled values of the measured $C(v)$ and $I(v)$ data. The Figure 5.28 indicates a maximum possible efficiency of 33 % for a single-barrier varactor tripler with an output power of 3.67 mW. Using the stacked varactor, the efficiency at low power levels is similar to that of the single-barrier varactor, because of its lower series resistance. However, at higher input power levels greater efficiencies can be obtained, with a maximum possible efficiency of 46.4 % at an output power of 19.95 mW. Table 5.3 summarizes the results of the simulations of triple stacked varactors of different areas.

Another parameter of interest is the maximum power that can be achieved by using the stacked varactor in a frequency tripler. These predictions must be calculated under realistic assumptions. The input power used in the simulation has to be lower than the power level at which the device dynamic voltage reaches V_{br} . The RF device current at this power level should be less than the velocity-limited current I_{sat} . We calculate the saturation current density, $J_{sat} = q_e N_d v_{max}$ to be $2.64 \times 10^9 \text{ A/m}^2$. A maximum electron velocity of $3.3 \times 10^7 \text{ cm/sec}$ in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is assumed. It can be seen from Table 4.3 that the maximum RF diode current i_{dmax} at a drive level corresponding to $v_{dmax} = V_{br}$ is less than I_{sat} , indicating that the power output predictions are not accompanied by current saturation. For example, a stacked device with area $1257 \mu\text{m}^2$ in Table 5.3 has a maximum device current 359 mA corresponding to the fully pumped condition. The i_{sat} is 3.3 A and is larger than i_{dmax} . This characteristic of stacked-barrier varactors will have important implications in the generation of power above 200 GHz where *GaAs* Schottky varactors have shown output power saturation due to velocity saturation [Eri90].

5.7 Ka Band Planar Tripler Experiment

The mechanical and electronic design of a planar tripler is reported in Chapter 3. This design is believed to be the first planar implementation of a stacked SBV device in a millimeter-wave tripler circuit. Figure 5.29 indicates the tripler circuit on a 5 mil alumina substrate. This section deals with the experiment and results obtained in the design. Two planar triplers with the stacked varactors were assembled to be tested. The first device behaved as a short circuit and the experiment was performed using the second circuit. Details of the experimental set up are shown in Figure 5.30.

Figure 5.29: Photomicrograph of the Ka band planar tripler. The bias circuit is designed to monitor the self-bias dc current. No appreciable amount of dc current is detected.

The input is derived from a HP 8350B sweep oscillator. A solid state power amplifier HP8344 is used to derive a power output up to a maximum of ~ 24 dBm. A harmonic reject filter is used to reject the second and third harmonic that can be

Figure 5.30: Experimental set up to measure tripler performance.

generated by the saturated power amplifier. The actual power at the tripler input differs from the power output indicated by the amplifier. This can be monitored or measured by using a HP8485A power detector and HP438A power meter. The cabling and filter loss also contribute to lower power entering the tripler.

The tripler is mounted in the jaws of a Universal test jig Wiltron 3680 K. The output is extracted via a K-connector cable followed by a coaxial to WR-28 adaptor, coupler and HP8486A power detector. An isolator is used to counter the effects of non-ideal load of the power detector. The WR-28 waveguide has a passband from 26-40 GHz.

5.7.1 Experimental Results

The input to the tripler is fixed at either 18 dBm or 22 dBm. With the 22 dBm input the tripler is found to saturate. The P_{in} of 22 dBm also represents the maximum

Figure 5.31: Frequency response of the tripler shown at $P_{in} = 18$ dBm and $P_{in} = 22$ dBm.

power delivered by the power amplifier at 13.00 GHz. Although the input power varied during the frequency sweep in the range 13.0-14.0 GHz the input power from the sweep generator is adjusted to deliver a constant power input to the tripler. Figure 5.31 shows the power output in the frequency range 13.0-14.0 GHz. The narrow band performance of the tripler is due to the low impedances (due to the high zero bias capacitance of 0.6 pF) that have to be matched to 50Ω . Figure 5.32 indicates the P_{in} versus P_{out} characteristics of the tripler at the center frequency, 13.45 GHz. A minimum conversion loss of 11.22 dB with a maximum power output of 10.78 dBm is obtained at 40.35 GHz.

5.7.2 Discussion

This experiment is the first planar tripler experiment using stacked SBVs. The experimental tripler is found to work very well with its own limitations. The output

Figure 5.32: P_{in} versus P_{out} of the tripler at the center frequency 13.45 GHz.

line of the coupled line bandpass filter ended up being a low impedance line as the mask was designed in error. This was remedied by cutting the tile at the output of the last coupled line section and attaching a $50\ \Omega$ line. The line was connected by wire bonds to the filter. The unavoidable gap between the output line and the last filter section would have resulted in a loss that could not be ascertained. The output of 10.78 dBm is less than the theoretical prediction of 17 dBm but sufficient to drive a double balanced mixer. The P_{out} is limited by the availability of source power. A waveguide experimental tripler which was tested at Philips Microwave, Hazelgrove, UK, yielded a maximum power output of 20 dBm with 7 dB conversion loss using the same device. Maximum efficiency of the tripler circuit was obtained at the device breakdown, thus indicating a purely reactive tripling [Rog93]. The second harmonic was found to be rejected by the device/circuit combination, with a value of -38 dBc with respect to the third harmonic. The input signal power leakage at the output is

-16 dBm for a P_{in} of 18 dBm. This planar tripler performance is comparable with that of an idler-based Ka band varactor tripler reported earlier [Hin87].

Chapter 6

Summary of Contributions and Recommendations

The thesis is centered around a novel device for idler-free, bias-free frequency tripling. The thesis is concluded by summarizing its contributions to improving the devices and also indicating the directions for future work. The publications resulting from this thesis are also indicated in this section.

6.1 Summary

The problem of leakage currents in the early single barrier varactors has been solved in the thesis. The origin of the leakage currents have been identified. Alternative structures have been grown and high- Q , low-leakage varactors demonstrated on *GaAs* [KH92][KHL⁺92]. The low-leakage characteristics of these varactors have been quantified by barrier height measurements. The early single barrier varactors had an effective barrier height of 180 meV. The best varactors reported in this thesis have a barrier height of 372 meV, a twofold increase in the barrier height [KHL⁺94] [KNH94].

Accurate capacitance measurements using a special mount indicates a C_{max}/C_{min} ratio of 4 for diodes with $In_{0.2}Ga_{0.8}As$ spacers. This thesis is the first to report a

simultaneous low-leakage and good capacitance modulation in a *GaAs* SBV using pseudomorphic *InGaAs* spacers.

Further large-signal tripler simulations using *GaAs* varactor indicate a two-fold improvement in tripler efficiency due to reduced-leakage currents and absence of the output saturation at low input power levels reported by other authors [KHL⁺94].

A simple cubic charge model is proposed in this thesis to model the SBV nonlinearity. This model is used in a straightforward circuit analysis to obtain closed-form results for frequency tripler impedances and efficiencies [KH93]. This simple analysis is compared with a computer-based harmonic balance of Seigel and Kerr [SKH84] and good agreement is observed.

A triple-stacked varactor with a 1.4 THz cut-off frequency is demonstrated. Very accurate modeling by microwave characterization is demonstrated and large-signal harmonic balance simulations indicate good power output capability without velocity-limited saturation effects[KHR⁺94]. Simulation of a 200 GHz stacked device indicates a possibility of 20 mW output when pumped by a solid-state source. This figure is a factor of 5 more than highest power output obtained from a Schottky tripler [Räi92].

A planar tripler is demonstrated on 5 mil alumina. It is shown to be free of resistive tripling effects that plagued earlier varactors. The output of the tripler is 40.35 GHz which falls close to the PCN radio band. This tripler driven by a FET DRO and amplifier is a potential low phase noise source for PCN radio[KBH95]. The contribution of the thesis is summarized in Figure 6.1 and 6.2.

6.2 Recommendations

Most of the basic device-circuit interactions have been studied in this work and shortcomings of previous investigations have been solved. Due to lack of resources and time, some development work has not been undertaken. The work has been kept to a tractable limit in terms of device sizes and the highest frequency of RF characterization.

Figure 6.1: Flow chart depicting the problem of early *GaAs* SBVs and the thesis contribution towards solving the problem.

Future work with these devices can be directed towards developing smaller planar devices on *GaAs* and *InP*. The design of wafer layers can be the same as for the devices with the desirable characteristics realized in this thesis.

RF characterization can be extended by using coplanar probe techniques up to 50 GHz. This work will be undertaken by Mr. Ali Rahal of Ecole Polytechnique, Montreal.

Practical tripler circuit design and optimisation is an area by itself. To successfully realize the predictions in the thesis, planar and waveguide tripler design at Ka and W bands have to be undertaken.

Another interesting possibility with these devices is broadbanding the tripler cir-

Figure 6.2: Flow chart depicting the limitations of basic SBVs and the thesis contribution towards improving the state of the art in symmetric $C(v)$ device by stacked approach.

cuit with distributed techniques [CCK+92]. The high efficiency of the reactive approach combined with the broadband technique will make the tripler a cost effective millimeter-wave source. These devices have demonstrated not only the possibility of simpler tripler design but also good potential for the use of symmetric heterostructure barrier varactors in future millimeter-wave sources.

Bibliography

- [ACK⁺87] T.G. Andersson, Z.G. Chen, V.D. Kulakovskii, A. Uddin, and J.T. Vallin. Variation of the critical layer thickness with In content in strained $In_xGa_{1-x}As - GaAs$ quantum wells grown by molecular beam epitaxy. *Appl. Phys. Lett.*, 51:752-754, September 1987.
- [Ave64] W.R. Avellino. Efficient odd harmonic generation with opposingly biased varactor diodes. *Proceedings IEE*, pages 868-869, 1964.
- [Bla82] J.S. Blakemore. Approximations for the Fermi-Dirac Integrals, especially the function $\mathcal{F}_{1/2}(\eta)$ used to describe electron density in a semiconductor. *Solid State Electronics*, 10:1067-1076, 1982.
- [Boc88] E. Boch. Design of a rugged millimeter-wave doubler using a series varactor configuration. *Proc. Intl. Infrared and Millimeter Wave Symposium*, pages 785-787, 1988.
- [Boc89] E. Boch. A planar wideband mm-wave frequency doubler. *Microwave Journal*, pages 123-125, December 1989.
- [Bur65] C.B. Burckhardt. Analysis of varactor frequency multipliers for arbitrary capacitance variation and drive level. *Bell System Technical Journal*, pages 675-690, 1965.

- [BW86] J. Batey and S.L. Wright. Energy band alignment in $GaAs : (Al, Ga)As$ heterojunctions: The dependence on alloy composition. *J. Appl. Phys.*, 59:201-209, January 1986.
- [CCC+86] A. Chu, W.E. Courtney, C.L. Chen, L.J. Mahoney, M.J. Manfra, and H.A. Atwater. Monolithic analog phase-shifters and frequency multipliers for mm-wave phased array applications. *Microwave Journal*, pages 105-119, December 1986.
- [CCK+92] E. Carman, M. Case, M. Kamegawa, R. Yu, K. Giboney, and M.J.W. Rodwell. V-band and W-band broad-band, monolithic distributed frequency multipliers. *IEEE Microwave and Guided Wave Letters*, pages 253-254, 1992.
- [CFB93] D. Choudhury, M.A. Frerking, and P.D. Batelaan. A 200 GHz tripler using a single barrier varactor. *IEEE Trans. Microwave Theory and Tech*, 41:595-599, April 1993.
- [CM87] F. Capasso and G. Margaritondo. *Heterojunction Band Discontinuities, Physics and Device Applications*. North-Holland, New York, 1987.
- [CMM+93] R.E. Carnahan, M.A. Maldonado, K.P. Martin, A. Nogaret, R.J. Higgins, L.A. Cury, D.K. Maude, J.C. Portal, J.F. Chen, and A.Y. Cho. $\Gamma - \lambda$ intervalley tunneling in InAs/AlSb resonant tunneling diodes. *Appl. Phys. Lett.*, 62, March 1993.
- [Dic67] L.E. Dickens. Spreading resistance as a function of frequency. *IEEE Trans. Microwave Theory and Tech.*, 15:101-109, February 1967.
- [DLBH+89] G. Duggan, D.E. Lacklison, S.J. Battersby, J.J. Harris, C.T. Foxon, D. Hilton, C. Roberts, J. Hewett, and C.M. Hellon. Effect of undoped $GaAs$ spacers on the characteristics of $GaAs - (Al, Ga)As - GaAs$ single barrier structures. *J. Appl. Phys.*, 65:1183-1187, February 1989.

- [Eri90] N.R. Erickson. High efficiency submillimeter frequency multipliers. *Proc. IEEE MTT-S International Microwave Symposium*, pages 1301-1304, 1990.
- [Eri93] N.R. Erickson. A high power doubler for 174 ghz using a planar doubler diode array. *Proceedings of International Symposium on Space Terahertz Technology*, pages 287-296, 1993.
- [FE92] M.A. Frerking and J.R. East. Novel heterojunction varactors. *Proceedings of the IEEE*, 80:1853-1860, November 1992.
- [Fik64] J. Fikart. Efficient odd harmonic generation with opposingly biased varactor diodes. *Electronics Letters*, 4:544-546, 1964.
- [Get66] W.J. Getsinger. The packaged and mounted diode as a microwave circuit. *IEEE Trans. Microwave Theory and Tech.*, 14:58-69, 1966.
- [HCS80] M. Hatzakis, B.J. Canavello, and J.M. Shaw. Single-step lift-off process. *IBM J. Res. Development*, 24:452-468, July 1980.
- [Hin87] D.J.M. Hindson. A microstrip tripler to 47 GHz. In *Proc. Intl. Infrared and Millimeter Wave Symposium*, pages 43-44, June 1987.
- [Hu86] C.P. Hu. Millimeter-wave frequency multipliers employ semiconductor diodes in a balanced configuration. *Microwave Journal*, pages 109-112, December 1986.
- [Ihm87] J. Ihm. Effects of the layer thickness on the electronic character in *GaAs/AlAs* superlattices. *Appl. Phys. Lett.*, 50:1068-1070, April 1987.
- [IMN⁺87] T. Inata, S. Muto, Y. Nakata, S. Sasa, T. Fujii, and S. Hiyamizu. A pseudomorphic $In_{0.53}Ga_{0.47}As/AlAs$ resonant tunneling barrier with a peak-to-valley current ratio of 14 at room temperature. *Japanese Journal of Applied Physics*, 26:L1332-L1334, August 1987.

- [KBH95] Kathiravan Krishnamurthi, E. Boch, and R. G. Harrison. A Ka-band planar tripler based on a stacked symmetric *InP* heterostructure-barrier varactor. *Proc. IEEE MTT-S International Microwave Symposium*, May 1995.
- [Ker75] A.R. Kerr. A technique for determining the local oscillator waveforms in a microwave mixer. *IEEE Trans. Microwave Theory and Tech.*, 23:828, 1975.
- [KH92] Kathiravan Krishnamurthi and R. G. Harrison. Comments on millimeter- and submillimeter-wave multipliers using quantum-barrier-varactor (QBV) diodes. *IEEE Electron Device Letters*, 13:131, February 1992.
- [KH93] Kathiravan Krishnamurthi and R. G. Harrison. Analysis of symmetric-varactor frequency triplers. *Proc. IEEE MTT-S International Microwave Symposium*, pages 649-652, 1993.
- [KHL⁺92] Kathiravan Krishnamurthi, R. G. Harrison, H.C. Liu, A.J. SpringThorpe, and M. Buchanan. High Q Quantum-Barrier-Varactor (QBV) diodes for millimeter wave multipliers. *Proc. Intl. Infrared and Millimeter Wave Symposium*, pages 74-75, December 1992.
- [KHL⁺94] Kathiravan Krishnamurthi, R. G. Harrison, H.C. Liu, M. Buchanan, Z.R. Wasilewski, and J.R. Thompson. Chair-barrier varactors on *GaAs* for frequency triplers. *Proc. IEEE MTT-S International Microwave Symposium*, pages 313-316, May 1994.
- [KHR⁺94] Kathiravan Krishnamurthi, R. G. Harrison, C. Rogers, J. Ovey, S. M. Nilsen, and M. Missous. Stacked heterostructure barrier varactors on *InP* for millimeter wave triplers. *Proceedings European Microwave Conference*, pages 758-763, September 1994.

- [KKN⁺89] C.S. Kyono, V.P. Kesan, D.P. Neikirk, C.M. Maziar, and B.G. Streetman. Dependence of apparent barrier height on barrier thickness for perpendicular transport in *AlAs/GaAs* single-barrier structures grown by molecular beam epitaxy. *Appl. Phys. Lett.*, 54:549–551, February 1989.
- [KNH94] Kathiravan Krishnamurthi, S. M. Nilsen, and R. G. Harrison. Single barrier varactors on *GaAs*: Guidelines for enhanced performance. *IEEE Trans. Microwave Theory and Tech.*, 42, December 1994.
- [KR89] E. Kollberg and A. Rydberg. Quantum-barrier-varactor diodes for high efficiency millimeter-wave multipliers. *Electronic Letters*, 25:1696–1697, 1989.
- [KTFE92] E.L. Kollberg, T.J. Tolmunen, M.A. Frerking, and J.R. East. Current saturation in submillimeter wave varactors. *IEEE Trans. Microwave Theory and Tech.*, 40:831–838, May 1992.
- [LHM87] U. Lieneweg, B. Hancock, and J. Maserjian. Barrier-Intrinsic-N diodes for near millimeter-wave generation. *Proc. Intl. Infrared and Millimeter Wave Symposium*, pages 6–7, 1987.
- [Liu87] H.C. Liu. Resonant tunneling through single layer heterostructures. *Appl. Phys. Lett.*, 51:1019–1021, September 1987.
- [LLBS89] D. Landheer, H.C. Liu, M. Buchanan, and R. Stoner. Tunneling through *AlAs* barriers: $\Gamma - X$ transfer current. *Appl. Phys. Lett.*, 54:1784–1786, May 1989.
- [LSD⁺93] H.X. Liu, L.B. Sjögren, C.W. Domier, N.C. Luhmann, D.L. Sivco, and A.Y. Cho. Monolithic quasi-optical frequency tripler array with 5 W output power at 99 GHz. *IEEE Electron Device Letters*, pages 329–331, July 1993.

- [Maa86] S.A. Maas. *Microwave Mixers*. Artech House, Norwood, Mass, 1986.
- [Maa88] S.A. Maas. *Nonlinear Microwave Circuits*. Artech House, Norwood, Mass, 1988.
- [Mar91] S.L. March. Simple equations characterize bond wires. *Microwaves and RF*, pages 105–110, November 1991.
- [MCW86] E.E. Mendez, E. Calleja, and W.I. Wang. Tunneling through indirect-gap semiconductor barriers. *Physical Review B*, 34:6026–6029, October 1986.
- [MH90] I. Mehdi and G. Haddad. Lattice matched and pseudomorphic $In_{0.53}Ga_{0.47}As/In_xAl_{1-x}As$ resonant tunneling diodes with high current peak-to-valley ratio for millimeter-wave power generation. *J. Appl. Phys.*, 67:2643–2646, March 1990.
- [Nil94] S.M. Nilsen. *Design and fabrication of III-V semiconductor devices for millimeter-and submillimeter wave applications*. PhD thesis, Chalmers's University of Technology, Göteborg, Sweden, 1994.
- [OC70] R.P. Owens and D. Cawsey. Microwave equivalent-circuit parameters of gunn-effect packages. *IEEE Trans. Microwave Theory and Tech.*, 18:790–798, 1970.
- [Pag58] C.H. Page. Harmonic generation with ideal rectifiers. *Proceedings IRE*, 46:1738–1740, October 1958.
- [Pan58] R.H. Pantell. General power relationship for positive and negative nonlinear resistive elements. *Proceedings IRE*, 46:1910–1913, December 1958.
- [PC90] W.C.B. Peatman and T.W. Crowe. A high electron mobility varactor diode. *Proc. Intl. Infrared and Millimeter Wave Symposium*, pages 473–475, 1990.

- [Pet90] D.F. Peterson. The varactor power frequency multiplier. *Microwave Journal*, pages 135–146, May 1990.
- [Pie87] R.F. Pierret. *Advanced Semiconductor Fundamentals*. Addison Wesley, 1987.
- [Poz90] D.M. Pozar. *Microwave Engineering*. Addison-Wesley Publishing Company, Reading, Massachusetts, 1990.
- [PR62] P. Penfield and R. Rafuse. *Varactor Applications*. MIT Press, Cambridge, Mass, 1962.
- [PWAC83] R. People, K.W. Wecht, K. Alavi, and A.Y. Cho. Measurement of conduction band discontinuity of molecular beam epitaxially grown $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ N-n heterojunction by CV profiling. *Appl. Phys. Lett.*, 43:118–120, July 1983.
- [Räi92] A.V. Räisänen. Frequency multipliers for millimeter and submillimeter wavelengths. *Proceedings of the IEEE*, 80:1842–1852, 1992.
- [RGK90] A. Rydberg, H. Grönqvist, and E. Kollberg. Millimeter- and submillimeter-wave multipliers using quantum barrier varactor diodes (QBV). *IEEE Electron Device Letters*, 11:373–375, September 1990.
- [RLK91] M. Rossmanith, J. Leo, and K. Von Klitzing. Model of $\Gamma-X$ transition in thermally activated tunneling current across $Al_xGa_{1-x}As$ single barriers. *J. Appl. Phys.*, 69:3641–3645, March 1991.
- [RN93] V.K. Reddy and D.P. Neikirk. High breakdown voltage AlAs/InGaAs quantum barrier varactor diodes. *Electronics Letters*, 29, March 1993.
- [Rog93] C. Rogers. Stacked quantum barrier high power multiplier varactors. Technical Report RP6-127, Philips Microwave, Hazelgrove, UK, 1993.

- [RSC+92] C. Raman, J.P. Sun, W.L. Chen, G. Mains, J. East, and G. Haddad. Superlattice barrier varactors. *Third International Symposium on Space Terahertz Technology*, pages 146–157, 1992.
- [SA91] M.M. Sayed and G.F. Anderson. 50-110 GHz high-performance millimeter-wave source modules. *Hewlett-Packard Journal*, pages 50–64, April 1991.
- [SCST93] C.V. Sammut, N.J. Cronin, R.D. Schnell, and H. Tews. Accurate small-signal modeling of a double barrier resonant tunneling diode. *Proc. IEEE MTT-S International Microwave Symposium*, pages 1041–1044, 1993.
- [SHOC87] P.W. Staecker, M.E. Hines, F. Occhiuti, and J.F. Cushman. Multi-watt power generation at millimeter-wave frequencies using epitaxially-stacked varactor diodes. *Proc. IEEE MTT-S International Microwave Symposium*, pages 917–920, 1987.
- [SKH84] H. Seigel, A.R. Kerr, and W. Hwang. Topics in the optimization of millimeter-wave mixers. NASA Tech. Paper 2287, 1984.
- [Ste67] D.H. Steinbrecher. An interesting impedance matching network. *IEEE Trans. Microwave Theory and Tech.*, page 382, 1967.
- [Swa92] V. Swaminathan. *Indium Phosphide and Related Materials: Processing, Technology and Devices*, chapter Properties of *InP* and related materials. Artech House, 1992.
- [Sze91] S.M. Sze. *High speed semiconductor devices*. John Wiley and Sons, New York, 1991.
- [Tan66] C.H. Tang. An exact analysis of varactor frequency multipliers. *IEEE Trans. Microwave Theory and Tech.*, pages 210–212, 1966.

- [TNB⁺91] T. Tolmunen, S. Nilsen, O. Boric, M. Frerking, and E. Kollberg. Accurate characterisation of varactors with fF capacitance. *Proc. Intl. Infrared and Millimeter Wave Symposium (IRMMW)*, pages 214–215, 1991.
- [TRB⁺94] T.J. Tolmunen, A.V. Räisanen, E. Brown, H. Grönqvist, and S.M. Nilsen. Experiments with single barrier varactor tripler and quintupler at millimeter wavelengths. *Proceedings of Space Terahertz Technology Conference*, 1994.
- [Uhl58] A. Uhlir. The potential of semiconductor diodes in high frequency communications. *Proceedings of the IRE*, 46:1099–1115, June 1958.
- [UM88] H. Unlu and H. Morkoc. Strained layer InGaAs/AlGaAs quantum wells for ultra high frequency modfets. *Solid state technology*, pages 83–87, March 1988.
- [VW87] D. Vakhshoori and S. Wang. Resonant tunneling diodes with AlAs barrier: Guides for improving room-temperature operation. *J. Appl. Phys.*, 62:3474–3476, October 1987.

Appendix A

SIMS Measurement on *GaAs* Wafers

SIMS measurement is used to chart out the *Si* dopant profile throughout the single barrier varactor device. It also yields the profile of *Al*, *In* and *Ga* in the structure. Layers of the order of 100 Å or less cannot be resolved in SIMS profiles. This is seen in a rather high *Si* concentration displayed in the SIMS plot in barrier region but the *Si* concentration on the substrate is close to the nominal value. However the presence of *Al* in the barrier regions shows up as spikes in *Al* SIMS profile and a dip in the *Ga* SIMS profile. The spike in *In* occurs at the spacer region as expected.

The plots in Figure (A.1) and (A.2) show *Si* dopant distribution in relation to the barrier position. The top electrode doping for 1206 device is lower than the design value of $4 \times 10^{18} \text{ cm}^{-3}$ while for the 1411 device the measured *Si* concentration is close to the design value. The *Al* spikes on the SI substrate in 1411 indicates the Multiple Quantum Well (MQW) used to calibrate the growth rate by X-ray measurement.

An asymmetry in the *Si* profile as well as nonuniformity and nonabrupt *Si* doping concentration in the the depletion layers is due to effects nonideal dopant switching during growth. This asymmetry is noted in the $I(v)$ measurements as well as in the $C(v)$ measurements.

Figure A.1: SIMS profile for the SBV device 1206.

Figure A.2: SIMS profile for the SBV device 1411.

Appendix B

Series Resistance of Upright Devices

The series resistance of the varactor is an important parameter in determining the varactor performance. It depends on the geometry of the device, contacts, epitaxial layers doping and substrate. A simple model of the series resistance will be applied to calculate the frequency dependent series resistance of the device. The results of calculations using this model agree with the measured data.

The series resistance is the sum of four components: $R_S = R_c + R_{cs} + R_{spread} + R_{und}$, where

1. R_c is the finite ohmic resistance of the contacts,
2. R_{cs} is the bulk resistance of the contact layer,
3. R_{spread} is the spreading resistance of the substrate,
4. R_{und} is the resistance of the undepleted epitaxial layer.

The contact resistance is an important part of the total series resistance. Contact resistance is usually specified by specific contact resistivity, ρ_c , where

$$R_c = \frac{\rho_c}{\text{Area}}. \quad (\text{B.1})$$

The bulk resistance R_{cs} of the contact layer depends on the thickness, contact region bulk resistivity and the area of the device.

$$R_{cs} = \frac{\rho_{cs} t_{cs}}{\text{Area}}. \quad (\text{B.2})$$

The undepleted portion of the active region in the varactor contributes to the series resistance, R_{und} .

$$R_{und} = \frac{\rho_{und} t_{und}}{\text{Area}}. \quad (\text{B.3})$$

This series resistance can be made smaller by increasing the doping. Lower N_d results in higher value of this resistance and also improves the breakdown capability of the devices. A high value of N_d would decrease the the series resistance and breakdown voltage. In the SBV device the current is a strong function of the Fermi-level of the electrons in front of the barrier and higher doping would raise the Fermi level in front of the barrier, increasing the device current. The capacitance variation would also be reduced by higher doping levels.

The spreading resistance of the substrate is calculated assuming an outward flow of current from the circular anode to the edge of the chip and then down the side walls thick to a skin depth $\delta_s = \sqrt{\rho_{sub}/\pi f \mu}$. This is illustrated in Figure B.1 that indicates the current flow in a narrow strip and the chip parameters t_c , b and d . Dickens [Dic67] finds the substrate spreading resistance to be

$$R_{spread} = R_{lateral} + R_{sides} \quad (\text{B.4})$$

$$= \frac{0.5 \rho_{sub} \ln(b/d)}{\pi \delta_s} + \frac{\rho_{sub} t_c}{\pi \delta_s b}. \quad (\text{B.5})$$

For calculation of R_S of InP devices a value of ρ_{sub} of $2.4 \times 10^6 \Omega\text{-cm}$ is used for gold. Resistivity values of $1 \times 10^{-3} \Omega\text{-cm}$ for the n^+ doped substrate, $1.5 \times 10^{-4} \Omega\text{-cm}$ for the contact region and $1.56 \times 10^{-2} \Omega\text{-cm}$ for the active region were used.

Figure B.1: Series resistance model.

Appendix C

Touchstone File-Passive Circuit Design for a 39 GHz Planar Tripler

This Appendix lists the circuit file used to design a 39 GHz planar tripler based on a stacked varactor device. The design technique is explained in Chapter 4 (section 4.4). The filters and matching circuits are optimized using TOUCHSTONE¹ software. The large-signal equivalent circuit of the pumped device is used at the input and output frequencies. The equivalent circuit is obtained using the cubic model or harmonic balance technique.

DIM

FREQ GHZ

RES OH

ind nh

CAP PF

TIME PS

VAR

! The variables for input matching are listed

! with suffix 'm' 'in'

¹TOUCHSTONE is Trade Mark of HP-EEsof, Lindero Canyon Rd., Westlake Village, CA 91362.

```
Wm1in=36.30307
Lm1in=78.85292
Wm2in=3.500253
Lm2in=23.49918
! length adjustment of a 50 ohm line for
!input isolation.
LADJin\25.92535
! Input low-pass filter parameters
WH=1.9
WL=26.46
LL1=13.00
LH1=47.10
LL2=15.00
LH2=86.5
LL3=10.20
LH3=34.99
! Output matching circuit parameters
! the suffixes are op
W1Mop=1.569
L1Mop=15.2
W2Mop=15.96
! L2Mop=7.1126
W3Mop=15.823
L3Mop=22.3
! Band-pass output filter variables
S1=1.0
S2=2.0
L2=28.035
WC2=3.59
```

```

S3=1.0
L3=28.95
L1=28.95
WC1=2.43
WC3=2.43
! length adjustment for output circuit
! isolation at the input frequency
LADJop=73.62059
! choke circuit parameters
Wch=1.2
ANGch=141.0
L1ch=96.17
L2ch=46.49

CKT
  MSUB_P3 ER=9.9 H=5 T=0.1968 RHO=1.0 RGH=0
! Low-pass filter circuit. Cut-off frequency
! of 14 GHz.
  MLIN 1 2 W=Wch L=L1ch
  MTEE 2 3 4 W1=Wch W2=Wch W3=Wch
  MRSTUB 4 W1=Wch L=L2ch ANG=ANGch
  MLIN 3 5 W=Wch L=40
  MLEF 5 W=40 L=70
  DEF1P 1 0 CHOKE

  MLIN 1 21 W=4.79 L=75
! choke 21

```



```

MSTEP 21 22 W1=4.79 W2^WL
MLIN 22 23 W^WL L^LL1
MSTEP 23 24 W1^WL W2^WH
MLIN 24 25 W^WH L^LH1
MSTEP 25 26 W1^WH W2^WL
MLIN 26 27 W^WL L^LL2
MSTEP 27 28 W1^WL W2^WH
MLIN 28 29 W^WH L^LH2
MSTEP 29 30 W1^WH W2^WL
MLIN 30 31 W^WL L^LL3
MSTEP 31 32 W1^WL W2^WH
MLIN 32 33 W^WH L^LH3
MSTEP 33 34 W1^WH W2=4.79
MLIN 34 35 W=4.79 L=100
DEF2P 1 35 LPFILTER
LPFILTER 1 2
MTEE 2 3 4 W1=4.79 W2=4.79 W3^Wch
MLIN 3 5 W=4.79 L^LADJin
CHOKE 4
DEF2P 1 5 LPFILT

```

! We then have the input matching circuit

```

MSUB_P1 ER=9.9 H=5 T=0.196 RHO=1.0 RGH=0
MLIN 1 2 W=4.79 L=1
MSTEP 2 3 W1=4.79 W2^Wm1in
MLIN 3 4 W^Wm1in L^Lm1in
MSTEP 4 5 W1^Wm1in W2^Wm2in
MLIN 5 6 W^Wm2in L^Lm2in
DEF2P 1 6 imatch
MSUB_P2 ER=1 H=1.5 T=0.314 RHO=1.0 RGH=0

```

```

MLIN 1 2 W=1.96 L=10.5
! IND 1 2 L=0.1
RES 2 3 R=1.8
CAP 3 0 C=0.33
deflp 1 0 indev
imatch 20 21
indev 21 0
deflp 20 0 inmatch
! Input filter plus matching circuit
!together.
lpfilt 1 2
inmatch 2 0
defip 1 0 ifilmth
lpfilt 1 2
imatch 2 3
res 1 0 r=50
defip 3 0 lpfm
! The output matching circuit
MSUB_P4 ER=9.9 H=5 T=0.196 RHO=1.0 RGH=0.0
MLIN 1 2 W=4.79 L=15
MSTEP 2 3 W1=4.79 W2~W1Mop
MLIN 3 4 W~W1Mop L~L1Mop
MSTEP 4 5 W1~W1Mop W2~W3Mop
! MLIN 5 6 W~W2Mop L~L2Mop
! MSTEP 6 7 W1~W2Mop W2~W3Mop
MLIN 5 8 W~W3Mop L~L3Mop
def2p 1 8 omatch
MSUB_P5 ER=1 H=1.5 T=0.315 RHO=1 RGH=0
RES 1 2 R=7.5

```

```

!   IND 11 12 L=0.15
      MLIN 2 3 W=1.96 L=10.5
      CAP 3 0 C=0.25
      deflp 1 0 opdev

! The output band-pass filter circuit is
! defined
      MSUB_P6 ER=9.9 H=5 T=0.196 RHO=1.0 RGH=0.0
      MLIN 1 2 W=4.79 L=LADJop
      MSTEP 2 3 W1=4.79 W2=WC1
      MCFIL_T40 3 4 W=WC1 S=S1 L=L1 W1=4.79 W2=WC2
      MSTEP 4 5 W1=WC1 W2=WC2
      MCFIL_T52 5 6 W=WC2 S=S2 L=L2 W1=WC1 W2=WC3
      MSTEP 6 7 W1=WC2 W2=WC3
      MCFIL_T57 7 8 W=WC3 S=S3 L=L3 W1=WC2 W2=4.79
      MSTEP_T2 8 9 W1=WC3 W2=4.79
      MLIN 9 10 W=4.79 L=15
      DEF2P 1 10 bpfilter
      omatch 20 21
      opdev 21 0
      deflp 20 0 opmatch
      bpfilter 90 91
      opmatch 90 0
      deflp 91 0 ofilmth
      bpfilter 100 101
      res 101 0 r=50
      omatch 100 102
      deflp 102 0 bpfm

! Input tripler circuit with output loading

```

```

lpfilt 1 2
imatch 2 3
  MSUB_P6 ER=1 H=1.5 T=0.314 RHO=1 RGH=0
! Bond tape is air microstrip line
  MLIN 3 4 W=1.96 L=10.5
  CAP 4 5 C=0.33
  RES 5 0 R=1.8
  MLIN 4 6 W=1.96 L=10.5
! substrate change for connecting the output loading
! output loading circuit at the device plane

  MSUB_P7 ER=9.9 H=5 T=0.196 RHO=1 RGH=0
  bpfm 6 0
  deflp 1 0 tripin
  MSUB_P8 ER=1.0 H=1.5 T=0.314 RHO=1 RGH=0
  MLIN 1 2 W=1.96 L=10.5
  MSUB_P9 ER=9.9 H=5 T=0.196 RHO=1 RGH=0
  bpfm 2 0
  deflp 1 0 inload
! Tripler output circuit with input loading
  bpfilter 1 2
  omatch 1 3
  MSUB_P8 ER=1 H=1.5 T=0.315 RHO=1 RGH=0
  MLIN 3 4 W=1.96 L=10.5
  CAP 4 5 C=0.25
  RES 5 0 R=7.5
  MLIN 4 6 W=1.96 L=10.5
  MSUB_P11 ER=9.9 H=5 T=0.196 RHO=1.0 RGH=0
  lpfm 6 0

```

```

deflp 2 0 tripop
MSUB_P8 ER=1 H=1.5 T=0.315 RHO=1.0 RGH=0
MLIN 1 2 W=1.96 L=10.5
MSUB_P12 ER=9.9 H=5 T=0.196 RHO=1.0 RGH=0.0
lpfm 2 0
deflp 1 0 opload
FREQ
SWEEP 38 40.0 1.0      !output sweep range
!SWEEP 12.6 13.3 0.1 !input sweep range
OUT
!inmatch db[s11]
!lpfm z11
!inmatch z11
lpfilt db[s21] gr1
!lpfilter db[s11] gr1
!bpfilter db[s21] gr1
!bpfm z11
!choke s11
!tripin db[s11]
!inload z11
!filmth db[s11]
!nmatch db[s11]
tripop db[s11]
ofilmth db[s11]
opload z11
UPT
freq 12.65 13.25 0.10
!bpfm re[z11]<2
!inmatch DB[s11] < -14.0

```

```
!inmatch DB[S11] >-16.0
tripin db[s11]<-14.0
!freq 38.0 40.0
tripop db[s11]<-20
opload re[z11]>100
grid
! freq 4 40 0.1
gri -12 0 0.1
```

Appendix D

Determination of S4 Package Parasitics

This Appendix explains the details of determination of the package parasitics of the S4 package used for characterization of *InP* devices. The package model and its physical origin are explained in Chapter 5.

Figure D.1: Dimensions of S4 package in cms.

It is possible to find an estimate of the package inductance L_p . From the geometry

of the package we can use transmission line theory to estimate the coaxial post-inductance. For the length l_c in cm [Poz90],

$$L_c = 138 \frac{l_c}{c} \log_{10} \left(\frac{d_4}{d_1} \right) \text{ H} \quad (\text{D.1})$$

where $d_4=7.0$ mm is the outer conductor diameter, $d_1 = 1.02$ mm is the post diameter, and $l_c = 1.52$ mm is the height of the ceramic. We have $L_c = 0.584$ nH. The inductance of the 0.2 cm diameter d_3 and 0.0178 cm thick flange supporting the ceramic is $L_f = 44.29$ pH, giving a total inductance L_p of 0.628 nH. Likewise the

Figure D.2: Equivalent circuit of open and short circuit packages.

inductance of a bondwire with diameter d and length l , can be estimated from [Mar91]

$$L = (\mu_0 l / 2\pi) \times [\ln(4l/d) + \mu_r \delta - 1] \quad (\text{D.2})$$

where δ is the skin effect factor given by $\delta = 0.25 \tanh(4d_s/d)$, d_s being the skin depth of the bond wire given by

$$d_s = (\rho / \pi f \mu_0 \mu_r) \quad (\text{D.3})$$

Figure D.3: A plot of fitted and measured admittance of a short circuit package as a function of frequency.

where ρ is the resistivity of the bond wire ($2.44 \times 10^{-8} \Omega\text{m}$ for gold), and f is the frequency in hertz. From the geometry of the package we estimate a bond wire $l=787 \mu\text{m}$ long. Using a bondwire $17.5 \mu\text{m}$ diameter, we have $2L_{\text{bond}} = 0.789 \text{ nH}$. (We use two bond wires in parallel for a V bond).

To determine the package parameters by experiment, two dummy packages were prepared. One is an open-circuited package, the other is a short-circuited package. The open-circuit package has a device mounted on the post and bond wires are bonded across the package flange and the middle left close to, but not touching, the mesa.

Figure D.4: A plot of fitted and measured admittance of an open circuit package as a function of frequency.

The parameters L_p , C_p and C_1 can be determined by measuring the open package. The values are $L_p = 0.63$ nH, $C_p = 0.082$ pF and $C_1 = 0.162$ pF. The measured package inductance is remarkably close to the estimated value of 0.628 nH.

The short-circuit package consists of bond wires bonded to the post. $L_{bond} = 0.405$ nH determined from short-circuit measurements is close to the estimated value of $L_{bond} = 0.3945$ nH and other element values calculated using the open circuit package agree with the values used to simulate the short circuit impedance. Figures D.4 and D.3 show plots of measured and fitted package impedances from measured S

parameters of the package. The close agreement of the fit and measured results and also the closeness of the estimated inductor values to measurement establishes the validity of the package model.

END

2 9-05-95

FIN