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**Design and Implementation of
Multi-GHz Energy-Efficient Asynchronous Pipelined
Circuits in MOS Current-Mode Logic**

by

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A thesis submitted to the Faculty of Graduate Studies and Research in
partial fulfillment of the requirements for the degree of

Master of Applied Science

Ottawa-Carleton Institute for Electrical Engineering

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Abstract

This report presents the design, the delay estimation methodology and the performance of multi-GHz energy-efficient asynchronous pipelined circuit using MOS current-mode logic. Asynchronous MCML pipelined circuits combine the potential advantages of MCML and asynchronous circuits to improve performance, to reduce energy consumption, and to provide an analog-friendly environment. An MCML C-element gate and an MCML double-edge triggered flip-flop are introduced to implement micropipeline circuits. Furthermore, a delay estimation methodology for single-level and double-level MCML gates is proposed to help obtain the associated transistor sizes. An asynchronous MCML FIFO, implemented as a micropipeline structure, demonstrates a throughput of 4 GHz and dissipates 3.65 mW. The MCML micropipeline control circuit for this FIFO dissipates up to four times less energy compared to a conventional CMOS control circuit with the same throughput. Our asynchronous MCML implementation of a 4-bit Brent-Kung carry lookahead adder runs at 2 GHz and dissipates 17.6 mW, while its 8-bit version runs at 0.45 GHz and dissipates 51.37 mW. The simulated results are based on extracted post-layout simulations. All circuits are implemented in a standard 0.18 μm CMOS technology.

The information used in this thesis comes in part from the research program of Dr. Maitham Shams and his associates in the VLSI group. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Maitham Shams and his associates for educational and research purposes, including publication in open literature with appropriate credits.

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List of Abbreviations

Nomenclature

I_{ss}	Current of MOS current-mode logic
ΔV	Voltage swing of MOS current-mode logic
I_{avg}	Average of tail current
V_{in}	Input voltage swing
V_{cm}	Input common-mode voltage
mp	Label of PMOS load transistor
md	Label of NMOS differential input transistors
mn	Label of current source transistor
V_{rep}	Control voltage of PMOS load transistor
V_{ren}	Control voltage of current source
V_x	Drain voltage of the current source
V_H	Output logic-high voltage
V_L	Output logic-low voltage
γ_1	Body effect coefficient when the substrate doping concentration is N_{ch}
γ_2	Body effect coefficient when the substrate doping concentration is N_{sub}
N_{ch}	Channel doping density in atoms/ m^3
N_{sub}	Channel doping density of the p-type substrate in atoms/ m^3
ϕ_f	Fermi potential in the bulk
G_{ox}	Gate oxide thickness

q	Magnitude of electronic charge
ϵ_s	Permittivity of silicon
V_{mb}	Maximum substrate bias voltage
X_t	Depletion width
X_{bx}	Body bias when the depletion width is X_t
ΔV_{th}	Threshold voltage reduction due to the short channel effect
$\theta_{th}(L)$	Short channel effect coefficient
V_{bi}	Built-in voltage of a PN junction between the substrate and the source
K	Technology dependent parameter,
α	Velocity saturation index
D_r	Delay of charging up $C_{L,pos}$
D_f	Delay of discharging $C_{L,neg}$
D_{AMCML}	Propagation delay of asynchronous MCML gate
$C_{L,pos}$	Estimated load capacitance in charging
$C_{L,neg}$	Estimated load capacitance in discharging
R_D	Effective resistance of the PMOS load transistor
dI/dt	Changing power supply current due to the switching activities
C_L	Output load capacitance

Abbreviations

AMCML	Asynchronous MOS current-mode logic
C-element	Control circuit of Micropipelines

CMRR Common Mode Rejection Ratio

CMOS..... Complementary-Metal-Oxide-Semiconductor

CMOSP18..... Fabrication technology (Standard CMOS 0.18 μm)

CORDIC..... COordinate Rotation DIgital Computer

CQFP Ceramic Quad Flat Pack, a type of package

DETFF Double-Edge Triggered Flip-Flop

DC..... Direct Current

DRC Design Rule Checker, a tool

EDA Electronic Design Automation

ESD..... Electrostatic Discharge

EMI..... Electro-Magnetic Interference

FIFO First In First Out

HSPICE A circuit simulator

KVL Kirchhoff's Voltage Law

LVS..... Layout vs. Schematic, a tool

MCML MOS Current-Mode Logic

MOSFET Metal-Oxide-Semiconductor Field Effect Transistor

N.A. Not Available/Not Applicable

PCB..... Printed Circuit Board

ringosc Ring Oscillator

Spectre A circuit simulator

SMA/SMB Types of RF connectors

TYPICAL..... A process corner

VLSI..... Very Large Scale Integration

This chapter describes the focus of this thesis and the motivation behind this work. Furthermore, it explains the thesis organization.

1.1 Motivations

In the past decade, many researchers have sought new digital circuit strategies to reduce the effect of clock skew, the effect of switching noise, and the problem of clock synchronization, while maintaining high speed and acceptable levels of power dissipation. The implementation of asynchronous circuits in MCML satisfies such demands.

Static synchronous CMOS circuits have increasingly difficult challenges to overcome in terms of clock skew and switching noise in ultra-deep-submicron design. This has made asynchronous circuit design an increasingly practical alternative. Potential advantages of asynchronous circuits over synchronous circuits are higher speed, lower power dissipation, and higher modularity [1,3]. Asynchronous circuits are also free from the problem of clock skew and have relatively low electromagnetic interference, because of their distributed switching activities in time. MOS current-mode logic, on the other hand, is a high-speed design topology that has primarily been employed in CMOS transceivers for SONET applications in broadband communication circuits [24]. The operation and structure of MCML circuits are discussed in [17]. Advantages of MCML over conventional CMOS logic style include higher speed due to much smaller signal swing and fre-

Chapter 4 illustrates an algorithm to estimate an MCML gate delay and find the transistors' sizes. The theory in Chapter 4 is later used in Chapter 5 and Chapter 7 to find the transistors' sizes of the MCML gates.

Chapter 5 presents the transistor-level design of an MCML C-element gate and two different topologies of MCML C-element gates. Their simulation results are also presented along with a comparison with conventional CMOS C-element gate. The asynchronous MCML C-element gates in Chapter 5 are later used in Chapter 7 to construct a FIFO circuit and a pipelined binary carry-lookahead adder as the basic elements of arithmetic and signal processing units.

Chapter 6 presents the transistor-level design of an MCML Double-Edge Triggered Flip-Flop. This chapter also illustrates two topologies of MCML DETFF gates and their simulation results. Comparison of two different MCML DETFF gates and a conventional CMOS DETFF is reported as well.

Chapter 7 presents the use of an MCML C-element gate and an MCML DETFF to construct an asynchronous MCML FIFO and asynchronous MCML pipelined adders. The layout and simulation results are detailed.

Chapter 8 concludes the thesis with a discussion of the results and future work on asynchronous MCML pipelined circuits.

Appendices contain supporting information on delay estimation procedure and MCML gate layouts.

MCML Gate Design Description

This chapter briefly discusses the design of MCML gates. The historical background of MCML, basic architecture, operation and theory of MCML gates are discussed. The advantages of MCML over conventional CMOS logic are presented. The challenges of MCML design are discussed.

2.1 Brief history of MCML gates

MCML style is one of the high-speed CMOS circuit topologies and have been adapted from bipolar CML, a derivative of emitter-coupled logic (ECL). Some circuit designers in Japan first introduced and employed MCML gates in a processor operating at a GHz frequency range in the early 1990s [7]. In [8] and [9], a 64-bit MCML adaptive pipelined adder and an MCML adaptive pipelined CORDIC logic were developed and simulated. They demonstrated that the MCML adaptive pipelined circuit dissipates less power than the equivalent CMOS circuit and is less sensitive to common-mode noise and clock skew. Furthermore, a feedback MCML design technique is proposed in [24] which demonstrates that the tolerance for threshold voltage fluctuations and the bandwidth are both enhanced by introducing the feedback in MCML circuits. Additionally, multi-threshold MCML and self-timed MCML circuits are introduced in [29] and [30]. Both modified

MCML circuits demonstrate lower power consumptions, while maintaining the throughput, compared to ordinary CMOS circuits. In recent time, MCML is primarily employed in CMOS transceivers for SONET applications in broadband communication circuits.

2.2 Basic structure of MCML

The structure of an MCML gate consists of a differential logic tree, resistor loads and a constant current source. The differential structure of MCML gate is advantageous in terms of performance and noise tolerance. Similar to Differential Cascode Voltage Switch Logic (DCVS) [10], Differential Split-level Logic (DSL) [11] and Charge-Recycling Differential Logic (CRDL) [12], MCML has a differential structure and complementary inputs. However, unlike the other logic styles, MCML has a constant current source and PMOS devices as resistor loads. Constant current source in MCML can substantially reduce dI/dt effect on the voltage supply rail. The structure of load resistance in MCML is simpler than that of a cross-coupled NMOS-PMOS load in other differential CMOS logic styles. Output nodes of MCML have less parasitic capacitance and produce faster response. MCML is chosen for high-speed applications over other differential CMOS logic styles. A simple MCML block diagram is presented in Figure 2.1 below:

The constant current source provides steady current I_{ss} to the MCML gate. The load is the Pull-up network PMOS transistors operating in the linear region. The logic function of the MCML gate is represented by the configuring of the NMOS differential logic tree. In general, the NMOS differential logic tree may have more than two pairs of differential transistors stacked on top of each other. The performance of an MCML gate may degrade if the NMOS differential logic tree has more than two differential input signals, because the input differential transistors do not switch on or off completely.

Figure 2.1: Block diagram of an MCML gate

2.3 Basic operation and theory of MCML

The fundamental idea of an MCML gate operation is to switch the differential pair transistors on or off completely in response to the input differential signals. Input differential pair transistors ideally steer the steady current I_{ss} completely to either the left or right branch of the MCML gate. The drain terminals of the differential-pair transistors in series with the PMOS load are the complementary output nodes. During the operation, one of the differential output voltages is V_{dd} and the other output voltage node swings to $V_{dd} - I_{ss}R_D$ where R_D is the effective resistance of the PMOS load. The typical output voltage swing is about 20% of the power supply. In our MCML circuit design, V_{dd} is 1.8 V and the output voltage swing is chosen to be 300 mV to 500 mV for robustness and noise immunity. That range of voltage swing is chosen based on the experimental results. Due to the differential structure of MCML, it is immune to common-mode noise. Before

we elaborate the design of MCML circuits, the theoretical formulas and mathematical equations of MCML design are introduced. Two setups and sets of equations are utilized to calculate the delay, power and energy of MCML gates in this thesis. The first testbench is to connect the output of an asynchronous MCML chain to its input to form a ring oscillator to find the maximum speed of the single asynchronous MCML gate. The second testbench is to excite the MCML gates by connecting an external input signal and an output load capacitance, C_L . In the first set of equations, the propagation delay of a single asynchronous MCML gate is

$$D_{AMCML} = \frac{2}{f_{stage}} \quad (2.1)$$

where f_{stage} is the frequency of operation of each stage. The above equation is the total propagation delay of a single asynchronous MCML gate in response to a single input event from the adjacent stage in the ring oscillator circuit. The total propagation delay D_{AMCML} is the duration of the output waveform swinging from logic level high to logic level low and is equivalent to a half of the period of the oscillation frequency. D_{AMCML} is independent of the number of stages because each stage of an asynchronous MCML pipelined circuit operates at its own speed. First set of equations will be used in Chapter 5 and 7 to find the propagation delay and power dissipation of asynchronous MCML pipelines.

In the second set of equations, corresponding to the second setup, total propagation delay of a single MCML gate are calculated as follows [13].

$$D_{MCML} = \frac{C_L \times \Delta V}{I_{ss}} \quad (2.2)$$

$$P_{MCML} = I_{ss} \times V_{dd} \quad (2.3)$$

where ΔV is the voltage swing of the MCML gate, I_{ss} is the constant current source and C_L is the output load capacitance. In MCML power dissipation equation, the sum of static

and dynamic components is constant, to first order [13]. The second set of equations will be used in the delay estimation procedure in Chapter 4.

The delay and power dissipation of a conventional CMOS logic gate are expressed below [6]. The CMOS logic voltage waveform is assumed to be full swing. The equation of power dissipation below is the power of the conventional CMOS logic gate at its maximum frequency.

$$D_{CMOS} = \frac{C_L \times V_{dd}}{2 \times I_{CMOS}} \quad (2.4)$$

$$P_{CMOS} = C_L \times V_{dd}^2 \times f \quad (2.5)$$

where f is the switching activity of the conventional CMOS logic gate. I_{CMOS} is the current from power supply to charge and discharge C_L . Equation (2.4) and Equation (2.5) will be used for design circuits in Chapter 5, 6, and 7.

2.4 Advantages of MCML over conventional CMOS logic

In high-speed, low-power design, MCML has many advantages over conventional CMOS logic in terms of high speed, low power, power/ground noise, immunity to common-mode noise and dynamic frequency adjustment.

2.4.1 High speed

MCML has a differential architecture and responds to differential input signals that switch on or off the NMOS differential transistors. The input capacitances of the differential architecture have only the parasitic capacitances associated with the gate terminals of the NMOS differential transistors. On the other hand, conventional CMOS gate architecture has the PMOS transistor in series with the NMOS transistor to achieve the full voltage swing at the output node. The input capacitances of the conventional CMOS gate have the parasitic capacitances associated with gate terminals of both the NMOS transistor and

PMOS transistor. Also, the switching time of an NMOS transistor is faster than that of a PMOS transistor, due to faster mobility of the electrons than that of holes. An MCML gate is faster than a similar conventional CMOS logic gate because of the absence of PMOS gate capacitances. Furthermore, the reduction of the output voltage swing can improve the speed of the MCML gate. From Equation (2.2), the delay of an MCML gate is directly proportional to the voltage swing. The smaller the voltage swing, the higher the speed of the MCML gate. The voltage swing in an asynchronous MCML circuit is chosen to be about 300 mV - 500 mV.

2.4.2 Low power

The constant current source of MCML provides steady current to the differential logic tree that is switched on or off in response to the differential input voltages. Hence, the power dissipation of MCML gates is independent of the input signal frequency. An MCML gate dissipates the same amount of power as the operation frequency increases. However, conventional CMOS gate has frequency-dependent power dissipation. Power dissipation of a conventional CMOS gate is directly proportional to the operating frequency. Hence, in multi-GHz range, MCML gates dissipate less power than conventional CMOS logic gates performing the same function [6].

2.4.3 Low power/ground noise

Power/ground noise, or dI/dt , effect from digital circuits has adverse effects on neighbouring noise-sensitive analog or RF circuits. MCML gates, with its constant current source, has nearly negligible dI/dt effect. However, conventional CMOS gates have a substantial amount of current spike during switching of the output nodes.

2.4.4 Immunity to common-mode noise

The differential operation of an MCML gate is immune to common-mode noise [25]. A noisy signal line corrupts the sensitive and differential signals which are distributed as two equal and opposite phases. The corruptions on the differential signal lines disturb the differential signal lines by equal amounts. The undesirable effects on the differential signal lines are cancelled out. However, a conventional CMOS gate has no immunity to the common-mode noise and may malfunction in the presence of common mode noise. However, the rail-to-rail voltage swing in conventional CMOS gate boosts its noise tolerance.

2.4.5 Dynamic frequency adjustment

The propagation delay of an MCML gate is directly proportional to the amplitude of the output voltage swing and can be increased or decreased by changing the control voltage of the current source and control voltage of the PMOS load transistor.

2.5 Challenges of MCML design

MCML has many advantages over conventional CMOS logic. However, MCML designers must overcome many challenges of MCML design in terms of large circuit area, complex design and overhead of bias voltage circuits.

2.5.1 Large circuit area

MCML has the symmetrical structure and differential signals. Transistor count of MCML gates is more than that of conventional CMOS gates. Also, MCML gates are powered by the constant current source which consume extra silicon area. Area of MCML gates are larger than that of the conventional CMOS gates.

2.5.2 Complex design

The structure of MCML gates is more complex than that of conventional CMOS gates. More design parameters need to be considered in the MCML design, such as non-linearity of the PMOS load resistor, control voltages of PMOS load resistor and current source, signal voltage swing and bias current, etc. Those parameters complicate the MCML design. More expertise is required on MCML design. MCML gate delay estimation procedure in Chapter 4 is fast and convenient way to obtain the transistor sizes in single and double-level MCML gates.

2.5.3 Overhead of bias voltage circuits

MCML gates consist of PMOS load transistor and NMOS current source. Constant and reliable bias voltages are necessary to keep the PMOS load transistor and NMOS current source in linear region and saturation region respectively. Band-gap-referenced bias circuits are employed to provide such constant bias voltages. However, area penalty of Band-gap-referenced bias circuits is added on the MCML circuit system.

2.6 Basic MCML gates

Schematic diagrams of the basic MCML gates are given in this section. Schematic diagrams of MCML inverter, buffer, XOR gate, AND gate, OR gate, and MUX gates are presented in Figure 2.2 below:

Figure 2.2: Schematic diagrams of basic MCML gates

Asynchronous Circuits - System Level Design

This chapter describes the potential advantages of asynchronous circuits in ultra-deep submicron design. Challenges of asynchronous circuit design are discussed. Basic elements for building asynchronous circuits are illustrated. Asynchronous circuits based on micropipeline are introduced and their operations are described. The handshaking signal protocol of asynchronous MCML pipelined circuit is illustrated. In this chapter, the word “event” stands for a signal transition on a control signal in an asynchronous circuit.

3.1 Potential advantages of asynchronous circuits

Conventional CMOS synchronous circuits in ultra-deep submicron design have increasingly difficult challenges to overcome in terms of clock skew, clock network distribution and switching noise. These challenges make asynchronous circuits a more practical alternative. Potential advantages of asynchronous circuits over synchronous circuits are high-speed, low-power, high modularity, no clock skew and low electromagnetic interference.

3.1.1 High-speed

Synchronous circuits have a global reference clock signal to regulate the speed of the circuit. The clock period must be long enough to accommodate the maximum delay of the critical path, clock skew, delay of interconnect wire and process or environment varia-

tion. These make synchronous circuits exhibit worst-case performance. On the other hand, asynchronous circuits have no clock restriction and run at their own speed. When the sub-modules inside asynchronous circuits complete a job earlier, the next job can be started earlier. Asynchronous circuits exhibit average-case performance and potentially run faster than synchronous circuits with equivalent throughput.

3.1.2 Low-power

Clock-related power dissipation can reach up to 30-40% of the total power dissipation of a synchronous microprocessor [4] and [5]. The absence of a global clock signal means there is no power consumption related to the clock; such as, clock networks and clock buffers. Asynchronous circuits only consume power when the incoming data is available. In contrast, synchronous circuits consume power at every clock edge regardless of the presence of new data.

3.1.3 High-modularity

Asynchronous circuits are composed of circuit blocks with well-defined interfaces. Integrating asynchronous circuits is a simple matter of connecting the wires of two circuits with identical interconnect specifications. Also, asynchronous circuits run at their own speed. This allows designers to replace obsolete circuits easily because they can connect two circuits with different speeds by identical interconnect specifications in an asynchronous system. However, in synchronous circuits, designers need to spend substantial time and resources to consider the clock related problems when they replace the obsolete circuits.

3.1.4 No clock skew

Clock skew is defined as the different arrival time of the clock in different parts of the circuit. Asynchronous circuits do not have a global clock. Problems related to clock skew do not exist in asynchronous circuit design. On the other hand, synchronous circuits

have clock skew that makes the digital circuit design more difficult in the ultra-deep sub-micron regime.

3.1.5 Low electromagnetic interference

In asynchronous circuits, the switching activities are evenly distributed in time across the chips. The latches and logic gates are active in the presence of new incoming data. When no new data is available, they are in an idle state. However, latches and logic gates in synchronous circuits are activated at every clock cycle. Hence, the switching activities in synchronous circuits are almost all concentrated at or near the clock edge. This generates a relatively large dI/dt and results in high electromagnetic interference.

3.2 Challenges of asynchronous circuit design

Asynchronous circuit designer has to overcome many challenges of asynchronous circuit design. These challenges are overhead of control circuits, unpopular asynchronous circuit design CAD tools and complex timing model.

3.2.1 Overhead of control circuits

Asynchronous circuits have handshaking signals to regulate the data flow of the pipelining. Control circuits of asynchronous circuits handle the handshaking signals to cooperate each stage. Asynchronous circuits suffer the area penalty of the control circuits.

3.2.2 Unpopular asynchronous circuit design CAD tools

Most of the digital design CAD tools focuses on synchronous circuit design. It is necessary to make the in-house CAD tools of asynchronous circuit design.

3.2.3 Complex timing model

Asynchronous circuit design depends on the high accurate timing model to ensure the correctness of operation. Asynchronous circuit designers have to spend more time on estimating the delay of the asynchronous logic and interconnect wires.

3.3 Basic building blocks of asynchronous pipelines

Micropipeline was first introduced by Ivan Sutherland in his Turing award lecture in 1988 [1]. He demonstrated that complex asynchronous pipelined systems can be constructed of two basic elements: Mullar C-element and event-controlled storage element.

3.3.1 Mullar C-element

The Mullar C-element, a control circuit of micropipelines, synchronizes the data signal from the previous stage by handshaking signals. The behavior of the Mullar C-element is described as follows. The output value is changed to 0 (1) if the input values are 0

(1); otherwise the output value remains the same. The Boolean function of the Mullar C-element is expressed by $c = \{[c \cdot (a + b)] + (a \cdot b)\}$ [3]. A symbol and schematic diagram of the Mullar C-element is shown in Figure 3.1.

Figure 3.1: Symbol and schematic diagram of Mullar C-element

3.3.2 Event-controlled storage element

The event-controlled storage element captures new data from the adjacent stage of the micropipeline at rising and falling edges of the control signal. An event-controlled storage element is illustrated in Figure 3.2.

Figure 3.2: Symbol and block diagram of event-controlled storage element

The event-controlled storage element incorporates two inverter loops, input switches, $s1$, output switch, $s2$, and an output inverter. Capture, C , and Pass, P , are control signals

represented by the solid lines. The direction of the data flow is represented by the dashed lines with arrows. Capture and Pass control signals regulate the timing of the data flowing through the storage element. Input switches, s_1 , are controlled by C . Output switch, s_2 , is regulated by P . The capture Acknowledge signal, Cd and Pass Acknowledge, Pd , signal are used to signal the adjacent stage for completion of the data transition. The operation of the two-phase micropipeline is shown in the following steps:

- 1) The event-controlled storage element is in the initial state and is in transparent mode as shown in the Figure 3.2.
- 2) Sender sets up new data and issues an event on the Capture signal to request the latch to capture the incoming data. Input switches, s_1 , are flipped to the lower position to form an inverter loop latch.
- 3) An acknowledge event, Cd , is sent back to the sender after the data is latched.
- 4) When the data at the output is captured by the next stage, an event is issued on the Pass control signal. Output switch, s_2 , is flipped to the upper position.
- 5) The storage element is in the transparent mode again. An event is issued to the control circuit of the previous stage through the Pass Acknowledge, Pd . The control circuit of the previous stage acknowledges that the storage element is in transparent mode and ready to capture the next input data.
- 6) The storage element is in its complementary state compared to the initial state. The procedure of operation is repeated in step one until no new data is presented.

3.4 Micropipeline

Pipelining is a powerful technique for constructing low-power high-performance processors. Power reduction can be obtained by using an architecture-based voltage scaling strategy, which includes pipelining and parallelism [6]. Further power reductions can potentially be made in asynchronous pipelined circuits, because asynchronous circuits have no clock-related power dissipation through clock network and clock buffers. Ivan Sutherland's elastic Micropipelines [1] are practical asynchronous circuits that have gained much attention in the VLSI community. The block diagram of a four-stage micropipeline is shown in Figure 3.3.

Figure 3.3: Block diagram of the four-stage micropipeline

The block diagram of four-stage micropipeline consists of a control circuit as C-element, storage element as REG, delay element as Delay and combinational logic as Logic. The solid lines represent the control signal lines, and the dashed lines with arrows represent the direction of the data flow. The handshaking signals, Req_{in} and Ack_{out} , are utilized to communicate between the sender and the first stage. Req_{out} and Ack_{in} are the handshaking signals to synchronize the output data with the consumer and the last stage. Data is implemented with single-rail encoding [3], and the data path is as wide as the registers can accommodate. Adjacent stages of the micropipelines communicate through a two-

phase, bundled-data signalling protocol [3]. To satisfy the data bundling constraint, delay elements may be required to slow down the propagation of the request signals. The operation of two-phase micropipeline is shown by following steps:

- 1) Data is setup by the sender of the micropipeline.
- 2) Sender issues an event on $Req_{(in)}$ line to indicate the presence of new incoming data.
- 3) C-element receives the event and signals the latch to transparent.
- 4) Latch passes the data to the logic and issues an event on $Ack_{(out)}$ to inform the sender the completion of the data transition.
- 5) To align the arrival time of the acknowledge signal with the arrival time of data from the preceding stage, the acknowledge signal is delayed with the same time as the maximum delay of the preceding stage logic.
- 6) The second stage C-element receives a signal from the first stage and issues an event.
- 7) Second stage latch responds to the event from the C-element and becomes transparent. Then the second stage latch fires an event which goes to the first stage and the delay element of the second stage.
- 8) The first stage latch receives the event from the second stage, changes from transparent to opaque state and holds the data value.
- 9) The same procedure repeats from step 4 until the input data propagates to the consumer of the micropipelines.

3.5 Handshaking protocol

A handshaking protocol is used to maintain the correct ordering of data and operations. When data is transferred, it is bundled with a control signal which represents the timing information to indicate data validity. In an asynchronous circuit, there are two handshaking protocols which are the two-phase and the four-phase handshaking protocol [3]. Two-phase handshaking protocol is employed in the asynchronous MCML pipelined circuit. In this thesis, the two-phase handshaking protocol, which is explained in the next sub-section, is used.

3.5.1 Two-phase handshaking protocol

The block diagram and timing diagram of two-phase handshaking protocol is shown in Figure 3.4

Figure 3.4: Block diagram and timing diagram of two-phase handshaking protocol

Data is passed by the sender which issues an event on the request line to inform the receiver of the availability of valid data. Valid data is sampled by the receiver which issues an event on the acknowledge line. Falling and rising transitions alternate on the request and acknowledge lines. Both transitions on a line carry the same meaning and the signal levels are not important [3].

MCML Gate Delay Estimation

This chapter proposes a method to estimate delay of single-level and two-level MCML gates. This procedure gives designers a guideline on estimating MCML gate delay and finding the associated MCML transistor sizes. The results of the delay estimation procedure are reported. Throughout this chapter, the smallest transistor width in the layout is set to $0.6\ \mu\text{m}$ due to layout consideration.

4.1 Delay estimation goal and strategy

The principal goal of the MCML gate delay estimation procedure is to allow designers to quickly estimate the MCML gate delay and find associated transistor sizes of MCML gates without blindly sweeping all transistor parameters in the simulator. Also, the delay estimation procedure provides designers with critical parameters, such as propagation delay and power. Asynchronous circuit design requires an accurate timing model of the logic gate. Timing in asynchronous circuit design is extremely important. This procedure can estimate the propagation delay of an MCML gate with less than 18% discrepancy compared to Spectre simulation. The designer selects the initial values of two design parameters, voltage swing ΔV and current I_{ss} in the beginning of the delay estimation procedure. The delay estimation procedure incorporates the following equations: equivalent linear resistance equation [17], equation for threshold voltage of the MOSFET with non-uniform substrate doping effect and short channel effect [18], Alpha-Power Law [14]

and other fundamental circuit equations to obtain the transistor aspect ratio of the MCML gates. The proposed delay estimation procedure can be extended to develop an automation tool for MCML design optimization in future work.

4.2 Simulation testbench

An MCML ring-oscillator is a good testbench to estimate the speed of the MCML gate without inserting any additional capacitance. Therefore, prior to the delay estimation procedures of MCML gate, the ring-oscillator testbench is introduced.

Figure 4.1: Nine-stage MCML inverter ring oscillator

A nine-stage MCML inverter chain is shown in Figure 4.1. An odd number of stages is used to maintain the MCML ring-oscillator in an unsteady state and to self-oscillate with reasonable gain in each stage. MCML inverters are used in the nine stage ring-oscillator as a simple example to compare the theoretical results with the simulated results. Spectre transient analysis is used for simulation.

4.3 List of core equations in procedure

In this proposed delay estimation procedure, several basic microelectronic circuit equations and the method of extracting their parameters are reviewed prior to the description of the delay estimation procedure. The symbols in the equations refer to Figure 4.2 below:

Figure 4.2: Schematic diagram of an MCML inverter gate

mp represents the PMOS load transistor. *md* represents the differential pair transistor. *mn* represents the NMOS current source. The first core equation given below models the equivalent linear resistance of the PMOS load transistor in the MCML gate [17] and [18]:

$$R_D = \frac{R_{int}}{1 - \frac{R_{DS}}{R_{int}}} \quad (4.1)$$

where R_{DS} , source/drain parasitic resistance, is denoted by [17]:

$$R_{DS} = (R_{DSW} \cdot 0.18e^{-6} / W_{mp}) \quad (4.2)$$

R_{int} , the intrinsic PMOS resistance in Equation (4.1), is expressed by:

$$R_{int} = \left[\mu_{eff,p} G_{ox} \frac{W_{mp}}{L_{mp}} (V_{dd} - |V_{th,mp}|) \right]^{-1} \quad (4.3)$$

where $\mu_{eff,p}$ is the effective hole mobility and its expression can be found in [18], W_{mp} and L_{mp} are the channel width and length of the PMOS load transistor, G_{ox} is the gate oxide thickness, $V_{th,mp}$ is the threshold voltage of the PMOS load transistor and V_{dd} is the supply voltage.

The second core equation is for the MOSFET threshold voltage including the non-uniform substrate doping and short channel effects. Although this equation ignores the lateral non-uniform doping effect, it is accurate enough to model the MOSFET threshold voltage in our procedure. This equation is given below [18]:

$$V_{th} = V_{th0} + K_1(\sqrt{|2\phi_f| + V_{sb}} - \sqrt{|2\phi_f|}) + K_2 V_{sb} - \Delta V_{th} \quad (4.4)$$

where V_{th0} is the threshold voltage for a source-body voltage equal to zero, i.e. $V_{sb} = 0$. ϕ_f is the Fermi potential in the bulk and ΔV_{th} is the threshold voltage reduction due to the short channel effect. K_1 and K_2 are determined by the criteria that V_{th} and its derivative versus V_{sb} should be the same at V_{mb} , where V_{mb} is the maximum substrate bias voltage. K_1 and K_2 are denoted as following [18]:

$$K_1 = \gamma_2 - 2K_2\sqrt{|2\phi_f| + V_{mb}} \quad (4.5)$$

$$K_2 = (\gamma_1 - \gamma_2) \frac{(\sqrt{|2\phi_f| + V_{bx}} - \sqrt{|2\phi_f|})}{2\sqrt{|2\phi_f|}(\sqrt{|2\phi_f| + V_{mb}} - \sqrt{|2\phi_f|}) - V_{mb}} \quad (4.6)$$

where γ_1 (or γ_2) is the body effect coefficient when the substrate doping concentration is N_{ch} (or N_{sub}). γ_1 and γ_2 are given as follows:

$$\gamma_{1/2} = \frac{1}{G_{ox}} \sqrt{2q\epsilon_s N_{ch/sub}} \quad (4.7)$$

where G_{ox} is the gate oxide thickness, q is the magnitude of electronic charge, ϵ_s is the permittivity of silicon, N_{ch} is the channel doping density and N_{sub} is the doping density of the p-type substrate. ϕ_f in Equation (4.4) is denoted as follows:

$$\phi_f = \phi_t \ln\left(\frac{N_{sub}}{n_i}\right) \quad (4.8)$$

where ϕ_t is thermal voltage [16] and n_i is the intrinsic carrier concentration.

The third core equation is the Alpha-Power Law, which includes the carrier velocity saturation effect in the short-channel MOSFET. This equation is an extension of Shockley's square-law MOS model in the saturation region [14]. Alpha-Power Law model in equation form is given below:

$$I_{ss} = \frac{W}{L} K (V_{gs} - V_{th})^\alpha \quad (4.9)$$

where K is a technology dependent parameter, α is the velocity saturation index, I_{ss} is the drain current of the transistor, W and L are the channel width and length and V_{gs} is the gate-source voltage.

The delay of the MCML gate is always associated with charging or discharging total capacitances at the output node. The general delay equation of MCML is denoted in Equation (2.2). The load capacitances of positive and negative voltage transitions, $C_{L,pos}$ and $C_{L,neg}$, are not the same because PMOS and NMOS transistors at the output node are in different operation regions during these transitions. The delay equation states that the delay, D_r , for charging up capacitance $C_{L,pos}$ with current I_{ss} is:

$$D_r = \frac{C_{L,pos} \Delta V}{I_{ss}} \quad (4.10)$$

The delay, D_f , for discharging capacitance $C_{L,neg}$ with current I_{ss} is:

$$D_f = \frac{C_{L,neg} \Delta V}{I_{ss}} \quad (4.11)$$

The total propagation delay of an MCML gate, shown in Equation (4.12), is the average of its rising and falling output signal transition delays:

$$D = \frac{D_r + D_f}{2} \quad (4.12)$$

4.4 Design parameters & constraints

Design parameters in the delay estimation procedure are categorized into three groups, input parameters, median parameters and output parameters. They are tightly coupled with each other and are calculated in order.

4.4.1 Input parameters

The input parameters are the designer defined parameters. The list of input parameter names and their descriptions are shown in Table 4.1 below:

TABLE 4.1: Input Parameter Descriptions

<i>Input Parameter Name</i>	<i>Description</i>
ΔV	Peak-to-peak voltage swing
I_{ss}	Current produced by current source

4.4.1.1 Voltage swing

Voltage swing of MCML is the voltage drop across the PMOS load transistor. Reducing the voltage swing on the output node is an effective way to minimize the total propagation delay of MCML gates. From Equation (2.2), the total propagation delay is directly proportional to the voltage swing. However, inadequate voltage swing reduces the gate's noise margin and causes the malfunction of MCML in the presence of noise during operation. Based on experimental results, the voltage swing of MCML gate in our delay estimation procedure is chosen between 300 mV to 500 mV.

4.4.1.2 Current

Current is the fundamental design parameter in MCML delay estimation. Minimizing the amount of current flowing through MCML gates is the most important design strategy of low-power circuit design. Furthermore, increasing current decreases the propagation delay of the MCML gates because of the faster charging and discharging time of the output load capacitances.

4.4.2 Median parameters

The median parameters are generated in the middle of the delay estimation procedure. The list of median parameter names and descriptions are shown below:

TABLE 4.2: Median Parameter Descriptions

<i>Median Parameter Name</i>	<i>Description</i>
V_H	Upper limit of voltage swing
V_L	Lower limit of voltage swing
V_{cm}	Common-mode voltage
V_{th}	Threshold voltage with $V_{sb} \neq 0$
V_x	Drain voltage of current source
$C_{L,pos}$	Load capacitance of positive output transition
$C_{L,neg}$	Load capacitance of negative output transition

4.4.2.1 Upper and lower limit of voltage swing

The upper and lower limit of the voltage swing determines the logic high voltage or logic low voltage of the MCML. With a larger difference between V_H and V_L , better noise margin can be obtained. The disadvantage of large difference between V_H and V_L is a delay penalty. V_H is given below:

$$V_H = V_{dd} \quad (4.13)$$

The output node is logic high when the differential input transistor is inactive. The output node voltage is pulled up to the highest voltage potential of the gate. Therefore, V_H is equal to voltage supply V_{dd} . V_L is denoted as follows:

$$V_L = V_{dd} - I_{ss} \times R_D \quad (4.14)$$

The output node is pulled down to V_L when the differential input transistor is active. All current is steered to the one branch.

4.4.2.2 Common-mode voltage

Common-mode voltage V_{cm} is the mid-swing voltage or DC operating point. The value of V_{cm} is the average voltage of V_H and V_L . V_{cm} is given below:

$$V_{cm} = \frac{V_H + V_L}{2} \quad (4.15)$$

4.4.2.3 Drain voltage of current source

It is critical to minimize the voltage fluctuation of V_x when the MCML gate operates in the multi-GHz range. V_x is denoted as follows:

$$V_x \geq V_{dd} - \Delta V - V_{th} \quad (4.16)$$

One of the methods is to increase the output impedance of the current source by increasing its length. However, the channel width of the current source transistor has to increase as much as the length to keep the same amount of current. For proper switching, the voltage $V_{dd} - \Delta V$ must be low enough to switch off NMOS differential transistors of the next stage. Reducing V_x can improve the performance of the circuit because a smaller threshold voltage V_{th} of the differential transistor is obtained. V_x is the source voltage of differential-pair transistor. Decreasing V_x will decrease V_{sb} of differential-pair transistor. In Equation (4.4), decreasing V_{sb} will decrease V_{th} . The following table illustrates the relationship between V_x and other parameters.

TABLE 4.3: Relationship between drain voltage of the current source and other parameters

I_{ss}	w_{M_d}	V_x
↓	↑	↑
↑	↓	↓

where w_{M_d} is the width of the differential-pair transistor. I_{ss} is the parameter. V_x is inversely proportional to I_{ss} . Increasing I_{ss} increases V_{gs} of the NMOS differential pair. Increasing V_{gs} will decrease V_x because the source terminal voltage of the NMOS differential pair decreases. On the other hand, if I_{ss} is constant, decreasing w_{M_d} will increase V_{gs} of the NMOS differential pair and decrease V_x .

4.4.2.4 Load capacitances of positive and negative transitions

Load capacitances of positive and negative transitions, $C_{L, pos}$ and $C_{L, neg}$, are calculated according to the total parasitic capacitances at the output node of the MCML gate.

Figure 4.3 illustrates the different parasitic capacitances at the output node. Two stages of

Figure 4.3: Different parasitic capacitances at the output node

the nine-stage MCML inverter ring-oscillator are shown in the Figure 4.3. The connection between out_cell and in_drive is drawn in the diagram for illustration. The rest of the connections are removed for clarity. $C_{L, pos}$ and $C_{L, neg}$ are composed of the drain capacitance of the PMOS load transistor, $C_{d_{PMOS}}$, in the cell stage, the drain capacitance of the NMOS, $C_{d_{NMOS}}$, in the cell stage and the gate capacitance of the NMOS, $C_{g_{NMOS}}$, in the drive stage. However, the capacitances $C_{L, pos}$ and $C_{L, neg}$ are not the same because the PMOS and NMOS transistors at the output node are in different operating regions during

positive and negative transitions. In the negative output transition, $C_{L,neg}$ has an initial value of logic high and is discharged by the cell stage. The total output load capacitance of the negative transition is the summation of the parasitic capacitances as shown in the following table:

TABLE 4.4: List of output parasitic capacitances for negative transition

<i>Transistor</i>	<i>Operating mode</i>	<i>Capacitance</i>	<i>Description</i>
PMOS (Cell)	Triode	$C_{d_{PMOS}}$	$\frac{C_{gc}}{2} + C_{ov} + C_{jdb} + \frac{C_{cb}}{2}$
NMOS (Cell)	Off	$C_{d_{NMOS}}$	$C_{jdb} + C_{ov}$
NMOS (Drive)	Saturation	$C_{g_{NMOS}}$	$\frac{2}{3}C_{gc} + 2C_{ov}$

where C_{gc} is the gate-to-channel capacitance, C_{ov} is the gate-drain overlap capacitance, C_{jdb} is the drain-bulk junction capacitance and C_{cb} is the channel-to-bulk capacitance. Expressions for these parasitic capacitances are shown in [19] and [20]. In the positive

output transition, $C_{L, pos}$ has an initial value of logic low and is charged up to V_{dd} by the cell stage. The total output load capacitance of the positive transition is the summation of the parasitic capacitances in the following table:

TABLE 4.5: List of output parasitic capacitances for positive transition

<i>Transistor</i>	<i>Operating mode</i>	<i>Capacitance</i>	<i>Description</i>
PMOS (Cell)	Triode	$C_{d_{PMOS}}$	$\frac{C_{gc}}{2} + C_{ov} + C_{jdb} + \frac{C_{cb}}{2}$
NMOS (Cell)	Saturation	$C_{d_{NMOS}}$	$C_{jdb} + C_{ov}$
NMOS (Drive)	Off	$C_{g_{NMOS}}$	$C_{gc} + 2C_{ov}$

Models of the output load capacitances are rough approximations because the load capacitances during positive and negative transitions change dramatically according to voltage values at the output nodes. More accurate load capacitance models can be found in [26].

4.4.3 Output parameters

Output parameters are the results of the delay estimation procedure. The list of output parameter names and their descriptions are shown below:

TABLE 4.6: Output Parameter Descriptions

<i>Output Parameter Name</i>	<i>Description</i>
W_{mp}	Width of PMOS load transistor
L_{mp}	Length of PMOS load transistor
V_{rep}	Control voltage of PMOS load transistor
W_{md}	Width of NMOS differential pair
L_{md}	Length of NMOS differential pair
D_{MCML}	Propagation delay
P_{MCML}	Power

4.4.3.1 Width and length of PMOS load transistor

Equivalent linear resistance of the PMOS load transistor R_D is tightly coupled with W_{mp} and L_{mp} . Reducing W_{mp} and L_{mp} can minimize the output parasitic capacitances. The tradeoff of PMOS load transistor size and R_D is to optimize the W_{mp} and

L_{mp} with the required R_D . The bandwidth of the MCML gate is maximized by using minimum L_{mp} . By default, L_{mp} is chosen to be $0.18 \mu m$. The following table illustrates the relationship between R_D and PMOS load transistor size.

TABLE 4.7: The relationship between PMOS load resistance and PMOS load transistor size

W_{mp}	L_{mp}	R_D
↓	↑	↑
↑	↓	↓

It is interesting to mention that R_D increases significantly when L_{mp} increases.

4.4.3.2 Control voltage of PMOS load transistor

By default, V_{rep} is chosen as $0 V$ to keep the PMOS load transistor operating in triode region. R_D is linearly proportional to V_{rep} .

4.4.3.3 Width and length of NMOS differential pair

Sizing W_{md} and L_{md} is a critical step in design procedure. High performance of the MCML gate requires low input gate capacitances of the NMOS differential pair. If the size of NMOS differential pair is bigger than necessary, the performance of the MCML gate will be degraded. The same W_{md} and L_{md} for all differential pair transistors are used in order to achieve good matching and symmetrical differential voltage swing. By default, L_{md} is kept to the minimum channel length of $0.18 \mu m$ to minimize the parasitic capacitance. W_{md} is directly proportional to the gain of the MCML gate. With the same amount

of current, increasing W_{md} will increase transconductance, g_m , and decrease V_{gs} . However, an MCML gate requires only a gain of 1.4 [21]. Oversized W_{md} has no benefit on the performance of MCML gate but adds extra parasitic capacitance.

4.4.3.4 Propagation delay and power

Minimizing propagation delay and power are the ultimate goals of low-power, high-speed circuit design. The propagation delay of MCML gate is calculated by using Equation (4.12). Power of MCML gate is calculated by using Equation (2.3).

4.5 MCML gate delay estimation

The proposed delay estimation procedure of the MCML gates provides a guideline on finding the minimum transistor sizes and estimating the delay of MCML gates. The goal of this delay estimation methodology is to achieve an initial starting point on all the transistor sizes in MCML gates and their propagation delay under the ideal environment. Some adjustments of the transistor sizes may be necessary in presence of the capacitance associated with the interconnecting wires in the layout. Here is a flow chart for the proposed single-level MCML delay estimation procedure.

Figure 4.4: Flow chart of proposed delay estimation procedure

The following steps summarize the delay estimation of single-level MCML gate.

1. Select a reasonable output voltage swing ΔV and current I_{ss} . Upper limit swing V_H , lower limit swing V_L and common-mode voltage V_{cm} are calculated by using Equation (4.13) - Equation (4.15).

2. Step 2 is comprised of two sections. The first section is to find the width of the PMOS load transistor W_{mp} . The equivalent linear resistance of the PMOS load transistor R_D is found by using the following:

$$R_D = \frac{\Delta V}{I_{ss}} \quad (4.17)$$

Once R_D is obtained, we use Equation (4.1) - Equation (4.3) to find W_{mp} . The second section is to find the threshold voltage of the NMOS differential transistor $V_{th,md}$ and the drain voltage V_x of the current source. Applying Equation (4.4) and Equation (4.16), we find $V_{th,md}$ and V_x by using the two linear equations, two unknowns method.

3. After finding $V_{th,md}$ and V_x , we apply the Equation (4.9) to find the optimum width W_{md} of the NMOS differential transistor. V_{gs} in Equation (4.9) is determined from:

$$V_{gs} = V_H - V_x \quad (4.18)$$

When calculating W_{md} , the NMOS differential transistor is assumed to be completely on and has a logic high voltage at its gate terminal.

4. Calculate the total propagation delay D_{MCML} and power consumption P_{MCML} of the MCML gate by using Equation (4.12) and Equation (2.3).

4.6 Width and length of NMOS current source

The amount of current is tightly coupled to the size of NMOS current source. Once we know the amount of current required from the current source, the width W_{mn} and the length L_{mn} of the NMOS current source can be found. First, set the channel length of NMOS current source to 1.5 μm to have high output impedance of the current source to ensure the robustness of MCML. Next, sweep the channel width of the NMOS current source with the control voltage $V_{ren} = 0.89\text{ V}$. V_{ren} is chosen to be 0.89 V to keep NMOS

current source operating in saturation region. Two major issues of sizing the NMOS transistor are the silicon area and robustness. The NMOS current source only provides the DC current and has no voltage transition. Parasitic capacitances of the current source do not influence the speed of MCML. However, a capacitive-loaded current source has negative impedance and causes the MCML gate to be unstable. Increasing the output impedance of the current source helps to resolve the effect of negative impedance. One of the strategies is to increase the output impedance of the current source by increasing the channel length of the NMOS current source. However, the channel width of the NMOS current source has to increase as much as the length to keep the same amount of current. The typical channel length of the NMOS current source is about $1.5 \mu\text{m}$ and output impedance of the current source is equal to or above $3 \text{ k}\Omega$ [28]. An example of sweeping W_{mn} to find the required $I_{ss} = 125 \mu\text{A}$ is shown in Figure 4.5. For this example, $V_{ren} = 0.89 \text{ V}$ and $L_{mn} = 1.5 \mu\text{m}$.

Figure 4.5: Current versus width of NMOS current source

From this figure, it is observed that current I_{ss} is linearly proportional to the width of the NMOS current source W_{mn} . I_{ss} is 125 μA when W_{mn} is 5.75 μm . A plot of output impedance of the current source versus W_{mn} is shown in Figure 4.6 below:

Figure 4.6: Output impedance vs. width of NMOS current source

Output impedance of the current source is 4.75 $\text{k}\Omega$ for W_{mn} equal to 5.75 μm . It meets our expectation that output impedance of the current source is above 3 $\text{k}\Omega$ to ensure robustness of the MCML gate.

4.7 Control voltage of NMOS current source

The voltage level of V_{ren} is chosen to keep the NMOS current source in saturation mode. The typical value of V_{ren} is chosen between 0.75 V and 1.0 V. V_{ren} is directly proportional to the amount of current generated by the current source.

4.8 Simulation results based on procedure

The theoretical results from the procedure have been validated by comparison with Spectre simulation results. The testbench is a nine-stage MCML ring-oscillator as shown in Figure 4.1. The supply voltage V_{dd} is set to 1.8 V. The transistor aspect ratio and other parameters in the simulator are the output results from the procedure. I_{ss} is varied from 80 μA to 500 μA . The output swing ΔV is 300 mV. Discrepancies between simulated results and theoretical results are less than 7.0%. A plot of I_{ss} from 80 μA to 500 μA with output voltage $\Delta V=300$ mV is shown in Figure 4.7.

Figure 4.7: Theoretical and simulated delay for voltage swing = 300 mV

Increasing I_{ss} decreases the propagation delay of the MCML inverter in Figure 4.7. The percentage of discrepancy between theoretical and simulated delay is about 2% when I_{ss} is between 80 μA and 150 μA . The percentage discrepancy rises to 6.6% when I_{ss} increases from 150 μA to 500 μA . One of the discrepancy sources are the inaccurate par-

asitic capacitance model. More sources of discrepancies are presented at the end of the chapter. All the theoretical results in Figure 4.7 are higher than simulated results. Another plot of I_{ss} from 80 μA to 500 μA with $\Delta V=500\text{ mV}$ is shown in Figure 4.8 below:

Figure 4.8: Theoretical and simulated delay for voltage swing = 500 mV

In Figure 4.8, the percentage of discrepancy between the theoretical and simulated delay is about 3% when I_{ss} is between 80 μA and 150 μA . The percentage of discrepancy rises to 6.7% when I_{ss} increases from 150 μA to 500 μA .

4.9 Two-level MCML delay estimation

The delay estimation procedure of single-level MCML is extended to two-level MCML. The symbols of the two-level MCML delay estimation procedure refer to Figure 4.9 below:

Figure 4.9: Schematic diagram of MCML NAND gate

The extra steps in the two-level MCML delay estimation procedure are illustrated. An MCML NAND gate is employed as an example of this procedure. The differences between the two-level and single-level delay estimation procedures are to find the saturation drain voltage of the first level NMOS differential pair $V_{DSAT,md1}$ and the drain voltage of the second level NMOS differential pair V_{x-pi} . The equation of $V_{DSAT,md1}$ is denoted as follows [20]:

$$V_{DSAT,md1} \approx I\zeta_c = \frac{Iv_{sat}}{\mu_n} \quad (4.19)$$

where L is the channel length of the first level NMOS differential transistors. ζ_c is the critical value of the electrical field along the channel. v_{sat} is the saturation velocity for the electrons and holes. μ_n is the electron mobility. V_{x-pi} can be obtained from the following equation:

$$V_{x-pi} = V_{DSAT,md1} + V_x \quad (4.20)$$

Here is a flow chart for the proposed delay estimation procedure for two-level MCML gates.

Figure 4.10: Flow chart of proposed delay estimation procedure

The following steps summarize the delay estimation procedure of two-level MCML gates.

1. Select a reasonable output voltage swing ΔV and current I_{ss} . Upper limit swing V_H , lower limit swing V_L and common-mode voltage V_{cm} are calculated by using Equation (4.13) - Equation (4.15).
2. Step 2 consists of two sections. The first section is to find the width of the PMOS load transistor W_{mp} . The equivalent linear resistance of the PMOS load transistor, R_D , is found by using the following:

$$R_D = \Delta V / I_{ss} \quad (4.21)$$

Once R_D is obtained, we use Equation (4.1) - Equation (4.3) to calculate W_{mp} . The second section is to find the threshold voltage of the first-level NMOS differential transistor $V_{th,md1}$ and drain voltage of the current source V_x . Applying Equation (4.4) and Equation (4.16), we find $V_{th,md1}$ and V_x by using the two linear equations, two unknowns method.

3. Step three is comprised of two sections. In the first section, we apply Equation (4.9) to calculate the optimum width of the first-level NMOS differential transistor W_{md1} . $V_{gs,md1}$ in Equation (4.9) is denoted by:

$$V_{gs,md1} = V_H - V_x \quad (4.22)$$

When we calculate W_{md1} , the NMOS differential transistor is assumed to be completely on and has a logic high voltage at its gate terminal. In the second section, the saturation drain voltage of the first-level NMOS differential transistor is calculated using Equation (4.19).

4. Calculate V_{x-pi} by using Equation (4.20).

5. The threshold voltage of the second-level NMOS differential transistor $V_{th,md2}$ is calculated using Equation (4.4)
6. Apply Equation (4.9) to calculate the optimum width of the second level NMOS differential transistor W_{md2} . $V_{gs,md2}$ in Equation (4.9) is denoted by:

$$V_{gs,md2} = V_H - V_{x-pi} \quad (4.23)$$

When we calculate W_{md2} , the NMOS differential transistor is assumed to be completely on and has a logic high voltage at its gate terminal.

7. Calculate the total propagation delay D_{MCML} and power P_{MCML} of the MCML gate using Equation (4.12) and Equation (2.3).

The following plot shows a sweep of I_{ss} from 180 μA to 500 μA with $\Delta V=420$ mV.

Figure 4.11: Theoretical and simulated delay for voltage swing =420 mV

In Figure 4.11, the percentage discrepancy between the theoretical and simulated delay for $\Delta V=420$ mV is below 18.0%.

4.10 Example of delay estimation in combinational logic

An example of delay estimation in combinational logic is presented in this section. One bit full adder circuit is used as a test vehicle. The theoretical and simulated propagation delays of the critical path are reported. The block diagram of the one-bit full adder (adder's critical path is represented as a dashed arrow) is shown in Figure 4.12 below:

Figure 4.12: Block diagram of the one-bit full adder

The block diagram of the one-bit full adder has three inputs a , b and cin and two outputs, sum and $cout$. This combinational logic contains heterogeneous logic gates which have more than one fan out and extra output capacitances. The calculation of $C_{L,pos}$ and $C_{L,neg}$ in the delay estimation procedure is modified to include the extra capacitances. The delay of each logic gate along the critical path is calculated. The following table shows the theoretical and simulated propagation delay of the critical path.

TABLE 4.8: Theoretical and simulated propagation delay

	<i>Theoretical</i>	<i>Simulated</i>
Propagation delay (ps)	108.6	124.4

The percentage of discrepancy between theoretical and simulated result is 12.67%.

4.11 Concluding Remarks

The delay estimation procedure has been addressed in this chapter. The percentage discrepancy between theoretical and simulated results is less than 18%. The following sources for the discrepancy have been identified:

- The equation of parasitic capacitance is an approximated model. Miller effect is not considered in the delay estimation procedure. A topic of the future work is to incorporate with the Miller effect to the delay estimation procedure.
- Most of the process parameter values used in the equations come from transistor model files. These parameter values are extracted by using a square-wave input signal to the logic gate. However, ramp signal inputs are used in the ring-oscillator test-bench.
- The equivalent resistance model incurs high discrepancy between theoretical and simulated results when the width of the PMOS is close to its minimum channel width 0.60 μm .
- V_x and V_{x-pi} are assumed not to fluctuate when the MCML gate operating at high-speed.

Design of MCML C-element

This chapter illustrates the novel design and delay estimation of an MCML C-element. A comparison of two topologies for the C-element in MCML and conventional CMOS logic is presented and all the results are recorded. The MCML C-element dissipates up to four times less energy compared to a conventional CMOS C-element with the same throughput. Delay estimation of the first version MCML C-element is illustrated. The words “MCML C-element” are used to represent the control circuit of an asynchronous MCML pipelined circuit.

5.1 Design of MCML C-element

The MCML C-element receives handshaking signals from the adjacent stage and regulates the data flow by controlling the latches in either opaque or transparent states. The operation and structure of a conventional CMOS C-element are mentioned in Chapter 3. MCML C-element design is derived from the conventional CMOS C-element shown in Figure 3.1. Two topologies for the MCML C-elements are proposed. Their simulation results have been compared and analyzed. The performance of the proposed first version MCML C-element is better than that of the proposed second version MCML C-element.

5.1.1 Proposed first version of MCML C-element

The schematic diagram of the proposed first version MCML C-element is shown in Figure 5.1 below:

Figure 5.1: Schematic diagram of first version of MCML C-element

The architecture of the MCML control circuit is originally based on the conventional pull-up and pull-down C-element circuit [22]. The MCML control circuit consists of a constant current source, mn , controlled by a reference voltage, V_{ren} . mp are PMOS transistors used as active loads biased by reference voltage, V_{rep} . ma and mb are the differential pair transistors stacked on top of each other to form an AND structure. The two my devices are cross-coupled transistors and form a latch structure. Four mc transistors,

below my transistors, are in parallel with each other to form an OR structure. When both inputs are the same, one side of the stacked differential pair transistors (ma , mb) is switched on and the other side is switched off, creating a path from one of the output nodes to V_{ss} . One of the latch branches (my , mc) is completely active and preserves the output value. When the input signals are different, both stacked differential pair (ma , mb) branches are inactive because of the AND structure. The only conducting branches are the two latch branches (my , mc) because of the OR structure (four mc). The output value is unchanged and preserves its previous value with the latch structure, cross-coupled transistors my .

5.1.2 Delay estimation of first version MCML C-element

The proposed first version MCML C-element is a two-level MCML gate. Delay estimation of the first version MCML C-element can be done by using the two-level MCML delay estimation procedure in Chapter 4. The MCML C-element is assumed to operate in the worst-case scenario and only one path from the output node to V_{ss} is active.

Inputs a and b have different states ($a = 1$ and $b = 0$). The latch transistors are active and preserve the previous output values ($out = 1$ and $\overline{out} = 0$). The current path from the output node to V_{ss} is annotated in Figure 5.2 below:

Figure 5.2: Current path in first version of MCML C-element

The current path from the output node to V_{ss} passes through two active transistors which are latch transistor my and control transistor mc . Transistors with “\” symbol are shut off. At the beginning of the delay estimation procedure, two input parameters, I_{ss} and ΔV , are chosen as $110 \mu A$ and $300 mV$ respectively. The optimum transistor parameters for the proposed first version MCML C-element are generated from the two-level MCML delay

estimation procedure. As mentioned in Chapter 4, the transistor widths in the NMOS differential pair are chosen to be all the same for matching and layout reasons. If the transistor widths of the first level and second level are similar, it is better to set them to the same value because of good matching and reduction of layout complexity. The following table shows the theoretical and simulated propagation delay of the critical path.

TABLE 5.1: Theoretical and simulated propagation delay

	<i>Theoretical</i>	<i>Simulated</i>
Propagation delay (ps)	71.6	77.5

The percentage discrepancy between the theoretical and simulated results is 7.63%. The sources of the discrepancy are discussed in the concluding remarks of Chapter 4.

fighters against the active stacked input differential branch. This race conditions, results in longer response time and does not allow any power savings compared with the conventional CMOS C-element in the multi-GHz range.

5.1.4 Simulation results and discussion

This section reports the simulation results of the C-element in MCML and conventional CMOS logic. All simulations are performed with the Spectre simulator in the Cadence Design Environment. All the transistor sizes in the MCML and conventional CMOS logic gates are carefully optimized to achieve multi-GHz operating frequency. Simulation data tables of C-elements are given to compare their power dissipation, performance and layout area in MCML and conventional CMOS logic styles. Power results of conventional CMOS C-element include dynamic power and leakage power. The constant current source is the major source of MCML C-element power dissipation including the dynamic power and leakage power. In these simulations, the signal voltage swing is about 300 mV.

The following simulation compares the power dissipation, performance and layout area of the first version MCML C-element, second version MCML C-element and conven-

tional CMOS C-element. The testbench of the MCML and conventional CMOS C-elements is described as follows:

Figure 5.4: Testbench of MCML C-element

A four-stage FIFO architecture in Figure 5.4 is used. Handshaking signals, Req_{in} and Ack_{out} , are connected and inverted by flipping the polarity of the Req_{in} differential signals. Similarly, Req_{out} and Ack_{in} are also connected together. A FIFO with two feedback handshaking signals forms an oscillator which is self-excited and operates without any external input. Their power dissipations at 1.9 GHz operating frequency are recorded and shown in Table 5.2.

TABLE 5.2: Power of MCML and CMOS C-element at 1.9GHz

	MCML C1	MCML C2	CMOS
Power(μ W)	51.29	134.70	205.74

In Table 5.2, power consumption of the first version MCML C-element, MCML C1, is four times less than that of the conventional CMOS C-element at 1.9 GHz operating frequency. Also the power consumption of the second version MCML C-element, MCML C2, is about twice that of MCML C1. It indicates that *mc* transistors in the first version of

the MCML C-element are critical design components to improve the performance of the MCML C-element. The operating frequencies of MCML and conventional CMOS C-elements at 205.74 μ W power dissipation are recorded and shown in Table 5.3.

TABLE 5.3: Frequency of MCML and CMOS C-element at 205.74 μ W

	MCML C1	MCML C2	CMOS
Frequency(GHz)	4.85	2.58	1.90

The frequency of the first version MCML C-element is two times faster than that of the second version MCML C-element and conventional CMOS C-element at the same power level in Table 5.3.

Figure 5.5: Frequency versus Power in MCML and CMOS C-elements

A plot of MCML and CMOS C-element performance is shown in Figure 5.5. The circle dot is the power of the conventional CMOS C-element operating at 1.9 GHz. The graph with "X" markers is the power of first version MCML C-element. The square dot repre-

sents the power of the second version MCML C-element. This graph is plotted by manipulating the bias voltages of the current source and active load and keeping the output voltage swing at 300 mV. The first version MCML C-element can operate up to 5 GHz. However, the conventional CMOS C-element can only run up to 1.9 GHz. The conventional CMOS C-element has no hope of matching the performance of the MCML C-element. Layout areas of both versions of the MCML C-elements and conventional CMOS C-element are recorded and shown in Table 5.4.

TABLE 5.4: Layout areas of MCML and CMOS C-elements

	MCML C1	MCML C2	CMOS
Area(μm^2)	173.63	141.19	124.20

In Table 5.4, layout area overhead percentages of the first version MCML C-element over the second version MCML C-element and conventional CMOS C-element are only 20% and 30% respectively. The area penalty of first version MCML C-element is caused by the M_c transistors and their extra interconnecting wires. However, the layout area overhead percentage of the first version MCML C-element is insignificant because its power consumption and performance are far better than the other two.

5.2 Concluding remarks

This chapter has proposed a low-power, high-speed implementation of an MCML C-element and estimates its delay. It has also detailed the design and optimization of an MCML C-element. Based on the simulation results, the MCML C-element implemented in a standard 0.18 μm CMOS technology demonstrates an operating frequency of 5 GHz and dissipates 0.22 mW. The frequency of the first version MCML C-element is twice as fast as that of the second version MCML C-element and conventional CMOS C-element at the same power level.

Design of MCML Double-Edge Triggered Flip-Flop

This chapter presents the design of an MCML Double-Edge-Triggered Flip-Flop (DETFF). A comparison of two topologies for the DETFFs in MCML and the conventional CMOS DETFF is presented and all results are recorded. The MCML DETFFs dissipates up to two times less energy compared to the conventional CMOS DETFF with the same throughput. The words “MCML DETFF” are used to represent the latches of an asynchronous MCML pipelined circuit.

6.1 Design of MCML DETFF

Latches and flip-flops are the core circuits required to form high-performance microprocessors. Most of the latches and flip-flops are utilized as storage elements in pipelined logic, such as a pipelined arithmetic-logic-unit (ALU) in high-speed low-power applications. Unlike traditional latches and flip-flops, a DETFF samples the data at both the rising and falling edges of the clock signal. It is very desirable to use both rising and falling edges of the clock signal in high-speed applications because the throughput of the DETFF circuit is twice that of conventional single-edge flip-flop circuits. MCML DETFF

is the storage element in our asynchronous MCML FIFO circuit. DETFF samples the input data at both the rising and the falling edges of the clock signal. Figure 6.1 illustrates the block diagram of the DETFF [23].

Figure 6.1: Block diagram of the DETFF

The DETFF incorporates two opposite polarity, level sensitive latches and a multiplexer. The solid line and dash line represent the clock signal and data path respectively. Latches labelled $D1$ and $D2$ operate in either transparent or opaque mode in response to the voltage level of the clock signal. The multiplexer labelled Mux is described by the Boolean function $out = d1\bar{e} + d2e$. When the clock signal CLK is high, the latch $D1$ is transparent. Data stored in latch $D2$ is multiplexed to the global output. When the clock signal CLK is low, the latch $D2$ is transparent and Mux multiplexes the stored value in $D1$ to the global output. The schematic diagram of a conventional CMOS DETFF is shown in Figure 6.2 below:

Figure 6.2: Schematic diagram of conventional CMOS DETFF

The implementation of MCML DETFFs is based on the conventional CMOS DETFF. The schematic diagram of a proposed first version MCML DETFF is shown in Figure 6.3 below:

The MCML DETFF has the same architecture as Figure 6.1 and consists of two opposite polarity level sensitive MCML latches and an MCML multiplexer. The proposed first version MCML DETFF is different from the conventional MCML DETFF because the MCML latches and MCML multiplexer connect to the common input clock differential pair transistors, *mck* which turn the latches in either transparent or capture mode and multiplexes the data stored in one of the latches to the global output. Advantages of using the same input clock differential pair are the reduction of the input clock capacitance load, the reduction of layout area and routing complexity.

6.1.2 Proposed second version of MCML DETFF

The schematic diagram of proposed second version MCML DETFF is shown in Figure 6.4 below:

Figure 6.4: Schematic diagram of second version MCML DETFF

The proposed second version MCML DETFF consists of two conventional MCML latches and a conventional MCML multiplexer. Unlike the first version MCML DETFF, the second version DETFF has three separate input clock differential pair transistors, mck , governing the MCML latches and MCML multiplexer. Extra routing complexity and a larger drive strength clock buffer are required in the proposed second version MCML DETFF. More energy is consumed when the second version MCML DETFF operates at the same frequency as the first version MCML DETFF.

6.2 Simulation results and discussion

This section reports the simulation results of DETFFs in MCML and conventional CMOS logic. All simulations are performed using the Spectre simulator in the Cadence Design Environment. All the transistor sizes in MCML and conventional CMOS Logic gates are carefully optimized to achieve multi-GHz operating frequency. Simulation data tables of DETFFs are given to compare their power dissipation, performance and layout area in MCML and conventional CMOS logic styles. Power results of the conventional CMOS DETFF include dynamic power and leakage power. The constant current source is the major source of MCML DETFFs power dissipation including the dynamic power and leakage power. In these simulations, the signal voltage swing is about 400 mV.

The following simulation is used to compare the power dissipation, performance and layout area of first version MCML DETFF, second version MCML DETFF and conventional CMOS DETFF. The testbench of MCML DETFFs and conventional CMOS DETFF is shown in Figure 6.5 below:

Figure 6.5: Testbench of DETFFs

The DETFF testbench consists of a chain of cascaded DETFFs and a clock buffer. Clock signal, *clk*, is indicated by solid lines. The dashed lines with arrows show the direction of data flow. The output of the last stage DETFF is connected back to the input of the first

stage DETFF. A chain of cascaded DETFF with feedback data path forms a shift register with rotation. In this testbench, the clock duty-cycle is 50% and the clock slope of an ideal signal is 10% of the clock pulse width. Power results of the DETFFs include the clock power and data power. Frequencies of DETFFs are the maximum clock frequency that the DETFFs can sample and hold the data correctly without any loss of the data signal. Their power dissipations at 2.1 GHz throughput are recorded and shown in Table 6.1.

TABLE 6.1: Power of MCML and conventional CMOS DETFFs at 2.1GHz

	MCML DET1	MCML DET2	CMOS
Power (μ W)	226.08	253.44	403.56

In Table 6.1, power dissipation of conventional CMOS DETFF is almost two times larger than the first version MCML DETFF. The power dissipations of the first version MCML DETFF is slightly smaller than that of the second version MCML DETFF. The first version MCML DETFF with common input clock differential pair transistor has reduced input clock capacitance. A smaller drive strength clock buffer is needed and less power consumption is reported in the first version MCML DETFF. The frequencies of MCML and conventional CMOS DETFFs at 0.40 mW power dissipation are recorded and shown in Table 6.2.

TABLE 6.2: Frequency of MCML and CMOS DETFFs at 0.40 mW

	MCML DET1	MCML DET2	CMOS
Frequency (GHz)	6.67	6.67	2.09

Frequencies of the first version and second version MCML DETFFs are three times faster than that of the conventional CMOS DETFF at the same power level in Table 6.2. MCML DETFFs are more energy efficient than the conventional CMOS DETFF at multi-GHz operating frequencies. Layout areas of both MCML DETFFs and the conventional CMOS DETFF are shown in Table 6.3.

TABLE 6.3: Layout areas of MCML and CMOS DETFFs

	MCML DET1	MCML DET2	CMOS
Area (μm^2)	369.29	387.75	338.00

In Table 6.3, the second version of MCML DETFF has the largest layout area due to the overhead of separate input clock differential pair transistors. Also, layout area overhead percentage of the first and second version MCML DETFFs over conventional CMOS DETFF are about 10%. This is acceptable since the power consumption and performance of MCML DETFFs are far better than that of the conventional CMOS DETFF.

Design of Asynchronous MCML Pipelined Circuits

This chapter illustrates the design of asynchronous MCML pipelined circuits. An asynchronous MCML FIFO is presented first. A comparison of two topologies for the MCML FIFO and a conventional CMOS FIFO is presented. Then, asynchronous MCML pipelined adders are designed. A comparison of schematic and post layout simulation results for the MCML FIFOs and MCML pipelined adders is included.

7.1 Asynchronous MCML pipelined circuits

Asynchronous MCML pipelined circuits based on micropipelines are proposed and implemented. The block diagram shown in Figure 7.1 illustrates the architecture of a four-stage pipelined circuit with double-edge-triggered flip-flops (DETFFs) as storage elements.

Figure 7.1: Block diagram of the asynchronous MCML four-stage pipelined circuit

The structure of an asynchronous MCML pipelined circuit is simpler than that of the original micropipelines. An asynchronous MCML pipelined circuit is composed of C-element, DETFFs, buffers and combinational logic. The DETFFs represent the registers in Figure 7.1. In asynchronous MCML pipelined circuits, data is implemented with single-rail encoding. Adjacent stages communicate through a two-phase, bundled-data signaling protocol. However, the asynchronous MCML pipelined circuits operate at worst-case performance because the throughput of asynchronous MCML pipelined circuits is restricted by the maximum latency of the combinational logic. The asynchronous MCML FIFO circuit is modified from Figure 7.1 by removing the buffer and the logic between the stages.

7.2 Simulation results of MCML and CMOS FIFOs

This section reports the comparison of power dissipation and performance of asynchronous FIFO circuits in MCML and conventional CMOS logic topologies. Asynchronous FIFO circuits in MCML and conventional CMOS logic are simulated. All results in this section are based on schematic simulation. Signal voltage swing is about 300 mV. The first FIFO circuit uses the first version MCML C-elements and MCML DETFFs from Chapter 5 and 6 respectively. The second FIFO circuit includes the second version MCML C-elements and MCML DETFFs from Chapter 5 and 6 respectively. The last FIFO circuit uses only conventional CMOS C-elements and DETFFs. Power results of the FIFO circuit include four C-elements and four DETFFs. The testbench of the MCML and conventional CMOS FIFOs is the same structure as the C-element testbench in Figure 5.4. Their power dissipations at 1.9 GHz throughput are recorded and shown in Table 7.1.

TABLE 7.1: Power of MCML and conventional CMOS FIFOs at 1.9GHz

	MCML FIFO1	MCML FIFO2	CMOS
Power (mW)	0.86	1.58	2.23

As listed in Table 7.1, MCML FIFO1 dissipates two times less power than the MCML FIFO2 and about three times less power than the conventional CMOS FIFO at the same throughput. The conventional CMOS FIFO dissipates 40% more power than the MCML FIFO2. As a result, the asynchronous FIFO in MCML topology is more power efficient than that of the conventional CMOS topology at multi-GHz operating frequencies. The maximum operating frequencies and power dissipations of MCML and conventional CMOS FIFO are recorded and shown in Table 7.2.

TABLE 7.2: Maximum operating frequencies and power dissipations of MCML and CMOS FIFOs

	MCML FIFO1	MCML FIFO2	CMOS
Maximum operating frequency (GHz)	5	2.10	1.9
Power (mW)	1.84	2.23	2.23

In Table 7.2, MCML FIFO1 dissipates only 1.84 mW power and runs at 5 GHz. MCML FIFO2 and conventional CMOS FIFO consume 20% more power but their operating frequency is only half of the MCML FIFO1. Layout areas of both versions of the MCML FIFO and conventional CMOS FIFO are recorded and shown in Table 7.3.

TABLE 7.3: Layout areas of MCML and CMOS FIFOs

	MCML FIFO1	MCML FIFO2	CMOS
Area (μm^2)	2606.00	2538.92	2218.56

In Table 7.3, layout area overhead percentages of MCML FIFO1 over MCML FIFO2 and conventional CMOS FIFO are only 3% and 15% respectively.

7.3 Simulation results of MCML FIFOs with reset circuit

Two version of four-stage MCML FIFO layouts are presented. The first version MCML FIFO layouts does not have dummy elements, but the second version does. A comparison of their schematic simulation results and their post layout simulation results are reported. The block diagram of first and second version MCML FIFOs with reset circuit is shown in Figure 7.2 below:

Figure 7.2: Block diagram of MCML FIFO with reset circuit

In Figure 7.2, a four-stage MCML FIFO with two feedback handshaking signals is similar to an oscillator which self-oscillates in an unstable state. Multiplexers are the reset circuits of the MCML FIFO oscillator. The MCML FIFO oscillator is reset when a pulse signal is applied to the control signal line. When the control signal is logic high, the four-stage MCML FIFO ring oscillator is inactive. All handshaking signals are logic high because the multiplexer multiplexes the logic high signal to the input of the MCML C-element. The MCML C-element outputs logic high signal. When the control signal is logic low,

MCML FIFO oscillator is in an unstable state and oscillates. The following two layouts are based on the block diagram of the MCML FIFO in Figure 7.2. The layout of the first version of the MCML FIFO oscillator is shown in Figure 7.3 below:

Figure 7.3: Layout of first version MCML FIFO oscillator

The layout area of the first version four-stage asynchronous MCML FIFO oscillator with reset circuit is confined to $85 \mu\text{m} \times 35 \mu\text{m}$. No dummy elements are used. Several layout techniques are utilized to ensure the good matching and easy routing in MCML logic gate layout. Multi-finger and interdigitation are used to reduce the effect of mismatch and manufacturing defects. The second version of the MCML FIFO oscillator is shown in Figure 7.4 below:

Figure 7.4: Layout of second version MCML FIFO oscillator

The layout area of the second version four-stage MCML FIFO oscillator with reset circuit is confined to $123.5 \mu\text{m} \times 62 \mu\text{m}$. The layout area of the second version MCML FIFO oscillator is larger than that of the first version MCML FIFO oscillator because the second version MCML FIFO oscillator has dummy elements and extra spacing between each stage. The dummy elements and extra spacing incur additional parasitic capacitances and longer interconnect wires in the second version MCML FIFO oscillator. The performance of the first version MCML FIFO oscillator is better than that of the second version MCML FIFO oscillator. The plot of the first version and second version MCML FIFO oscillator's performance is shown in Figure 7.5 below:

Figure 7.5: Maximum frequency vs. Power in MCML FIFO oscillators

A plot of frequency versus power in the first and second version of the MCML FIFO oscillator layouts is shown in Figure 7.5. Control voltages of the current source and PMOS load transistor are adjusted to give the oscillation frequency and same voltage swing. The plot is categorized into two groups. The first group is solid lines to represent the schematic simulation results of the first and second versions MCML FIFO oscillators. The second group is dashed lines to represent the post layout simulation results of first and second versions MCML FIFO oscillator. This graph is plotted by manipulating the control voltages of the current source and PMOS load transistor to keep the output voltage swing at 450 mV. All plots increase exponentially and saturate at the high frequency range and high power range because of nonlinearity in the PMOS load resistance. Increasing I_{ss} increases the frequency of MCML gates. ΔV is kept constant and the PMOS load resistance R_D must decrease according to Equation (3.16). Reducing the control voltage of the PMOS load transistor V_{rep} decreases R_D . However, the PMOS load resistance is nonlinear and saturates when V_{rep} is close to 0 V. A plot of PMOS load resistance versus control voltage of the PMOS load transistor with $W_{mp} = 0.6 \mu\text{m}$ and $L_{mp} = 0.18 \mu\text{m}$ is shown in Figure 7.6 below:

Figure 7.6: PMOS load resistance versus the control voltage

In Figure 7.6, the plot is obtained by using Equation (4.1). R_D increases exponentially when V_{rep} sweeps from -0.6 V to 1.2 V. In a mathematical way, R_D curve is saturated and exhibits nonlinear behaviour when V_{rep} decreases. It verifies our explanation that all plots in Figure 7.5 increase exponentially and saturate at the high frequency range and high power range because of nonlinearity in the PMOS load resistance. Furthermore, the first version MCML FIFO oscillator can run up to 5 GHz and 4 GHz in post layout simulation and schematic simulation respectively. A twenty percentage difference exists between the post layout simulation result and schematic simulation result. It is reasonable because the typical performance penalty of post layout simulation is about twenty percentage. When post layout simulation and schematic simulation results are both 4 GHz, the MCML FIFO oscillator dissipates 3.8 mW and 2.8 mW in post layout simulation and schematic simulation respectively. A thirty-five percentage difference exists between post layout simulation result and schematic simulation result. The MCML FIFO oscillator in post layout simulation consumes more power than the MCML FIFO oscillator in schematic simulation due to the parasitic capacitances of interconnect wires. Furthermore, the second version MCML FIFO oscillator can run up to 4.6 GHz and 3.4 GHz in post layout simulation and schematic simulation respectively. A twenty-eight percentage difference exists between the post layout simulation result and schematic simulation result. More parasitic capacitances are present in the second version MCML FIFO because of the dummy elements and longer interconnect wires. When post layout simulation and schematic simulation results are both 3.35 GHz, the MCML FIFO oscillator dissipates 3.48 mW and 2.46 mW in post layout simulation and schematic simulation respectively. A forty-two percentage difference exists between the post layout simulation result and schematic simulation result.

7.4 Asynchronous MCML pipelined adder

Asynchronous MCML pipelined 4-bit and 8-bit Brent-Kung adders are designed and implemented. The structure and algorithm of Brent-Kung adder are well-known [20, 27]. Main goal of asynchronous MCML adder implementation is to verify the performance and feasibility of asynchronous MCML pipelined circuit. Their simulation results are reported in this section. Since the adders are pipelined into several stages, their latency is significantly long. The focus of the simulated result is the throughput of the adders. Test data bundled with handshaking signals are applied to the adders. Frequency of input handshaking request signal increases to the speed that the adder can produce the correct results. The simulated throughput of the adder is the maximum speed of the adder. The block diagram of an asynchronous MCML pipelined 4-bit Brent-Kung adder is shown below in Figure 7.7 [20].

Figure 7.7: Asynchronous MCML pipelined 4-bit Brent-Kung adder

The post layout simulation and schematic simulation results are shown in Table 7.4.

TABLE 7.4: Simulation results of MCML 4-bit Brent-Kung adder

	Throughput (GHz)	Power (mW)
Schematic simulation	2.44	14.0
Post layout simulation	2.05	17.6

The block diagram of an asynchronous MCML pipelined 8-bit Brent-Kung adder is shown below in Figure 7.8 [20].

Figure 7.8: Asynchronous MCML pipelined 8-bit Brent-Kung adder

where the diamond and circle symbols are referred to Figure 7.7. The post layout simulation and schematic simulation results are shown below in Table 7.5.

TABLE 7.5: Simulation results of MCML 8-bit Brent-Kung adder

	Throughput (GHz)	Power (mW)
Schematic simulation	1.01	40.37
Post layout simulation	0.45	51.37

There are several important points in Table 7.4 and Table 7.5. Adders in schematic simulation have superior power dissipation and speed over the adders in post layout simulation. Differential signal lines are parallel with each other and incur significant cross-coupling capacitance. Capacitances of interconnect wires have the big impact on the performance of the adder circuit in the deep submicron regime. The future work of the asynchronous MCML pipelined circuits is to focus on new layout strategies, to minimize the length of the interconnect wire and to use different metal layout on interconnect wires. Furthermore, the power dissipation of asynchronous MCML pipelined adder will be reduced significantly if the power-saving mechanism is employed.

Conclusion and Future Work

In this thesis, the concept and design of asynchronous MCML pipelined circuits have been proposed. The reported simulation results meet our initial expectation that the combination of asynchronous circuits and MCML is the perfect candidate for designing high-speed, energy-efficient, and analog-friendly digital circuits. We have also presented a delay estimation technique to assist in designing these circuits. In the delay estimation procedure, the percentage discrepancies in single-level and double-level MCML gate delay estimation are about 7% and 18%, respectively. Two primitive asynchronous MCML gates, the MCML C-element and MCML double-edge triggered flip-flop, are also introduced in the thesis. Based on the schematic simulation, the MCML C-element demonstrates operating frequency of 5 GHz and dissipates 0.22 mW, while the MCML double-edge triggered flip-flop demonstrates operating frequency of 6.7 GHz and dissipates 0.40 mW. The frequency of operation of the MCML C-element is two times higher than that of a conventional CMOS C-element at the same level of power dissipation. The MCML double-edge triggered flip-flop runs three times faster than a conventional CMOS double-edge triggered flip-flop with the same level of power consumption.

Using the MCML C-element gate and double-edge triggered flip-flop, we implemented an asynchronous FIFO and two adder circuits. Based on the extracted post layout simulation, the asynchronous MCML FIFO implemented as a micropipeline structure

demonstrates a throughput of 4 GHz and dissipates 3.65 mW. Our asynchronous MCML implementation of a 4-bit Brent-Kung carry lookahead adder runs at 2 GHz and dissipates 17.6 mW, while its 8-bit version runs at 0.45 GHz and dissipates 51.37 mW. All circuits are implemented in a standard 0.18 μm CMOS technology. The chip layouts have been sent for fabrication through CMC and one of them is currently under test.

As far as the future work is concerned, the delay estimation technique may be extended to develop an automated tool for design and optimization of MCML gates. The implementation of other asynchronous primitives in MCML is also an appealing next step. Currently, we are working on a power-saving mechanism to further reduce the power dissipation of asynchronous MCML pipelined circuits.

Supporting information on delay estimation procedure

A.1 Miller effect

Miller effect has a considerable impact on the gate capacitance and drain capacitance of the MOS transistor. The aim of this section is to illustrate the importance of Miller effect on delay estimation results of Chapter 4. Figure A.1 illustrates the Miller effect on the gate capacitance and drain capacitance of NMOS transistor [19].

Figure A.1: Miller effect on the NMOS transistor

In Figure A.1, the NMOS transistor represents one side of the differential-pair transistors in an MCML gate. C_{eff} is the effective capacitance of the gate-to-drain terminal and is equal to C_{gd} of NMOS transistor. C_{gd} is equivalent to C_{ov} in the delay estimation procedure. Due to the charging and discharging C_{gd} , the capacitance of C_{eff} is twice larger than

that of C_{gd} . If we assume that the gain of differential pair transistor is -1, the Miller effect causes parasitic capacitances $C1$ and $C2$ to be twice larger than C_{eff} . The modified output parasitic capacitances for rising transition and falling transition are shown in table below:

TABLE A.1: List of new output parasitic capacitances

<i>Transition</i>	<i>Transistor</i>	<i>Operation mode</i>	<i>Capacitance</i>	<i>Description</i>
Positive	PMOS (Cell)	Triode	C_{dPMOS}	$\frac{C_{gc}}{2} + C_{ov} + C_{jdb} + \frac{C_{cb}}{2}$
Positive	NMOS (Cell)	Saturation	C_{dNMOS}	$C_{jdb} + 2 \cdot C_{eff}$
Positive	NMOS (Drive)	Off	C_{gNMOS}	$C_{gc} + C_{ov} + 2 \cdot C_{eff}$
Negative	NMOS (Drive)	Triode	C_{gNMOS}	$\frac{C_{gc}}{2} + C_{ov} + C_{jdb} + \frac{C_{cb}}{2}$
Negative	NMOS (Drive)	Off	C_{gNMOS}	$C_{jdb} + 2 \cdot C_{eff}$
Negative	NMOS (Drive)	Saturation	C_{gNMOS}	$\frac{2}{3}C_{gc} + C_{ov} + 2 \cdot C_{eff}$

New output load capacitance is about 43% bigger than old output capacitance. Single-level MCML delay estimation with $I_{ss} = 300 \mu A$ and $\Delta V = 300 mV$ is used as an example to demonstrate the impact of the Miller effect on propagation delay. Theoretical propagation delay are shown in the table below:

TABLE A.2: Calculated propagation delay with and without Miller effect

	<i>With Miller effect</i>	<i>Without Miller effect</i>
Propagation delay (ps)	28.48	19.92

The propagation delay with Miller effect is 43% bigger than the propagation delay without Miller effect. In the future work, it is preferable to incorporate the Miller effect into the delay estimation procedure.

A.2 Discrepancy in PMOS load resistance model

This section is to present the comparison of simulated and theoretical results of equivalent resistance model. The simulated and theoretical results of PMOS load resistance are shown below in Figure A.2. For this example, W_{mp} sweeps from 0.6 μm to 4 μm .

Figure A.2: PMOS load resistance versus width of PMOS load transistor

There are several important points in Figure A.2. Discrepancy between simulated and theoretical results is significant when W_{mp} is below 1 μm . Large discrepancy exists when W_{mp} is close to 0.6 μm . It verifies that the equivalent resistance model has high discrepancy between theoretical and simulated results when W_{mp} is close to its minimum channel width 0.60 μm . Furthermore, the theoretical result is very close to simulated result when W_{mp} is greater than 1 μm .

A.3 Estimation of junction capacitances

Junction capacitances of MOFET are categorized into reverse-biased source-body pn-junction and reverse-biased drain-body pn-junction. These capacitances change dramatically according to the voltage across the junctions [20]. The focus of this section is to find the approximation equation of drain-body pn-junction capacitance that uses in the delay estimation procedure. Drain-body pn-junction capacitance C_{jdb} is comprised of three side-wall junction capacitances and one bottom-plate junction capacitance. An expression of total drain-body pn-junction capacitance is shown below [20]:

$$C_{jdb} = C_j \cdot L_S \cdot W + C_{jSW} \cdot x_j \cdot (2 \cdot L_S + W) \quad (\text{A.1})$$

where C_j is the junction capacitance per unit area. L_S is the length and W is the width of the drain region. C_{jSW} is the side-wall capacitance per unit perimeter. x_j is the junction depth. Equation (A.1) is manipulated to fit into the first order linear equation and is shown below:

$$C_{jdb} = W \cdot (C_j \cdot L_S + C_{jSW} \cdot x_j) + 2 \cdot C_{jSW} \cdot x_j \cdot L_S \quad (\text{A.2})$$

where the term $C_j \cdot L_S + C_{jSW} \cdot x_j$ is the slope. The term $2 \cdot C_{jSW} \cdot x_j \cdot L_S$ represents y-intercept point when $W = 0$. With Cadence spectre simulation, the plots of C_{jdb} versus the width of the PMOS transistor and the NMOS transistor are shown in Figure A.3. In this example, the width of PMOS W_p and the width of NMOS W_n are swept from $0.6 \mu\text{m}$ to $5 \mu\text{m}$.

Figure A.3: Junction capacitance versus width of NMOS / PMOS

In Figure A.3, y-axis and x-axis represent C_{jdb} and width of the PMOS/NMOS respectively. The slopes of these graph are the term $C_j \cdot L_S + C_{jSW} \cdot x_j$ in Equation (A.2). Y-intercept points in these plots are very small. The term $2 \cdot C_{jSW} \cdot x_j \cdot L_S$ in Equation (A.2) is ignored. The approximation equation of drain-body pn-junction capacitance are shown in Equation (A.3) below:

$$C_{jdb} = W \cdot (C_j \cdot L_S + C_{jSW} \cdot x_j) \quad (\text{A.3})$$

Equation (A.3) indicates that C_{jdb} is linearly proportional to the W .

LAYOUTS OF MCML GATES

B.1 MCML gate layouts

The layouts of various MCML gates are presented and are categorized into two groups in this appendix. First group includes the first version of MCML gates found in Chapter 5 - Chapter 7. Second group includes the second version of MCML gates found in Chapters 5 - Chapter 7. The layout areas of the first versions are smaller than these of the second versions because the first version MCML gates have no dummy elements and no extra spacing between the transistor devices. Furthermore, the interconnect wires in the first version MCML gates are shorter than these of the second version MCML gates. The first version MCML gates are faster than the second version MCML gates because of less parasitic capacitances.

B.2 MCML C-element

First version

Second version

Figure B.1: First and second versions of MCML C-elements

B.3 MCML DETFF

First version

Second version

Figure B.2: First and second versions of MCML DETFFs

B.4 MCML AND gate

Figure B.3: First and second versions of MCML AND gates

B.5 MCML OR gate

Figure B.4: First and second versions of MCML OR gates

B.6 MCML XOR gate

First version

Second version

Figure B.5: First and second versions of MCML XOR gates

B.7 MCML MUX gate

Figure B.6: First and second versions of MCML MUX gates

B.8 MCML inverter gate

First version

Second version

Figure B.7: First and second versions of MCML inverter gates

B.9 Layout of tapeout (ICFCUWK1)

Figure B.8: Layout of second tapeout

B.10 Layout of tapeout (ICFCUKTW)

Figure B.9: Layout of first tapeout

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