1

National Library
of Canada

Bibliothèque nationale
du Canada

Canadian Theses Service

Service des thèses canadiennes

Ottawa, Canada
K1A 0N4

NOTICE

The quality of this microform is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Previously copyrighted materials (journal articles, published tests, etc.) are not filmed.

Reproduction in full or in part of this microform is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30.

AVIS

La qualité de cette microforme dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

Les documents qui font déjà l'objet d'un droit d'auteur (articles de revue, tests publiés, etc.) ne sont pas microfilmés.

La reproduction, même partielle, de cette microforme est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30.

MULTI-STAGE SIGMA DELTA MODULATORS

by

Lorenzo L. Longo, B.Sc.(Eng.)

This thesis is submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada

April, 1988

© 1988, Lorenzo L. Longo

Permission has been granted to the National Library of Canada to microfilm this thesis and to lend or sell copies of the film.

The author (copyright owner) has reserved other publication rights, and neither the thesis nor extensive extracts from it may be printed or otherwise reproduced without his/her written permission.

L'autorisation a été accordée à la Bibliothèque nationale du Canada de microfilmer cette thèse et de prêter ou de vendre des exemplaires du film.

L'auteur (titulaire du droit d'auteur) se réserve les autres droits de publication; ni la thèse ni de longs extraits de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation écrite.

ISBN 0-315-46275-2

The undersigned recommend to the Faculty of Graduate Studies
and Research the acceptance of the thesis:

"Multi-Stage Sigma Delta Modulators"

submitted by Lorenzo L. Longo in partial fulfillment of the
requirements for the degree of Master of Engineering.

M. A. Copeland

Prof. M. A. Copeland
Thesis Supervisor

M. A. Copeland

Prof. M. A. Copeland
Chairman,
Department of Electronics

April, 1988

ABSTRACT

The objective of this thesis has been to investigate and develop new architectures for high performance oversampled analog-to-digital converters (ADC) suitable for monolithic realization. Achievement of this goal has required work in the following areas. First, analytical techniques are extended to model the performance sensitivity of multi-stage architectures to nonideal components. This analysis has led to the development of a novel architecture, composed of second and first order sigma delta modulators in cascade, which reduces sampling frequency, opamp gain and capacitor matching requirements.

In the next area, the design considerations for three different oversampled ADC's are compared and contrasted using a discrete-time simulation technique. The simulation results obtained here confirm the predictions made using the analytical models and provide further implementation guidelines.

Finally, the novel two-stage third order noise shaping modulator is implemented in a 1.5 micron CMOS process. Test results are within 1 dB of simulated performance and indicate 13 bits of resolution and linearity using a sampling fre-

quency of only 2.56MHz; performance which compares
favourably with results published to date.

7

ACKNOWLEDGEMENTS

I would like to express my gratitude to my thesis supervisor, Prof. M. A. Copeland, for his support and guidance during the course of this M. Eng. program.

I am indebted to my management at Bell-Northern Research for providing a productive atmosphere for doing cooperative research. In particular, I would like to thank my manager, Dr. P.S. Kasbia, my Dept. head, Mr. G.F. Mein, and my director, Dr. I.L. McWalter, for their support and encouragement during the course of this work. I am also indebted to my previous manager, Mr. T.N. Little, for instituting a workable arrangement for me. I would also like to thank Ed MacRobbie for opamp and comparator design, and Patrick Goulet for his work on the data acquisition system.

Last but by no means least, I wish to thank my wife Donna for her endless patience and support during the course of this work.

The financial support of the Natural Sciences and Engineering Research Council of Canada and Bell-Northern Research is gratefully acknowledged.

TABLE OF CONTENTS

Chapter 1: Introduction	1
1.1 Thesis Motivation and Objective	1
1.2 Background	3
1.3 Oversampling Principle	4
1.4 Thesis Overview	5
Chapter 2: Architecture Alternatives for Sigma Delta Modulators	8
2.1 Introduction	8
2.2 Single-Stage Architectures	9
2.2.1 Sigma Delta Modulator	12
2.2.2 Double Integration Sigma Delta Modulator	17
2.3 Multi-Stage Architectures	22
2.3.1 Two-Stage Second Order Noise Shaping Modulator	22
2.3.2 Three-Stage Third Order Noise Shaping Modulator	30
2.3.3 Two-Stage Third Order Noise Shaping Modulator	33
2.4 SQNR Comparison	36
2.5 Decimation Filter Requirements	38
2.6 Conclusions	41
Chapter 3: Design Considerations for Sigma Delta Modulators	42
3.1 Introduction	42
3.2 Simulation Technique	43
3.3 Coefficient Selection and Capacitor Matching	49
3.3.1 Double Integration Sigma Delta Modulator	50
3.3.2 Three-Stage Third Order Noise Shaping Modulator	56
3.3.3 Two-Stage Third Order Noise Shaping Modulator	65
3.4 Opamp Gain Requirements	69
3.4.1 Double Integration Sigma Delta Modulator	72
3.4.2 Three-Stage Third Order Noise Shaping Modulator	74
3.4.3 Two-Stage Third Order Noise Shaping Modulator	74
3.5 Settling Requirements	76
3.5.1 Double Integration Sigma Delta Modulator	88
3.5.2 Three-Stage Third Order Noise Shaping Modulator	81
3.5.3 Two-Stage Third Order Noise Shaping Modulator	84
3.6 Noise Rejection and Comparator Requirements	84
3.7 Conclusions	88
Chapter 4: Two-Stage Third Order Noise Shaping Modulator	92
4.1 Introduction	92
4.2 Implementation	94
4.3 Switches and Capacitors	100
4.4 Opamp and Comparator	106
4.5 Test Results	111
4.5.1 Test System	112
4.5.2 Measurements	114
4.6 Conclusions	118
Chapter 5: Conclusions	120
5.1 Summary	120

5.2 Recommendations for Future Work	121
References	123

LIST OF ILLUSTRATIONS

Figure 1.	Delta Modulator.	10
Figure 2.	Discrete-time simulation of delta modulator.	11
Figure 3.	Sigma delta modulator: (a) Block diagram. (b) z-domain model.	13
Figure 4.	Discrete-time simulation of sigma delta modulator.	14
Figure 5.	Quantization noise shaping for 1st, 2nd and 3rd order systems.. . . .	16
Figure 6.	Double integration sigma delta modulator: (a) Block diagram. (b) z-domain model.	18
Figure 7.	Discrete-time simulation of DISDM.	20
Figure 8.	z-domain model of two-stage noise shaping modulator.	23
Figure 9.	Discrete-time simulation of two-stage noise shaping modulator	25
Figure 10.	z-domain model of two-stage noise shaping modulator with feedforward.	27
Figure 11.	Discrete-time simulation of two stage noise shaping modulator with feedforward.	29
Figure 12.	z-domain model of three-stage noise shaping modulator.	31
Figure 13.	z-domain model of two-stage third order noise shaping modulator.	34
Figure 14.	SQNR comparison for 1st, 2nd and 3rd order noise shaping.	37
Figure 15.	Frequency response of sinc cubed function for $N=64$	40
Figure 16.	DISDM ideal simulation and analytical calculation.	45
Figure 17.	Three-stage third order noise shaping modulator ideal simulation and analytical calculation.	46
Figure 18.	Two-stage third order noise shaping modulator ideal simulation and analytical calculation.	47
Figure 19.	DISDM circuit diagram.	51
Figure 20.	Effect of opamp saturation on DISDM performance, varying parameter α	53
Figure 21.	Effect of coefficient G_{lfb} variation on DISDM performance.	55
Figure 22.	Three-stage third order noise shaping modulator circuit diagram.	57
Figure 23.	Effect of opamp saturation on three-stage third order noise shaping modulator performance.	59
Figure 24.	Effect of coefficient G_{lfb} variation on three-stage third order noise shaping modulator performance.	61
Figure 25.	Effect of coefficient G_2 variation on three-stage third order noise shaping modulator performance.	62
Figure 26.	Effect of coefficient G_{2ff} variation on three-	

	stage third order noise shaping modulator performance.	63
Figure 27.	Effect of coefficient G_{2fb} variation on three-stage third order noise shaping modulator performance.	64
Figure 28.	Two-stage third order noise shaping modulator circuit diagram.	66
Figure 29.	Effect of overload and opamp saturation on two-stage third order noise shaping modulator performance, varying α	68
Figure 30.	Effect of coefficient G_{1fb} variation on two-stage third order noise shaping modulator performance.	70
Figure 31.	Switched-capacitor integrator using an opamp with finite open-loop DC gain A_o	72
Figure 32.	Effect of finite opamp DC gain on DISDM performance.	73
Figure 33.	Effect of finite opamp DC gain on three-stage third order noise shaping modulator performance.	75
Figure 34.	Effect of finite opamp DC gain on two-stage third order noise shaping modulator performance.	77
Figure 35.	Effect of linear settling error on DISDM performance.	79
Figure 36.	Effect of nonlinear settling error on DISDM performance.	80
Figure 37.	Effect of linear settling error on three-stage converter performance.	82
Figure 38.	Effect of nonlinear settling error on three-stage converter performance.	83
Figure 39.	Effect of linear settling error on two-stage converter performance.	85
Figure 40.	Effect of nonlinear settling error on two-stage converter performance.	86
Figure 41.	Effect of comparator resolution on DISDM performance.	89
Figure 42.	Effect of comparator resolution on three-stage converter performance.	90
Figure 43.	Effect of comparator resolution on two-stage converter performance.	91
Figure 44.	Block diagram of two-stage modulator.	95
Figure 45.	Circuit diagram of two-stage modulator.	96
Figure 46.	Circuit diagram of one bit DAC in feedback loop.	98
Figure 47.	Timing diagram for two-stage modulator.	99
Figure 48.	Small-signal on resistance for a CMOS transmission gate.	102
Figure 49.	Switch induced harmonics.	104
Figure 50.	Resettable switched-capacitor integrator with normal timing.	105
Figure 51.	Resettable switched-capacitor integrator with special timing.	107
Figure 52.	Folded cascode opamp 1: (a) DC gain vs V_o	

	(b) Harmonics.	108
Figure 53.	Folded cascode opamp 2: (a) DC gain vs V_{DD} . (b) Harmonics.	110
Figure 54.	Test system.	113
Figure 55.	Photomicrograph of test chip.	115
Figure 56.	Measured and simulated performance curves.	116
Figure 57.	Measured output spectrum for a 10kHz input signal at -4dB.	118

LIST OF SYMBOLS AND ABBREVIATIONS

A_o	Opamp open loop DC gain
ADC	Analog-to-digital converter
CMOS	Complementary metal oxide semiconductor
CODEC	Coder-Decoder integrated circuit
DAC	Digital-to-analog converter
dB	Decibel
DISDM	Double integration sigma delta modulator
Δ	Distance between quantization levels
f	Frequency
f_o	Highest frequency in passband
f_s	Sampling frequency
FFT	Fast Fourier Transform
ISDN	Integrated services digital network
k	Boltzmann's constant
K	Effective gain of quantizer
n	Order of noise shaping
SNR	Signal-to-noise ratio
SNR	Signal-to-quantization noise ratio
$S/(N+D)$	Signal-to-noise plus distortion ratio
V_p	Peak input signal level
α	Integrator gain
ω	Radian frequency

CHAPTER 1: INTRODUCTION

1.1 Thesis Motivation and Objective

A conventional analog-to-digital converter (ADC), such as the successive approximation type, typically requires large amounts of analog circuitry and is extremely sensitive to component variations. This is due to the fact that a large number of quantization levels must be set in the constituent digital-to-analog converter (DAC) through the use of precision components. Also, conventional ADC's usually sample the analog signal at approximately twice the Nyquist frequency¹. Consequently, they require several stages of switched-capacitor anti-aliasing filters in addition to an initial continuous filter stage.

Recently, oversampled ADC's have begun to gain widespread popularity because of the advantages they provide. The need for precision components to achieve high accuracy is removed by reducing the number of quantization levels to two. This is accomplished by filtering the baseband quantizer noise.

¹ The Nyquist frequency represents the highest frequency at which there is significant signal energy.

Since oversampled ADC's typically use sampling frequencies that are several orders of magnitude above the Nyquist, analog anti-aliasing filter requirements are substantially reduced; a simple RC low pass filter is usually sufficient. The bulk of the filtering is performed digitally before decimation occurs. In addition, the amount of analog circuitry and its sensitivity to digital noise is greatly reduced. As we will show, oversampled ADC's are typically only sensitive to noise injection at the input node. These converters reduce the amount of analog circuitry by utilizing the speed available in advanced processes.

Oversampled sigma delta ADC's can be classified in a variety of ways. For the purpose of this thesis, we will define two major categories: i) single-stage and ii) multi-stage converters. Classical single-stage architectures are characterized by the fact that they contain a single quantizer while multi-stage architectures are composed of classical single-stage converters in cascade.

At the start of the present work the concept of multi-stage sigma delta modulators had only recently been introduced [1]. Thus, it was considered a fruitful area for research. The objective of this work has been to investigate and develop new architectures for oversampled sigma delta ADC's suitable for monolithic realization.

1.2 Background

Over the past decade the sigma delta modulator (SDM) has been analyzed and implemented by a number of researchers [3,5-13]. A block diagram of the SDM is shown in Figure 3 on page 13. This architecture has gained widespread popularity because of its suitability to monolithic realization and because it does not require precision components [11]. It has been primarily used for voiceband applications. The SDM has been extended to provide second order noise shaping as shown in Figure 6 on page 18 [3]. This converter has been used in a variety of applications including voiceband codecs [3] and the ISDN 'U'-interface [17]. Although it is desirable to further extend this classical architecture to provide third order noise shaping, both experimental [3] and analytical studies [4] have shown that the third order feedback loop can become unstable at high signal levels.

Multi-stage architectures enable the creation of nth-order noise shaping modulators without the use of a nth-order feedback loop. Thus, stability is not a concern. Recently, multi-stage noise shaping modulators have been designed for voiceband [1] and high quality audio [18] applications. These converters are composed of first order SDM's in cascade and rely on the cancellation of quantization noise to achieve high resolution. Consequently, they re-

quire relatively high opamp gain and good capacitor matching compared to classical SDM's. In this thesis we will use a multi-stage approach to create a novel architecture which substantially reduces these requirements.

1.3 Oversampling Principle

Oversampled ADC's eliminate the need for high precision components by reducing the number of quantizer levels required to as low as two. This is accomplished through the use of oversampling and feedback techniques. Conventional ADC's require components with the same order of precision as the overall converter accuracy.

The number of quantizer levels is decreased through two mechanisms: i) oversampling and ii) noise shaping. Assuming that the quantizer noise is uniform, doubling the sampling frequency (f_s) will decrease the noise spectral density by 3dB. This applies to both oversampled and conventional ADC's. Sigma delta modulators further reduce the number of quantization levels by using feedback and integration to shape the quantizer noise. A nth-order converter shapes the quantizer noise by the function $(1-z^{-1})^n$; this is a high pass function with a substantial amount of baseband atten-

uation for large oversampling factors (f_o/f_s). Assuming $f_o \ll f_s$, this function has the following characteristic [3]:

$$\int_0^{f_o} \left| (1 - z^{-1})^n \right|^2 df \propto (f_s)^{-2n}$$

$z = e^{j\omega T}$

Consequently, doubling the sampling frequency of an n th-order converter will reduce the baseband quantization noise by $6n$ dB due to the noise shaping action alone. The total increase in signal-to-quantization noise ratio (SQNR) for a n th-order noise shaping modulator will be $(6n+3)$ dB when the sampling frequency is doubled.

1.4 Thesis Overview

The investigation and development of new architectures for high performance oversampled ADC's requires work in a number of related areas. This work will be dealt with in detail in the following chapters. The present section provides a brief overview of the topics covered.

Chapter 2 begins by reviewing the operation of classical single-stage SDM architectures. Analytical models useful for predicting SQNR are presented. Multi-stage converters are then investigated using analytical techniques extended to model performance sensitivity to component variations. This analysis leads to the development of a novel architecture which reduces implementation requirements.

Chapter 3 presents design considerations for three different oversampled ADC's: i) double integration sigma delta modulator, ii) ~~three~~-stage third order noise shaping modulator and iii) two-stage third order noise shaping modulator. The analytical models presented in Chapter 2 along with results of time domain simulations are used to determine coefficients. The implementation requirements for the three architectures are compared and contrasted using discrete-time simulations; including capacitor matching, opamp gain, settling and comparator requirements. These simulation results confirm the predictions made using the analytical models and provide further implementation guidelines.

In Chapter 4, the implementation requirements determined in Chapters 2 and 3 are used to design the novel two-stage third order noise shaping modulator. This converter is optimized for the ISDN 'U'-interface using the North American standard 2B1Q line code and implemented in a 1.5 micron CMOS

process. Test results are within 6dB of simulated performance and indicate 13 bits of resolution and linearity using a sampling frequency of only 2.56MHz. This performance compares favourably with results published to date.

In Chapter 5 conclusions are drawn and suggestions for future work in this area are made.

CHAPTER 2: ARCHITECTURE ALTERNATIVES FOR SIGMA DELTA MODULATORS

2.1 Introduction

In this thesis we will concentrate on architectures which use only two quantization levels. Thus, the quantizer can be implemented using a comparator. Another advantage is that the feedback DAC can be implemented using a switched-capacitor fed by a voltage reference. This is an important advantage because the accuracy of the converter is closely related to the linearity of the DAC. In CMOS technology, the linearity of a switched-capacitor is much higher than that of a multi-bit DAC.

The chapter begins by reviewing the operation of classical single-stage architectures. Analytical models useful for predicting SQNR are presented. These models contain parameters which are equal to one and thus are usually not included in the analysis of single-stage converters. We will find that these parameters are essential to model the performance sensitivity of multi-stage architectures to nonideal components.

Next, multi-stage converters composed of first order SDM's in cascade are analyzed. These architectures enable the creation of nth-order noise shaping modulators without the use of a nth-order feedback loop. The extended analytical models show that these converters are more sensitive to coefficient variations than classical architectures. This analysis leads to the development of a novel two-stage third order noise shaping modulator which reduces implementation requirements.

2.2 Single-Stage Architectures

Classical oversampled analog-to-digital converters are based on single-stage architectures. In fact, until recently [1] these were the only structures in use. One of the first converters developed was the delta modulator [20], shown in Figure 1. The high loop gain and oversampling ratio enables the output of the integrator to approximate the input signal, as shown in Figure 2. Thus, the receive signal can be reconstructed by digitally integrating the one bit output V_o .

The delta modulator is very sensitive to DAC and integrator nonidealities since its performance is dependent on matching the outputs of the digital and analog

Figure 1. Delta Modulator.

integrators [3]. This disadvantage can be eliminated by placing an integrator ahead of the summing node. Now we can replace the input and feedback integrator with a single integrator in the feedforward path. This architecture is called the sigma delta modulator.

Figure 2. Discrete-time simulation of delta modulator.

2.2.1 Sigma Delta Modulator

A block diagram of the sigma delta modulator is shown in Figure 3(a). This converter generates a one bit digital output which has an average value equal to the average input. In general, a multi-bit output can be generated. This requires the use of a multi-bit ADC as the quantizer and a multi-bit DAC in the feedback loop. Thus, circuit complexity is increased substantially and the increase in resolution may be more than offset by a decrease in linearity.

The results of an ideal discrete-time simulation are shown in Figure 4. The high oversampling ratio (f_s/f_i , where f_s =sampling frequency & f_i =input frequency) allows the coarse digital output to follow the input signal. The low frequency components of the output give a good representation of the input, while the high frequency components are dominated by quantization noise. To prevent aliasing, a digital lowpass filter is used to remove this out of band quantization noise before decimation. One should also note that the maximum output of the integrator is approximately equal to the maximum input level plus the feedback voltage. In an actual implementation this level would have to be controlled to prevent overloading the modulator. Implementation details will be discussed in Chapters 3 and 4.

(a)

Figure 3. Sigma delta modulator: (a) Block diagram. (b) z-domain model.

Figure 4. Discrete-time simulation of sigma delta modulator.

An analytical model of the SDM can be derived from its z-domain representation, shown in Figure 3(b). The quantizer is modelled by an additive noise source q preceded by its effective gain K . Simulations, using sinusoidal inputs, show that the gain of the modulator, V_o/X , is not affected by the gain of the integrator, α_1 . The effective gain of the quantizer, K , adjusts itself to make the effective loop gain equal to one. This has been shown previously by Candy [3]. Consequently, assuming that $\alpha_1 K = 1$, the output of the SDM can be represented as follows:

$$V_o(z) = X(z) + (1-z^{-1})Q(z) \quad (2.1)$$

where $Q(z)$ is the quantization noise. We should note that the inclusion of parameter α_1 and K , although seemingly unimportant at this point, will be essential to model the performance of multi-stage architectures. The multiplying factor $(1-z^{-1})$ is a high-pass function, as illustrated in Figure 5, and its magnitude is given by:

$$|1-z^{-1}| = 2\sin(\pi f/f_s) \quad (2.2)$$

$z = e^{j\omega T}$

Thus, the quantization noise is filtered by the feedback action. Increasing the oversampling ratio increases the in-band filtering and leads to a higher signal-to-quantization noise ratio (SQNR).

Figure 5. Quantization noise shaping for 1st, 2nd and 3rd order systems.

The SQNR of a first order noise shaping modulator is given by the following expression [3]:

$$\text{SQNR} = 30\log(f_s/f_o) + 20\log(V_p/\Delta) - 6.42 \text{ dB} \quad (2.3)$$

where f_s = sampling frequency, the passband is $0 \leq f \leq f_o$, V_p = peak input voltage, and Δ = distance between quantization levels. This equation is valid provided that $f_o/f_s \ll 1$ and the quantizer can be modelled as an additive noise, q , which is random. For a given implementation, V_p/Δ is a constant, and thus doubling the oversampling ratio will increase the resolution by 9dB (1.5 bits).

It has been shown [3] that the SDM exhibits high idle channel noise which is dependent on the DC input to the modulator. This is an important factor in applications such as voiceband codecs which have stringent idle channel noise requirements, but it is not a concern in applications such as ISDN where there is no idle channel condition. This impairment can be eliminated by using a dither signal; an out of band signal which is added to the input signal and removed digitally.

2.2.2 Double Integration Sigma Delta Modulator

For a given oversampling ratio, the resolution of the SDM can be increased substantially by adding a second integrator and feedback loop, as shown in Figure 6(a). The results of an ideal discrete-time simulation, shown in Fig-

(a)

(b)

Figure 6. Double integration sigma delta modulator: (a) Block diagram. (b) z-domain model.

ure 7 , illustrate that the density of ones and zeros in the output represents the input signal. The major disadvantage of this architecture can be seen by examining the output of the second integrator, I_2 . For input signals within approximately 6dB of the feedback voltage, I_2 becomes large and the modulator overloads. This produces harmonic distortion and consequently reduces the converter's resolution.

An expression for the output can be derived from the z-domain model shown in Figure 6(b). Again we will assume that the loop gains are unity; that is, $\alpha_1\alpha_2K=1$ and $\alpha_2K=1$. The output is represented as follows:

$$V_o(z) = X(z) + (1-z^{-1})^2 Q(z) \quad (2.4)$$

This equation shows that the DISDM is a second order noise shaping modulator since the quantization noise is filtered by the following second order high-pass function:

$$\left| 1-z^{-1} \right|^2 \bigg|_{\substack{z=e^{j\omega T} \\ z=e^{j2\pi f/f_s}}} = 4\sin^2(\pi f/f_s) \quad (2.5)$$

A plot of this function, along with the first and third order high-pass functions, is shown in Figure 5. Thus, the increase in resolution is due to the increase in passband filtering which the quantization noise experiences. At high frequencies the quantization noise is actually increased by

Figure 7. Discrete-time simulation of DISDM.

the feedback system. The SDM increases the noise by 6dB at half the sampling frequency and the DISDM by 12dB. Consequently, the DISDM requires a better decimation filter than the SDM. This will be discussed in Section 2.5 .

The following expression gives the SQNR of a second order noise shaping modulator [3]:

$$\text{SQNR} = 50\log(f_s/f_o) + 20\log(V_p/\Delta) - 20.17 \text{ dB} \quad (2.6)$$

Thus, doubling the oversampling ratio will increase the theoretical resolution by 15dB (2.5 bits). One should note that this equation does not predict a decrease in resolution at high input signal levels. This is due to the fact that the derivation assumes the quantizer can be modelled as an additive random noise source. This is not a good assumption when the output of the second integrator becomes larger than the quantizer level.

This architecture can be extended to create a third order noise shaping modulator by adding a third integrator and feedback loop. Unfortunately, the classical third order SDM can become unstable at high signal levels [4]. Consequently, the input signal must be attenuated substantially to avoid instability due to integrator saturation [14].

2.3 Multi-Stage Architectures

The concept of multi-stage oversampled analog-to-digital converters was introduced only recently in 1986 [1]. In this conference paper a group from NTT presented results for a second order noise shaping modulator which does not require a second order feedback loop. Consequently, this architecture can be used to produce higher order modulators without encountering instability problems at high input signal levels.

2.3.1 Two-Stage Second Order Noise Shaping Modulator

The discrete-time representation of a two stage noise shaping modulator is shown in Figure 8. This converter is comprised of two sigma delta modulators in cascade, with the output of the first integrator being used as the input to the second stage. The outputs of the first and second stage, $D_1(z)$ and $D_2(z)$, are one bit numbers. The final output of the converter is a multi-bit number which can be represented as follows, assuming $\alpha_1 K_1 = 1$ and $\alpha_2 K_2 = 1$:

Figure 8. z-domain model of two-stage noise shaping modulator.

$$D_o(z) = \alpha_1 H_1 z^{-1} X(z) + H_1 (1-z^{-1})^2 Q_1(z) + z^{-2} (1-\alpha_1 H_1) X(z) + z^{-2} (1-z^{-1}) (1-\alpha_1 H_1) Q_1(z) \quad (2.7)$$

where α_1 and H_1 are the integrator and digital gain factors, respectively. To create a second order noise shaping modulator, H_1 is set equal to $1/\alpha_1$. Consequently, the output becomes :

$$D_o(z) = z^{-1} X(z) + H_1 (1-z^{-1})^2 Q_1(z) \quad (2.8)$$

This equation shows that the SQNR is decreased by the digital gain factor H_1 . To avoid opamp saturation and second stage overload, the maximum value of α_1 which can be used is 0.5. This will result in a 6dB drop in resolution compared to the DISDM and a 12dB drop in resolution if a third stage is added, compared to an ideal third order noise shaping modulator.

A discrete-time simulation with $\alpha_1=0.5$ is shown in Figure 9. The digital output D_o has six equally spaced levels and thus requires a three bit representation. The decrease in SQNR due to H_1 can be eliminated by inserting this gain ahead of the second stage. Unfortunately, this is not possible in this architecture because the second stage will overload.

Figure 9. Discrete-time simulation of two-stage noise shaping modulator

As shown in Figure 10, a slight modification to the above circuit can decrease this overload problem and increase the resolution to the theoretical limit for a second order noise shaping modulator. Here, the output of the first stage multiplied by F_1 is subtracted from the first stage integrator output multiplied by H_1 , and the result is used as the input to the second stage. For $H_1=1/\alpha_1$, the input to the second stage is equal to $-z^{-1}Q_1(z)$ and its maximum value is $\Delta/2$. Consequently, overload will not occur in the second stage. The results of a discrete-time simulation with $\alpha_1=0.5$ are shown in Figure 11. The final output is a two bit number representing four levels.

The output of the first and second stage of the converter shown in Figure 10 can be represented as follows :

$$D_1(z) = X(z) + (1-z^{-1})Q_1(z)$$

$$\begin{aligned} D_2(z) = z^{-1}(\alpha_1 H_1 - F_1)X(z) &+ z^{-2}(F_1 - \alpha_1 H_1)Q_1(z) \\ &- F_1 z^{-1}Q_1(z) + (1-z^{-1})Q_2(z) \end{aligned}$$

The final output is :

$$\begin{aligned} D_0(z) = z^{-1}X(z) &+ (1-z^{-1})^2 Q_2(z) \\ &+ z^{-1}(1-z^{-1})(\alpha_1 H_1 - F_1)X(z) + z^{-1}(1-z^{-1})(1-F_1)Q_1(z) \\ &+ z^{-2}(1-z^{-1})(F_1 - \alpha_1 H_1)Q_1(z) \end{aligned} \quad (2.9)$$

Figure 10. z-domain model of two-stage noise shaping modulator with feedforward.

For $H_1 = 1/\alpha_1$, and $F_1 = 1$:

$$D_o(z) = z^{-1}X(z) + (1-z^{-1})^2Q_1(z)$$

Consequently, with perfect coefficient realization, this architecture gives the same resolution as the DISDM without overloading at high input signal levels. The third term in equation (2.9) creates a high frequency zero in the signal transfer function. This term is negligible because for an oversampling ratio of 128 and only 90% cancellation, the in-band gain variation is only 0.001 dB. The matching sensitivity due to the last two terms in equation (2.9) can be investigated by taking the partial derivative of $D_o(z)$ with respect to α_1 , H_1 and F_1 :

$$\frac{\partial D_o(z)}{\partial \alpha_1} = -z^{-2}H_1(1-z^{-1})Q_1(z) \quad (2.10)$$

$$\frac{\partial D_o(z)}{\partial H_1} = -z^{-2}\alpha_1(1-z^{-1})Q_1(z) \quad (2.11)$$

$$\frac{\partial D_o(z)}{\partial F_1} = -z^{-1}H_1(1-z^{-1})^2Q_1(z) \quad (2.12)$$

The above equations show that variations in α_1 and H_1 will create first order effects while variations in F_1 will only create second order matching effects. This sensitivity to

Figure 11. Discrete-time simulation of two stage noise shaping modulator with feedforward.

coefficient variation will be investigated in more detail in Chapter 3 through the use of time domain simulations.

2.3.2 Three-Stage Third Order Noise Shaping Modulator

The previous architecture can easily be extended to provide third order noise shaping by adding another stage, as shown in Figure 12. The output of each stage can be represented as follows :

$$D_1(z) = X(z) + (1-z^{-1})Q_1(z) \quad (2.13)$$

$$\begin{aligned} D_2(z) = & z^{-1}(\alpha_1 H_1 - F_1)X(z) + z^{-2}(F_1 - \alpha_1 H_1)Q_1(z) \\ & - z^{-1}F_1 Q_1(z) + (1-z^{-1})Q_2(z) \end{aligned} \quad (2.14)$$

$$\begin{aligned} D_3(z) = & z^{-2}(\alpha_1 H_1 - F_1)(\alpha_2 H_2 - F_2)X(z) - z^{-2}F_1(\alpha_2 H_2 - F_2)Q_1(z) \\ & + z^{-3}(F_1 - \alpha_1 H_1)(\alpha_2 H_2 - F_2)Q_1(z) - z^{-1}F_2 Q_2(z) \\ & + z^{-2}(F_2 - \alpha_2 H_2)Q_2(z) + (1-z^{-1})Q_3(z) \end{aligned} \quad (2.15)$$

Figure 12. z-domain model of three-stage noise shaping modulator.

Neglecting the second order terms in equation (2.15) :

$$\begin{aligned}
 D_o(z) = & z^{-2}X(z) + (1-z^{-1})^2Q_1(z) + z^{-1}(1-z^{-1})(\alpha_1H_1-F_1)X(z) \\
 & + z^{-1}(1-z^{-1})(F_1-\alpha_1H_1)Q_1(z) - z^{-2}(1-z^{-1})(1-F_1)Q_1(z) \\
 & + z^{-2}(1-z^{-1})^2(F_2-\alpha_2H_2)Q_2(z) - z^{-1}(1-z^{-1})^2(1-F_2)Q_2(z) \\
 & - z^{-2}(1-z^{-1})^2F_1(\alpha_2H_2-F_2)Q_1(z)
 \end{aligned} \tag{2.16}$$

Using the same procedure as in the previous section, one can show that variations in α_1 and H_1 produce first order effects while variations in F_1 , α_2 , H_2 , and F_2 produce second order effects.

Assuming $H_1=1/\alpha_1$, $F_1=1$, $H_2=1/\alpha_2$, and $F_2=1$ the output is :

$$D_o(z) = z^{-2}X(z) + (1-z^{-1})^2Q_1(z) \tag{2.17}$$

The theoretical signal-to-quantization noise ratio is given by the following equation:

$$SQNR = 70\log(fs/fo) + 20\log(Vp/\Delta) - 34.67 \text{ dB} \tag{2.18}$$

Consequently, doubling the oversampling ratio will increase the resolution by 21dB (3.5 bits).

2.3.3 Two-Stage Third Order Noise Shaping Modulator

In the previous section we found that the cancellation of quantization error from the first stage is more sensitive to parameter variations than that from the second stage. This is due to the fact that elimination of first stage noise requires cancellation of two signals which are nominally equal to $z^{-1}(1-z^{-1})Q_1(z)$ while elimination of second stage noise requires cancellation of two signals which are nominally equal to $(1-z^{-1})^2Q_2(z)$. Consequently, removing the requirement for cancellation of the larger quantization noise would make coefficient realization a second order effect. For example, with an oversampling ratio of 128, the accuracy requirement for a SQNR of 96dB would be approximately 8%.

Figure 13 shows the z-domain representation of a novel third order noise shaping modulator comprised of two stages; a DISDM followed by a SDM. The final output can be represented as follows :

$$\begin{aligned}
 D_o(z) = & z^{-1}X(z) + (1-z^{-1})^3Q_2(z) + z^{-1}(1-z^{-1})^2(1-F_1)Q_1(z) \\
 & + z^{-1}(1-z^{-1})^2(z^{-1}-\lambda)(\alpha_1, \alpha_2, H_1-F_1)Q_1(z) \\
 & + z^{-1}(1-z^{-1})^2(\alpha_1, \alpha_2, H_1-F_1)X(z)
 \end{aligned} \tag{2.19}$$

Figure 13: z-domain model of two-stage third order noise shaping modulator.

The last term in the equation can be neglected because for an oversampling ratio of 128 and 90% cancellation, the in-band gain variation is only 0.002dB. The matching sensitivity due to α_1 , α_2 , H_1 and F_1 can be examined by taking the partial derivative of $D_o(z)$ with respect to these gains :

$$\frac{\partial D_o(z)}{\partial \alpha_1} = -z^{-2} \alpha_2 H_1 (1-z^{-1})^2 (2-z^{-1}) Q_1(z) \quad (2.20)$$

$$\frac{\partial D_o(z)}{\partial \alpha_2} = -z^{-2} \alpha_1 H_1 (1-z^{-1})^2 (2-z^{-1}) Q_1(z) \quad (2.21)$$

$$\frac{\partial D_o(z)}{\partial H_1} = -z^{-2} \alpha_1 \alpha_2 (1-z^{-1})^2 (2-z^{-1}) Q_1(z) \quad (2.22)$$

$$\frac{\partial D_o(z)}{\partial F_1} = -z^{-1} (1-z^{-1})^2 Q_1(z) \quad (2.23)$$

The above equations show that coefficient variation for this architecture is a second order effect;

Assuming $H_1 = 1/(\alpha_1 \alpha_2)$ and $F_1 = 1$, the output can be represented as follows :

$$D_o(z) = z^{-1} X(z) + (1-z^{-1})^2 Q_1(z)$$

Consequently, this architecture provides third order noise shaping and is less sensitive to coefficient variations compared to the three-stage modulator. Its major disadvantage is that it is more prone to overload at high signal levels than the three-stage converter, which can be designed to exhibit no overload at all. This will be investigated in more detail in Chapter 3.

2.4 SQNR Comparison

In the previous two sections various oversampled analog-to-digital converter architectures have been examined. The major factor governing the signal-to-quantization-noise-ratio is the order of noise shaping provided by the given architecture. The SQNR of a n th-order noise shaping modulator is given by the following [3]:

$$\begin{aligned} \text{SQNR} = & 10(2n+1)\log(f_s/f_o) + 20\log(V_p/\Delta) \\ & - 20n\log(2\pi) + 10\log(6n+3) \end{aligned} \quad (2.24)$$

where f_s/f_o is the oversampling ratio, Δ is the distance between quantization levels, n is the order of noise shaping and V_p is the peak input level.

The benefit of higher order noise shaping is shown in Figure 14. For a given oversampling ratio, a higher order

Figure 14. SQNR comparison for 1st, 2nd and 3rd order noise shaping.

of noise shaping produces a higher SQNR. Conversely, to achieve a given SQNR, the higher the order of noise shaping, the lower the oversampling ratio required. For example, a SQNR of 96dB requires an oversampling ratio of 275 for second order noise shaping and only 88 for third order noise shaping.

2.5 Decimation Filter Requirements

Oversampled analog-to-digital converters with only two quantization levels yield high resolution by pushing most of the quantization noise out of band, as shown in Figure 5. This quantization noise must be attenuated sufficiently before decimation to prevent a decrease in SQNR. The digital decimation filter is usually implemented on the same chip as the analog modulator.

To reduce fold-over of quantization noise into the baseband during decimation, a common practice is to use a filter which has zeros at the new sampling rate and its multiples. A function with this property is :

$$H(z) = \frac{1 - z^{-N}}{N(1 - z^{-1})}$$

where N is the decimation factor. This function is commonly referred to as the sinc function since their frequency responses are approximately equal for $f/f_s \ll 1$.

Figure 5 shows that the out of band quantization noise rises more rapidly as the order of noise shaping is increased. Consequently, the decimation filter requirement also increases for higher order modulators. For a n th-order noise shaping modulator, the following filter function provides sufficient attenuation to prevent an increase in the inband quantization noise when decimating by a factor of N [3]:

$$H(z) = \left[\frac{1 - z^{-N}}{N(1 - z^{-1})} \right]^{(n+1)} \quad (2.25)$$

The magnitude of the frequency response of this function is given below:

$$|H(z)|_{z=e^{j\omega T}} = \left[\frac{\sin(N\pi f/f_s)}{N\sin(\pi f/f_s)} \right]^{(n+1)} \quad (2.26)$$

A plot of this function for $N=64$ and $n=2$ is shown in Figure 15.

Figure 15. Frequency response of 'sinc cubed function for $N=64$.

The requirement of a more complicated decimation filter is a clear disadvantage of using higher order oversampled ADC's. These digital filters require more silicon area and therefore are more costly. One must tradeoff the gain in performance over the cost due to an increase in area.

2.6 Conclusions

Architecture alternatives for both classical single-stage and newer multi-stage sigma, delta modulators were presented in this chapter. The advantage of higher order noise shaping was emphasized; namely, greater resolution for a given oversampling factor. Multi-stage converters are shown to be capable of providing n th-order noise shaping without the use of a n th-order feedback loop. Consequently, stability is not a concern.

Analytical techniques are extended to model the performance sensitivity of multi-stage architectures to nonideal components. Converters composed solely of first order SDM's in cascade are shown to be sensitive to component variation. This analysis has led to the development of a novel architecture which substantially reduces this sensitivity; the two-stage third order noise shaping modulator.

3.1 Introduction

One of the major advantages of oversampled ADC's is that they require a relatively small amount of analog circuitry compared to conventional ADC's. Design of this small amount of analog circuitry is complicated by the high sampling frequency required to achieve acceptable performance. The sampling frequency is usually several orders of magnitude above the Nyquist frequency, compared to conventional converters which sample at approximately twice the Nyquist.

In this chapter design considerations for oversampled analog-to-digital converters will be investigated. Three architectures introduced in the previous chapter are used as a basis of comparison. The three architectures are : i) Double integration sigma delta modulator, ii) Three-stage third order noise shaping modulator, and iii) Two-stage third order noise shaping modulator. The implementation sensitivities of these converters are compared and contrasted using a discrete-time simulation technique which is described in the next section. This technique is then used to determine coefficients, sensitivity to component mis-

match, opamp requirements, comparator requirements, settling requirements and sensitivity to noise injection.

3.2 Simulation Technique

The analytical models presented in Chapter 2, although useful for calculating theoretical performance limits, do not include nonidealities which can determine actual performance. For example, the linear models, by definition, cannot predict nonlinearities which in many cases limit performance. In addition to this, the analytical models are not capable of predicting the overload phenomenon which occurs in oversampled ADC's. Consequently, a more comprehensive method of analysis is needed.

A common and useful method of analysis is to perform a time domain simulation of the system. This can be done by writing the discrete-time equations for the ADC and solving numerically. Nonidealities such as component matching and settling time can be incorporated by adjusting the equations appropriately. Their effect on converter performance can be evaluated by transforming the digital output from the time to the frequency domain using a fast Fourier transform (FFT). Once in the frequency domain, the signal to noise

ratio (SNR) or signal to noise plus distortion ratio, $S/(N+D)$, can easily be calculated.

In order to measure high performance, care must be taken when transforming from the time to frequency domain. Otherwise, leakage errors will be produced by the FFT. These errors arise because of the practical requirement that we must limit observation of the signal to a finite interval and because the FFT assumes that the signal is periodic. A method of reducing this computational error is to analyze an integer number of input sinewaves. This does not completely eliminate the error because the digital output is not necessarily periodic in time due to the presence of quantization noise. The method used here to reduce computational error is to window the digital output before performing the FFT. A four-term Blackman-Harris window [15] is used. The window reduces spectral leakage by reducing the discontinuity at the observation boundary. This is accomplished by smoothly bringing the windowed data to zero at the boundaries.

The results of ideal discrete-time simulations for the three architectures are shown in Figure 16, Figure 17 and Figure 18. The conditions under which these simulations were performed are listed below and will be maintained for the remainder of the chapter, unless noted otherwise.

Figure 16. DISDM ideal simulation and analytical calculation.

Figure 17. Three-stage third order noise shaping modulator ideal simulation and analytical calculation.

Figure 18. Two-stage third order noise shaping modulator ideal simulation and analytical calculation.

Architecture	f_s (MHz)	f_o (kHz)	f_i (kHz)	SQNR(dB)
DISDM	7.68	40	9.375	87.8
Three-stage TONSM	2.56	40	10.0	85.7
Two-stage TONSM	2.56	40	10.0	85.7

These conditions were chosen for the following reasons. The 40kHz bandwidth represents the approximate signal bandwidth on the ISDN 'U'-interface for the North American standard 2B1Q line code. The oversampling factor (f_s/f_o) used for each architecture produces a theoretical SQNR which is greater than the requirement for the 'U'-interface. Although this requirement was not specified in the T1D1 specification at the time this thesis was written, it is usually regarded that 12-13-bits (72-78dB) is sufficient. Using equations 2.6 and 2.18 we find that the theoretical SQNR for the DISDM is 87.8dB if $f_s/f_o=192$ and for the third order modulators the SQNR is 85.7dB if $f_s/f_o=64$. The frequency of the sinusoidal input signal was selected so that the second, third and fourth harmonics would be inband.

The number of points (N) used in the FFT was determined by comparing performance for the three architectures while varying N from 8,192 to 524,288. As the number of points

was increased, the performance curves became more linear in the nonoverload region. Unfortunately, the computation time is proportional to $N \cdot \log(N)$. Consequently, N was selected to be 65,536 as an acceptable compromise.

The simulated ideal performance for the DISDM, shown in Figure 16, compares well with the analytical prediction (represented by the straight line) except in the overload region. This is also the case for the three-stage and two-stage third order noise shaping modulators which are shown in Figure 17 and Figure 18, respectively.

3.3 Coefficient Selection and Capacitor Matching

In this section, the simulation technique introduced in the previous section will be used to select coefficients for the three architectures. The following constraints will be considered during coefficient selection : i) circuit stability, ii) circuit overload, iii) opamp swing, and iv) quantization noise cancellation. The sensitivity of performance to coefficient variations caused by capacitor mismatch will also be investigated.

3.3.1 Double Integration Sigma Delta Modulator

Coefficient selection for this architecture is constrained by circuit stability, circuit overload and opamp swing. It is not constrained by quantization noise cancellation because the DISDM uses a single-stage architecture. Figure 19 shows a circuit diagram of the DISDM implemented using switched-capacitor techniques. The stability of this circuit has been investigated in [4] and will not be repeated here. In this paper the authors found that the DISDM is stable provided that $\alpha_1 < 2$, assuming $\alpha_1 K = 1$. In section 2.2 we assumed that $\alpha_1 \alpha_2 K = 1$ and $\alpha_2 K = 1$, consequently we will restrict ourselves to designs with $\alpha_1 = 1$. Thus, stability is ensured.

Figure 19 shows a circuit diagram of the DISDM implemented using switched-capacitor techniques. Comparing this diagram to the z-domain model of the DISDM in Figure 6 on page 18 we find the following relationships between parameters:

$$\alpha_1 = G_2 \frac{G_{1fb}}{G_{2fb}} \qquad \alpha_2 = G_{2fb}$$

Notice that the z-domain model assumes that $G_1/G_{1fb} = 1$ and that the maximum peak input signal is equal to the magnitude

Figure 19. DISDM circuit diagram.

of the feedback voltage. We will continue to make these assumptions until noted otherwise. In addition to $G_1=G_{lfb}$ and $\alpha_1=1$, we require two more constraints to determine the four coefficients. These two constraints will be set by limiting opamp output levels.

We will start by considering the maximum output level of the first integrator. As will be shown in section 3.7, noise and distortion introduced at this point will dominate those introduced in the second integrator. Assuming $G_1=G_{lfb}$ and $V_{pmax}=V_{pp}$, the maximum output of the first opamp is approximately equal to $2 \cdot G_{lfb} \cdot V_{pmax}$, provided that the modulator is not in the hard overload region. We will further assume that the opamp saturation level is V_{pmax} . Consequently, to avoid saturation of the first opamp G_{lfb} must be less than 0.5. Another factor which must be considered at this point is that opamp linearity decreases as the saturation limit is approached. To minimize this source of degradation we will limit the swing of the first opamp to one-half the saturation voltage by setting $G_{lfb}=0.25$. This source of nonlinearity will be examined in more detail in Chapter 4.

The last constraint is set by the saturation of the second opamp. Figure 20 shows the effect of opamp saturation on DISDM performance with $\alpha_1=1$, $G_1=G_{lfb}=0.25$ and α_2 varied

Figure 20. Effect of opamp saturation on DISDM performance, varying parameter α .

from 1 to 0.25. Consequently, α_1 is chosen to be 0.25. This makes $G2=1$ and $G2fb=0.25$.

Overload occurs in oversampled ADC's when the quantizer input exceeds its effective range. Figure 16

shows that this phenomena occurs at high signal levels in the DISDM. A certain amount of performance degradation at high signal levels can be tolerated in ISDN. This is due to the fact that the ADC input signal is comprised of two components; the far end signal and the near end echo. At high input signal levels, the far end signal is relatively large. Consequently, the $S/(N+D)$ requirement is relatively low and is dependent on system architecture.

DISDM performance is relatively insensitive to component mismatch because it does not rely on cancellation of quantization noise, as do multi-stage architectures. This is shown in Figure 21, where coefficient $G1fb$ is varied by 0%, 5% and 10%. There is no noticeable decrease in performance due to this variation. Similar results are obtained when the three remaining coefficients are varied.

Figure 21, Effect of coefficient $Glfb$ variation on DISDM performance.

3.3.2 Three-Stage Third Order Noise Shaping Modulator

Coefficient selection for this architecture is constrained by circuit overload, opamp swing and quantization noise cancellation. Circuit stability is not a concern, because the modulator is comprised of first order SDM's in cascade. A circuit diagram of the converter is shown in Figure 22. Comparing this diagram with the z-domain model shown in Figure 12 on page 31, we find the following relationships between parameters:

$$G1 = \alpha_1 \quad G1fb = \alpha_1$$

$$G2 = \alpha_1 H_1 \quad G2ff = F_1 \alpha_1 \quad G2fb = \alpha_1$$

$$G3 = \alpha_2 H_2 \quad G3ff = F_2 \alpha_2 \quad G3fb = \alpha_2$$

Equation (2.16) shows that to maintain quantization noise cancellation, the following equations must hold:

$$H_1 = \frac{1}{\alpha_1} \quad F_1 = 1$$

$$H_2 = \frac{1}{\alpha_2} \quad F_2 = 1$$

Figure 22. Three-stage third order noise shaping modulator circuit diagram.

Consequently, assuming that the constants α_1 , α_2 , and α_3 are set equal to the variable G , the switched-capacitor coefficients are:

$$G_1 = G$$

$$G_{1fb} = G$$

$$G_2 = 1$$

$$G_{2ff} = G$$

$$G_{2fb} = G$$

$$G_3 = 1$$

$$G_{3ff} = G$$

$$G_{3fb} = G$$

The variable G is selected by considering opamp saturation, as shown in Figure 23. Here G is varied from 1.0 to 0.25 and the hard saturation of the three opamps is set at the maximum peak input level. The reference feedback voltage is also set at the maximum peak input level. The simulated results show that G must be less than or equal to 0.5 in order to avoid a drop in performance due to opamp saturation. The maximum output of each opamp is equal to $G(V_{pmax} + V_{ref})$. If $G=0.5$ and $V_{pmax}=V_{ref}=1.5v$, then the maximum output of each opamp will be 1.5v. As the opamp output approaches its saturation level, the open loop gain usually drops. This will cause a drop in integrator gain and result in imperfect quantization noise cancellation. Consequently, we will set G at 0.25, limiting opamp swings to one half the saturation voltage. As mentioned previously, this will also improve the converter linearity. One

Figure 23. Effect of opamp saturation on three-stage third order noise shaping modulator performance.

of the major advantages of this architecture is that circuit overload can be avoided with proper design, as shown in Figure 23.

In section 2.3 we showed that the performance of the three-stage modulator is most sensitive to variations in parameters α_1 and H_1 . Variations in parameters F_1 , α_1 , H_1 and F_2 were shown to produce second order effects. These results have been verified and quantified using discrete-time simulations.

One of the causes of variations in the above mentioned parameters is capacitor mismatch. Figure 24 shows the effect of varying coefficient G_{1fb} on performance. This coefficient corresponds to parameter α_1 . Similarly, Figure 25 and Figure 27 show the effect of varying G_2 and G_{2fb} on performance. These two coefficients correspond to parameter H_1 . Variation in coefficient G_{1ff} is shown to have less effect on performance in Figure 26. This compares well with the analytical prediction as G_{2ff} corresponds to parameter F_1 . One should note the peculiar behavior of the curves in Figure 24, Figure 25 and Figure 27. As the input signal level is lowered the performance degrades until the input reaches -40dB. Below this level the performance is not affected by capacitor mismatch. The author has been unable to explain this phenomenon.

Figure 24. Effect of coefficient G_{lfb} variation on three-stage third order noise shaping modulator performance.

Figure 25. Effect of coefficient G_2 variation on three-stage third order noise shaping modulator performance.

Figure 26. Effect of coefficient G_{2ff} variation on three-stage third order noise shaping modulator performance.

Figure 27. Effect of coefficient G_{2fb} variation on three-stage third order noise shaping modulator performance.

As mentioned previously, to maintain perfect cancellation of first stage quantization noise, the following expressions must hold: $\alpha_1 H_1 = 1$ and $F_1 = 1$. We will concern ourselves with the first expression since the second one produces second order effects. Substituting the circuit coefficients for α_1 and H_1 , the following equation must hold:

$$G_{1fb} \frac{G_2}{G_{2fb}} = 1 \quad (3.3)$$

or

$$\frac{C_{1fb}}{C_{i1}} \frac{C_2}{C_{2fb}} = 1 \quad (3.4)$$

Consequently, variations in G_{1fb} , G_2 or G_{2fb} will degrade performance. This agrees well with what was shown in the previous paragraph.

3.3.3 Two-Stage Third Order Noise Shaping Modulator

Coefficient selection for this architecture is constrained by circuit stability, circuit overload, opamp swing and quantization noise cancellation. A circuit diagram of this modulator is shown in Figure 28. The first stage of this converter is a DISDM and the second stage is a SDM. The

Figure 28. Two-stage third order noise shaping modulator circuit diagram.

coefficients of the first stage have been determined previously: $G1=0.25$, $G1f=0.25$, $G2=1$ and $G2f=0.25$.

Comparing the circuit diagram in Figure 28 to the z-domain model of the two-stage modulator shown in Figure 13 on page 34 we find the following relationships between parameters:

$$\alpha_1 = G1fb \frac{G2}{G2fb} \quad H_1 = \frac{G3}{G3fb} \quad F_1 = \frac{G3ff}{G3fb}$$

$$\alpha_2 = G2fb \quad \alpha_3 = G3fb$$

To determine the three remaining coefficients, $G3$, $G3ff$ and $G3fb$, we require three constraints. The need to cancel quantization noise provides two of these constraints. From equation (2.19), the following must hold for perfect quantization noise cancellation:

$$F_1 = \alpha_1 \alpha_2 H_1 \quad F_1 = 1$$

Thus, $G3=4 \cdot G3fb$ and $G3ff=G3fb$. The last constraint comes from overload and opamp saturation in the second stage. Figure 29 shows the effect of overload and opamp saturation in the second stage while varying $\alpha_3=G3fb$ from 1 to 0.25. Consequently, $G3fb=G3ff=0.25$ and $G3=1$ are chosen.

Figure 29. Effect of overload and opamp saturation on two-stage third order noise shaping modulator performance, varying α .

In section 2.3 we showed analytically that coefficient variation only produces second order effects for the two-stage architecture. These results have been verified with discrete-time simulations. Figure 30 shows that varying coefficient G_{lfb} by up to 5% will not have a significant effect on performance. Similar results are obtained when the remaining coefficients are varied. This is a significant advantage which the two-stage architecture has over the three-stage architecture.

3.4 Opamp Gain Requirements

The most important component in an oversampled ADC is the operational amplifier. In this section we will show that multi-stage converters are more sensitive to finite opamp gain than single-stage converters. This results from the fact that finite opamp gain affects integrator gain which affects quantization noise cancellation. The output of the integrator, shown in Figure 31, with finite opamp gain, A_o , can be represented as follows:

$$V_o(n) = \frac{V_o(n-1)}{1 + \frac{G_l + G_{lfb}}{1 + A_o}} + \frac{G_l \cdot V_i(n-1/2)}{1 + \frac{1 + G_l + G_{lfb}}{A_o}} \quad (3.5)$$

Figure 30. Effect of coefficient G_{1fb} variation on two-stage third order noise shaping modulator performance.

Consequently, the gain of the integrator is altered by the finite DC gain of the opamp. This will affect the cancellation of quantization noise in multi-stage converters.

The open loop DC gain of an opamp is usually measured with the output biased at mid-rail. As the output approaches the saturation level, the gain and linearity of the opamp drops. The drop in gain can further impair cancellation of quantization noise and the drop in linearity can produce harmonic distortion. Consequently, these factors must be considered when specifying opamp gain.

3.4.1 Double Integration Sigma Delta Modulator

The effect of finite opamp gain on DISDM performance is shown in Figure 32. The gain is varied from 40dB to 80dB and is assumed to be independent of the opamp output voltage. The simulations show that the performance is not sensitive to opamp gain, assuming the gain is constant. As will be shown in Chapter 4, this is not a good assumption. The effect of voltage dependent gain will be investigated at that time.

Opamp DC Gain = A_o

$$G_1 = \frac{C_1}{C_{11}}$$

$$G_{1fb} = \frac{C_{1fb}}{C_{11}}$$

Figure 31. Switched-capacitor integrator using an opamp with finite open-loop DC gain A_o .

Figure 32. Effect of finite opamp DC gain on DISDM performance.

3.4.2 Three-Stage Third Order Noise Shaping Modulator

In section 2.3 we showed that the performance of this architecture is most sensitive to variations in parameters α_1 and H_1 . In addition to being affected by capacitor mismatch, parameter α_1 is also affected by the DC gain of the opamp in the first stage. Consequently, we expect that the performance of the three-stage converter would be sensitive to finite opamp gain; even if this gain is voltage independent. This is proven in Figure 33. Here, the DC gain of the first opamp is varied from 40dB to 80dB. Note that the parameter H_1 is only affected by capacitor matching and not by integrator gain. Therefore, finite opamp gain in the second and third stages will have less effect on performance. This has also been verified by simulation.

3.4.3 Two-Stage Third Order Noise Shaping Modulator

As was shown in section 2.3, one of the major advantages of this architecture is that it is less sensitive to parameter variations compared to the three-stage modulator. This is due to the fact that the two-stage converter only requires cancellation of two noise components which are nomi-

Figure -33. Effect of finite opamp DC gain on three-stage, third order noise shaping modulator performance.

nally equal to $(1-z^{-1})^2 Q_1(z)$, while the three-stage converter requires cancellation of two noise components which are significantly larger; nominally equal to $(1-z^{-1})Q_1(z)$. Consequently, we expect opamp gain requirements to be less stringent for the two-stage converter. This is verified in Figure 34. Consequently, implementation requirements for the two-stage converter are reduced compared to the three-stage converter.

3.5 Settling Requirements

One of the most stringent requirements for oversampled ADC's is the settling requirement. This is due to the fact that these converters require sampling frequencies that are several orders of magnitude above the Nyquist frequency; compared to conventional converters which sample at approximately twice the Nyquist. Sigma delta modulators also have large integrator swings from sample to sample, further complicating the design. For example, the maximum change in the output voltage of the first opamp is $(G_1 \cdot V_p + G_{1fb} \cdot V_{rp})$. Using switched-capacitor techniques, both RC time constants and opamps must be given sufficient time to settle.

Figure 34: Effect of finite opamp DC gain on two-stage third order noise shaping modulator performance.

For analysis purposes, we will distinguish between two types of settling error: i) linear settling error and ii) nonlinear settling error. Linear and nonlinear settling are defined as settling which are independent and dependent, respectively, of output voltage level. Linear settling error results in an integrator gain error while nonlinear settling causes harmonic distortion.

3.5.1 Double Integration Sigma Delta Modulator

The effect of linear settling error on DISDM performance is shown in Figure 35. Here the linear settling error is varied from 0% to 2% without any significant drop in performance. This result is as expected since the performance of the DISDM is relatively insensitive to integrator gain. The effect of nonlinear settling error is shown in Figure 36. Positive voltages are assumed to settle perfectly while the settling error for negative voltages is varied from 0.0% to 0.2%. The simulation results show that harmonic distortion is produced at high signal levels. Consequently, the settling error must be less than 0.1%.

Figure 35. Effect of linear settling error on DISDM performance.

Figure 36. Effect of nonlinear settling error on DISDM performance.

3.5.2 Three-Stage Third Order Noise Shaping Modulator

Previously, we have shown that this architecture is sensitive to variations in integrator gain caused by capacitor mismatch and finite opamp DC gain. Since linear settling error results in integrator gain error, we expect that this error will affect performance. Figure 37 verifies this conjecture. These results are similar to those obtained by varying coefficient G_{lfb} , as shown in Figure 24.

The effect of nonlinear settling is shown in Figure 38. The harmonic distortion produced in this architecture is similar to that produced in the DISDM under the same conditions and is dominated by the first integrator.

Figure 37. Effect of linear settling error on three-stage converter performance.

Figure 38. Effect of nonlinear settling error on three-stage converter performance.

3.5.3 Two-Stage Third Order Noise Shaping Modulator

Since this architecture is relatively insensitive to integrator gain compared to the three-stage converter, linear settling error should not have a significant effect on performance. This is shown in Figure 39, where the linear settling error is varied from 0.0% to 2.0% without any noticeable degradation in performance. The effect of nonlinear settling error on the two-stage converter is similar to the effect on the other two architectures. This is shown in Figure 40.

3.6 Noise Rejection and Comparator Requirements

An important consideration in the design of high performance analog circuits is an architecture's sensitivity to sources of noise and distortion. Here lies one of the advantageous characteristics of oversampled ADC's. In the next paragraph we will show that sigma delta modulators are relatively insensitive to sources of noise and distortion introduced after the first integrator.

2 of /de 2

Figure 39. Effect of linear settling error on two-stage converter performance.

Figure 40. Effect of nonlinear settling error on two-stage converter performance.

Referring to the z-domain model of the DISDM in Figure 6 on page 19, the transfer function from the input of the second summing node to the output, assuming $\alpha, \alpha, K=1$ and $\alpha, K=1$, is:

$$\frac{V_o(z)}{V_{i_2}(z)} = 1 - z^{-1}$$

Thus noise introduced at this point will see a considerable amount of inband attenuation. For an oversampling factor of 192, the attenuation will be 99.7dB. This includes high frequency noise which is folded down to baseband by the sampling action of the switched-capacitors. This is a major source of performance degradation in switched-capacitor circuits. Similarly, the transfer function from the input to the quantizer to the output is $(1 - z^{-1})^{1/\alpha}$. Similar results are found when the three-stage and two-stage noise shaping modulators are analyzed. Simulations show that this insensitivity to noise introduced after the first integrator also applies to distortion.

Applying the results obtained in the previous paragraph, we expect that comparator resolution should not pose a stringent requirement since the quantizer is placed after the first integrator in all three architectures. This is shown in Figure 41, Figure 42 and Figure 43. Here, limited comparator resolution is modeled as a 'dead' zone in which

the decision is random. These results show that comparator resolutions as low as 40mv do not affect performance. Consequently, the major comparator requirement is speed.

3.7 Conclusions

Design considerations for three different sigma delta modulators are presented in this chapter. Simulation results confirm the predictions made using analytical techniques in Chapter 2; that is, multi-stage converters composed solely of SDM's are relatively sensitive to integrator nonidealities compared to classical single-stage converters. These integrator nonidealities include capacitor mismatch, finite opamp gain and linear settling errors. The two-stage third order noise shaping modulator has been shown to be much less sensitive to these impairments.

Figure 41. Effect of comparator resolution on DISDM performance.

Figure 42. Effect of comparator resolution on three-stage converter performance.

Figure 43. Effect of comparator resolution on two-stage converter performance.

CHAPTER 4: TWO-STAGE THIRD ORDER NOISE SHAPING MODULATOR

4.1 Introduction

In Chapter 3 we compared and contrasted the circuit sensitivities of three converter architectures. In this chapter we will concentrate on the implementation of one of these architectures: the two-stage third order noise shaping modulator. This converter is selected for implementation because it is a novel structure which has potential advantages over the other two. The two-stage architecture reduces sampling frequency, opamp gain and capacitor matching requirements and does not require a dither signal to achieve good idle channel noise performance. The circuit will be optimized for the ISDN 'U'-interface using the North American standard 2B1Q line code. However, this does not preclude its use in other applications with high resolution and high bandwidth requirements.

The two-stage third order noise shaping modulator will be implemented in a two level poly and metal 1.5 micron CMOS process using single-ended switched-capacitor techniques. Differential circuit techniques are not used because of constraints on design, simulation and layout time. The goal of this design is to demonstrate the functionality and perform-

ance of the two-stage architecture, a goal which should be achievable without the use of differential techniques. Differential techniques would result in a circuit which is less sensitive to power supply noise; a characteristic which is of great importance in practice.

There are many sources of degradation in analog-to-digital converters implemented using switched-capacitor techniques. In some applications, such as voice-band codecs, noise is the dominant requirement for ADC performance, while in other applications, such as ISDN, both noise and distortion must be considered. Here, both will be considered when evaluating performance.

In Chapter 2, the theoretical signal to quantization noise ratio of various architectures was determined. In practice, performance is usually not limited by quantization noise. Other sources of noise and distortion usually limit performance of oversampled ADC's. The following sources of noise will be considered during the implementation of the two-stage converter: i) Switch thermal noise, ii) opamp noise, ii) quantization noise and iv) external noise. The following sources of harmonic distortion will also be considered: i) nonlinear opamp gain, ii) nonlinear settling, and iii) nonlinear charge injection from switches.

Section 4.5 presents test results on the two-stage third order noise shaping modulator [19]. One of the major objectives of this thesis was to develop new architectures for high performance oversampled ADC's suitable for monolithic realization. This objective has been met through the achievement of 13 bits of resolution and linearity over a 40kHz passband using a sampling frequency of only 2.56MHz.

4.2 Implementation

A block diagram of the two-stage third order noise shaping modulator is shown in Figure 44(a). For implementation using switched-capacitor techniques, the block diagram is transformed as shown in Figure 44(b). The block containing the integration symbol preceded by a minus sign represents a switched-capacitor inverting integrator; a common building block. The plus and minus signs beside the summing node inputs represent noninverting and inverting switched-capacitor resistors, respectively.

A circuit diagram of the ADC is shown in Figure 45. The two-stage third order noise shaping modulator will be optimized using the same constraints as in Chapter 3; $f_s=2.56\text{MHz}$ and $f_o=40\text{kHz}$. The coefficients determined in Chapter 3 will

Figure 44. Block diagram of two-stage modulator.

also be used; $G1=0.25$, $G1fb=0.25$, $G2=1$, $G2fb=0.25$, $G3=1$, $G3ff=0.25$, and $G3fb=0.25$. The converter will use a folded-cascode operational amplifier and a latching comparator. These components will be discussed in more detail in the following sections.

A circuit diagram of the feedback one bit digital-to-analog converter is shown in Figure 46. The four feedback voltages are generated as follows:

$$V_{r1} = \begin{cases} V_{rp}, D_1=0 \\ V_{rn}, D_1=1 \end{cases} \quad V_{r2}=V_{r3} = \begin{cases} V_{rp}, D_1=1 \\ V_{rn}, D_1=0 \end{cases} \quad V_{r4} = \begin{cases} V_{rp}, D_1=1 \\ V_{rn}, D_1=0 \end{cases}$$

The reference voltages, V_{rp} and V_{rn} , are generated externally and are set at ± 1.5 volts with respect to analog ground. A timing diagram is shown in Figure 47. All signals are generated on chip with the master clock, MCK , supplied to the device. Q_1 and Q_2 are non-overlapping clocks. Referring to the circuit diagram in Figure 45, the plain switches are closed during clock phase Q_1 and the switches with a small circle are closed during Q_2 . Thus, the input signal is sampled at the end of Q_1 and the integration takes place during Q_2 .

Figure 46. Circuit diagram of one bit DAC in feedback loop.

Figure 47. Timing diagram for two-stage modulator.

4.3 Switches and Capacitors

In this section we will concentrate on the selection of appropriately sized switches and capacitors. Opamp selection and simulation will be done in section 4.4. Although it is difficult to separate these two activities, we will attempt to follow a methodological design procedure in which capacitors and switches are selected based on a set of constraints and then the opamp is designed. In practice, this is usually an iterative procedure.

The first step of this procedure is to select absolute values for the switched-capacitors based on the constraint that switch thermal noise should be at least 6 dB below the quantization noise. Assuming the two noise sources are uncorrelated, the resulting drop in performance will be less than 1 dB. Once the values of the switched-capacitors are determined, the integrating capacitors can be calculated using the coefficients determined in Chapter 3.

Assuming $f_0 \ll f_s$, the total switch thermal noise in the frequency band $0 < f < f_0$ is given by [16]:

$$V^2 = \frac{4kT}{C} \cdot \frac{f_0}{f_s} \text{ volts}^2 \quad (4.1)$$

where k = Boltzmann's constant, T = absolute temperature, C = capacitance, and f_s = sampling frequency. The noise from the two switched-capacitor resistors at the input to the first stage has the same transfer function to the output as the input signal. Consequently, with $C_1 = C_{lfb} = 1\text{pF}$, the total noise from these switches, referred to the input, is 25uv rms. This is more than 6 dB below the theoretical quantization noise, which is 55uv rms assuming $V_{pmax} = V_{rp} = 1.5\text{v}$.

As was found in Chapter 3, noise sources which occur after the first integrator have less effect on performance because their transfer functions to the output are high pass functions with a substantial amount of inband attenuation. Switch thermal noise sources in the second and third integrators have transfer functions to the output of $(1-z^{-1})$ and $(1-z^{-1})^2$, respectively. Consequently, the minimum capacitor size in these integrators can be dropped to 0.5pF without any adverse effect on performance.

A lower bound for switch size is set by the need for adequate settling, while an upper bound, although more difficult to quantify, is needed to limit charge injection and degradation of power supply rejection. The simulated small-signal on-resistance of a CMOS transmission gate versus input voltage is shown in Figure 48. The aspect ratios of both the n and p-channel transistors are $W/L = 16$; they are

Figure 48. Small-signal on resistance of a CMOS transmission gate.

kept equal to reduce charge injection. The two curves represent nominal and worst case slow conditions. From these curves we see that the resistance of a transmission gate is dependent on input voltage. Thus, settling due to switches and capacitors will be a highly nonlinear process. In section 3.5, we showed that nonlinear integrator settling produces harmonic distortion. To make this source of distortion negligible compared to quantization noise, we will design for a worst case integrator settling error of less than 0.03%. Since opamp settling is more difficult to achieve than switch settling, switches and opamps will be designed to yield settling errors of less than 0.01% and 0.02%, respectively.

Transistor level simulations show that charge injection from switches is a nonlinear phenomenon and causes significant harmonic distortion. The results of a time domain simulation of the resettable integrator, shown in Figure 50, are shown in Figure 49(a). A voltage controlled voltage source with 120 dB of gain is used to represent an ideal opamp and an ideal switch is used for the reset switch. The results show that the charge injection from the switches causes harmonics which are approximately 66dB below the fundamental. This distortion is mainly caused by the input switch because its charge is directly related to the input voltage, while the charge of the virtual ground switch is almost constant from sample to sample.

(a)

(b)

Figure 49. Switch induced harmonics.

Figure 50. Resettable switched-capacitor integrator with normal timing.

A method of reducing this charge injection is to turn off the switches in sequence, with the switches connected to the virtual ground turned off first; as shown in Figure 51. This prohibits the charge of the input switch from being transferred to the integrating capacitor. Consequently, only charge from the virtual ground switch is injected onto the integrating capacitor. As the results in Figure 49(b) show, this reduces the harmonic distortion to more than 80dB below the fundamental.

4.4 Opamp and Comparator

Opamp selection will be based on the DC gain and settling time requirements determined in Chapter 3, as well as linearity and noise requirements. In section 3.4, we showed that the performance of the two-stage modulator is relatively insensitive to opamp gain, assuming the gain is independent of the output level. Figure 52(a) shows, however, that this is not a good assumption. For a folded cascode opamp [16], the simulated open loop DC gain is shown to decrease as the output level moves away from midrail. This is due to the fact that the transistors are beginning to move out of the saturation region. The effect of this nonlinearity is shown in Figure 52(b). Here, the resettable integrator, shown in Figure 50, is simulated in the time

Figure 51. Resettable switched-capacitor integrator with special timing.

(a)

(b)

Figure 52. Folded cascode opamp 1: (a) DC gain vs V_o .
(b) Harmonics.

domain using ideal switches and a folded cascode opamp. The sampling frequency is made artificially low, so that the output settles to its final value before it is sampled and transformed to the frequency domain. The output spectrum shows that a substantial amount of harmonic distortion is produced by the opamp; the second harmonic is only 65 dB below the fundamental.

Since it is difficult to completely remove the opamp gain variation with output level, the gain must be increased to limit this source of distortion. Figure 53(b) shows the simulated results of a second folded cascode opamp with higher gain, as shown in Figure 53(a). These results show that the harmonic distortion is reduced substantially by the increase in opamp gain.

The sampling frequency of the switched-capacitor circuit is 2.56MHz, giving a time of approximately 190ns for integrator settling. This can be increased by changing the duty cycle of the master clock. Thus, clock phase Q_1 can be increased and Q_2 decreased. Transistor level simulations show that a folded cascode opamp with a unity-gain bandwidth of approximately 20MHz is sufficient to produce settling errors of less than 0.02%.

As was shown in section 3.7, comparator resolution requirements are not stringent. Consequently, a latching

(a)

(b)

Figure 53. Folded cascode opamp 2: (a) DC gain vs V_o .
(b) Harmonics.

comparator is a good choice for this application since it is capable of providing the resolution and speed required.

4.5 Test Results

This section presents test results on the two-stage third-order noise shaping modulator [19]. The goal of this design was to demonstrate the functionality and performance of the two-stage architecture. This objective has been met through the achievement of 78 dB of $S/(N+D)$ over a 40kHz passband.

Circuit testing is complicated by the unavailability of test equipment for oversampled ADC's. This is due to the fact that these converters have only recently begun to gain widespread use. Further, the concept of multi-stage converters was only introduced in 1986 [1] and the circuit under test here is a novel architecture. Consequently, a customized test system was needed.

4.5.1 Test System

The main requirements for evaluating the two-stage converter are: i) to acquire a large number (up to 524,288) of samples of the two bit output, and ii) to perform a variety of processing tasks on the digital output, such as an FFT. The data acquisition is accomplished with a fast memory board. Two options exist for the digital processing; it can be done locally on a bench top computer or the data can be up-loaded to a mainframe and the processing can be performed there. We have chosen the second option so that the software developed to simulate the performance of the oversampled ADC's can be used to evaluate the fabricated device.

A diagram of the test system is shown in Figure 54. The digital output from the device under test is sent to the custom RAM board which resides in an IBM PC. The data acquisition is controlled by software on the PC. Once the data is acquired, it is up-loaded to the mainframe and the PC is used to emulate a terminal. The digital output is multiplied by a Blackman-Harris window, transformed to the frequency domain and then the frequency domain postprocessing is performed. This test system has been designed to enable evaluation of a variety of different oversampled ADC's. The link between the test board and the RAM board can handle a maximum word width of 6 bits at rates up

Figure 54. Test system.

to 20Mhz. The maximum storage capacity on the RAM board is 1.5Mbits.

4.5.2 Measurements

A photomicrograph of the test chip is shown in Figure 55. The chip contains two implementations of the converter with variations in switched-capacitor timing. A single converter occupies an area of 4.1mm^2 , including bonding pads. Little effort was expended to minimize area.

The measured and simulated performance curves, $S/(N+D)$, are shown in Figure 56. The input signal is a 10kHz sinewave and its maximum level is 1.1 volts peak. The sampling frequency is only 2.56MHz and the reference voltages are set at ± 1.5 volts. The noise and distortion are integrated over a bandwidth of 40kHz. The measured performance curve is within 6dB of the simulated curve and indicates approximately 13 bits of resolution and linearity. Figure 57 shows the output spectrum of the converter for a 10kHz input signal at -4dB. Harmonics are more than 80dB below the fundamental and therefore are not limiting performance. The power dissipation of the ADC is 20mW.

Figure 55. Photomicrograph of test chip.

The performance presented here compares favourably with the results published to date. For example, in [17] 12 bits of resolution and linearity were achieved over a bandwidth of approximately 60kHz. These researchers implemented a DISDM using current steering techniques which required a sampling frequency of 15.36MHz. Another example of an ADC designed for ISDN is given in [21], where a DISDM was used to achieve approximately 11 bits of resolution and linearity over a bandwidth of 60kHz.

The factor limiting the measured performance of the two-stage converter is thought to be external noise sources such

Figure 56. Measured and simulated performance curves.

as power supply noise. Evidence to support this conjecture is given below. When the sampling frequency is doubled to 5.12MHz, the performance of the ADC decreases and there is a noticeable increase in test board noise. Theoretically, the performance of the converter should increase. When the sampling frequency is decreased to 1.28MHz, there is a noticeable decrease in test board noise. As expected, the performance of the converter decreases because the theoretical limit is only 11 bits.

In order to measure the performance of the converter the test board must be electrically connected to the RAM board. When this connection is broken, the board noise decreases. This is monitored by viewing the digital output of the DISDM on a spectrum analyzer. Unfortunately, the performance of the two-stage converter can not be measured in this mode. A possible solution to this degradation could be to optically isolate the two boards.

The two-stage architecture was implemented using single-ended switched-capacitor circuit techniques which typically have poor power supply rejection, especially at frequencies around multiples of the sampling frequency. Consequently, high frequency noise injected into the circuit will be sampled and folded down to baseband. The use of differential

7

FIGURE 5 : MEASURED OUTPUT SPECTRUM.

Figure 57. Measured output spectrum for a 10kHz input signal at -4dB.

circuits has the potential to decrease this source of degradation.

4.6 Conclusions

Implementation considerations for the two-stage converter are presented in this chapter. Both noise and dis-

tortion are considered as sources of performance degradation. Charge injection from switches is shown to be a nonlinear phenomenon. Consequently, switches are turned off in sequence to reduce this source of distortion. Also, we have shown that opamp gain variation with output level can cause a significant amount of harmonic distortion.

One of the major objectives of this thesis was to investigate recent advances in oversampled sigma delta ADC's and, if possible, improve upon these advances. In this chapter, we have presented test results which demonstrate the functionality and performance of the two-stage third order noise shaping modulator; a novel architecture with significant advantages compared to architectures proposed previously. The performance achieved using this design compares favourably with results published to date.

CHAPTER 5: CONCLUSIONS

5.1 Summary

A desire to investigate and develop new architectures for high performance oversampled ADC's suitable for monolithic realization has provided the motivation for this thesis. Achievement of this objective has required work in the areas described below.

After an introduction to the thesis in Chapter 1, architecture alternatives for sigma delta modulators were investigated in Chapter 2. The operation and modelling of classical single-stage SDM's was reviewed. Multi-stage converters were then investigated using analytical techniques extended to model performance sensitivity to nonideal components. Converters composed solely of first order SDM's in cascade were shown to be relatively sensitive to nonideal components, compared to classical SDM's. This analysis has led to the development of a novel architecture, the two-stage third order noise shaping modulator, which significantly reduces implementation requirements.

Design considerations for three different sigma delta modulators were presented in Chapter 3. Converter coeffi-

cients were determined using discrete-time simulation results along with the analytical models presented in Chapter 2. The following implementation requirements for the three architectures were compared and contrasted using time domain simulations: capacitor matching, opamp gain, settling and comparator requirements. The predictions made in Chapter 2 using analytical models were confirmed by the simulation results in Chapter 3.

A major objective of this thesis has been to implement a high performance oversampled ADC on a 1.5 micron test chip. In Chapter 4 we presented the design and measurements of the two-stage third order noise shaping modulator. Test results were within 6 dB of simulated performance and indicated 13 bits of resolution and linearity over a 40kHz bandwidth; performance which compares favourably with results published to date.

5.2 Recommendations for Future Work

Oversampled ADC's have received a great deal of attention over the past five years. Consequently, this field has become very competitive with significant advances being made yearly. Despite this, it is felt that there still exist some fruitful areas for research.

One area which has not received a great deal of attention is the simulation of nonideal oversampled ADC's. It is very important to be able to simulate nonideal performance in order to develop high performance ADC's. In this thesis we used a discrete-time simulation technique where sampled-data equations are modified to introduce nonidealities such as finite opamp gain and settling error. As performance requirements increase, it becomes essential to have a closer coupling between transistor level and ADC simulators. Oversampled ADC's are highly nonlinear circuits and thus linear switched-capacitor simulators cannot be used. Consequently, a new type of simulator is needed.

The multi-stage architectures presented in this thesis can be extended to provide higher order noise shaping. For example, a fourth order modulator can be realized by cascading two DISDM's, or a single DISDM followed by two SDM's, or four SDM's. These higher order converters may be useful in high bandwidth applications such as video encoding. For example, a sixth order noise shaping modulator would theoretically provide a SQNR of 56.7 dB over a 8MHz bandwidth using a sampling frequency of 100MHz. This would require the use of a sub-micron CMOS process or GaAs technology.

REFERENCES

- [1] T. Hayashi, Y. Inabe, K. Uchimura, and T. Kimura, "A multi stage delta-sigma modulator without double integration loop," ISSCC Dig. Tech. Papers, pp. 182-183, Feb. 1986.
- [2] K. Uchimura, T. Hayashi, T. Kimura, and A. Iwata, "VLSI A to D and D to A converters with multi-stage noise shaping modulators," Proc. ICASSP, pp. 1545-1548, Apr. 1986.
- [3] J.C. Candy, "A use of double integration in sigma delta modulation," IEEE Transactions on Communications, Vol. COMM-33, pp. 249-258, Mar. 1985.
- [4] S.H. Ardalan and J.J. Paulos, "An analysis of nonlinear behavior in delta-sigma modulators," IEEE Transactions on Circuits and Systems, vol. CAS-34, pp. 593-603, June 1987.
- [5] J.C. Candy, "A use of limit cycle oscillations to obtain robust analog-to-digital converters," IEEE Transactions on Communications, vol. COM-22, pp. 298-305, Mar. 1974.
- [6] J.D. Everhard, "A single-channel PCM codec," IEEE J. Solid-State Circuits, vol. SC-11, pp. 25-38, Feb. 1979.
- [7] T. Misawa, J.E. Iwerson and J.G. Rush, "A single-chip CODEC with filters - architecture," Conf. Rec., IEEE Conf. Commun., vol. 1, pp. 30.5.1-30.5.6, June 1980.
- [8] L. vanDe Meeberg and D.J.G. Janssen, "PCM codec with on-chip digital filters," Conf. Rec., IEEE Int. Conf. Commun., vol. 2, pp. 30.4.1-30.4.6, June 1980.
- [9] J.C. Candy, B.A. Wooley and O.J. Benjamin, "A voiceband codec with digital filtering," IEEE Trans. Commun., vol. COM-29, pp. 815-830, June 1981.
- [10] J.C. Candy and O.J. Benjamin, "The structure of quantization noise from sigma delta modulation," IEEE Trans. Commun., vol. COMM-29, pp. 1316-1323, Sept. 1981.
- [11] M.W. Hauser, P.J. Hurst and R.W. Brodersen, "MOS ADC-filter combination that does not require precision analog components," ISSCC Dig. Tech. Papers, pp. 80-81, Feb. 1985.
- [12] M.W. Hauser and R.W. Brodersen, "Circuit and technology considerations for MOS delta-sigma A/D converters," Proc. ICASSP, pp. 1310-1315, Apr. 1986.

- [13] B.H. Leung, R. Neff, P.R. Gray and R.W. Brodersen, "A four-channel oversampled CMOS PCM voiceband coder," ISSCC Dig. Tech. Papers, pp. 106-107, Feb. 1988.
- [14] T.A. Kwasniewski and E. Keyes, "Test results for a third order, noise shaping coder for oversampled A/D conversion," Proc. CCVLSI, pp. 49-54, Oct. 1987.
- [15] F.J. Harris, "On the use of windows for harmonic analysis with the discrete Fourier Transform," Proc. IEEE, vol. 66, no.1, pp.51-83, Jan. 1978.
- [16] D.B. Ribner, "Design considerations for high-frequency switched-capacitor filters," Ph.D. dissertation Carleton University, Ottawa, Sept. 1985.
- [17] P. Koch, B. Heise, F. Eckbauer, E. Engelhardt, J.A. Fisher and F. Parzefall, "A 12 bit sigma-delta analog to digital converter with 15MHz clock rate," IEEE J. Solid-State Circuits, vol. SC-21, pp. 1003-1009, Dec. 1986.
- [18] Y. Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, M. Ishikawa, T. Yoshitome, "A 16-bit oversampling A-to-D conversion technology using triple-integration noise shaping," IEEE J. Solid-State Circuits, vol. SC-22, Dec. 1987.
- [19] L. Longo and M. Copeland, "A 13 bit ISDN-band Oversampled ADC using Two-stage Third Order Noise Shaping," Proc. IEEE CICC, to be published May 1988.
- [20] F. deJager, "Delta-modulation, a method of PCM transmission using a 1-unit code," Philips Res. Rep., vol.7, pp. 442-466, 1952.
- [21] B. Roessler, E. Wolter and H. Sporer, "CMOS analog front end of a transceiver with digital echo cancellation for ISDN," Proc. IEEE CICC, pp. 457-460, May 1987.

END

06-07-89

FIN