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**"/ "PERFORMANCE ANALYSIS OF TWO HOP"
"CSMA_CD/TDMA NETWORKS"**

by

ROBERT J. MACDONALD, B.Sc.

A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfilment of the requirements
for the degree of
Master of Science

Faculty of Engineering
Department of Systems and Computer Engineering
Carleton University
December 1989

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ABSTRACT

The recent proliferation of local area networks (LANs) and the increasing demands for interconnected LANs has resulted in the evolution of multi-hop metropolitan and wide area networks which satisfy these requirements.

This thesis considers a homogeneous network in which a number of CSMA_CD LANs (outer hops) are interconnected through a TDMA network (inner hop). Packets are transmitted by the CSMA_CD outer hops to a finite buffer inner hop controller. Upon reaching the top of queue, individual inbound packets are transmitted to the TDMA master station and rebroadcast using a separate outbound channel. During buffer full conditions the inner hop controller exercises flow control by applying a busy tone to the respective outer hop.

The objective of this thesis is to study the behaviour of the inbound channel and the outbound channel is not addressed. A mathematical approach for calculating average system delay versus throughput for two hop CSMA_CD/TDMA networks is presented and independently verified by a CSMA_CD/TDMA simulation program.

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LIST OF SYMBOLS

λ :	Packet arrival rate
T:	TDMA inner hop frame time
M:	Number of inner hop controllers
T/M:	TDMA slot transmission time
Θ :	Delay imposed by the inner hop controller on an outer hop due to buffer overload
N:	Inner hop controller/bridge buffer size (Chap 2) Number of controllers ready in outer hop (Chap 5)
Φ :	Packet interdeparture time from inner hop
Z:	Idle time experienced by inner hop controller due to empty buffer
X:	Service time of a packet which arrives to an empty system
Y:	Time between packet arrival to empty system and start of transmission
$\pi(n)$:	Probability that the inner hop buffer contains n packets given that no blocking has occurred
$r(k)$:	Unconditional probability that the inner hop contains k packets
$r(N)$:	Blocking probability at inner hop controller
Q:	Number of packets in the inner hop controller buffer

Q_t : Number of packets in the inner hop controller buffer at time t
 $T(k)$: Departure epochs of inner hop controller. Point where inner hop controller has successfully transmitted " k th " packet
 $m(n)$: n th moment of random time interval between $T(k)$ and $T(k+1)$
 $H^*(s)$: Laplace transform of random variable Θ
 h_1 : First moment of $H^*(s)$
 h_2 : Second moment of $H^*(s)$

 τ : maximum end to end propagation delay
 Q_n : Number of ready users in outer hop at departure epoch " n "
 U_n : Number of packets which arrive during channel assignment
 V_n : Number of packets which arrive during the transmission of packet n
 W_n : Number of packets which arrive during Θ
 C_n : Transmission time of packet n

 $B^*(s)$: Laplace transform of V_n
 $C^*(s)$: Laplace transform of U_n

R_n : Time required to assign channel during
collision between epochs $(n-1)$ and n
 Z_n : Idle period during epoch $(n-1)$ and n
 σ : Probability of successful transmission
during collision situations

 $W(z)$: z transform of W_n
 $J^*(s)$: Product of $H^*(s)$ and $B^*(s)$
 j_1 : First moment of $J^*(s)$
 j_2 : Second moment of $J^*(s)$

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

The widespread use of computers in the office and the requirement for these computers to communicate has created a corresponding demand for efficient computer communication networks. Network designers require an efficient, flexible modelling tool to predict network performance before building a particular network. Two general methods are available for modelling communication networks and often one is used to verify the other. The first method is mathematical analysis of networks using classical queuing theory [1,2]. With system parameters such as traffic intensity, frame transmission time, propagation delay, arrival rates, packet or message length and controller buffer size, system capabilities are calculated in terms of traffic intensity versus expected delay, blocking probability and expected queue size.

The second method involves the creation of an equivalent software model using a simulation programming language (eg. SLAM II [3]) and is referred to as simulation. Once verified, these programs are run repeatedly and the same system capabilities are obtained by collecting system statistics at various points during a sufficiently lengthy simulation run. Since simulation is less dependent on pure mathematics and is

a more tangible tool, it is often used to confirm numerical results obtained through mathematical performance analysis.

One drawback to a "simulation only" approach is the heavy CPU load associated with simulation programs. For example, the two hop CSMA_CD/TDMA simulation used in this thesis, while not optimized for execution efficiency, required 36 hours of continuous execution on an IBM PC/XT to process 1000 packets in a test run. The corresponding mathematical programs, also not execution optimized, required less than 20 minutes on the same computer.

Simulation programs also tend to be quite rigid in that a particular program will evaluate a specific system over a certain time interval. Changes to system parameters are achieved through the manual editing of simulation code unless a user interface program is designed to perform such operations on the user's behalf. Computer programs which process mathematical formulae may be modified in a program loop during execution and are significantly more flexible as a result. These programs require, in general, less computing time than their simulation counterparts. A compromise is also possible where mathematical models of some sub-systems are incorporated in the overall system simulation program.

Recently there has been a trend towards interconnection of local area networks (LANs) as large organizations begin to connect subordinate office LANs to their head offices in a hierarchical or distributed network. One approach is to have

two or more "hops" where the outer LANs or hops are connected to a central station through an intermediate network (inner hop). The central station receives data packets on an inbound channel and broadcasts them using a separate outbound channel to all LANs. Niktash et al [4] analyzed CSMA_CD/CSMA_CD two hop networks which could be used in a packet radio or cable television environment.

This thesis will utilize and extend the modelling technique of decoupling which was developed by Niktash [4] to decouple a two hop metropolitan area network into its respective single hops and perform independent delay/throughput analysis. In these networks data packets from the outer hops were buffered and relayed across the system through an inner hop which also performed flow control by blocking outer hop transmissions whenever buffer overflow was imminent.

In order to model this feature mathematically an expression for inner hop induced blocking and delay was developed and incorporated into the outer hop mathematical model for expected delay. As discussed previously, the particular configurations studied in [4] were CSMA_CD/CSMA_CD two hop metropolitan area networks in packet radio and CATV environments in which inner hop flow control was exercised by physically applying a busy tone to the source of the congestion, in this case, the applicable outer hop.

Since data transmission via satellite is a very popular method of providing high speed, long distance computer communications at local area network speeds and, since TDMA is a commonly used protocol in satellite networks, this thesis studies two hop wide area networks using TDMA as the inner hop protocol and CSMA_CD as the outer hop protocol. Interconnection of inner to outer hops is accomplished by an intelligent bridge which buffers incoming packets and provides positive, lossless flow control of the system through the same "channel busy" outer hop blocking technique.

1.2 LOCAL AREA NETWORKS

In terms of computer communication networks, a LAN is defined as two or more computers communicating in close proximity (eg. less than 2.5 kilometres for IEEE 802.3 ETHERNET) which are physically linked by some communication media for the purpose of exchanging data by some mutually understood rules or protocol. Two important features of a LAN are topology and access protocols [5-12]. The main LAN topologies are the ring (as in IEEE 802.5), bus (as in IEEE 802.3) and star architectures. Certainly there have been slight alterations to these basic configurations and networks have been mixed or "hybridized" but the basic architectures described many years ago in [11] continue to form the basis of modern computer communications networks.

Similarly, random and deterministic access protocols have evolved in slight variations from the ALOHA nets, ETHERNETS, and time division multiple access (TDMA) networks reviewed in [12] and again, to a reasonable extent, network protocols have remained essentially the same. Personal computer (PC) LAN's [8] have become quite popular as a low cost means of providing office automation. The architectures used in PC LANs follow traditional configurations used to network mainframes and minicomputers. LAN interconnection is becoming quite vital in providing efficient communications services between departments of geographically dispersed organizations.

The emphasis of this research is to develop, analyze and validate a mathematical model for a two hop CSMA_CD/TDMA network. The outer hops are individual, homogeneous CSMA_CD LANs and are each connected to a separate, finite buffer, inner hop controller. The inner hop controllers are interconnected and run a fixed assignment TDMA protocol where each controller is allocated one transmit slot in every TDMA frame. Packets originated by outer hop terminals are transmitted to a central station via the inner hop using an inbound channel. The central station broadcasts these packets using an outbound channel which is different from the inbound channel. The subject of this thesis is to study the performance of the inbound channel and the outbound channel is not considered. The mathematical modelling procedure

described and verified in the following chapters may be applied to various network architectures.

1.3 WIDE AND METROPOLITAN AREA NETWORKS

Wide and metropolitan area networks (WANs and MANs) are complex networks where the connected users are separated by greater physical distances than is customary for local area networks. Certain random access protocols which are used quite effectively in LANs such as CSMA_CD do not apply to wide area networking since their efficiency decreases as the maximum network propagation delay increases. At the same time, since WANs and MANs tend to interface many more computers in a single or multi hop fashion, deterministic access protocols such as TDMA or token passing rings are favoured since they may be used over longer distances than random access protocols.

1.4 NETWORK SURVEY

In narrowing down the selection of an inner and outer hop network protocol for this thesis, various publications and technical papers were reviewed. Those articles which discuss similar two hop networks and other related concerns such as interface bridge design, new protocol standards or LANs which have two hop potential are briefly summarized as follows:

1.4.1 The TORNET local area network [13]

Implemented in the University of Toronto, this LAN consists of independent, modular rings which employ a slotted register insertion technique for packet transmission. This method permits a station to transmit at a fixed time, for example, at the end of a message currently in progress, upon receipt of a token, or at the start of fixed, synchronized time slot. If an "upstream" message is received during transmission, it is inserted into a register and transmitted after the station's own message. Bridge devices are used to interconnect two TORNET LANs at a common point and these LANs may also be concatenated to form a multiple ring network. Inter-LAN communication is regulated by a name server whose address is known throughout the network and a call service request/confirm transport protocol. This system assures connectivity and a minimum bandwidth but suffers from buffer congestion at the LAN bridges since the bridge only has a single packet buffer. The TORNET LANs may also be interconnected by an inner hop to form a two hop MAN.

1.4.2 HIPERLAN [9]

The need for a high capacity (greater than 100 Mbps) data transmission has resulted in the development of HIPERLAN. Initially this network achieved the required bandwidth through

multi-mode fibre optics. It has recently been upgraded with the newer single mode fibre optic which uses ultra fast modulation techniques such as wavelength division multiplexing (WDM) to achieve transmission rates approaching 1 Gbps over short distances. While each node in HIPERLAN is designed to interface multiple hosts, there is no outer hop because each host is allowed to transmit and receive simultaneously within the limitations of the node processor. The objective of this system is to achieve "a host to host throughput which is limited only by the present hosts Direct Memory Access capacity...". Of significance is the inner hop protocol which operates between network nodes. HIPERLAN designers, after considering CSMA_CD and token passing ring protocols, selected the latter since token passing was easier to implement in hardware under a high speed data transmission scenario and because it offered superior fairness as compared to CSMA_CD in the equitable distribution of data transmission opportunities. Higher level transport and application level protocols control the host to host data transfer using a reservation type call request system thus assuring that adequate bandwidth is always available.

1.4.3 ADNET [10]

ADNET is a distributed naval vessel command and control system using a polled multi-drop bus architecture with centralized control. Dual highway controllers and dual internode cabling are used for the survivability which is critical in a military network. The bus transmits data at a rate of 3 Mbps over a 300 metre cable which connects a total of 63 computers. The measured effective throughput rate is approximately 1.8 Mbps. Polling is performed in a deterministic fashion by a highway controller. Individual stations respond with a "nothing to transmit" message or a data message. Data messages can be either a general broadcast variety and received by all other stations or uniquely addressed to a specific station. This system could be used as a outer hop and linked by highway controllers to other ships or possibly a mainland command and control system for the purpose of exchanging tactical or strategic information. The problem of inner hop buffering would require special consideration since the outer hop stations must be free to exchange data within a particular ship without interference from an inner hop controller. A reservation or call request system would be appropriate for this potential two hop network where inter-ship communication is desired.

1.4.4 SATELLITE TRANSMISSION EXPERIMENT LINKING LABORATORIES - STELLA [7]

Initially, STELLA-I was a wide area network which linked various Physics laboratories by a fixed allocation satellite TDMA network. Participants were limited to those computers which were directly connected to the satellite interface processors or line driver computers (LDC's) and applications were limited to large file transfers. The requirement for a more flexible data transfer environment involving local area networks resulted in the expansion of STELLA-I which was renamed STELLA-II. This new network interconnects several local and remote X.25 networks as well as various Cambridge Ring LAN's. As with STELLA-I, a line driver computer is used to interface each relevant LAN to the satellite channel. Access to the 2 Mbps satellite channel is controlled by a central LDC which employs a mixture of fixed and dynamic assigned TDMA slots to transmit data over the satellite channel. Remote X.25 networks are connected to STELLA via a public EURONET packet switched X.25 network.

In order to guarantee circuit continuity, a Virtual Circuit (VC) is dedicated to each participating X.25 network. If more than one remote terminal from the same network requires access to STELLA, the central LDC has the ability to multiplex multiple transmissions into one EURONET virtual

circuit which is de-multiplexed by the remote X.25 network LDC in an effort to conserve VC usage.

Figure 1.1 illustrates a portion of the STELLA-II configuration. This network is a practical example of a two hop satellite TDMA system. The first hop involves data transfer from a remote user terminal to the central LDC. The second hop relays data from the central LDC to the Orbital Test Satellite (OTS). The main differences between STELLA-II and the two hop system analyzed in this thesis is the outer hop protocol (CSMA_CD versus empty slot Cambridge ring and X.25) and the absence of a flow control mechanism in the outer hop controller (central LDC).

STELLA-II network designers assume that the large buffer size of the LDC, the low error rate of the satellite channel and the transport protocols used by the user stations will provide sufficient throughput and error recovery. However, flow control will undoubtedly become an overriding requirement in a real-time, no loss satellite TDMA system and, although not used in STELLA-II, flow control has many potential applications. Packet addressing is a multi-layer scheme which involves the addition and deletion of inter-network and sub-network headers by the respective gateways involved in the packet transfer process. The X.25 protocol, while ubiquitous, does not easily lend itself to closed form analysis. Network topology and alternate route selection algorithms create additional variables which do not exist in simpler LAN

STELLA II NETWORK

Figure 1.1

protocols such as the Cambridge Ring and CSMA_CD. In situations where remote X.25 networks are interconnected via wide area public packet switched networks such as EURONET in Figure 1.1, analytical complexities would surely increase.

In examining Figure 1.1, the Cambridge Ring, which is interfaced directly into the LDC, would closely approximate the system studied in this paper if the protocol was changed to CSMA_CD and if the LDC was given a flow control mechanism such as a "channel busy" tone which effectively disables a contention based access protocol.

1.4.5 THE UNIVERSITIES EXTENDED RING SATELLITE EXPERIMENT (UNIVERSE) NETWORK [14,15]

This network involves various communications research establishments and universities in Great Britain. Similar to STELLA, the UNIVERSE system interconnects several Cambridge Ring local area networks via satellite TDMA, in fact the same Orbital Test Satellite, with a public packet switched X.25 network as backup. Unlike STELLA, an INTERNET structure of gateways and addressing is not used. Delays induced by such gateways and the characteristics of the Cambridge Ring protocol (CR 82) employed precludes real time data transfer such as voice, video or remote file access applications. A global address format is used and data transfer is accomplished between host computers by pre-arranged virtual

Figure 1.2

circuits through the appropriate network gateways. Address information and port numbers are obtained from a network "name server". A UNIVERSE multi-network connection effectively provides the same level of circuit continuity as intra-LAN data transmission via the Cambridge Ring protocol plus the unavoidable propagation delay of the satellite channel. Again, flow control is not provided at the gateway level. As traffic load and the number network users increase, some form of statistical or dynamic multiplexing may be required with flow control for overload situations. The UNIVERSE network topology is shown in Figure 1.2. The satellite transmission protocol is a variation of the FPODA demand assigned TDMA. Earth stations are allocated specific slots within a time frame which may be used for short data packets (<100 bytes) or requests for additional slots which are received and granted by a master station in a subsequent reference burst or re-allocation cycle.

1.4.6 INTEGRATED SERVICES DIGITAL NETWORK (ISDN) [16,17]

The potential for inner hop connections via ISDN terrestrial circuits cannot be overlooked. The basic terminal access of 2B+D is designed for a voice/data application with the 64 Kbps "B" channels used for transmission and reception of data and the 16 Kbps "D" channel used for control and low speed data transmission. As a method of interconnecting

several LANs which run at speeds of 10 Mbps the basic access is obviously quite underpowered but primary ISDN access at 1.544 Mbps could be used as an inner hop transmission media as long as the traffic flow generated by the participating LANs was "controllable" by the inner hop interface processors. If ISDN is expanded to offer broadband services as discussed in [16] wide area LAN networking will become much more feasible with significantly increased capacity. Again, fixed or demand assigned TDMA could be used as an inner hop protocol as well as token passing or ALOHA.

The use of CSMA_CD over longer distances is questionable since the throughput of this access method for a given input arrival rate decreases as the ratio of circuit length to packet transmission time increases.

1.4.7 FIBRE DISTRIBUTED DATA INTERFACE (FDDI) [18]

FDDI was developed to provide a standard for high-performance, multi-station networks. FDDI operates at 100 Mbps (as well, it will be operating at 600 Mbps using GaAs technology) and uses a protocol which is similar but not identical to the token passing ring standard IEEE 802.5. Dual fibre optic cables are employed for enhanced reliability. The high capacity of FDDI will eventually be used in the design and implementation of large, higher speed LANs. More germane

to this thesis is the ability of FDDI to interconnect regular CSMA_CD LANs over a total distance of 100 kilometres.

Media access control is performed by all connected nodes or LAN interface stations through a Timed Token Protocol (TTP). TTP has two transmission modes: asynchronous or synchronous. In the synchronous mode, stations obtain a predetermined amount of transmission bandwidth on each token rotation and share the remaining bandwidth in the asynchronous mode. While not exactly a fixed slot TDMA protocol, there are similarities especially in a network where all available bandwidth is divided equally among the participating stations. The mathematical approach developed in this thesis could be extended to analyze a two hop CSMA_CD/FDDI network, assuming that a suitable single hop FDDI analytical model becomes available.

1.4.8 QUEUED PACKET AND SYNCHRONOUS SWITCH (QPSX) [19]

QPSX is a distributed network which is based on two high speed (150 Mbps) contra-directional buses. Within a single hop, the connected nodes are treated as one distributed queue. The orderly transmission of packets by the constituent users is achieved through the accurate maintenance of outstanding requests for transmission from all network nodes and a corresponding knowledge of individual slot allocations or transmit times by each node. Packets are segmented in

accordance with the slot size of the bus involved and as a result, "bus hogging" is avoided when different packet sizes are used by different nodes in the same hop. QPSX individual networks may be interconnected as two hop Metropolitan Area Networks using bridges which perform basic route selection and support route diversity in multi-hop networks. Clearly there is no inter-hop flow control mechanism in QPSX since node to node data transfer is coordinated through a call setup procedure. This method does not incorporate inner hop blocking and, as a result, total expected system delay is the sum of inner and outer hop expected delays with no interdependencies.

1.5 SUMMARY

In this chapter a number of two hop networks have been reviewed as well as various metropolitan area network standards and individual local area networks. The UNIVERSE and STELLA-II networks have components which closely parallel the general two hop model described and analyzed in this thesis. There are also MAN standards such as DQDB (IEEE 802.6) and FDDI which could be used as inner hops in future two hop networks and analyzed using the same mathematical techniques.

1.6 THESIS STRUCTURE

The remaining chapters of this thesis are briefly summarized as follows:

In Chapter 2 the mathematical model for a finite buffer TDMA protocol is presented and results are compared to the associated simulation program. The CSMA_CD mathematical model is then verified by two different simulation programs. The first program is based on random packet selection from a single infinite queue using the limiting throughput of S-ALOHA in the retransmission algorithm. The second program is a true contention based simulation of 1-persistent CSMA/CD protocol.

In Chapter 3, a technique for using a loss TDMA mathematical model to approximate a lossless TDMA inner hop model is presented and discussed. This approximation is used in Chapter 6 to compare two hop simulated (lossless) results to mathematical (loss) results.

In Chapter 4, the theory of residual life is used to approximate the inner hop to outer hop blocking delay. The corresponding unconditional Laplace transform of the probability distribution function is also derived.

In Chapter 5, the delay equation of the outer hop is derived. Included in this derivation is the Laplace transform of the distribution of the inner hop blocking time obtained previously in Chapter 4.

In Chapter 6, two CSMA_CD/TDMA systems with different network parameters are analyzed numerically and the results for 2, 3 and 5 packet buffer configurations are compared to simulation.

In Chapter 7, conclusions and proposals for future research are discussed.

1.7 CONTRIBUTIONS

The contributions of this thesis are the following:

In Chapter 2, the TDMA and 1-persistent CSMA_CD simulation programs are verified through favourable comparisons with established mathematical results [20,21]. These validated programs are then used to successfully confirm the specific TDMA and CSMA_CD mathematical models derived in this thesis.

In Chapter 6, the system expected delay results are reviewed. The inaccurate assumption of expected delay based on Poisson arrivals to the inner hop for stable systems is replaced by a deterministic inner hop delay. The recalculated numerical expected delay results show close agreement to simulation.

Also in Chapter 6, a procedure for using a lossy TDMA mathematical model to approximate a lossless TDMA protocol is verified. The residual life probability distribution function used to approximate inner hop blocking delay is found to be

inaccurate under high input traffic intensity. A more accurate value of one TDMA frame is substituted and confirmed.

Generally this research extends the efforts of Niktash et al [4] and applies the "divide and conquer" modelling approach to CSMA_CD/TDMA networks.

In Chapter 7, two sets of rules are developed for stable and potentially unstable two hop networks. These rules may be applied to all CSMA_CD/TDMA configurations.

CHAPTER 2

PROBLEM DEFINITION

2.1 INTRODUCTION

This Chapter will describe the two hop system under study and establish the general assumptions and methodologies to be used in network modelling and performance analysis. Simulation models for single hop TDMA and CSMA_CD are also presented and verified against proven numerical results [21,20].

2.2 SYSTEM DESCRIPTION

As discussed in Chapter 1, the system under consideration is a two hop CSMA_CD/TDMA network in which various outer hop LAN users transmit data packets from their terminals to a central station through finite buffer inner hop controllers. The general topology of this network is illustrated in Figure 2.1. Data packets originating from user terminals are first transmitted over a CSMA_CD outer hop to the associated inner hop controller. The inner hop controller then transmits these packets to a central station using a fixed assignment TDMA protocol. It is assumed that the central station broadcasts all received packets to all users over a separate outbound channel and that maintenance of

Figure 2.1 Sample Two Hop System

Figure 2.2 TDMA Inner Hop

packet sequencing (packets sent and received in the same order) is the responsibility of a higher level protocol. Although many terminals use multi-packet messages or files, this thesis only considers expected delay for unipacket systems and multiple or "batch" transmissions will not be analyzed.

The outer hop terminals are assumed to form a large but finite population which as a group form an independent Poisson process with a combined mean packet generation rate of λ packets per second. It is further assumed that the time between the generation of successive packets by a terminal is very large compared to the time that it takes to transmit the same packet to its associated controller and, as a result, there will be no more than one packet in queue at an individual terminal. Thus, the generation of a message by a user effectively increases the number of ready terminals (terminals with one packet to transmit) by one. Flow control is exercised by the inner hop controller which applies a busy signal to the outer hop during buffer full conditions.

Figure 2.2 depicts a snapshot of the inner hop TDMA channel. Each inner hop controller is assigned one slot in a frame cycle and transmits one packet at its allocated time. The frame cycle time (T) is the product of the number of controllers (M) and the controller slot transmission time (T/M). It also includes a small period of time required to perform frame synchronization which is assumed to be

negligible. The additional control information required for the TDMA protocol is also assumed to be negligible in comparison to the length of a TDMA frame and will also be ignored.

Packets transmitted by the outer hop are received individually by the inner hop controller and retransmitted on the inner TDMA hop during that controller's allocated slot. There is no concatenation or segmentation of packets and as a result, the outer hop packet lengths and the inner hop TDMA slot sizes are equal. The finite buffer TDMA protocol which is similar to the protocol examined in [21] and [22] will be thoroughly specified and analyzed in Chapter 3.

Once received by the inner hop controller, the packet is buffered in a finite, FIFO queue. Upon reaching the top of queue, the packet is transmitted during the controller's allocated time slot. Note that the inner hop controllers do not perform packet assembly or disassembly. The outer hop CSMA_CD network is assumed to be full duplex with separate frequencies for incoming and outgoing packets and hence there is no contention between transmitted and received packets. The inner hop also employs full duplex transmission. Once a packet is received by the master station it is retransmitted on a separate broadcast frequency to all other inner hop controllers during the next outbound (master station to inner hop) time slot. As with the outer hop, there is no contention between inbound and outbound packets. In addition, there is

no contention among inner hop controllers since a fixed slot TDMA protocol is employed. This inner hop controller independence feature will be used in the development of the TDMA numerical analysis and simulation where the behaviour of a multiple station network will be reduced to observing the performance of a single controller.

The important performance parameters of this system are the expected delay experienced by a packet from its generation time, that is, the time an outer hop terminal becomes ready to the time that the packet is completely transmitted on the inner hop to the central station. The packet transmission delay to the central station and the subsequent retransmission time of the packet on a separate, uncontested, outbound channel are constants which are not considered in this thesis. However, these values may be easily obtained and added to the inbound expected delay is a total network delay time is required. The expected delay results presented in Chapter 6 reflect inbound expected delay only.

2.3 AN OVERVIEW OF THE MODELLING PROCESS

Analysis of the two hop CSMA_CD/TDMA network will be accomplished using a two phase procedure. In the first phase, mathematical models used in [1],[2],[20] and [4] will be adapted and applied to this problem. The process of "decoupling" inner and outer hops as developed in [4] will

result in expressions for individual expected delays as well as the blocking probability for the inner hop. Next, the distribution of the duration of the inner hop's "busy tone" (random variable Θ) will be obtained and subsequently incorporated into the analysis of the outer hop expected delay. Finally, the sum of inner and outer hop average delays will yield the system expected delay for the network.

Two different network configurations will be analyzed under varying traffic intensities. In phase two, simulation programs will be developed which simulate the characteristics of TDMA and 1-persistent CSMA_CD protocols in every detail. These two simulations will be developed separately and tested against proven analytical results [21,20]. Once the "decoupled" simulation programs are verified, they will be combined and enhanced to incorporate an equivalent inner hop blocking mechanism. The two hop CSMA_CD/TDMA program will then be run using the same network parameters as those employed in the mathematical model. The various statistics (blocking probability, expected number of packets in queue and expected delay) will be gathered and compared to the mathematical results.

2.4 RESULTS OF INDEPENDENT PROTOCOL SIMULATION

SLAM II diagrams for TDMA and CSMA_CD are presented in Appendix C along with a comparison of mathematical and

simulation results for expected delay. The TDMA simulation was configured to match the network parameters used by Yan [21] and Figures C.4 to C.7 illustrate the close agreement between simulation and analytical results for expected delay. The CSMA_CD simulation program was configured to correspond with values used by Lam [20]. Initially the CSMA_CD program was based on two contending terminals and, although expected delay comparisons were favourable, program execution time was excessive. A more efficient CSMA_CD program using a contention resolution algorithm based on the throughput of slotted ALOHA was substituted and found to closely match Lam's results [20]. Tables C.1 and C.2 contain detailed simulation and numerical results for two different CSMA_CD configurations.

2.5 CONCLUSION

As observed in Appendix C, the system expected delay results obtained for the TDMA and CSMA_CD simulation programs closely match their associated mathematical results [20,21]. In Chapter 6, these simulation programs will be merged into a two hop CSMA_CD/TDMA program and modified to perform outer hop blocking. This combined program will be used for the verification of the CSMA_CD/TDMA mathematical model which will be developed in Chapters 3, 4 and 5.

CHAPTER 3

PERFORMANCE ANALYSIS OF FINITE BUFFER TDMA NETWORK

3.1 INTRODUCTION

In this Chapter the inner hop protocol is examined, various analytical techniques are reviewed and the most suitable mathematical process for modelling the finite buffer TDMA inner hop is selected. The chosen model is then presented in detail along with supporting mathematical derivations.

3.2 REVIEW OF INNER HOP MODELLING TECHNIQUES

Nikdash et al [4,23] developed two techniques for modelling the inner hop of a two-hop CSMA_CD/CSMA_CD network. The first method was applicable to small systems with less than 5 inner hop controllers. A Markov chain analysis was performed using a state vector which reflected the number of messages in the buffer of each controller and the identity of the controller which had most recently transmitted without collision. This small system model could be used to model a TDMA inner hop since the state vector contained all the required information to determine if and when a given controller will transmit. As discussed in [4] this approach

suffers from intractability as the inner hop controller population and buffer size increases.

A large system model was introduced in [4] to significantly reduce the number of state transitions for the CSMA_CD inner hop. The large system state vector reflected the number of active controllers less a randomly selected controller, the number of packets in the buffer of the selected controller and an indication as to whether or not the selected controller was the last to successfully transmit. This model was suitable for a non-deterministic access schemes such as CSMA_CD since every controller had an equal opportunity to transmit in each time slot.

For TDMA or any other deterministic access protocol there is no tractable method of defining a similar Markov model which would yield an approximation for the distribution of the time period Θ during which the buffer of an inner hop controller is full. Such a model would need to contain the buffer or queue states of each TDMA controller and would rapidly become unmanageable. A different modelling approach was required and the ensuing search resulted in a procedure which was drawn from four sources. Hayes [7] and Kleinrock [12] supplied the basic M/G/1 queuing theory and techniques for analyzing single server queuing systems where the initiator of a busy period receives exceptional or non-standard service. This general theory was specifically

applied to an infinite buffer, multi-queue, variable length message, TDMA system by Lam [13].

Lam's TDMA model was further extended through the consideration of a finite message buffer, lossy system by Yan [21] where messages were discarded by a controller under buffer full conditions. Yan's model was enhanced by Hillier and Jabbarian [22] by adding and analyzing a variable slot or batch message mode. The latter model could be used to evaluate demand assigned satellite TDMA (DAMA) systems. This thesis considers homogeneous two hop systems in which controllers have identical statistical properties and user terminals transmit single packets. As a result, Yan's model was selected as the basis for the inner hop TDMA analysis and eventually the derivation of the distribution of random variable θ .

3.3 FINITE BUFFER TDMA PERFORMANCE ANALYSIS

To briefly summarize the analytical process, the TDMA inner hop will be modelled as an M/G/1 FCFS queuing system. In this system a packet which enters an empty inner hop buffer is given immediate access to the server and thus encounters random service delay. Packets which enter a partially full buffer wait a random period of time before entering the server and accrue a constant service delay of one TDMA frame. A Markov chain analysis of packet departure epochs is developed

and permits the calculation of the expected number of packets in queue, the expected packet delay, the probability of blocking (buffer full) and the expected time during which the buffer of a controller is full. The latter result will be carried over into the analysis of the outer hop, in order to reflect inter-hop dependence and is explained in Chapter 5. In order to provide an overview of Appendix D which contains a detailed derivation of inner hop expected delay, the following notation is introduced:

TDMA frame duration:	T (seconds)
Number of inner hop controllers:	M
Controller slot length:	T/M (seconds)
Arrival rate to inner hop:	λ (packets/sec)
Inner hop controller buffer size:	N (packets)
Interdeparture time from Inner hop controller:	Φ (seconds)

It should be noted that this analysis only concerns a single inner hop controller and its associated outer hop. Since TDMA is used as the inner hop protocol each inner hop controller functions independently and cannot affect the performance of other controllers. This feature also permits the analysis of heterogeneous systems of mixed buffer sizes since each controller is analyzed separately and could also be extended to variable length packets assuming that a variable slot TDMA protocol exists.

The TDMA loss model is based on a single step Markov chain which is established using transition probabilities between various queue or buffer states. Poisson arrivals are assumed and an arriving packet will encounter one of two situations, an empty controller buffer or a partially filled buffer. The respective empty and busy controller packet queuing delays have different distributions since packets which arrive to an empty system are granted immediate access to the TDMA server and have a random service time with no queuing delay. Arrivals to a partially filled system have a random queuing delay and a constant service time of one TDMA frame. The expected value of the inter-departure time, $E[\Phi]$, is T for a non-empty system and $[Z + X]$ where Z is the idle time where no arrivals occur and X is the service time of a packet which arrives to an empty system and must wait for the next transmission opportunity. Overall $E[\Phi]$ is therefore:

$$E[\Phi] = [1 - \pi(0)]T + \pi(0)(E[Z] + E[X]) \quad (3.1)$$

where $\pi(k)$ is the steady state probability that the system is found to be at state " k " (" k " packets are in the system at departure epochs and as a result, $\pi(N) = 0$). The random variable X is the sum of random variable Y which is the time period between packet arrival to an empty system and start of a transmission plus T/M which is the constant slot transmission time. The detailed derivation of random variable

Y is contained in Appendix D. The expected inter-departure time is:

$$E[\Phi] = [1-\pi(0)]T + \pi(0)[1/\lambda + T/M + e\lambda^{T/M} (\lambda T - 1 + e^{-\lambda T})] \quad (3.2)$$

Since this model is a loss model, the average arrival rate to the controller is equal to the average departure rate. Therefore:

$$\lambda(1-r(N)) = 1/E[\Phi] \quad \text{where } r(N) \text{ is the blocking probability} \quad (3.3)$$

Solving for $r(N)$, the expected number of packets in the system $E[Q]$ may now be obtained as follows:

$$E[Q] = \sum_{k=0}^N k[r(k)] \quad (3.4)$$

where k represents the system queue size and $r(k)$ is the probability that the system is in state k at any point in time whereas $\pi(k)$ is the observation made at departure epochs.

Little's result is then used to obtain the expected value for packet delay, D :

$$D = \frac{E[Q]}{\lambda[1-r(N)]} \quad (3.5)$$

Packets which arrive during inner hop buffer full conditions will be discarded. This is a significant difference in that the two hop CSMA_CD/TDMA system under

consideration prohibits new arrivals to or data transmission from the outer hop when the inner hop controller's buffer becomes full. Consequently, in order to use this loss model to approximate a lossless model, a method for estimating lossless performance based on the system queue state is required. The preceding numerical analysis provides a blocking probability $r(N)$ which can be used as an approximation to the lossless inner hop arrival rate or the effective arrival rate of packets which were not blocked by the inner hop controller. Specifically:

$$\lambda(\text{effective}) = \lambda(\text{total}) \times [1 - r(N)] \quad (3.6)$$

3.4 CONCLUSION

The lossless two hop system analyzed in this thesis effectively queues packets at user terminals in the outer hop by prohibiting outer hop transmissions when the buffer of its associated inner hop controller becomes full. Packets that arrive during the time which the controller's buffer is full are not lost. They will enter the system once buffer space is available at the inner hop controller and the outer hop channel is reset to idle. However, the mathematical loss model for the inner hop discards packets received under similar "buffer full" circumstances. Assuming that the arrival rate is $\lambda(\text{total})$, $\lambda(\text{effective})$ represents that portion

of $\lambda(\text{total})$ which is not blocked and hence may be used to approximate a lossless inner hop with arrival rate of $\lambda(\text{effective})$. In Chapter 6, $\lambda(\text{total})$ is used to obtain $r(N)$ and subsequently $\lambda(\text{effective})$. Simulation (lossless) results at $\lambda(\text{effective})$ are then compared to numerical (loss) results at $\lambda(\text{total})$ and show close agreement.

CHAPTER 4

DELAY INDUCED BY THE TDMA INNER HOP

4.1 INTRODUCTION

This Chapter defines the random time delay experienced by the CSMA_CD outer hops as a result of blocking induced by inner hop controller during buffer full conditions. The theory of residual life is used to approximate this delay and the corresponding Laplace transform is derived.

4.2 THE LAPLACE TRANSFORM OF RANDOM VARIABLE Θ

Random variable Θ represents the time period during which a controller blocks its associated outer hop due to buffer runaway. As discussed previously, the distribution of random variable Θ can be approximated using the theory of residual life [2] (page 172). Note that two independence assumptions are necessary when applying classical residual life theory. First, the frame time durations are independent and second, arrivals into the buffer of a controller are independent from the state of the system. The latter assumption is not quite true since the system under study inhibits packet arrival at state N where N represents the controller's buffer capacity. However, for reasons of analytical tractability, residual life is used to approximate the inner hop induced blocking delay.

Controller Buffer Capacity: 3 Packets

Figure 4.1 Residual Life Model of Random Variable θ

Since inner hop blocking does not occur in each TDMA frame, the residual life assumption must be unconditioned by the probability that the inner hop buffer is at state $N-1$ and a transmission has occurred.

Since the queuing system is embedded at fixed departure points, a packet arriving to an inner hop controller which observes $N-1$ buffered packets will cause the controller to send a busy tone to the terminals of the outer hop thus blocking packet transmissions. Given that this packet arrives between $T(k)$ and $T(k+1)$, where $T(k)$ and $T(k+1)$ represent successive departure epochs, the blocking time is approximated by the residual life time from packet arrival to the next packet departure epoch where the inner hop controller's buffer will again hold $N-1$ packets and outer hop blocking will cease. Thus the blocking time is affected by several system parameters such as the outer hop packet departure rate, inner hop buffer capacity and number of packets waiting in the queue of a controller. Recall that blocking starts when a packet arrives and finds $N-1$ packets in queue. Figure 4.1 illustrates the problem of deriving a distribution for random variable θ . The residual lifetime pdf, $f^{\sim}(y)$, is initially based on the condition that the system queue is at state $N-1$ and an arrival has occurred. To assist in this derivation, the following notation is introduced:

$f^{\sim}(y)$ = residual lifetime pdf

$$= \frac{1 - F(y)}{m(1)} \quad (4.1)$$

where $F(y)$ is the PDF of the time interval between
inner hop packet departures (T),

$m(1)$ is the first moment of

$T(k+1) - T(k)$; and,

$$m(n) = E [(T(k+1) - T(k))^n] \quad (4.2)$$

$$m(1) = T \quad m(2) = T^2 \quad m(3) = T^3 \quad (4.3)$$

$$H^{\sim*}(s) = \text{Laplace transform of } f^{\sim}(y) \quad (4.4)$$

$$F^*(s) = \text{Laplace transform of } F(y) \quad (4.5)$$

$$H^{\sim*}(s) = \frac{1 - F^*(s)}{s m(1)} \quad (4.6)$$

$$= \frac{1 - e^{-sT}}{sT}$$

$h^{\sim}(n)$ = nth moment of residual life given

that the system is in state $N-1$

and one arrival has occurred.

= nth derivative of $H^{\sim*}(s)$

evaluated at $s=0$

$$= \frac{m(n+1)}{(n+1) m(1)} \quad (4.7)$$

$$h^{\sim}1 = \frac{m(2)}{2m(1)} = \frac{T}{2} \quad (4.8)$$

$$h^{\sim}2 = \frac{m(3)}{3m(1)} = \frac{T^2}{3} \quad (4.9)$$

$H^{\sim*}(s)$, $h^{\sim}1$, and $h^{\sim}2$ may be unconditioned to $H^*(s)$,

$h1$ and $h2$ as follows:

$$H^*(s) = \tilde{H}^*(s) [r(N-1)] [1-r(0)] \quad (4.10)$$

= unconditional Laplace transform of
random variable Θ

h_1 = first derivative of $H^*(s)$ evaluated at
 $s=0$

h_2 = second derivative of $H^*(s)$ evaluated at
 $s=0$

where $r(N-1)$ is the probability that the inner hop buffer is at state $N-1$, and $[1-r(0)]$ is the probability that there is a transmission by the outer hop. $r(0)$ and $r(N-1)$ are obtained using the Markov chain analysis described in Chapter 3.

4.3 CONCLUSION

The analysis of random variable Θ , namely $H^*(s)$, h_1 and h_2 , forms an important part of the outer hop's average delay versus throughput result. In Chapter 5, in order to reflect interdependence, the Laplace transform of the distribution of the number of arrivals during random variable Θ is incorporated into the analysis of the outer hop and the expected number of ready users in the outer hop is obtained. Little's result will then be employed to obtain a numerical value for outer hop expected delay.

CHAPTER 5

OUTER HOP ANALYSIS

5.1 INTRODUCTION

This chapter will describe the analytical approach used for calculating expected delay in the outer hop. This model is based on Lam's analysis of CSMA_CD [20] as modified by Niktash et al [4] to include random outer hop delay caused by the inner hop controller during buffer full conditions. The following sections will describe the outer hop performance analysis techniques presented in [4].

5.2 CSMA_CD PROTOCOL DESCRIPTION

The CSMA_CD outer hop is synchronized into time slots of duration 2τ where " τ " is the maximum end to end propagation delay of the network. Therefore, in the worst case situation, a collision will be detected, aborted and the channel cleared within 2τ seconds. User terminals attempt to transmit at the start of a time slot. If a user terminal is ready, i.e. it has one packet in queue, it senses the channel:

- a. If the channel is sensed idle the terminal transmits with probability one.

- b. If the channel is sensed busy for whatever reason (transmission, collision, abort, controller buffer full), the terminal waits and continues to sense the channel at start of slot. Transmission commences as above when the channel is sensed idle. This variation is more commonly known as 1-persistent CSMA_CD.
- c. If a collision is detected during transmission the user terminals will immediately abort their respective transmissions. Each user will use an adaptive backoff algorithm for determining its transmission probability in the next time slot. This algorithm is based on initially transmitting with probability one and after each collision, reducing this probability through multiplication by 0.5.
- d. If the inner hop controller experiences a buffer full condition, it will apply a busy tone to the outer hop as indicated previously and thus prohibit further transmissions from user terminals until at least one packet is removed from its buffer.

5.3 THE CSMA_CD PROTOCOL ASSUMPTIONS

Processing delay and carrier sense time are assumed to be negligible. Retransmissions caused by sources other than collisions are also negligible and will be ignored.

The source of traffic to the outer hop is created by an infinite population of users which together form an independent Poisson process with a mean packet generation rate of λ packets per second. This assumption is used to approximate a finite number of user terminals which originate packets at a relatively infrequent rate so that there is no queuing of packets at user terminals. In order to achieve an expected delay which is less than infinity, the overall throughput must be less than the theoretical maximum for the CSMA_CD network involved. For example, a CSMA_CD network where the "a" value or ratio of bit propagation time to packet transmission time is 0.1, the maximum throughput (arrival rate)*(packet transmission time) is approximately 0.62.

Each user has a queue of one packet and hence the generation of a new packet is the same as increasing the number of ready user terminals by one. Packets arrive and depart one at a time. Ready users form a distributed queue with random service order thus the transmission time of each packet which includes physical packet transmission (fixed time) and channel assignment delay (random time) is

Figure 5.1 A Snapshot of the Outer Hop Channel

an independent, identically distributed random variable. The notion of randomness and independence in channel assignment delay is supported by the assumption of memoryless Poisson arrivals to the distributed queue as well as the random, exponential backoff algorithm which is employed during collision situations.

The outer hop has separate transmit and receive paths. Inner hop controller busy tones will only be applied to the input (transmit) path. The output (receive) path is considered to be an uncontested broadcast channel where user terminals examine each packet and retain those which contain an address matching their own.

5.4 OUTER HOP ANALYTICAL OVERVIEW

The assumptions of Poisson arrivals and single packet transactions (transmit and receive) permit systems statistics calculated by Markov chain analysis at departure epochs to be valid for all points in time. Initially, a Markov chain will be established with departure times or epochs embedded at the instances where a packet has been successfully transmitted and propagated to all user terminals. Figure 5.1 illustrates activity on the inner hop channel at a specific point in time. Using the assumption which equates the number of packets in the system with the number of ready users, the network

statistic under scrutiny is the number of ready users in the system. The following terms are introduced to clarify figure 5.1:

System state = Q_n

= the number of ready users
in an outer hop at time point n .
"n" is a number which increases
sequentially and this increase takes
place immediately after each departure
epoch (packet transmission)

$$= Q_{(n-1)} + U_n + V_n + W_n - 1 \quad (5.1)$$

where U_n = the random number of packets which
arrive during the channel
assignment delay following the
successful transmission of packet
 $C_{(n-1)}$

V_n = the random number of packets which
arrive during the transmission
of packet C_n

W_n = the random number of packets which
arrive during inner hop blocking
of the outer hop

- 1 reflects the transmission of packet C_n and its subsequent removal from queue

The value of Q_n is influenced by three factors:

- a. The probability that the system is in state $Q_{(n-1)}$,
- b. the random time interval T between $Q_{(n-1)}$ and Q_n (i.e the time between successful packet transmissions), and
- c. the Poisson probability of k arrivals during a fixed time slot $= 2\tau$

Assuming that the network is stable, i.e. the product of packet arrival rate and total transmission time is less than 1, the distribution of the random variables Q_n , $Q_{(n-1)}$, U_n , V_n and W_n will reach a steady state distribution. The probability that the system is in state Q_n will equal that of $Q_{(n-1)}$ as $n \rightarrow \infty$. Before solving for equation 5.1 the z transforms for random variables V_n , U_n and W_n will be derived.

As stated earlier, V_n = random number of packets which arrive during the transmission of packet C_n .

$V(z)$ = the z transform of V_n

$$= E [z^{V_n}] = \sum_{k=0}^{\infty} P [V_n = k] z^k \quad (5.2)$$

$$P [V_n = k] = P [k \text{ arrivals in fixed time } X + \tau] \\ * P [\text{time } X < x]$$

$$= \sum_{k=0}^{\infty} \frac{(\lambda X)^k e^{-\lambda X}}{k!} \\ * \int_{x=0}^{\infty} b(x) dx \quad (5.3)$$

where $b(x) dx$ is the pdf of the packet transmission time which includes " τ " seconds for the time it takes for all stations to sense the channel idle.

The Laplace transform of $b(x) dx$ is

$$B^*(s) = e^{-s(T+\tau)} \quad (5.4)$$

with first moment = $b_1 = T + \tau$ and

second moment = $b_2 = T + 2T\tau + \tau^2$

therefore,

$$V(z) = \int_{x=0}^{\infty} e^{-\lambda x} e^{\lambda x z} b(x) dx \quad (5.5) \\ = \int_{x=0}^{\infty} e^{-(\lambda - \lambda z)x} b(x) dx \\ = B^*(\lambda - \lambda z) \\ = \text{the Laplace transform of the packet} \\ \text{transmission time evaluated at } s = \lambda - \lambda z$$

It should be noted that the first derivative of $B^*(\lambda - \lambda z)$ will yield an expression for the first moment of V_n and when

evaluated at $z=1$ will produce the expected value or mean of V_n .

The z transforms for U_n and W_n are derived in a similar fashion. This time two independent random variables are involved:

$$\begin{aligned} U(z) &= \text{the } z \text{ transform of } U_n \\ &= E [z^{U_n}] = \sum_{k=0}^{\infty} P [U_n = k] z^k \end{aligned} \quad (5.6)$$

$$\begin{aligned} P [U_n = k] &= P [k \text{ arrivals in random time } Y] \\ &\quad * P [\text{random time } Y < y] \end{aligned} \quad (5.7)$$

where Y = channel idle time +
collision resolution time
and pdf $Y = c(x)$

$$U(z) = C^*(\lambda - \lambda z)$$

The Laplace transform of $C^*(s)$ is a more involved procedure since there are three mutually exclusive scenarios which could exist:

- a. The outer hop is idle and channel assignment will be immediate upon the arrival of the first packet. In terms of time slots or transmission opportunities:

$$\begin{aligned}
 P\{Z_n = k\} &= P\{\text{idle period} = k \text{ slots}\} \\
 &= (1-P_0) P_0^{(k-1)} \quad (5.8)
 \end{aligned}$$

where $P_0 = P\{\text{zero arrivals in one slot}\}$

The start of transmission or channel assignment delay due to channel contention will clearly not occur in this situation.

- b. The outer hop has one message for transmission thus channel assignment is immediate with no contention or idle periods.
- c. There is more than one message in the system, i.e. two or more terminals will attempt transmission. This is the inverse of a. in that the idle period will be zero and collision resolution time will now determine overall channel assignment delay. In mathematical terms:

$$P\{R_n = k\} = \sigma(1 - \sigma)^{(k-1)} \quad (5.9)$$

where $P\{R_n = k\} = P\{k \text{ slots are required to assign the channel during collision resolution}\}$

and $\sigma = P\{\text{successful transmission}\}$

therefore,

$$P(R_n = k) = P\{\text{no success in } (k-1) \text{ slots}\} \quad (5.10)$$

$$* P\{\text{success in } k\text{th slot}\}$$

The random variable σ is obtained by assuming that at the beginning of a time slot ready controllers transmit with equal probability and in a busy system where all N controllers are assumed to be busy, the probability σ that one controller transmits successfully is:

$$\sigma = (1 - 1/N)^{(N-1)} \quad (5.11)$$

$$= P\{N-1 \text{ controllers do not transmit}\}$$

In order to derive the Laplace transform of the collision resolution period, the system state at departure epoch " n " or Q_n must be greater than or equal to two. For $Q_n \geq 2$ there is no channel idle time and $C^*(s)$ is obtained by transforming the expression for R_n and σ , equations 5.9 and 5.11 respectively:

$$C^*(s) = \frac{\sigma e^{-s\tau}}{1 - (1-\sigma) e^{-s\tau}} \quad (5.12)$$

By taking the first and second derivatives of $C^*(s)$ and evaluating the result at $s = 0$, the moments of U_n are obtained to be [4]:

$$(5.13)$$

1st moment: $2\tau/\sigma$

2nd moment: $(2\tau)^2 ((2-\sigma)/\sigma^2)$

The number of arrivals during random time period Θ

involves two random variables, Θ and the Poisson probability of k arrivals during random variable random variable Θ and is denoted by W_n .

$$W(z) = E [z^{W_n}] = \sum_{k=0}^{\infty} P [W_n = k] z^k \quad (5.14)$$

$$P [W_n = k] = P [k \text{ arrivals in random time } \Theta]$$

* $P[\text{random time } \Theta < \text{a given time } x]$

where Θ = the time period during

which the inner hop controller

prohibits outer hop packet

transmissions

the pdf of random variable Θ is $h(x)$ and is derived in Chapter 4.

Using the technique previously described for $V(z)$ the Laplace transform of $W(z)$ is determined to be $H^*(\lambda - \lambda z)$. $H^*(s)$ and the first two moments h_1 and h_2 were obtained in the latter part of Chapter 4 using the theory of residual life and appear as equations 4.1 and 4.2 respectively. Note again that these values are calculated using steady state queue probabilities of the loss TDMA model and require adjustment to reflect those instances where inner hop blocking actually occurs.

The packet transmission time and the delay due to channel blocking are independent random variables and since our system

is embedded at departure epochs, the unconditional mean of random variable θ represents the steady state time period by which each packet transmission is prolonged due to inner hop blocking. This effective outer hop packet transmission time may be viewed as the sum of two independent variables, θ and $T+\tau$ and will be referred to as random variable J with Laplace transform $J^*(s)$:

$$\begin{aligned} J^*(s) &= H^*(s)B^*(s) \\ &= e^{-s(b_1+h_1+\tau)} \end{aligned} \quad (5.15)$$

$$\text{with first moment } j_1 = b_1 + h_1 \quad (5.16)$$

$$\text{and second moment } j_2 = (b_1 + h_1)^2$$

As before, the probability of "k" Poisson arrivals during random variable J is another random variable with Laplace transform $J^*(\lambda - \lambda z)$.

Rewriting 5.1 by incorporating random variable j results in the following:

$$Q_n = Q_{(n-1)} + U_n + J_n - 1 \quad (5.17)$$

Assuming that limiting random variables Q , U and J exist, an expectation for Q_n may be created:

$$(5.18)$$

$$E(z^{Q_n}) = E(z^{Q_{(n-1)}+U_n}) * E(z^{J_n}) * E(z^{-1})$$

$E(z^{J_n})$ is given as equation 5.15. $E(z^{Q_{(n-1)}})$ and $E(z^{U_n})$ are dependent random variables and determined by the state of the system at departure epochs n and $(n-1)$. Using equations

5.6 to 5.13 inclusive the following expression is derived for $E(z^{[Q(n-1)+U_n]})$ [4,23]:

$$\begin{aligned}
 E(z^{[Q(n-1)+U_n]}) = & Q(0) \{E(z^X)E(z^Y) - \\
 & P[X=0]E(z^Y) - z(P[X=1]E(z^Y)) \\
 & + z(P[X=1])\} + Q(1)z \\
 & + \sum_{k=2}^{\infty} Q(k)z^k E(z^Y) \quad (5.19)
 \end{aligned}$$

where random variable X represents the number of arrivals during the last slot of the idle period and random variable Y represents the number of arrivals during busy or collision time periods. $Q(0)$ and $Q(1)$ are the probabilities that $Q_n = 0$ and 1 as " n " approaches infinity. Appendix F contains a detailed derivation of $E(z^{[Q(n-1)+U_n]})$ which was used by Niktash in [4].

The z transform of Q_n , the number of packets in the system at time departure epoch n , is defined as:

$$Q(z) = \sum_{k=0}^{\infty} Q(k) z^k$$

$$\text{where } Q(k) = \lim_{n \rightarrow \infty} P[Q_n = k]$$

Substituting 5.19 and 5.15 into 5.18 and combining various terms results in the following:

$$\begin{aligned}
Q(z) = & J^*(\lambda - \lambda z) \{ Q(1) z[1 - C^*(\lambda - \lambda z)] + \\
& \frac{Q(0)}{1 - P(0, 2\tau)} [P(1, 2\tau) z(1 - C^*(\lambda - \lambda z)) - \\
& C^*(\lambda - \lambda z) (1 - e^{-2\tau\lambda(1-z)})] \} \\
& \times [z - J^*(\lambda - \lambda z) C^*(\lambda - \lambda z)]^{-1}
\end{aligned} \tag{5.20}$$

$$\text{where } Q(0) = \frac{1 - \lambda(j_1 + \tau + 2\tau/\sigma)}{(2\tau)\lambda \left\{ \frac{1}{(1 - P(0, 2\tau))} - \frac{1}{J^*(\lambda)\sigma} \right\}} \tag{5.21}$$

$$\text{and } Q(1) = Q(0) \left\{ \frac{1}{J^*(\lambda)} - \frac{P(1, 2\tau)}{1 - P(0, 2\tau)} \right\} \tag{5.22}$$

Little's result may be applied to derive an expression for expected outer hop packet delay D:

$$\begin{aligned}
D = & j_1 + 2\tau + 2\tau/\sigma \\
& - \frac{1 - P(0, 2\tau)}{2[J^*(\lambda)\sigma - (1 - P(0, 2\tau))]} (2/\lambda - 4\tau) \\
& + \frac{\lambda[(j_2 + 2j_1 + 2\tau(j_1) + \tau^2) + 2(j_1 + \tau)(2\tau/\sigma) + 4\tau^2(2 - \sigma)/\sigma^2]}{2[1 - \lambda(j_1 + \tau + 2\tau/\sigma)]}
\end{aligned} \tag{5.23}$$

5.5 CONCLUSION

Outer hop packet delay is the time interval between packet generation at a user terminal and successful reception by the inner hop controller. Equation 5.23 will be used to calculate the expected outer hop packet delay. Two hop system

expected delay will then be obtained by adding the outer hop average delay to the queuing and transmission delay of the inner hop. This process will be repeated for various packet arrival rates and data transmission speeds. Chapter 6 compares these numerical values to the corresponding simulation results.

CHAPTER 6
TWO HOP CSMA_CD/TDMA SYSTEM
NUMERICAL CALCULATIONS AND SIMULATION RESULTS

6.1 INTRODUCTION

In this Chapter the numerical results for system expected delay will be compared to results obtained by simulation. The analytical methodology is reviewed and various programs which were used in the data gathering process are introduced. The results are compared graphically and discrepancies explained in the accompanying text. As a point of interest, the final series of graphs compare the performance of the CSMA_CD/TDMA network modelled in this thesis to the CSMA_CD/CSMA_CD system analyzed by Niktash et al [4] using identical inner and outer hop parameters.

6.2 CALCULATION OF SYSTEM EXPECTED DELAY

System expected delay is calculated using GW BASIC programs which are executed using the double precision mathematics option. Appendices A.1.1, A.1.2, A.2 and A.3 contain the various programs used in these calculations. As mentioned previously, the general approach was to decouple the inner and outer hops, form an expression for the impact (blocking) of the inner hop and convert this expression into

a delay random variable which would then be incorporated into the outer hop delay calculation. Using the equations generated in Chapters 3, 4 and 5, the inner hop delay is obtained as follows:

- a. Run the programs contained in Appendix A.1.1 and Appendix A.1.2 which calculate the inner hop queue length probabilities for empty and busy systems.
- b. Run the program contained in Appendix A.2 using the queue length probabilities obtained in a. above. Fill the matrix according to the system parameters and buffer size required. Multiply the resulting matrix by itself until a convergence is achieved. Calculate the inner hop expected delay and note the probability of $(N-1)$ messages in queue for each case.
- c. Repeat a. and b. above for each value of traffic throughput and buffer size.

The outer hop delay may now be calculated by running the program in Appendix A.3. Upon supplying the propagation delay, and outer/inner hop packet transmission times, the program calculates outer hop delay using $P(N-1)$ and throughput

values supplied. The delay equation (5.23) of Chapter 5 is used to perform this calculation. Total system delay is the sum of inner and outer hop delays.

6.3 TWO HOP CSMA_CD/TDMA SYSTEMS UNDER STUDY

Two system configurations are chosen and in order to simplify comparison of results obtained in this thesis with the CSMA_CD/CSMA_CD network studied in [4], similar system parameters have been selected. The first system under study will be referred to as system 'A' and has the following parameters:

- a. A 1.0 Mbps TDMA inner hop which interfaces 10 CSMA_CD outer hops at 0.1 Mbps each.
The propagation delay has been calculated based on the assumption that the transmission medium is cable.
- b. Packet transmission time is 0.01 sec (1000 bit packets) on the outer hops and 0.001 sec on the inner hop. Total TDMA frame time for 10 inner hop controllers is 0.01 sec.
- c. A 20 km outer hop is simulated using a propagation time of 0.0001 for "a" = 0.01

which should allow the outer hops to sustain a throughput of approximately 0.9.

This system is inherently stable since the combined throughput of 10 outer hops at 0.9 generates a total throughput of 0.9 for the inner hop. Detailed SLAM II code is contained in Appendix B.1. Although System 'B' is shown in this Appendix, it may be easily modified to perform System 'A' simulation by changing the packet and frame transmission intervals.

The second system under study will be referred to as system 'B' and has the following parameters:

- a. A 150 Kbps TDMA inner hop which interfaces 10 CSMA_CD outer hops at 150 Kbps each. The transmission medium is free space.
- b. Packet transmission time is 0.00033 sec (50 bit packets) on the outer hops and 0.00033 sec on the inner hop for a total TDMA frame time of 0.0033 sec.
- c. A 10 km outer hop is simulated using a propagation time of 0.000033 sec for an alpha value of $0.000033/0.0033 = 0.1$ which should allow the outer hops to

sustain a throughput of approximately 0.6.

This system could become unstable if the combined throughput of 10 outer hops exceeds a total throughput of 1.0 for the inner hop. This would occur if each outer hop reached an input throughput of greater than 0.1. Appendix B.1 is a sample System 'B' program.

6.4 SIMULATION

Appendix B.1 contains the SLAM II simulation code and the FORTRAN user functions used to study two different CSMA_CD/TDMA wide area networks. The two hop simulation programs are essentially the standalone TDMA system described in Chapter 2 merged with the optimized CSMA_CD network explained in the same Chapter. Some modifications were required to incorporate the inner hop/outer hop blocking capability during inner hop buffer full conditions. In order to achieve the highest degree of accuracy and CPU efficiency during simulation the following method was used:

- a. A short (100) packet trace was taken for a heavily loaded system. The packet starting times and outer hop queue lengths were continuously monitored during outer hop collisions and outer hop blocking during inner hop buffer full

situations. The objective was to visually verify that the simulation program implemented the CSMA_CD/TDMA protocol described in Chapters 3 and 4.

- b. The length of simulation in terms of packets transmitted was then established by running the same simulation program for lengths of 500, 1000 2000, 4000 and 8000 packets. Results at 2000 4000, and 8000 packets were nearly identical, therefore a length of 2000 packets was chosen for all two hop simulation trials.
- c. For inner hop intensities of 0.2, 0.4, 0.6, 0.8 and 1.0, each network simulation was run 10 times using 10 different random number seeds. The sample variance and confidence interval was calculated using the procedure contained in Appendix E. The simulated mean value for expected delay was obtained, plotted and compared to numerical results for each configuration.

6.5 RESULTS FOR SINGLE HOP TDMA AND CSMA_CD SYSTEMS

The outer hop simulation for CSMA_CD was executed using the time values as described previously for systems 'A' and 'B'. However, for both simulations and system 'A' in particular, the observed arrival rate was much higher than specified. The resulting throughput caused system instability to occur at a throughput of 0.6. In order to achieve a finer resolution when examining inter-arrival times, the packet transmission times were raised to 1.0 from 0.00033 sec with a corresponding adjustment in slot and TDMA frame transmission times. When run in this fashion the standalone TDMA and CSMA_CD simulations compared favourably with numerical predictions.

In figures 6.1 and 6.2 the TDMA network parameters have been changed to match system 'A' and 'B' values. Expected delay results for TDMA simulation are compared to numerical results obtained using the equations derived in Appendix D. Although these equations yield the same results as those obtained by Yan [21], they are of a different form and, since the Appendix D formulae were developed as part of this thesis, they are used to calculate the inner hop numerical results for systems 'A' and 'B'. Of interest in figures 6.1 and 6.2 is the delay encountered over the same TDMA inner hop when operating in a two hop CSMA_CD/TDMA environment. The obvious

discrepancies will be discussed later during the analysis of two hop results.

Figures 6.3 and 6.4 display the results of simulation versus numerical analysis for standalone CSMA_CD in the system 'A' and 'B' configurations. Again, an excellent correspondence is achieved using the expected delay formula derived in Chapter 5 with random variable Θ (inner hop blocking) set to zero. Figures 6.5 and 6.6 compare the standalone CSMA_CD results (infinite queue) to the outer hop delay results obtained for systems 'A' and 'B' using various buffer sizes (2, 3, and 5). As anticipated, for the same throughput values, outer hop expected delay increases as the inner hop buffer size decreases due to the impact of inner hop blocking.

6.6 TWO HOP SIMULATION RESULTS FOR SYSTEM 'A'

In the first two hop system 'A' configuration examined, each inner hop controller has a buffer capacity of 2 packets. Figures 6.7 and 6.8 show average outer and inner hop delay versus throughput. It is apparent that there is a discrepancy between the numerical predictions and the results of simulation and these discrepancies become more severe as the throughput increases. As stated earlier in the system 'A' definition there is very little chance of inner hop blocking since the outer hop packet transmission time is the same as

the inner hop TDMA frame time. The discrepancy lies in the mathematical model since the assumption of Poisson arrivals is false in all cases where the inner hop capacity is greater than or equal to the sum of the capacities of the outer hops. Numerically, the inflated arrival rate assumption results in a higher probability of inner hop blocking and raises the expected value for inner hop delay.

Similarly, as discussed in Chapter 5, the expected value of random variable Θ is conditioned by $P(N-1) \cdot [1-P(0)]$ i.e. the probability that the system is in state $N-1$ and the probability that an arrival has occurred. Since these Poisson based probabilities are also exaggerated, as shown by figure 6.11, the resulting outer hop delay due to inner hop blocking becomes increasingly larger as throughput increases and diverges considerably from the results of simulation which only shows a slight increase at high throughput.

The first and second moments of random variable Θ for this configuration are plotted in figures 6.9 and 6.10. Since the outer hop packet transmission time is the same as the inner hop frame transmission time, inner hop blocking will almost never occur in a controller with a buffer capacity of 2 packets and will never occur in a controller with a buffer capacity of 3 or more packets. For a two packet buffer, a packet from the outer hop must arrive during the transmission of a single packet on the inner hop to cause a brief blocking condition which will be reset once the inner hop transmission

is complete. At low intensities there are very few instances of inner hop blocking since arrivals from the outer hop are much less frequent. At higher throughputs there are more arrivals and more cases where a second arrival occurs during inner hop packet transmission. Residual life theory does not take these factors into account and this explains the large discrepancies between numerical and simulation results.

Figures 6.12, 6.13, 6.19 and 6.20 have 95% confidence intervals indicated for each simulation result. In system 'A' average system delay does not suffer from the difference between simulation and numerical results for random variable θ since there are very few instances where the system is at state $(n-1)$. Figure 6.12 shows average system delay versus throughput for system 'A' with a 2 packet buffer. Clearly at high throughput values there is a considerable discrepancy between both results with errors in the mathematical assumptions accounting for all of the differences.

In order to more closely approximate the simulation program, the inner hop is modelled numerically as a fixed time interval which is the sum of the expected residual lifetime and the inner hop slot duration $(T/2 + T/M)$. Blocking probability is considered negligible and ignored. Figure 6.13 shows close agreement between simulation and this modified mathematical model which may be used in all cases where the inner hop frame transmission time is less than the outer hop packet transmission time. The numerical results for expected

delay now lie well within the 95% confidence intervals calculated for each group of delay values obtained through simulation. The effects of inner hop blocking are moderated by increased inner hop controller buffer capacity as shown by figures 6.14 to 6.19 which compare the same system characteristics for System 'A' with a 3 packet buffer. The main difference between the 2 and 3 packet buffer systems is the blocking probability simulation result which has now shrunk to zero as well as the simulation results for the first and second moments of random variable Θ which are also zero. With outer hop packet transmission time equal to inner hop total frame transmission time it is physically impossible to have more than 2 packets in the inner hop buffer.

In the numerical model, higher capacity buffers reduce the blocking probabilities at higher intensities and therefore the 3 packet numerical results more closely correspond to simulation as illustrated in figure 6.19. Using the same fixed time interval to model inner hop delay as described previously results in near perfect agreement.

Figure 6.20 is a graph of average system delay versus throughput for System 'A' using a 5 packet buffer and confirms the theory that higher capacity buffers will result in lower inner hop blocking probabilities and closer agreement between the original mathematical model and simulation.

Figure 6.5 Infinite Population CSMA_CD System Average Delay vs. Throughput For Inner-Hop Buffer Capacities Of 2,3,5 and Infinite Packets

The rationale for lower numerical results is confirmed by figures 6.23 and 6.24 where first and second moments of random variable Θ are shown to be lower than those achieved through simulation. Figure 6.25 illustrates the dramatic difference between numerical and simulated values of $P(N-1)*(1-P(0))$ or $P(\Theta)$ with simulation results significantly larger than numerical results at high throughput values.

The differences between the simulation model which exactly implements the two hop CSMA_CD/TDMA protocol as described in this thesis and the numerical model are shown in figure 6.35. The arrival rate to the inner hop controller is λ_i and reflects the initial arrival rate λ_1 less the collisions or aborted transmissions. That is,

$$\lambda_e = \lambda_1 - \lambda_c$$

Inner hop blocking can also occur and has a positive effect on the arrival rate λ_e and a similar effect on input traffic throughput. In the numerical model the outer hop delay is increased by a factor based on the inner hop "busy" condition or $P(N-1)$ but inner hop expected delay which forms the major delay component of System 'B' is calculated on a loss system which totally disregards all packets generated when the inner hop controller is at state "N" thus decreasing the ready user population and the expected packet delay.

In order to compensate for the delay lessening effects of this mathematical model, the single hop TDMA loss system of Yan [21] is used instead to approximate the lossless two hop CSMA_CD/TDMA system described in Chapter 3. The procedure to adapt [21] is as follows:

- a. Using the results of numerical analysis for a given throughput and buffer size, obtain the blocking probability (equation D.12).
- b. Calculate an effective simulation throughput by assuming that the numerical analysis throughput is based or conditioned on blocked messages not forming part of the input traffic load. i.e.

$$\begin{aligned} \text{Effective simulation throughput} &= \\ \text{Numerical throughput} &\times (1 - P[\text{Blocking}]) \end{aligned}$$

- c. Measure expected simulation delay at the effective throughput and compare these values to numerical results for expected delay at the original throughput values.

Figure 6.26a illustrates the reasonably close agreement which occurs between simulation and numerical results when effective throughput is used. At lower intensities the

numerical values are a close estimate for simulated results, the inherent assumptions provide a worst case estimate for expected delay up to a throughput of 0.6 where simulation overtakes numerical results and at 1.0 is approximately 20% higher. The reason for this phenomenon involves the residual life lengthening effect which occurs in simulation and is not accounted for by numerical assumptions during buffer full conditions. A packet in simulation, once the channel is reset idle by the inner hop controller, will be transmitted by the outer hop after a random number of time slots where one slot = one propagation delay. Since the frame time is much greater than the outer hop propagation time, the actual residual lifetime of the inner hop "time to next transmit slot" period will be much closer to T (frame time) than $T/2$ as calculated in Chapter 4. This will cause observed values of inner hop blocking to be larger than numerical predictions and this effect will be extended to overall delay.

Figure 6.26b demonstrates the difference between the numerical results when a worst case residual life of T is used in average calculations as opposed to the original value of $T/2$. There is a much closer agreement at high throughput and a good agreement, again worst case, at lower throughput rates. For reasons discussed previously, the two hop simulation tends to distort the original arrival rate or packet generation process in the outer hop by assuming a 0.367 fixed throughput

when more than one terminal is ready and a collision is imminent.

In both figures 6.26a and 6.26b, the effective numerical throughput as calculated by $(\text{Total throughput}) \times (1 - \text{blocking probability})$ is shown directly beneath the total throughput used in numerical calculations. The expected delay values shown for simulation are those obtained by extrapolating the simulation results obtained at specific throughputs (e.g. 0.2, 0.4, 0.6, 0.8). An approximate simulation delay result is then determined for the effective numerical throughput value (e.g. 0.751) under consideration and plotted as a single point.

Figures 6.26b, 6.33 and 6.34 have 95% confidence intervals plotted for each simulation result. Since there were few instances of inner hop blocking at lower throughput values the total system expected delay results obtained were very consistent and, as a result, the respective confidence intervals were very small and could not be plotted in some cases.

In order to examine an inner hop lossy TDMA protocol, the blocking mechanism was removed in the simulation program and the program was further modified to discard any packets which were generated in the outer hop during buffer full conditions. The revised program was then re-run at intensities of 0.2, 0.4, 0.6, 0.8, and 1.0 and compared to numerical results without compensating for effective intensity as before.

Figure 6.27 illustrates the very close agreement between the lossy mathematical model and the lossy simulation program.

As observed with System 'A' an increase in the inner hop buffer size tends to decrease the differences between mathematical and simulation models. Figures 6.28 to 6.32 show average inner/outer hop delay and the first and second moments of random variable θ for a 3 packet System 'B'. Differences in these graphs occur for the same reasons as those in the 2 packet 'B' System. Figures 6.33 and 6.34 show System 'B' average delay for 3 and 5 packet buffer configurations. The process of estimating effective throughput was applied to both graphs and clearly there is excellent agreement between the values with numerical results slightly higher than simulation. This is a desirable situation if the numerical model is to be used as a close approximation to simulation.

Figure 6.36 is a general comparison graph which illustrates the characteristics of the numerical model for different buffer capacities. The upper graphs show that the total average delay increases in direct proportion to the inner hop buffer size due to increased queuing delay. At the same time, the lower graphs indicate that the outer hops experience less delay as inner hop buffer size increases since there are fewer buffer full conditions encountered by the inner hop controller. It should be noted that the expected delays are plotted on a logarithmic scale hence one should be conscious when, for instance, comparing the rate of average

outer hop delay with the rate of its associated total delay. Although the difference is shown to be minor, the scale of the upper graphs are ten-fold larger than that of their lower counterparts. Hence, the value of the rates of the total delay are larger than the associated rates of the outer hop delay.

6.8 COMPARISON BETWEEN CSMA_CD/TDMA AND CSMA_CD/CSMA_CD TWO HOP SYSTEMS

As mentioned before, Niktash et al [4] modelled a CSMA_CD/CSMA_CD two hop system using two network configurations which match the 'A' and 'B' systems examined in this thesis. Figure 6.37 compares two hop expected delay results for CSMA_CD/CSMA_CD and CSMA_CD/TDMA networks which have a two packet buffer controller. Numerical and simulation results are shown for the CSMA_CD/TDMA network. Taking into account the underlying assumptions made for these systems, the total expected delay of the CSMA_CD/CSMA_CD network is lower than the CSMA_CD/TDMA network up to a throughput of 0.5. This is due to the ability of a CSMA_CD inner hop controller to transmit each packet as it arrives and not wait for a designated time slot as in a TDMA controller.

After a throughput of 0.5 however, the CSMA_CD inner hop delay begins to increase rapidly ("a" = 0.1) due to excessive collisions and eventually becomes infinite at a throughput of

0.62. TDMA simulation, on the other hand, with a CSMA_CD outer hop at "a" = 0.01 is able to function effectively at a throughput of 0.8 and slightly beyond. Figure 6.38 repeats the comparison for a 3 packet buffer configuration.

Figures 6.39 and 6.40 perform the same comparison for 'B' systems. Again, CSMA_CD/CSMA_CD provides lower expected delay up to a throughput of 0.5 where it rises above TDMA. It should be noted that for System 'B' with a TDMA inner hop, the outer CSMA_CD hops could only run at a maximum throughput of 0.1 since the 10 outer hops were each as fast as the inner hop and instability would occur at higher throughput. In contrast, CSMA_CD inner hops could support higher individual outer hop transmission rates due to CSMA_CD's inherent ability to transmit packets immediately on the inner hop. But, as with TDMA, a System 'B' CSMA_CD inner hop could not process a total outer hop throughput greater than its own without becoming unstable.

6.9 CONCLUSION

A closed form equation for calculating system delay in a two hop CSMA_CD/TDMA network is not achievable using the M/G/_ modelling approach for the inner hop. Two separate mathematical procedures for stable and unstable two hop configurations have been developed and verified by simulation.

Figure 6.1 Buffered TDMA System Average Delay vs.
Average Input Arrival Rate

Figure 6.2 Buffered TDMA System Average System Delay vs. Average Input Arrival Rate

Figure 6.3 Infinite Population CSMA_CD System Average Delay vs. Throughput

Figure 6.4 Infinite Population CSMA_CD System Average Delay vs Throughput For Throughput Less Than .1

Figure 6.5 Infinite Population CSMA_CD System Average Delay vs. Throughput For Inner-Hop Buffer Capacities Of 2,3,5 and Infinite Packets

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Figure 6.6 Infinite Population CSMA_{CD} System Average Delay vs. Throughput For Inner-Hop Buffer Capacities of 2,3,5 and Infinite Packets

Figure 6.7 Average Outer Hop Delay vs. Throughput

Figure 6.8 Average Inner Hop Delay vs. Throughput

Figure 6.9 First Moment of RV θ vs. Throughput Figure 6.10 Second Moment of RV θ vs. Throughput

Figure 6.11 Inner hop blocking probability vs throughput

Figure 6.12 Average Two-Hop CSMA_CD/TDMA System Delay vs. Throughput

Figure 6.13

CSMA CD/TDMA Two Hop System: Average System Delay vs. Throughput With Inner Loop modelled numerically as a fixed time ($T/2 + T/M$)

Figure 6.14 Average Outer Hop Delay vs. Throughput

Figure 6.15 Average Inner Hop Delay vs. Throughput

Figure 6.16 First Moment of RV θ vs. Throughput Figure 6.17 Second Moment of RV θ vs. Throughput

Figure 6.18 Inner hop blocking probability vs throughput

Figure 6.19 Average Two-Hop CSMA_CD/TDMA System Delay vs. Throughput

Figure 6.20 Average Two-Hop CSMA_CD/TDMA System Delay vs. Throughput

Figure 6.21 Outer Hop Delay vs. Throughput

Figure 6.22 Inner Hop Delay vs. Throughput

Figure 6.23 First Moment of $RV \theta$ vs. Throughput Figure 6.24 Second Moment of $RV \theta$ vs. Throughput

Figure 6.25 Inner hop blocking probability vs throughput

Figure 6.26a Average Two-Hop CSMA_CD/TDMA System Delay vs. Throughput

Figure 6.26b Average Two-Hop CSMA_CD/TDMA System Delay vs. Throughput Worst Case Comparison

Figure 6.27 Average Two-Hop CSMA_CD/TDMA System Delay Using a Blocking (Loss) Inner Hop Simulation

Figure 6.28 Outer Hop Delay vs. Throughput

Figure 6.29 Inner Hop Delay vs. Throughput

Figure 6.30 First Moment of RV θ vs. Throughput

Figure 6.31 Second Moment of RV θ vs. Throughput

Figure 6.32 Inner hop blocking probability vs. throughput

Figure 6.33 Average Two-Hop CSMA_CD/TDMA System Delay vs. Throughput

Figure 6.34 Average Two_Hop CSMA_CD/TDMA System Delay vs. Throughput

ARRIVAL PROCESS - MATHEMATICAL MODEL

Figure 6.35 Arrival Processes

Figure 6.36 Comparison of Average Delay for Two-Hop CSMA/CD/TDMA Systems with Buffer Capacities of 2, 3 and 5 Packets

Figure 6.37 Average Two-Hop CSMA_CD/TDMA System Delay vs. Throughput Comparison

Figure 6.38 Average Two-Hop CSMA_CD/TDMA System Delay vs. Throughput Comparison

Figure 6.39 Average Two-Hop CSMA_CD/TDMA System Delay vs. Throughput Comparison

Figure 6.40 Average Two-Hop CSMA_CD/TDMA System Delay vs. Throughput Comparison

CHAPTER 7

CONCLUSIONS AND SUGGESTIONS FOR FUTURE RESEARCH

7.1 CONCLUSIONS

A closed form expected delay equation for two hop CSMA_CD/TDMA networks was not obtained using M/G/1 queuing theory for the inner hop. Instead, two general methodologies were developed and verified in Chapter 6 for stable and unstable systems. These procedures are briefly summarized below:

- a. For stable systems, where the sum of the outer hop capacities is less than or equal to the capacity of the inner hop, use a deterministic time interval $= T/2 + T/M$ to approximate inner hop delay. Assume that the expected value of random variable $\Theta = 0$.
- b. For unstable systems, where the sum of the outer hop capacities is greater than the capacity of the inner hop, use the residual life pdf up to an intensity of 0.6 to approximate inner hop blocking delay. Use a constant value of T for inner hop blocking delay at higher intensities to account for the outer hop's tendency

to transmit almost immediately after a blocked channel is cleared. Uncondition both approximations using $P(N-1)*(1-P(0))$. Use the numerical blocking probability to determine an effective simulation intensity.

The concept of decoupling the inner and outer hops, as employed in [4] to analyze CSMA_CD/CSMA_CD two hop networks, was confirmed to be a valid approach when extended to a CSMA_CD/TDMA system. In Chapter 2, the process of approximating the throughput of the CSMA_CD protocol during collision time periods with the maximum throughput of S-ALOHA was verified.

Many wide area networks, such as STELLA-II and UNIVERSE use simple bridge systems which do not have flow control. Packets received during buffer full conditions are discarded and packet continuity is left to higher layer protocols. Also, the requirement for intra-LAN packet transmissions may override the need for lossless, inter-LAN traffic flow and an associated blocking mechanism. The mathematical model presented in thesis is based on a lossy system and may be used, without the lossless modifications, to analyze any lossy CSMA_CD/TDMA network.

It is important to note that this thesis does not consider any local traffic in the outer hops. In LAN interconnection, there is local traffic and therefore the flow

control mechanism introduced in this approach will have a more noticeable impact on the performance of the outer hops. In this thesis we have assumed that each outer hop user terminal communicates via the central station of the inner hop.

7.2 SUGGESTIONS FOR FUTURE RESEARCH

In order to obtain a closed form result for CSMA_CD/TDMA two hop systems, the inaccurate assumption of Poisson arrivals to the inner hop controller must be resolved. A recommended solution, and proposal for future research is to define a precise, general distribution which would be used to determine inner hop state transition probabilities for all system configurations. The ensuing Markov chain analysis, as described in Appendix D, would be more accurate and would not be adversely affected by different inner and outer hop packet transmission times.

Another relevant extension to this thesis would be to derive a suitable finite buffer, inner hop mathematical model for the token passing ring protocol (IEEE 802.5) or FDDI and analyze a two hop CSMA_CD/token passing network. An expression for random variable Θ would also be required as well as a matching two hop simulation program for verification purposes.

Also, more flexible TDMA systems such as demand assigned multiple access (DAMA), Frequency Division Multiple Access (FDMA) and Adaptive TDMA could be used as the inner hop

protocol and the single step state transition probabilities redefined to account for multiple transmissions by one controller in a single TDMA frame. In addition, the TDMA simulation program would require adjustment to reflect the characteristics of the new protocols.

Finally, multi-hop network performance analysis could be attempted in systems which have three or more hops. Clearly the analytical problems would become more complex and the "decoupling" approach may be used in "mesh" type distributed networks where member networks are connected to more than two other networks at the same time. The arrival process to each hop would depend on the characteristics of the protocols involved. The quality of the system model would depend heavily on the accuracy of the desired arrival rate distributions and the modelling of all inter-hop dependencies.

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APPENDIX A.1.1

STATE TRANSITION PROBABILITY CALCULATIONS - BUSY SYSTEM

```
10 REM CALCULATE ARRIVAL PROBABILITIES TO A BUSY SYSTEM
12 REM phusy.bas using Poisson arrivals during T Frame
15 CLEAR:DEFINT F,I,J,M,B,K:DEFSNG R,T,L:DEFDBL S,P
20 T=.1067:M=10:ROW=0
30 INPUT "enter printer status (0=OFF, 1=ON): ";F
40 INPUT "enter buffer size: ";BUFF
50 FOR J=1 TO 10:ROW=ROW+.1
55 L=ROW/T:PRSUM=0:PROB=0
56 PRINT BUFF;"PACKET BUFFER PROB FOR INTENS=";ROW;" LAMBDA=";L
57 IF F=1 THEN LPRINT "          ";BUFF;"PACKET BUFFER PROB FOR INTENS=";ROW;
  "LAMBDA ";L:LPRINT " "
60 FOR K=0 TO BUFF-2
65 KF=K:GOSUB 2000:T2=KFACT
150 PR2=EXP(-L*T)*(L*T)^K
160 PR3=PR2/T2
330 PRINT "prob of ";K;"packets in queue: ";PR3
335 IF F=1 THEN LPRINT "          prob of ";K;"packets in queue: ";PR3
340 PRSUM=PRSUM+PR3
350 NEXT K
360 PRINT "prob of ";K;"packets in queue: ";1-PRSUM
365 IF F=1 THEN LPRINT "          prob of ";K;"packets in queue: ";1-PRSUM:
  LPRINT " "
370 NEXT J
380 GOTO 15
2000 KFACT=1
2005 IF KF=0 THEN KF=1
2010 FOR I=1 TO KF
2020 KFACT=KFACT*I
2030 NEXT I
2040 RETURN
```

APPENDIX A.1.2

STATE TRANSITION PROBABILITY CALCULATIONS - EMPTY SYSTEM

```

10 REM CALCULATE ARRIVAL PROBABILITIES TO AN EMPTY SYSTEM
12 REM pek.bas using summation of arrivals during rv Y and t/m
15 CLEAR:DEFINT F,I,J,M,B,K:DEFSNG R,T,L:DEFDBL S,P
20 T=.1067:M=10:ROW=0
30 INPUT "enter printer status (0=OFF, 1=ON): ";F
40 INPUT "enter buffer size: ";BUFF
50 FOR J=1 TO 10:ROW=ROW+.1
55 L=ROW/T:PRSUM=0:PROB=0
56 PRINT BUFF;"PACKET BUFFER PROB FOR INTENS=";ROW;" LAMBDA=";L
57 IF F=1 THEN LPRINT "          ";BUFF;"PACKET BUFFER PROB FOR INTENS=";ROW;"
LAMBDA=";L:LPRINT " "
60 FOR K=0 TO BUFF-2
65 PROB=0
70 FOR X=0 TO K
80 T1=EXP(-L*(T-T/M))
85 T2=T^(X+1)
90 T3=EXP(-L*T/M)
95 T4=(T-T/M)^(X+1)
100 T8=EXP(-L*T)
105 KF=K-X:GOSUB 2000:T5=KFACT
115 KF=X:GOSUB 2000:T7=KFACT
120 SUM1=L*T1*T2/((X+1)*(1-T8))-L*T1*(T2-T4)/(X+1)
125 SUM2=SUM1/(((T/M)^X)*T5*T7)
135 PROB=PROB+SUM2
140 NEXT X
150 PR3=PROB*T3*(L*T/M)^K
330 PRINT "prob of ";K;"packets in queue: ";PR3
335 IF F=1 THEN LPRINT "          prob of ";K;"packets in queue: ";PR3

```



```
340 PRSUM=PRSUM+PR3
350 NEXT K
360 PRINT "prob of ";K;"packets in queue: ";1-PRSUM
365 IF F=1 THEN LPRINT "          prob of ";K;"packets in queue: ";1-PRSUM:
LPRINT " "
370 NEXT J
380 GOTO 15
2000 KFACT=1
2005 IF KF=0 THEN KF=1
2010 FOR I=1 TO KF
2020 KFACT=KFACT*I
2030 NEXT I
2040 RETURN
```

APPENDIX A.2

STEADY STATE QUEUE LENGTH PROBABILITY AND INNER LOOP EXPECTED DELAY

```
10 OPTION BASE 1
15 DEFINT I,C,B,N,X,Y:DEFDBL T,L,R,P,D,M,V:DEFSTR S,F
20 DIM MAT1(8,8),MAT2(8,8),MAT3(8,8),STATES(8)
22 PFLAG=0
25 GOTO 120
30 PRINT "MATRIX MANIPULATION PROGRAM"
40 PRINT " "
50 PRINT "1.  READ IN MATRIX"
60 PRINT "2.  WRITE OUT MATRIX"
70 PRINT "3.  FILL NEW MATRIX"
80 PRINT "4.  ADD UP MATRIX ROWS"
90 PRINT "5.  DISPLAY MATRIX"
95 PRINT "6.  MULTIPLY MATRICIES"
97 PRINT "7.  PRINT OUT MATRIX AND SYSTEM PARAMETERS"
100 PRINT "8.  CALCULATE SYSTEM PARAMETERS"
101 PRINT "9.  REPEAT USING SAME PARAMETERS"
103 PRINT " "
105 INPUT "ENTER SELECTION: ";CHOICE
110 RETURN
120 INPUT "ENTER BUFFER SIZE: ";BUFF
125 PRINT "SYSTEM STATES"
130 FOR I=1 TO BUFF
140 STATES(I)=STR$(I-1)
150 PRINT STATES(I)
160 NEXT I
170 GOSUB 8000
180 INPUT "ENTER TDMA FRAME TIME: ";T
182 INPUT "ENTER NUMBER OF CONTROLLERS: ";NC
184 INPUT "ENTER INPUT TRAFFIC INTENSITY: ";ROW
186 L=ROW/T
200 GOSUB 30
210 ON CHOICE GOSUB 1000,2000,3000,4000,5000,6000,7100,9000,9500
220 GOTO 200
1000 INPUT "ENTER DISK FILE NAME: ";FILE
1005 INPUT "ENTER MATRIX NUMBER: ";N
1010 OPEN "I",2,FILE
1020 FOR Y=1 TO BUFF
1030 FOR X=1 TO BUFF
1040 INPUT #2, VALUE
1045 IF N=2 THEN GOTO 1055
1050 MAT1(X,Y)=VALUE:GOTO 1060
1055 MAT2(X,Y)=VALUE
1060 NEXT X
1070 NEXT Y
1080 CLOSE 2
1090 RETURN
2000 INPUT "ENTER DISK FILE NAME: ";FILE
2005 INPUT "ENTER MATRIX NUMBER: ";N
2010 OPEN "O",3,FILE
2020 FOR Y=1 TO BUFF
```

```

2030 FOR X=1 TO BUFF
2040 IF N=2 THEN GOTO 2050
2045 VALUE=MAT1(X,Y):GOTO 2055
2050 VALUE=MAT2(X,Y)
2055 PRINT #3, VALUE
2060 NEXT X
2070 NEXT Y
2080 CLOSE 3
2090 RETURN
3000 INPUT "ENTER MATRIX NUMBER: "; N
3005 FOR Y=1 TO BUFF
3010 FOR X=1 TO BUFF
3020 PRINT "PROB";STATES(Y);" -->";STATES(X);
3030 INPUT VALUE
3035 IF VALUE > 1 THEN RETURN
3040 IF N=2 GOTO 3060
3050 MAT1(X,Y)=VALUE:GOTO 3070
3060 MAT2(X,Y)=VALUE
3070 NEXT X
3080 NEXT Y
3090 RETURN
4000 INPUT "ENTER MATRIX NUMBER: ";N
4005 FOR Y=1 TO BUFF:VALUE=0
4010 FOR X=1 TO BUFF
4020 IF N=2 THEN GOTO 4040
4030 VALUE=VALUE+MAT1(X,Y):GOTO 4050
4040 VALUE=VALUE+MAT2(X,Y)
4050 NEXT X
4060 PRINT Y-1,VALUE
4070 NEXT Y
4080 RETURN
5000 INPUT "ENTER MATRIX NUMBER: ";N
5010 FOR Y=1 TO BUFF
5020 FOR X=1 TO BUFF
5030 IF N=2 THEN GOTO 5045
5035 VALUE=MAT1(X,Y)
5040 PRINT STATES(Y);" -->";STATES(X),VALUE
5041 IF PFLAG=1 THEN LPRINT "          ";STATES(Y);" -->";STATES(X),VALUE
5042 GOTO 5060
5045 VALUE=MAT2(X,Y)
5050 PRINT STATES(Y);" -->";STATES(X),VALUE
5051 IF PFLAG=1 THEN LPRINT "          ";STATES(Y);" -->";STATES(X),VALUE
5060 NEXT X
5070 GOSUB 7000
5080 NEXT Y
5085 PRINT " "
5090 PRINT "EXPECTED DELAY :";DELAY
5095 PRINT "EXPECTED NUMBER IN SYSTEM :";MSYSTEM
5100 PRINT "BLOCKING PROBABILITY: ";PBLOCK
5110 PRINT "INTENSITY: ";ROW;" BUFFER SIZE: ";BUFF
5180 IF PFLAG=0 THEN RETURN
5185 LPRINT " "
5190 LPRINT "          EXPECTED DELAY :";DELAY
5195 LPRINT "          EXPECTED NUMBER IN SYSTEM :";MSYSTEM

```

```
5200 LPRINT "          BLOCKING PROBABILITY: ";PBLOCK
5210 LPRINT "          INTENSITY: ";ROW;"  BUFFER SIZE: ";BUFF
5212 LPRINT " "
5214 LPRINT " "
5220 RETURN
6000 INPUT "ENTER FIRST MATRIX NUMBER: ";N1
6010 INPUT "ENTER SECOND MATRIX NUMBER: ";N2
6015 GOSUB 8200
6020 IF N1<>N2 THEN GOTO 6125
6028 FOR Y1=1 TO BUFF
6030 FOR X1=1 TO BUFF
6033 FOR X=1 TO BUFF
6040 MAT3(X1,Y1)=MAT3(X1,Y1)+MAT1(X,Y1)*MAT1(X1,X)
6045 NEXT X
6050 NEXT X1
6060 NEXT Y1
6070 GOTO 6500
6125 FOR Y1=1 TO BUFF
6130 FOR X1=1 TO BUFF
6133 FOR X=1 TO BUFF
6140 MAT3(X1,Y1)=MAT3(X1,Y1)+MAT1(X,Y1)*MAT2(X1,X)
6145 NEXT X
6150 NEXT X1
6160 NEXT Y1
6500 FOR Y=1 TO BUFF
6510 FOR X=1 TO BUFF
6520 MAT1(X,Y)=MAT3(X,Y)
6530 NEXT X
6540 NEXT Y
6550 RETURN
7000 INPUT "PRESS ENTER TO CONTINUE"; S
7010 RETURN
7100 PFLAG=1
7110 GOSUB 5000
7120 PFLAG=0
7130 RETURN
8030 FOR Y=1 TO BUFF
8010 FOR X=1 TO BUFF
8020 MAT1(X,Y)=0:MAT2(X,Y)=0:MAT3(X,Y)=0
8030 NEXT X
8040 NEXT Y
8050 RETURN
8200 FOR Y=1 TO BUFF
8210 FOR X=1 TO BUFF
8220 MAT3(X,Y)=0
8230 NEXT X
8240 NEXT Y
8250 RETURN
9000 P0=MAT1(1,1)
9010 T1=EXP(L*(T/NC))
9020 T2=EXP(-L*T)
9025 T4=T1*(L*T-1+T2)
9027 T5=L*(1-T2)
9030 T6=L*(T+P0*(1/L+T/NC+(T4/T5)-T))
```

```
9035 PBLOCK=1-(1/T6)
9038 MSYSTEM=0:REM Initialize MSYSTEM
9040 PRINT P0,T1,T2,T4,T5,T6,PBLOCK
9050 MAT1(BUFF+1,1)=PBLOCK
9055 FOR X=1 TO BUFF:REM uncondition steady state matrix
9056 MAT1(X,1)=MAT1(X,1)*(1-PBLOCK)
9057 NEXT X
9060 FOR X=2 TO BUFF+1
9070 MSYSTEM=MSYSTEM+MAT1(X,1)*(X-1)
9080 NEXT X
9090 PRINT "EXPECTED NUMBER IN SYSTEM";MSYSTEM
9100 DELAY=MSYSTEM/(L*(1-PBLOCK));
9105 PRINT "EXPECTED DELAY";DELAY
9110 RETURN
9500 INPUT "ENTER INPUT TRAFFIC INTENSITY: ";ROW
9505 L=ROW/T
9510 RETURN
```

APPENDIX A.3

OUTER LOOP EXPECTED DELAY CALCULATIONS

```

10 DEFDBL B,E,H,S,P,D,T,L,O,I,A,C,R:DEFINT X
100 INPUT "Enter propagation delay: ";TAW
110 INPUT "Enter outer loop tx time: ";OLTX
120 INPUT "Enter inner loop frame tx time: ";ILTX
130 INPUT "Enter printer status: ";XSTAT
150 INPUT "Enter Pi(n-1) for inner loop: ";PIN1
160 INPUT "Enter inner loop traffic intensity: ";ROW
1500 L=ROW/ILTX
1510 PIO=EXP(-L*ILTX):REM P no tx in TDMA frame
1520 ROWO=OLTX*L
2100 H1C=ILTX/2
2110 H1=H1C*PIN1*(1-PIO)
2200 EFFOLTX=OLTX+H1:REM Effective outer loop tx time
2300 B1=EFFOLTX+TAW
2310 B2=B1^2
3000 S=.367
3500 BSTAR=EXP(-L*(EFFOLTX+TAW))
3990 T=ILTX
4500 P0=EXP(-L*TAW*2):REM P no tx in 2*taw
4900 REM part one of delay equation
5000 PART1=B1+2*TAW+2*TAW/S
5090 REM part two of delay equation
5100 D1=1-P0
5110 D2=2/L-4*TAW
5120 D3=2*(BSTAR*S-(1-P0))
5130 PART2=D1*D2/D3
5190 REM part three of delay equation
5200 C1=B2+2*B1*+2*TAW*B1+TAW^2

```

Figure C.1 SLAM II Diagram for TDMA

Note: Some of the non-essential troubleshooting and variable recording program statements have not been shown in this diagram.

APPENDIX B.1

TWO HOP CSMA_CD/TDMA SLAM II SIMULATION PROGRAM

GEN,B.MACDONALD,TDMA.CSMA,11/14/88,1,NO,YES,YES/YES,YES,YES/1,72;
LIMITS,4,4,100,

```
;
;   *** TWO HOP TDMA-CSMA SYSTEM B.2 PARAMETERS ***
;   -----
;   NUMBER OF OUTER LOOPS:      10 CSMA/CD AT 150 KBPS
;   OUTER LOOP PACKET SIZE:     50 BITS
;   OUTER LOOP PACKET TX TIME:  .00033 SEC
;   TPROP/TFRAME = ALPHA:      .1
;(UNGUIDED) PROPAGATION DELAY (10 KM): .000033 SEC
;
```

```
;   TDMA INNER LOOP TX SPEED:      150 KBPS
;   INNER LOOP PACKET (SLOT) SIZE:  50 BITS
;   SINGLE SLOT TX TIME:           .00033 SEC
;   NUMBER OF CONTROLLERS (OUTER LOOPS): 10
;   INNER LOOP FRAME TIME:        .0033 SEC
;   BUFFER CAPACITY:              2 PACKETS
;
```

INTERARRIVAL TIME (1/L)	UTILIZATION TDMA (LT)	UTILIZATION CSMA/CD (LT)	INNER LOOP LAMBDA (L)
10.0 SEC	1.0	.10	.10 PKT/SEC
12.5 SEC	.8	.08	.08 PKT/SEC
16.67 SEC	.6	.06	.06 PKT/SEC
25.0 SEC	.4	.04	.04 PKT/SEC
50.0 SEC	.2	.02	.02 PKT/SEC

```
;   NOTE:  PACKET AND FRAME TRANSMISSION TIMES HAVE BEEN RAISED BY
;   A FACTOR OF 3030.303 DURING ACTUAL SIMULATION.
;
```

```
;   ***GLOBAL VARIABLES  TDMA***
;
;   INTLC,XX(2)=1.0;      SLOT LENGTH = PACKET TX TIME
;   INTLC,XX(4)=0;      SPARE
;   INTLC,XX(5)=2;      TDMA BUFFER MAX CAPACITY
;                        NOTE:  MUST CHANGE AWAIT SERVER
;                        VALUE AT LABEL BUFF TO XX(5)-1
;                        IF XX(5) IS CHANGED;
;
;   INILC,XX(6)=0;      MESSAGE COUNTER
;   INTLC,XX(7)=0;      BUFFER FULL START TIME
;   INTLC,XX(8)=0;      BUFFER FULL ELAPSED TIME
;   INTLC,XX(9)=0;      NUMBER OF BLOCKED MESSAGES
;   INTLC,XX(91)=10.0;  TDMA FRAME TIME LENGTH (SEC)
;
```

```
;   *** CSMA/CD GLOBAL VARIABLES ***
;
```



```

INTLC,XX(3)=1.0;      OUTER LOOP PACKET TX TIME
INTLC,XX(21)=0;       TIME OF LAST PACKET DEPARTURE
INTLC,XX(31)=0;       OUTER LOOP STATUS (0=IDLE, 1=BUSY
;                     SUCCESS, 2=BUSY COLLISION)
INTLC,XX(41)=0;       0=START OF COLLISION, 1=END OF SUCCESS
INTLC,XX(51)=12.5;    OUTER LOOP PACKET INTERARRIVAL TIME
INTLC,XX(61)=0;       START TIME OF TRANSMITTING PACKET
INTLC,XX(99)=.1;      LENGTH OF ONE TIME SLOT = TAW
;
;
NETWORK;
;
;   *** TDMA GATE AND RESOURCE DEFINITIONS ***
;
;       GATE/TDMA,CLOSE,4;          TDMA FRAME SYNC GATE (IFL 4)
;       RESOURCE/SERVER(1),2;      TDMA SERVER RESOURCE (IFL 2)
;
;   *** CSMA/CD GATE DEFINITIONS ***
;
;       GATE/CMGO,CLOSE,1;
;       GATE/CNTO,CLOSE,3;
;
;   O U T E R   L O O P
;   T H E   L O G I C   F O R   C H A N N E L   M A N A G E R
;
;   CREATE,,0,1,1,1;
;   COLCT,XX(99),TAW;
;   COLCT,XX(3),OL PKT TX TIME;
;   COLCT,XX(99)/XX(3),ALPHA;
;   COLCT,XX(51),PKT INTERARR;
;   COLCT,XX(3)/XX(51),TFC INTENS;
;   COLCT,XX(2),IL PKT TX TIME;
;   COLCT,XX(5),IL BUFF SIZE;
;
CCNO   AWAIT(1),CMGO;
;       CLOSE,CMGO;
;       ACT,,XX(41).EQ.0,BCL0;
;       ACT,,XX(41).EQ.1,ESCO;
;
;
;   END OF A SUCCESSFUL TRANSMISSION
;
ESCO   ASSIGN,XX(21)=TNOW,1;
;       ACT,,NNQ(3).GT.1,A1;
;       ACT,,NNQ(3).EQ.1,A2;
;       ACT,,NNQ(3).EQ.0,A3;
A1     ASSIGN,XX(31)=2,1;
;       ACT,,BCL0;
A2     ASSIGN,XX(31)=1,XX(71)=1,1;
;       ACT,,SBC0;
A3     ASSIGN,XX(31)=0,1;
;       ACT,,CCNO;
;
;   BEGINNING OF A COLLISION PERIOD
;

```

```

BCLO    ASSIGN, ATRIB(4)=USERF(13),1;
        ASSIGN, XX(31)=2,1;
        ACT, ATRIB(4),,ADPO;
;
ADPO    ASSIGN, XX(31)=1,1;
        ASSIGN, XX(71)=USERF(14),1;
        ACT,,,SBCO;
;
SBCO    OPEN, CNT0;
        ACT,,,CCN0;
;
;
;      INPUT TRAFFIC TO OUTER LOOP
;
INPT    CREATE, EXPON(XX(51),2),1,1;      RAND STRM 2
;
;      THE LOGIC FOR INPUT TRAFFIC
;
IETO    GOON,1;
        ASSIGN, ATRIB(4)=USERF(15),1;
        ACT, ATRIB(4),,SNS0;
;
SNS0    GOON,1;
        ACT,,XX(31).EQ.0,B1;
        ACT,,XX(31).GT.0,B2;
B1      GOON,1;
        ACT,,XX(61).GT.0,B2;
        ACT,,XX(61).EQ.0,B3;
B2      ASSIGN, XX(31)=2,1;
        ACT,,,PSQ0;
B3      ASSIGN, XX(61)=TNOW,1;
        ACT,,,CPR0;
;
PSQ0    AWAIT(3),CNT0;
        CLOSE, CNT0;
        ASSIGN, XX(71)=XX(71)-1,1;
        ACT,,XX(71).EQ.0,MC0;
        ACT,,XX(71).NE.0,PSQ0;
;
MC0     GOON,1;
        ACT,XX(99),XX(7).EQ.0,NC10;      TDMA WILL SET XX(7)
        ACT,,XX(7).NE.0,PSQ0;            IF INNER LOOP BLOCKED
;
CPR0    GOON,1;
        ACT,XX(99),XX(7).EQ.0,FPC0;      TDMA WILL SET XX(7)
        ACT,,XX(7).NE.0,PSQ0;            IF INNER LOOP BLOCKED
;
FPC0    ASSIGN, XX(61)=0,1;
        ACT,,XX(31).EQ.0,C1;
        ACT,,XX(31).GT.0,C2;
C1      ASSIGN, XX(31)=1,1;
        ACT,,,NC10;
C2      ASSIGN, XX(41)=0,1;
        ACT,,,OPM0;

```

```

;
OPMO      GOON,1;
          OPEN,CMGO;
          ACT,,,PSQO;

;
NC10      GOON,1;
          ACT,XX(3)-XX(99),,TSYO;

;
TSYO      ASSIGN,XX(61)=0,XX(41)=1,1;
          ACT,XX(99);

;
          ASSIGN,XX(21)=TNOW;
          COLCT,INT(1),OUTERL DLY;

;
          OPEN,CMGO;
          ACT,,,TDMS;

;
;        ***** TDMA INNER LOOP CODE *****
;
TDMS      GOON,1;
          ACT,,XX(6).LT.XX(5),COUNT;      COUNT INPUT PACKETS
          ACT,,XX(6).GE.XX(5),ERROR;

;
COUNT    ASSIGN,XX(6)=XX(6)+1,1;
          ACT,,XX(6).EQ.XX(5),SBUSY;      BUFFER FULL INSTANT
          ACT,,XX(6).LT.XX(5),BUFF;

;
SBUSY     ASSIGN,XX(7)=TNOW,1;      SET START TIME FOR BUSY PERIOD

;
BUFF      AWAIT(2/1),SERVER,BALK(ERROR),1;      WAIT FOR FREE BUFFER
          AWAIT(4/1),TDMA,BALK(ERROR),1;      WAIT FOR TDMA GATE
          ACT,XX(2),,DECRB;

;
DECRB     ASSIGN,XX(6)=XX(6)-1,1;
          FREE,SERVER/1,1;
          COLCT,INT(1),TOTAL PCKT DELAY;
          ACT,,XX(7).NE.0,ENDB;
          ACT,,XX(7).EQ.0,QUIT;

;
ENDB      ASSIGN,XX(8)=TNOW-XX(7),XX(7)=0,1;
          OPEN,CMGO;      ACTIVATE OUTER LOOP
          COLCT,XX(8),THETA;      CHANNEL MANAGER

;
QUIT      TERM,2000;

;
ERROR     COLCT,XX(6),ERRORS;
          TERM,1;

;
;        ***TDMA SLOT GATE***
;
          CREATE;      START TDMA GATE CYCLE

;
LOOP      CLOSE,TDMA;
          ACT,XX(91);      CLOSE GATE FOR ONE FRAME

```

```
OPEN,TDMA;  
  ACT,,,LOOP;      OPEN GATE FOR 1 MESSAGE  
;  
  ENDNETWORK;  
;  
INIT,0,135000;  
;MONTR,TRACE,0,5,ATRI(1),NNQ(3);  
FIN;
```

TWO HOP TDMA-CSMA/CD SYSTEM USER FUNCTIONS

```

REAL FUNCTION USERF(IFN)
    COMMON/SCOM1/ATRIB(100),DD(100),DDL(100),DTNOW,II,MFA,
    1MSTOP,NCLNR,NCRDR,NPRNT,NNRUN,NNSET,NTAPE,SS(100),SSL(100),TNEXT,
    1TNOW,XX(100)
    REAL TAW,RCT
    GOTO(1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21
    1,22,23,24),IFN
C
C    XX(21) = TIME LAST SUCCESSFUL TRANSMISSION OCCURED
C
    1  CONTINUE
    2  CONTINUE
    3  CONTINUE
    4  CONTINUE
    5  CONTINUE
    6  CONTINUE
    7  CONTINUE
    8  CONTINUE
    9  CONTINUE
    10 CONTINUE
    11 CONTINUE
    12 CONTINUE
    13 CONTINUE
C*****
C
C    RETURN A RANDOM TIME PERIOD AFTER CHANNEL IS SENSED IDLE
C    AND A COLLISION IS AHEAD.
C    IN SLOTTED PROTOCOLS ALL COLLIDING PACKETS HAVE THE SAME
C    SENSING TIME I.E. AT THE BEGINING OF A TIME SLOT XX(6*N+K)
C    IS SET TO -1 ANYWHERE OUTSIDE A COLLISION INTERVAL, HOWEVER

```

C DURING A COLLISION INTERVAL IT CONTAINS THE TNOW.

C

TAW=.0001

S=.367

TEMP2=S

TEMPR=UNFRM(0.,1.,5)

TEMP=ALOG(TEMPR)/ALOG(1.-TEMP2)

ITEMP = TEMP

IF(ITEMP.LT.TEMP) ITEMP=ITEMP+1

USERF=2.*TAW*ITEMP

RETURN

C

C

C

14 CONTINUE

C*****

C

C

C RANDOM SELECTION OF A USER AT THE END OF A COLLISION PERIOD

C

TEMPR=UNFRM(0.,1.,4)

TEMPR=TEMPR*NNQ(3)

ITEMP=TEMPR+1

USERF=ITEMP

RETURN

C

C

C

15 CONTINUE

C*****

C

C CALCULATE TIME REQUIRED TO DELAY PACKET TO START OF NEXT SLOT

C

TAW=.0001

```
TEMP=TNOW-XX(21)
RCT=TEMP/(2.*TAW)
ICT=INT(RCT)
TEMP1=RCT-ICT
IF(TEMP1.GT.0.0) GOTO 610
C      ELSE
      ATRIB(4)=0
      GOTO710
C      THEN
610      ATRIB(4)=2.*TAW*(1.-TEMP1)
C      ENDIF
710      CONTINUE
C
      USERF=ATRIB(4)
      RETURN
C
C
C
16  CONTINUE
17  CONTINUE
18  CONTINUE
19  CONTINUE
20  CONTINUE
21  CONTINUE
22  CONTINUE
23  CONTINUE
24  CONTINUE
      END
```

APPENDIX C

VERIFICATION OF STANDALONE TDMA AND CSMA_CD SIMULATION

C.1 VERIFICATION OF TDMA SIMULATION

A SLAM II simulation program which reflects the TDMA protocol of [21] is incorporated into the two hop TDMA-CSMA_CD program and is attached as Appendix B.1. It should be noted that this is not optimized for CPU efficiency and there are probably other more optimized methods of achieving the same simulation. In its favour, this simulation was written without FORTRAN user function calls. It is modular, understandable and lends itself quite easily to amalgamation with the CSMA_CD simulation program.

Figure C.1 is A SLAM II diagram using the graphic notation of [3] which corresponds to the TDMA simulation code. Additional code was implemented to measure the potential blocking periods during heavy traffic loads (Random variable 0). A pseudo-code description of the TDMA simulation logic of Appendix B.1 follows:

Simultaneous activities A and B

- A:
- Generate packet
 - Increment queue length
 - Buffer full?
 - Yes: - Record buffer full start time
 - Block further transmissions

- Pass packet to server
- No: - Pass packet to server
- Server
 - Transmit packet
 - Terminate busy period and record duration if applicable
 - Record packet delay, number in queue and length of busy period
- B:
 - Close TDMA gate for one frame cycle
 - Instantaneously open and close gate to simulate slot synchronization

This standalone TDMA simulation was executed using the same configuration as that analysed in [21]. Specific parameters are:

TDMA frame time (T): .3 sec
Number of users (M): 450
Slot duration (T/M): .00066667 sec

Buffer size was fixed at 2,3,5 and 8 packet buffers while traffic intensities were varied from .2 to 1.0 in increments of .2 for each fixed buffer configuration. Figures C.4 to C.7 inclusive are graphs of simulation vs. mathematical models for expected delay in a single-hop finite buffer TDMA network.

Inner hop
controllers (C1-C4)

Figure C.2 Sample Four LAN Two Hop System

Figure C.3 Snapshot Of The TDMA Inner Hop

Expected * : Yan's result [27]

Delay (sec) @ : Simulation

Figure C.4 Comparison of a Two Packet Buffer
TDMA network

Expected * : Yan's result [27]
Delay (sec) @ : Simulation

Figure C.5 Comparison of a Three Packet Buffer
TDMA network

Expected

Delay

(sec)

* : Yan's result [27]

@ : Simulation

Figure C.6 Comparison of a Five Packet Buffer
TDMA network

Expected

Delay

(sec)

* : Yan's result [27]

e : Simulation

Figure C.7 Comparison of an Eight Packet Buffer
TDMA network

C.2 VERIFICATION OF CSMA_CD SIMULATION

The goal of CSMA_CD and TDMA protocol simulation verification is to ensure that the statistics collected at sample points are in reasonable agreement with current accepted mathematical models [20,21]. As such exhaustive simulation runs using multiple random number seed variables were not performed for these tests. Exhaustive simulation of this nature will be performed when analyzing the two hop CSMA_CD/TDMA systems of Chapter 6.

A SLAM II simulation program which reflects the CSMA_CD protocol of [20] is described pictorially in Figure C.8 using the graphical notation of [3]. Again, it should be noted that this program is not optimized for CPU efficiency. A pseudo-code description of Figure C.6 follows:

Simultaneous activities A (controller 1),
B (controller 2), and C

- A:
- Generate packet (controller 1)
 - Wait for server 1
 - Wait for slot synchronization
 - Transmit with probability P_1
 - Wait for next slot with $P=1-P_1$
 - Collision?
 - Yes: - Re-compute P_1 and wait

for next slot

- No: - Release server 1 and collect
expected delay stats

- B:
- Generate packet (controller 2)
 - Wait for server 2
 - Wait for slot synchronization
 - Transmit with probability P_2
 - Wait for next slot with $P=1-P_2$
 - Collision?
 - Yes: - Re-compute P_2 and wait
for next slot
 - No: - Release server 2 and collect
expected delay stats
- C:
- Close CSMA gate for one time slot =
end to end propagation delay
 - Instantaneously open and close gate to
simulate slot synchronization

SLAM II simulation code based on Figure C.8 was executed using the same parameters as the network analyzed in [20]. The critical ratio of propagation delay to frame transmission time or "a" was set to 0.1 and expected delay statistics were collected for controllers 1 and 2 for traffic intensities from 0.1 to 0.6 in intervals of 0.1. The value of "a" was then set to 0.01

Figure C.8 SLAM II Logic for Single CSMA/CD controller

Note: Some of the non-essential troubleshooting and variable recording program statements have not been shown in this diagram. With slight variations in variable names, the Controller 2 diagram would be identical to this figure.

and examined at traffic intensities of 0.4 and 0.8. Prior to these tests, a single simulation run was made for 1000, 1500, 2000 and 5000 packet transmissions. There was no significant difference between the 1000 and 5000 packet trials hence a standard execution length of 1000 packets was established for the $a=0.01$ experiments. Since execution time decreased considerably in the $a=0.1$ trials, packet length was extended to 1500 successfully transmitted packets for all experiments in this configuration. It should also be noted that for $a=0.1$ the maximum throughput or traffic intensity achievable by a stable CSMA_CD system is 0.6. The results were very close to the mathematical results of Lam in [20] and have been compiled in tabular form as Tables C.1 and C.2.

C.3 OPTIMIZED CSMA_CD SIMULATION

Unfortunately, the CSMA_CD simulation described in the preceding section was excessively slow when exhaustive tests were conducted in a two hop environment and consequently a modified version of a SLAM II program used in [4] was used instead. This simulation used the probability of successful transmission which was proved in [20] to resolve collision situations and FORTRAN user functions to perform pseudo time slot synchronization. The ensuing execution time decreased by a factor of 20 to 1 and permitted the degree of two hop network simulation

required to adequately confirm mathematical results. It is nonetheless a valid exercise to compare the optimized CSMA_CD simulation to the standalone results of the original simulation which emulates a working Ethernet and the theoretical results of Lam. All three results appear in Tables C.1 and C.2 and, as can be seen by examination, there is little difference between them. A SLAM II diagram depicting this optimized simulation is contained in Figures C.9 and C.10. This optimized CSMA_CD simulation forms the outer hop of the two hop CSMA_CD/TDMA simulation program of Appendix B.1 and is also described in pseudo-code below:

Simultaneous Activities A (Input traffic) and B (Channel Manager)

A: Input traffic

- Generate input packets at an exponentially distributed interarrival rate
- Delay each packet to start of next slot
- If channel status = idle then
 - If start time of current packet = 0 then
 - Set start time = TNOW
 - Goto CPR0
 - Else set channel status = busy
 - Goto PSQ0

- Else set channel status = busy PSQ0
- Await gate CNT0
- Close CNT0
- Transmit selected packet to MC0 and return all others to PSQ0.

MC0 - Transmit Taw (slot duration)

 - Goto NC10

CPR0 - Transmit Taw (slot duration)

 - Set packet start time to 0

 - If channel status = idle then

 - Set channel to busy successful tx

 - Goto NC10

 - Else set channel to start of collision

 - Initiate channel manager

 - Return packet to PSQ0

NC10 - Transmit rest of packet

 - Reset channel status

 - Collect statistics

 - Initiate channel manager

 - Terminate packet

B: Channel Manager

CCN0 - Await CMGO. Opened by input traffic activity

 - Close CMGO

BCL0 - If channel status = start of collision then

 - Wait a random time period based on

the throughput of S-ALOHA

- Set channel status = start of successful tx
- Select a random packet from PSQ0 queue
- Open PSQ0 gate (CNT0)
- Goto CCN0
- Else channel status = end of successful tx
 - Check packet queue at PSQ0
 - If queue contain > 1 packet then
 - Set channel status = collision
 - Goto BCL0
 - If queue = 1 then
 - Set chan status = success tx
 - Open PSQ0 gate and return to CCN0
 - If queue = 0 then return to CCN0

Table C.1 Simulation vs Lam's result for "a" = .1

Intensity	Ctrlr 1 Delay (sec)	Ctrlr 2 Delay (sec)	Optimized CSMA/CD (sec)	Lam's Result (sec)
.1	.376	.373		.39
.2	.425	.419	.427	.44
.3	.537	.594		.53
.4	.717	.701	.642	.69
.5	1.15	1.260		1.26
.6	5.30	2.280	5.640	6.00

It is noted that as the value of intensity approached maximum throughput, the system became less stable and consequently the values for delay suffered from severe fluctuations.

Table C.2 Simulation vs Lam's result for "a" = .01

Intensity	Ctrlr 1 Delay (sec)	Ctrlr 2 Delay (sec)	Optimized CSMA/CD (sec)	Lam's Result (sec)
.2			.342	.35
.4	.403	.438	.407	.42
.6			.592	.59
.8	1.180	1.320	1.310	1.20

Figure C.10 Optimized CSMA/CD Channel Manager

APPENDIX D

EXPECTED DELAY FOR THE TDMA INNER HOP

D.1 INNER HOP DESCRIPTION

TDMA or synchronous time division multiplexing (STDM) is a simple, widely used protocol. User stations are joined in a physical hop and transmit data into pre-assigned or demand assigned slots. Slots are organized into frames and, for this analysis, each controller is assigned one slot at a pre-determined time in each frame. Each controller is then able to transmit in its own slot once every frame. A TDMA channel is formed by slots of the same index or user in consecutive frames. Each user has a fixed buffer for storing incoming messages. The buffers are all of the same length for all stations hence a homogeneous network is assumed. In the two hop TDMA network, a user station is analogous to an inner hop controller and the latter term will be used from this point on. Since Yan's model [21] is used, it is assumed that each inner hop controller is assigned one slot per frame. The following notation is introduced to further define the M/G/1 FCFS inner hop:

- TDMA frame duration: T (seconds)
- Number of inner hop controllers: M
- Individual user slot length: T/M (seconds)

- Inner hop controller
 arrival rate: λ (packets/sec)
- Inner hop controller
 buffer size (max): N (packets)

The following derivation is based on the work of Yan [21] and amplifies the explanation given by Hayes [1]:

Fixed length packets arrive to each inner hop TDMA controller according to identical Poisson processes, of λ packets/sec. Since there is no inter-dependency between inner hop controllers as is the case with a contention based inner hop protocol such as S-ALOHA or CSMA_CD, the delay analysis of one TDMA controller is representative of the entire system. A message arriving to an inner hop controller will be confronted by one of two possible queuing situations. Either the destination controller will have from one to $N-1$ in its buffer or its buffer will be empty and the arriving message will effectively start a "busy" period for that controller. The distinction is important because the ensuing message service times are different for each case. Also, recall the assumption that the inner hop controller is equipped with a mechanism which effectively disables the outer hop when it experiences a buffer full condition.

Since each inner hop controller processes packets individually, the transmission unit which will be analyzed is

the packet. The service time of each packet is defined as the time interval between the instant that the packet reaches the head of the inner hop controller's queue and the instant that it has been completely transmitted. Where queuing or busy controllers are involved, an individual packet has a constant service time of T seconds since the service time interval starts at the preceding packet's departure point or epoch. Actual packet transmission starts $T - T/M$ seconds later at the controller's next time slot and terminates T/M seconds later thereby consuming a total of T seconds.

A packet which arrives to an empty controller has a service time which is non-standard or extraordinary. Packets of this nature will wait a random period of time distributed between 0 and T seconds since a packet which arrives immediately after the start of a slot will wait one slot length (T/M) as well as the standard $T - T/M$ seconds before start of transmission hence the service time of such a packet is also random and distributed between T/M and $T + T/M$ seconds. This system is shown in figure D.1. These additional variables are summarized below:

- Packet service time (busy system): T (sec)
- Idle time period : Z (sec)
- Packet service time (empty system): X (sec)
- Number of packets in queue at time t : Q_t

GRAPH OF $RV\ Y$ vs. IDLE PERIOD per FRAME

Figure D.1 TDMA packet service time

The packet service time probability distribution function (PDF) for packets which arrive to a busy controller is defined as:

$$F_b(x) = \text{constant } T$$

The PDF for packet service time X when a packet arrives to an idle or empty controller is defined as:

$$F_e(x) = P [X < x]$$

$F_e(x)$ is a PDF which describes random variable (random variable) X which has two components. The first component, random variable Y , is defined as the elapsed time between a packet's arrival to an empty controller and the time that the controller starts transmission of that packet. The second component of random variable X is the packet transmission time which is a constant $= T/M$. Therefore:

$$X = Y + T/M$$

The state transition matrix which will eventually describe the steady state probabilities that the controller contains from 0 to $N-1$ packets will use Poisson arrival probabilities over constant time T and random time X in order to be embedded at the system departure epochs. Thus, the

derivation of the PDF for random variable Y or F(y) now becomes vital to this analysis. Once derived, the probability density function (pdf) of random variable Y = f(y) may be determined by taking the first derivative of F(y) and the expected or mean value of Y obtained by evaluating:

$$\int_0^T y f(y) dy \quad 0 < y < T$$

D.2 THE EXPECTED VALUE OF RANDOM VARIABLE "Y"

In general the PDF of random variable Y is based on the distribution of the idle period or random variable Z which is exponential since a Poisson arrival process is assumed. Random variable Y will be described in terms of random variable Z and since the exponential pdf of random variable Z is defined as:

$$f(z) = \int_{t1}^{t2} \lambda e^{-\lambda t} dt \quad (\lambda = \text{packet arrival rate})$$

the PDF of random variable Y may be found by applying the limits of random variable Y to the pdf of random variable Z. In all cases:

$$\text{random variable } Y = (T - T/M) - Z$$

Figure D.2

Figure D.2 describes three separate cases which form $F(y)$.

Case 1 occurs when the idle period extends from the time of the last packet departure to the start of that controller's next transmission slot. In this instance:

$$\begin{aligned}
 F(y) &= P[Y < y] \\
 &= P[(T-T/M)-Z < y \quad 0 < Z < (T-T/M)] \\
 &= P[(T-T/M)-y < Z < (T-T/M)] \\
 &= \int_{(T-T/M-y)}^{(T-T/M)} \lambda e^{-\lambda t} dt \\
 &= (e^{\lambda y} - 1)e^{-\lambda(T-T/M)}
 \end{aligned}$$

Case 2 describes a unique instance where a packet arrives during its controller's transmit slot i.e. between $T-T/M$ and T . Case 2 applies for situations where the idle period is terminated during the next or subsequent transmit slots ($iT, (i+1)T, (i+2)T, \dots$) and not just the initial arrival to start of next slot as in Case 1.

random variable $Y = T-Z$ since the time interval from
packet arrival to start of
transmission has an upper
bound of T vs $T-T/M$ seconds

$$\begin{aligned}
 F(y) &= P[T-Z < y, \quad 0 < Z < T] \\
 &= P[0 < Z < T-T/M-y]
 \end{aligned}$$

$$= P \text{ [idle period is between } 0 \text{ and } T-T/M-y]$$

$$= \int_0^{T-T/M-y} \lambda e^{-\lambda t} dt$$

$$= U(y-T+T/M) * (1 - e^{-\lambda(T-T/M-y)})$$

where $U(x) = 1$ when $x > 0$ or $x = 0$

and $U(x) = 0$ when $x < 0$

Case 3 is an infinite sum of probabilities similar to Case 1 in that the idle period is terminated somewhere between the end of transmit slot e.g. $(i+1)T$ and the start of the next transmit slot e.g. $(i+2)T$. The PDF derived for Case 1 is put into an infinite geometric series as follows:

$$\begin{aligned} F(y) &= \sum_{i=1}^{\infty} P [(i)T-T/M-y < Z < (i+1)T-T/M] \\ &= \sum_{i=1}^{\infty} e^{-\lambda[(i+1)T-T/M]} (e^{\lambda y} - 1) \\ &= \frac{e^{-\lambda(2T-T/M)} (e^{\lambda y} - 1)}{(1 - e^{-\lambda T})} \quad \begin{aligned} a &= e^{-\lambda(2T-T/M)} \\ r &= e^{-\lambda T} \end{aligned} \end{aligned}$$

The final PDF of random variable Y is the sum of the expressions derived for cases 1, 2 and 3, specifically:

$$\begin{aligned}
 F(y) &= \frac{e^{-\lambda(T-T/M)} (e^{\lambda y} - 1)}{(1 - e^{-\lambda T})} \\
 &\quad + U(y-T+T/M)(1-e^{-\lambda(T-T/M-y)}) \quad 0 < y < T \\
 &= 1 \quad y > T
 \end{aligned} \tag{D.1}$$

The pdf of random variable Y , $f(y)$, is obtained in the traditional manner, namely:

$$\begin{aligned}
 f(y) &= d F(y)/dy \\
 &= \frac{\lambda e^{-\lambda(T-T/M-y)} + \delta(y-T+T/M)(1-e^{-\lambda(T-T/M-y)})}{1 - e^{-\lambda T}} \\
 &\quad - U(y-T+T/M)\lambda e^{-\lambda(T-T/M-y)} \tag{D.2}
 \end{aligned}$$

where $\delta(y-T+T/M)(1-e^{-\lambda(T-T/M-y)})$

$$= d/dy [U(y-T+T/M)\lambda e^{-\lambda(T-T/M-y)}]$$

The expected value of random variable Y , $E[Y]$, is then determined by integrating the product of $f(y)$ dy and y :

$$E[Y] = \int_0^T y f(y) dy$$

$$= \int_0^T y [\lambda e^{-\lambda(T-T/M-y)}] dy \quad (D.3)$$

$$+ \int_0^T y [\delta(y-T+T/M)(1-e^{-\lambda(T-T/M-y)})] dy \quad (D.4)$$

$$- \int_0^T y [U(y-T+T/M)\lambda e^{-\lambda(T-T/M-y)}] dy \quad (D.5)$$

Equations D.3, D.4 and D.5 are then integrated using integration by parts and summed to arrive at the final value for $E[Y]$ which is:

$$E[Y] = \frac{e^{(\lambda T/M)} (\lambda T - 1 + e^{-\lambda T})}{\lambda(1 - e^{-\lambda T})} \quad (D.6)$$

D.3 STEADY STATE DISTRIBUTION OF SYSTEM QUEUE SIZE

The "system", in this context, is the finite buffer of the inner hop controller. In terms of single step Markov chain analysis, the queuing system has its transition points embedded at the packet departure epochs. Packet flow equilibrium is assumed in that over a sufficiently lengthy period of time, the number of arrivals to the system equal the number of departures. This assumption is critical in the development and calculation of the packet expected delay

using Little's result which will be performed in the next section.

The statistic of interest at the departure epochs is the number of packets in the buffer of the inner hop controller. Since a deterministic access protocol is the subject of analysis, these epochs correspond to the controller "end of transmit slot" time instances. These slots, when considered in sequence from time zero to infinity, constitute a homogeneous Markov chain which is aperiodic and irreducible providing that the previous assumption of equilibrium is maintained. Using the Poisson arrival probabilities for a fixed time T and random time period $X = Y+T/M$, the following expressions are introduced to calculate the single step state transition probabilities:

$$P(b,k) = \frac{e^{-\lambda T} (\lambda T)^k}{k!} \quad k > 0 \quad (D.7)$$

$$= 0 \quad k < 0$$

= { Probability of k arrivals
given that the system has one
or more packets in queue }

$$P(c,k) = \sum_{x=0}^k \left\{ \left[\int_0^T \frac{(\lambda y)^x e^{-\lambda y} f(y) dy}{x!} \right] \right. \quad (D.8)$$

$$\left. * \frac{[e^{-(\lambda T/M)} (\lambda T/M)^{(k-x)}]}{(k-x)!} \right\} \quad k > 0$$

$$\begin{aligned}
&= 0 \quad k < 0 \\
&= \sum_{x=0}^k \{ (\text{Probability that } x \text{ arrivals occur} \\
&\quad \text{during random variable } Y) * \\
&\quad (\text{Probability that} \\
&\quad k-x \text{ arrivals occur during packet} \\
&\quad \text{transmission time} = T/M) \} \\
&= \{ \text{Probability that } k \text{ arrivals occur} \\
&\quad \text{during random variable } X = Y+T/M \\
&\quad \text{given that the system was empty} \} \\
&\text{where } f(y) \text{ is defined by equation D.2}
\end{aligned}$$

$$\begin{aligned}
P(e,k) &= e^{-\lambda T/M} (\lambda T/M)^k \sum_{x=0}^k \frac{(T/M)^{-x}}{x! (k-x)!} \\
&\quad * \frac{\{ \lambda e^{-\lambda(T-T/M)} * T^{(x+1)} \}}{(1 - e^{-\lambda T})(x+1)} \\
&\quad - \frac{\lambda e^{-\lambda(T-T/M)} * [T^{(x+1)} - (T-T/M)^{(x+1)}]}{(x+1)}
\end{aligned}$$

$P(e,k)$ may now be used to define transition probabilities from state 0 (empty system) to states 1,2,3... N-1 (recall that the system is embedded at the departure epochs hence a state of N will never exist). $P(b,k)$ may be used to define transition probabilities from states 1,2,3...N-1 to states 1,2,3... N-1. The resulting state transition matrix P is shown below:

$$P = \begin{matrix} & \begin{matrix} Q_i & 0 & 1 & 2 & \dots & N-2 & N-1 \end{matrix} \\ \begin{matrix} 0 \\ 1 \\ 2 \\ : \\ : \\ N-2 \\ N-1 \end{matrix} & \begin{bmatrix} P(e,0) & P(b,0) & 0 & \dots & 0 & 0 \\ P(e,1) & P(b,1) & P(b,0) & \dots & 0 & 0 \\ P(e,2) & P(b,2) & P(b,1) & \dots & 0 & 0 \\ : & : & : & & : & : \\ : & : & : & & : & : \\ P(e,N-2) & P(b,N-2) & P(b,N-3) & P(b,1) & P(b,0) & \\ \text{(see below)} & & & & & \end{bmatrix} \end{matrix}$$

The state transition to $N-1$ must consider the probabilities that additional packets arrived to the system but were blocked due to a full buffer. In terms of the system under consideration, the outer hop or generator of these packets would be prohibited from transmission but in order to completely describe the system states, this simplification is used to arrive at a steady state distribution for state $N-1$. Assuming that the system is at state Q_i , the probability that a transition is made from $N-2$ to $N-1$ is:

$$1 - \sum_{i=0}^{N-(Q_t+1)} P(b,i) \quad \text{for a busy system or,}$$

$$1 - \sum_{i=0}^{N-(Q_t+1)} P(e,i) \quad \text{for an empty system}$$

For example if $Q_t=2$, the probability that a transition is made from $N-2$ to $N-1$ is:

$$1 - [P(b,0)+P(b,1)+P(b,2)\dots+P(b,n-3)]$$

that is, the remaining probability not consumed in previous state transitions.

The steady state distribution of P is defined as π . π is computed by the multiplication of P by itself until a convergence is achieved for each state $[\pi(0), \pi(1), \pi(2)\dots\pi(N-2), \pi(N-1)]$. This represents a steady state, stable queuing system as the departure epochs are evaluated from zero to infinity and assumes that the matrix P is ergodic. Each value of $\pi(k)$ for $k=0$ to $N-1$ represents the probability of state $\pi(k)$ with the condition that the arrival or arrivals are not blocked by the system. In order to arrive at an unconditional steady state system distribution which is defined as $r(k)$, $\pi(k)$ must be unconditioned for each value of k as follows:

$$r(k) = \pi(k)[1 - r(N)] \quad (D.10)$$

where $r(N)$ is the system blocking probability

D.4 EXPECTED NUMBER OF PACKETS IN SYSTEM QUEUE

Using the assumption that the steady state number of messages which arrive to the system is equal to the total number of messages which depart from the system, the average arrival rate must equal the average departure rate. The inter-departure time between the (n) th and $(n+1)$ th packets is defined as $\phi(n)$. In a busy system ($Q_t > 0$) as t approaches infinity, the expected value $E[\phi]$ of the inter-departure time is:

$$E[\phi] = T$$

In an empty system:

$$E[\phi] = (Z + X) \quad \begin{array}{l} \text{where } Z \text{ is the idle time} \\ \text{and } X \text{ is the service time} \\ \text{of a packet which arrives} \\ \text{to an empty system.} \end{array}$$

Therefore, overall $E[\phi]$ for all situations is:

$$E[\Phi] = [1-\pi(0)]T + \pi(0)(E[Z]+E[X])$$

where: $\pi(0)$ = the conditional steady state probability that the system is empty

$E[Z] = 1/\lambda$ due to exponentially distributed idle period

$$E[X] = T/M + E[Y] \text{ (see equation (D.6))}$$

$$\begin{aligned} E[\Phi] &= [1-\pi(0)]T + \pi(0) \left[\frac{1/\lambda + T/M + \frac{e^{\lambda T/M} (\lambda T - 1 + e^{-\lambda T})}{\lambda(1-e^{-\lambda T})}}{\lambda(1-e^{-\lambda T})} \right] \\ &= T + \pi(0) \left[\frac{1/\lambda + T/M + \frac{e^{\lambda T/M} (\lambda T - 1 + e^{-\lambda T})}{\lambda(1-e^{-\lambda T})} - T}{\lambda(1-e^{-\lambda T})} \right] \end{aligned} \quad (D.11)$$

The unconditional departure rate is equal to $1/\{\text{expected inter-departure time}\} = 1/E[\Phi]$. As stated previously, in a stable system over a sufficiently lengthy period of time, the average packet departure rate equals the average packet arrival rate. With this knowledge, the unconditional arrival rate is obtained as follows:

$$\lambda(1-r(N)) = 1/E[\Phi]$$

The blocking probability, $r(N)$ is:

$$r(N) = 1 - \frac{1}{\lambda(E[\Phi])} \quad (D.12)$$

where $E[\Phi]$ is given by equation D.11

The expected number of packets in the system $E[Q_e]$ is:

$$\sum_{k=0}^N k[r(k)] \quad \text{where } r(k) \text{ is given by} \quad (D.10)$$

Using Little's result as described in [2], the expected value for packet delay, defined as D is:

$$D = \frac{E[Q_e]}{\lambda[1-r(N)]} \quad (D.13)$$

APPENDIX E

SAMPLE SIZE AND CONFIDENCE INTERVAL

System 'A' simulation was executed 10 times at an intensity of .6 for sample sizes of 1000, 2000, 4000, and 8000 packets. Although there was a slight increase in the average expected delay between 2000 and 8000 packets, it was less than 2% and was therefore judged to be negligible. A sample size of 2000 packets was established for the remaining simulation runs. In retrospect, considering the number of individual simulation runs required and the resulting mainframe CPU time, 8000 packet simulations would have created excessive processing delays with no visible improvement to the obtained results.

Since the two hop simulation differed from the predicted numerical results at higher intensity levels (.8 and beyond) for valid reasons which were attributed to the assumptions made in the numerical derivations, a complete set of confidence intervals were not obtained for each point in the two-hop simulations. Shown below is reliable data gathered for 'B' system at an intensity of .6:

Random Seed	Expected Delay ($\times 10^{-3}$ sec)	$(D_i - D)^2$
1	5.10	.060025
2	4.99	.018225
3	4.63	.050625
4	4.58	.075625
5	4.53	.105625
6	4.77	.007225
7	4.83	.000625

8	5.26	.164025
9	4.92	.004225
10	4.94	.007225

$$S^2 = 4.9345 \times 10^{-9}$$

$$\text{Mean Delay} = 4.86 \times 10^{-3} \text{sec}$$

$$S = 7.0246 \times 10^{-5}$$

Since each value for expected delay is an independent, identically distributed random variable (IIDRV), the mean delay is normally distributed using the Central Limit Theorem. The following is introduced to clarify the process of establishing confidence intervals:

D = Mean delay of sample

M = Expected mean delay = $E[D]$

n = Number of samples (simulation runs)

S = Sample variance

V = Actual variance of distribution

Since V , D , and M are normally distributed random variables (sum of IIDRV's) then:

$$\text{random variable } Z = \frac{D - M}{V/\sqrt{n}}$$

is also normally distributed with a mean of 0 and a variance of 1 or $N(0,1)$ and

$$\begin{aligned} A &= P\left[-a < \frac{D - M}{V/\sqrt{n}} < a\right] \\ &= P\left[D - \frac{aV}{\sqrt{n}} < M < D + \frac{aV}{\sqrt{n}}\right] \end{aligned}$$

is the probability that Z lies between $-a$ and $+a$. In terms of expected mean delay $= M$, the random variable $D - aV/\sqrt{n}$ and $D + aV/\sqrt{n}$ is the confidence interval of M . Since V is not known, it is estimated by:

$$S^2 = \frac{(D_i - D)^2}{(n-1)}$$

where D_i is the expected delay of the i th sample. Using the previous values for D_i and D :

$$S^2 = 4.9345 \times 10^{-9} \text{ and } S = 7.0246 \times 10^{-5}$$

Therefore, for a 98% confidence interval for $n-1$ samples using the Student's T distribution the value of $a = 2.821$ and

$$.004855 - \frac{(2.821)(7.0246 \times 10^{-5})}{\sqrt{10}} < M < .004855 + \frac{(2.821)(7.0246 \times 10^{-5})}{\sqrt{10}}$$

or $M = .004855 \pm .00006266$ with 98% confidence. Since these values represent worst case fluctuations for all valid results, they are indicative of the accuracy of all simulations undertaken in this thesis.

APPENDIX F

DERIVATION OF $E(z^{Q(n-1)+U_n})$

$Q_{(n-1)}$ is the state of the system in terms of packets in queue at departure epoch $(n-1)$. U_n is the random number of packets which arrive to the system during the interval between the end of a successful packet transmission at departure epoch $(n-1)$ and the start of the next successful packet transmission.

As discussed in Chapter 5, U_n is dependent on $Q_{(n-1)}$, since the system could be idle, contain one packet or be in a collision situation with more than one packet ready for transmission at the next time slot. It is assumed that limiting random variables exist for Q_n and U_n as $n \rightarrow \infty$ and the sub-scripts which indicate departure epochs will be dropped. Continuing from equation 5.18:

$$\begin{aligned}
 E(z^{Q+U}) &= Q(0)E(z^U \mid Q=0) + Q(1)E(z^U \mid Q=1) + \\
 &\quad \sum_{k=2}^{\infty} Q(k)z^k E(z^U \mid Q \geq 2) \\
 &= Q(0)E(z^U \mid Q=0) + Q(1)E(z^U \mid Q=1) + \\
 &\quad [Q(z) - Q(0) - Q(1)z] E(z^U \mid Q \geq 2)
 \end{aligned} \tag{F.1}$$

Where $Q(z)$ is defined in Chapter 5 after equation (5.19)

Let X be a random variable which represents the number of arrivals during the last time slot of an idle time period.

Let Y be a random variable which denotes the number of arrivals during the collision time period R .

Therefore, $Y = U - X$. For $n \geq 2$:

$$\begin{aligned}
 & \text{Prob}(U=n \mid Q=0) \\
 &= \text{Prob}(X+Y=n \mid Q=0) = \sum_{k=0}^n \text{Prob}(X=n-k) \text{Prob}(Y=k) \\
 & \quad - \text{Prob}(X=0) \text{Prob}(Y=n) \\
 & \quad - \text{Prob}(X=1) \text{Prob}(Y=n-1)
 \end{aligned} \tag{F.2}$$

$$\begin{aligned}
 E(z^U \mid Q=0) &= \text{Prob}(U=0 \mid Q=0) + z \text{Prob}(U=1 \mid Q=0) \\
 & \quad + \sum_{n=2}^{\infty} \text{Prob}(U=n \mid Q=0) z^n \\
 &= z \text{Prob}(U=1 \mid Q=0) \\
 & \quad + \sum_{n=2}^{\infty} \text{Prob}(U=n \mid Q=0) z^n
 \end{aligned} \tag{F.3}$$

since U cannot equal 0

Since $\text{Prob}(U=1 \mid x=0) = 0$ and $\text{Prob}(Y < 0) = 0$ the value of n may be set to 0 without changing the value of following equation (F.4).

$$\begin{aligned}
 & \sum_{n=2}^{\infty} \text{Prob}(U=n \mid Q=0) \\
 &= \sum_{n=0}^{\infty} \left\{ \sum_{k=0}^n \text{Prob}(X=n-k) \text{Prob}(Y=k) - \text{Prob}(X=0) \text{Prob}(Y=n) \right. \\
 & \quad \left. - \text{Prob}(X=1) \text{Prob}(Y=n-1) \right\} z^n
 \end{aligned} \tag{F.4}$$

Therefore,

$$\begin{aligned} \sum_{n=2}^{\infty} \text{Prob}(U=n \mid Q=0) z^n &= E(z^X)E(z^Y) \\ &\quad - \text{Prob}(X=0)E(z^Y) \\ &\quad - z \text{Prob}(X=1)E(z^Y) \end{aligned} \quad (\text{F.5})$$

Substituting equation (F.5) into (F.3) results in the following:

$$\begin{aligned} E(z^U \mid Q=0) &= z \text{Prob}(U=1 \mid Q=0) + E(z^X)E(z^Y) \\ &\quad - \text{Prob}(X=0)E(z^Y) \\ &\quad - z \text{Prob}(X=1)E(z^Y) \end{aligned} \quad (\text{F.6})$$

$$\begin{aligned} E(z^U \mid Q=1) &= 1 \text{ since } \text{Prob}(U=0 \mid Q=1) = 1 \text{ for} \\ &\quad U=0 \text{ and zero elsewhere} \end{aligned} \quad (\text{F.7})$$

$$\begin{aligned} E(z^U \mid Q \geq 2) &= \text{Prob}(U=n \mid Q \geq 2) z^n \\ &= C^*(1-z) \end{aligned} \quad (\text{F.8})$$

Substitute equations (F.6), (F.7), and (F.8) into equation (F.1) to obtain equation (5.19) as follows:

$$\begin{aligned} E(z^{Q+U}) &= Q(0) [E(z^X)E(z^Y) - \text{Prob}(X=0)E(z^Y) \\ &\quad - z \text{Prob}(X=1)E(z^Y)] + Q(1) z \\ &\quad + \sum_{k=2}^{\infty} Q(k) z^k E(z^Y) \end{aligned}$$

END

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