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**SUBMICRON CMOS BUILDING BLOCKS
FOR HIGH SPEED FREQUENCY SYNTHESIS
AND CLOCK RECOVERY APPLICATIONS**

Fangxing Wei, B.Eng., M.Eng., Beijing

A thesis submitted to the Faculty of Graduate Studies and Research in partial
fulfilment of the requirements for the degree of Master of Engineering

Department of Electronics
Carleton University
Ottawa, ONT. K1S 5B6
May 1997

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submitted by

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in partial fulfilment of the requirements for
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Thesis Supervisor

Chair, Department of Electronics

Carleton University
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ABSTRACT

The submicron CMOS technology offers operating speed today attainable by bipolar and/or Gallium Arsenide technologies. In particular digital radio applications using frequency range up to 2 GHz and frequency synthesizer/clock recovery applications operating in this range are subject of high interest. In this thesis report, exploration results aimed at using CMOS technology for frequency synthesis and clock recovery applications. The circuits critical to the performance of high frequency PLL sub-systems are analysed in detail. They include the phase detector, loop filter and frequency prescaler. The VCO circuits have been previously reported by our research group. The loop filter for the frequency synthesis and clock recovery applications has a very low frequency zero. To realize this filter as a fully integrated circuit requires an unrealistically large on-chip capacitor in microfarad range. Currently the most popular method is to use an off-chip capacitor. In this thesis, the general impedance converter and the Miller effect are employed to realize an emulated microfarad range on-chip capacitor to allow the loop filter full integration. Due to process parameter variations and thermal environment instability, the frequency response of the loop filter can vary significantly. Two tuning structures are proposed to tune the loop filter automatically. The true single phase clock dynamic technique is employed for the design of the frequency prescaler and the Hogge phase detector with the objective of achieving high speed with moderate power consumption. SPW is used to model all the building blocks and loops for the PLL applications to achieve efficient simulation. It's believed all this research can contribute to a fully integrated CMOS high speed frequency synthesis or clock recovery application. Work reported here does not include measurement results of the fabricated structures. Measurement results are however expected to be available as an outcome of continuing research in that area.

The information used in this thesis comes in part from the research program of Dr. T. A. Kwasniewski and his associates in the VLSI in Communications group. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Kwasniewski and his associates for education and research purposes, including publication in the open literature with the appropriate credits. Matters of intellectual property may be pursued collaboratively with Carleton University and Dr. Kwasniewski where and as appropriate.

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LIST OF SYMBOLS

Antenna
Filter
Mixer
Summer
Adjustable capacitor
Capacitor
Resistor
PMOS transistor
PMOS transistor
NMOS transistor
NMOS transistor
Switch
Power supply
Ground
Reference voltage

Connection
Port
Current source
Current source
Unit delay
Operational amplifier
Operational amplifier with balanced outputs
Operational transconductance amplifier
Amplifier with gain A
Integrator
Buffer
Inverter

AND gate

NAND gate

OR gate

NOR gate

XOR gate

D-flip-flop

LIST OF ABBREVIATIONS

AC	Alternating Current
BATMOS	A BiCMOS process
BiCMOS	Bipolar CMOS
BW	Band Width
C	Capacitor
C ² MOS	Clocked CMOS
CICC	Custom IC Conference
CMOS	Complementary MOS
CRC	Clock Recovery Circuit
D/A	Digital to Analog converter
DAC	Digital to Analog Converter
DC	Direct Current
DEMUX	De-multiplexer
DFF	D type Flip-Flop
DLL	Delay-Locked Loop
DPLL	Delay- and Phase-Locked Loop
DSP	Digital Signal Processing
FET	Field Effect Transistor
FF	Flip-Flop
FFT	Fast Fourier Transformation
GIC	General Impedance Converter
HSPICE	High speed Simulation Programming with IC Emphasis
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input and Output ports
IF	Intermediate Frequency
ISSCC	International Solid State Circuits Conference

LIST OF ABBREVIATIONS

JSSC	Journal of Solid State Circuits
L	represent inductance
LF	Loop Filter
LO	Local Oscillator
LPF	Low Pass Filter
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MUX	Multiplexer
NMOS	Negative Metal Oxide Semiconductor
NORA	No RAc
NRZ	Non Return to Zero
OPAMP	OPerational AMPlifier
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PD	Phase Detector
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
PMOS	Positive Metal Oxide Semiconductor
R	Resistor
RC	Resistor and Capacitor or their product
RF	Radio Frequency
RX	Receiver
RZ	Return to Zero
SAW	Surface Acoustical Wave
SC	Switched-Capacitor
SONET	Synchronous Optical NETwork
SPW	Signal Processing Workbench
TCXO	Crystal oscillator
TSPC	True Single Phase Clock
TX	Transmitter
VCCS	Voltage Controlled Current Source

LIST of ABBREVIATIONS

VCF	Voltage Controlled Filter
VCO	Voltage Controlled Oscillator
VCPS	Voltage Controlled Phase Shifter
VCVS	Voltage Controlled Voltage Source
VLSI	Very Large Scale Integrated circuits
XOR	eXclusive OR gate

CHAPTER 1

Introduction

1.1 Thesis motivation and objectives

Communication systems use electromagnetic signals to send a message from one place to the other through a medium such as space, optic fibre, or cable. In this modern information era, people deeply depend on many kinds of communication systems in nearly every aspect of their lives. They can use radio and TV to entertain themselves, use the telephone to do business negotiating and to keep in contact with family members and friends, use the graphic data received from satellites to forecast the weather, and use the internet to visit every corner of the world, etc. For this reason, communication system design has become one of the fastest growing fields in the engineering world.

The performance of a communication system can be judged by its information transmission rate, its physical size, and its power consumption. The transmission rate should be as high as possible, while the physical size and power consumption should be as small as possible. All these requirements push the IC designer to face the challenge by designing larger and larger scale ICs, integrating more circuit components, and imagining new high speed and low power circuit structures. All the research work presented in this thesis can be a part of that endeavour.

In communication system design, the phase-locked loop (PLL) circuit structure plays a very important role. It can be used as a frequency synthesizer to generate high speed carrier signal for mobile cellular systems. It also can be used as clock recovery circuit to extract the clock from the received data to synchronize the post-stage digital signal processing (DSP). Of course, the PLL

has other kinds of applications, such as carrier recovery, tracking filter, frequency modulation and demodulation, phase modulation and demodulation, etc.

Fig. 1.1• Architecture of a cellular telephone transceiver

An integrated portable transceiver front end block diagram [1] is shown in Fig. 1.1. For the receiving part, the received signal is mixed with the carrier signal generated by the frequency synthesizer to move it to the baseband, then mixed again to move it to standard IF frequency. For the transmission part, the frequency synthesizer is used to generate the carrier signal and modulated by the baseband signal to be transmitted. A multichannel data transmission system block diagram [2] is shown in Fig. 1.2. In this system, a PLL based clock recovery circuit is used to regenerate the data and to demultiplex the data channels.

Fig. 1•2• Architecture of a data transmission system

The object of this thesis is to design a fully integrated loop filter (LF), high speed Hogge phase detector (PD), and high speed frequency prescaler for the PLL based frequency synthesizer (shaded boxes in Fig. 1.1) and clock recovery circuit (shaded box in Fig. 1.2). Power consumption is also a big concern in this research work. HSPICE is the simulation tool, and 0.8μ BATMOS process is employed for the chip design. All chips are submitted to CMC for manufacture. All the PLL building blocks are modelled with SPW. Several aspects of the PLLs' performance are examined with SPW.

1•2• Thesis outline

Chapter 2 reviews basic PLL theory, the structure options for its building blocks, the development of the frequency synthesizer and clock recovery structures. The advantages to base the frequency synthesizer and clock recovery structures on the PLL are also discussed. Chapter 3 reviews the development of high speed dynamic circuit techniques and tries to show that the most advanced TSPC technique is the solution to a lot of dynamic high speed design problems. In chapter 4, a continuous-time OTA-C type loop filter is designed with on-chip automatic tuning: the calculation procedure is shown; the LF structure is designed; the GIC structure and the Miller effect are

employed to emulate large capacitance; and two automatic tuning schemes are constructed. In chapter 5, the principle of the Hogge phase detector is reviewed. Several Hogge phase detectors are designed with the TSPC technique to work for 622 Mbps clock recovery applications. In chapter 6, the principle of the frequency prescaler and the work done in this field are reviewed. Two new circuit structures are designed to achieve the goals of high speed and low power consumption. In chapter 7, the SPW models for all PLL building blocks are given. The PLL is simulated with SPW. Some SPW simulation results are shown. In chapter 8, conclusions and suggestions for future research are made. Design details are given in the appendixes. Published papers and books referenced are listed at the end of this thesis.

CHAPTER 2

Frequency synthesis and clock recovery overview

2•1• Basics of phase-locked-loop (PLL)

PLLs are widely used in fields such as communication instruments, wireless mobile systems, and disk drive electronics. PLL is not a new concept; it has been in use for more than half a century. All the PLL applications in engineering push the demand for higher performance and lower cost in electronics systems. The development of VLSI techniques in terms of circuit speed, power consumption and integration complexity makes this possible.

2•1•1• Advantages of phase-locking [3]

Why is PLL so popular in so many applications? The reason is that phase-locking offers elegant solutions to all the applications mentioned above.

- **Jitter Reduction**

Fig. 2•1• Timing jitter

Signals often experience timing jitter as they propagate through a communication channel

or as they are retrieved from a storage medium. Shown in Fig. 2.1, jitter manifests itself as variation of the period of a waveform, a type of corruption that cannot be removed by amplification and clipping even if the signal is of a binary nature.

A PLL can be used to reduce the jitter.

- **Skew Suppression**

Fig. 2•2• Clock skew in a digital system

Fig. 2.2 illustrates a critical problem in high-speed digital systems. Here, a system clock, CK_s , enters a chip from a printed-circuit board (PCB) and is buffered (in several stages) to sharpen its edges and drive the load capacitance with minimal delay. The principal difficulty in such an arrangement is that the on-chip clock, CK_c , typically drives several nanofarads of device and interconnect capacitance, exhibiting significant delay with respect to CK_s . The resulting skew reduces the required timing margin budget for on-chip and inter-chip operations.

In order to lower the skew, the clock buffer can be placed in a PLL, thereby aligning CK_c with CK_s .

- **Frequency Synthesis**

Many applications require frequency multiplication of periodic signals. For example, in the digital system of Fig. 2.2, the bandwidth limitation of the PCB constrains the frequency of *CKs*, whereas the on-chip clock frequency may need to be much higher. As another example, a wireless transceiver employs a local oscillator (LO) whose output frequency must be varied in small, precise steps, for example, from 900MHz to 925MHz in steps of 200 kHz.

These exemplify the problem of “frequency synthesis”, a task performed efficiently using phase-locked systems.

- **Clock Recovery**

Fig. 2•3• Clock recovery from random data

In many systems, data is transmitted or retrieved without any additional timing reference. In optical communications, for example [2], a stream of data flows over a single fibre with no accompanying clock, but the receiver must eventually process the data synchronously. Thus, the timing information (e.g., the clock) must be recovered from the data at the receiver end. As shown in Fig. 2.3.

Most clock recovery circuits (CRC) employ phase locking.

2.1.2. Basic theory [3,4]

The PLL is a negative feedback phase loop that can be used to synchronize the frequency of the output signal generated by a voltage controlled oscillator (VCO) with the frequency of a reference signal by means of stabilizing the phase difference of the signals. The basic structure of PLL is shown in Fig. 2.4.

Fig. 2.4• Basic Structure of PLL

Phase-locked systems exhibit nonlinear behaviour at least during part of their operation (e.g., transient process during locking), thus requiring time-domain analysis in almost all applications. This can be done by performing time domain transient simulation of a PLL circuit with SPICE simulator. The loop simulation with SPICE (or its derivative HSPICE) is very slow and inefficient. The modelling work done with SPW, as shown in Chapter 7, is an effort to find a fast and efficient method of large signal transient simulation in time-domain for PLL design. This kind of simulation can show the locking process, the response of loop filter output voltage to a frequency step, and the VCO output spectrum (by using FFT utility).

When a PLL is in the steady state or in a very slow transient process, it is very useful to represent the loop with small signal model and study the PLL's response in the frequency domain.

The frequency domain study is also extremely helpful to show the noise performance of the PLL by studying the PLL output spectral purity. In this case, a linear model of the PLL is required.

The PLL system is composed of three basic blocks (See Fig. 2.4).

- **Phase detector (PD):**

Phase detector is a component used to compare the phase and frequency difference between the input signal and the VCO output signal and to convert the phase difference to a voltage output. Its ideal characteristic is shown in Fig. 2.5. Its output can be expressed by equation (2.1).

Fig. 2.5• Characteristic of an ideal PD

$$v_d = K_d f(\phi_r - \phi_o) = K_d f(\phi_e) \quad (2.1)$$

Where,

v_d — the output voltage of PD,

K_d — the conversion gain of the PD expressed in unit of volts per radian,

ϕ_r — the phase of input signal,

ϕ_o — the phase of VCO output,

ϕ_e — the phase difference.

The output signal amplitude of PD is a function of the phase difference between input reference signal and the PLL output VCO signal. Only the DC component of the output is needed to

adjust the PLL. For the linearized PLL model, PD is characterized as:

$$v_d = K_d \phi_e \quad (2.2)$$

- **Loop filter (LF)**

The loop filter is used to filter out the higher frequency components of the PD output signal, drive the VCO and hence force the PLL to operate in the lock mode. For the loop filter with transfer function given as $H(s)$, the output of the filter can be denoted as:

$$v_c = H(s)v_d \quad (2.3)$$

- **Voltage-controlled oscillator (VCO)**

The transfer characteristic of an ideal VCO is shown in Fig. 2.6.

Fig. 2.6• Characteristic of an ideal VCO

The filter output voltage v_c controls the VCO angular frequency according to the following transfer characteristic:

$$\omega_1 = \omega_0 + K_0 v_c \quad (2.4)$$

Where,

ω_0 — the VCO output angular frequency when v_c is zero,

ω_1 — the anycase VCO output frequency,

K_0 — the VCO conversion gain in unit of radians per second per volt.

By definition, the angular frequency is the derivative of phase, thus:

$$\omega_1 - \omega_0 = K_0 v_c = \frac{d\phi_o}{dt} \quad (2.5)$$

$$\phi_o = \int K_0 v_c dt \quad (2.6)$$

The linear transfer characteristic of a VCO can be expressed by equation (2.7).

$$\phi_o = \frac{K_0 v_c}{s} \quad (2.7)$$

By combining the models for three building blocks, the linear model for the PLL is obtained, as shown in Fig. 2.7.

Fig. 2.7• Linear model of PLL

From the above linear model of the PLL, the phase transfer function ϕ_o/ϕ_r can be obtained, as shown in equation (2.8). This small signal frequency domain response of the PLL can be used to study the PLL stability, PLL bandwidth, PLL step response, phase error response, and PLL noise performance etc.

$$\frac{\phi_o}{\phi_r} = \frac{K_d K_0 H(s)}{s + K_d K_0 H(s)} \quad (2.8)$$

2.1.3• VCO circuit options [3-9]

For a VCO that is to be used in a PLL, the following performance criteria are of main concern:

Tuning range: Tuning range is a range between the minimum and maximum values of the VCO frequency. The variation of the output amplitude and jitter must be minimal in the tuning range. The tuning range must accommodate the PLL input frequency range as well as process and temperature induced variations in the VCO frequency range.

Jitter and phase noise: The timing accuracy and spectral purity requirements for the PLL to be designed impose an upper bound on the VCO jitter and phase noise.

Supply and substrate noise rejection: If integrated together with digital circuits, VCOs must be highly immune to supply and substrate noise.

Linearity: The frequency versus voltage relation should be linear. Nonlinearity will cause harmonic distortion of importance in some applications.

Power consumption: For communication applications, the working frequency usually is very high. Low power consumption is very critical.

Cost: Using an inexpensive process (such as CMOS process) to design a very high speed VCO is preferred. Expensive and high power consumption processes like bipolar should be avoided.

There are two classes of VCO design methods: resonant tank VCOs and relaxation VCOs. For the resonant structure, an L-C tank is required. It is still very difficult to integrate precisely controlled, high-Q inductors. A relaxation type of VCO is currently a preferred choice regardless of implementation technology.

The operation of a relaxation VCO is based on charging, discharging, recharging and re-discharging. The prototype model of the relaxation VCOs is a ring oscillator, as shown in Fig. 2.8,

which has an odd number of inverters connected in a negative feedback loop.

(Odd number of inversions)

Fig. 2•8• Ring Oscillator

To use the ring oscillator as a VCO, a tuning scheme should be introduced to control the individual inverter delay (Fig. 2.9). Tuning can be applied to only one or any number of inverters.

Fig. 2•9• Voltage controlled oscillator

Fig. 2•10• Ring oscillator frequency tuning schemes

Two of the most often used tuning schemes are: capacitive tuning and resistive (current)

tuning, as shown in Fig. 2.10. The capacitive tuning scheme varies the value of the node capacitance and therefore controls the delay of each inverter resulting in the frequency control of the VCO. The resistive tuning scheme varies the current through each inversion stage. In this way, the charging and discharging speed can be controlled.

The new submicron CMOS processes make it possible to design complete CMOS gigahertz frequency range and low power VCOs. In Fig. 2.11, several CMOS inverter stages are shown.

Fig. 2.11• Inversion blocks with tuning

2.1.4• Phase detector design options

For a phase detector to be used in a PLL, the following performance criteria are of main concern [5]:

Phase detection range: Different PDs have different phase detection ranges. The PD structure should be chosen according to a particular application.

Frequency of operation: Some high speed applications require a very high speed PD or PFD. In such cases, special circuit techniques need to be utilized in the PD or PFD design.

Linearity: Good linearity can lower the harmonic distortion, reduce loop noise, and influence acquisition performance

Dead zone: The dead zone is a region where the magnitude of the PD DC output sticks at a fixed value. It is caused either by PD output being driven into output voltage range limits or by PD input going below input stage threshold. If the phase difference varies within the dead zone, the DC output does not change sufficiently to correct the resulting error and a peak-to-peak jitter approximately equal to the width of the dead zone can arise in the VCO output.

Power consumption: Low power design is very critical to portable communication applications.

Cost: Small die area and an inexpensive process (such as CMOS) will reduce the device cost.

There are many PD structures currently in use (detailed analysis in [4]):

- Four-Quadrant Multiplier
- Gilbert Multiplier
- Double Balanced Multiplier
- Exclusive-OR (XOR) Phase Detector
- Two-State Phase Detector
- Three-State Phase Detector

- Z-State Phase Detector
- Sample-and-Hold Phase Detector
- Hogge Phase Detector

All the conventional PDs can only detect the phase difference between two input signals. They can be modified to detect the frequency difference also by adding frequency discriminators to them and form phase frequency detectors (PFD).

A PFD structure [5,10,11] derived from XOR PD is shown in Fig. 2.12. This PFD delivers a 360° detection range and eliminates the dead zone by moving it to the ends of the detection range. When incorporated in a PLL, this results in the phase detector operating in the linear region when the loop is in lock. Frequency detection in this type of PFD overrides the phase detection function whenever the reference input and the VCO output are different in frequency. This feature helps to pull the VCO output frequency back to a stable locked condition quickly and to reduce the lock in time.

Fig. 2•12• PFD with no dead zone

Among PLL based clock recovery applications, the Hogge phase detector is considered to

be a very good choice [12]. Its structure is shown in Fig. 2.13. It will be discussed in detail in Chapter 5.

Fig. 2•13• Hogge phase detector

A differential PD or PFD structure will offer a better noise performance [13,14]. A simple way to construct a differential structure is to replicate the single ended circuit and cross couple the two inputs, as shown in Fig. 2.14. This also will require a differential input loop filter to go with the differential structure PD or PFD. The differential structure can cancel common mode jitter at the output of the detector and thus provide high immunity to noise coupled from digital circuitry.

Fig. 2•14• Differential structure of PD

All digital style PDs and PFDs can be combined with charge pumps to form the charge

pump version PDs and PFDs [3]. Charge pumps are utilized to convert the timed output logic levels of these digital style PDs or PFDs into analog quantities for controlling the loop VCO. The charge pump can smooth the digital PD or PFD output signal, prevent overdriving the active loop filters and improve the noise performance of PLL. PLLs employing charge-pumps are called charge-pump PLL [15-25], as shown in Fig. 2.15. The function of the charge pump is to provide an infinite gain (integration effect) for a static (DC) phase difference at the input of the PD; the static phase difference is zero when a charge pump version PLL is in lock. Its role in a PLL is very much like a loop filter. A detailed schematic will be shown in the following section.

Fig. 2-15• Charge pump PLL

2-1-5• LF structure options [3-5,26]

The function of the LF in a PLL is to filter out the DC component from the PD output, drive the VCO, and force the PLL to operate in the lock mode. When designing an on-chip LF, the accuracy of the pole and zero frequency positions, the Q factors, filter noise sensitivity, and power efficiency are of main concern.

The loop filters can be varied from simple first order passive RC networks to complex high order structures. The choice is determined by the critical parameters of the PLL application. A higher order filter is good for AC filtering, but it increases the circuit design complexity and can possi-

bly cause instability of the PLL. In Fig. 2.16, the main options for loop filter implementation are listed.

Fig. 2.16• Choices of loop filter implementation

This part will be mainly devoted to the discussion of LF types. The integration techniques will be discussed in a following chapter.

For certain applications where large PLL bandwidth is not required, a first order passive RC low-pass filter usually can be chosen. This kind of filter can offer unit DC gain and doesn't contribute or even attenuate the overall loop gain of a PLL. Several passive filters are shown in Fig. 2.17.

$$H(s) = 1 / (s/\omega + 1)$$

$$\omega = 1 / RC$$

$$H(s) = (1 + s/\omega_2) / (1 + s/\omega_1)$$

$$\omega_1 = 1 / (R_1 + R_2)C$$

$$\omega_2 = 1 / R_2C$$

Fig. 2•17• Several passive loop filter forms

For other applications, with wide PLL bandwidth, one can use an active filter to provide additional gain. For the active filter design, a infinity DC gain and finite AC gain is usually required. The transfer function, signal flow diagram and realization of a general form of active filter is shown in Fig. 2.18.

Fig. 2•18• Model of active filter

Fig. 2.19 shows a single amplifier implementation of the active filter model discussed in Fig. 2.18.

Fig. 2•19• Single amplifier implementation of the active filter model

In some applications, it is desirable to purposely introduce an additional pole ω_3 . In one method R_1 is split, as shown in Fig. 2.20(a), into two halves and a capacitor C_3 is used to bypass to ground. Another method is to connect the output of the filter to ground by a resistor and a capacitor in series, as shown in Fig. 2.20(b). If the new pole ω_3 is properly located, it allows suppression of high-frequency components that the OPAMP can't handle [4]. This pole is also used in some applications to reduce phase jitter of a synthesized frequency [27].

Fig. 2.20• The filter structures with extra pole

Any filter structure listed in this part can be modified to offer differential inputs. For example, Fig. 2.20(a) can be changed to the following style to offer two differential inputs, as shown in Fig. 2.21.

Fig. 2•21• An example of loop filter with differential inputs

In the charge pump PLL, the charge pump itself is not an independent building block. Digital style PDs or PFDs combined with charge pumps form charge pump version PDs or PFDs. The function of the charge pump is to change the digital outputs of PDs or PFDs into analog quantities. Introducing some passive or active components to the output of the charge pump can also make it function as a loop filter [3,15-25]. Some charge pump examples of this type are shown in Fig. 2.22.

Fig. 2•22• Charge pump version loop filters

2•2• PLL based frequency synthesizer

2•2•1• Introduction

Frequency synthesizers are widely used in mobile communication systems to generate the carrier frequencies for transceiver modulation and demodulation. Their main function is to generate an output whose frequency is derived from a fixed stable frequency reference. Frequency synthesis techniques evolved from the early open-loop and costly synthesizer to modern phase-locking synthesizers. Frequency synthesis techniques can be classified into two categories: direct synthesis and indirect synthesis. Each category can be subdivided into several different techniques, as shown in

Fig. 2.23.

Fig. 2.23• Frequency synthesis techniques

Direct frequency synthesis techniques are relatively old [28-33]. In the following sections, the emphasis is put on the phase-locking frequency synthesis techniques.

2.2.2• PLL based indirect frequency synthesis

By introducing a frequency divider into the feedback loop of the basic PLL (Fig. 2.24), a simple PLL based indirect synthesis structure can be constructed.

Fig. 2.24• PLL based indirect frequency synthesis

When the PLL shown in Fig. 2.24 is in lock, $f_{REF} = f_{VCO}/N$. So if the division rate of the divider can be controlled, a number of frequencies, which are multiples of f_{REF} , can be synthesized

by controlling the division rate N . Here the division rate N is an integer. The smallest synthesized frequency step is f_{REF} . In order to improve frequency resolution, f_{REF} has to be reduced. For the PLL, the loop settling time is in reverse proportion to the reference frequency. The reduction of reference frequency will reduce the switching speed of the frequency synthesizer. The design rule for that switching speed is $t_s = 50/f_{REF}$ [34].

The above contradictory requirements lead to the idea of division rate N being a fractional number. If N can be fractional, high frequency resolution can be achieved without lowering the reference frequency. This idea leads to the development of the PLL based fractional division frequency synthesis technique.

2.2.3• PLL based fractional division frequency synthesis

Fig. 2.25• PLL based fractional division frequency synthesis

By introducing a frequency prescaler (a dual modulus frequency divider) into the feedback loop of the basic PLL (Fig. 2.25), a PLL based fractional division frequency synthesis structure can be constructed. The two states of the binary logic control input to the frequency prescaler correspond to the two division rates, N and $N+1$. The modulus controller is responsible for the generation

of a control sequence to switch the division rate between N and $N+1$ randomly to generate the fraction wanted. If in $(p+q)$ division operations, the number of division rate N ($\div N$) is p , and the number of division rate $N+1$ ($\div(N+1)$) is q , the synthesized frequency f_{VCO} and the fractional number N_1 are:

$$f_{VCO} = N_1 \times f_{REF} \quad (2\cdot9)$$

$$N_1 = \frac{p \times N}{p + q} + \frac{q \times (N + 1)}{p + q} = N + \frac{q}{p + q} \quad (2\cdot10)$$

As for the modulus controller, there are several algorithms for its construction. The current practice shows the Δ - Σ modulator has the best performance [35,36].

As for the frequency prescaler, the most popular circuit structure used for its construction is just a simple Johnson counter [37-40]. The problem is, how to choose a proper circuit building block to build the counter and to make it work at high speed with low power consumption and low design cost. Detailed discussion will be given in chapter 6.

Among all the frequency synthesis techniques, the PLL based fractional division frequency synthesizer is regarded as the most promising technique [35].

In the PLL based fractional division frequency synthesizer, only the VCO and the frequency prescaler work at high frequency. The design of high speed, low power and low cost frequency prescalers and VCOs is critical to this type of frequency synthesizer design.

2•3• PLL based clock recovery

2•3•1• Introduction

In digital communication systems, information is conveyed by a series of bits—1's and

0's. In order to process the data correctly, the receiver needs to use a functional block, called clock recovery, to synchronize a clock to the data so that the clock frequency f_0 is equal to the bit rate (baud) f_B of the data. Applications like satellite data links, floppy disk readers, etc., require clock recovery.

Two data formats employed for digital data communications are: return-to-zero (RZ) data and non-return-to-zero (NRZ) data. For each different data format, the spectrum of the data stream differs, the clock recovery structure should also be different. Fig. 2.26 shows the spectrum difference between RZ and NRZ data formats. For the RZ data format, the spectrum has a frequency component at f_B and a background broad spectral density due to random gaps of 0's in the data stream. For the NRZ data format, the spectrum doesn't even have a frequency component at f_B . For the recovered clock, only the spectrum at f_B is left.

Fig. 2•26• Data formats, recovered clock and their spectrum

The NRZ data format can be transformed into RZ data format [4]. There are several kinds

of converters available (see [4] for detail).

A conventional clock recovery circuit structure is shown in Fig. 2.27 [4, 41]. NRZ data is changed to RZ data first, then fed to a high-Q filter. The output of that filter will be the clock to be recovered. The disadvantages of this structure are that, the noise power in the vicinity of f_B will also pass through the filter and corrupt the clock; it doesn't have the ability to adjust itself to the bit rate deviation from the designed one; and the most important thing is, it cannot be integrated onto a chip.

Fig. 2•27• Conventional clock recovery structure

The above problem can be solved with a PLL based clock recovery structure [41]. It can be easily integrated, but data and clock outputs have large jitter caused by the random feature of the input data stream, and the loop easily loses lock also for the random input patterns. A lot of effort has been put to create new PLL structures suitable for clock recovery applications [2, 12, 41-52]. Any of the clock recovery structures can be classified as one of delay-locked loop (DLL), Delay- and Phase-locked loop (DPLL), PLL, or Hogge PLL.

2•3•2• Clock recovery with PLL

PLL based clock recovery structures are shown in Fig. 2.28. The application of PLLs to clock recovery has some special design considerations. Because of the random nature of data, the selection of PD is restricted [4]. For example, three-state PDs will not work for the PLL based clock

recovery applications; in high noise applications, a multiplier is usually used as a PD; in low noise applications, a simple XOR gate can be used to replace the relatively complicated multiplier; a two-state PD can help to suppress the random data pattern related jitter. Frequency detectors [5,10,11] should be included with PDs to form PFDs in order to aid the loop lock acquisition.

Fig. 2•28• PLL based clock recovery structures

The dilemma [50,52] with the design of PLL based clock recovery applications is that the data randomness causes output jitter in the recovered clock; in order to suppress the jitter, the PLL should have a narrow bandwidth (BW); in turn the narrow bandwidth will cause longer acquisition time, which creates a problem especially for a random data (burst mode) clock recovery system. Usually a preamble data bits (data transition density is 100%) is used to aid the PLL to acquire the lock.

The advantages of PLL based clock recovery are that, it can be fully integrated, and it has the tracking ability to adjust the bit rate deviation. The PLL theory is very well understood and practised. This theoretical background facilitates new circuit technique explorations as well as new

processing technology trials [2,12,41-52], and leads to the reduction of PLL power consumption, output jitter, and locking acquisition time, increase of PLL top operating frequency, and so on.

The disadvantages are the circuit complexity, high output jitter, high power consumption, and high design cost.

2.3.3• Hogge clock recovery structure

Strictly speaking, Hogge clock recovery structure [12] is also a PLL. A Hogge PD is used inside this kind of clock recovery structure, and makes it possible to recover clock directly from NRZ data. A block diagram of Hogge structure is shown in Fig. 2.29. The principle of Hogge PD will be discussed in the following chapter.

Fig. 2.29• Hogge clock recovery structure

In most clock recovery structures, the recovery of the synchronous clock from NRZ data requires a nonlinear process since the spectrum of the NRZ signal is a continuous $(\sin x)/x$ function with no predominant clock related component. The conventional approach to this problem is to pass the NRZ signal to an NRZ-to-RZ converter [4] to produce a reference signal having a strong component at the clock frequency. Then the newly generated RZ signal is filtered with a narrow bandwidth PLL, or a high-Q filter. In any of these cases, clock extraction occurs in a spur circuit off the data path and the alignment of the clock in the centre of the data “eye” is not self correcting. In the

Hogge clock recovery structure, the Hogge PD uses the same flip-flop, which is the integral part of the Hogge PD, to detect the incoming data synchronously and make a jitter tolerant logic decision at each clock period. The Hogge PD in a PLL forces the clock to be positioned at the centre of the data eye and is inherently self correcting.

Hogge PLL constitutes a complete clock recovery circuit. Any clock recovery architecture can be simplified when the Hogge clock recovery structure is used.

The main disadvantages are that, the conversion gain of the Hogge PD is determined by the random data transition density, and the Hogge PD is not a PFD. The Hogge clock recovery circuit needs to use an additional sweep acquisition circuit to assist lock acquisition.

The Hogge PD will be discussed in detail in the following chapter.

2.3.4• DLL or DPLL based clock recovery

The difference between a PLL and a DLL is that the VCO is replaced by a voltage-controlled phase shifter (VCPS) [51]. For PLL based clock recovery, the power supply noise-induced jitter is very hard to deal with, and acquisition time is often very long due to the time it takes to drive the VCO to the correct frequency. DLL based clock recovery can help to overcome these problems and achieve a low jitter and low rail noise sensitivity recovered clock and can be applied to high noise applications. A very stable external reference clock (its frequency is equal to the input data bit rate) is required for this system. The DLL can be used to align data with the reference clock. The phase shifted data can also be processed to recover the clock.

A DLL also can be combined with a PLL to form a DPLL [50]. By doing so, the good points of both DLL and PLL circuits can be combined to achieve a good jitter filtering without compromising acquisition speed.

Another data recovery technique, called matched delay sampler, was also reported [49]. It is a digital implementation of data recovery. To assure accurate sampling of data, a DAC is used to delay the standard reference clock and to align it with the input data. A multiple input and output digital PLL is used to recover the data from the sampled data. A controller is used to compare the phase of the multiple outputs from the PLL and control the DAC to control the delay unit to align the input clock. The delayed clock is the recovered clock. This method can be applied for high data rate clock recovery. The problem is that the standard reference clock frequency has to be exactly equal to the data bit rate.

2.4. Summary

Basic PLL theory, circuit structure options for the PLL building blocks, and the development of frequency synthesis and clock recovery design techniques have been reviewed. It is believed that phase-locking is one of the best choices for the design of frequency synthesizers and clock recovery circuits, even though many problems still exist. By introduction of new circuit building techniques and with the development of new manufacture processes, these problems are being solved gradually. In this thesis, the author undertakes to research the following aspects for the design of frequency synthesis and clock recovery applications:

- Fully integrated continuous-time LF with on-chip automatic tuning.
- High speed frequency prescaler with moderate power consumption.
- High speed Hogge PD with proper linear range.
- PLL simulation with SPW.

The research results are reported in the following chapters.

CHAPTER 3

High speed circuit design techniques

In order to push the phase-locking applications to higher operating frequency ranges, phase detectors and prescalers should be designed to meet the speed requirements while meeting low power consumption and low design cost requirements. Dynamic circuit structures can be chosen to achieve that goal. In this chapter, several digital dynamic techniques [53-58] will be reviewed and evaluated.

3.1• Basic dynamic structure

Fig. 3.1• Building blocks of the basic dynamic structure

The dynamic logic is a precharging (or predischarging) and clocked logic, as shown in Fig. 3.1. For the logic circuit shown in Fig. 3.1(a), when signal *clk* is low, precharging occurs; when signal *clk* is high, evaluation occurs. For the logic circuit shown in Fig. 3.1(b), when signal *clk* is

high, predischarging occurs; when signal *clk* is low, evaluation occurs.

Two building blocks of either Fig. 3.1(a) or Fig. 3.1(b) together will form a latch, and two blocks of both Fig. 3.1(a) and Fig. 3.1(b) together will form a D flip-flop, as shown in Fig. 3.2.

d_inv1 and *d_inv2* are defined in Fig. 3.1.

Fig. 3.2• Dynamic D-latch and D-flip-flop

The advantage of the basic dynamic structure over its static CMOS counterpart is that it only has one PMOS transistor for precharging or one NMOS transistor for predischarging. So the transistor count is reduced, speed is increased, and power consumption is lowered.

The limitation of this structure is that the logic functions must be monotonously inverting. Thus, turning on a switch in the pull-down (pull-up) network can leave the output unchanged or pull-down (pull-up) but never push it back. Also, since the dynamic circuits use parasitic capacitance to store information, charge sharing can cause glitches or even cause malfunction. In dynamic circuits, charge sharing is considered potentially difficult to optimize.

3.2• Clocked CMOS (C²MOS) structure [54]

The basic building block of the clocked CMOS structure is shown in Fig. 3.3. In Fig. 3.3, a clock and its inversion phase are required to work as synchronization clocks. In order to form a

latch or a flip-flop, more basic building blocks are needed. In this case, the clocks between two adjacent basic building blocks should be non-overlapping. For this reason, four clock signals have to be distributed in such a system built with the clocked CMOS logic. Clock skews in this type of system could cause serious problems and typically result in difficulties in increasing circuit speed. For those reasons, the clocked CMOS logic is not recommended for high speed applications.

Fig. 3.3• Basic building block of the clocked CMOS (C²MOS) structure

However, the C²MOS dynamic structure reduces some of the problems existing in the basic dynamic structure discussed in section 3.1, such as charge sharing and monotonousness at the expense of one more transistor added to the basic building block. It is considered a good choice for applications in a low frequency range.

3.3• Domino structure [55]

From Fig. 3.1, it can be observed that the outputs of the building blocks are the inverted reversion of inputs. Adding static CMOS inverters to the outputs of those building blocks creates another dynamic logic family, called the Domino structure. The Domino structure constitutes an I/

O consistent class of circuits.

The Domino structure still has charge sharing problems like the basic dynamic structure. Dynamic circuits usually use small size transistors which result in smaller current driving capability. By adding static inverters, the drivability of dynamic circuits can be improved. The overall circuit speed also increases.

Fig. 3•4• Basic building block of the Domino structure

The non-inverting property of Domino structure does not allow constitution of a complete family of logic elements.

3•4• NORA (NO RAcE) structure [54]

The building blocks of the NORA structure are shown in Fig. 3.5. The NORA dynamic CMOS technique uses a true two-phase-clock signals clk and $\overline{clk}$ instead of a four-phase-clock used in the clocked CMOS structure. For this reason, it is expected that the NORA dynamic structure can operate faster than the clocked CMOS dynamic structure. Also, the NORA dynamic structure overcomes Domino's restriction to non-inverting logic gates.

The basic NORA building blocks are *n-latch* (Fig. 3.5(a)) and *p-latch* (Fig. 3.5(b)). The

n-latch has an n-block followed by a clocked CMOS inverter. The *p-latch* has a p-block followed by a clocked CMOS inverter. A more complicated logic can be formed by alternating n-blocks and p-blocks followed by a clocked CMOS inverter at the end. Because of this feature, the NORA structure can have a race problem caused by clock skews removed with those logic composition rules.

Fig. 3•5• Building blocks of the NORA structure

The NORA structure is very sensitive to charge sharing and capacitance coupling, caused by a floating node driving another floating node. Thus, the signal is not restored to full rail voltage levels, as in the Domino structure where the static inverter restores the levels. Another drawback of the NORA structure is the need of an inverted clock signal and the use of p-blocks. Moreover, if an output of an n-block has to be connected to another n-block, one has to use a clocked CMOS inverter to buffer it as in the Domino logic. The same rule holds for connection between two p-blocks, in which case, the two clocks for the clocked CMOS inverter need to be swapped.

3.5• TSPC structure

The dynamic logic structures discussed up to this point all require two or more clocking signals. Further improvement requires simplification of the clocking scheme. The true single-phase clocking (TSPC) technique was developed. The TSPC dynamic structure uses only one clock signal. The absence of the inverted signal results in removal of the clock skew problem except for clock delay. Higher clock frequency can therefore be reached. This technique overcomes most of the problems of the above 4 dynamic structures. It is compatible with not only dynamic but also static CMOS circuits, and can replace all of early discussed dynamic structures in most applications. The TSPC structure development can be classified into the following four types.

3.5.1• Clocked CMOS derivative — Single-Phase Dynamic Logic [53]

Fig. 3.6• A dynamic D-flip-flop with inverting output

The basic circuit element of this structure type is a dynamic D-flip-flop with inverting out-

put, as shown in Fig. 3.6. This circuit consists of three stages. The input signal enters a p-C²MOS stage, the C²MOS stage is followed by an n-C²MOS stage. There is no signal transparency existing from input to output in that circuit, so a proper D-flip-flop is formed. Any arbitrary block can be designed in this technique. A single-phase n-latch and a single-phase p-latch are shown in Fig. 3.7.

Fig. 3•7• n-latch and p-latch circuits

3•5•2• NORA derivative — Single-Phase Precharge Logic [53]

A typical TSPC structure type derived from the NORA structure is shown in Fig. 3.8. The basic logic unit consists of an n-block performing the precharging and logic functions and an n-C²MOS stage performing latching. This basic n-unit must be followed by an inverted type unit, a p-unit, consisting of a p-block followed by a p-C²MOS stage. The output of the n-unit can drive any p-unit input and vice versa.

In case of n-unit, low value of *clk* signal causes n-block to be precharged. Its n-C²MOS stage is off while the output remains stable. When signal *clk* transits from low to high, the n-block evaluates and the n-C²MOS passes the signal. In case of p-unit, high value of *clk* signal causes p-block to be precharged. Its p-C²MOS stage is off while the output remains stable. When signal

clk transits from high to low, the p-block evaluates and the p-C²MOS block passes the signal. It should be noted that deep cascading of logic blocks can reduce the speed of TSPC circuits.

Fig. 3•8• A pipeline of precharged logic circuits using the single phase clock

3•5•3• Domino derivative — Single-Phase Precharge Logic [53]

In the TSPC structure type described in the above section, the output of the n-unit cannot be used to drive another n-unit using the same clock. However, a p-unit using the same clock will act exactly as an n-unit using the inverted clock, so a p-unit can follow an n-unit without causing any performance deterioration. Thus, by ensuring that the n-unit always drives the p-unit and vice versa, all units can be driven by the same clock, they form a true single-phase-clock (TSPC) structure. For two n-blocks to drive each other and share the same clock, an inverter can be used to isolate the output of one n-block from the input of the other n-block. This means that, directly cascaded n-blocks of the Domino structure also forms a TSPC structure. Such an arrangement is shown in Fig. 3.9. As in simple phase precharge logic, excessive logic depth can also have a negative effect

on the operating speed, as the Domino structure itself is very sensitive to the charge sharing effect.

Fig. 3.9• Directly cascaded n-blocks of the Domino structure using the single phase clock

3.5.4• Improved TSPC structure — Simplification of all above [54]

By splitting the output of selected logic stages and applying synchronization clock to NMOS and PMOS transistors alternatively between adjacent logic stages, the TSPC circuits can be simplified. These new circuits cannot be classified into one of the three types of TSPC structures discussed above. In this thesis, they will be called an improved TSPC structure. For example, the *n-latch* and *p-latch* circuits shown in Fig. 3.7 can be simplified to the circuits shown in Fig. 3.10, and a TSPC D-flip-flop circuit derived from the NORA structure can be simplified to the circuit shown in Fig. 3.11. The advantages of this improved TSPC structure are that the output logic stage has only two transistors, the logic levels and drivability can hence be improved; one transistor in each building block can be saved; it also offers a new logic composition rule. The disadvantages are that this improved logic circuit uses more PMOS transistors resulting in an increased layout ar-

ea; the optimization can also be difficult. It is believed that this improved logic version can give the best performance of all. This improved TSPC structure does not employ charge sharing, has good current drivability, and is characterized by higher speed and a smaller implementation area.

Fig. 3•10• n-latch and p-latch circuits of the improved TSPC structure

Fig. 3•11• D-flip-flop circuit of the improved TSPC structure

3•5•5• Summary of the TSPC technique

The single-phase precharge logic normally has no charge sharing problem. The negative charge sharing effect can only occur in Domino based TSPC logic. They can be however avoided

if the clock signals between n-blocks are connected to the transistor closest to the clocked n-transistor in the proceeding n-block. The reason is that these input signals can change at the same time as the n-block starts to evaluate. The same condition applies to the p-block.

The true single-phase-clocking strategy has advantages of a simple and compact clock distribution, high speed and logic design flexibility. The maximum operating speed can be affected by the logic cascading depth and transistor sizes. In order to reach a higher operating speed, the logic depth needs to be minimized, and the transistor sizes to be increased [58].

3.6• Summary

The dynamic logic structures are suitable for high-speed digital design. The dynamic structure uses the parasitic gate capacitance to store the information, has fewer transistors per building block compared with its static counterpart, resulting in higher speed and lower power consumption. In the precluding chapter, a review of dynamic structures is given, and an ordinal analysis is also performed. The frequency synthesis and clock recovery building blocks, the Hogge phase detector and frequency prescaler, often use TSPC techniques and this will be discussed in detail in the following chapters.

CHAPTER 4

Fully integrated LF design and its automatic tuning

4.1• The functions of LFs in the PLL based applications

In a PLL, the conversion gains of the phase detector and VCO are predetermined by circuit design. Typically, only the loop filter (LF) gain and its filtering parameters can be adjusted. The transfer function of the most popular LF is given in equation (4.1).

$$H(s) = K_h \frac{s + \omega_2}{s(s/\omega_3 + 1)} \quad (4.1)$$

If a PLL employs a LF with the transfer function as defined by equation (4.1), the PLL performance can be adjusted by adjusting the values of K_h , ω_2 and ω_3 . The loop bandwidth of this PLL becomes:

$$\omega_{3dB} = K_h \times K_d \times K_0 \equiv K \quad (4.2)$$

Where,

K_d — the conversion gain of the PD expressed in unit of volts per radian,

K_0 — the VCO conversion gain in unit of radians per second per volt,

K_h — the LF AC component attenuation coefficient.

By using ω_2/K as a reference, the frequency response of the PLL can be classified into three types [4]: over damping, critical damping, and under damping.

The order of the PLL is also determined by the order of LF. If there is no filter in a PLL, that is, $H(s)=1$, the PLL is said to be of first order. If a first order LF is inserted into a PLL, the PLL is of second order, and so on. It can be stated that the order of a PLL system is equal to the order of

the filter plus one. A second order PLL can satisfy most of PLL based applications. Higher order PLLs are potentially unstable and are considered difficult to analyse.

The LF is an important component of a PLL, as it determines the PLL's BW, frequency response type, locking range, capture time, stability and so on.

4•2• Integration techniques for the LFs

After so many years of practice, designers have accumulated a large number of filter design models [59] and filter integration methods [60-62]. The filter integration methods can be classified into three main groups:

- continuous-time filters,
- digital filters (quantized),
- switched-capacitor filters (discrete time).

In order for an integrated filter to work as a loop filter for a PLL, the continuous-time type may be the only effective choice. Each type of integration method will be discussed separately below.

4•2•1• Loop filter integration discussion

A loop filter is only a small part of a PLL circuit. It should have a small size, low power consumption and easy adjustment. It also needs to be compatible with various types of PD outputs: small signal or large, continuous output or width-variant pulse.

4•2•1•1• Switched-capacitor filters

Theory has shown that, when the sampling frequency is much higher than the frequency of the signal being sampled, a switched-capacitor (as shown in Fig. 4.1) can form a very precise

resistor. Switched-capacitor circuits can therefore be used to form the basic units of filters: the integrator, the summer, the inverter and so on.

Fig. 4•1• Switched-capacitor diagram

The whole switched-capacitor filter system is shown in Fig. 4.2. It requires two continuous-time filters to work as antialiasing and smoothing filters. It will also need a complicated clock generator to offer two non-overlapping clocks to serve as sampling signals.

Fig. 4•2• Switched-capacitor filter system as a loop filter

From the above diagram it can be seen that switched-capacitor filter could be too complicated to be used as a loop filter. For the modern PLL-based personal communication applications, the VCO working frequency is high (several hundred MHz), the frequency of the output of phase detector will double that frequency. In order to make the switched-capacitor resistor precise

enough, the sampling frequency should be about 10 times of the phase detector output frequency. The sampling frequency could reach the 10 GHz range. This is nearly impossible for current technology to produce such a switched-capacitor filter operating at such a high frequency. The cost, the size, the power consumption, and the technology, etc. make it an undesirable choice.

4•2•1•2• Digital filters

A digital loop filter is shown in Fig. 4.3. It can be seen that this also is a very complicated system. In order to process the output of the PFD, an A/D converter is needed to interface between the digital filter and the PFD. In order to control the VCO, another D/A converter is needed to interface between the digital filter and the VCO. If the phase detector output is a pulse, the pulse will have a random width. If the phase detector output is to be sampled just at the Nyquist frequency, the sampling instant could be early and miss the pulse. This will cause a large PD dead zone. In order to minimize the dead zone, the sampling frequency needs to be increased by several times. As discussed in the switched-capacitor filter section, this in turn requires a very high clock frequency for the whole digital filter system. The cost, the size, the power consumption, the technology etc. also make a digital loop filter an undesirable choice.

Fig. 4•3• Digital filter system as a loop filter

4.2.1.3• Continuous-time filters

For continuous-time filters, no sampling scheme is needed, so no aliasing problems are present and no pre- or post-filtering is required as in the switched-capacitor filter case. One can just try to use the components (within a given integration process) to form the resistors, capacitors and amplifiers needed. The characteristics of continuous-time filter is determined by the precision of both the integrating constant of the integrator and the DC gain of the lossy integrator. Usually, the integrated resistors and capacitors are not precise, their values vary with the process and operating environment. This makes the accuracy of these kind of filters in the order of 30-50%. This is the main disadvantage of the continuous-time filters. So for continuous-time filters, in order to maintain a stable frequency response, a tuning scheme needs to be integrated with these filters, and this requirement will complicate the continuous-time filter design. Several techniques have been developed to monolithically implement continuous-time filters. They can be divided into RC active filters, MOSFET-C filters and OTA-C filters.

a) Integrated passive or active RC filters

RC active filters are commonly used in low-frequency applications. These filters use OPAMPs, resistors and capacitors as basic components. In integrated circuits, the resistors can be implemented either as diffused or polysilicon resistors. Capacitors can be implemented by gate polysilicon plate capacitors. The absolute accuracy of the resistance is in the order of 30-50%. The linearity of the poly-silicon resistors is quite good and the accuracy of resistor ratios can be as good as 1%. But the RC product can be as bad as 50% and depend heavily on both technology tolerances and temperature variations. The poles and zeroes of filters are determined by the RC product, so the poles and zeroes also have large errors as the RC product changes. Typically, the quality factor of the filter is determined by the resistor and/or capacitor ratios, so the quality factor can be very

precise. The frequency response is determined by poles and zeroes, so the integrated RC active filters have very low accuracy. A tuning scheme should therefore be advised in order to obtain a relatively precise frequency response.

All the off-chip passive and active RC filters can be transplanted onto the chip by replacing all the resistors and capacitors with chip version resistors and capacitors. The VLSI version resistors and capacitors mentioned here usually are 2-terminal devices, and don't have a control terminal, so an automatic tuning scheme is not available. In this kind of transplantation, capacitor banks can now be used to replace each capacitor in the original design. A tuning circuit digitally tune some switches on and some off. The tuning accuracy is determined by the resolution of the banks. A reasonable size of banks can tune frequency response to an accuracy of 5% [63]. This scheme is shown in Fig. 4.4.

Fig. 4•4• Passive or active RC loop filter with tuning

Many mature off-chip loop filter designs are known in the design practice. By using the scheme discussed here, one can transplant them directly onto the chip. Successful designs based on such a concept are already reported [63-65].

b) MOSFET-C filters [66-69]

The MOSFET-C filters are basically active RC filters, but with the resistors implemented by equivalent voltage-controlled NMOS tunable resistors that are biased in the linear region. Due to the use of simulated resistors, buffered low output impedance OPAMPs have to be employed. This means at least two-stage OPAMPs have to be used. The frequency response is limited by two or more stages of OPAMPs and limit this type of filter design to the low frequency range. The basic integrator structure for MOSFET-C filters is shown in Fig. 4.5(a).

Fig. 4.5• MOSFET-C integrator structure

Active RC filter designs can be converted into MOSFET-C filters by the above mapping technique. For better linearity, immunity to substrate noise and common-mode offsets, an improved integrator shown in Fig. 4.5(b) can also be used.

For MOSFET-C filters, the resistor linearity is a primary concern. The NMOS substitution resistors have to be biased in the linear region. What is also required is that the input signals must be small in order not to drive NMOS transistors into the pinch-off region. MOSFET-C filters are not suitable to extract the DC component from large amplitude pulses at the phase detector output. For those reasons, they will not be considered as a design technique to implement the PLL loop

filter.

c) OTA-C filters [70-74]

The OTA-C filter technique is more versatile than the MOSFET-C technique. It allows design of filters to operate from very low frequencies to very high frequencies. OTA-C filters have only two building blocks, operational transconductance amplifier (OTA) and capacitance (C). OTA is a voltage to current transducer with a very high output impedance. The capacitor can be implemented in many available VLSI technologies. In the following paragraphs, OTA and C symbols shown in Fig. 4.6 are used.

Fig. 4.6• (a) OTA symbol (b) Equivalent circuit of ideal OTA (c) C symbol

The OTA transconductance, g_m , is proportional to the control current, as given in equation (4.3).

$$g_m = kI_c \quad (4.3)$$

The proportionality constant k depends on the working temperature, device geometry and the process. The OTA output current is given by equation (4.4).

$$I_0 = g_m(V_+ - V_-) \quad (4.4)$$

The OTA-C filter frequency response is determined by g_m and C . Tuning of OTA-C filters can be accomplished by varying the control current I_c .

Basic OTA-C filter building blocks are shown in Fig. 4.7.

(a) Differential-input OTA-C integrator

(b) OTA summer

(c) OTA basic inverter

(d) OTA basic non-inverter

(e) OTA grounded resistor

(f) OTA floating resistor

Fig. 4•7• OTA-C basic building blocks

By using one or more of the OTA-C building blocks, any off-chip RC passive and active loop filters can be translated into their corresponding OTA-C version. By controlling the OTA control current, the filter can be tuned to operate in the desired frequency range. The current dependence of the OTA transconductance also allows the introduction of automatic tuning techniques as discussed in the following section.

4•2•2• Tuning schemes [60, 75-77]

Tuning techniques can be divided into two main categories.

4•2•2•1• Direct tuning

The first direct tuning method uses capacitor banks to adjust the possible capacitance de-

viation of the integrated capacitors. This method has been mentioned in the former section.

The second direct tuning method is illustrated in Fig. 4.8. This technique employs two identical filters. While one filter is placed in the signal path, another is tuned by the on-chip tuning circuit. After a period of time, the control circuit switches the filter in the signal path and the filter being tuned. This process continues as long as the filter is powered. Since the working filter is tuned directly, this is considered a very precise tuning method.

Fig. 4.8• One of the direct tuning schemes

4.2.2.2• Indirect tuning

In the indirect tuning technique, the main filter itself is designed by using g_m - C building blocks. The control or the reference block is designed to closely match the main filter. Both of them need to be in the same process environment and temperature environment, and they can encounter the same process and operating disturbance. Through this kind of matching, any disturbing factor will influence the filter and the sensing component of the tuning circuit at the same time. The tuning circuit adjusts the control voltage of the sensing component to the desired, predetermined value. The same voltage is also applied to the voltage control terminal of the filter in order to cancel the influence of the disturbance on the filter. Some of the currently used indirect tuning schemes are

shown in Fig. 4.9.

Fig. 4.9• Indirect tuning schemes

In Fig. 4.9(a), an OTA transconductance is used as a tuning state detecting component. The tuning circuit adjusts the resistance of the transconductor until it is equal to the resistance of the external reference resistor.

In Fig. 4.9(b), the filter designer usually uses two integrators to form a VCO through a proper positive feedback connection to work as a detecting component. The tuning circuit is a PLL. By tuning the VCO frequency to the precise input reference frequency, the signal path integrator RC product can be stabilized, yielding stability of the filter.

In Fig. 4.9(c), the detecting component is a voltage-controlled filter (VCF); it can be the same structure as the main filter, and also can be a different structure, but has to be constructed with the same building blocks. The input reference clock will be divided into two signal channels. One goes to the phase detector directly. Another goes through the VCF first, then goes to the phase detector. At the output of the filter, a phase difference will be generated relative to the other channel. The phase difference is converted to the tuning voltage by the phase detector. When the VCF RC product changes, the phase difference also changes. If the tuning loop has a large enough gain, the loop will quickly tune the phase difference back to the former value, and get the RC product of the

whole system tuned at the same time.

In Fig. 4.9(d), a special integrator is used. V_R is a constant voltage used as reference. If the R or C in the integrator changes its value, V_C will change. This change will bring change to the frequency of the two non-overlapping clocks which are used to control the switched-capacitor (SC). The feedback action stabilizes the V_C voltage. The RC product of the system is also stabilized. This scheme can be used to tune the filters designed with fixed Rs and Cs but can be tuned by voltage.

4.2.3• Currently available practice on loop filter integration

In most reported PLL designs, on-chip passive RC loop filters are the choices. They don't have any tuning, occupy a large die area, usually use charge pumps to achieve infinity DC gain. In some cases where active loop filters are required, off-chip active filters or off-chip resistors/capacitors are employed to achieve the design goals. Fully integrated on-chip active loop filters with automatic tuning are rarely reported.

In [15], an OTA-C type loop filter was designed, and only simulation results were presented. No measurement results are available. This loop filter circuit is shown in Fig. 4.10. It is equivalent to a first-order low-pass passive RC filter.

In [41, 79, 80]], integrated loop filters which have the structure shown in Fig. 2.17(b) were reported. In order to achieve a very low frequency pole for the first-order passive RC low-pass filters, large resistance and capacitance are required. The on-chip resistors and capacitors occupy most of the total die area for the whole PLL design.

In [78], an integrated active loop filter which has the structure shown in Fig. 2.19 was reported. A voltage-controlled resistor is used. The resistor structure is shown in Fig. 4.11. This active structure can reduce a lot of die area occupied by the loop filter. The control input also gives some

flexibility to adjust the frequency response of the loop filter externally.

In [81], an on-chip second order passive RC loop filter was reported. The circuit is shown in Fig. 4.12. Two capacitors and one resistor also occupy most of the die area for the whole PLL design.

In [82], an OTA-C integrated loop filter was reported and no detailed circuit is available.

In [83], an integrated loop filter which has the structure shown in Fig. 2.17(c) was reported. Three resistors and one capacitor also occupy most of the die area for the whole PLL design.

All the above reported integrated loop filters don't have any tuning circuits.

Fig. 4•10• Schematic of loop filter based on a transconductance amplifier

Fig. 4•11• On-chip variable-resistance circuit

Fig. 4•12• Second-order loop filter

4.3• OTA and OPAMP circuits design

The operational transconductance amplifier (OTA) is the basic building block for the OTA-C type filter. Generally, the OTA circuit can be formed by a basic differential pair followed by a cascode structure. The reason for this can be stated in three points. First, the operational amplifier does not have the level shift problems that the basic differential pair does. It can be designed without offset. Second, the addition of the output stage increases the output impedance and increases the DC gain. This makes the OTA circuit behave more like real VCCS and allows the low frequency pole to be at a frequency much lower than the frequency of interest. Third, with the use of the operational amplifier, both double-ended and single-ended filters can be constructed.

4.3.1• Cascode OPAMP

Fig. 4.13• Simple cascode stage

A typical implementation of a simple cascode amplifier is shown in Fig. 4.13. A cascode configuration increases the voltage gain due to increased effective output impedance.

The gain of the above cascode structure is proportional to the product of g_{M1} and R_{OUT1} . The load also has to be cascoded ($M5$ and $M7$) in order to increase its effective impedance to a level comparable to the driver pair ($M1$ and $M3$). The great advantage of cascode is that it operates in current mode, and the bandwidth is very stable. The main limitation of the cascode structure is that a high power supply voltage is needed to achieve a given output signal amplitude. The maximum output amplitude is $V_{dd} - 2*V_{DSATp}$. The minimum output amplitude is $V_{ss} + 2*V_{DSATn}$. V_{DSATp} and V_{DSATn} are the saturation voltages of PMOS and NMOS transistors respectively. So when designing a cascode amplifier, the main design goal is to maximize the output dynamic range without degrading other properties of the amplifier. This can be achieved by properly selecting the bias voltages inside the cascode circuits: $VB3$, $VB4$ and $VB5$.

4.3.2• Basic OTA structures

The cascode amplifier is the core of OTA amplifiers. A combination of cascode and basic differential pair is used in many types of analog building blocks. The two well-known structures are: the folded-cascode and the telescopic-cascode [62]. Their circuit structures are shown in Fig. 4.14 and Fig. 4.15 respectively.

There is no significant difference in operating principles of these two structures. The main shortcoming of the telescopic cascode structure is that it requires one more stage between V_{dd} and V_{ss} than the folded-cascode does. This means that both its input dynamic range and its output dynamic range are smaller. In the research reported here, the telescopic cascode structure is chosen as the basic OTA structure. Two points contributed to this decision:

Power dissipation: In the folded-cascode structure (Fig. 4.14), the pair $M9$, $M10$ has to carry at least two times of current as $M0$. Otherwise one of the transistors in the pair $M3$, $M4$ may turn

off under large input signal conditions, thus increasing the recovery time during a transient.

Die area: Compared to the folded-cascode, the telescopic cascode structure (Fig. 4.15) has fewer transistors and makes a smaller die area possible.

Fig. 4•14• Folded-cascode OTA with differential outputs

Fig. 4•15• Telescopic cascode OTA with differential outputs

In this project, a single-ended telescopic cascode is employed to design a loop filter. The

circuit schematic is shown in Fig. 4.16.

Fig. 4•16• Telescopic cascode OTA with single output

In order to achieve the best output dynamic range for the telescopic cascode, *M3* and *M4* have to be biased in such a state as to leave the input pair *M1* and *M2* and the common-mode transistor *M0* biased just above their saturation voltages.

The chosen telescopic cascode structure was designed in the 0.8 μ m BATMOS (CMOS used) technology. The structure is to achieve an intended transconductance, and was optimized to realize maximum possible DC gain in the integrator configuration. The sizes of all the transistors in the telescopic cascode were chosen according to relations shown in Table 4.1.

The optimized sizes ensure that the balance within the cascode is maintained. The designer can determine the ratios (W/L) according to the magnitude of the bias current and desired transconductance. Optimization of the DC gain of the OTA in an integrator configuration can then be performed by changing the value of variable x .

Transistor	size
M0	$(2*W*x)/(L*x)$
M1, M2	$(W*x)/(L*x)$
M3, M4	$(W*x)/(L*x)$
M5, M6	$(W*x)/(L*x)$
M7, M8	$(W*x)/(L*x)$

Table 4.1. Telescopic OTA transistor size arrangement

In Table 4.1, the L of W/L ratio is set to $L = 0.8 \mu\text{m}$, W is in microns, and x is unitless.

4.3.3. OTA input differential pair design

The basic square law drain-source current equation for a MOS transistor in the pinch-off state is given by:

$$I_{ds} = \frac{\mu C_{ox}}{2} \left(\frac{W}{L} \right) (V_{gs} - V_T)^2 = \frac{\beta}{2} \left(\frac{W}{L} \right) (V_{gs} - V_T)^2 \quad (4.5)$$

Where μ is the minority carrier's mobility, C_{ox} is the capacitance between gate and substrate, (W/L) is the size of the transistor, V_T is the threshold voltage of the transistor, β is the product of μ and C_{ox} .

Taking the derivative of equation (4.5) with respect to V_{gs} , transconductance of the transistor is obtained.

$$g_m = \frac{dI_{ds}}{dV_{gs}} = \beta \left(\frac{W}{L} \right) (V_{gs} - V_T) = \sqrt{2\beta \left(\frac{W}{L} \right) I_{ds}} \quad (4.6)$$

In a given design, the required magnitude of g_m can be determined from the required 3 dB

frequency and the value of the capacitance chosen for integration by using equation (4.7).

$$g_m = \omega_{3dB} C \quad (4.7)$$

From other specifications (such as power, dynamic range etc.), the bias current can be determined. Next the transistor sizes can be calculated.

The square law equation of the transistor in pinch-off state can also be used for an approximate analysis of the input dynamic range, cutoff voltage and linearity of the input differential pair. The differential pair is shown in Fig. 4.17.

Fig. 4.17• Differential pair input stage

The currents through the input transistors of this differential pair can be denoted as i_1 and i_2 . i_1 and i_2 in turn can be expressed as functions of input voltages V_1 , V_2 and V_s . The sum of i_1 and i_2 must be equal to the bias current I_B through $M0$. These corresponding equations are:

$$i_1 = \frac{\beta}{2} \left(\frac{W}{L} \right) (V_1 - V_s - V_T)^2 \quad (4.8)$$

$$i_2 = \frac{\beta}{2} \left(\frac{W}{L} \right) (V_2 - V_s - V_T)^2 \quad (4.9)$$

$$i_1 + i_2 = I_B \quad (4.10)$$

The above three equations can be combined to eliminate V_s and i_2 to give the basic square law equation that can be used to describe the differential pair, as expressed in equation (4.11).

$$\sqrt{\frac{\beta}{2} \left(\frac{W}{L} \right)} (V_1 - V_2) = (i_1)^{1/2} - (I_B - i_1)^{1/2} \quad (4.11)$$

By setting i_1 to either I_B or zero in equation (4.11), equation (4.12) is obtained.

$$|V_1 - V_2| = \left(\frac{I_B}{\frac{\beta}{2} \left(\frac{W}{L} \right)} \right)^{1/2} \quad (4.12)$$

Equation (4.12) determines the input dynamic range. By increasing the bias current I_B and decreasing W/L ratio, the input dynamic range can be improved while keeping the transconductance g_m constant.

If i_1 is equal to I_B minus a small quantity ΔI and i_2 is equal to I_B plus a small quantity ΔI , equation (4.11) can be re-arranged to give equation (4.13).

$$\sqrt{\frac{\beta}{2} \left(\frac{W}{L} \right)} (V_1 - V_2) = (I_B - \Delta I)^{1/2} - (I_B + \Delta I)^{1/2} \quad (4.13)$$

Since ΔI is a small quantity, a binomial expansion of the right side of equation (4.13) can be performed to analyse the linearity of the differential pair. In this work, the design objective is to create a low pass filter for PLL. This filter will be used to remove higher frequency components of the signal, thus linearity is not a major concern in this design.

4.3.4. OTA bias circuit [62]

In the telescopic cascode, five different bias voltages are required: $VB1$ through $VB5$.

Those are:

$VB1$: set one V_{GSn} above V_{ss} (i.e., $VB1 = V_{GSn} - V_{ss}$),

$VB2$: set one V_{DSATn} above $VB1$ (i.e., $VB2 = V_{DSATn} + V_{GSn} - V_{ss}$),

$VB3$: set two V_{DSATn} above $VB1$ (i.e., $VB3 = 2 * V_{DSATn} + V_{GSn} - V_{ss}$),

VB5: set one V_{GSp} below V_{dd} (i.e., $VB5 = V_{dd} - V_{GSp}$),

VB4: set one V_{DSATp} below **VB5** (i.e., $VB4 = V_{dd} - V_{GSp} - V_{DSATp}$).

VB1 is generated simply by forcing the desired OTA bias current through a diode-connected transistor (called **I1**) with a dimension ratio (W/L) identical to that of **M0** in the OTA circuit. **VB2** is generated also simply by forcing the desired OTA bias current over a diode-connected transistor (called **I2**) with one quarter of the W/L dimension ratio of **M0**. The following equations provide the analytical justification.

$$V_{GS11} = \sqrt{\frac{2I_0}{\beta_{I1}}} + V_T \quad (4.14)$$

$$\beta_{I2} = \beta_{I1}/4 \quad (4.15)$$

$$V_{DSATn} = V_{GS11} - V_T = \sqrt{\frac{2I_0}{\beta_{I1}}} \quad (4.16)$$

$$V_{GS12} = \sqrt{\frac{2I_0}{\beta_{I2}}} + V_T = 2\sqrt{\frac{2I_0}{\beta_{I1}}} + V_T = V_{GS11} + \sqrt{\frac{2I_0}{\beta_{I1}}} = V_{GS11} + V_{DSATn} \quad (4.17)$$

VB5 and **VB4** can be generated in the same way. The approximate value of **VB3** can also be generated in the similar way as **VB2**. An accurate **VB3** generator is shown Fig. 4.18.

In Fig. 4.18, **VB3** is taken from the drain of **M9**. If the potential at the drain of **M6** is the reference, **M9** combined with **M7** forms the equivalent of **M2** of Fig. 4.16. Therefore, the sum of the channel lengths of **M7** and **M9** has to be four times larger than **M8**, or if **M9** matches **M10**, **M7** has to be three times larger. It is important to note that this circuit combines both negative and positive feedback, a situation that can lead to two different stable points: a correct one and an incorrect one with zero current through both **M8** and **M7**. To avoid the latter, some form of start-up circuit is required, which in this case can be implemented by transistor **M15** which draws a small start-up current. **M15** has a longer channel length than **M8**. Again, channel lengths of **M7** and **M9** can be

slightly increased to compensate for body bias errors.

Fig. 4•18• VB3 generator

4•3•5• OPAMP circuit design

Due to the high output impedance of the OTA, the output of the OTA-C filter can't be used to drive other circuits. OPAMPs are needed to buffer the input and output of the OTA-C filter.

In this project, a load resistor driving class-AB OPAMP structure [62] is chosen. The circuit is shown in Fig. 4.19.

The OPAMP circuit used consists of three stages. The first stage is a differential input stage. It is biased by current source I_0 , loaded with an NMOS current mirror and has differential outputs. The first stage is also a gain stage. The second stage is a gain stage and changes the differential inputs to single ended output. The third stage is a class AB output stage of unit gain and uses common-source configuration. The output stage also gives the name to the amplifier circuit called class-AB OPAMP.

In the class-AB output stage, both complementary transistors have to be biased with a voltage which establishes the desired operating current. If this current is too low, the bandwidth will be degraded; if it is too high, the power dissipation can become unacceptable.

When optimizing the sizes of all the transistors in the OPAMP, the currents through $M3$, $M4$, $M5$ and $M6$ are chosen to be the same, they are all $I_0/2$. That is, the sizes of $M1$ and $M2$ are to be identical; sizes of $M3$, $M4$, $M5$ and $M6$ are also to be the same; sizes of $M7$ and $M8$ are also equal. The ratios of $M10$ to $M8$ and $M9$ to $M6$ are also set to be equal. If the ratio is denoted as n , the total static current in this OPAMP can thus be calculated to be $(I_0/2)*(4+n)$. For known V_{dd} , the total power dissipation can be determined.

Fig. 4-19• The structure of class-AB OPAMP

Capacitors $C1$ and $C2$ are used to achieve the frequency compensation of the OPAMP. Their values could be 5 times greater than the gate capacitance of the transistors in the OPAMP. If the chosen value is too large, the bandwidth of this OPAMP is limited; if the chosen value is too small, compensation might not be effective.

4.4• Loop filter structure design

In this project, a loop filter with the following transfer function is to be designed.

$$H(s) = K_h \frac{s + \omega_2}{s(s/\omega_3 + 1)} \quad (4.18)$$

The above transfer function can be rewritten as equation (4.19).

$$H(s) = \left(1 + \frac{\omega_2}{s}\right) K_h \left(\frac{1}{\frac{s}{\omega_3} + 1}\right) \quad (4.19)$$

From the above transfer function, it can be seen, this loop filter can be realized by the signal flow graph shown in Fig. 4.20.

Fig. 4.20• The loop filter signal flow graph

The summer & attenuator can be formed by the OPAMP summer and inverter in series, as shown in Fig. 4.21.

The integrator can be formed with an OTA and a capacitor, as shown in Fig. 4.24. In order to achieve a zero at a very low frequency, the principle of general impedance converter (GIC) or Miller effect is employed to achieve large equivalent capacitance, as shown in Fig. 4.22 and Fig. 4.23 respectively. This removes the requirement to put a very large capacitor on a chip.

Fig. 4•21• OPAMP summer&attenuator

Fig. 4•22• Equivalent capacitor using GIC

Fig. 4•23• Equivalent capacitor using the Miller effect

A small on-chip capacitance times a scale factor K_1 or K_2 could provide a very large equivalent capacitance. K_1 and K_2 are the ratios of resistors and thus can be very precise.

The lossy integrator can be formed with the structure shown in Fig. 4.25.

Fig. 4.24• OTA-C integrator

Fig. 4.25• OTA-C lossy integrator

The specification used in this loop filter design is:

$$K_h = 1/650.13$$

$$\omega_2 = 400 \text{ Hz} = 2513.3 \text{ rad/s}$$

$$\omega_3 = 1.2\text{E}6 \text{ Hz} = 7.54\text{e}+6 \text{ rad/s}$$

With g_m chosen to be $1/(25\text{K}\Omega)$, the bias current in the OTA to be $10\mu\text{A}$, the sizes of the transistors in the OTA can be determined by choosing the variable W equal to $1.4\mu\text{m}$. The integrating capacitance is calculated to be 16 pF . The capacitance in the lossy integrator is calculated to be 5.3 pF .

The complete structure of the loop filter on chip is shown in Fig. 4.26.

Fig. 4.26• Overall filter system structure

4.5• Tuning circuit structure design

Two different tuning schemes were considered.

The diagram of the first tuning circuit structure is shown in Fig. 4.27.

Fig. 4.27• The first self-tuning scheme

This tuning structure is just a negative feedback loop. The OTA and the switched-capacitor (SC) form an OTA-SC amplifier. If R_{eq} is used to represent the equivalent resistance of the switched-capacitor, then the amplification factor is the product of g_m and R_{eq} . If $1/g_m$ is equal to

Req , the output of the OTA-SC amplifier is equal to $v25$. If $1/g_m$ is less than Req , then the output of the OTA-SC amplifier will be greater than $v25$. The feedback loop inverts and amplifies the voltage difference and controls the bias circuit to reduce the g_m of OTA in the OTA-SC amplifier. If $1/g_m$ is larger than Req , then the output of the OTA-SC amplifier will be less than $v25$. The feedback loop inverts and amplifies the voltage difference and control the bias circuit to increase the g_m of OTA in the OTA-SC amplifier. Here $v23$ and $v25$ are two reference voltages used to set the output current of the OTA, and keep the output current smaller than the bias current of the OTA. The g_m in the tuning circuit can be seen as a sensor to the manufacture and thermal variations. The OTA-SC amplifier can be considered as a converter from g_m change to voltage change. The role of the negative feedback loop is to adjust g_m to keep it constant.

The diagram of the second tuning circuit structure is shown in Fig. 4.28.

Fig. 4.28• The second self-tuning scheme

This tuning structure is also a negative feedback loop and works in the same principle as the first structure. An equivalent transconductance resistor (as shown in Fig.4.8(f)) and an equivalent switched-capacitor resistor and an OPAMP form an amplifier. The gain of the amplifier is the

ratio of the equivalent resistance of the g_m resistor to the equivalent resistance of the switched-capacitor resistor. The negative feedback loop also tries to keep the gain to be unity so that g_m/C is constant.

In the physical IC layout, the OTA of the OTA-SC amplifier and the capacitor of switched-capacitor should be placed close to the core filter so that they undergo the same process and environment variation. This will guarantee that when the tuning loop adjusts the OTA in the OTA-SC amplifier, the OTAs in the core filter are also properly adjusted to maintain a stable frequency response.

4.6• Post layout HSPICE simulation results

All simulation results listed from Fig. 4.29 to Fig. 4.32 are post layout simulation results using netlists extracted from the corresponding layout.

Fig. 4.29• Simulated post layout frequency response of filter lpf1

Fig. 4-30 Simulated post layout frequency response of filter lpf2

Fig. 4-31• Simulated post layout transient response of automatic tuning circuit No. 1

Fig. 4-32• Simulated post layout transient response of automatic tuning circuit No. 2

The frequency response shown in Fig. 4.29 is for the OTA-C loop filter in which the equivalent capacitance is realized with the GIC structure. The simulation results show that this structure offers desired zero-pole frequencies, DC gain, and AC attenuation. Since the OPAMPs in the GIC

structure operate in open-loop, this loop filter structure requires a very precise DC bias to prevent these OPAMPs from saturating.

The frequency response shown in Fig. 4.30 is for the OTA-C loop filter in which the equivalent capacitance is realized with the Miller effect. The simulation results show that this structure offers more precise zero-pole locations, proper AC attenuation, and a little lower DC gain compared with the result shown in Fig. 4.29. Since no OPAMP in this filter structure is in open-loop application, this loop filter structure doesn't require a precise DC bias.

The two simulation results of the loop filter frequency response also show that the two designed loop filters can withstand the power supply variation to some extent. In the HSPICE simulations, the power supply is swept from 4.5 V to 5.5 V.

The transient response shown in Fig. 4.31 is for the automatic tuning structure shown in Fig. 4.27. The simulation results show that the bias control output is stabilized after a setting time.

The transient response shown in Fig. 4.32 is for the automatic tuning structure shown in Fig. 4.28. The same conclusion can be drawn as above.

For the two automatic tuning structures, the simulation results just show that the two tuning circuits are properly designed negative feedback loops, and the bias voltages can be stabilized in time. It is very difficult to generate a random process or operating environment disturbance using HSPICE simulation.

CHAPTER 5

High speed Hogge phase detector design

5.1• Principle of operation

Fig. 5.1• Hogge phase detector for square wave NRZ data

The Hogge phase detector is used to compare the phase of NRZ data to that of clock directly without converting NRZ data to RZ data. This makes it possible to recover the clock directly from real data stream. The basic Hogge phase detector structure is shown in Fig. 5.1. The function of the Hogge phase detector is to center the positive edge of the recovered clock to the data eye. This can be demonstrated by the three waveforms shown in Fig. 5.2, Fig. 5.3, and Fig. 5.4. Waveforms shown in Fig. 5.2 show the case when the positive edge of the recovered clock is centred at the data eye, and the DC components of v_a and v_b are equal. Waveforms shown in Fig. 5.3 show the case when the positive edge of the recovered clock is delayed w.r.t. the center of the data eye, and the DC component of v_a is greater than that of v_b . Waveforms shown in Fig. 5.4 show the case when the positive edge of the recovered clock is advanced from the center of the data eye, and the

DC component of v_a is less than that of v_b .

Fig. 5•2• Working waveforms of Hogge phase detector @ $\Delta\Phi = 0$

Fig. 5•3• Working waveforms of Hogge phase detector @ $\Delta\Phi > 0$

Fig. 5.4• Working waveforms of Hogge phase detector @ $\Delta\Phi < 0$

v_d is used to represent the voltage difference between v_a and v_b . Usually in a Hogge structure based clock recovery circuit, an active loop filter with infinite DC gain is employed. When the positive edge of the recovered clock is entered at the data eye, v_d is zero, and the output of the loop filter is zero. Any position deviation of the positive edge of the recovered clock from the center of the data eye will make v_d not equal to zero, and cause large DC change at the output of the loop filter. The negative feedback of the PLL will adjust the edge position until it is re-centered and v_d is equal to zero.

The Hogge phase detector has a phase difference ($\Delta\Phi$) detection range of $-\pi$ to $+\pi$, with $\Delta\Phi=0$ when the recovered clock is centered at the data eye. Its conversion gain is influenced by the randomness of the data stream, also called data transition density of the data stream. The Hogge phase detector's conversion transfer function is shown in Fig. 5.5. The maximum slope of the transfer function depends on the data transition density. For a 50% data transition density, the maximum is $(V_H - V_L)/4$, where V_H is the high logic level, and V_L is the low logic level of the Hogge phase

detector output.

Fig. 5.5• Conversion characteristic of Hogge phase detector

5.2• Hogge phase detector designed with TSPC circuits

In order to make it possible for the Hogge phase detector to work at the data rate of 622Mb/s, a TSPC version of the Hogge phase detector structure is proposed, as shown in Fig. 5.6. The basic building blocks for this structure is: the TSPC *n-latch*, the TSPC *p-latch*, the static buffer and the transistor logic XOR gate.

By different arrangements of the *n-latch* and *p-latch*, positive edge triggered and negative edge triggered TSPC D-flip-flops can be built. The inverted clock signal used in the Hogge phase detector can be removed, and the phase detector becomes a TSPC phase detector. The structure is shown in Fig. 5.6.

For the high speed circuit design, random delay is an impairment, and can negatively influence the performance of the circuit. In the Hogge phase detector, random delay can create a large dead zone and reduce linearity. Techniques of parallelism and segmentation make it possible to obtain systems with high data flow rates as long as the latency does not constitute an important restriction. A pipelined TSPC Hogge phase detector is thus investigated. By making the signals travel with the same delay in all signal channels, the delay effect on the circuit designed can be minimized,

and the operating frequency of the circuit designed can be improved. The structure shown in Fig. 5.6 also can achieve this goal.

Fig. 5•6• The pipelined TSPC structure for the Hogge phase detector

The buffer has two stages of inverters in series, two XOR gate circuits [84] are tried (as shown in Fig. 5.7), and two sets of *n-latch* & *p-latch* are also tried. The circuits of the first set of *n-latch* & *p-latch* is shown in Fig. 3.7. The circuits of the second set of *n-latch* & *p-latch* is shown in Fig. 3.10. The corresponding simulation results will be shown in the following section.

Fig. 5.7• XOR gate circuits employed for the Hogge phase detector design

5.3• Post layout HSPICE simulation results

Details of the Hogge phase detector design are given in Appendix C. The building block combinations for different Hogge phase detectors and their post layout HSPICE simulation results are summarized in Table 5.1.

<div style="display: flex; align-items: center; justify-content: center;"> <div style="writing-mode: vertical-rl; transform: rotate(180deg);">XOR circuits</div> <div style="text-align: center;">Latch circuits</div> </div>	LATCHES		LATCHES	
	n latch1 shown in Fig. 3.7(a)	platch1 shown in Fig. 3.7(b)	n latch2 shown in Fig. 3.10(a)	platch2 shown in Fig. 3.10(b)
XOR1 shown in Fig. 5.7(a)	shown in Fig. 5.8		shown in Fig. 5.10	
XOR2 shown in Fig. 5.7(b)	shown in Fig. 5.9		shown in Fig. 5.11	

Table 5.1. Summary of the Hogge phase detector simulation results

Fig. 5•8• hpd1 post layout simulation result

Fig. 5•9• hpd2 post layout simulation result

Fig. 5•10• hpd3 post layout simulation result

Fig. 5•11• hpd4 post layout simulation result

The simulations were conducted with the data input of 100% data transition density, that is, the data input is a 1, 0, 1, 0, ... regular data series. The average power consumption of hpd1 and hpd2 is about 19 mW at the input data bit rate of 622 Mbit/s. The average power consumption of hpd3 and hpd4 is about 14 mW at the input data bit rate of 622 Mbit/s. The linear phase detection range is about 60% of the total phase detection range. The simulation results show that the Hogge phase detector hpd3 gives the best performance among the four Hogge phase detectors simulated.

CHAPTER 6

High speed frequency prescaler design

6.1• Principle of frequency prescaler

A frequency prescaler is a dual modulus frequency divider realized by using the digital counter principle [6, 37-40]. The problem in frequency prescaler design is in selecting circuit techniques and designing the proper circuit structure to make it work in the gigahertz range with moderate power consumption.

There are two types of counters in use: synchronous and asynchronous.

The Johnson counter, also called the twisted ring counter or shift counter, is a synchronous counter. Synchronous counters have a high operating speed, so can be chosen to be a first stage in a high frequency prescaler. Fig 6.1 shows the general form of the Johnson counter.

Fig. 6.1• Johnson counter

The ripple counter is an asynchronous counter. It can be formed by several toggle flip-flops in series, one flip-flop's output drives its follower's input as shown in Fig. 6.2, and it is very

easy to design. Because of the ripple counter's asynchronous nature, its operating speed is much lower than a synchronous counter. For this reason, the ripple counter can be employed as the second stage in a frequency prescaler.

Fig. 6•2• Ripple counter

Synchronous counters can be designed to be any module (maximum module is 2^n for a counter with n storage components) by using properly designed combinational logic as a controller. So the general form of a synchronous counter can be shown as in Fig. 6.3. Usually, state machine diagrams, truth tables, and Karnaugh maps are the tools to design synchronous counters.

Fig. 6•3• A sequential system

Asynchronous counters can only be the counters using 2^n module, where n is the number of stages of toggle flip-flops.

The state machine diagram, truth table, Karnaugh maps, and a schematic of a 3/4 dual

modulus synchronous counter are shown in the following. This gives an example to show the design process of synchronous counters.

(a) State machine of the 3/4 dual modulus synchronous counter

MC	Q1	Q0	D1	D0
0	0	0	0	1
0	0	1	1	1
0	1	1	0	0
0	1	0	x	x
1	0	0	0	1
1	0	1	1	1
1	1	1	1	0
1	1	0	0	0

(b) Truth table of the 3/4 dual modulus synchronous counter

MC \ Q1Q0	00	01	11	10
0	0	1	0	x
1	0	1	1	0

$$D1 = (\overline{Q1} + MC) Q0$$

MC \ Q1Q0	00	01	11	10
0	1	1	0	x
1	1	1	0	0

$$D0 = \overline{Q1}$$

(c) Karnaugh maps of the 3/4 dual modulus synchronous counter

(d) Schematic of the 3/4 dual modulus synchronous counter

Fig. 6•4• Design process of the 3/4 dual modulus synchronous counter

By using the above 3/4 dual modulus synchronous counter as the first stage and combining it with a ripple counter as the second stage, a 15/16 dual modulus frequency prescaler can be designed (as shown in Fig. 6.5).

Fig. 6•5• 15/16 dual modulus frequency prescaler

The highest operating frequency of the 15/16 dual modulus frequency prescaler is determined by the highest operating frequency of the first stage counter — the 3/4 dual modulus syn-

chronous counter. The highest operating frequency of the first stage counter is determined by the rise and fall times of the storage components and the logic propagation delay times through the combinational logic circuits. Detailed analysis can be found in [37,40].

6.2• Review of prescalers designed with CMOS process

In the past, the high speed circuits usually were designed with bipolar circuits or with GaAs technology. The development of the submicron CMOS processes makes it possible to design the high speed frequency prescaler fully with CMOS technology. In recent years, several fully CMOS high speed frequency prescalers were constructed and reported [6, 37-40].

In reference [37], a 15/16 dual modulus frequency prescaler was designed with a 1.2 μm CMOS process. The storage component used in the first stage is a latch, as shown in Fig. 6.6. The storage component used in the second stage is a TSPC D-flip-flop, as shown in Fig. 3.11. Its highest operating frequency is 1.4GHz, and the average power consumption is about 14 mW at the highest operating frequency under 5V power supply.

Fig. 6.6• D latch circuit used in reference [37]

The problem with the structure shown in Fig. 6.6 is that the low voltage level of the input

clock should be at least one threshold voltage higher than the ground to keep two NMOS transistors in the D latch open. To make the circuit work faster will require an even higher low voltage level of the input clock. Thus, this circuit can't accept a rail-to-rail input clock. Since the storage components are latches, there also exists a very high low operating frequency limit to prevent logic chaos.

In reference [6], a 15/16 dual modulus frequency prescaler was designed using a 0.8 μm BiCMOS process. The storage component used in the first stage is a TSPC D-flip-flop, as shown in Fig. 6.7. The storage component used in the second stage is a static D-flip-flop, as shown in Fig. 6.8. Its highest operating frequency is 1.2 GHz, and the average power consumption is about 17 mW at the highest operating frequency under a 5V power supply.

Fig. 6-7• TSPC D-flip-flop used in reference [6]

The frequency prescaler reported in reference [6] has a wide operating frequency range, 280 MHz to 1.2 GHz for the division ratio of 16 and 280 MHz to 1.15 GHz for the division ratio of 15. This is achieved at the price of more transistors, larger die area, lower top operating frequency,

and lower power consumption when compared with the frequency prescaler reported in [37]. It also avoids the strict requirement for the clock input used in [37].

Fig. 6•8• Static D-flip-flop used in reference [6]

In reference [38,39], a 8/9 dual modulus frequency prescaler and a 128/129 dual modulus frequency prescaler were designed in a 1.2 μm CMOS process. The storage component used in the whole structure is a TSPC D-flip-flop, as shown in Fig. 6.9. The highest operating frequency of the first stage circuit reported in [38] is 1.16 GHz, and the average power consumption is about 45 mW at the highest operating frequency under 5V power supply. The frequency prescaler reported in [39] still uses the same storage component, except that the storage component was equipped with spike removal circuit, as shown in Fig. 6.10. So the highest operating frequency of the first stage circuit reported in [39] is 1.4 GHz, and the average power consumption is about 35 mW at the highest operating frequency under a 5V power supply.

The frequency prescalers reported in [38,39] have the same problems existing in [6] except

that the prescaler reported in [39] has a little higher top operating frequency.

Fig. 6.9• TSPC D-flip-flop used in reference [38]

Fig. 6.10• Improved TSPC D-flip-flop used in reference [39]

The division ratio control circuit structure in [6, 37] is shown in Fig. 6.11. This is a very power consuming structure. It also introduces more capacitance to the main counter loop and re-

-99-

6.3• New circuits proposed

In this thesis, the goal for the frequency prescaler design is to work out a 15/16 dual modulus frequency prescaler with an applicable high frequency range, small transistor count, and low power consumption.

Fig. 6.13• Latches used for the first stage circuit design

In order to achieve the design goal, TSPC latches are employed to replace the DFFs used in the first stage circuit of the 15/16 dual modulus frequency prescaler. The combinational logic for

the dual modulus control is also combined with one of the TSPC D-latches. The two TSPC D-latch circuits are shown in Fig. 6.13. By doing so, the rising and falling times of the storage components are reduced, the control logic propagation delay is eliminated, the operating frequency is increased, and the transistor number and power consumption are reduced. For this second stage circuit design, since it works at a much lower frequency range, the circuit speed and power consumption are not the main concern, and the choices can be very wide. The circuit chosen for the second stage circuit design is shown in Fig. 3.11.

Fig. 6•14• An improved structure for the first stage circuit design

The disadvantage of the above suggested design is that using latches as the storage components can cause logic races and hazards, and can cause the frequency prescaler to have a high frequency boundary and a low frequency boundary at the same time. Consequently, the operating frequency range of the designed frequency prescaler is narrow. Even so, the advantage of this design offers some insight for further improvement of the 15/16 dual modulus frequency prescaler.

In order to combat the logic race and hazard problems, another frequency prescaler design is offered in this thesis. The block diagram of this design is shown in Fig. 6.14. Latches are still

employed to be the storage components for the first stage circuit. The difference is that a p-type latch is inserted into the first stage circuit to combat the logic race and hazard. The higher power consumption modulus control circuit shown in Fig. 6.11 is employed to replace the lower power consumption modulus control scheme used in the first design to make an easy fit into the circuit.

The p-type and n-type latch circuits used in the first stage circuit are shown in Fig. 3.10. There is no change for the second stage circuit design. This design offers applicable high operating frequency and operating frequency range. The power consumption and transistor count are moderate.

6.4• Post layout HSPICE simulation results

Fig. 6.15• Post layout simulation results of the first designed frequency prescaler

For the first designed frequency prescaler, its top operating frequency can go to 1.4 GHz,

with the power consumption of about 7 mW; and its bottom operating frequency is about 900 MHz, with the power consumption of about 4 mW. The problem is that if a fast process is employed for the manufacture of this circuit, the bottom operating frequency will be moved up and top operating frequency will be moved down. The whole operating frequency range will be greatly narrowed. This is caused by the logic race and hazard when DFFs are replaced with D latches.

Fig. 6•16• Post layout simulation results of the second designed frequency prescaler

For the second designed frequency prescaler, its top operating frequency can go to about 1.11 GHz, with the power consumption of about 9 mW; and its bottom operating frequency is about 650 MHz, with the power consumption of about 6 mW. The simulation results also show that the worst case and fast case process don't change its operating frequency range significantly. This

means that the added p-latch between two n-latches really remove the logic race and hazard existing in the first designed frequency prescaler.

If the advantages of the two designed frequency prescalers can be combined, the author believes a lower power consumption and higher operating frequency range frequency prescaler can be achieved.

CHAPTER 7

SPW modelling of the PLL based applications

For PLL transient response simulation, SPICE is the most commonly used tool. This usually takes an extremely long simulation time and causes convergence problems. In this thesis, a new simulation tool, SPW, has been tried to examine the PLL performance in the Z domain.

An efficient tool to simulate the PLL is very important to the complete examination of the performance of a PLL design. SPICE, MATLAB and SPW have been tried to simulate PLL performance, and SPW is shown to be the most efficient tool among these three. In the following, the SPW models for PLL simulation and two simulation output waveforms are shown.

7.1• Models of the PLL building blocks

SPW is a tool used for discrete-time system simulation. In order to simulate the PLL with SPW, all PLL blocks need to be modelled in the Z domain. SPW offers libraries for many common building blocks such as signal generation and store, data conversion, mathematic operations, basic logic blocks, filters, and table-lookup, etc.

The SPW building block, multiplier, can represent a phase detector, as shown in Fig. 7.1.

Fig. 7.1• Multiplier as phase detector

An XOR gate plus two sine wave to pulse converters form another simple type of phase detector used to detect phase difference between two sine waves, as shown in Fig. 7.2.

Fig. 7.2• XOR as phase detector

The Hogge phase detector is often used in the clock recovery applications. This kind of phase detector can be built by using SPW blocks, as shown in Fig. 7.3.

Fig. 7.3• Hogge phase detector

Phase detectors or phase frequency detectors all have some sort of nonlinearity and dead zones. Their SPW models shown above are ideal ones. To get the non-ideal factors included in the simulation, the table-lookup function block can be used to convert the ideal characteristic of phase detectors or phase frequency detectors to the non-ideal characteristic. The table-lookup data can be determined by SPICE simulation or real chip testing. By doing so, a real case phase detector or phase frequency detector is shown in Fig. 7.4.

Fig. 7•4• Non-ideal phase detector or phase frequency detector

The transfer function of the most used loop filter in PLL design is,

$$H(s) = K_h \frac{s + \omega_2}{s(s/\omega_3 + 1)} \quad (7•1)$$

its Z domain SPW model is shown in Fig. 7.5.

Fig. 7•5• Loop filter model in Z domain

The parameters α_{R2} and α_{R3} in the above model are determined by the loop filter zero ω_2 , loop filter pole ω_3 , and the sampling frequency f_s of the discrete-time system simulated. Their relation is shown in the following two formulas.

$$\alpha_{R2} = \frac{\omega_2}{f_s} \quad (7•2)$$

$$\alpha_{R3} = \frac{\omega_3}{f_s} \quad (7.3)$$

A model of an ideal VCO used in SPW simulation is shown in Fig. 7.6.

Fig. 7.6• Ideal SPW model for VCO

In all electronics systems there exists noise. There are mainly two types of noise: $1/f$ noise, and thermal noise. These noises will cause phase jitter in VCO. The noise model is shown in Fig. 7.7.

Fig. 7.7• Noise model

The ideal VCO model shown in Fig. 7.6 can be modified to include the noise model shown in Fig. 7.7. The new model is shown in Fig. 7.8.

Fig. 7•8• VCO model with noise

For a real VCO, its conversion gain is not a constant. An SPW table-lookup function block can be used to accommodate real non-linear conversion gain. As shown in Fig. 7.9. The real data can be determined by simulation or real chip testing.

Fig. 7•9• VCO with simulated or testing conversion gain

The reference input model is shown in Fig. 7.10, with *offset* and *phase* inputs to inject noise and phase step to a PLL system. All reference inputs have noise included. For clock recovery applications, the random data input stream causes random phase step. With these two inputs, the reference input noise strength and the phase step amplitude that a PLL can withstand can be exam-

ined.

Fig. 7•10• Reference input model

The above models of PLL blocks can be connected to form a PLL. The parameters employed by each block model in the PLL SPW simulation are shown in the following table. These parameters come from the industrial standard (SONET) for the 622 Mb/s PLL based clock recovery application.

Parameters	Values
K_{VCO}	$6.28 \times 10^8 \text{ rad/s/v}$
K_D	$2.5/6.283 \text{ v/rad}$
ω_2	400 Hz
ω_3	1.2 MHz
K_h	1/650.13

Table 7.1. Parameters employed in the PLL SPW simulation

The overall PLL interconnection is shown in Fig. 7.11. Each block can use different model

or parameters. The transient locking process can be monitored through simulation. Once the PLL is in lock, a phase step can be introduced to examine the PLL response. By performing an FFT on the VCO output, noise contribution to jitter of the VCO output can be studied. The influence of PLL parameters on the loop filter output ripple also can be monitored.

Fig. 7-11• PLL connection for the SPW simulation

7.2• SPW simulation results

The following curve shows the locking behavior of the PLL.

Fig. 7.12• The simulated PLL locking process

The following curve shows the ripple ($\sim 7\mu\text{V}$) when the simulated PLL is in lock.

Fig. 7.13• Loop filter output ripple when the simulated PLL is in lock

CHAPTER 8

Conclusions

8.1• Summary

This thesis presented an approach to design a fully integrated loop filter with a very low frequency zero using a 0.8μ CMOS process. A negative feedback loop was employed to be an automatic tuning scheme to maintain a stable frequency response for this fully integrated loop filter. This method eliminated the area consuming buffers and pads used when external components were employed to realize the loop filter's low frequency zero.

This thesis presented that by using a pipelined TSPC structure with the Hogge phase detector design, a 622 Mb/s Hogge phase detector can be designed with a standard 0.8μ CMOS process. The designed Hogge phase detector is linear over more than 60% of its total detection range and consumes about 14 mW power.

This thesis also investigated several frequency prescaler structures. Two new frequency prescaler circuits were proposed and designed using a 0.8μ CMOS process with gigahertz range operating frequency, small transistor count and die area, and low power consumption.

Finally, a new PLL simulation method was explored. The results show that by converting the PLL model from the S domain to the Z domain and simulating PLL using SPW, the simulation efficiency can be increased dramatically.

8.2• Suggestions for future research

The scope of this research included only the design of PLL components. The designs have been submitted for fabrication. The devices will be tested as the continuation of the research group's effort in that area. Future improvements can be made in several areas. The automatic tuning approach can be extended to the charge pump. For the Hogge phase detector design, a more tight signal delay compensation can further improve its linearity. For the frequency prescaler design, if a further improved circuit structure can be chosen, the speed and the power consumption can be improved at the same time. Given the encouraging results obtained in research by this author, the PLL simulation using SPW also can be fully employed in the performance examination for frequency synthesizer and clock recovery designs.

Appendix A

HSPICE parameters for 0.8 μ BiCMOS process

All the HSPICE parameters listed in the following table are extracted from the devices with 0.8 μ channel lengths under the minimum, typical, and maximum conditions.

Parameters	Minimum conditions		Typical conditions		Maximum conditions		Units
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	
LEVEL	3	3	3	3	3	3	-
LMIN	0.6E-6	0.6E-6	0.6E-6	0.6E-6	0.6E-6	0.6E-6	m
LMAX	0.9E-6	0.9E-6	0.9E-6	0.9E-6	0.9E-6	0.9E-6	m
WMIN	1.4E-6	1.4E-6	1.4E-6	1.4E-6	1.4E-6	1.4E-6	m
WMAX	500E-6	500E-6	500E-6	500E-6	500E-6	500E-6	m
ACM	2	2	2	2	2	2	-
VTO	0.6806	-0.710	0.8165	-0.8500	0.9452	-0.9994	V
UO	458.5	167.0	446.6	161.5	428.3	147.9	cm ² /Vs
TOX	16.5E-9	16.5E-9	17.5E-9	17.5E-9	18.5E-9	18.5E-9	m
NSUB	2.396E16	2.350E16	2.884E16	2.550E16	3.273E16	2.762E16	1/cm ³
NFS	837.0E9	660.0E9	776.3E9	630.3E9	570.2E9	610.3E9	1/cm ²
DELTA	2.053	1.823	1.819	1.284	1.620	0.8187	-
THETA	24.19E-3	114.6E-3	20.58E-3	121.1E-3	12.86E-3	84.47E-3	1/V
WD	149.0E-9	178.0E-9	148.2E-9	176.0E-9	137.0E-9	174.0E-9	m
LD	85.00E-9	7.639E-9	90.00E-9	8.356E-9	95.00E-9	18.60E-9	m
LDIF	915.0E-9	992.4E-9	910.0E-9	991.6E-9	905.0E-9	981.4E-9	m
XJ	224.8E-9	114.7E-9	194.9E-9	104.3E-9	146.2E-9	102.2E-9	m
VMAX	148.0E3	299.4E3	148.6E3	275.0E3	147.6E3	268.2E3	m/s
ETA	24.72E-3	57.87E-3	34.56E-3	60.00E-3	43.51E-3	68.68E-3	-
KAPPA	35.47E-3	7.714	49.20E-3	8.00	20.09E-3	9.051	-
RS	1.000E3	1.095E3	1.2E3	1.200E3	1.400E3	1.350E3	ohm
RSH	0.0	0.0	0.0	0.0	0.0	0.0	ohm/sq
HDIF	1.2E-6	1.2E-6	1.2E-6	1.2E-6	1.2E-6	1.2E-6	m

Parameters	Minimum conditions		Typical conditions		Maximum conditions		Units
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	
RD	1.000E3	1.095E3	1.200E3	1.200E3	1.400E3	1.350E3	ohm
TLEV	1	1	1	1	1	1	-
TCV	980.8E-6	943.5E-6	980.8E-6	973.4E-6	980.8E-6	1.060E-3	V/K
BEX	-1.650	-1.100	-1.650	-1.100	-1.650	-1.100	-
TRS	-1.000E-9	1.000E-9	-1.000E-9	1.000E-9	-1.000E-9	1.000E-9	1/K
TRD	-1.000E-9	1.000E-9	-1.000E-9	1.000E-9	-1.000E-9	1.000E-9	1/K
JS	1.0E-4	1.0E-4	5.0E-4	5.0E-4	1.0E-3	1.0E-3	A/m ²
JSW	1.0E-10	1.0E-10	5.5E-10	5.5E-10	1.0E-9	1.0E-9	A/m
CJ	266.0E-6	410.0E-6	322.0E-6	450.0E-6	378.0E-6	490.0E-6	F/m ²
MJ	0.46	0.61	0.46	0.61	0.46	0.61	-
CJSW	270.0E-12	155.0E-12	322.0E-12	170.0E-12	374.0E-12	185.0E-12	F/m
MJSW	0.20	0.26	0.20	0.26	0.20	0.26	-
CJGATE	235.0E-12	175.0E-12	279.0E-12	190.0E-12	323.0E-12	205.0E-12	F/m
PB	0.923	0.919	0.925	0.921	0.928	0.924	V
PHP	0.923	0.919	0.925	0.921	0.928	0.924	V
CGSO	316.0E-12	233.8E-12	288.4E-12	214.8E-12	279.9E-12	210.7E-12	F/m
CGBO	547.6E-12	547.6E-12	568.3E-12	568.3E-12	620.6E-12	620.6E-12	F/m
CGDO	316.0E-12	233.8E-12	288.4E-12	214.8E-12	279.9E-12	210.7E-12	F/m
TLEVC	1	1	1	1	1	1	-
PTA	2.90E-3	1.39E-3	2.90E-3	1.39E-3	2.90E-3	1.39E-3	V/K
PTP	8.24E-3	4.55E-3	8.24E-3	4.55E-3	8.24E-3	4.55E-3	V/K
CTA	1.36E-3	1.35E-3	1.36E-3	1.35E-3	1.36E-3	1.35E-3	1/K
CTP	12.2E-6	941E-6	12.2E-6	941E-6	12.2E-6	941E-6	1/K
NLEV	2	2	2	2	2	2	-
KF	0.75E-24	125.0E-27	1.5E-24	250.0E-27	3.0E-24	500.0E-27	-
AF	0.85	0.95	0.85	0.95	0.85	0.95	-

Appendix B

Circuits for OTA-C loop filter design

fil_with_tuning_1 Schematic

fil_with_tuning_2 Schematic

lpf1 Schematic

lpf2 Schematic

tuning1 Schematic

bias1 Schematic

opa1 Schematic

integrator1 Schematic

integrator2 Schematic

lossy_int1 Schematic

miller1 Schematic

GmR Schematic

summer1 Schematic

vol_follower1 Schematic

vol_n_amp Schematic

vol_p_amp Schematic

clk1 Schematic

When frequency of c1 and c2 is half of 19.44 MHz, and the capacitance is 4pF, the equivalent resistance is 25K.

Switch capacitor as a reference resistor.

sc1 Schematic

sc2 Schematic

Appendix C

Circuits for high speed Hogge phase detector design

hpd1 Schematic

hpdc2 Schematic

hpds Schematic

hp4 Schematic

n latch1 Schematic

n latch2 Schematic

platch1 Schematic

platch2 Schematic

inv Schematic

xor1 Schematic

xor2 Schematic

nlat1 Schematic

nlat2 Schematic

15/16 Prescaler Schematic, No. 2

div34 Schematic

n-latch Schematic

p-latch Schematic

tff Schematic

nor3 Schematic

inv Schematic

Appendix E

Chip configurations and layout diagrams

The implemented layouts for this thesis work are presented here. IBACUFX3 and IBACUFX4 chip layouts, pinout diagrams, and the layout diagrams for some important function blocks are given in this section.

- **IBACUFX3**

Four Hogge phase detectors and a frequency prescaler are the included cells on IBACUFX3.

- **IBACUFX4**

Two loop filter designs and two automatic tuning designs are the included cells on IBACUFX4.

The pinout of IBACUFX3 chip

Layout diagram for IBACUF3 chip

The pinout of IBACUFX4 chip

Layout diagram for IBACUFX4 chip

Layout diagram for OTA

Layout diagram for OPAMP

Layout diagram for nlatch

Layout diagram for platch

Layout diagram for tff

Layout diagram for xor1

Layout diagram for xor2

Layout diagram for hpd1

Layout diagram for the second frequency prescaler design

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