A Dual Channel
RF Front End Receiver
with RF Q-enhanced LC Filters

By

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Abstract

A dual channel RF front end receiver is presented in this thesis project. The receiver architecture makes the use of Q-enhanced LC filtering at RF band and subsampling technique to down convert the RF signal to low frequency. Each channel includes LNA, Q-enhanced LC filter and subsampling block, performs independent channel selection and downconversion. A wide band LNA is designed as the input stage to drive both channels. Analysis and comparison between Q-enhanced LC filter and Gm-C filter is presented in detail. The major issue of substrate coupling when multi channels are implemented on a single die area is discussed. Simulations using Cadence SCA (Substrate Coupling Analysis) tool show the effect of substrate coupling as well. The test chip is fabricated using standard 0.18um CMOS process. A bond wire package is used to test the system performance. Each channel performs channel selection from 1.57GHz to 1.80GHz respectively. Each filter can be tuned with different Q factor. Subsampling function is confirmed for both channels. The interchannel coupling issue is examined and measured.

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Table of Contents

Chapter 1: Introduction	1
1.1 Motivation.....	1
1.2 Thesis Outline	3
1.3 Thesis Contributions	4
Chapter 2: Receiver Architectures	5
2.1 Introduction.....	5
2.2 Heterodyne Receiver.....	6
2.3 Direct Conversion Receiver.....	11
2.4 Digital Receiver and Subsampling	16
2.5 Architecture of the Design Project.....	19
Chapter 3: LNA Design.....	22
3.1 Introduction.....	22
3.2 Noise Optimization	24
3.3 LNA Topologies.....	30
3.4 A Wide-band LNA Design	35
Chapter 4: Q-Enhanced Filter and Subsampling Mixer Design	46
4.1 Introduction.....	46
4.2 Filter Topologies	48
4.3 Filter Dynamic Range	55
4.4 Q-enhanced LC Filter Design	61

4.5	Subsampling Mixer Design	73
4.5.1	Mixer Alternatives	73
4.5.2	Subsampling Circuits Design.....	77
Chapter 5: System Integration and Measurement		84
5.1	System Integration	84
5.2	Substrate Coupling Analysis.....	92
5.2.1	Substrate Coupling Mechanism	92
5.2.2	Substrate Modeling	95
5.2.3	Substrate Coupling Reduction	97
5.2.4	SCA Simulation	98
5.3	Measurement.....	100
5.3.1	Test setup	100
5.3.2	Measurement results	102
Chapter 6: Conclusion and Future Work		106
References.....		109
Appendix A: Detail Design Schematics.....		113

List of Figures

Figure 2.1:	Basic heterodyne receiver.....	6
Figure 2.2:	Typical superheterodyne receiver	8
Figure 2.3:	Two stage superheterodyne receiver.....	9
Figure 2.4:	Hartley image-reject receiver.....	10
Figure 2.5:	Direct conversion receiver	11
Figure 2.6:	Self-mixing of LO or RF interferer.....	12
Figure 2.7:	Time-domain waveforms of I/Q mismatch.....	14
Figure 2.8:	Digital-IF receiver.....	16
Figure 2.9:	Low-IF receiver	17
Figure 2.10:	Subsampling in frequency domain	18
Figure 2.11:	System architecture for this project	19
Figure 3.1:	Cascaded system	22
Figure 3.2:	Input referred noise model	24
Figure 3.3:	MOSFET noise model	26
Figure 3.4:	LNA topologies (Biasing not shown)	30
Figure 3.5:	Small signal model for common-source LNA	32
Figure 3.6:	Small signal model for shunt-series LNA.....	33
Figure 3.7:	Wide band LNA	35
Figure 3.8:	1 dB compression point definition.....	38
Figure 3.9:	IIP3 definition	39
Figure 3.10:	NF, Gain, IIP3 trade off with R_f	40
Figure 3.11:	NF, Gain, IIP3 trade off with R_s	40
Figure 3.12:	Input and output stability circle	42

Figure 3.13:	Load stability circle on the Smith chart	43
Figure 3.14:	Simulation results of stability factor K and B1	44
Figure 3.15:	Layout of the wide band LNA	45
Figure 4.1:	On-chip bandpass filter alternatives	46
Figure 4.2:	Parallel RLC resonator.....	48
Figure 4.3:	Active inductor	49
Figure 4.4:	Equivalent Active Resistor	50
Figure 4.5:	Gm-C based bandpass filter	50
Figure 4.6:	Q-enhanced LC filter	51
Figure 4.7:	Master-slave tuning architecture	53
Figure 4.8:	Direct-tuning architecture	54
Figure 4.9:	Gm-C filter with noise sources	56
Figure 4.10:	Q-enhanced LC filter with noise sources.....	58
Figure 4.11:	Differential Q-enhanced filter.....	61
Figure 4.12:	Q-enhanced filter input transconductors layout.....	62
Figure 4.13:	Unit capacitors	63
Figure 4.14:	Switched capacitor bank	64
Figure 4.15:	Capacitors changing range.....	64
Figure 4.16:	Anisotropic conductive adhesive attachment	65
Figure 4.17:	Layout of the Q-enhanced block.....	68
Figure 4.18:	AC simulation with frequency tuning.....	69
Figure 4.19:	AC simulation with Q tuning.....	70
Figure 4.20:	Noise figure of the system (Wide-band LNA + filter).....	70
Figure 4.21:	IIP3 of the system (Wide-band LNA + Filter).....	71
Figure 4.22:	IIP3 vs. Filter Q	71

Figure 4.23:	Gilber type mixer	73
Figure 4.24:	Subsampling mixer	74
Figure 4.25:	Subsampling in time domain	74
Figure 4.26:	Sampling jitter.....	76
Figure 4.27:	S/H circuit	77
Figure 4.28:	Clock generator.....	79
Figure 4.29:	Input sine reference and output clock waveform.....	80
Figure 4.30:	Two stage buffer for S/H block.....	81
Figure 4.31:	Layout of subsampling circuits.....	81
Figure 4.32:	S/H circuits transient simulation result	83
Figure 4.33:	Subsampling block NF.....	83
Figure 4.34:	IIP3 result from PAC simulation.....	83
Figure 5.1:	Dual channel RF front end system diagram.....	85
Figure 5.2:	8-bit Digital-to-Analog converter circuit	86
Figure 5.3:	RF buffer and coupling circuit.....	87
Figure 5.4:	RF output buffer.....	87
Figure 5.5:	Dual channel receiver front end layout.....	89
Figure 5.6:	System noise figure.....	90
Figure 5.7:	System AC simulation	90
Figure 5.8:	Channel 1 RF output spectrum	91
Figure 5.9:	Channel 2 RF output spectrum	91
Figure 5.10:	Subsampling output spectrum.....	91
Figure 5.11:	Capacitive link to the substrate	94
Figure 5.12:	The substrate coupling process	95
Figure 5.13:	Using Green function through substrate ports	96

Figure 5.14:	Extracted view simulation without the substrate coupling model	99
Figure 5.15:	Extracted view simulation with the substrate coupling model	100
Figure 5.16:	Measurement system setup	101
Figure 5.17:	Test Board	101
Figure 5.18:	Filter frequency tuning.....	102
Figure 5.19:	Filter Q-tuning	103
Figure 5.20:	Down-converted signal spectrum with one channel enable.....	104
Figure 5.21:	Down-converted signal spectrum with both channels enable.....	105

List of Tables

Table 3.1:	Parameters of the wide band LNA.....	41
Table 3.2:	Performance of the wide band LNA	44
Table 3.3:	Comparison with published LNA designs	45
Table 4.1:	Transistor size of the Q-enhanced filter	72
Table 4.2:	System performance (LNA + Q-enhanced LC filter)	72
Table 4.3:	Subsampling circuit performance	82
Table 5.1:	System Performance	88
Table 5.2:	Comparison between substrate doping levels (p-type substrate).....	93

List of Abbreviations

ADC	Analog to Digital Converter
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital to Analog Converter
dB	decibel
dBm	milli-decibel (decibels with respect to 1 mW)
GPIO	General Purpose Interface Bus
IC	Integrated Circuit
IF	Intermediate Frequency
IP2	Second Order Inter-modulation Product
IP3	Third Order Inter-modulation Product
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NF	Noise Figure
Q	Quality Factor
RF	Radio Frequency
SAW	Surface Acoustic Wave
SNR	Signal to Noise Ratio
SOC	System On a Chip
VCS	Voltage Controlled Oscillator

1.1 Motivation

An increasing demand for wireless broadband internet access and short-range multimedia communication in homes and offices has led to a likewise increasing interest in low-cost, low power, fully integrated radio transceiver implementations. A single fully integrated transceiver not only reduces the device size which is desirable in most wireless applications, but also eliminates the expansive off-chip components, and as the result reduces the system cost. New wireless technology such as Ultra-wideband (UWB) systems provides the capability of transmitting data over a wide spectrum of frequency bands with very low power and high data rates. Although the UWB standard (IEEE 802.15.3a) has not been completely defined, it most likely needs the design of wide band LNA and multi band selection circuits.

GaAs and Bipolar technologies have been favoured for transceiver front end (RF part) implementations because of their high unity-gain frequencies f_t and high device transconductance g_m . However, these technologies are incompatible with the CMOS

technology which dominates the digital design implementation. If a single integrated solution such as system on a chip (SoC) is to be realized, CMOS technology proves to be more attractive. The lower power consumption of CMOS circuits is one of these advantages. Furthermore, a steady scaling down of CMOS device size and cost makes the use of CMOS in RF integrated circuits more and more attractive.

One of the main challenges facing complete integration of receiver hardware has been a difficulty to accomplish on-chip RF and IF filtering [1]. This is mainly because the passive on-chip elements, such as inductors and resistors have poor Quality factors (Q) and exhibit large process variations. Various approaches have been found to improve the Q factor [2], [3],[4]. A Q-enhanced filter is a simple circuit that helps to cancel losses in inductors, thereby enhancing the effective inductor Q. For this reason, it is a suitable solution for on-chip filtering for RF applications.

Another problem in modern SOC architectures is the interference between integrated circuit (IC) RF, analog and digital blocks. For example, coupling of digital switching transients to analog circuitry may take place via the substrate or by parasitic capacitive coupling. The RF circuitry can interfere with the operation of digital and other analog circuitry in a similar way. System performance is generally degraded, timing errors may be introduced and total functional failure may occur.

This thesis describes a fully integrated dual channel receiver front end, and the above coupling issue is examined in the context of the design. The circuit, implemented in 0.18 μm CMOS technology, is designed to work in the 5GHz range. It has two separate channels with LNAs, Q-enhanced LC filters and subsampling blocks. A flip-chip package is used to

reduce bonding wire inductance. Simulation and test results are compared to evaluate interchannel coupling. The main goals of this project include,

- Implement multi-channel receiver front end in a single die area.
- Examine channel selecting performance for each channel.
- Evaluate interchannel coupling issue.
- Examine subsampling function.

1.2 Thesis Outline

As a background, existing integrated receiver structures are reviewed in Chapter 2. The advantages and problems associated with each are discussed.

Basic LNA topologies are discussed in chapter 3. Design techniques directed at noise optimization, linearity improvement, and stability analysis are reviewed. The wide band LNA design used in this thesis is then presented.

Chapter 4 starts with a review of typical off-chip and on-chip filter types. Two types of filters, the Gm-C and Q-enhanced LC filters, which are suitable for on-chip implementation are discussed and compared in detail. The Q-enhanced LC filter design used in this thesis is covered in this chapter. The subsampling block design is presented at the end of this chapter.

System integration considerations are examined in chapter 5. Substrate coupling issues are then discussed in this chapter. A simulation using Cadence Substrate Coupling Analysis (SCA) tool is done to examine the extent of the signal coupling between the two channels.

Finally, the test system is described, and test results are discussed and compared with the simulation results. The thesis conclusion is presented and suggestions for future research are made in chapter 6.

1.3 Thesis Contributions

The main contributions of this thesis project are listed as follow:

- A dual channel receiver front end is implemented in a single die area using standard CMOS technology.
- Independent channel selection and subsampling down-conversion function are examined.
- Independent filter frequency tuning and Q tuning are confirmed.
- Interchannel coupling issue is demonstrated and measured using the test chip.

Receiver Architectures

2.1 Introduction

Basic radio receiver functionality includes[1]:

- Selectivity: isolation of desired signals against dense spectral backgrounds.
- Gain: amplifying selected signals to levels useful for further processing.
- Information recovery (demodulation, amplification).

The evolution of receiver architectures directed at realizing these fundamental requirements began at the time of the earliest radio experiments of H.R. Hertz in 1887 [5].

Measures of sensitivity, dynamic range, selectivity and fidelity allow one to quantify receiver performance. In addition to these factors, the choice of a suitable receiver architecture is further influenced by complexity, cost, power consumption and the need for off-chip components in the design. Technological limitations of past decades have led to the dominance architectures that are less than ideal with respect to these issues, but recent

improvements in IC technology have made it possible to integrate off-chip functions and thereby reduce the size and cost of commercial products. Previously impractical architectures may now be reconsidered.

In this chapter some basic receiver architectures, namely superheterodyne, direct-conversion, digital-IF and subsampling types, are reviewed, and the characteristics and advantages of each are discussed. Finally, the architecture selected for development in this thesis is examined.

2.2 Heterodyne Receiver

The heterodyne or superheterodyne structure, introduced by Armstrong and others in 1918 [6], was the most widely-used architecture during the last century. The basic configuration is shown in Figure 2.1.

Figure 2.1: Basic heterodyne receiver

The term heterodyne is derived from the Latin components hetero (different) and dyne (to mix). The basic idea is one of converting the incoming signal to a lower frequency before demodulation. For example, assume the input signal is a simple sinusoid, $A_1 \cos \omega_1 t$. When this is mixed (analogue multiplied) with a second sinusoid $A_o \cos \omega_o t$,

which is generated locally, there results a product signal which may be written $\frac{A_o A_1}{2} \cos(\omega_o - \omega_1) t + \frac{A_o A_1}{2} \cos(\omega_o + \omega_1) t$. The higher frequency part is removed by low pass filtering, with the overall result that the input signal frequency is downshifted (the first term in the mixer product). It is this difference-frequency term that is used for further processing.

The advantage of downshifting the input frequency is a simple result of the relation between the Quality factor (Q) and the bandwidth of the filters that appear in subsequent circuitry. This relation is $Q = \frac{\omega_o}{\Delta\omega}$ - it is clear that the narrow bandwidth required for selectivity means that higher operating frequencies necessitate higher filter Qs. Channel selection at the original RF in a narrow band communication receiver would require an extremely high filter Q value, and these are difficult to obtain even when external (off-chip) components are used. The mixing down of the signal to a lower frequency relaxes the Q requirement according to the equation, and ultimately leads to reduced system cost and complexity.

The main problem associated with the heterodyne architecture is that of images. In addition to the desired signal ω_1 at the mixer input, there may be an image frequency of ω_1 , which is $\omega_{im} = 2\omega_o - \omega_1$. After mixing and filtering, this image term will have been downshifted to the same frequency as the desired signal. If the image interference is too strong, the desired signal will not be detected correctly. For this reason, an image reject filter is usually inserted into the mixer input line. A typical superheterodyne receiver is shown in Figure 2.2:

Figure 2.2: Typical superheterodyne receiver

The preselect filter plays a band selection role by attenuating the out-band signal and providing partial image rejection. The LNA (low noise amplifier) increases the input signal amplitude while not materially degrading receiver noise performance (the noise figure (NF) of an entire system is typically dominated by that of its first stage). The image filter provides additional image frequency rejection. The mixer combines the local oscillator output with the amplified and filtered RF signal to produce an intermediate frequency (IF), as described previously. The IF signal level is brought to a level suitable for further processing by a gain adjustable amplifier. The desired channel is selected from the relatively low frequency IF band by the IF filter. The selected signal is then sent on to the demodulation or detection block.

Another issue that the heterodyne receiver designer is faced with is the selection of a suitable intermediate frequency. The choice of the IF depends on trade-offs involving three parameters: the amount of image noise, the spacing between the desired band and the image, and image-reject filter losses [7]. Usually a lower IF is desired because channel selection using a low-Q filter is then possible. But on the other hand, when the IF is lowered the desired band gets closer to the image band making a higher-Q image-reject filter necessary.

One popular means of dealing with the performance trade-off between image rejection and channel selection is the multiple conversion superheterodyne receiver. Figure 2.3 shows a two stage superheterodyne receiver:

Figure 2.3: Two stage superheterodyne receiver

The first intermediate frequency (IF1) is made relatively high so as to reduce the design complexity of the image-reject filter. The IF filter operating at frequency IF1 provides pre-channel selection. The second intermediate frequency (IF2) is then made somewhat lower so that the narrow band channel selection filter will be easier to implement. The main drawback of this idea is that more components for additional filters are needed, and two oscillators are needed to generate two local frequencies. A single chip implementation for this architecture is also more difficult.

Various modified heterodyne architectures have been developed in efforts to reduce image-reject filter complexity. One widely-used such strategy involves the use of image rejection mixers for the cancellation of image interference. In the Hartley image reject architecture [8], the input signal is split into two paths (I and Q), mix each of them with

out-of-phase (90°) local oscillator signals, low-pass filter them, subject one to a further 90° shift, and finally add them to produce an IF signal from which the image interference has been removed. See Figure 2.4:

Figure 2.4: Hartley image-reject receiver

In particular, suppose that the desired input signal is a sum of a desired term and an image interference term $A_{RF}\cos\omega_{RF}t + A_{im}\cos\omega_{im}t$. Before mixing, the signals are separated into two paths I and Q. After mixing, the low pass filters remove the higher frequency components of signals and the resulting two paths become:

$$x_I(t) = -\frac{A_{RF}}{2}\sin(\omega_{RF}-\omega_{LO})t + \frac{A_{im}}{2}\sin(\omega_{LO}-\omega_{im})t \quad (2.1)$$

$$x_Q(t) = \frac{A_{RF}}{2}\cos(\omega_{RF}-\omega_{LO})t + \frac{A_{im}}{2}\cos(\omega_{LO}-\omega_{im})t \quad (2.2)$$

The I path signal is then shifted by a further 90° to

$$\overline{x_I(t)} = \frac{A_{RF}}{2}\cos(\omega_{RF}-\omega_{LO})t - \frac{A_{im}}{2}\cos(\omega_{LO}-\omega_{im})t \quad (2.3)$$

The signals in the separate paths are finally combined to

$$x_{out}(t) = A_{RF} \cos(\omega_{RF} - \omega_{LO}) t \quad (2.4)$$

in which no image interference term appeared.

Another example of an image rejection architecture is the Weaver architecture, which uses two-stage mixers to get the same effect [7].

Image rejection receivers suffer from sensitivity to gain and phase mismatch. If the I and Q signal paths are not matched with one other, the image interference will not be fully cancelled and the desired signal will be attenuated. The Weaver architecture exhibits yet another problem, namely secondary image interference at a second mixer stage. This is discussed in Razavi's book [7].

2.3 Direct Conversion Receiver

We now turn to the direct conversion receiver. Figure 2.5 shows the architecture of a direct conversion receiver.

Figure 2.5: Direct conversion receiver

Unlike the case of the heterodyne receiver, the direct conversion device's local oscillator frequency ω_{LO} is equal to the input radio frequency (RF). This means that there is no IF:

$$\omega_{IF} = \omega_{RF} - \omega_{LO} = 0.$$

For this reason, the direct conversion structure is sometimes called a 'zero-IF' or homodyne architecture. No IF signal means that there is no image frequency and no need for an image rejection filter. Furthermore, there is only one conversion stage in this architecture, a situation which facilitates a one-chip implementation.

The direct conversion architecture is in some ways simpler than the heterodyne architecture. However a number of problems, such as DC offset, LO leakage, I/Q mismatch, even-order distortion and 1/f noise, which are not greatly important in heterodyne architectures, can act to limit direct-conversion performance:

DC Offset

Perhaps the most serious problem is that of DC offset in the baseband section of the homodyne receiver [9]. DC-offset is caused by the self-mixing phenomenon illustrated schematically in Figure 2.6:

Figure 2.6: Self-mixing of LO or RF interferer

The LNA and mixer are not perfectly isolated: the local frequency signal can leak to the input port via substrate or bond wire coupling. This is commonly referred to as 'LO leakage'. In the same manner, the input signal can also leak to the mixer's LO port. When such

unintentional coupling occurs, the leakage signal is mixed with itself and a DC component appears at the mixer output. This DC level can corrupt the desired signal and/or saturate the following stages. It is true that this DC voltage can appear at the output of a heterodyne mixer for the same reasons, but the heterodyne IF is nonzero and any DC component is removed by the IF filter so that subsequent circuitry will not be affected.

A simple way of removing DC offset is to use ac-coupling in the signal path. However, in many modulation schemes, DC components contain signal information and cannot be removed without losing said information and increasing the bit error rate.

Other popular methods use baseband analog or digital signal processing (DSP) techniques to estimate and remove the DC-offset [7],[10]. At the system level, a 'DC free' modulation method (FSK for example) can be chosen to minimize the signal energy near DC, and ac-coupling used to remove any offset. DC free modulation schemes other than FSK have been developed [11].

I/Q Mismatch

Many modulation methods (such as FM and QPSK) produce signals which contain different transmit information at either side of the carrier frequency, and a quadrature downconversion method, like that of Figure 2.5, is usually indicated. The 90° phase shift is normally carried out at the LO frequency because phase shifting an RF signal generally entails difficult noise-power-gain trade-offs [12].

The amplitude and phase error caused by the phase shifting block can corrupt the constellation of the down converted signal and increase the bit error rate. Suppose for instance,

that the input signal is $x_{in}(t) = a\cos\omega_c t + b\sin\omega_c t$, where a and b are either 1 or -1. The mismatching of both amplitude and phase of the LO signal used in the I and Q paths is described by

$$x_{LO,I}(t) = 2\cos\omega_c t \quad (2.5)$$

$$x_{LO,Q}(t) = 2(1+\epsilon)\sin(\omega_c t + \theta) \quad (2.6)$$

where ϵ and θ are amplitude and phase mismatch values.

After downconversion using the mismatched LO signals and then low pass filtering, the I and Q signals will have become

$$x_{BB,I}(t) = a \quad (2.7)$$

$$x_{BB,Q}(t) = (1+\epsilon)b\cos\theta - (1+\epsilon)a\sin\theta \quad (2.8)$$

Figure 2.7 shows a corrupted QPSK signal in time domain:

Figure 2.7: Time-domain waveforms of I/Q mismatch

We see that if $\theta = 0$ (no phase mismatch), the downconverted signal will contain only a gain error, the result of LO amplitude mismatch. Phase mismatch, on the other hand, not

only changes the amplitude, but also shifts a fraction of the information from one channel to the other. If a and b are uncorrelated, the effect of this transfer is similar to the introduction of noise - the SNR will be degraded.

I/Q mismatch was especially difficult to deal with in the times when discrete components were used. But as IC technology improved the problem was steadily overcome through the use of easily-matched on-chip structures and advanced layout procedures. Furthermore, signal processing techniques can also be used, since this type of mismatch varies only slowly with time.

Even-order Distortion & Flicker Noise

Even-order distortion and flicker noise also affect the performance of direct conversion equipment. Even-order distortion is caused by second order LNA nonlinearity like, for instance $y(t) = a_1 x(t) + a_2 x(t)^2$. If two strong interferers are spectrally near to one another and to the channel, a very low frequency interference will be generated because of the second order LNA nonlinearity. This interference can be coupled to the mixer because of the imperfect isolation described earlier, and introduce distortion into the downconverted signal.

The creation of flicker noise ($1/f$ noise) takes place by a number of different mechanisms, and is most prominent in devices that are sensitive to surface phenomena [13]. Since its spectral density is inversely proportional to the frequency, it will have its strongest effects on low frequency downconverted signals. It also tends to be more severe in CMOS devices rather than in Bipolar ones.

2.4 Digital Receiver and Subsampling

In modern digital communication systems, the received analog signal is converted to a digital one so that DSP (digital signal processing) methods may be applied to it. The advanced coding and equalization techniques in digital domain can be used to alleviate or solve problems like multipath distortion, as a result improve the error bit rate. Placing the ADC at the IF output tends to minimize or eliminate the requirement for on-chip analog filtering, reducing system complexity and cost. Figure 2.8 shows an architecture called Digital-IF receiver:

Figure 2.8: Digital-IF receiver

This is a modification of the traditional two-stage IF heterodyne architecture: the IF signal is transformed to the digital domain after the first stage of mixing and the second set of mixing and filtering is performed in the digital domain where it can be done more efficiently. Furthermore, since the second mixer operates in the digital domain, no gain or phase mismatch is possible and the I/Q mismatch problem described previously is avoided.

A remaining difficulty for this architecture is that it needs an ADC operating at IF and having much high (up to 14-bit) resolution[7]. Such high ADC performance tends to be incompatible with low or even reasonable power consumption.

ADC requirements are somewhat relaxed in the so-called low-IF architecture shown in Figure 2.9:

Figure 2.9: Low-IF receiver

In this architecture, the RF signal is mixed down to the IF band using a complex mixer (I/Q path) to eliminate the image problem [9]. The name low-IF is due to the way in which the circuit differs from the digital-IF receiver, namely in the choice of the LO frequency. In the low-IF receiver, an IF as low as one or two times of channel bandwidth is chosen because it is easier to sample a low-IF signal with high resolution ADCs. Since the performance of integrated ADCs is improving rapidly, this architecture will likely come to be a preferred one[14]. Another advantage in using the low-IF method is that the DC-offset problem is easier to deal with than in the homodyne architecture - the converted signal is not located around DC. The I/Q mismatch problem is completely avoided as in the case of a digital-IF architecture.

If the RF transmit signal has a narrow bandwidth, the subsampling technique can be used to sample it at a rate much lower than the Nyquist-rate.

Figure 2.10: Subsampling in frequency domain

Figure 2.10 illustrates the basic idea of subsampling in the frequency domain. When sampling rate is at least twice higher than the bandwidth of bandlimited signal, the bandlimited signal can be downconverted to baseband without aliasing. There are a number of advantages to using the subsampling technique, not the least of which is that fewer stages are needed before the input signal is transformed to the digital domain and the complexity of the entire system is greatly reduced. IC implementation is facilitated because the radio's functionality can be implemented on a single chip, including the RF front end and the following DSP blocks. The reduction of the downconversion rate leads to simplified designs for the local oscillator and its associated synthesizer loop.

However the subsampling method is not without its problems. First, reducing the sampling rate does not lessen the sample and hold circuit bandwidth requirements. The bandwidth for S/H circuit must still meet the highest signal frequency - when the RF signal is in the several giga-hertz region, S/H circuit design is difficult. Second, any noise or other

extraneous signals that reach the mixer input will be aliased or shifted into the baseband. A preselect filter is necessary in the circuit to prevent this. Furthermore, noise generated by the S/H circuit will also be aliased into the baseband with a resulting SNR degradation.

2.5 Architecture of the Design Project

The main goal of this project is to evaluate the performance of a receiver having two separate selective channels on a single chip. An outline of the proposed architecture is presented in Figure 2.11:

Figure 2.11: System architecture for this project

The two channel selection and downconversion paths are capable of independent operation, and each can be enabled or disabled by a control signal. Both channels are designed working at 5GHz range with the filter Q factor of 100~200. This structure is an effective tool for studies of channel selection and cross channel interference phenomena, the main areas of research in this project.

In Figure 2.11, a wide band low noise amplifier forms the first stage. It drives the two separate channels with an input signal that has been amplified while a low noise figure (NF) is maintained. Since two channels are designed to have different channel selection properties in the 5GHz band, the LNA must provide flat gain over a wide band centred on 5GHz. Another important requirement of this LNA is that it must present a fixed input load for an off-chip matching network. The load change which occurs when the signal paths are turned on or off do not affect the matching network. Good linearity will be another property of the LNA since the linearity for the following channel selection filters is critical as discussed in the following chapters.

Q-enhanced LC filters are used for channel selection. The central frequency and Q factor of each filter will be independently controllable so that independently tunable channel selection and filter bandwidth will be possible. A subsampling block is used in each channel to mix the RF signal down to a low frequency. RF buffers are placed between the filters and the subsampling blocks. These buffers increase the power of the signal sent to the sub-sampler and also help to isolate the RF signal from the sampling block. The resulting down-converted signal is sent to a two stage buffer which drives the output port to a level suitable for further DSP processing. The output buffer, having a design bandwidth of a few hundred MHz, also acts as a low pass filter for removing high-frequency components.

A buffered version of the RF signal coming from the channel-selection filters is provided so that the performance of these filters can be monitored.

Part of the system is a digital core with SPI interface which generates control signals. It can be used to set registers. Eight and sixteen-bit digital to analog converters (DAC) are used to convert control bits in the registers to control voltages which are then used to tune filter frequencies, Q factors and amplifier and buffer bias levels. The sampling clock is produced by a clock generation circuit - a reference sinusoid is converted to a sharp squared clock waveform.

In the following chapters, the design of the main function blocks, LNAs, Q-enhanced LC filters, and subsampling blocks are described in some detail.

3.1 Introduction

Low noise amplification is usually the first step performed in a wireless receiver, and the low noise amplifier (LNA) is the first component in the signal path. The principal task of the LNA is the provision of suitable gain while adding a minimum of additional noise. A system with several cascaded gain stages is shown in Figure 3.1:

Figure 3.1: Cascaded system

Since noise factor is defined as,

$$F = \frac{N_{\alpha(total)}}{N_{\alpha(source)}} = \frac{N_{\alpha(source)} + N_{\alpha(add)}}{AN_i} = 1 + \frac{N_{\alpha(add)}}{AN_i} \quad (3.1)$$

where A is the gain, N_i and N_o are the input and output noise power respectively.

The total output noise of the cascaded system is,

$$N_{\alpha(total)} = N_i A_1 A_2 \cdots A_n + N_{A1} A_2 \cdots A_n + \cdots + N_{A(n-1)} A_n + N_{An} \quad (3.2)$$

where N_{Ai} is the noise power added to the propagating signal by stage i .

The output noise due to noise in the source (input noise - N_i) is

$$N_{\alpha(source)} = N_i A_1 A_2 \cdots A_n \quad (3.3)$$

The noise factor can now be written in a more explicit form:

$$\begin{aligned} F &= \frac{N_{\alpha(total)}}{N_{\alpha(source)}} = 1 + \frac{N_{A1}}{N_i A_1} + \frac{N_{A2}}{N_i A_1 A_2} + \cdots + \frac{N_{An}}{N_i A_1 A_2 \cdots A_n} \\ &= F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} + \cdots + \frac{F_n - 1}{A_1 A_2 \cdots A_n} \end{aligned} \quad (3.4)$$

where $F_1, F_2, \dots, F_n$ are the noise factors for each block.

It is seen that the system noise is dominated by the contributions of the first few gain stages - for this reason, an LNA is used for the first stage of amplification and obviously its design should be one whose noise factor is as low as possible.

Another important issue in LNA design is input impedance matching. The usual requirement here is that of a stable match to a 50Ω resistive input impedance. But unfortunately the input impedance of the MOSFET at the LNA's input is inherently capacitive, a situation which leads to difficult-to-reconcile constraints on the topology of a LNA which must satisfy both matching and noise requirements.

The LNA must also satisfy linearity conditions (The linearity is usually measured by IP3), exhibit stable performance in the frequency range of interest and have low power consumption. These requirements are not independent of one another and judicious design trade-offs are usually called for if optimum performance is to be obtained.

In this chapter, the optimization of noise factor using the classical analysis approach is first introduced, and then the process is extended by incorporating power consumption restrictions. Several LNA topologies are then examined in the light of these results. Finally, the wide band LNA design used in this project is presented.

3.2 Noise Optimization

In classical noise analysis theory, noisy amplifiers are regarded as noiseless units to which two external noise sources have been connected as shown in Figure 3.2:

Figure 3.2: Input referred noise model

The noise factor is defined as

$$F \equiv \frac{\text{total output noise power}}{\text{output noise power due to input source noise}} \quad (3.5)$$

The individual power contributions are proportional to the short-circuit mean-square noise current, and input noise source is assumed to be uncorrelated with the device equivalent noise source. The output noise power due to input source can be expressed as $\alpha A \overline{i_s^2}$, and the added noise power can be expressed as $\alpha A \overline{[i_n + Y_s v_n]^2}$, where α is some constant, A is the gain of the device and Y_s is the source admittance. Then the noise factor becomes,

$$F = \frac{\overline{i_s^2} + \overline{[i_n + Y_s v_n]^2}}{\overline{i_s^2}} \quad (3.6)$$

The quantities i_n and v_n in equation (3.6) will generally be correlated. To express this relation more explicitly we write i_n as the sum of two contributions:

$$i_n = i_c + i_u \quad (3.7)$$

where i_c is correlated with v_n and i_u is independent of v_n . The correlated part i_c is related to v_n by

$$i_c = Y_c v_n \quad (3.8)$$

The substitution of equations (3.7) and (3.8) into (3.6) results in

$$F = \frac{\overline{i_s^2} + \overline{[i_u + (Y_s + Y_c)v_n]^2}}{\overline{i_s^2}} = 1 + \frac{\overline{i_u^2} + |Y_s + Y_c|^2 \overline{v_n^2}}{\overline{i_s^2}} \quad (3.9)$$

The noise currents and voltages can also be written in terms of resistance and conductance:

$$\overline{v_n^2} \equiv 4kT\Delta f \cdot R_n \quad (3.10)$$

$$\overline{i_u^2} \equiv 4kT\Delta f \cdot G_u \quad (3.11)$$

$$\overline{i_s^2} \equiv 4kT\Delta f \cdot G_s \quad (3.12)$$

Thus the noise factor can be written in terms of impedances and admittances:

$$\begin{aligned} F &= 1 + \frac{G_u + |Y_s + Y_c|^2 R_n}{G_s} \\ &= 1 + \frac{G_u + [(G_s + G_c)^2 + (B_s + B_c)^2] R_n}{G_s} \end{aligned} \quad (3.13)$$

Where, $Y_s = G_s + jB_s$, $Y_c = G_c + jB_c$.

The noise factor is now minimized with respect to G_s and B_s by equating the appropriate derivative to zero. The minimizing values of these parameters are

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt} \quad (3.14)$$

$$B_s = -B_c = B_{opt} \quad (3.15)$$

The corresponding minimum noise factor is,

$$F_{min} = 1 + 2R_n[G_{opt} + G_c] = 1 + 2R_n \left[\sqrt{\frac{G_u}{R_n} + G_c^2} + G_c \right] \quad (3.16)$$

Using classical noise analysis we have found, for a given device, the source impedance which minimizes noise in that device. In other words, it is possible to adjust device parameters to obtain the best noise figure while keep matching the input impedance. But we still don't have specific guidelines for determining what is the device size which will minimize noise. Furthermore, the very important matter of power consumption was not included in the previous analysis, and the results just obtained could turn out to be impractical.

The typical MOSFET noise model of Figure 3.3 will now be used to find the parameters corresponding to the best NF:

Figure 3.3: MOSFET noise model

Where

In Figure 3.3, $\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f$ (3.17)

$$\overline{v_{ng}^2} = 4kT\delta r_g\Delta f \quad (3.18)$$

$$r_g \approx \frac{1}{5g_{d0}} \quad (3.19)$$

where g_{d0} is the drain-source conductance at zero V_{ds} . The parameter γ has a value between 2/3 and 1. The gate noise coefficient δ has a value of 4/3 in long-channel devices.

To use the classical noise analysis method, we want to find the values of R_n , G_u , and Y_c in equations (3.14)~(3.16). The drain noise current i_{nd} is equivalent to a noise voltage source and a noise current source at the input side and the gate noise voltage is equivalent to a gate current source. All of these noise sources are taken together lead to the noise factor parameters [13]:

$$R_n = \frac{\gamma g_{d0}}{g_m^2} = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \quad (3.20)$$

$$G_u = \frac{\delta \omega^2 C_{gs}^2 (1 - |c|^2)}{5 g_{d0}} \quad (3.21)$$

$$G_c \approx 0 \quad (3.22)$$

$$B_c = \omega C_{gs} \left(1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right) \quad (3.23)$$

where c is the correlation coefficient between gate noise and drain noise. α is defined as $\alpha = g_m / g_{d0}$.

The optimized source impedance and corresponding minimum noise figure are

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} = C_{gs} \sqrt{\frac{\delta}{5\gamma}} (1 - |c|^2) \quad (3.24)$$

$$B_{opt} = -B_c = -\omega C_{gs} \left(1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right) \quad (3.25)$$

$$F_{min} = 1 + 2R_n [G_{opt} + G_c] \approx 1 + \frac{2}{\sqrt{5}} \cdot \frac{\omega}{\omega_T} \sqrt{\gamma \delta (1 - |c|^2)} \quad (3.26)$$

In Equation (3.26), F_{min} is inversely proportional to ω_T , and so any technology advance that results in an improvement of ω_T will automatically bring about one in the noise figure. It is further seen that an increase in the drain/gate current noise correlation would also improve the noise figure.

In principle, equations (3.24) - (3.25) can be used to find the MOSFET size which leads to a minimal noise figure but sometimes this optimization does not lead to usable results. For instance, Lee [13] describes a numerical example where an optimum device NF can be obtained only when the device has a width of 4mm and the bias current is in the region of 100mA. This finding suggests that other parameters are important when carrying out noise optimization - power consumption for one. Careful trade-offs between gain, noise, power, and input match requirements consistent with performance goals are usually vital.

To include power consumption in the noise optimization calculations, one writes the noise factor as [13]:

$$F = F_{min} + \left[\frac{\gamma}{\alpha g_m R_s} \right] \left[1 - \frac{Q_{opt}}{Q_s} \right]^2 \quad (3.27)$$

$$\text{where, } Q_{opt} = \frac{G_{opt}}{\omega C_{gs}} = \alpha \sqrt{\frac{\delta}{5\gamma}} (1 - |c|^2) \quad (3.28)$$

$$Q_s \equiv \frac{1}{\omega C_{gs} R_s} \quad (3.29)$$

The parameters α , g_m , Q_{opt} , Q_s are linked to power dissipation.

Furthermore g_m and Q_s can be expressed as

$$g_m = \alpha \left[\mu_n C_{ox} \frac{W}{L} V_{od} \right] = \alpha g_{m0} \quad (3.30)$$

$$Q_s = \frac{P_0}{P_D (1 + \rho)} \quad (3.31)$$

$$\text{where, } P_0 = \frac{3}{2} \frac{V_{DD} V_{sat} E_{sat}}{\omega R_s} \quad (3.32)$$

$$P_D = V_{DD} I_D = V_{DD} W L C_{ox} v_{sat} E_{sat} \frac{\rho^2}{1 + \rho} \quad (3.33)$$

$$\rho = \frac{V_{gs} - V_t}{L E_{sat}} = \frac{V_{od}}{L E_{sat}} \quad (3.34)$$

E_{sat} is the field strength in short-channel devices, and v_{sat} is given by $v_{sat} = \frac{\mu_n}{2} E_{sat}$.

It can be shown[13] that minimum noise figure occurs when,

$$\rho^2 \approx \frac{P_D}{P_0} \sqrt{\frac{\delta}{5\gamma}} (1 - |c|^2) \left[1 + \sqrt{\frac{7}{4}} \right] \quad (3.35)$$

And the width of the optimum device is,

$$W_{opt, P} \approx \frac{1}{3\omega L C_{ox} R_s} \quad (3.36)$$

and the power-constrained minimum noise figure is

$$F_{min, P} \approx 1 + 2.4 \frac{\gamma}{\alpha} \left[\frac{\omega}{\omega_T} \right] \quad (3.37)$$

A comparison of equations (3.37) and (3.26) shows that at a given frequency, $F_{min, P}$ is worse (as expected) than F_{min} by 0.5dB to 1dB. But this difference is so slight that, in effect, an excellent noise figure is retained while the power consumption is optimized. And importantly, equation (3.36) provides a very simple means of computing the optimum device width in the presence of power consumption limitations.

In brief summary then, a simple means of designing an LNA which satisfies noise figure and power consumption strictures consists of the following steps:

- 1) Use equation (3.36) to determine the necessary device width.
- 2) Bias the device with the suitable current permitted by the power constraint.
- 3) Determine component values consistent with input matching specifications.

It should be noted that this analysis does not take into account the thermal noise generated by other LNA components, chiefly resistors. The presence of resistors in an LNA circuit will cause changes to the F_{min} condition. But even so, equation (3.36) represents a good starting point in the determination of a device width - a starting value which can be refined by simulation.

3.3 LNA Topologies

Since the LNA is the first functional block of a receiver, matching its input impedance to that of the driving source is necessary. The driving source is conventionally resistive (50Ω), but unfortunately the input impedance of a MOSFET is capacitive and making it appear resistive to the source without degrading noise performance is difficult. Various matching methods have been studied to improve LNA performance. Four common LNA topologies which are capable of the required input matching are shown in Figure 3.4. All have single ended organizations which can easily be extended to their differential analogues:

Figure 3.4: LNA topologies (Biasing not shown)

Circuit (a) puts a 50Ω resistor across the input terminals of a common-source amplifier. This straight forward matching technique sees the driver source experiencing a resistive impedance over a wide frequency range. But the resistor will contribute its own thermal noise, and when $R_I = R_s$ the input signal will be attenuated by factor of 2. These two factors lead to an unacceptably high noise figure, and this topology is seldom used in LNA design.

Circuit (b) is a common-gate configuration. A small signal analysis yields an input impedance of $1/g_m$ and it is quite easy to size a transistor so that $1/g_m = 50\Omega$. But restricting g_m in this way also restricts the gain - it cannot be made as large as desired. The associated condition on transistor size also puts a limit on the possible noise figure. It can be shown the noise figure for single common-gate transistor is [7]

$$F \geq 1 + \frac{\gamma}{\alpha} \quad (3.38)$$

For a long-channel device one has $\gamma = 2/3$. If in addition, $\alpha = 1$, the noise figure is $5/3$, or 2.2dB ($10 \log(5/3)$). In the short channel case, γ is larger than $2/3$ and the noise figure will be larger than 2.2dB. So even though it is easier to provide wide-bandwidth impedance matching with circuit (b), it is difficult to achieve high gain and good noise performance.

Circuit (c), which offers an improvement over (a) and (b), is a common-source topology with inductive source degeneration. It finds frequent use in applications where narrow-band impedance matching is required. The small signal model for this topology is shown in Figure 3.5:

Figure 3.5: Small signal model for common-source LNA with inductive source degeneration

In Figure 3.5,

$$V_{in} = (I_{in} + g_m V_{gs}) \cdot sL_s + V_{gs} + I_{in} \cdot sL_g \quad (3.39)$$

$$I_{in} = sC_{gs} \cdot V_{gs} \quad (3.40)$$

The input impedance, by definition is,

$$\begin{aligned} Z_{in} &= \frac{V_{in}}{I_{in}} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s \\ &\approx s(L_s + L_g) + \frac{1}{sC_{gs}} + \omega L_s \end{aligned} \quad (3.41)$$

It shows that at the resonance frequency, the input impedance is purely real and proportional to the source degeneration inductor L_s , so that input matching to 50Ω can be had by adjustment of L_s and L_g . And but for the parasitic resistance of the inductors, there are no additional resistances in the topology - the sole noise source is the transistor itself. The noise optimization method of section 3.2 can be used to obtain an excellent noise performance. The disadvantage of this circuit is that the impedance is real only at the resonance frequency. Thus it is best suited to narrow-bandwidth applications and not the wide bandwidth one of this project. It is noted that recent research shows a trend to use this architecture to provide wide band matching by embedding the input network of the amplifying device in a multisection reactive network.

Circuit (d) is a shunt-series amplifier, one whose shunt feedback and series degeneration resistances makes it capable of broadband input impedance matching. The small signal

model for the shunt-series configuration is shown in Figure 3.6:

Figure 3.6: Small signal model for shunt-series LNA

The effective transconductance of a common-source amplifier with source degeneration is

$$g_{m,eff} = \frac{g_m}{1 + g_m R_1} \quad (3.42)$$

If a test voltage V_{in} is applied between the gate and ground, there will be at nodes d and g the voltages

$$V_{out}(G_L + Y_f) + g_m V_{gs} - V_{in} Y_f = 0 \quad (3.43)$$

$$V_{in} = V_{gs} + (V_{gs} Y_{gs} + g_m V_{gs}) R_1 \quad (3.44)$$

$$\text{where, } G_L = \frac{1}{R_L}, Y_{gs} = \frac{1}{sC_{gs}}, Y_f = \frac{1}{R_f} + \frac{1}{sC_{gd}}$$

The gain of this model circuit is

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{g_m - Y_f(1 + Y_{gs}R_1 + g_m R_1)}{(1 + Y_{gs}R_1 + g_m R_1)(Y_f + G_L)} \quad (3.45)$$

At low frequency, the capacitances C_{gs} & C_{gd} may be disregarded and the gain expression simplified to

$$\begin{aligned} A_v &= -\frac{g_m - \frac{1}{R_f}(1 + g_m R_1)}{(1 + g_m R_1)\left(\frac{1}{R_f} + \frac{1}{R_L}\right)} \\ &= -\frac{R_L}{R_1} \left[\frac{1}{1 + 1/g_m R_1} \right] \left[\frac{1}{1 + R_L/R_f} \right] \left[1 - \frac{1}{g_{m,eff} R_f} \right] \end{aligned} \quad (3.46)$$

It can be seen that the gain of the amplifier, from the gate to the drain, is approximately $-R_L/R_1$, but there are also three attenuation factors. The first one (in brackets) accounts for the effect of source degeneration, the second for the loading of the output node by R_f , and the third for input/output feedforward. But so long as $g_m R_1$ is larger than 1, R_f larger than R_L , and $g_{m,eff} R_f$ is larger than 1, gain loss will be negligible.

The input impedance of this circuit can be deduced from the current at node g :

$$\begin{aligned} I_{in} &= V_{gs} \cdot Y_{gs} + (V_{in} - V_{out}) \cdot Y_f \\ &= \frac{g_{m,eff}}{g_m} \cdot V_{in} \cdot Y_{gs} + (1 - A_v) V_{in} Y_f \end{aligned} \quad (3.47)$$

$$\text{Then, } Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{Y_{gs,eff} + (1 - A_v) Y_f} \quad (3.48)$$

$$Y_{gs,eff} = \frac{g_{m,eff}}{g_m} Y_{gs}$$

The input impedance at low frequency is mainly resistive and dominated by $R_f/(1 - A_v)$.

The value of the feedback resistance R_f can be adjusted to obtain the desired input resistance of 50Ω . At higher frequencies, C_{gs} & C_{gd} cannot be ignored and the input capacitance will be the sum of two terms: C_{gs} degenerated by R_1 , and one due to the Miller effect involving C_{gd} :

$$C_{in} \approx \frac{C_{gs}}{g_m R_1} + C_{gd} \frac{|A_v|}{2} \quad (3.49)$$

The resulting capacitive reactance can be cancelled with a inserted series inductance inserted into the gate line and a 50Ω resistive impedance can then be matched.

The main drawback of a shunt-series amplifier is that the feedback resistance and the source degeneration resistance contribute their own thermal noise to that of other sources, and the observed noise factor will be greater than the device F_{min} by a few decibels. Nonetheless, the broadband capabilities of this circuit make it the one of choice for wide-band applications.

3.4 A Wide-band LNA Design

In this project, the signal can be made to propagate along one of two paths (channels). The central operating frequency of each of them is designed to be tuned over a range from 4.5GHz to 5.5GHz. This requires that the first stage LNA have a wide bandwidth. This requirement was seen to be met by the common gate and the shunt-series feedback topologies (section 3.3). In practice, common gate configuration was found difficult to have a suitable dc bias to the following circuits in this project, and so a differential extension of a shunt-series architecture was chosen for the thesis project:

Figure 3.7: Wide band LNA

Design Setup

The LNA design process starts with the selection of a transistor size guided by considerations of noise figure and power consumption (section 3.2, equation (3.36)). In the present case, this is $120\ \mu$ ($2.5\ \mu$ X 48). The basic shunt-series architecture is modified by placing a capacitor C_F in series with R_F , one whose relatively large value of 1pF provides DC blocking and adequate AC coupling between the input and output nodes. The DC blocking permits the biasing of transistors M_1 and M_2 and the maximization of their g_m values to be done independently, reducing system power consumption and increasing gain. The drain loads R_I also provide DC bias for the output node. To ensure a suitable DC level for driving the next stage, a value R_I of about $200\ \Omega$ was chosen. Once transistor size and loading have been decided, adjustment of resistors R_F and R_S can be used to set other LNA characteristics.

Noise, Gain, Linearity Trade-off

In large transistors, the resistance of a long line of gate polysilicon will be one source of this noise, one which can be diminished by using a multi-finger technique in fabrication [15]. Other thermal noise sources are the resistors R_F and R_S . There is a trade-off to consider when selecting values for these components: high resistances are needed for high gain, but high resistance values are associated with higher noise levels.

An important characteristic of an LNA is its linearity. Since nonlinear effects become worse as signal levels increase, the maximum acceptable level of system distortion can be thought of in terms of the maximum signal level permissible in the system, in other words,

in terms of the system's dynamic range. If a weak desired signal is spectrally near to a strong interferer, which frequently happens when multiple applications share same frequency band, nonlinearity will force desensitization and blocking[7].

Other effects of nonlinearity include cross modulation and intermodulation. The linearity of an LNA is commonly measured by its 1dB compression ('IP1') and the third-order intermodulation product ('IP3').

For instance, suppose an ideal linear input/output relationship ($y(t) = ax(t)$) is supplanted by terms due to nonlinear circuit behavior, thus:

$$y(t) = a_0 + a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \dots \quad (3.50)$$

In such a case, when a sinusoid input signal $x(t) = A \cos(\omega t)$ is applied, the output will be

$$\begin{aligned} y(t) &= a_0 + a_1 A \cos(\omega t) + a_2 A^2 \cos^2(\omega t) + a_3 A^3 \cos^3(\omega t) \\ &= \left(a_0 + \frac{a_2 A}{2} \right) + \left(a_1 A + \frac{3 a_3 A^3}{4} \right) \cos \omega t + \frac{a_2 A^2}{2} \cos 2\omega t + \frac{a_3 A^3}{4} \cos 3\omega t \end{aligned} \quad (3.51)$$

The second term is the desired amplified input signal, but its amplitude does not have the simple form expected from $y(t) = ax(t)$ - there are two terms, the desired gain $a_1 A$, and an undesired part $\frac{3 a_3 A^3}{4}$. Furthermore, a_1 and a_3 are usually of opposite sign in a non-linear system. This means that there are values of A for which the combined amplitude will vanish. It is clear that when A is small ($A < 1$), the linear part dominates the output

signal. But when $A > 1$, the ideal gain is reduced by $\frac{3a_3A^3}{4}$. One defines the 1-dB compression point as being that input signal power for which the small-signal gain is decreased by 1dB, as shown in Figure 3.8:

Figure 3.8: 1 dB compression point definition

Another effect of circuit nonlinearity is intermodulation (IM) distortion, a term describing the situation wherein harmonics of the input wave are multiplied by one another. IM distortion is typically measured by means of the 'two-tone' test in which two sinusoids, $x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$, are applied to the circuit under test. IM products will involve all possible frequency combinations of the form $n\omega_1 \pm m\omega_2$, the dominant ones of which will be the lower-order ones, namely $\omega_1 \pm \omega_2, 2\omega_1, 2\omega_2, 3\omega_1, 3\omega_2, 2\omega_1 - \omega_2, 2\omega_2 - \omega_1$. Of especial interest are the third-order ones at the frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ because they are spectrally near to the desired signal and difficult to separate by filtration. In the two-tone test, one usually sets $A_1 = A_2 = A$ and finds that the third-order IM product amplitudes behave like $\frac{3a_3A^3}{4}$. In other words, the third order IM products increase in

proportion to A^3 while the fundamentals increase in proportion to A . The third intercept point ('IP3') occurs where the total signal amplitude of the third-order IM products equals the fundamental signal amplitude, as shown in Figure 3.9:

Figure 3.9: IIP3 definition

The value of IP3, referred to the input, is called IIP3, and is given by

$$IIP3 = P_{in} + \frac{1}{2}[P_{out} - P_{out, IM3}] \quad (3.52)$$

Because linearity depends strongly on overdrive voltage, IIP3 improvements generally come at the expense of either increased power consumption or reduced gain. It is well known that a source degeneration resistor R_s (Figure 3.7) can improve linearity [16]. But it can also lead to a worsened noise figure and decreased gain. And linearity will also be affected by the shunt feedback resistor (R_f). These effects have been studied by simulation, the simulation results of which are illustrated in Figures 3.10 and 3.11:

Figure 3.10: NF, Gain, IIP3 trade off with R_f Figure 3.11: NF, Gain, IIP3 trade off with R_s

Once again, noise, gain and linearity are not independently controllable when there are two parameters (R_f and R_s) to adjust, and skill at making design tradeoffs will serve the engineer well.

In this project, the main purpose of the input LNA is the driving of two separate Q-enhanced filters. The linearity of the following Q-enhanced filter is critical to this research, therefore it is desirable for the LNA to provide a good linearity. The linearity of

the LNA can be addressed with only peripheral regard to its gain, since the Q-enhanced filter which follows in the signal path can be designed to provide a second stage of gain. We will therefore concentrate on LNA linearity and noise.

This said, we choose the following set of component values:

Components	Value
M_1	$2.5\mu m/0.18\mu m \quad M = 48$
M_2	$2.5\mu m/0.18\mu m \quad M = 48$
R_1	$200 \quad \Omega$
R_f	$800 \quad \Omega$
R_s	$40 \quad \Omega$
C_f	$1 \quad pF$

Table 3.1: Parameters of the wide band LNA

Stability

Stable performance in the frequency range of interest is another issue of amplifier design and is especially important in a feedback system. The stability of a system is related to a reflection at a certain frequency. The conditions for unconditional stability for a two-port system are [17],

$$|\Gamma_L| < 1, |\Gamma_S| < 1 \quad (3.53)$$

$$|\Gamma_{in}| = \left| \frac{S_{11} - \Gamma_L \Delta}{1 - S_{22} \Gamma_L} \right| < 1 \quad (3.54)$$

$$|\Gamma_{out}| = \left| \frac{S_{22} - \Gamma_S \Delta}{1 - S_{11} \Gamma_S} \right| < 1 \quad (3.55)$$

where, $\Delta = S_{11} S_{22} - S_{12} S_{21}$.

$|\Gamma|$ can be represented by a stability circle in the Γ plane. Let,

$$S_{11} = S_{11}^R + jS_{11}^I, S_{22} = S_{22}^R + jS_{22}^I, \Delta = \Delta^R + j\Delta^I, \Gamma = \Gamma^R + j\Gamma^I$$

Submit them into equation (3.54) and (3.55), we can get input stability circle and output stability circle as,

$$(\Gamma_L^R - C_{out}^R)^2 + (\Gamma_L^I - C_{out}^I)^2 = \left(\frac{|S_{12}S_{21}|}{|S_{22}|^2 - |\Delta|^2} \right)^2 = r_{out}^2 \quad (3.56)$$

$$\text{Where, } C_{out} = C_{out}^R + jC_{out}^I = \frac{(S_{22} - S_{11}^* \Delta)^*}{|S_{22}|^2 - |\Delta|^2} \quad (3.57)$$

$$(\Gamma_s^R - C_{in}^R)^2 + (\Gamma_s^I - C_{in}^I)^2 = \left(\frac{|S_{12}S_{21}|}{|S_{11}|^2 - |\Delta|^2} \right)^2 = r_{in}^2 \quad (3.58)$$

$$\text{Where, } C_{in} = C_{in}^R + jC_{in}^I = \frac{(S_{11} - S_{22}^* \Delta)^*}{|S_{11}|^2 - |\Delta|^2} \quad (3.59)$$

Figure 3.12 shows input and output stability circles in Γ plane.

Figure 3.12: Input and output stability circle

When $S_{11} < 1$ and $S_{22} < 1$, unconditionally stability occurs only if the stability circles lie entirely outside of the $|\Gamma_s| < 1$ and $|\Gamma_L| < 1$ boundaries:

$$||C_{in}| - r_{in}| > 1 \quad (3.60)$$

$$||C_{out}| - r_{out}| > 1 \quad (3.61)$$

The conditions for unconditional stability described by equation (3.60) and (3.61) can be written in terms of a stability factor K [17]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1 \quad (3.62)$$

$$\text{and, } B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \quad (3.63)$$

$$\text{where, } |\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$$

A common and effective way to satisfy these conditions is to add a series resistance or a shunt conductance to the input port, and this was done for the project design. The value chosen must of course be small enough to allow signal flow and large enough to render the system unconditional stable. The stability circle and stability factors are shown in Figure 3.13 and 3.14 respectively.

Figure 3.13: Load stability circle on the Smith chart

Figure 3.14: Simulation results of stability factor K and B_1

Summary

A wide band LNA was designed with the preceding considerations in mind and then built using CMOS 0.18 μm technology. Its performance is summarized in Table 3.2:

Operating BW	Gain	NF	K	B_1	$P_{1\text{dB}}$	IIP3	Power
4.0~6.0 GHz	7.0dB $\pm$ 0.5dB	4.5dB	>1	>0	-3.0dB	2.9dB	16.2mW (Vdd = 1.8V)

Table 3.2: Performance of the wide band LNA

A comparison of this design with some published LNA designs is listed in Table 3.3. Most of the LNA designs used inductive degeneration architecture, essentially have good NF. Although this architecture can work at a wide bandwidth, it is mainly used in the narrow band applications by using LC tank loads. This design, on the other hand, is working on a wider band, and has a good linearity performance. The NF performance is degraded by adding the shunt feedback and source degeneration resistance which have more effect on the noise performance than that of transistors in this design.

Author	Arch.	Tech.	Op. BW (GHz)	Gain (dB)	NF (dB)	P _{1dB} (dBm)	IIP3 (dBm)	V _{dd} (V)	Power (mW)
This Design	Shunt-Series Feedback	CMOS 0.18 μ m	4.0-6.0	7.0	4.5	-3.0	2.9	1.8	16.2
S. Lee (2002) [18]	Shunt-Series Feedback	SiGe 0.5 μ m	0.8-1.6	8.4	3	-6			23.1
P. Crippa (2003) [19]	L-degen	SiGe 0.25 μ m	4.4-5	12.8	2.21	-6.2	11.6	2	23.77
H.-R. Kim (2002) [20]	L-degen	SiGe 0.5 μ m	5	18.3	1.65	-12.25	3.95	3	31
Westerwick (2001) [21]	L-degen	CMOS 0.25 μ m	5.15-5.35	16	2.5	-11.7	-1.5	3	48
R.A. Rafla (2000) [22]	L-degen	CMOS 0.25 μ m	5.8	10	3.0	N/A	2	2	24
T. Nguyen (2002) [23]	L-degen	CMOS 0.18 μ m	5.2	18.9	1.7	-15.7	-6	2.7	22.3
W. M. Lim (2003) [24]	L-degen	CMOS 0.18 μ m	5.1-5.9	14.6	3	-17.1	-9	1.5	12.36
C.-W. Kim (2005) [25]	Shunt-Series Feedback	CMOS 0.18 μ m	2-9	10.5-13.5	2.5-7.4	N/A	-5.4	1.8	25.2

Table 3.3: Comparison with published LNA designs

The layout of the integrated LNA is shown in Figure 3.15. A common-centroid method was used:

Figure 3.15: Layout of the wide band LNA

Q-Enhanced Filter and Subsampling Mixer Design

4.1 Introduction

As mentioned in Chapter 2, the full integration of a transceiver front end is contingent upon the ability to realize high performance on-chip RF bandpass filters. Numerous methodologies are available [26] (Figure 4.1):

Figure 4.1: On-chip bandpass filter alternatives

Digital filters of any type and which work at any frequency are possible in principle, but in practice high power demands at high frequencies limits their use in these situations. It has in fact been shown that the power consumption of a digital filter having a 60-80 dB dynamic range and fabricated using a 1- μm process is of the order of

$n/2 \times (\text{number of poles}) \times f_0$, where f_0 is the central frequency [27]. An example supporting this relation is found in [1] - a 4-pole IF filter working at only 10MHz is found to dissipate approximately 40mW. Reductions of these unfavorable DSP power consumption figures have been taking place only gradually, and digital filters will not be displacing their analogue counterparts in high-frequency roles in the foreseeable future.

Currently, analog filters are the only choice for RF band-pass filter implementation. Both passive and active analogue RF filters are amenable to construction using current IC processes, and we will of course concentrate on the active variety. The choices one is faced with when deciding upon an implementation will now be discussed. RC designs are unsuitable for RF work because of op-amp gain and linearity problems at high frequency. Switched capacitor types require amplifiers having very short settling times and their design is complicated by a need for anti-aliasing filtering and 'over-sampling' [1].

There are however two promising configurations: the 'Gm-C' and 'Q-enhanced LC' designs, both of which are suitable for use at high frequencies and have good power-consumption characteristics. The two are conceptually identical but differ in implementation details. Both will be examined in this chapter and comparisons made. It will turn out that the Q-enhanced LC filter is best fitted for the work of this thesis, and its design will be presented.

In all receiver architectures discussed in chapter 2, the RF input signal must be converted to a lower frequency signal for further demodulation or digital signal processing (DSP). This down conversion is usually done by a mixer (an analogue multiplier). A subsampling mixer design is discussed at the end of this chapter.

4.2 Filter Topologies

Second-order Gm-C and Q-enhanced LC bandpass filters can both be developed from the parallel RLC resonator circuit, a single-ended form of which, driven by a transconductance buffer, is shown in Figure 4.2:

Figure 4.2: Parallel RLC resonator

The input transconductor, which furnishes I/O isolation while acting as the resonator current source, can also be made to supply gain should that prove necessary. Practical transconductors and filters are usually implemented in differential form to take advantage of properties including simple biasing, inherent rejection of power supply and crosstalk noise, and the provision of both inverted and non-inverted output. In order that the analysis be simple, a single ended form will be studied - the differential results will be clearly analogous.

The parallel RLC resonator of Figure 4.2 has a transfer function

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{s \cdot \frac{g_{mi}}{C}}{s^2 + s \cdot \frac{1}{RC} + \frac{1}{LC}} \quad (4.1)$$

When this is compared with the general expression of H for a second-order bandpass filter

$$H_{BP}(s) = k \cdot \frac{s \cdot \omega_o}{s^2 + s \cdot \frac{\omega_o}{Q} + \omega_o^2} \quad (4.2)$$

the following identifications can be made:

$$\omega_o = \sqrt{\frac{1}{LC}} \quad (4.3)$$

$$Q = R \cdot \sqrt{\frac{C}{L}} \quad (4.4)$$

That is, the centre frequency is determined by the LC product and the Quality factor (or equivalently, the filter's selectivity) is proportional to R.

Gm-C Filter

The passive RLC resonator is modified by replacing both the passive inductance and resistance with active devices. Figure 4.3a illustrates the active inductor concept, 4.3b the basic circuit topology corresponding to 4.3a, and Figure 4.4 shows an active resistance.

Figure 4.3: Active inductor

Figure 4.4: Equivalent Active Resistor

In Figure 4.3 (a) one has, in the frequency domain,

$$V(s) = I(s) \cdot s \cdot \frac{C}{g_{m1} \cdot g_{m2}} \quad (4.5)$$

The equivalent inductance is read off by inspection: $L_{eff} = \frac{C}{g_{m1} g_{m2}}$.

The resistance equivalent to the circuit of Figure 4.4 is, trivially, $R_{eff} = \frac{1}{g_m}$.

The block diagram of a second-order Gm-C filter employing these ‘synthetic’ R and L elements is

Figure 4.5: Gm-C based bandpass filter

The transfer function, centre frequency, quality factor and gain of this circuit are

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{s \cdot \frac{g_{mi}}{C_1}}{s^2 + s \cdot \frac{g_{mQ}}{C_1} + \frac{g_{m1} g_{m2}}{C_1 C_2}} \quad (4.6)$$

$$\omega_o = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \quad (4.7)$$

$$Q = \sqrt{\frac{C_1}{C_2} \cdot \frac{g_{m1} g_{m2}}{g_{mQ}^2}} \quad (4.8)$$

$$\left. \frac{V_{out}}{V_{in}} \right|_{\omega_o} = \frac{g_{mi}}{g_{mQ}} \quad (4.9)$$

When $C_1 = C_2 = C$ and $g_{m1} = g_{m2} = g_m$, equations (4.7) and (4.8) take on the simple forms

$$\omega_o = \frac{g_m}{C} \quad (4.10)$$

$$Q = \frac{g_m}{g_{mQ}} \quad (4.11)$$

These show that ω_o depend on quantities whose values are independently subject to process variations. Therefore, it will be very hard to achieve accurate frequencies and frequency tuning will be necessary. The ratios of transconductances are more controllable in fabrication than are individual ones, but even so Q-tuning will almost certainly be needed at high-frequencies[1].

Q-enhanced LC Filter

Another topology is using on-chip spiral inductor. Unfortunately, integrated inductors suffer from very low Q values (~ 5) which will degrade the selectivity of the bandpass filter. To compensate for the losses in the inductor, active components can be used to achieve a negative resistance. These filters are commonly referred to as Q-enhanced LC filter as shown in Figure 4.6.

Figure 4.6: Q-enhanced LC filter

In Figure 4.6, L is an ideal inductor and g_o an equivalent parallel conductance whose effects are equivalent to the losses in a real inductor and g_m is the compensative transconductance.

$$\text{Thus, } R_{eff} = \frac{1}{g_o} \parallel \left(-\frac{1}{g_m} \right) = \frac{1}{g_o - g_m} \quad (4.12)$$

$$Q_{eff} = \frac{1}{g_o - g_m} \sqrt{\frac{C}{L}} = \frac{\omega_o C}{g_o - g_m} = \frac{1}{(g_o - g_m) \omega_o L} = \frac{1}{1 - g_m/g_o} Q_o \quad (4.13)$$

The desired Q_{eff} can therefore be brought about with transconductance adjustments.

When $g_m \geq g_o$, the circuit becomes an oscillator. Since g_o is dependent on the IC fabrication process and is uncorrelated with g_m , both Q tuning and frequency tuning will be necessary.

Comparing Gm-C filter with Q-enhanced LC filter, the active inductor in Gm-C filter normally takes less chip area than a spiral on-chip inductor. The advantage of small chip area and high tenability in Gm-C filters make them possible candidates for applications in the frequency range (several hundred megahertz, for example) where the geometric sizes of passive inductors are too large to be integrated[28]. However, more noise and nonlinearity are caused by active components than integrated inductor. This degrades the dynamic range (DR) of the filter. Further quantitative analysis is shown in later section. Q-enhanced LC filter, on the other hand, has advantages of lower power consumption and superior dynamic range than Gm-C filter, is a suitable solution for on-chip Bandpass filter design at higher frequency.

Filter Tuning

Equations (4.10) through to (4.13) tell us that both the central frequency and the Q factor of an active filter depend on the values of on-chip components such as inductors, capacitors and transconductors. Process variation, in-use temperature fluctuation, and parasitics can affect the accuracy of these parameters. The problem becomes even more serious at high frequencies or with high Q-factor circuits, where circuit parasitics and increased sensitivity may even cause the filter to be unstable[34][35]. These problems require the incorporation into the filter design of some means of frequency and Q tuning.

A traditional filter tuning technique is the master-slave arrangement of Figure 4.7:

Figure 4.7: Master-slave tuning architecture

The master circuitry supplies both frequency and Q tuning voltages to the slave. In the case of frequency tuning, the control voltage is generated by a PLL whose loop filter has the same structure as the slave filter, and whose master oscillator, which runs at the filter

centre frequency, is locked to a stable reference. The frequency tuning voltage developed by the PLL can be used to adjust the centre frequency of the slave. The Q tuning voltage, on the other hand, is generated by a peak detector and fed in both the master and the slave filters. In other words, the slave uses control voltages developed in matching master sections, to control the slave sections. Unfortunately, the required degree of matching is hard to obtain in high-Q LC filter. For instance, the maximum frequency deviation between the master and slave filters should be less than half the filter bandwidth. In a typical case of, say, $Q = 500$ and center frequency = 5 GHz, this requirement translates into a maximum frequency deviation of about 0.1%. This requires that the inductors and capacitors of the two filters match to a tolerance of 0.2%, which is very difficult to achieve. Other disadvantages, especially important in portable battery-powered equipment, are the additional power demands of the complicated circuitry of the M/S filter and the larger silicon areas needed.

Another option is to use a 'direct tuning' scheme (Figure 4.8).

Figure 4.8: Direct-tuning architecture

This method can be implemented in digital domain at an early stage, right after the signal is mixed down and sampled. This architecture uses the filter itself to measure the filter parameters, and does not suffer from the high power consumption, large chip areas and reference oscillator interference problems of the master/slave tuning method[34],[36]. The component-matching problems of the latter filter are also absent. The direct-tuning technique is of advantage in RF high-Q LC filters since use can be made of the same ADC and other digital circuitry that are used for demodulating the signal [37]. A disadvantage of direct tuning is that the filter needs to be switched between normal filter and tuning modes. But in many applications, an idle ‘time slot’ is available for this filter tuning cycle.

4.3 Filter Dynamic Range

Filter dynamic range (DR) is an important performance parameter. It determines whether a filter can be used in a given interference environment. Dynamic range is typically defined

$$DR = \frac{P_{1dB}}{P_{noise}} \quad (4.14)$$

where P_{1dB} is the output power at the 1-dB compression point and P_{noise} the output noise floor. Since P_{1dB} and P_{noise} are measured at the same output node, an equivalent definition of dynamic range in terms of voltages is possible:

$$DR = \frac{V_{max}^2}{V_{noise}^2} \quad (4.15)$$

V_{max} is the maximum output voltage attained before the circuit reaches its 1 dB compression point and V_{noise} is the total RMS noise voltage within the specified bandwidth. If V_{max} is known in a given circuit, DR has an inverse dependence on the noise introduced by the circuit elements. In a filter, noise is due mainly to passive resistances and the active transconductors; passive capacitors and inductors ideally do not generate noise. A resistor's contribution to the RMS noise current is found to be [29], [30]

$$i_n^2 = 4kT/R \quad (4.16)$$

Where k is Boltzmann's constant ($1.38 \times 10^{-23} \text{ J/K}^{-1}$), T is the temperature in Kelvins, and R is the resistance value.

The RMS noise current density of a transconductor is approximately[31],

$$i_{ng_m}^2 = 4kT\hbar g_m \quad (4.17)$$

where F is a noise figure peculiar to the transconductor construction details (and usually between 1 and 2), and g_m is the transconductance value.

When the equivalent sources are included in the Gm-C filter of Figure 4.5, there results the circuit of Figure 4.9:

Figure 4.9: Gm-C filter with noise sources

The noise sources in a Gm-C filter are the transconductors, and these are uncorrelated, a situation which simplifies analysis. If we assume the midband gain of the Gm-C filter is unity, then we will have from equation (4.9) that $g_{mi} = g_{mQ}$. Furthermore, if Q is very large (for high selectivity), then $g_{mQ} \ll g_m$ (equation (4.11)). Since the noise power of a transconductor is proportional to the g_m value, the noise contribution from g_{mi} and g_{mQ} will be much less than that of g_m and so can be neglected.

With reference to Figure 4.7, we write two s-domain expressions involving the noise voltage V_n at the output node due to one i_{ng_m} source:

$$V_n \cdot (sC) + V_n \cdot g_{mQ} + V_2 \cdot g_m = 0 \quad (4.18)$$

$$V_2 \cdot (sC) - i_{ng_m} - V_n \cdot g_m = 0 \quad (4.19)$$

Having the solution

$$V_n = -i_{ng_m} \cdot \frac{g_m}{(sC)^2 + (sC)g_{mQ} + g_m^2} \quad (4.20)$$

Thus, at resonant frequency $\omega_0 = g_m/C$, we have

$$V_n^2(f_0) = i_{ng_m}^2 Q^2 \left(\frac{1}{\omega_0 C} \right)^2 = (4kTf_g) Q^2 \left(\frac{1}{\omega_0 C} \right)^2 \quad (4.21)$$

Where $Q = g_m/g_{mQ}$

The total mean squared noise voltage at the output node is the integral over all frequencies of the noise voltage power spectral density (PSD) over all frequencies. Since the two g_m noise sources are uncorrelated, they may be added:

$$\begin{aligned}
V_{noise}^2 &= 2 \int_0^\infty V_n^2(f_0) |H(f)|^2 df = 2 V_n^2(f_0) \int_0^\infty |H(f)|^2 df \\
&= 2 V_n^2(f_0) B_n \\
&= 2 k T F \frac{Q}{C}
\end{aligned} \tag{4.22}$$

Where B_n is the noise bandwidth of the filter, and is given by the well-known

$$\text{result } B_n = \frac{\pi f_0}{2 Q} [1].$$

The dynamic range of the second order Gm-C filter (Figure 4.7) is

$$DR_{Gm-C} = \frac{V_{max}^2}{V_{noise}^2} = \frac{V_{max}^2 C}{2 k T F Q} \tag{4.23}$$

And for higher-order bandpass filters, the optimum dynamic range is found to satisfy [32],

$$DR_{Gm-C} \leq \frac{V_{max}^2 C}{2 k T F Q} \tag{4.24}$$

In a Q-enhanced LC filter whose midband gain is unity, the noise due to the loss resistances of the inductor and the Q-enhanced transconductor is the major part of the total output noise (Figure 4.10):

Figure 4.10: Q-enhanced LC filter with noise sources

where we have,

$$i_{ng_m}^2 = 4kT\tilde{F}g_m \quad (4.25)$$

$$i_{ng_0}^2 = 4kTg_0 \quad (4.26)$$

In the case of a large Q, where $g_m \approx g_0$ (equation (4.13) shows), equation (4.26) becomes

$$i_{ng_0}^2 = 4kTg_m \quad (4.27)$$

The same analysis applied to the functionally-equivalent Gm-C filter yields

$$V_n^2(f_0) \approx 4kT(F+1)g_m Q^2 \left(\frac{1}{\omega_0 C} \right)^2 \quad (4.28)$$

However the g_m of a Q-enhanced LC filter is related to other filter parameters by

$$g_m \approx g_0 = \frac{\omega_0 C}{Q_0} \quad (4.29)$$

and so the dynamic range of the second-order Q-enhanced LC filter of Figure 4.10 is

$$DR_{Q-LC} \approx \frac{V_{max}^2 C}{kT(F+1)Q} Q_0 \quad (4.30)$$

A comparison of equations (4.23) and (4.30) shows clearly that the noise power due to the ordinary- and negative-resistance circuit transconductances found in the Q-enhanced LC filter is a factor of Q_0 less than that from the two transconductances used to implement the active inductance in the Gm-C filter. One can then expect the dynamic range of a Q-enhanced LC filter to be superior to that of a Gm-C filter.

The commonly-used dynamic range expressions (4.23) and (4.30) have been subject to frequent misinterpretation in the form of the widespread notion that the DR of an active bandpass filter is inversely proportional to its quality factor. This idea comes from treating

the voltage V_{max} appearing in these equations as being fixed once the circuit details have been decided upon, when in fact V_{max} depends on the filter's Q factor.

To see this dependence, we start by rewriting the DR equations of the two filter types in terms of power consumption efficiency

$$\eta = \frac{V_{max} i_{max}}{P_{dc}} = \frac{V_{max}^2 \omega_0 C}{P_{dc}} \quad (4.31)$$

and bandwidth

$$f_0 = BQ \quad (4.32)$$

If we consider constant power consumption and constant bandwidth, from definition of power consumption efficiency and bandwidth, Equations (4.23) and (4.30) can be rewritten in terms of these[26]:

$$DR_{GC} = \frac{\eta P_{dc}}{4\pi k T F B Q^2} \quad (4.33)$$

$$DR_{Q-LC} \approx \frac{\eta P_{dc}}{2\pi k T (F+1) B Q^2} Q_0^2 \quad (4.34)$$

These shows that the dynamic range of an active filters actually varies inversely as the square of the filter Q. A more precise dynamic range expression which takes this behavior of V_{max} into account in the case of the Q-enhanced LC filter has been presented in [33]

$$DR_{Q-LC} = \frac{4C^2(x-1)}{K_N^2 L k T (F+1) Q^2} \quad (4.35)$$

where x is 1dB. K_N is a parameter of the MOS device, and is given by $K_N = \sqrt{\frac{1}{2} \mu_n C_{ox} \frac{W}{L}}$.

A midband gain of unity was assumed throughout the previous developments. When this is the case, the noise produced by active transconductors is larger than that due to the input gain stage. However, if it should turn out that a large midband gain (for example, 40dB) is

required of a filter, this situation will be reversed and the input transconductor will become the dominant source of noise, and the effect of the enhancement transconductor can be neglected. A refined expression for the Q-enhanced LC filter DR, which covers the case of large midband gains, is derived in [33]:

$$DR_{Q-LC} \propto \frac{1}{\eta_0 \eta^2} \quad (4.36)$$

This indicates that the dynamic range of the Q-enhanced filter can actually be improved by using a lower Q_0 tank, so long as the filter's midband gain is sufficiently large. This is only true up to the point where the noise due to g_m is significant.

4.4 Q-enhanced LC Filter Design

The Q-enhanced LC filter architecture was selected for this project largely because of its dynamic range and frequency range are both superior to the Gm-C alternative. The full differential Q-enhanced LC filter structure to be used for channel selection is shown in Figure 4.11:

Figure 4.11: Differential Q-enhanced filter

Input Transconductor

The input transconductance is performed by transistors $M_{1a,b}$ and $M_{2a,b}$. This stage boosts the input signal and drives the tank circuit. $M_{2a,b}$ also help in isolating the tank from the input stage. The value of this gain is not critical since most of that required to drive the tank and the output has already been supplied by the first-stage LNA and the following buffer. However, when the gain of the first-stage LNA is not high enough, the NF of the input transconductance will have more effect on the system NF. Low noise performance and suitable gain are the main considerations of this input transconductance.

The circuit is based on a previous design [33], down to device sizing and bias levels. Since it is not used as the first input stage, input matching is not required and the source degeneration inductor can be removed from the previous circuit. The transistors $M_{5a,b}$ are used as current sinks. The gain-controlling input bias levels are produced by a current mirror in reference generation circuit. A common-centroid method was used to lay out the circuit so as to provide good matches of both the input transconductors and the split current sources. The layout of the input stage is shown in Figure 4.12.

Figure 4.12: Q-enhanced filter input transconductors layout

Tank Circuit

A fully-integrated circuit would see the LC tank implemented on-chip. However, because of chip area limitations in this project (1.8 μ mX1.0 μ m granted by CMC), on-chip spiral inductor implementation for two channels is impossible, but it could be done in a ‘real-world’ device. Off-chip inductors, and also on-chip binary-code-controlled switched capacitor banks were used in this design. The latter function as replacements for the varactors found in conventional RF tank circuits, because their use leads to higher Q values, wider tuning ranges and better noise rejection[38]. The physical layout of the actual capacitors is shown in Figure 4.13:

Figure 4.13: Unit capacitors

The fringing electric field capacitance between adjacent metal lines was used to store energy in one of these devices. The resulting ‘vertical’ capacitor have been shown to have higher capacitance density and better matching than that achievable with a parallel-plate structure [39].

A switched capacitor bank using these capacitor units is shown in Figure 4.14:

Figure 4.14: Switched capacitor bank

The banks are made up of capacitors having values $2^k \cdot C_{min}$ when bit number 'k' in the control register is set, and 0 when the bit is cleared. The small unit capacitor C_{min} is about 1.1fF. Values of capacitance from C_{min} , $2 \cdot C_{min}$, ..., $255 \cdot C_{min}$ are therefore possible with an eight-bit control register. The switches are PMOS transistors with size of 3 μ m.

Extracted view simulation result shows the range of the switched capacitor bank varies from 336fF to 606fF shown in Figure 4.15.

Figure 4.15: Capacitors changing range

To build an LC tank working at 5GHz, the two inductor values must be approximately 1nH, and a standard surface mount inductor could be used. However, one cannot ignore the parasitic inductance associated with IC packaging, as the highest available frequency will be limited by this parasitic inductance. For example, the bond-wire inductance of a typical ceramic flap package (CFP) is over 2nH, and the operating frequency of a tank in such a package would be limited to 4GHz. To minimize this effect a Flip-chip assembly method is selected. The previous bonding wires are replaced by solder bumps. In addition to minimizing stray inductance, flip-chip packaging has other important benefits, namely small package size, higher pin count and high clock speed or high signal frequency. Research indicates that the inductance of a solder bump is less than 10% of that of a typical wire bond[40]. This is especially significant in high-frequency applications where the incorrect choice of packaging can result in serious signal distortion.

In this design, gold stud bumping and anisotropic conductive film (ACF) were used to achieve the necessary electrical connections, as shown in Figure 4.16:

Figure 4.16: Anisotropic conductive adhesive attachment

In this assembly method, solder bumps are placed on the die pads in a process similar to that used to fix metal wires in the conventional method. Then the die is then turned over ('flipped') and placed on top of the package, with an ACF between the substrate and the die. The material of the ACF is an insulating plastic, throughout which is dispersed conductive (metal) particles. These particles are squeezed together in the direction that force is applied to the film. This means that it will become conductive in the regions of high compression, that is in the region between the solder bumps and the underlying circuit board (package), and in the direction defined by the force (vertical, 'z'). It will remain insulating in the transverse direction (pin-to-pin).

Enhancement Transconductance

The enhancement transconductance is made up of transistors $M_{3,a,b}$, M_4 and the resistor R_1 . $M_{3,a,b}$ is a differential pair connected to the tank circuit in positive mode. It acts as a negative conductance to cancel the loss conductance in the tank circuit. The differential pair's g_m is controlled by the bias current. As was seen in section 4.2, the high Q of the Q-Enhanced filter depends upon the difference $g_0 - g_m$, with $1/g_m$ being nearly equal to $1/g_0$ over a range extending from a few hundred to two or three thousand Ohms. To reduce the current required to obtain a given g_m in this range, a physically large transistor M_3 should be used. But equation (4.35) shows that a large sized M_3 will reduce the filter's dynamic range. Furthermore, its parasitic capacitance will increase as its size does, and that the nearer this value gets to that of the tank capacitor, the lesser will be the tuning

range. With these things in mind, a size of $W=6\mu\text{m}$ $L=0.22\mu\text{m}$ was chosen to give a good g_m /tuning-range compromise. With this size, the required g_m can be obtained with a reasonable amount of current.

As was mentioned in section 4.2, the Q factor of Q-enhanced LC filter, critical to circuit function, is very sensitive to transconductor nonlinearity. Linearity improvement is the purpose of the source degeneration resistor R_1 and the transconductor transistor M_1 . M_1 is biased to working in triode region, as a resistor whose conductance can be adjusted by V_{degen} for an optimum balance between dynamic range and power consumption. It can be shown the overall transconductance G_m with degeneration is [41],

$$G_m = \frac{g_m}{1 + g_m R} \quad (4.37)$$

where g_m is the transconductance of transistor $M_{3a,b}$ and R is the total degeneration resistance. It shows that the total transconductance G_m is reduced by the factor $(1 + g_m R)^{-1}$, and that as g_m increases without limit, the maximum G_m approaches a limit of $1/R$. This means the total degeneration resistance can not be set higher than the $1/g_0$ value which is equivalent to the tank circuit losses - otherwise a high Q value will not be achievable. It was not certain at the outset just how large R should be, an approach analogous to the switched capacitor bank was adopted. The degeneration resistor in the project IC is a parallel combination of several resistances, each of which has a laser fuse in its current path. In this design, several resistors are placed in parallel to permit resistances

from 700Ω to $1.5\text{K}\Omega$ to be obtained by melting appropriate laser fuses. One disadvantage to the use of degeneration resistors is of course the additional thermal noise that will be introduced, thus degrading the filter's performance.

$M_{6a,b}$ form the split current sinks. This prevents a DC voltage drop across the resistors. The current source transistors M_6 are sized as large as possible in order to minimize the effect of $1/f$ noise of the transconductor [42].

Once again, to achieve good matching, a common-centroid layout method is used for the enhancement transconductors $M_{3a,b}$ as well as for the other transconductors. The layout of the enhancement transconductance circuit is shown in Figure 4.17 and all transistor sizes used may be found in Table 4.1 in summary.

Figure 4.17: Layout of the Q-enhanced block

Performance Summary

Extracted view simulations are done using Cadence spectre tool to exam the performance of the Q-enhanced LC filter combined with the first-stage wide band LNA. Figure 4.18 and 4.19 show the frequency tuning and the Q tuning performance of the filter respectively. In Figure 4.18 we can see that the bandwidth of the filter is changing with the central frequency at the same Q bias condition. This is because the equivalent conductance g_o of the inductor depends on the working frequency. To obtain the same bandwidth at different frequency, Q enhancement biasing needs to be adjusted as well. Figure 4.19 shows that filter Q tuning also causes a slight frequency shift, since the total parasitic capacitance of the filter tank changes slightly with different biasing condition. These agree with the previous analysis that both frequency and Q tuning are needed to obtain accurate central frequency and Q factor for the Q-enhanced LC filter.

Figure 4.18: AC simulation with frequency tuning

Figure 4.19: AC simulation with Q tuning

Figure 4.20 and 4.21 show the noise figure and the IIP3 performance of the Q-enhanced LC filter respectively. It can be seen that the IIP3 of the Q-enhanced LC filter is much lower than that of the first-stage LNA. Improving the linearity performance is critical in the Q-enhanced LC filter design.

Figure 4.20: Noise figure of the system (Wide-band LNA + filter)

Figure 4.21: IIP3 of the system (Wide-band LNA + Filter)

IIP3 results with different filter Q factors are shown in Figure 4.22. The results agree with the analysis (equation (4.34)) that the dynamic range of the filter relates to its Q in an inverse square manner.

Figure 4.22: IIP3 vs. Filter Q

Summaries of transistor sizes used in the Q-enhanced LC filter and the performance of the system including both the wide-band LNA and the filter are listed in Table 4.1 and Table 4.2 respectively.

Transistor	Width (um)	Number of Fingers	Total Width (um)	Length (um)
M_1	2.5	24	60	0.18
M_2	2.5	24	60	0.18
M_3	6	8	48	0.22
M_4	6	16	96	0.22
M_5	10	40	400	0.5
M_6	5	16	80	0.5

Table 4.1: Transistor size of the Q-enhanced filter

Performance (LNA+Filter)	
Technology	0.18um CMOS
Filter order	2
Power Supply	1.8 V
Current at Q=125	
Wide-band LNA	9 mA
Filter input stage	1.8mA
Filter Q-enhancement	1.5mA
f_c tuning range	4.5~6.0 GHz
Voltage gain at Q=125	21 dB
IIP3 at Q=125	-24.3 dB
NF at 5GHz	8 dB

Table 4.2: System performance (LNA + Q-enhanced LC filter)

band limited, suppose f_l is the low frequency band and f_u is the upper band, the signal bandwidth is $B = f_u - f_l$. The classical bandpass theorem for uniform sampling states that the signal can be reconstructed without aliasing if the sampling rate f_s is,

$$\frac{2f_u}{n} \leq f_s \leq \frac{2f_l}{n-1} \quad (4.38)$$

Where n is the integer within f_u/B

$$1 \leq n \leq \left\lfloor \frac{f_u}{B} \right\rfloor \quad (4.39)$$

Figure 4.24 shows the basic structure of a subsampling mixer:

Figure 4.24: Subsampling mixer

A circuit made up of FET switches and capacitors can be used to track and hold the input to a subsampling mixer. The sampling clock performs a function equivalent to that of the local oscillator of the Gilbert mixer:

Figure 4.25: Subsampling in time domain

The diagram shows how a RF signal is sampled by a much lower frequency signal and is directly converted to a low-IF band or even to the baseband signal.

The sample/hold circuit can be combined with the ADC as well, helping to reduce the total system complexity and thereby making more feasible a one-chip realization of the RF front-end and baseband DSP functions.

Although a subsampling mixer has simpler architecture than the Gilbert type mixer, it does suffer from some fundamental problems of its own, such as a higher noise figure and higher power consumption, which will be discussed presently.

Noise

First, the noise issue: when the modulated RF signal is downconverted to the baseband, the noise and interference from external sources that reach the mixer will also be aliased to the baseband as well. Suppose the spectral power density of a bandpass signal is S , the in-band noise power density N_p and N_o is the out-of-band (from external sources) noise power density. The *analog* signal-to-noise ratio (SNR) is thus S/N_p , but the signal-to-noise ratio for the sampled signal will have been degraded by at least the noise aliased from the bands between DC and the passband, and becomes [44]

$$SNR_s \approx \frac{S}{N_p + (n-1)N_o} \quad (4.40)$$

where n is the integer selected for the sampling frequency in equation (4.39)

If the magnitudes of N_o and N_p are the same, and $n \gg 1$ is assumed, the SNR degradation will be around $10 \log(n)$ dB. Substantial out-of-band interference will swamp the

desired signal. An anti-aliasing filter must therefore be used before the subsampling mixer. In this project, the Q-enhanced LC filter acts in this role in addition to doing the channel selection.

Although the extrinsic noise introduced before the subsampling mixer can be reduced by a pre-select filter, the intrinsic noise generated by the sampling switch can not be filtered out. The sampling switch bandwidth of f_u , which is necessary if it is to track the input signal, means that the switching noise has a large bandwidth. This noise will be folded into the baseband of interest $2f_u/f_s$ times, something that is the principle reason for the high noise figure of a subsampling mixer. The reduction of this switch noise is an important concern in practical implementations, but it can never be entirely eliminated.

Power Consumption

The power consumption of the subsampling mixer is another concern. One of the causes of this is the need to minimize clock jitter, which exists even though the sampling frequency is very low compared to the RF. Jitter control of the S/H clock is important because clock inaccuracies reduce the system's SNR [45]. Figure 4.26 provides an example of jitter timing:

Figure 4.26: Sampling jitter

In this example, the ideal sampling time is that of a zero-crossing point of the sampling clock's (waveform Φ_{clk}) negative edge, when the switch is turned off. The effective time of turn-off is when $V_{clk} - V_{in} = V_{th}$, and a timing lag (or lead) therefore introduced if the slope of Φ_{clk} is finite. Timing lags (or leads) are also caused by an imprecise (jittery) clock frequency. The circuitry used to generate a clock signals having a short transition time and a stable frequency consumes more power than that needed for less-demanding requirements. An analysis of the trade off between noise performance and switch buffer power consumption can be found in[46].

4.5.2 Subsampling Circuits Design

Sample/Hold Circuit

Figure 4.27 shows the sample/hold circuit. An open-loop track and hold structure was selected over one employing feedback because of its faster operation speed.

Figure 4.27: S/H circuit

A major problem in S/H circuits is clock-feedthrough. Immediately after switch M_1 is turned off, the electric charge in its channel must flow out through its junctions. If the turn-off is rapid the charge will flow equally into both junctions [47], meaning that one-half of it will flow into the holding capacitor and result in a 'hold step' or 'sampling pedestal' unless measures are taken to prevent this. This is the reason for the 'dummy switch' M_2 between the switch and the capacitor. M_2 size is made one-half that of M_1 so it can accommodate one half of M_1 's channel charge and prevent its transfer to the holding capacitor. In real circuits the clock transition times can not be made fast as one would like and nor can the transistor size ratio be made exactly one-half, but the use of this technique usually results in a hold pedestal less than one-fifth of what it would be without the dummy switches [47]. The other dummy switches in Figure 4.27 ($M_{5, 6, 7, 8}$) help to prevent signals intended for one input port from feeding through to the other.

One must also consider circuit bandwidth when designing a S/H unit - it must of course be sufficient to permit tracking of the RF signal. The bandwidth of the S/H circuit in Figure 4.27 is simply

$$f_{3dB} = \frac{1}{2\pi R_{on}C} \quad (4.41)$$

Where R_{on} is the 'on' resistance of the switch M_1 .

$$R_{on} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L} \right) V_{eff}} \quad (4.42)$$

Large bandwidths mean small holding capacitors and small R_{on} values. But in a practical circuit the capacitor cannot be made too small, or the total output rms noise power will be

too large due to the well known equation $V_{noise(rms)}^2 = \frac{kT}{C_s}$. Furthermore, the holding capacitance must be much larger than the unavoidable parasitic ones so that its effects will dominate those of the latter. Equation (4.42) shows that increasing width of the switch transistor will decrease its on-resistance and thereby help to increase the S/H bandwidth and reduce noise. However, a larger switch size means a larger MOS capacitance must be switched over a large voltage range at high frequencies. This needs larger driving ability—in other words, increases S/H power consumption. With these considerations in mind, a width of 2.5μm was chosen for the four switches and a value of 50fF for the hold capacitors.

Clock Generation

A clock waveform having short transition times, desirable for the reasons discussed in section 5.1, may be produced by the simple circuit of Figure 4.28, where a four stage inverter is used to ‘sharpen’ the zero-crossings of an input sinusoid. Figure 4.29 shows the relevant input and output waveforms. The output duty cycle and the input/output phase can be adjusted by changing the DC level (bias) of the input sinusoid. The measured clock jitter is less than 0.8ps.

Figure 4.28: Clock generator

Figure 4.29: Input sine reference and output clock waveform

Output Buffer Design

The S/H output must be buffered so that the hold capacitor voltage will not be affected by subsequent circuitry. A two stage circuit was designed to do this (Figure 4.30). The input DC level is matched by the first stage of the buffer, which uses PMOS transistors and a PMOS active load. The gain of one source-follower stage is

$$G = \frac{g_m R}{1 + g_m R} \quad (4.43)$$

and for the two cascaded stages of Figure 4.30,

$$G_{total} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{m1}} \cdot \frac{g_{m3} R_L}{1 + g_{m3} R_L} \quad (4.44)$$

Figure 4.30: Two stage buffer for S/H block

The gain for each stage of the source follower is seen to be less 1 - this two-stage buffer therefore displays a net loss of gain (With an output load of 50Ω , this loss is about 5 dB.) Simulation results also show that the buffer's bandwidth is less than 1GHz, and so it will also act as a low pass filter and help to remove RF from the signal path.

Figure 4.31: Layout of subsampling circuits

Layout

Figure 4.31 shows the layout of the subsampling block. Layout methods similar to those described in previous chapters, using the common-centroid arrangement and guard rings, are used.

Simulation Result

Figure 4.32 - 4.34 show the performance of the subsampling block. A transient simulation result in Figure 4.32 shows the basic function of subsampling. A low frequency signal is generated from the RF signal. Figure 4.33 shows the NF of the subsampling circuit is up to 30dB near the sampling frequency. This is expected from the noise analysis in previous section (section 5.1.1). Simulation result in Figure 4.34 also proves the good linearity of the subsampling circuit. A summary of the performance of this subsampling design is listed in Table 4.3. It is noted that the clock generation buffer costs much more current than the S/H circuit and the output buffer. However, clock generation block in this project is only used for test purpose, optimized design of PLL and clock generation circuits in real design will significantly reduce the power consumption and the clock jitter.

Subsampling Block Performance	
NF @ 50MHz	32dB
Clock jitter	<0.8 ps
IIP3	7.2dB
Voltage	1.8V
Current	
S/H+buffer	2.6mA
Clock gen.	8.4mA
Total	11mA

Table 4.3: Subsampling circuit performance

Figure 4.32: S/H circuits transient simulation result

Figure 4.33: Subsampling block NF

Figure 4.34: IIP3 result from PAC simulation

System Integration and Measurement

With the main functional blocks (LNA, Q-enhanced filter, subsampling circuit) of previous chapters in hand, we are now ready to assemble the dual channel RF receiver front end. The integration of the dual channel RF front end system is presented first. A major issue when multi-channel RF circuits are implemented in a single chip die is the signal coupling between different channels. The substrate coupling issue is then examined. The chip measurement demonstrating the system performance and interchannel coupling issue are discussed at the end of this chapter.

5.1 System Integration

The system level block diagram is shown in Figure 5.1. Descriptions of the control blocks, used to coordinate the activities of the functional ones, follow.

Figure 5.1: Dual channel RF front end system diagram

Digital to Analogue Converters

The DAC circuits, used to convert digital control bits to analog control signals, are taken from a previous design, an 8-bit one of which is outlined in Figure 5.2. Control bits are used to apply either V_{dd} or V_{ref} to the PMOS transistors $M_5 - M_{12}$ and so control the current flowing through the diode-connected transistor M_1 and thus the voltage appearing at its drain node (V_{bias}) which in turn is fed as a control to a functional block. Control currents are generated in a similar fashion.

Figure 5.2: 8-bit Digital-to-Analog converter circuit

SPI Interface

The (digital) SPI core is also taken from a previous design. Sixteen 8-bit control registers which are set via the 4-bit SPI interface register provide 128 control bits all told, significantly reducing the number of input pins needed for the package. These are the bits which are fed to the digital to analog converters (DAC) as described above.

RF Buffer

An RF buffer and a biasing circuit are placed between the Q-enhanced LC filter and the sub-sampling block in each channel as shown in Figure 5.3. The buffer, a single stage source-follower, drives the sampling/hold circuit and isolates the subsampling block from the filter. The coupling and biasing circuit provides a suitable DC level to the S/H circuit.

Figure 5.3: RF buffer and coupling circuit

RF Driver

A two stage RF driver (Figure 5.4) is used to couple the Q-enhanced filter's RF output to external monitoring devices. Its load resistors are placed off-chip in order to save layout space and to increase flexibility.

Figure 5.4: RF output buffer

Receiver Implementation

The receiver was implemented using a standard 0.18 μ m CMOS process on an 1800 μ m x 1100 μ m chip. The chip layout is shown in Figure 5.5. The system performance is listed in Table 5.1.

System Performance							
Technology	Die area		NF (dB)	Gain (dB)	IIP3 (dB)	Current (mA)	Vdd (V)
0.18 μ m CMOS	1.8mm x 1.1mm	Wide band LNA	4.5	7	2.9	9	1.8
		LNA + Q-enhanced Filter	8	21 (Q=125)	-24.3	3.3 (x2)	
		Subsampling block	32		7.2	2.6 (x2)	
		System	10.4	13		Clk gen. 8 Bufs 2.4 <u>Others 4.2</u> Total 35.4	

Table 5.1: System Performance

Figure 5.5: Dual channel receiver front end layout

Simulation results in Figure 5.6 to 5.10 show the system performance. The system noise figure (NF) of 10.4dB at 5GHz is shown in Figure 5.6. Figure 5.7 shows the independent channel selection function of the dual channel system. Transient simulation results in Figure 5.8 and 5.9 give further examination of channel selection performance of each channel. And in Figure 5.10, subsampling function is shown - the RF signal is downconverted to a low frequency signal of 50MHz.

Figure 5.6: System noise figure

Figure 5.7: System AC simulation

Figure 5.8: Channel 1 RF output spectrum

Figure 5.9: Channel 2 RF output spectrum

Figure 5.10: Subsampling output spectrum

5.2 Substrate Coupling Analysis

On the substrate of a crowded one-chip transceiver, sensitive low-noise circuits will be integrated along with noise-generating digital and switching ones. Unless carefully controlled, the substrate coupling of noise in the congested environment will negate the expected system on chip (SoC) advantages of high-frequency performance, low cost and low power consumption.

In this project, two channels of a receiver front end are implemented within the confines of a single die area, and signal coupling between the two channels is an important issue. One major cause of interaction between circuit blocks is the less-than-ideal isolation provided by their common substrate [48]. Currents can flow through the substrate between blocks - either the 'displacement' current due to capacitance or the flow of charge enabled by substrate conductivity. In this section we will examine the sources, mechanisms and effects of substrate coupling along with the techniques used to model these. Various methods of substrate de-coupling will be discussed. Simulation using the Cadence Substrate Coupling Analysis (SCA) tool is used to demonstrate the coupling issues arising in this project.

5.2.1 Substrate Coupling Mechanism

Substrate Profile

The non-ideal isolation of circuit blocks lying on a common substrate is the main source of coupling problems. Items of concern include substrate resistivity and permittivity. The

resistivity depends on the level of impurity doping as shown in Table 5.2[49]:

Doping Level (cm^{-3})	Resistivity (Ωcm)	f_c
10^{14}	125.6	1.2
10^{15}	12.7	12.0
10^{16}	1.4	> 100
10^{18}	0.035	> 1000

Table 5.2: Comparison between substrate doping levels (p-type substrate)

The equivalent resistance and capacitance of the substrate are related by [50]

$$f_c = \frac{1}{2\pi r_{sub} C_{sub}} = \frac{1}{2\pi \rho_{sub} \epsilon_{Si}} \quad (5.1)$$

f_c being the cut-off frequency, r_{sub} and C_{sub} the equivalent resistance and capacitance of the substrate, and ρ_{sub} and ϵ_{Si} are respectively the resistivity of the substrate and the permittivity of silicon. Typical uniform substrate profile used in RF designs has resistivities varying from 10-20 Ωcm .

Substrate Current Injection

Every device on the substrate will be responsible to some extent for the injection of current into the substrate. In RF circuits, the problem is especially serious since it leads to considerable signal power loss in a particularly sensitive part of a radio IC. The three most important mechanisms of substrate current injection are now discussed:

1. Capacitive Injection

The depletion capacitance of the p-n junction and the capacitance of IC interconnect traces provide the routes for displacement current coupling between circuit elements, a mechanism that is particularly important at high frequencies. Figure 5.11 illustrates some circuit features that are responsible for this type of coupling:

Figure 5.11: Capacitive link to the substrate

2. Resistive Injection

If a layer on the substrate is metal or has the same doping type as the substrate, it will be responsible for a resistive link to the substrate. Substrate contacts placed near a device are examples of situations where signal can directly flow into the substrate. This effect is more dominant than the capacitive coupling in most circuits[49].

3. Impact Ionization

With increasing speeds of operation and decreasing IC feature sizes has come an increasing importance of the role of impact ionization as a cause of substrate current injection[51]. Impact ionization is a phenomena that electron-hole pairs are generated due to the collisions between highly energized electrons. When the electric field in the depleted drain end of a MOS transistor becomes large enough to cause impact ionization, the electron-hole pairs thus created act as carriers of charge into the substrate.

Substrate Coupling

The currents resulting in processes reviewed above couple to other devices through the substrate. Substrate coupling is of great concern in RF circuits, analog-digital mixed signal designs and high speed digital designs. Substrate coupling in RF circuits can seriously interfere with the low-power signals being processed, degrading amplifier gain and bandwidth. In high speed digital-only ASIC design, substrate coupling can be such as to cause cross talking problems and timing errors. Figure 5.12 shows a typical substrate coupling path.

Figure 5.12: The substrate coupling process

5.2.2 Substrate Modeling

An analysis of substrate coupling is contingent upon the availability of an accurate substrate model. Several works have done research on this issue during the past decades [48], [50]-[54]. When the operating frequency is up to several GHz, the substrate behaves essentially as a purely conductive medium, and resistive macromodels are adequate for the substrate modeling. Such macromodels can be developed using the single node model, the Finite Difference (FD) method or the Green function approach with the Boundary Element Method (BEM).

To determine a reduced-order substrate model, an equipotential port is defined for each device and every contact location of the physical implementation. An equivalent matrix of admittances interconnecting the ports is then extracted to form the substrate macromodel.

In the BEM, each port on the substrate is taken to consist of one or several panels. An impedance matrix is formulated using the Green function for the medium. The Green function for a medium is defined as the potential at any point therein subject to the boundary conditions appropriate to a unit current injected at any point also within the medium [52]. The admittance matrix is obtained on inverting the impedance matrix. Figure 5.13 shows how the Green function technique connects the resistive mesh to the substrate ports.

Figure 5.13: Using Green function through substrate ports

The panel-to-panel admittance matrix for Figure 5.13 is

$$\begin{bmatrix} y_{11} & y_{12} & y_{13} & y_{14} \\ y_{12} & y_{22} & y_{23} & y_{24} \\ y_{13} & y_{23} & y_{33} & y_{34} \\ y_{14} & y_{24} & y_{34} & y_{44} \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} & z_{13} & z_{14} \\ z_{12} & z_{22} & z_{23} & z_{24} \\ z_{13} & z_{23} & z_{33} & z_{34} \\ z_{14} & z_{24} & z_{34} & z_{44} \end{bmatrix}^{-1} \quad (5.2)$$

The resistances between the ports are

$$R_{ab} = \frac{1}{y_{13} + y_{23}}, R_{bc} = \frac{1}{y_{34}}, R_{ac} = \frac{1}{y_{14} + y_{24}} \quad (5.3)$$

The panel-to-panel impedance, z_{ij} is analytically determined using the substrate Green function in a preprocessing phase.

Once the substrate model has been determined, an analysis of the substrate coupling can then be done with an analog simulator.

5.2.3 Substrate Coupling Reduction

The substrate coupling problem must be kept in mind at all stages of the design process, including actual circuit design, layout and packaging.

Circuit Design

The differential circuit is a favorite of RF designers because of its immunity to common mode noise. Most of the circuits developed for this project are of the differential kind. However, the differential circuits may sometimes not be as effective as expected because of their non-differential bias circuitry being affected by substrate coupling.

Layout

Many processing and layout techniques have been developed in efforts to increase the isolation between devices[55][56][57] and so decrease substrate coupling. The use of guard ring structures around noisy and sensitive circuitry is one effective technique. The guard

ring is usually tied to ground via a dedicated package pin, the idea being to divert injected substrate current to ground. In the project of this thesis, guard rings are placed around each functional block and especially between the two channels (Figure 5.5). Another layout technique sees N-WELL trenches being deployed to isolate noisy from sensitive circuitry and to block any current that might otherwise flow near the surface of the substrate.

Packaging

To reduce the inductive noise caused by nonideal power supplies through bondwires and package pins, a packaging method having low parasitic inductance is desired. In this project, a flip-chip package was selected, as it has a significantly smaller stray inductance problem than seen with ordinary wire-bonding.

The coupling reduction techniques also include floor plan consideration. As shown in the layout view of Figure 5.5, two channels are put as far as possible. Tank circuits are located at opposite side of the chip. The idea is that the further the sensitive and noisy circuits are apart, the less substrate coupling will affect the circuit's performance.

5.2.4 SCA Simulation

A simulation showing the substrate coupling issue is done using Cadence SCA (Substrate Coupling Analysis) tool. In SCA flow[58], the modified DIVA rules are applied to extract the geometric shapes and connectivities from the layout view. The SCA core modeling engine uses this extracted information to generate the corresponding substrate model. the resulting parasitic substrate coupling model is then inserted in the extract view. Normal analog simulations (Spectre or SpectreRF) can be run using the updated extract view.

Simulation results with/without the substrate coupling model are shown in Figure 5.14 and 5.15 respectively. It can be seen that when considering the substrate coupling issue, the desired signal at 5 GHz is degraded by 6.8 dB. The inter-channel signal at 5.2GHz, on the other hand, is increased by 7.8 dB. There are mainly two reasons can be considered for the desired signal degradation. First, substrate current injection causes the signal loss as discussed in section 5.3.1. Second, when consider the substrate resistance, the equivalent resistance loss of the filter is increased which decrease the filter Q factor. As a result, the output signal is degraded. This effect can be tuned out by increasing the compensative conductance. The increasing of the inter-channel signal is mainly caused by the substrate coupling. The signal at 5.2 GHz is coupled to the desired channel of 5 GHz through the substrate. The simulation results show clearly the serious problem of substrate coupling in a multi-channel chip design. More research needs to be done to improve the channel isolation.

Figure 5.14: Extracted view simulation without the substrate coupling model

Figure 5.15: Extracted view simulation with the substrate coupling model

5.3 Measurement

5.3.1 Test setup

The dual channel RF front end design was implemented using TSMC 0.18 μ m CMOS process. To accomplish the chip measurement, both flip chip and bond wire packaging are used for the same spare die. Since the original design is designed to work at 5 GHz band, the flip chip package test is desirable which eliminates the bond-wire inductance. The standard surface mount inductor and the on-chip switched capacitor banks are expected to create a tank circuit oscillating at 5GHz range. However, with a continuous delay of flip chip packaging process, the measurement is done using a bond wire package. The higher inductance of the bond wire degrades the working frequency done to 1.6~2.0GHz. Even the bond wire chip does not work at the same 5GHz RF band as the flip chip does, most system performance such as frequency tuning, filter Q tuning, and interchannel coupling issue can be confirmed.

The measurement system is set up as Figure 5.16. Two signal generators are combined

together to create one or two tone RF signal. A signal generator generates a sine wave as the subsampling reference input. The FPGA is controlled by a PC through a GPIB interface, and is used to generate all control signals to the SPI core in the chip. All registers in the SPI core can be set from the PC. The RF output and the downconverted signal can be monitored by a spectrum or an oscilloscope. The source meter is used as the power supply and the current can be monitored.

Figure 5.16: Measurement system setup

Figure 5.17: Test Board

5.3.2 Measurement results

Frequency tuning

As discussed in section 4.2, when there is big enough current going through the Q-enhanced $-g_m$ transconductance, the filter becomes an oscillator. This is a easy method to determined the central frequency of the Q-enhanced filter. The filter can be tuned to oscillating at selected frequency first, then the desired filter Q can be obtained by reducing the bias current of the compensative transconductance. The central frequency of the filter can be tuned by adjusting the control bits of the switched capacitor bank. Figure 5.18 shows the frequency tuning performance of the filter in channel one. The central frequency can be tuned from 1.58GHz to 1.80GHz. The tuning range of the filter in channel two is slightly different from 1.57GHz to 1.78GHz due to the different tank inductance. The different tank inductance is mainly caused by the different length of the bond wires and the traces on the test board. It is also observed that the filter is much easier to be tuned oscillating at higher frequency with lower bias current. This agrees with the analysis and simulation result in section 4.4.

Figure 5.18: Filter frequency tuning

Filter Q tuning

The Q factor of the Q -enhanced filter is controlled by adjusting the bias current of the compensative transconductance. The on chip DAC (Digital to Analog Converter) changes sixteen digital control bits to a reference voltage which changes the bias current. Figure 5.19 shows the Q -tuning performance of the filter for channel one. To keep the filter central frequency at the same frequency, frequency control bits need to be adjusted slightly as well as discussed in the previous sections.

Figure 5.19: Filter Q -tuning

System measurement and inter-channel coupling

To test the dual channel front end system and the interchannel coupling issue, a two tone test is done by setting input RF signal as a combination of two RF carrier signals. One RF carrier signal is set to be 1.7940GHz, the other one is 1.7923GHz, 1.7MHz from the first one. The two RF signals are set with same power levels. The central frequencies of the two Q -enhanced filters are tuned to be 1.7940GHz and 1.7923GHz respectively. When filter Q is tuned high enough, each filter selects only one RF signal and filters out the other one. A sinusoid wave of 140MHz is used as the subsampling reference clock. The down-

converted signals of 26MHz ($13 \times 140\text{MHz} - 1794\text{MHz}$) or 27.7MHz ($13 \times 140\text{MHz} - 1792.3\text{MHz}$) can be confirmed from the low frequency output buffers of each channel. Ideally, only one RF signal is selected by the filter of each channel, and only one down-converted signal is sent out from its subsampling buffer. However, the RF signal selected by one channel can be coupled to the other channel through the substrate and the bond wire. From spectrum, two down-converted signal can be confirmed. Figure 5.20 shows perfect channel selection when only one channel is enabled. In this test, channel one is enabled and channel two is disabled. Only one RF signal at 1.794GHz is selected by the filter in channel one, the signal at 1.7923GHz is filtered out. Therefore, a down-converted signal of 26MHz can be monitored from the spectrum.

Figure 5.20: Down-converted signal spectrum with one channel enable

When two channels are enabled, the Q-enhanced filter of each channel selects one RF signal respectively. However, Selected RF signal can be coupled from one channel to the other one through the substrate and bond wire. The subsampling mixer then converts both the desired RF signal and the coupled RF signal to low frequency signals. Two down-converted signals can be seen from the spectrum analyzer as shown in Figure 5.21. The desired RF signal is converted to 26MHz, and the coupled RF signal is converted to

27.7MHz. With all the efforts of substrate coupling reduction methods used in this design, the coupled signal power is about 15.5dBm less than the desired signal power. The power levels of both desired signal and coupled signal are increased when input RF signals are increased simultaneously, but the difference between the two down-converted signals does not change significantly.

Figure 5.21: Down-converted signal spectrum with both channels enable

The channel interference shown in Figure 5.20 is caused by both substrate coupling and bond wire coupling. In order to have an accurate measurement of substrate coupling issue, a flip chip test is desired. However, the flip chip test board has not been received from CMC up to date. (We have been waiting for almost one year). Another issue in current test chip is that the wide band LNA at the input stage is not working properly. Although a large signal can be feed into the filters for further test, some system performance, such as NF and dynamic range, can not be measured properly. An assembly problem is thought to be the reason that the wide band LNA doesn't work well.

Even the two issues listed above limited the whole system measurement, the most major parts of this project are working well. Filter frequency tuning and Q tuning can be examined. Inter-channel coupling issue is confirmed. The main test goals are achieved.

Conclusion and Future Work

The dual channel RF front end receiver with Q-enhanced LC filters has been presented. This system includes two separate receive channels, each channel has LNA, Q-enhanced LC filter and subsampling mixer. In this receiver architecture, Q-enhanced LC filter is used to select the channel at RF band, subsampling mixer converts the selected RF signal directly down to low IF band. The on-chip RF filtering and simple subsampling mixing reduce the complexity of the whole system, make it easier to be integrated with further digital signal processing to create a SoC (System on a Chip). Successful down-conversion measurement demonstrates the feasibility of the system.

To drive the two separate channels over a wide frequency range, a wide band LNA is designed as the first input stage. Unlike using inductive source degeneration in the normal narrow band LNA designs, a common-source LNA with shunt-series feedback architecture is selected. Even this type of LNA has worse NF performance than the LNA with inductive source degeneration, it provides a wider working range, good linearity and reasonable gain performance.

The Q-enhanced LC filter and the subsampling mixer are the core circuits in this system. Analysis and comparison of Q-enhanced LC filter and Gm-C filter shows the super

dynamic range of the Q-enhanced LC filter. It is more suitable for on-chip filtering at RF band. Both frequency tuning and Q tuning are necessary for the Q-enhanced filter. The central frequency of the filter can be tuned by adjusting the on-chip switch capacitors. The filter Q factor can also be adjusted by changing the bias current of the compensative transconductance. The subsampling mixer has very simple structure. The S/H circuit can also be combined with the ADC, helping to reduce the total complexity and thereby making more feasible SoC design including RF front-end and baseband DSP functions. On the other hand, the subsampling mixer suffers high noise figure and high power consumption for its clock generation circuit.

In this project, the wide band LNA is newly designed. Other blocks such as Q-enhanced LC filter, subsampling mixer and RF buffers are redesigned in both circuit and layout with optimized parameters for the working frequency range of 5GHz band based on the previous design architectures. Circuits such as SPI interface, DAC, and clock generator are used the previous design, but the layouts are integrated at the chip level layout.

One of the main goals of this project is to examine the interchannel coupling issue when two channels are built on a single die area. Simulation and chip measurement show the effect of RF signal from one channel couples to the other channel. Different substrate coupling reduction techniques are discussed and used in this project. The main contributions of this project are listed as follows:

- A dual channel receiver front end is implemented in a single die area using standard CMOS technology.

- Independent channel selection and subsampling down-conversion function are examined.
- Independent filter frequency tuning and Q tuning are confirmed.
- Interchannel coupling issue is demonstrated and measured using the test chip.

There are some issues that await exploration in the future studies. Since the chip measurement in this project used a bond wire chip, the interchannel coupling issue includes the bond wire coupling effort. Further measurement using flip chip package expects fewer interchannel coupling. Also, to implement a full on-chip RF filter, the effect of on-chip inductor implementation is worth examining. Since the filter frequency is very sensitive to parasitic capacitance, the frequency tuning and Q tuning of two channels affect each other. Adaptive frequency tuning and Q tuning techniques need to be implemented for system integration. Finally, the high bandwidth and low noise implementation of subsampling block is another research topic.

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Appendix A: Detail Design Schematics

Appendix A.1: Top level Schematic

Appendix A.2: Wide band LNA schematic

Appendix A.3: Q-enhanced filter input stage schematic

Appendix A.4: Q enhancement circuit schematic

Appendix A.5: RF buffer schematic

Appendix A.6: RF coupling and DC bias schematic

Appendix A.9: Sampling clock generation schematic

Appendix A.10: Voltage bias generation circuit schematic

Appendix A.12: Q enhancement current bias generation circuit schematic