A Delay Cell for 40 Gb/s FFE

By

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Abstract

This thesis presents a new architecture for a delay cell, a basic building block of feedforward equalization (FFE). Design and analysis details of the delay cell are described, and simulation results are presented. A prototype is created in which 18 delay cells are cascaded into a tapped-delay-line, as would be used in an 18-tap transversal FFE filter. Experimental results of the prototype are reported and compared to expected results from simulation.

The delay cell designed in this thesis is used as part of a feedforward equalizer which reduces the effects of inter-symbol interference (ISI). Tradeoffs studied in this thesis involved the number of taps, the tap spacing, the frequency response, silicon area, power consumption, and tuning capabilities.

The delay cell presented in this work utilizes compact stacked-inductors to yield a solution having small area and low power consumption. These inductors also aid in achieving the bandwidth required for a 40 Gb/s data-rate, across 18 cascaded delay cells and in a CMOS process. Unlike an all-passive component solution, this delay cell provides no loss of signal strength due to its active elements. Tuning capacity was added to the delay cell to account for variations in process, voltage, and temperature.

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Abbreviations

ASITIC	Analysis and Simulation of Spiral Inductors and Transformers for Integrated Circuits
BER	Bit-Error Rate
CD	Chromatic Dispersion
CDR	Clock and Data Recovery
CMOS	Complementary Metal-Oxide Semiconductor
CMP	Chemical Mechanical Planarization
DCM	Dispersion Compensation Module
DFE	Decision-Feedback Equalization
DUT	Device Under Test
EDC	Electronic Dispersion Compensation
ESD	Electrostatic Discharge
FBE	Feedback Equalization
FFE	Feedforward Equalization
FIR	Finite Impulse Response
FSE	Fractionally-Spaced Equalizer
Gb/s	Gigabit per Second
ISI	Inter-Symbol Interference

LVS	Layout versus Schematic
MD	Modal Dispersion
MIM	Metal-Insulator-Metal
MMF	Multi-Mode Fiber
NRZ	Non-Return to Zero
PMD	Polarization Mode Dispersion
PCB	Printed Circuit Board
RF	Radio Frequency
SMF	Single-Mode Fiber
TWA	Traveling Wave Amplifier
VNA	Vector Network Analyzer

Chapter 1 Introduction

1.1 Motivation for This Work

As serial data rates in legacy optical fiber channels and backplanes continue to increase, dispersion and frequency dependent attenuation become increasingly more problematic. The pulse spreading of the transmission medium's impulse response leads to inter-symbol interference (ISI), which causes jitter and closure of the eye. At high data rates, low bit-error-rate clock and data recovery becomes impossible without some form of compensation for the non-ideal transfer characteristics of the medium.

Electronic dispersion compensation (EDC) is a term referring to a collection of electronic filtering techniques to provide such compensation. When compared to optical dispersion compensation, EDC provides a low-cost solution when produced in large volumes. One such EDC filtering technique is feedforward equalization (FFE). By increasing the data rate on a legacy medium, the number of transversal filter taps required in an FFE increases. Therefore, one of the design challenges presented for FFE with data rates greater than 10 Gb/s is the design of a tapped delay line with a large number of taps, and still capable of maintaining the signal bandwidth across it.

The principle motivation for this research was to develop a delay cell, that when cascaded into an 18-tap delay line with T/3 tap spacing, is capable of maintaining the bandwidth required for 40 Gb/s serial data. Additionally, this tapped delay line was to possess the properties that would make it feasible to include it in an actual product; these properties include low cost, small area, low power, no signal attenuation, constant group delay, and the ability to be tuned in order to counteract variations of process, voltage, and temperature.

1.2 Contributions to Research Field

The research presented in this work contributes to the knowledge of serial data equalization, specifically in the area of delay cells for receiver feedforward equalization. A novel transversal filter delay cell is presented. By using a combination of

active and passive circuit components, circuit area is greatly reduced and signal strength is maintained when compared to traditional all-passive implementations. The delay cell has been made tunable, providing the capability to counter variations of process, voltage, and temperature. When cascaded into an 18-tap delay-line, the bandwidth required for 40 Gb/s data equalization is achieved. This work demonstrates the feasibility of 40 Gb/s feedforward equalization in CMOS, capable of cancelling 6 symbols of ISI.

1.3 Thesis Overview

This thesis is organized as follows. First a background review of equalizers is presented in Chapter 2. This section describes some of the causes of distortion, and the need for equalization. Also presented are various types of equalizers, and a summary of receiver FFE delay cells architectures from the literature. A new architecture for an FFE delay cell is proposed in Chapter 3, along with analysis and design details of the cell. A subsection on the design of stacked-inductors used in the delay cell is also given. Chapter 4 and Chapter 5 describe the design, layout, and simulation of a testchip that was constructed to characterize the proposed delay cell. Details of the delay cell and tapped-delay-line portions of the prototype are given in Chapter 4, while the testchip top-level is described in Chapter 5. Chapter 6 presents and discusses the experimental results of the delay cell prototype, and for stacked-inductor test structures that were created in a different technology. Final conclusions are given in Chapter 7.

Chapter 2 Background

2.1 Inter-Symbol Interference

There are three basic components that all communication systems have in common: a transmitter, a channel, and a receiver (as shown in Figure 1). Communication channel mediums include printed circuit board (PCB) traces, optical fiber, twisted pair, coaxial cable, and air. Ideally, the signal at the receiver would be identical to that at the transmitter. However, due to non-ideal channel characteristics, there will always be some distortion of the received signal. This distortion will have varying effects at different frequencies, resulting in pulse-spreading. When pulse-spreading becomes severe, it results in inter-symbol-interference (ISI); this occurs when pulses overlap one another, and can lead to increased bit-error rates (BER) in receivers.

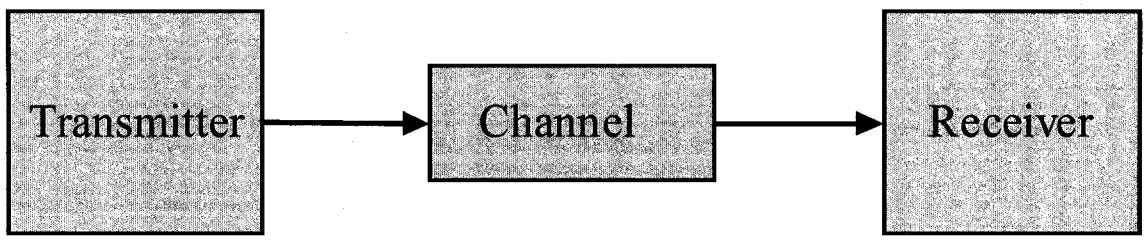


Figure 1 Basic Components of Communication Systems

Shown below in Figure 2 is an example of how ISI can cause bit-errors. An ideal non-return-to-zero (NRZ) bit stream is sent from the transmitter. As the transmitted data passes through the medium, pulse spreading occurs causing symbols to interfere with one another. In order to decipher the symbol elements at the receiver, a reference level is used; due to ISI, the 5^{th} bit does not reach the reference level. Therefore a bit-error results, as a bit which was transmitted as a '0' is interpreted as a '1'.

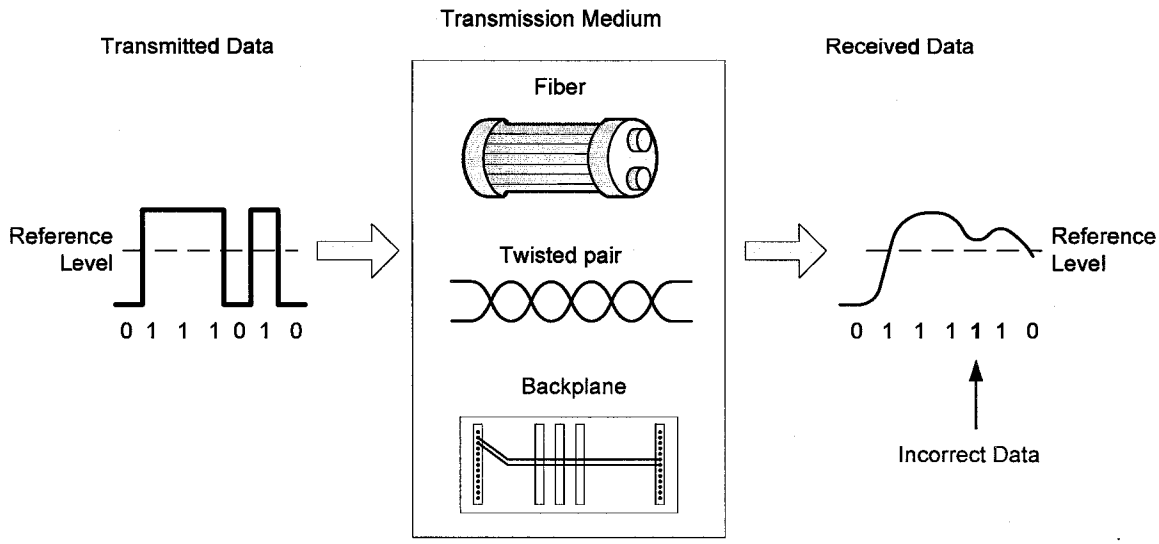


Figure 2 Example of ISI Causing a Bit-Error from [1]

2.2 Inter-Symbol Interference in Optical Fiber and Backplanes

Optical fiber and electrical backplanes are communication media that are used to transmit as fast as 40 Gb/s. As such, ISI is a limiting factor in achieving ever higher data rates and/or longer medium lengths. Although optical fiber uses light and backplanes are electrical, and thus the causes of distortion are different, electrical methods to counter the distortion are largely the same.

Single-mode fiber (SMF) and multi-mode fiber (MMF) are the two types of fiber used in telecommunications. Current approximations for 10 Gb/s transmission without dispersion compensation, are that SMF is limited to 80 km, and MMF (OM1 type) is limited to 26 m [1]. This limitation is not due to attenuation, but distortion. Distortion in fiber optics is caused by three types of dispersion: modal dispersion (MD), chromatic dispersion (CD), and polarization mode dispersion (PMD).

MD is the most problematic type of dispersion in MMF. In MMF, different modes of light travel at different speeds, and therefore arrive at the receiver at different times. MD does not occur in SMF as it takes more than one mode to occur. CD is due to optical fiber having different refractive indices for different wavelengths, and so different

spectral components travel at different speeds. PMD is caused by imperfections in the fiber; it occurs because SMF supports two perpendicular polarization planes. When imperfections or kinks occur in the fiber, phase shifting between the two polarizations will arise. CD and PMD are the main causes of distortion in SMF [1].

Transmission over copper backplanes involves many components and interfaces, as shown in Figure 3, with each one presenting potential signal integrity difficulties at high rates. At signal rates above 2 Gb/s, the skin effect of copper traces and dielectric loss dominates the frequency dependent losses, severely distorting the signal [4]. Additionally, open-ended vias at the linecard-backplane interfaces create reflections [5], further contributing to ISI. A further complication to the problem is that these characteristics can vary greatly from channel to channel, even within the same backplane.

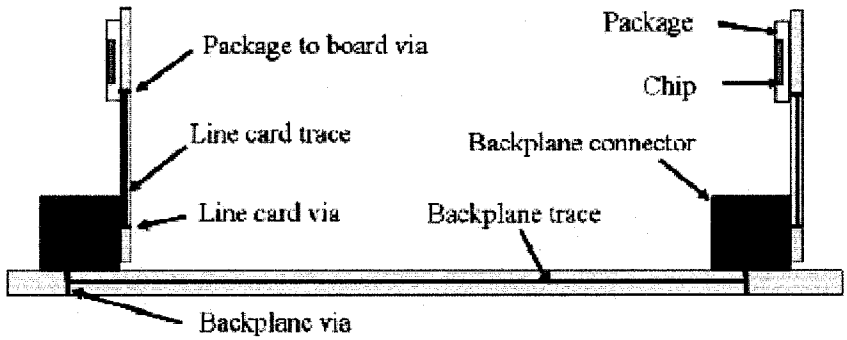


Figure 3 Typical Backplane from [3]

2.3 Equalization

In order to increase data rates over data networks while maintaining signal integrity, there are a few options available. The most obvious option is to simply upgrade channel media with improved versions. For example, replacing a 1 Gb/s backplane with a backplane having lower dielectric losses capable of operating at 5 Gb/s. This would prove to be very costly and disruptive, and would likely only be done as a last resort.

A more cost effective method would be to serially insert a component which has the inverse transfer function of the channel, effectively canceling the channel's ISI causing

characteristics. This is called equalization. One such method of equalization is to insert a component before or after the channel that has this channel inverting characteristic. In the case of optical fiber, this would consist of a dispersion compensation module (DCM). This is a serially connected component consisting of a long piece of fiber, a fiber Bragg grating, an etalon, or a virtually imaged phased array [7].

A much better equalization solution is electronic dispersion compensation (EDC). EDC allows for higher integration with existing circuitry (typically integrated on the receiver chip), allowing for a more compact and less expensive solution when compared to optical compensation [8]. The same EDC schemes are valid for both optical fiber and backplane compensation.

Figure 4 demonstrates the effect of equalization for a 10 Gb/s data rate. On the right-hand side, the lower curve shows the channel response for a legacy backplane (Tyco XAUI 34" backplane). For a 10 Gb/s NRZ data rate, the minimum bandwidth required is 5 GHz. The channel's frequency response shows attenuation as high as 35 dB within the signal bandwidth. In order to compensate for this ISI-causing response, a fractionally-spaced equalizer (FSE) at the receiver is used (ideal transversal filter, 50 ps tap spacing). The frequency response of the equalizer is shown as the top curve on the right-hand side; it approximates the inverse of the channel response. The middle curve shows the combination of the channel with the equalizer: the attenuation in the signal bandwidth has been greatly reduced. The left side of Figure 4 shows the impulse response of the channel, the impulse response of the equalizer, and the convolution of the two. The impulse response of the channel with equalizer shows an impulse (the desired response) delayed in time.

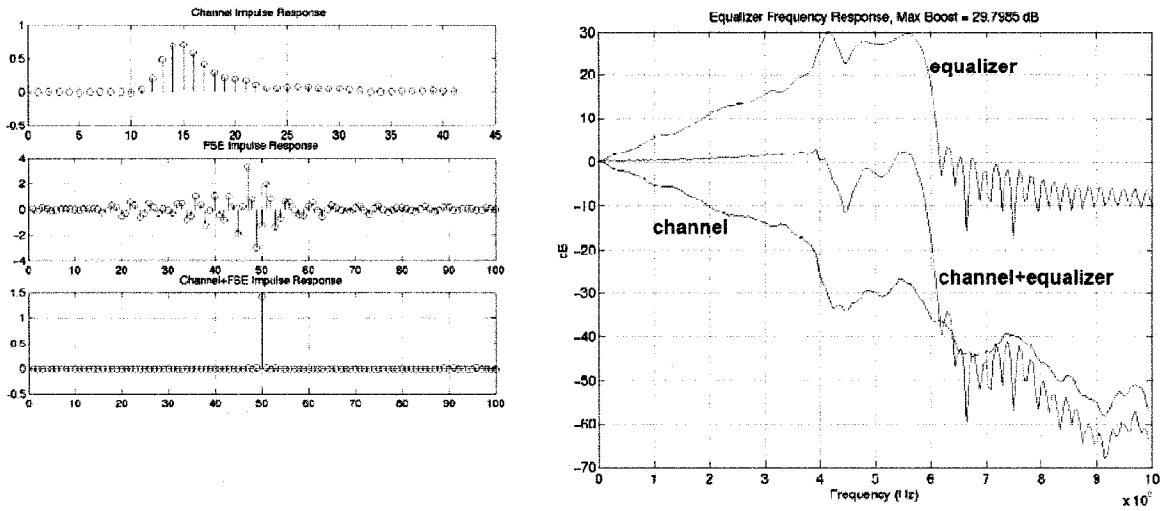


Figure 4 Example of 10 Gb/s Equalization from [6]

2.4 Types of EDC

EDC can be implemented either at the transmitter (commonly referred to as pre-emphasis), at the receiver, or at both. Whether at the transmitter or receiver, the general goal of equalizers is to emphasize high-frequency components and de-emphasize low-frequency components. Overall transfer functions are that of band-pass filters; this is due to bandwidth limitations of semiconductor devices as well as to avoid unwanted amplification of noise.

There are four main categories of electronic receiver equalizers: passive-component equalizers, active continuous-time equalizers using split-path amplifiers, active equalizers using discrete-time FIR filters, and active equalizers using continuous-time FIR filters [9]. Due to issues of bandwidth, adaptability, and speed-limited data conversion among the first 3 categories, the most commonly used type of receiver EDC for multi-Gb/s equalization is the continuous-time FIR filter (which can be combined with a discrete-time feedback FIR filter).

Figure 5 shows a continuous-time transversal FIR filter, commonly referred to as a feedforward equalizer (FFE). It consists of a tapped-delay-line having N taps, with each delay (τ) fixed to a fraction of the symbol period. On each tap of the delay line is a

multiplier, each having it's own multiplying coefficient (C_1 : C_N). The multiplier outputs are summed together to form the equalized output bit stream.

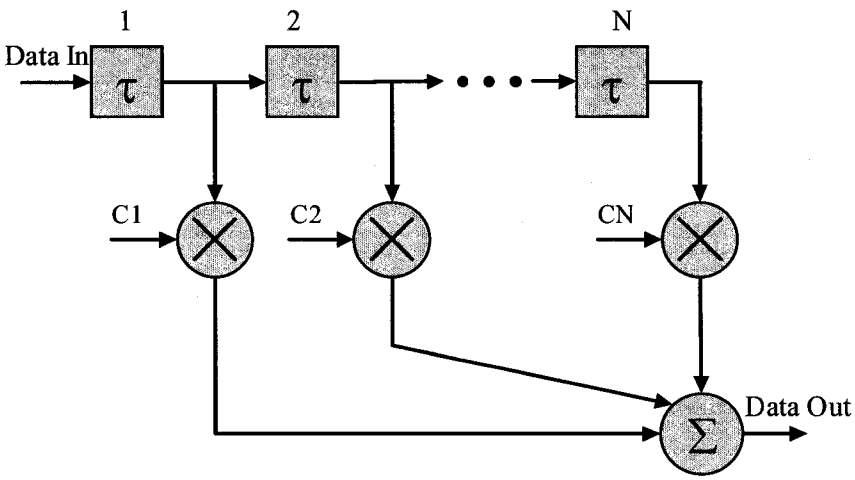


Figure 5 Transversal Feedforward Equalizer Block Diagram

Figure 6 shows a continuous-time traveling-wave (TWA)-FIR filter, another type of FFE. It has a similar structure to the transversal filter, but has delays on both sides of the multipliers. The principle behind it is similar to a distributed amplifier in that capacitances are distributed rather than lumped in order to reduce the loading on multipliers - this allows for higher bandwidths. It should be noted that the tap spacing in a TWA filter is made up of two delay cells, rather than one as in a transversal filter. Although transversal filters and traveling-wave filters are different structures, they still perform the same function in terms of linear equalization.

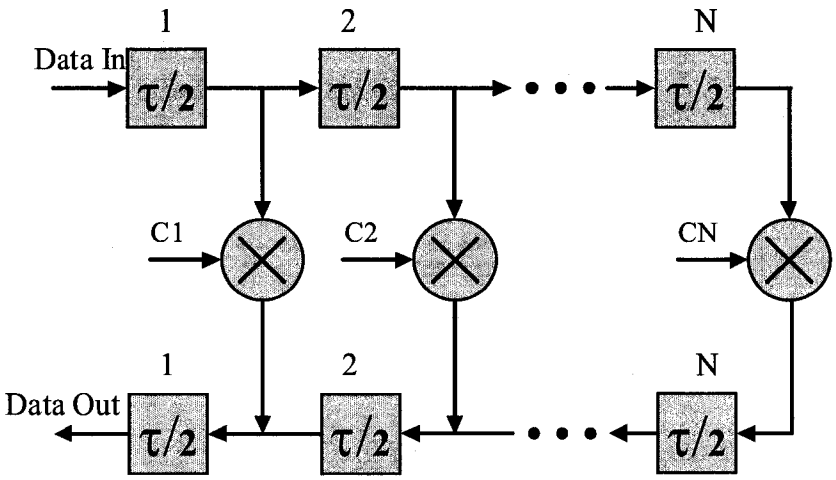


Figure 6 Travelling-Wave Feedforward Equalizer Block Diagram

The structure of a decision-feedback equalizer (DFE) is shown in Figure 7. It consists of a slicer (the decision-making device) and a feedback FIR, which is sometimes referred to as a feedback equalizer (FBE). The principle behind the DFE is that once the current symbol's value has been deciphered (high or low), the ISI contribution of that symbol can be removed from future symbols with feedback. This portion of the ISI that is removed by the non-linear feedback is called post-cursor ISI, and is the tail section of the spread-pulse, as shown in Figure 8. The input to the feedback FIR is a limited signal (the slicer output), but the delay cells can either be analog delays, or clocked digital delays where the clock is provided by a later stage, the clock and data recovery (CDR) circuit.

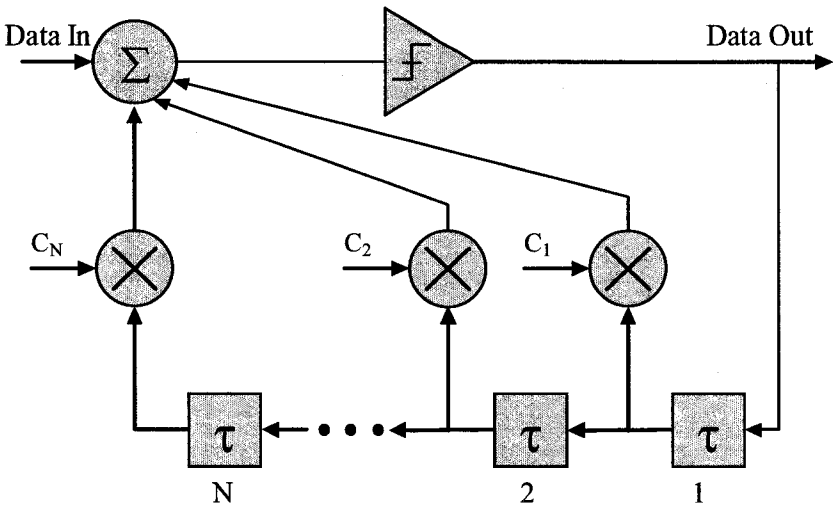


Figure 7 Decision-Feedback Equalizer Block Diagram

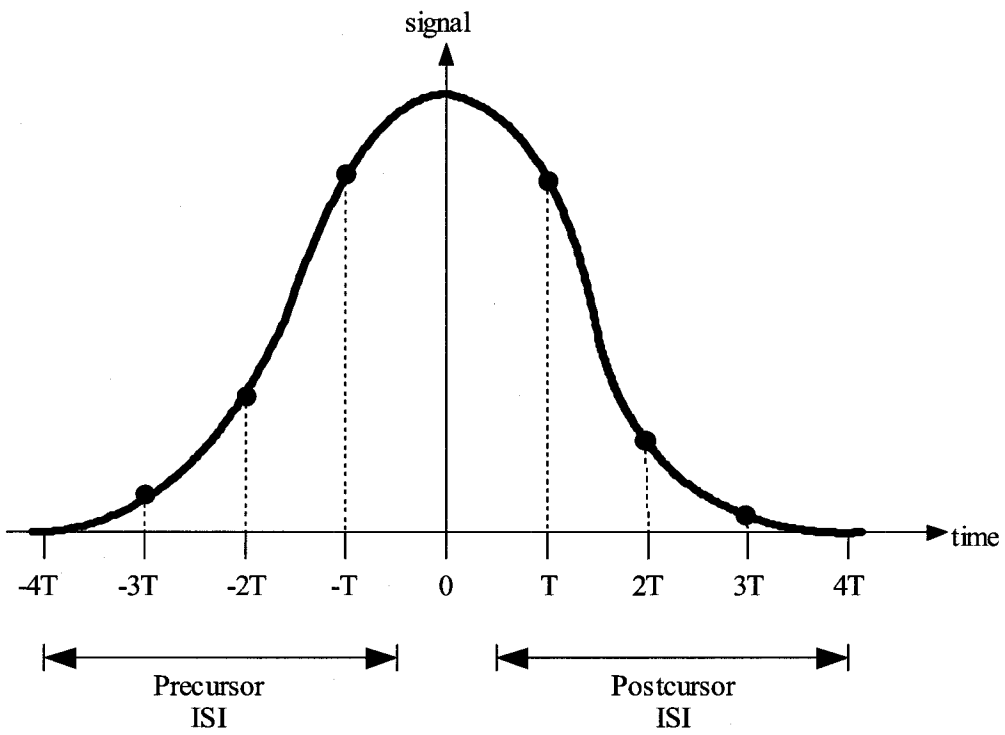


Figure 8 Pulse Spreading: Precursor and Postcursor ISI

2.5 Comparison of FFE to DFE

FFE and DFE serve to accomplish the same function – to remove ISI from a serial bit stream to achieve an acceptable BER. However, there are some fundamental differences between them. The choice of which to use is typically a matter of channel characteristics and system specifications. A summary of the following discussion is presented in Table 1.

Given enough taps, an FFE can approximate any linear transfer function [8]. Channel transfer functions can contain deep nulls at particular frequencies; if these nulls are not equalized, data at these frequencies can be unrecoverable [14]. Due to practical limitations on FFE filter length, it can be difficult for FFE to compensate these nulls. DFE is able to equalize nulls by using past decisions; a combination of feedback and nonlinearity makes DFE superior to FFE for equalization of the deep nulls, when compared to typical FFE filter lengths. Another benefit of DFE is that because of the slicer, its feedback does not add noise; FFE does add noise.

The nonlinearity and feedback makes the analysis of DFE much more complicated; FFE is inherently stable, whereas DFE can become unstable. When an incorrect decision is made in DFE, this error will be fed back and can cause error propagation. Errors in FFE do not propagate. ISI coverage in DFE is much more limited than FFE; it can only cancel post-cursor ISI, and the amount of coverage is limited due to a limitation in the number of feedback taps [10]. For example, of the ISI shown in Figure 8, a DFE may only be able to cancel the ISI at T or 2T. The entire precursor ISI and the rest of the postcursor ISI would have to be cancelled by another method. FFE can cancel both precursor and postcursor ISI, and its coverage is only limited by the number of taps. This is why DFE is most often preceded by FFE.

Table 1 Comparison of FFE and DFE

Characteristic	**FFE**	**DFE**
Linearity	Linear	Nonlinear
ISI Coverage	Precursor and Postcursor	Postcursor Only (limited)
Decision Errors	No Propagation	Errors Propagate
Noise	Adds Noise	No Added Noise

2.6 FFE Tapped-Delay-Lines and Delay Cells

The main architectural parameters of FFE tapped-delay-lines are the tap-spacing (the delay between taps) and the number of taps. The product of these two gives the total delay across a tapped-delay-line, which is equal to the total amount of ISI coverage of the equalizer. The choice of these parameters depends upon the specifications of the channel and the system, as well as the technological limitations.

The number of taps determines the granularity of the FFE transfer function; therefore, if a channel response has deep nulls in it more FFE taps would be needed to compensate the nulls. Tap-spacing can be at the symbol rate or at a fraction of the symbol period. Although symbol period tap-spacing will give more ISI coverage for the same number of taps, it is susceptible to phase variation in the sampling clock [24]. Smaller tap-spacing also has the benefit of adding more filtering granularity within a single symbol period; this allows the equalizer to remove horizontal jitter as well as opening the eye vertically. Therefore, if there is a lot of horizontal jitter in the eye diagram of the received signal, smaller tap-spacing may be needed.

Although a large number of FIR taps would be optimal, there are limitations due to parasitic capacitance, power consumption, and bandwidth across the tapped-delay-line. Tap-spacing is also limited due to a tradeoff between delay and bandwidth; typically, it is much easier to meet bandwidth requirements with a smaller tap-spacing.

The main function of delay cells used in tapped-delay-lines for FFE is to provide a constant group delay and amplitude within the signal bandwidth. A major design challenge for FFE delay cells is to achieve a large delay-bandwidth product, not only across a single delay cell, but across an entire tapped-delay-line. As delay cells are cascaded, the overall group delay is additive with each successive stage, however the overall bandwidth drops due to the transfer function roll-off. Delay cells with higher order roll-offs maintain more bandwidth when cascaded; the limit of this principle would be a cell exhibiting a "brick wall" low-pass filter transfer function, i.e. a cell with an infinite number of incidental poles at the cut-off frequency. Such a delay cell would have no loss of bandwidth with successive stages. Due to technological constraints,

such a delay cell is not physically possible, and thus there are limitations to how long an FIR filter can be made.

Another desirable property of FIR delay cells is to have no signal attenuation (or gain) and no peaking (peaking can lead to saturation across cascaded stages, or at multiplier outputs). Ideally, the input to each tap multiplier would be identical across taps, but simply delayed in time. The unavoidable presence of attenuation is one of the disadvantages of passive delay cells, and can be a limiting factor to FIR filter length in addition to the bandwidth limitation. It is also beneficial to have the same DC bias at the output of the delay cell as at the input; as these nodes are the multiplier inputs, it allows for each multiplier across the filter to have the same performance.

Due to variations in process, voltage, and temperature, it is also desirable to allow for some degree of delay cell tuning. This would typically be done with feedback control loops to tune measures of group delay, bandwidth, and gain/attenuation/peaking. Other properties typical of analog circuitry also apply such as linearity, low power, small area, and low noise.

Delay cells implemented in tapped-delay-lines for FFE can consist of passive elements, active elements, or a combination of the two. Passive delay cells are implemented as transmission lines [12], or more commonly as lumped LC ladders (artificial transmission lines) [4][5][11][13][14][15][16][17]. Active delay cells have been implemented as a current-mode two-integrator-loop biquad [18], an inverter-based delay with active-inductor [19], a modified Cherry-Hooper architecture [20], a two-pole Butterworth filter [21], and as cascaded emitter followers [22]. A combination of active and passive (defined as containing transistors and inductors) is presented in [23] as a lumped LC ladder delay followed by an active buffer.

The biggest difference between passive delay cells and active delay cells is a tradeoff between power consumption and circuit area. Passive delay cells are commonly implemented as LC ladders, which are much smaller in area than actual transmission lines, but due to the inductors, they are typically much larger than active delay cells.

However, active delay cells consume power, whereas passive delays do not (except for very small leakage currents). Another benefit of active delay cells is that they can be designed to have no signal attenuation, and to have the same DC level at the output as at the input. An all-passive solution will always attenuate the signal somewhat and have varying DC levels, a problem that grows with an increased number of taps.

2.7 Conclusions

This chapter presented background information on inter-symbol interference and the EDC that is used to help cancel it. Two basic architectures of receiver equalizers were discussed: FFE and DFE. Comparisons of the two types were made, outlining the advantages and disadvantages of each, including differences of ISI coverage, linearity, noise, and error propagation. It was found that by implementing FFE followed by DFE, advantages of both can be utilized.

The final section of the chapter focused specifically on delay cells used for FFE, as this is the topic of this thesis. Tradeoffs that are common to delay cell design were discussed, and specific architectures from literature were cited. It was found that there are two broad divisions of FFE delay cell architectures: passive (low power consumption, but large silicon area) and active (small silicon area, but high power consumption). The delay cell in [23] used a combination of both active and passive components. However, due to its implementation, it is assumed that this cell likely had high power consumption and large silicon area (the values were not provided in the paper).

A novel delay cell architecture is presented in the following chapter, and it is the focus of this thesis. This delay cell uses a combination of active and passive elements to achieve an area typical of an active solution, but with reduced power consumption.

Chapter 3 Active Delay Cell with Shunt and Series Inductive Peaking

3.1 Delay Cell Structure

Shown in Figure 9 is a schematic of the active delay cell with shunt and series inductive peaking. It consists of an NMOS differential pair (M1/M2), current source (M3), resistive load (R_L), shunt inductors (L_1), and series inductors (L_2). To account for variations in process, voltage, and temperature, additional devices were added to make the delay cell tunable. Varactors (C) were added to account for a large portion of the delay, but also to account for variations in inductance and parasitic capacitance in the cell. PMOS devices (M4/M5) operating in the linear region were added in parallel with the poly silicon resistive loads to account for variations in sheet resistance. A third tunable mechanism in the delay cell is tuning of the current source (M3) for variations in the transconductors (M1/M2).

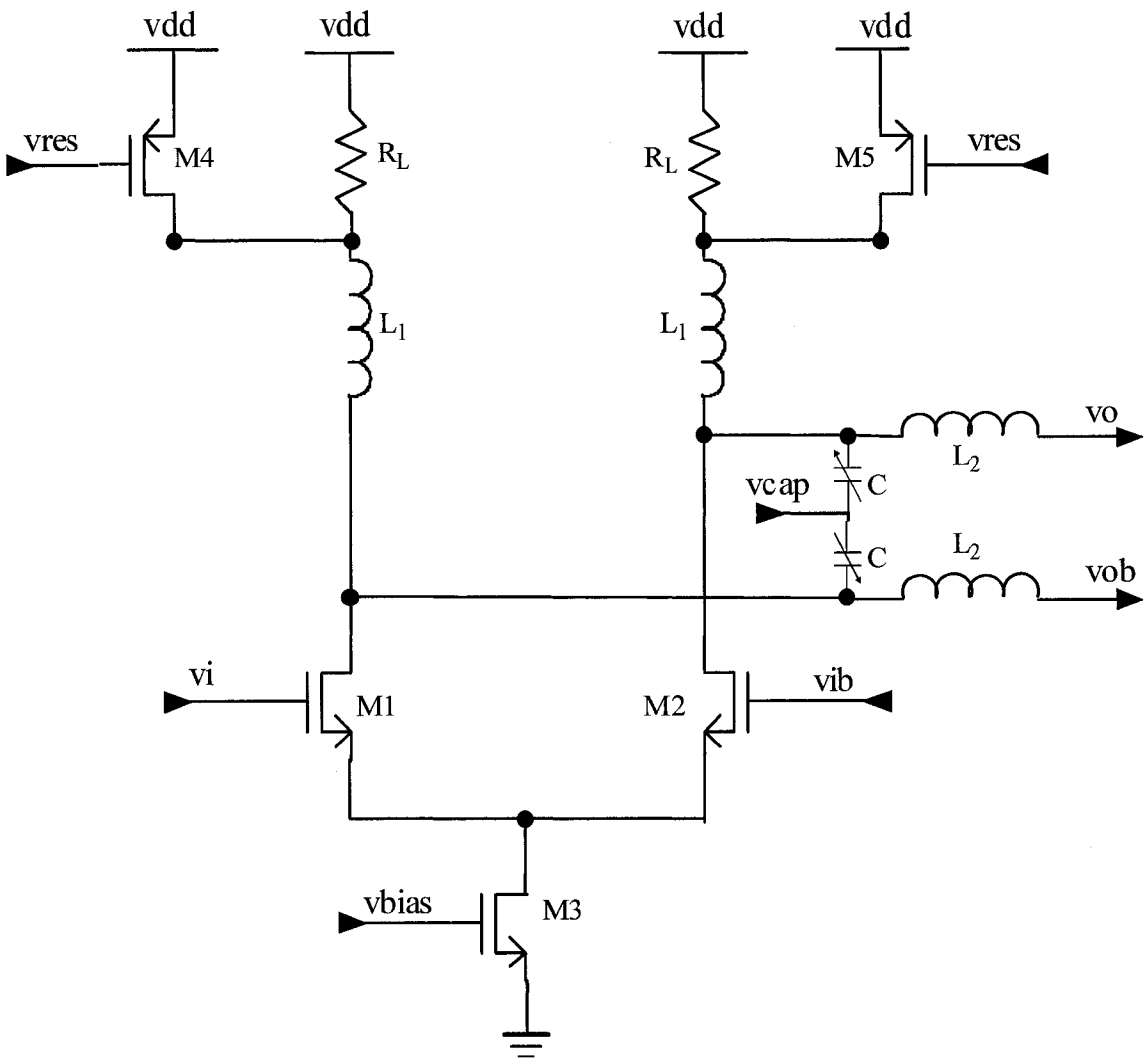


Figure 9 Delay Cell Schematic

A similar architecture was presented in [25], but for use as a cascaded amplifier rather than as a tapped-delay-line. Architecturally, it was slightly different in that it did not have the varactors or the PMOS resistors that the delay cell possesses. Another difference is that it was designed as an alternative to a distributed amplifier – it is designed for gain, is without specifications on group delay, and doesn't have taps between stages (FIR multipliers).

3.2 General Characteristics of Delay Cell

The delay cell uses a combination of active circuitry and passive devices. By using active circuitry, the delay cell is designed to have no signal attenuation, and to have the same DC bias on the output as on the input. The addition of L_1 (to the basic differential pair with resistive load) decreases the delay, but has a greater effect in its increase of bandwidth for an overall gain in the delay-bandwidth product. The delay-bandwidth product is further increased with the addition of L_2; adding this series inductance has no effect on delay (other than parasitic effects), but greatly adds to the bandwidth.

To achieve the cell's small silicon area, stacked inductors are used for both L_1 and L_2. By using 3-dimensional inductors, the inductance per silicon area is greatly increased when compared to planar inductors, due to the increased mutual inductance. To decrease the parasitic capacitance and further reduce inductor area, narrow metal traces are used for the inductor windings. This causes series resistance through the inductors to increase when compared to conventional winding widths in high-Q planar inductors. However, this resistance is of little consequence in the delay cell; for the case of the shunt inductors (L_1), this resistance simply becomes part of the load resistance, and for the series inductors (L_2) it slightly adds to the overall delay and helps prevent peaking in the delay cell's transfer function.

When these delay cells are cascaded to form a tapped-delay-line, a high percentage of the delay cell's bandwidth is maintained, making it suitable for the design of a very long FIR filter. This is due to the series inductance (L_2) which extends the bandwidth beyond what would be provided by the shunt inductance (L_1) alone.

3.3 Delay Cell Analysis

Shown in Figure 10 is a simplified small-signal model of the delay cell. The model is a single-ended equivalent circuit. The differential pair is represented as a transconductor (voltage-controlled current source). The load resistor R includes resistances from the poly silicon load resistors (R_L), the drain-source resistance of the linear PMOS transistors (M4/M5), and the parasitic resistance of the shunt inductors (L_1). The parasitic resistance

of the series inductors (L_2) has been added as a separate component, R_{L2}. Capacitance C_1 is an approximated component consisting of the varactor capacitance (C), the transconductor parasitic drain capacitance, L_1 parasitic capacitance, R_L parasitic capacitance, M4/M5 parasitic capacitance, approximately half of the L_2 capacitance, and the metal interconnect parasitic capacitance. Similarly, the Capacitance C_2 includes the other half of the L_2 capacitance, and the load capacitance. When used as an FIR tapped-delay-line, this load capacitance would include the input capacitance of the next stage delay cell, the input capacitance of the multiplier, and the parasitic capacitance of the metal interconnect.

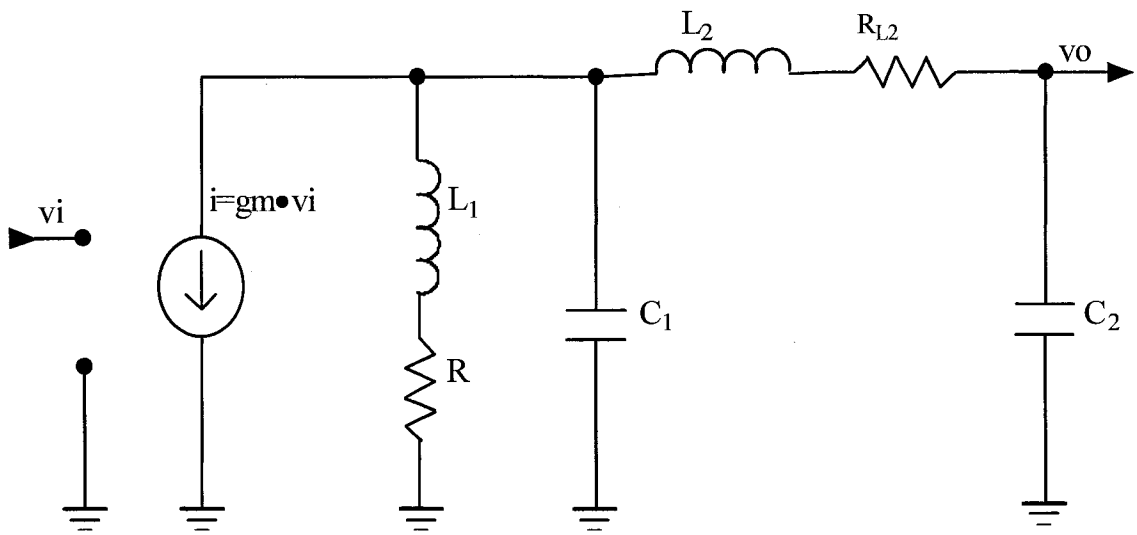


Figure 10 Simplified Small-Signal Model of Delay Cell

The transfer function of the simplified small-signal model is shown as (1); it contains four poles and one zero. Deriving the phase response from this equation results in (2). To find the group delay of the delay cell, the derivative of the phase response is taken with respect to frequency, as shown in (3).

$$\phi(\omega) = \tan^{-1}\frac{\omega L_1}{R} - \tan^{-1}\frac{\omega D - \omega^3 B}{\omega^4 A - \omega^2 C + 1} \tag{1}$$

$$\frac{v_o}{v_i}(\omega) = \frac{gm(R + j\omega L_1)}{[\omega^4 A - j\omega^3 B - \omega^2 C + j\omega D + 1]} \tag{2}$$

$$GroupDelay(\omega) = -\frac{\partial\phi}{\partial\omega} = \frac{-L_1/R}{1+(\omega L_1/R)^2} + \frac{1}{1+\left[\frac{\omega D - \omega^3 B}{\omega^4 A - \omega^2 C + 1}\right]^2} \bullet \left[\frac{(\omega^4 A - \omega^2 C + 1)(D - 3\omega^2 B)(4\omega^3 A - 2\omega C)}{(\omega^4 A - \omega^2 C + 1)^2}\right] \tag{3}$$

Where:

- $A=L_1L_2C_1C_2$
- $B=C_1C_2(L_2R+L_1R_{L2})$
- $C=L_2C_2+RR_{L2}C_1C_2+L_1(C_1+C_2)$
- $D=R_{L2}C_2+R(C_1+C_2)$

3.4 Delay Cell Design

Although the equations of the previous section may be interesting from an analysis perspective, they are not very useful when it comes to design. However, the small-signal model of Figure 10 is useful for design with some approximated equations. Although many design iterations are required to meet specifications, the steps outlined in the remainder of this section provide a very good starting point.

The most significant attributes to initially design for are unity-voltage gain, group delay, and bandwidth. To design for unity-gain, the DC voltage gain is first determined by (4). This equation allows one to choose the overall resistance (R), as well as the tail current and sizing of the differential pair.

$$A_V = g_m \cdot R = 1 \tag{4}$$

To design for the desired group delay, a simplification of (3) can be made. Realizing that one of the design goals for the delay cell is to have constant group delay within the signal bandwidth, the group delay across all frequencies of interest should be made approximately equal to that as when frequency approaches zero, resulting in (5).

$$GroupDelay(0) = R(C_1 + C_2) + R_{L2}C_2 - \frac{L_1}{R} \tag{5}$$

Due to the analysis relating R, C, and L of inductively shunt-peaked amplifiers in [26], this equation can be further simplified by realizing that a maximally flat frequency response is desired (a response without amplitude peaking). Defined in [26] is a factor m relating RC and L/R time constants; this factor is specified to have a value set to 2.41 for the maximally flat condition. Applying this factor to the model of Figure 10 results in (6). Simplifying further, it can be assumed that C_1=C_2= ½·C_{total} and that R>>R_{L2}; combining these assumptions with (5) and (6) results in (7). From this equation, the total capacitance (varactor plus parasitic capacitance) is determined, and therefore the value of L_1 can be calculated as well.

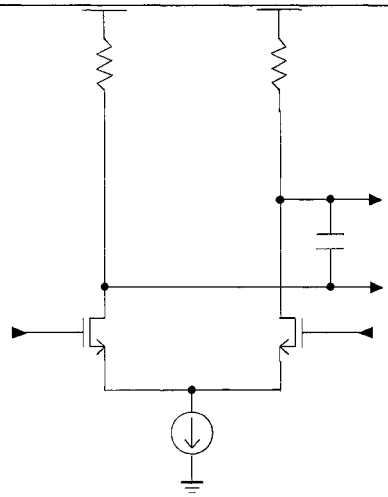
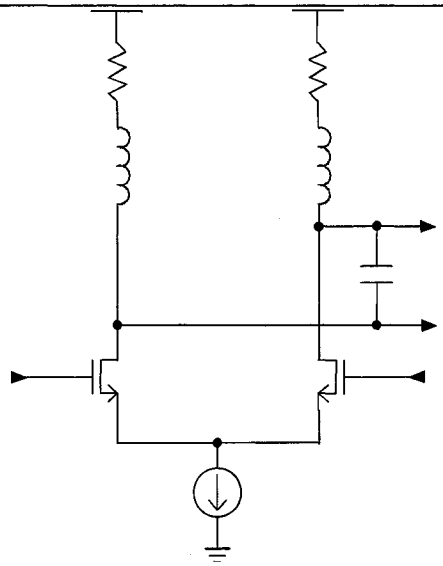
$$m = \frac{R \cdot (C_1 + C_2)}{L_1 / R} = 2.41 \tag{6}$$

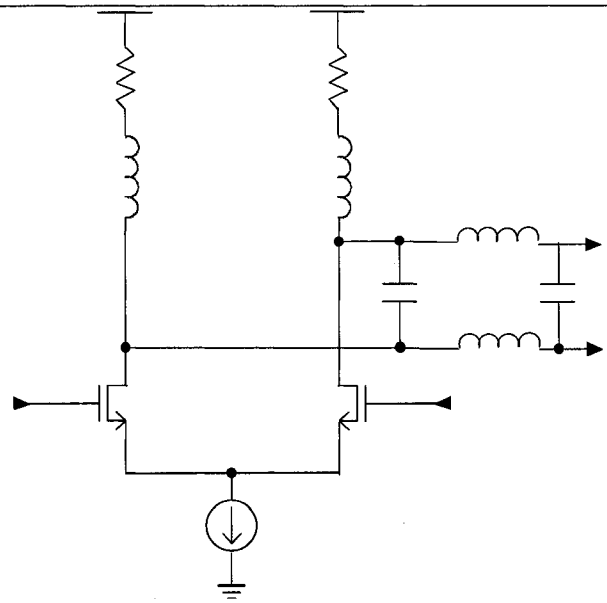
$$Delay = 0.58R \cdot C_{total} \tag{7}$$

After designing for unity-gain and the desired delay, the series inductor (L_2) can be sized to extend the delay cell's bandwidth. Table 2 shows the bandwidth improvement over a resistively loaded differential pair due to adding shunt peaking, and adding series and shunt peaking. In the case of an FIR with T/3 tap spacing, the bandwidth requirement of a single tap would be met without the addition of the series inductor; however, this requirement would not be met across the entire tapped-delay-line. The addition of L_2 is mainly to allow for the cascading of cells. Adding L_2 does not affect gain or delay at low

to mid frequencies (other than parasitic effects), but it does have an effect at high frequencies where its poles lie. If L_2 is sized too large, there will be peaking in the gain response; sizing it slightly smaller (but still too large) could result in no peaking of the gain response, but causes unacceptable peaking in the delay response. If it is sized too small, the result could be that its effect occurs at too high a frequency, and overall bandwidth is too low.

Table 2 Bandwidth Comparison of Inductively Peaked Circuits

Circuit Description	Schematic	Bandwidth Improvement Factor
Diff. Pair with: Resistive Load		1
Diff. Pair with: Resistive Load Shunt Peaking		1.72 (for m = 2.41)

Diff. Pair with: Resistive Load Shunt Peaking Series Peaking		3 – 5 (for no gain peaking, delay peaking less than 10 % within signal BW)

To properly size L_2, the entire tapped-delay-line should be simulated to measure the overall bandwidth. The best approach is simply to use simulation to sweep the size of L_2 to find the point at which: the bandwidth requirement is met, there is no peaking in the gain response, and peaking in the delay response is within specifications.

The addition of L_2 will typically mean that L_1 will have to decrease in size. Although most of the L_2 effect is at higher frequencies, at the L_1 zero it will already have a resonating effect on C_2, causing a smaller overall capacitance to be seen by the load resistor. Therefore in order to maintain the RC to L/R time constant ratios for the maximally flat condition, L_1 must be reduced.

3.5 Stacked-Inductor Design

Once inductor sizes have been determined through simulation, their physical design and corresponding equivalent models can be determined. For this project, the CAD tool ASITIC (Analysis and Simulation of Spiral Inductors and Transformers for Integrated Circuits) was used to design and model the inductors. ASITIC uses a technology file to describe the substrate, oxide, and interconnect layers of a specific process, and models the magnetic and electrical interaction of passive devices in the process.

Designing a stacked-inductor in ASITIC is an iterative process. In order to optimize tradeoffs between area, capacitance, and series resistance, one can vary the number of stacked metals, the inductor's width, the metal track width, the number of turns, and the spacing between turns. For a given inductance value, increasing the number of metals will result in more mutual inductance and therefore smaller area, but will increase resistance. Increasing the inductor's track width will decrease resistance, but will increase area and capacitance. Increasing the number of turns increases mutual inductance, and therefore smaller area, but will increase capacitance (due to the smaller opening at the inductor's center). For this particular application, capacitance and area were minimized at the expense of slightly higher resistance. Low capacitance was desirable as it then allows for a larger tuning varactor, and designing for a small overall delay cell area was one of the goals of the design.

Once the layout of an inductor is created, ASITIC will create a PI model of the inductor, as shown in Figure 11. However, this model is only valid for a particular frequency. In order to create a unified broadband model, many of these PI models are generated for different frequencies. These models are then reconstructed in Cadence, and through Spectre's S-Parameter Analysis, the S-parameters (S_{11}, S_{12}, S_{21}, S_{22}) are found for each. These S-parameters are then imported into HSPICE, and using the bisection optimization capabilities of HSPICE, these S-parameters are curve-fitted into a broadband model [27], as shown in Figure 12. This broadband model can then be re-created in schematics, to be simulated with the delay cell. The layout can be exported in CIF format from ASITIC, and imported into Cadence.

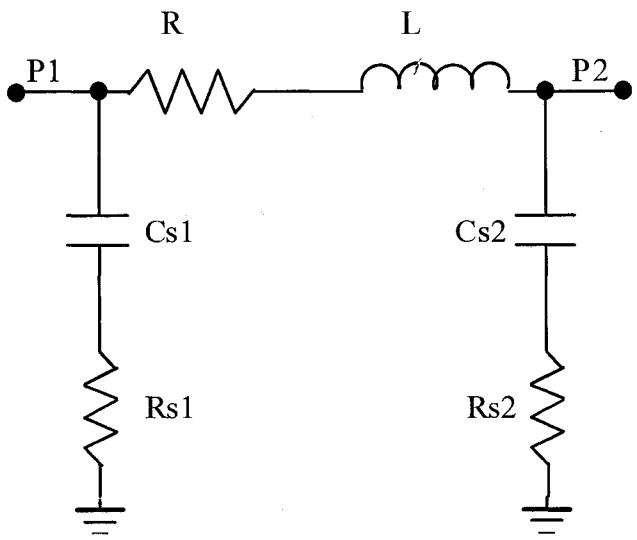


Figure 11 ASITIC Inductor Model

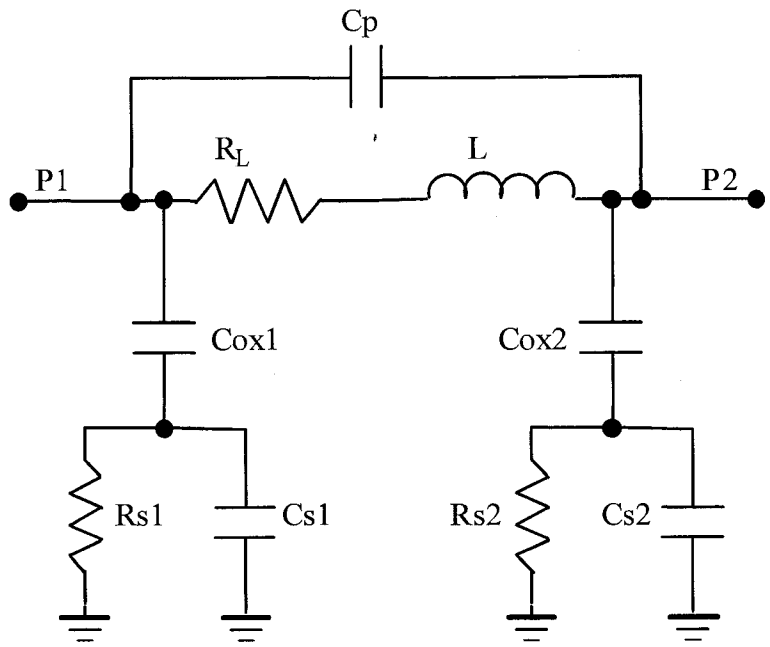


Figure 12 Broadband Inductor Model

3.6 Conclusions

The proposed delay cell has a relatively simple architecture, and is easily modified to allow for tuning to counteract variations of process, voltage, and temperature. The ability to tune the delay cell's current, resistance, and capacitance allows for specifications of gain, bandwidth, and group delay to be met in a real-world environment. This chapter presented a small-signal analysis, which with certain simplifications and assumptions, led to design equations and steps suitable for a first design iteration.

It was shown that the use of peaking inductors in the delay cell greatly improves the delay-bandwidth product when compared to an ordinary differential pair with resistor load. The architecture allows for low-Q inductors, thus permitting the use of compact stacked-inductors having large inductance per unit area. Significant power savings are realized by using such inductors as they allow for larger resistors to be used (and therefore less current), while still achieving bandwidth targets.

Chapter 4 Prototype Design: Tapped-Delay-Line

To demonstrate the performance of the active delay cell with shunt and series inductive peaking, a prototype was built. This chapter describes the core circuitry of the prototype: the delay cell and tapped-delay-line. The following chapter describes the top-level design: the additional circuitry required to facilitate testing of the delay cell and tapped-delay-line.

4.1 Tapped-Delay-Line Specifications

The specifications for the delay cell and tapped-delay-line used on the testchip are summarized in Table 3. The delay-line was designed for a data rate of 40 Gb/s, and having 18 taps with T/3 spacing.

Table 3 Tapped-Delay-Line Specifications

Specification	Delay Cell	Tapped-Delay Line
Data Rate	40 Gb/s	40 Gb/s
Number of Taps		18
Tap Spacing	T/3	T/3
Power Supply	1.2 V	1.2 V
Area	Minimize	Minimize
DC Gain	0 ± 0.1 dB	0 ± 2 dB
Peaking	none	none
Bandwidth		> 20 GHz
Min/Max Group Delay (0-20 GHz)	7.50 / 9.16 ps (8.33 ps ± 10%)	135 / 165 ps (150 ps ± 10%)
Linearity (1-dB Comp. @ 20 GHz)		100 mV $_{0\text{-pk, diff}}$

4.2 Tapped-Delay-Line Design

To demonstrate the performance of the tapped-delay-line, a testchip was designed in the IBM 8RF-DM process. This is a high-speed RF 0.13 μm CMOS process with 8 layers of metal interconnect. Although this is an RF process, the three specialized upper metals were not used for the tapped-delay-line layout, and thus the results would be applicable to a standard CMOS logic process.

An 18-tap delay-line was designed using the simulation setup shown in Figure 13. It was designed for a data rate of 40 Gb/s with each delay having T/3 spacing, where T is the bit period. Therefore, each delay (τ) was designed to have a nominal delay of 8.33 ps. As the application of such a delay-line is an FIR filter, a load was connected to each tap to represent that of a multiplier. This load is a differential pair with resistor load, as shown in Figure 14 (an explanation of the switches current source is given in Chapter 5). An extra delay cell is added after the 18th stage so as to give the final tap the same load to the other stages.

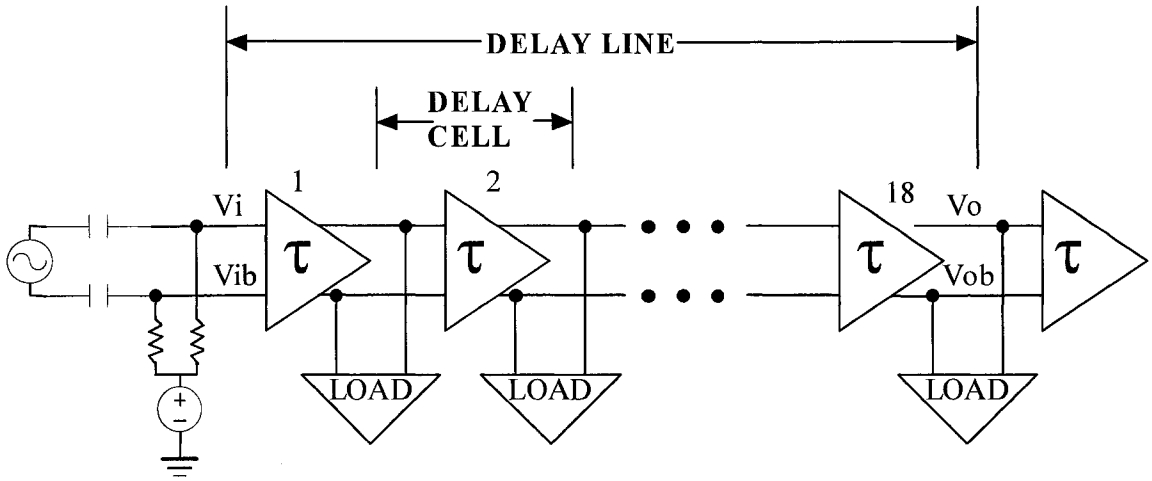


Figure 13 Block Diagram of Tapped-Delay-Line Design Setup

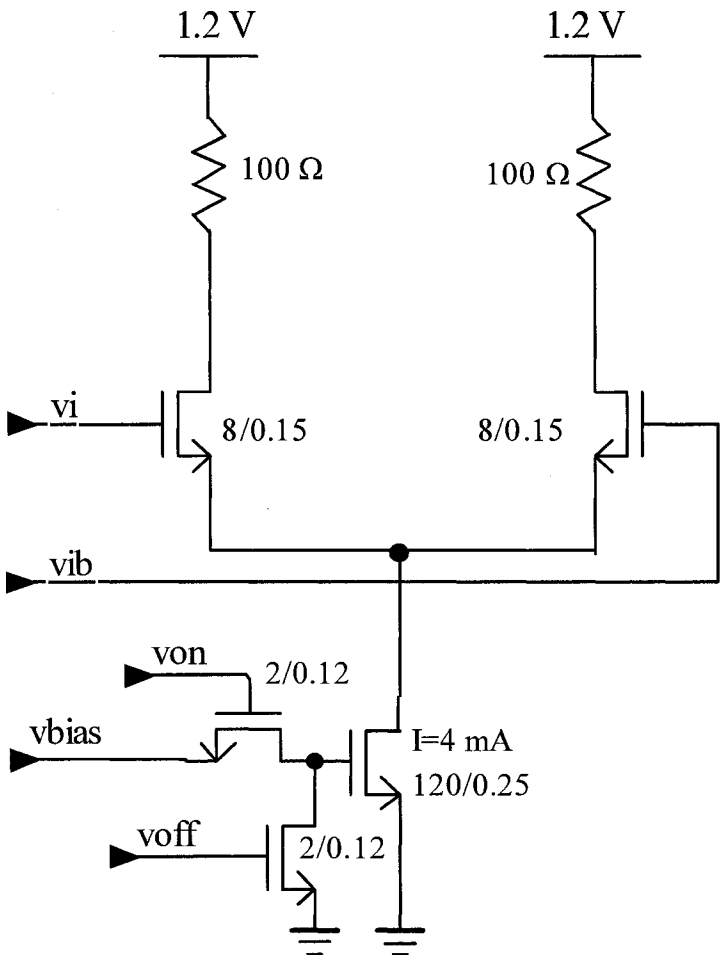


Figure 14 Schematic of Load at Each Tap

A schematic of the final delay cell with device sizes is shown in Figure 15. Due to their significance to the design, the stacked-inductors' parasitic resistor values are drawn here in the schematic; however, for actual simulations each inductor is represented as a PI circuit as was shown in Figure 12. Due to time constraints, the delay cell was designed for identical L_1 and L_2 inductors. Further optimization may have been possible. The total load resistance, including poly silicon resistors, PMOS devices, and L_1 resistance is 60 Ω. Delay cell inputs (vi/vib) and outputs (vo/vob) have a DC voltage of 1.0 V in nominal conditions. Tuning voltages vres, vcap, and vbias are nominally set to 0.5 V, 0.95 V, and 0.32 V (vbias is set by a current mirror). The delay cell draws a current of 6.66 mA from a 1.2 V supply, for a power consumption of 7.99 mW.

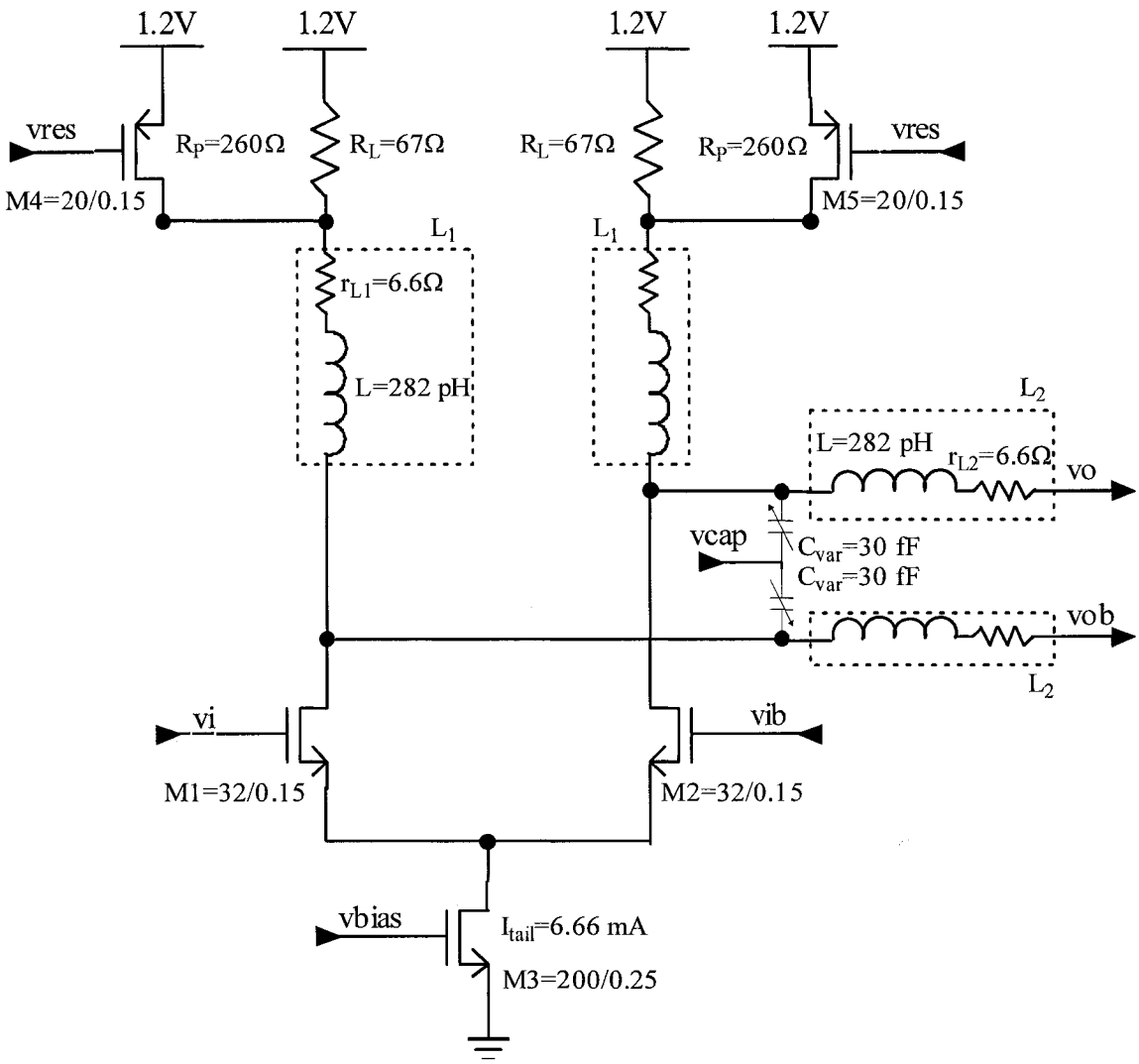


Figure 15 Schematic of Delay Cell

The annotated layout of the delay cell is shown in Figure 16. The layout occupies an area of 58.6 μm x 53.3 μm. The signal path is left to right (inputs on left, outputs on right), and the layout is completely symmetrical across the x-axis to minimize offsets.

Inductors L_1 and L_2 (identical) are 4-metal stacked-inductors composed of metals 2 to 5. The outer dimensions are 13.5 μm x 13.5 μm. The metal track widths are 1.9 μm, with 0.6 μm spacing. By using 4 layers with 1.5 turns/layer, the amount of interconnect capacitance was minimized due to the locations of the inductors' ports. For example, interconnect lengths from M1/M2 to L_1, L_1 to R_L, L_1 to L_2, and L_2 to the output were all

minimized due to the inductors' port locations.

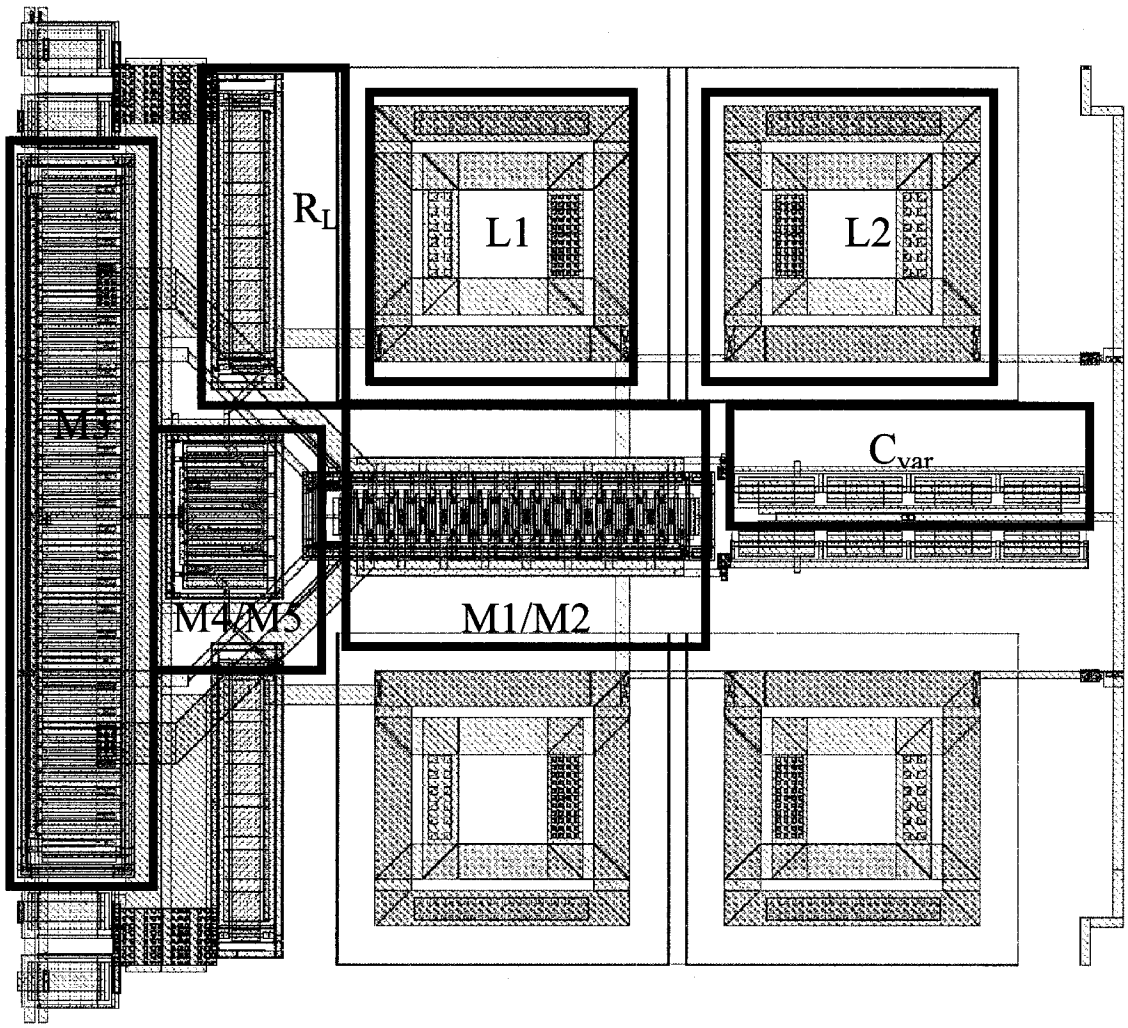


Figure 16 Delay Cell Layout (annotated devices)

4.3 Simulation Results

The following simulation results are based upon the setup of Figure 13. Simulated results for an individual cell are measured from the 2nd delay cell in the tapped-delay-line. All simulations use post-layout netlists containing extracted parasitic capacitances and diffusions.

4.3.1 Amplitude Response

Shown in Figure 17 is a plot of amplitude versus frequency for both the delay cell and the 18-tap delay-line. The low-frequency gain of the delay cell is 0.07 dB; for the delay-line it is 1.23 dB. The bandwidth of the delay cell is 59.6 GHz; for the delay-line it is 24.2 GHz, thereby exceeding the minimum specification of 20 GHz for a 40 Gb/s data rate. The effect of the series inductor (L_2) on bandwidth can be seen in this plot. Without this device, the transfer function roll-off of the single delay cell would occur at around 25 GHz; the peaking effect of this inductor can be seen as the bump at 45 GHz, thereby allowing the delay-line to maintain sufficient bandwidth across its length.

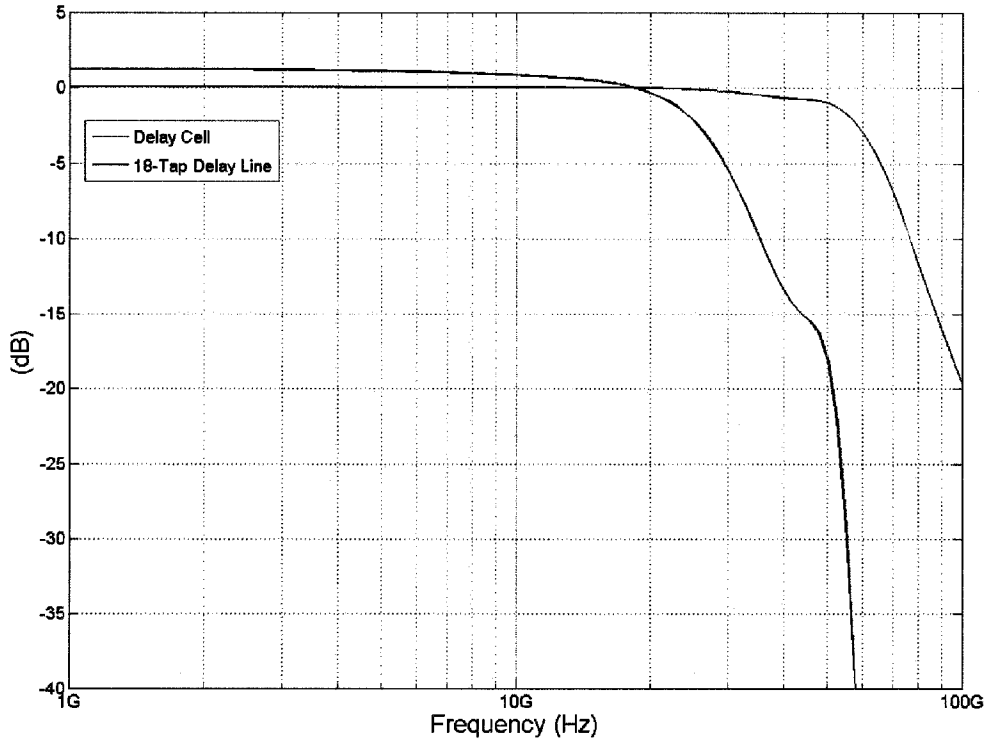


Figure 17 Simulated Amplitude Response of Delay Cell and Delay Line

4.3.2 Delay Response

The simulated delay response of the delay cell and delay-line are shown in Figure 18. Within the signal bandwidth of 20 GHz, the delay of the delay cell is well within specifications, varying between 8.19 ps and 8.52 ps. The delay of the delay-line is simply 18 times the value of the individual cell. The effects of both L_1 and L_2 can be seen here; L_1 causes delay peaking at around 28 GHz, and L_2 at around 55 GHz (note that both peaks are outside of the signal bandwidth).

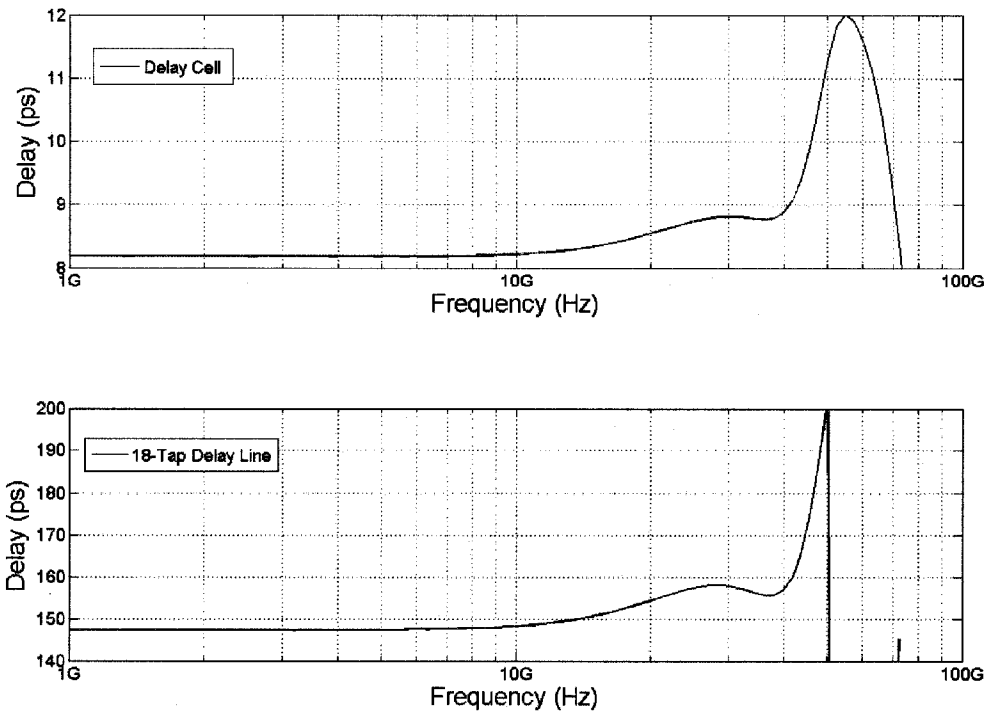


Figure 18 Simulated Delay Response of Delay Cell and Delay Line

4.3.3 DC Offsets

DC offsets were simulated using Monte Carlo analysis with device mismatch models provided by IBM. Of 47 such simulations, the average input referred DC offset of the delay cell was found to be 4.34 mV, and 9.55 mV for the 18-tap delay line. A graphical representation of these results is shown in Figure 19, and the average, maximum, and standard deviation of the results are shown in Table 4.

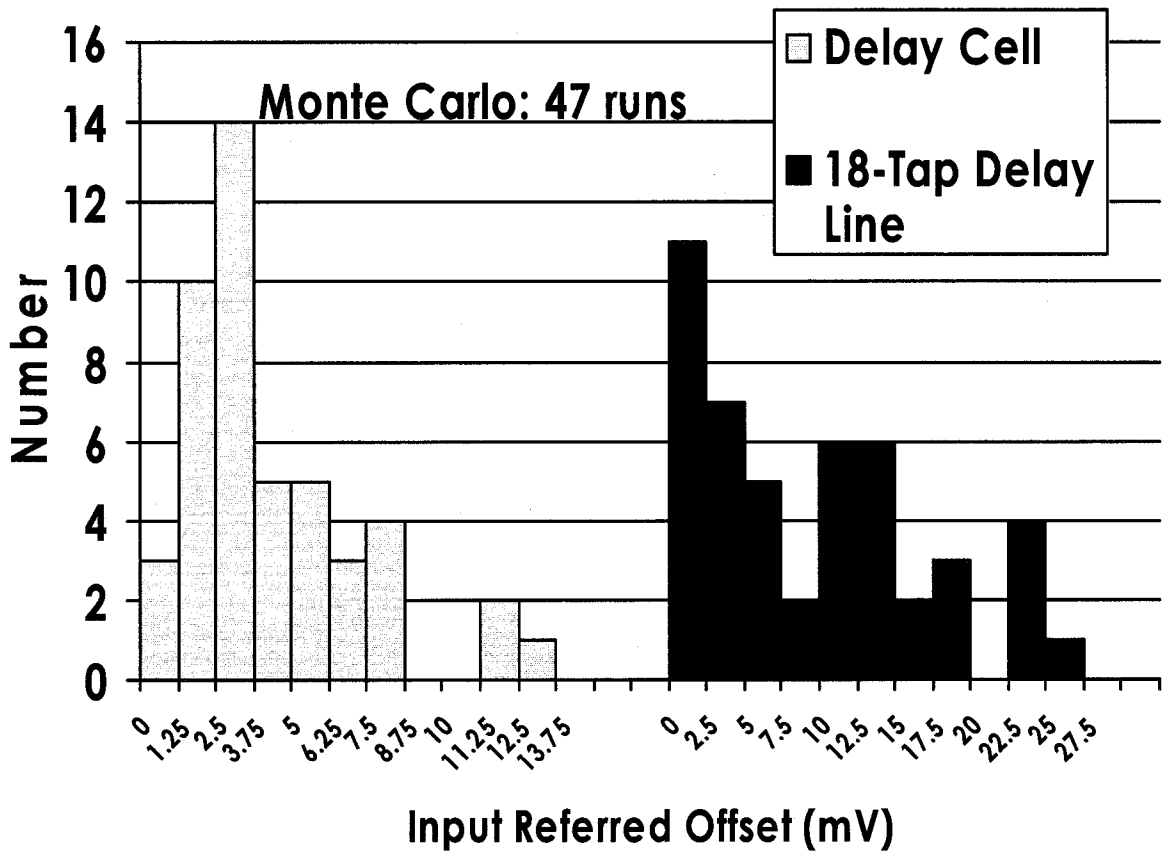


Figure 19 Input Referred DC Offsets: 47 Monte Carlo Runs

Table 4 Input Referred DC Offsets: Summary

Measure	Delay Cell	18-Tap Delay-Line
Average Offset	4.34 mV	9.55 mV
Maximum Offset	12.9 mV	27.4 mV
Standard Deviation	2.91 mV	7.49 mV

4.3.4 Simulations versus Specifications

Shown in Table 5 is a comparison of simulation results versus design specifications for the delay cell and the delay line. In addition to the simulation results presented in the previous sections, linearity (1-dB compression of a 20 GHz input) and input-referred noise were also simulated. Results show that all specifications were met.

Table 5 Summary of Simulation Results vs. Specifications for Delay Cell and Delay Line

Measure	Delay Cell		18-Tap Delay-Line	
	Specification	Simulation	Specification	Simulation
Power Supply	1.2 V	1.2 V	1.2 V	1.2 V
Current		6.66 mA		127 mA
Power		7.99 mW		152 mW
Area	Minimize	58.6 x 53.3 μm	Minimize	1520 x 53.3 μm
DC Gain	0 ± 0.1 dB	0.07 dB	0 ± 2 dB	1.23 dB
Peaking	none	none	none	none
Bandwidth		59.6 GHz	> 20 GHz	24.2 GHz
Min/Max Delay (0-20 GHz)	7.50 / 9.16 ps (8.33 ps ± 10%)	8.19 / 8.52 ps	135 / 165 ps	147 / 153 ps
Linearity (1-dB Comp. @ 20 GHz)		501 mV $_{0\text{-pk, diff}}$	100 mV $_{0\text{-pk, diff}}$	158 mV $_{0\text{-pk, diff}}$
Input Referred Noise		2.02 μV		2.32 mV
Average Input Referred DC Offset		4.34 mV		9.55 mV

4.3.5 Corner Simulations

To demonstrate the robustness of the delay cell, corner simulations were performed in which tuning voltages were tweaked in order to meet specifications. Since tuning these voltages is very time intensive (in a real product this would be done by feedback-control loops), only two corners were run in addition to the typical case: slow and fast.

For these corners, variations were made to process, voltage, and temperature. Process variation consisted of 1-Σ corner models as provided by the manufacturer, with variations affecting transistors, resistors, and capacitors. Inductors were custom made, therefore inductance values in the model were varied by ± 10% (which is probably closer to a 3-Σ than 1-Σ variation). Voltage was varied by ± 10%, and temperature varied from 0° to 125°. The corner conditions used are summarized in Table 6.

Table 6 Corner Conditions

		TYPICAL	**SLOW**	**FAST**
Process	NMOS/PMOS	Typ./Typ.	Slow/Slow	Fast/Fast
	Resistance	R_{nom}	R_{max}	R_{min}
	Capacitance	C_{nom}	C_{max}	C_{min}
	Inductance	Typ.	-10%	+10%
Voltage		1.2 V	1.08 V	1.32 V
Temperature		27°	125°	0°

The corner simulation results are shown in Table 7. Simulated values are given for uncompensated and compensated tuning of the delay cell. Uncompensated refers to the nominal values of ibias, vres, and vcap (these values were optimized for the typical case). The compensated simulation results are those for which these control signals have been tuned in order to meet specifications.

Specifications were not met for the slow corner, due to a flaw in the delay cell design. Due to lower VDD combined with slow NMOS process the current source did not have enough headroom (V_{DS}), causing it to operate in the linear region. Therefore, ibias had to be decreased to keep the current source in saturation, whereas it should have been increased in order to meet the DC gain specification. The result was that the DC gain is actually worse for the compensated case than for the uncompensated case (although specifications of peaking, bandwidth, and group delay were met). This problem could have been fixed by increasing the size of the current source, increasing the size of the differential pair, or with a combination of the two.

Table 7 Corner Simulation Results

MEASURE	UNCOMPENSATED			COMPENSATED	
	TYPICAL	SLOW	FAST	SLOW	FAST
DC Gain (cell/delay line)	0.07 / 1.23 dB	-1.26 / -22.7 dB	-0.06 / -1.083 dB	-2.36 / -42.5 dB *	-0.02 / -0.30 dB
Peaking (cell/delay line)	none/none	none/none	1.76 / 31.6 dB	none/none	none/none
Bandwidth (cell/delay line)	59.6 / 24.2 GHz	57.1 / 4.37 GHz	60.4 / 55.4 GHz	67.6 / 25.7 GHz	57.3 / 20.8 GHz
Min/Max Delay (cell)	8.19 / 8.52 ps	7.71 /10.79 ps	5.57 / 10.06 ps	8.06 / 8.42 ps	8.49 / 8.86 ps

* Specification not met

4.4 Conclusions

In this chapter, the prototype design of an 18-tap delay-line with T/3 tap spacing was presented based upon the proposed delay cell architecture of Chapter 3. The suitability of the architecture for use as a delay cell building block was demonstrated through simulated results. High bandwidth was achieved through the use of peaking inductors, and with just a ±2 % variation in group delay (within the signal bandwidth). The use of peaking inductors also allowed for a high inductance per area, allowing for a delay cell size of just 59 μm x 53 μm. Had planar inductors from the design kit been used (having the same inductance value), the minimum size would be 100 μm x 100 μm, compared to 13.5 μm x 13.5 μm for the stacked-inductors used in the delay cell. It should be mentioned however, that the kit inductor sizes are not optimized for such small inductance values; in this case, the kit inductor would have a lot of wasted space in its center.

Power consumption of the delay cell was 8 mW. This value is actually quite low (for an active architecture), given that it's for 40 Gb/s. Looking at power consumption per bit-rate, the equivalent power consumption values would be 2 mW/cell at 10 Gb/s, and 0.2

mW/cell at 1 Gb/s.

It was shown that the DC gain specification was not met at the 1-Σ slow corner. Due to limited design time, the process, voltage, and temperature corners were not simulated until after tapeout. Had this problem been discovered beforehand, it would have been a relatively simple problem to fix.

Chapter 5 Prototype Design: Top-Level

To facilitate testing of the single delay cell and tapped-delay-line, additional circuitry was required. This circuitry consists of input AC coupling, an active balun/input buffer, and output multiplexers/output drivers. The top-level was designed to:

- allow for de-embedding of test results
- provide input/output matching to approximately 50 Ω
- convert the single-ended input to a differential signal

5.1 Overview

Test measurements of the prototype were to be taken by die probing, and using a vector network analyzer (VNA). With the VNA, S_{21} forward transmission was to be measured from low frequency up to 40 GHz. In order to remove the influence on S_{21} from the die probes and testchip-level circuitry, a de-embedding scheme was used (full 2-port calibration using a calibration standards kit was performed to de-embed the VNA and input/output cables prior to testchip measurements).

A simplified example of the de-embedding scheme is shown in Figure 20. Shown in the figure are three components, each with their own contributions to S_{21} measurements. In order to de-embed measurements so that the device under test (DUT) can be characterized, two S_{21} measurements are taken by toggling VMUX; one path includes the DUT (DUT path), and the other bypasses it (REF path):

$$\mathbf{S_{21}(DUT\ path) = S_{21}\_1 + S_{21}\_DUT + S_{21}\_2}$$

$$\mathbf{S_{21}(REF\ path) = S_{21}\_1 + S_{21}\_2}$$

Taking the difference of these two measurements then yields the de-embedded result:

$$\mathbf{S_{21}\_DUT = S_{21}(DUT\ path) - S_{21}(REF\ path)}$$

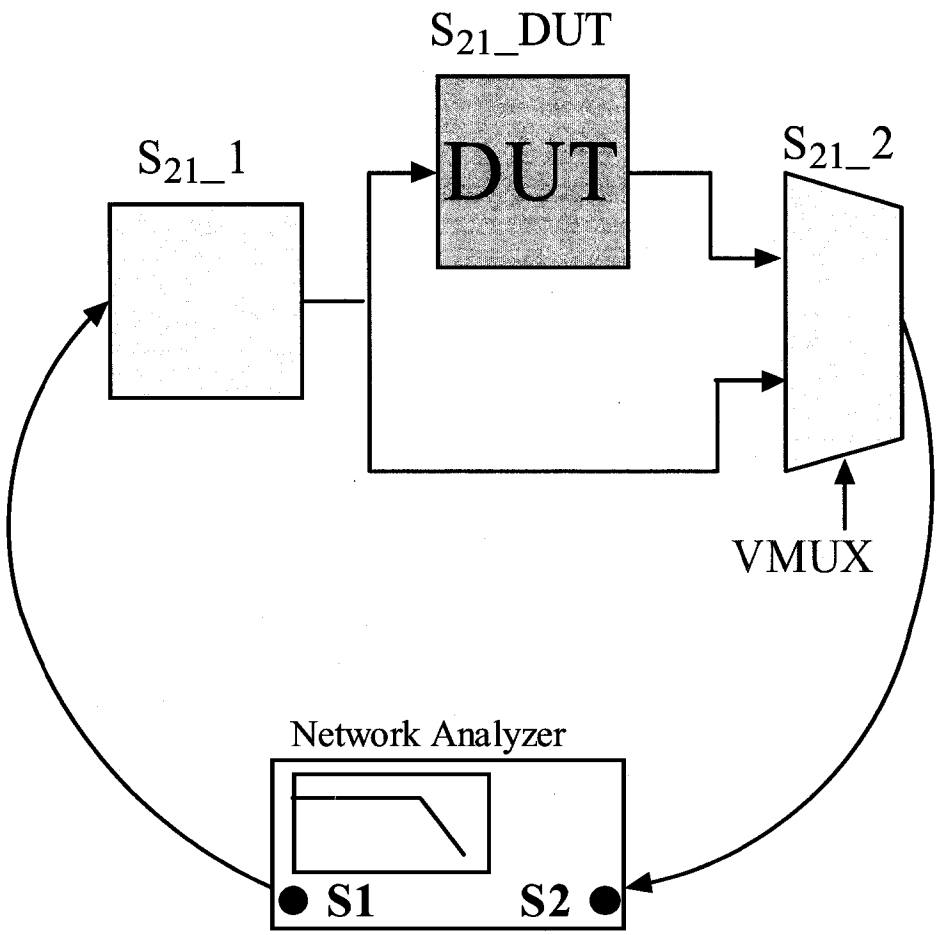


Figure 20 Example of S_{21} De-embedding

Shown in Figure 21 is a block diagram of the testchip prototype. It consists of the tapped-delay-line of the previous chapter, as well as the addition of testchip circuitry. It was designed to allow for S_{21} measurements to be de-embedded for both the delay cell, as well as the tapped-delay-line.

The VMUX digital signal chooses whether the DUT path's signal (delay cell/tapped-delay-line), or the reference path's signal (bypass of the delay cell/tapped-delay-line) is passed to the testchip outputs. Due to the physical distance from the input of the delay chain to 18th cell's output, a transmission line was used in the reference path used for de-embedding the tapped-delay-line. This was done to minimize the delay in the reference path and to ensure that signal strength does not roll-off within the signal bandwidth.

Not shown in the diagram is a 10 KΩ resistor connected between one of the output signals from delay cell #9 and a testchip pad named VDC_OFFSET. This was implemented as a precaution against DC offsets. If DC offsets had been much larger than simulations of section 4.3.3 showed, such that the tapped-delay-line became saturated, a DC voltage could be applied to VDC_OFFSET to either lower or raise the DC level of the signal it connected to, thereby cancelling the additive effect of DC offsets. It should be noted that this would only work if the delay-line became saturated after delay cell #9.

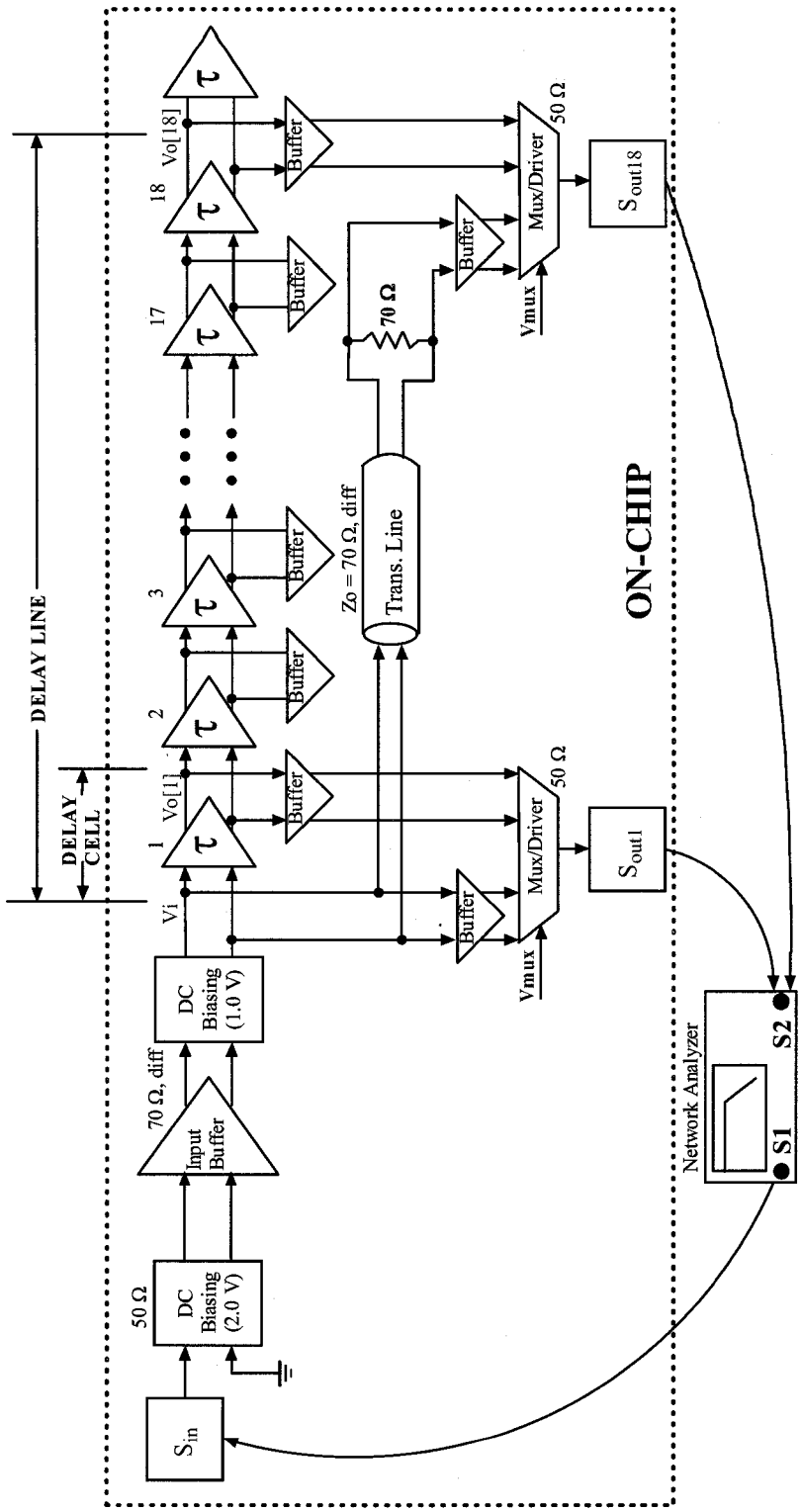


Figure 21 Testchip Block Diagram

As the method of testing was die probing, the testchip had to be designed for specific sets of probes. The probes used were 8-pin probes, with probe tips at 150 μm spacing on-center. The probe order of one set of 8-pin probes was power-ground-signal-ground-signal-signal-ground-power; the other set of 8-pin probes was just the mirrored version. The pad configuration of the testchip is shown in Figure 22, and a description of each signal is given in Table 8.

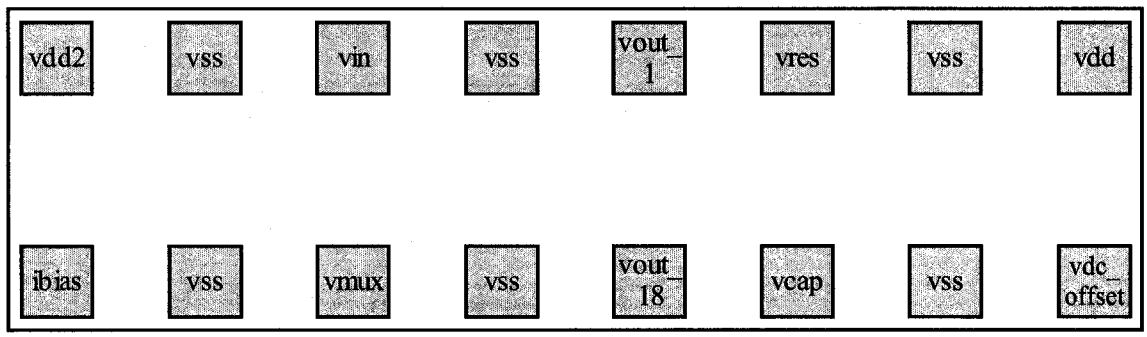


Figure 22 Testchip Pad Configuration

Table 8 Teschip Pad Descriptions

Pad	Type	Description
VDD2	Power	2.0 V DC supply
VSS	Ground	Ground
VIN	Signal	Input signal
VOUT_1	Signal	Output signal for single delay measurements
VRES	Tuning	Analog tuning signal (resistance)
VDD	Power	1.2 V DC supply
IBIAS	Current	Bias current for all current sources
VMUX	Digital	Selects DUT or reference paths at multiplexer
VOUT_18	Signal	Output signal for tapped-delay-line measurements
VCAP	Tuning	Analog tuning signal (capacitance)
VDC_OFFSET	Tuning	Analog tuning signal (DC offsets)

5.2 Input Buffer Design

The design of an input buffer was necessary in order to convert the single-ended input to a differential signal, which is applied to the input of the tapped-delay-line. Shown in Figure 23 is a schematic of the input buffer, the load that it drives, as well as the AC coupling/DC biasing at its input and output. In addition to making the broadband

conversion (up to 40 GHz), it had to have a relatively small input capacitance so as to not limit the input bandwidth. Preceding it was a 6.3 pF metal-insulator-metal (MIM) capacitor for AC coupling, and a 50 Ω resistor to VDD2 (2.0 V) for input matching and DC biasing. Therefore, the input capacitance from the input buffer added directly to the pad capacitance to set the input bandwidth. Due to bandwidth limitations, electrostatic discharge (ESD) protection circuitry was not implemented (on all high-frequency signal pads). The input bandwidth was simulated to be 50.9 GHz and the bandwidth of the input buffer was found to be 39.0 GHz. In order to achieve these bandwidths, tradeoffs of gain and power were made. The gain of the buffer was simulated to be -12.6 dB, and the power consumption was 65 mA from a 2.0 V supply.

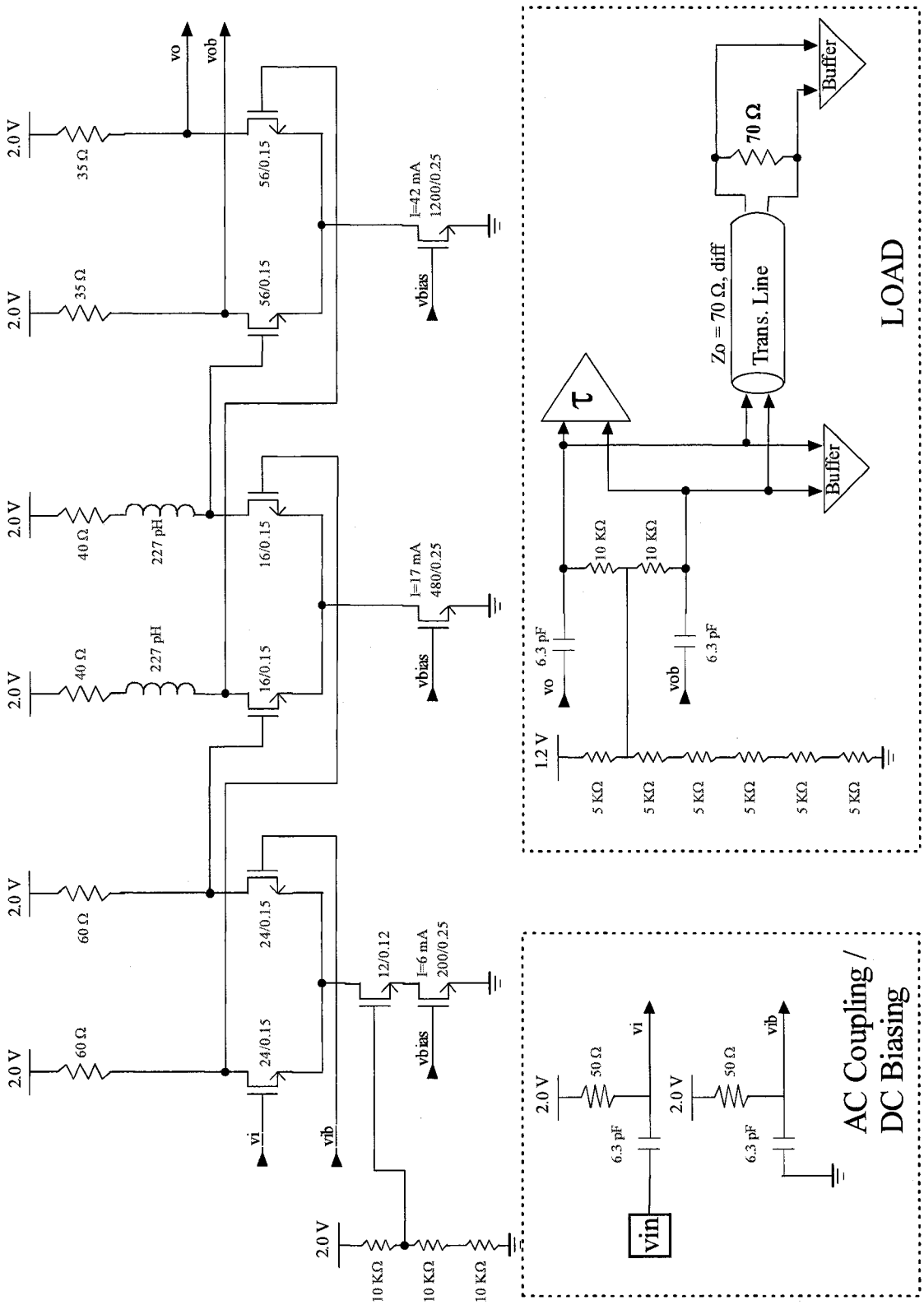


Figure 23 Input Buffer Schematic

The input buffer was designed as a three-stage amplifier. The first stage does most of the conversion from single-ended to differential. Having a single-ended input on vi and AC ground on vib, the common source of the differential pair is no longer considered AC ground, and therefore the circuit is not balanced. A small-signal model of the 1st stage of the input buffer is shown in Figure 24. Here the differential pair's source node is labeled v_s. Although the circuit's operation is not symmetric between the two sides, the transistors' values of DC bias parameters such as g_m, C_{gs}, C_{gd}, and r_o are still the same. A simplification made to the model is the current source – it is represented by an output impedance and a parasitic capacitance (r_{src} and C_{src}, respectively).

In order to generate a differential output signal, composed of two symmetrical signals (v_o and v_{ob}), equal currents (but opposite in polarity) across all frequencies must be delivered to the load. For the low to mid-band frequency range (all capacitors open-circuited), it can be seen that there are only 3 current paths to ground in the small-signal model. There are the paths through the two load resistors (R_L), and the path through the current source (R_{src}). By maximizing the output resistance of the current source, the differences between the two R_L currents are minimized. A cascode current source was used in place of a standard current source in order to increase R_{src}, and therefore improve symmetry in the output.

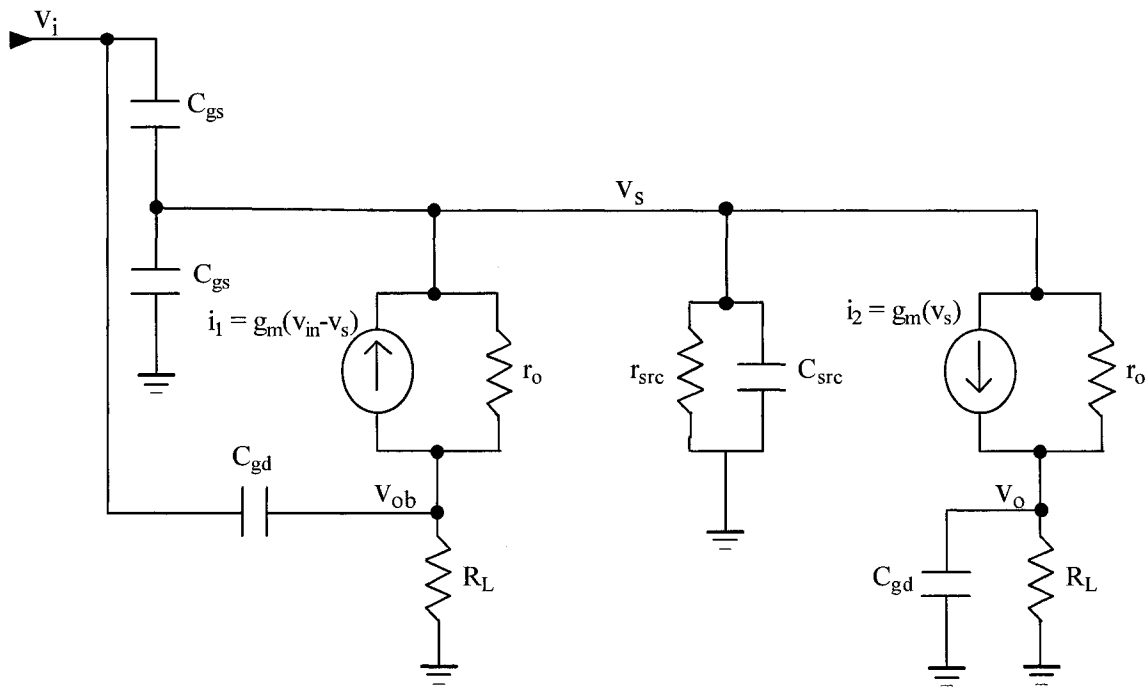


Figure 24 Small-Signal Model of Input Buffer 1st Stage

It should be noted that the currents of the two voltage-controlled current source are proportional to (v_{in} - v_s), and (v_s). Therefore, to better improve symmetry of the two branches, it is desirable to have $v_s = ½ v_{in}$. The small-signal transfer function relating signal v_s to v_i for low frequencies (no capacitors) was derived as shown in (8). Therefore, in order to achieve a value close to ½, an attempt was made to maximize values of g_m, r_o and r_{src}, within the previously mentioned limitations of input capacitance.

$$\frac{v_s}{v_i} = \frac{1}{2 \cdot \left(1 + \frac{1}{g_m \cdot r_o} + \frac{R_L + r_o}{2 \cdot r_{src} \cdot g_m \cdot r_o}\right)} \tag{8}$$

The high-frequency analysis is more complicated than the low-frequency operation. As can be seen from Figure 24, parasitic capacitances are the main source of asymmetry at high-frequency. The use of the cascode current source had an even greater effect at high-frequency than low-frequency. By choosing a cascode transistor having a small size and

large overdrive voltage, the drain capacitance (Csrc) was reduced from 75 fF to 4 fF for the same current. Also, by achieving a v_s value close to the v_i midpoint, the gate-source capacitances (Cgs) of the differential pair transistors more effectively cancelled each other out.

Another design challenge of the first stage was to design for a large input range. Given that the 1-dB linearity specification of the tapped-delay-line was 100 mV (0-peak, differential), the input buffer was to be capable of delivering such a signal. With an overall attenuation of 12.6 dB, the input buffer was to have an input 1-dB compression point of at least 427 mV (0-peak, single-ended) in order to deliver 100 mV at its output. Although meeting this specification could have been possible from a DC bias standpoint (enough headroom for the current source and differential pair), the differential pair transconductance was too high and/or tail current was too low to meet the specification. Had more time for further design iterations been available, meeting the specification may have been possible. Simulation showed a 1-dB input compression of 230 mV (0-peak, single-ended), resulting in a linear output limited to 54 mV (0-peak, differential).

The second stage of the input buffer effectively acted as a buffer between the first and third stages. The first stage load resistors were sized to 60 Ω, but the third stage effectively had a load of 17.5 Ω. In order to reduce the overall amount of attenuation in the input buffer while achieving high bandwidth, it was decided to use an intermediate stage (second stage) with load resistors of 40 Ω. Shunt inductive peaking, consisting of stacked inductors as described in section 3.5, was also used, allowing for a larger gain-bandwidth product. Inductive peaking was also considered for the first stage, but because each output node has a different RC time constant, each would require a different size inductor. Therefore peaking inductors weren't implemented due to matching concerns.

The third stage was an ordinary differential pair with 35 Ω load resistors. Part of its load was a transmission line (from the IBM 8RF-DM design kit), constructed of coupled wires on metal 7, over a metal 1 ground plane shield, and adjacent to metal 7 side shielding. The wires were 224 μm long, 1.5 μm wide, and distanced 20 μm apart. The transmission line had a DC resistance of less than 1 Ω over its length, and a characteristic impedance

of 70 Ω (differential). To prevent reflections, 35 Ω load resistors were chosen for matching at the near end, and a 70 Ω resistor (differential) was used for termination at the far end. Due to this termination resistor, the effective load resistance of the third stage was just 17.5 Ω (single-ended). AC coupling MIMs were used at the output of the input buffer (see the load in Figure 23), so this was the effective load resistance for high frequencies only (frequencies greater than approximately 4 GHz). In order to somewhat offset the effect of the small resistance on gain, a very large tail current of 42 mA was used for the third stage. Therefore, extra precautions were taken during layout to ensure that electromigration rules were closely followed for all metal interconnect and devices (particularly resistors). Inductive peaking was not used on this stage due to the implications on matching to the transmission line.

Shown in Figure 25 is the frequency response of the input buffer. The buffer's gain is shown as both a differential output signal, and separate single-ended outputs. From the single-ended curves it can be seen that they are fairly close at lower frequencies, but by 20 GHz there is a 1 dB difference, and by 40 GHz there is a 3.8 dB difference. The effect of the AC coupling on the output can be seen by the low-frequency roll-off; at low frequencies, the load resistance is 35 Ω, whereas at high frequency it is 17.5 Ω. This effect is of no consequence to testing however as the input buffer is de-embedded anyway.

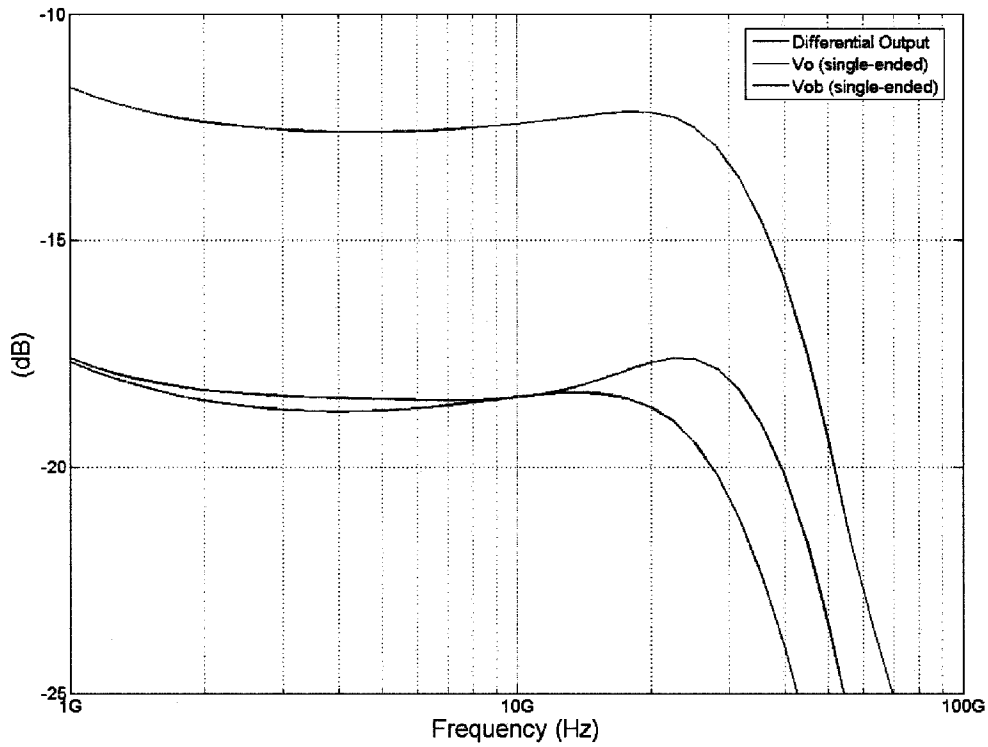


Figure 25 Input Buffer Frequency Response

Table 9 presents a summary of some design parameters and simulation results for the input buffer. Simulations include the full load of the input buffer, and with extracted parasitics (unless otherwise noted). Due to the AC coupling effect on the output at low-frequency, DC gain and 3-dB bandwidth values are based on mid-frequency values (~ 4 GHz).

Table 9 Input Buffer Design Parameters and Simulation Results

Value/Measure	First Stage	Second Stage	Third Stage	Overall
Load Resistors	60 Ω	40 Ω	35 Ω	
Tail Current	6 mA	17 mA	42 mA	65 mA
DC Gain	-2.6 dB	-6.0 dB	-4.0 dB	-12.6 dB
Bandwidth	53.2 GHz *	59.8 GHz *	62.2 GHz *	39.0 GHz
1-dB Input Linearity	230 mV (0-pk, single-ended)			230 mV (0-pk, single-ended)

* Simulated using estimated back-annotated parasitic capacitances, not full extraction

5.3 Multiplexer / Output Driver Design

For de-embedding test measurements, multiplexing at the output was needed to choose between the DUT path and the reference path (as shown in Figure 20). To be able to characterize the single delay cell as well as the tapped-delay-line, output signals were taken following the 1st delay cell and the 18th delay cells in the chain, respectively. To ensure that these cells would see the same load as the other cells in the tapped-delay-line, the first stage of the multiplexer / output driver had to be identical to the tapped-delay-line load as described in section 4.2.

Figure 26 shows a schematic of the multiplexer / output driver stage. Two instances of this block were placed on the prototype. One instance had v1/v1b connected to the 1st delay cell output and v2/v2b connected to the 1st delay cell input. The other instance had v1/v1b connected to the 18th delay cell output and v2/v2b connected to the 1st delay cell input (via the terminated transmission line).

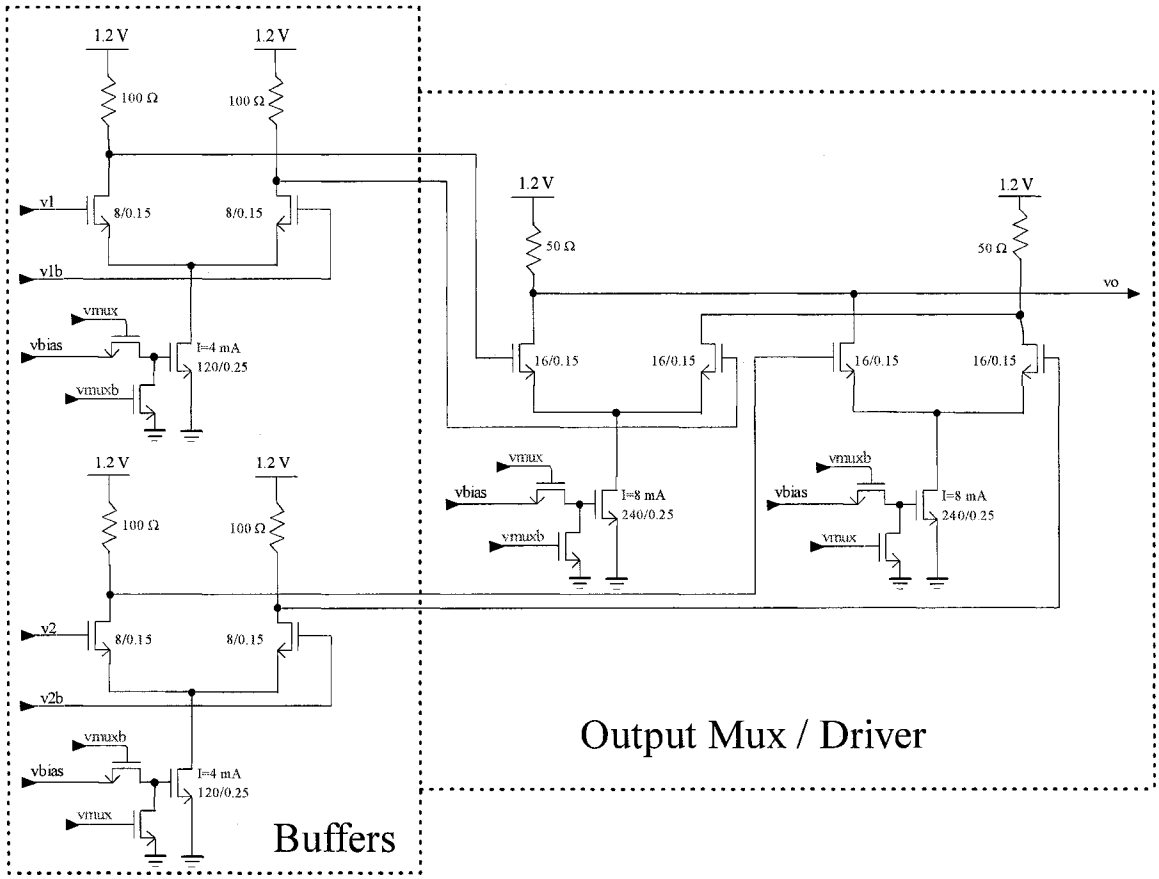


Figure 26 Schematic of Multiplexer / Output Driver

The first stage consists of two buffers, one for the DUT path and the other for the reference path. Their outputs are connected to the second stage consisting of two differential pairs with cross-coupled 50 Ω resistor loads (for impedance matching). Only one of the outputs is taken to the output pad, automatically resulting in a 6 dB loss of signal strength. A current mirror load would have converted the differential signal back to a single-ended signal without the signal strength penalty; however, the parasitic capacitance of the active circuitry required would have resulted in a much lower bandwidth.

Multiplexing is accomplished outside of the signal path to avoid a reduction in bandwidth and gain. Current sources are switched on or off with the digital signals vmux and vmuxb, effectively choosing whether the DUT or reference path is to be measured. Multiplexing mainly occurs at the second stage, but was added to the buffer stage as well

for further isolation, as there is no penalty in gain or bandwidth for doing so.

The multiplexer / output driver consumes a total of 24 mA from a 1.2 V supply. Post-layout simulation, which included a signal output pad and 50 Ω load, showed a bandwidth of 40.2 GHz. The circuit's gain was sacrificed in order to achieve this bandwidth; the gain was simulated to be -24.2 dB. Although this is a large amount of attenuation, 6 dB of it is due to only taking one of the two outputs at the final stage, and another 6 dB is due to the 50 Ω (off-chip) load that it was designed to drive.

5.4 Prototype Layout

Layout of the prototype is shown in Figure 27. Labeled in the figure are all of the pads, as well as select instances of the major blocks. In order to reduce the distance between the delay-line input and the multiplexer at the delay-line output (the reference path), the delay cells were cascaded in a half-loop. In the figure, the 1st and 18th delay cells are annotated, as well as the transmission line that separates them. The 19th delay cell (which simply acts as a load) can be seen to the left of the 18th cell. Below the input buffer are the AC coupling MIM capacitors (in green) and DC biasing resistors for the input buffer; above it are the MIM capacitors and biasing resistors for the delay-line.

Most of the decoupling capacitors for IBIAS, VRES, and VCAP are within the ring of delay cells. These signals were routed on a circularly-shaped bus on metal 2 (in pink); under this bus are the decoupling capacitors (NMOS-in-NWELL).

All extra space on the chip was used for power supply bussing and decoupling. Due to the high current consumption of the chip, power busses were made extremely wide. The VDD bus was 40 μm wide on metal 8 (copper, very thick); VSS was bussed directly underneath on metals 6 and 7 strapped together (40 μm). Decoupling capacitors (NMOS-in-NWELL) occupied all available space under this VDD/VSS bussing. Power supplies for the input buffer (VDD2/VSS) were bussed/decoupled in a similar manner, but with busses 20 μm wide. The remaining space on the chip was filled with MIM decoupling capacitors for VDD/VSS and VDD2/VSS; these can be seen in the layout as the green

rectangles in the lower half of the chip and at the center of the cascaded delay cells.

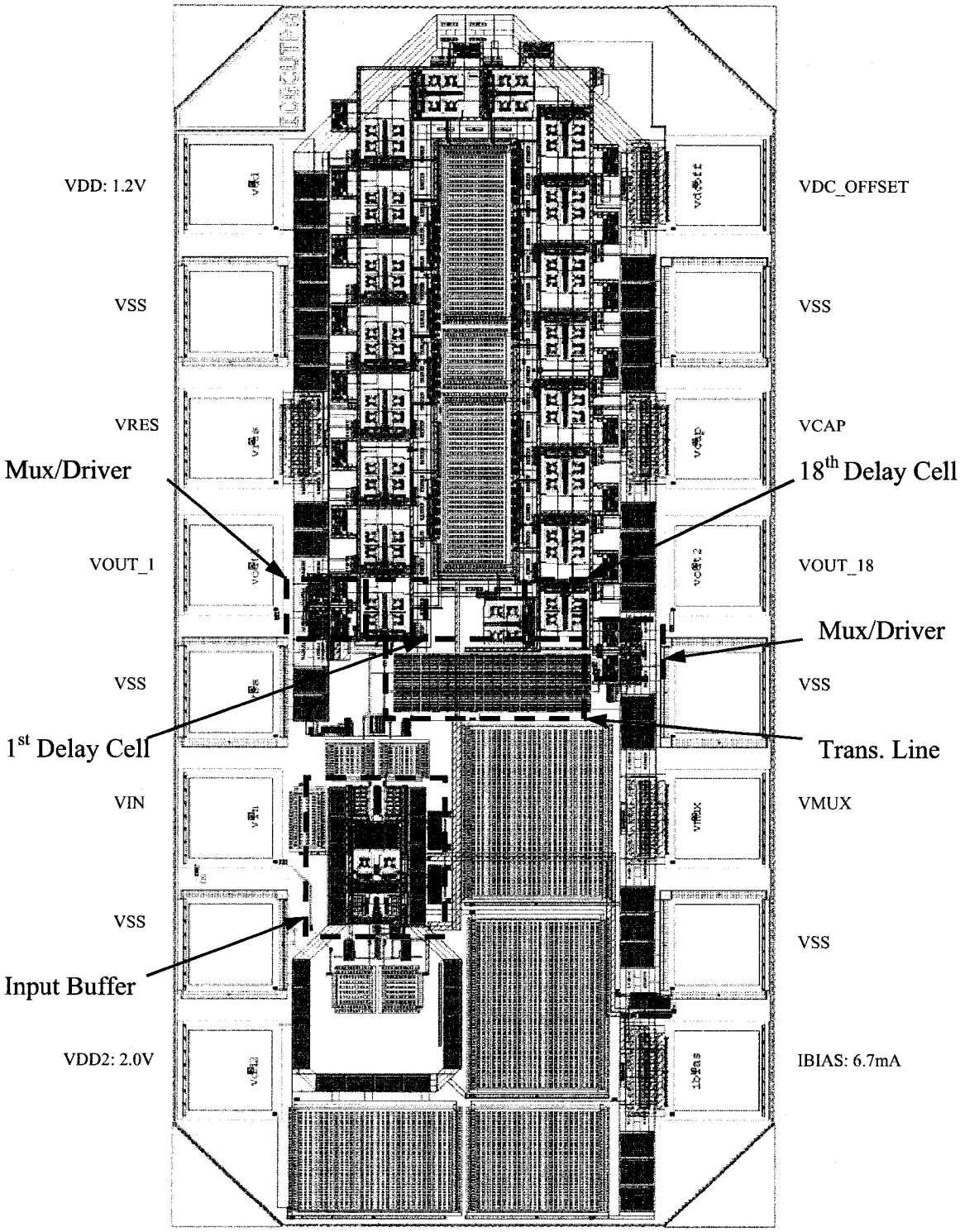


Figure 27 Annotated Prototype Layout

5.5 Prototype Simulation Results

After all layout of the prototype was complete, a full-chip extraction of all devices and parasitic capacitances and diffusions was taken. This extracted view was simulated in the same manner as it would be tested: by measuring the delay and reference paths, and taking their difference for a de-embedded result.

The following four figures show the results of these simulations. In each figure, there are two plots; the top plot shows the individual simulated measurements, and the bottom plot shows the difference. The S_{21} (amplitude) simulation results for the single delay cell and for the 18-tap delay-line are shown in Figure 28 and Figure 29, respectively. The group delay (S_{21} in delay format) results are shown in Figure 30 and Figure 31.

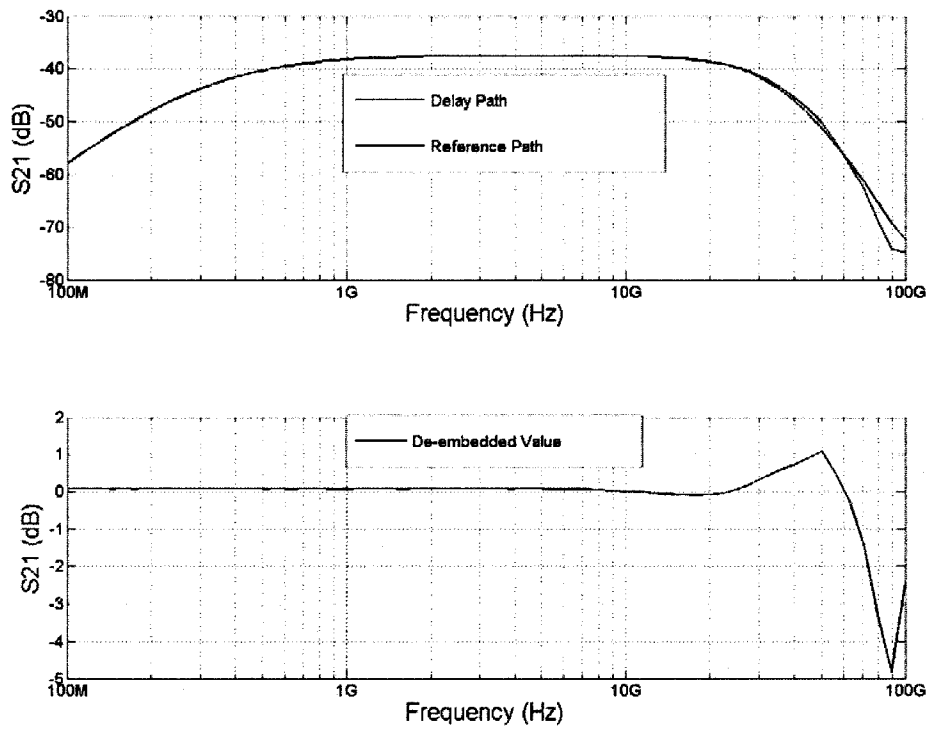


Figure 28 Full-chip S_{21} for Single Delay Cell

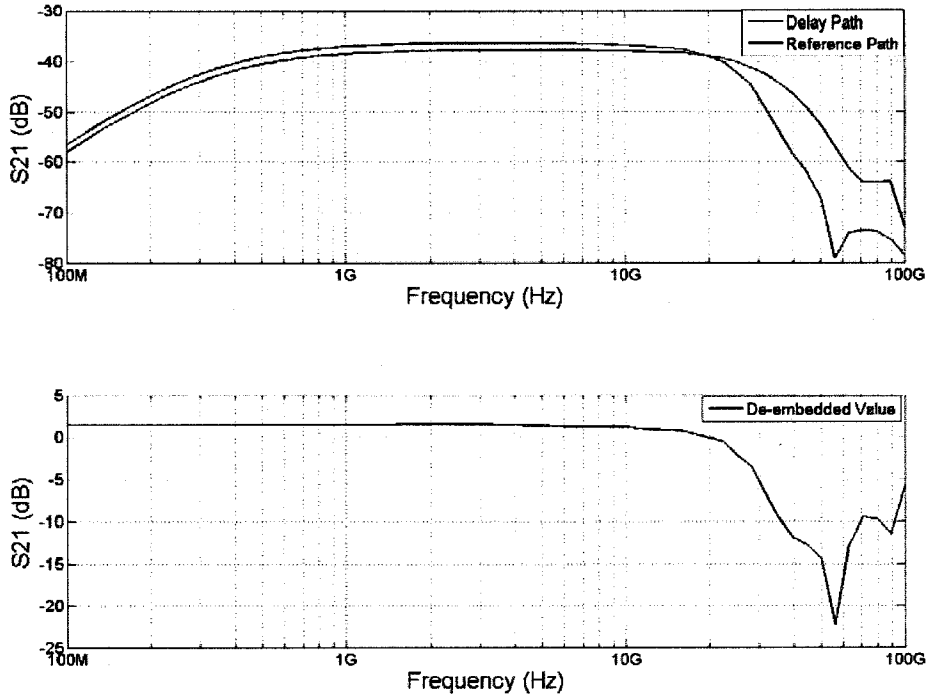


Figure 29 Full-chip S_{21} for 18-Tap Delay-Line

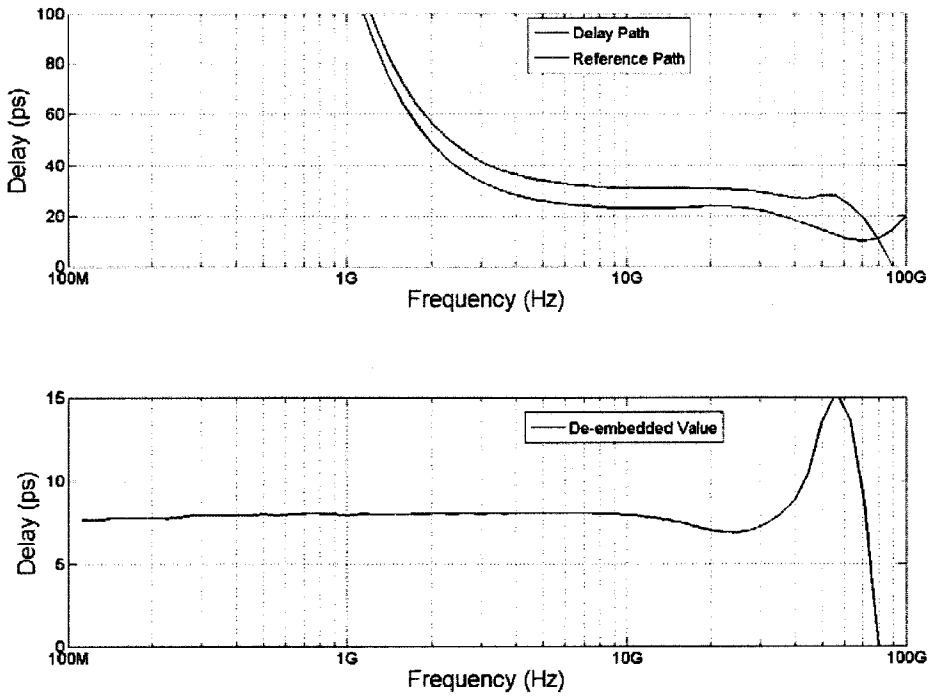


Figure 30 Full-chip Group Delay for Single Delay Cell

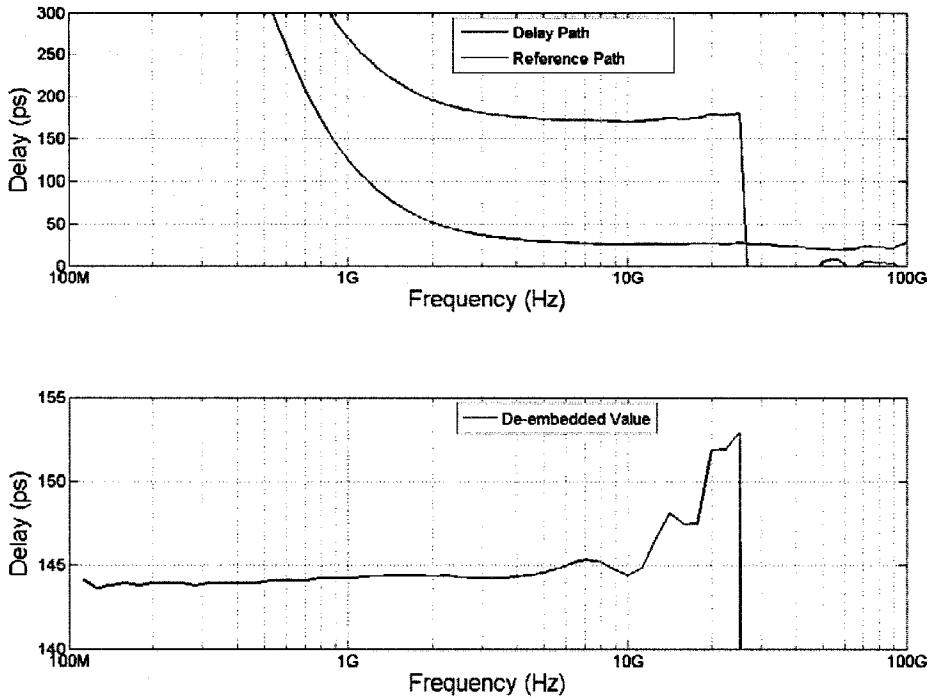


Figure 31 Full-chip Group Delay for 18-Tap Delay-Line

Shown in Table 10 is a comparison of the de-embedded simulation results (from the above figures) to the directly-simulated results from Section 4.3. Although the results for the delay-line compare quite well, there are noticeable differences for the single delay cell. These differences can be explained by the non-symmetrical single-ended to differential conversion of the input buffer. The tapped-delay-line is not affected as severely because for the delay path measurement, the single-ended signals become less skewed with each stage, and for the reference path measurement, the transmission line removes much of the skew.

Table 10 Comparison of Direct Simulation to Testchip De-embedding Simulation

Measure	**Delay Cell**		**18-Tap Delay Line**	
	Direct Simulation	**De-embedding Simulation**	**Direct Simulation**	**De-embedding Simulation**
DC Gain	0.07 dB	0.07 dB	1.23 dB	1.44 dB
Peaking	none	0.99 dB	none	none
Bandwidth	59.6 GHz	77.6 GHz	24.2 GHz	24.0 GHz
Min/Max Delay (0-20 GHz)	8.19 / 8.52 ps	6.83 / 8.02 ps	147 / 153 ps	144 / 152 ps

5.6 Conclusions

In order to characterize both the delay cell and the delay-line, die probing with a VNA was to be used. To do so, extra circuitry consisting of an input buffer, AC coupling/DC biasing circuitry, and a multiplexer/output driver were added to the prototype. This extra circuitry had to be able to pass 40 GHz signals (maximum frequency of the VNA), and therefore gain was sacrificed for bandwidth in these circuits. Overall, the de-embedding circuitry added as much as 58 dB of attenuation, and as little as 38 dB of attenuation within the 100 MHz to 40 GHz band to be tested. If the prototype had been developed in a BiCMOS process, this attenuation would probably have been much smaller. Had more appropriate test equipment been available, such as differential probes with calibration substrate, much of this circuitry would not have been necessary.

Of all circuits on the prototype, including the delay cell, the input buffer was the hardest to design. The design specifications were very difficult to meet given the limitations on input capacitance, the requirement of matching to the transmission line, the size of the load, and of course the conversion from single-ended to differential signaling. Originally, the 1.2 V supply was to be the only on-chip supply, used for the input buffer as well. The input buffer's supply was increased to 2.0 V when the importance of using the cascode current source was realized. With a large V_{DS} needed across the cascode device and a large input swing, this first stage could not operate at 1.2 V. It would have been advantageous to have used this 2.0 V supply for the multiplexer/output drivers as well (which were designed before the input buffer), but there wasn't time to make the change.

Chapter 6 Experimental Results

6.1 Inductor Test Structures

In order to determine the effectiveness of the stacked-inductors' design and modeling, as outlined in Chapter 3.5, test structures were created to characterize an inductor. It was originally intended to have inductor test structures on the same chip as the delay cell prototype, and therefore be able to characterize the same inductor that was used in the delay cell. However, due to a lack of granted silicon area, there wasn't enough room for them.

Inductor test structures were fabricated in a different process though. This was a 0.13 μm BiCMOS process with interconnect that was similar to the lower 5 metals of the IBM 8RF-DM process (the inductors used in the delay cells used metals 2-5). The inductor was designed and modeled in the same manner as the inductors used on the delay cell prototype.

6.1.1 Inductor Design

Figure 32 shows the annotated layout of the inductor. It was created in ASITIC, having the following physical characteristics:

- 5-metals stacked (metals 6-2)
- Size: 9.5 μm x 9.5 μm
- Turns/layer: 3
- Metal width: 0.8 μm
- Turn spacing: 0.46 μm

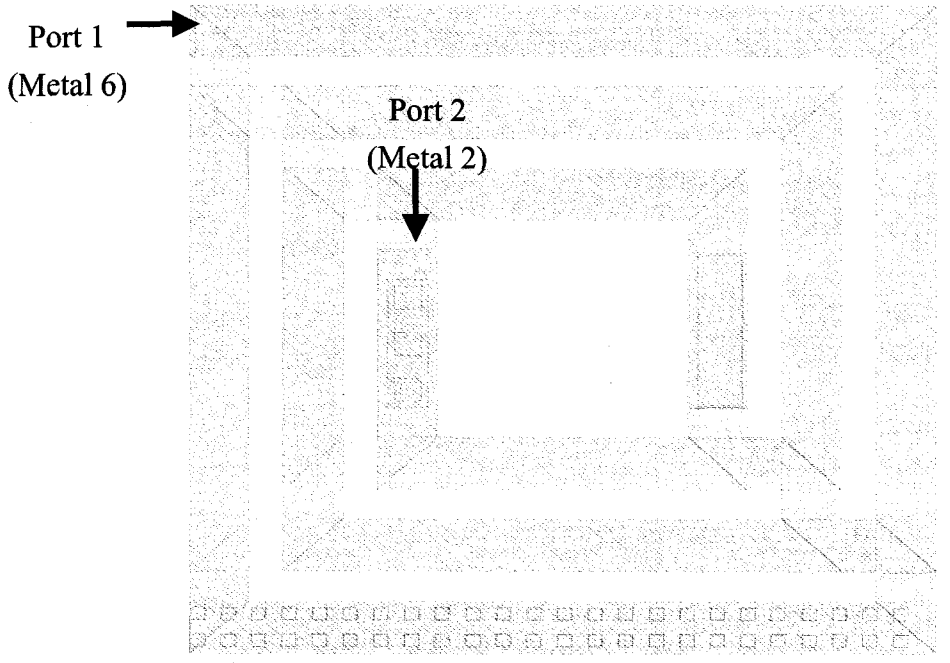


Figure 32 Annotated Inductor Layout

6.1.2 Layout of Inductor Test Structures

In order to de-embed the parasitic components from the measurement results, three test structures were created: DUT (device under test), open, and short. Normally such characterization would be performed using 2-port VNA measurements, however, due to limited available chip area, the test structures were designed for 1-port measurements. Further area savings were made by the sharing of ground pads. Figure 33 shows the layout of the test structures. For the characterization measurements, 3-pin probes were used (ground-signal-ground). The probe placements for each of the three measurements (DUT, open, short) are shown in the layout plot. The leftmost structure shows the inductor (DUT) connected between signal and ground pads. In the middle of the plot is the open structure; this structure is identical to the DUT, but without the inductor (pads and interconnect are the same). The rightmost structure is the short structure; it is identical to the DUT, but without the inductor and with an added piece of metal to short the interconnecting metal lines. Shown in Figure 34 is a zoomed-in plot of the DUT

portion. The transparent red rectangles over the inductor and interconnect are metal fill exclusion layers (to prevent automated pattern fill in signal areas).

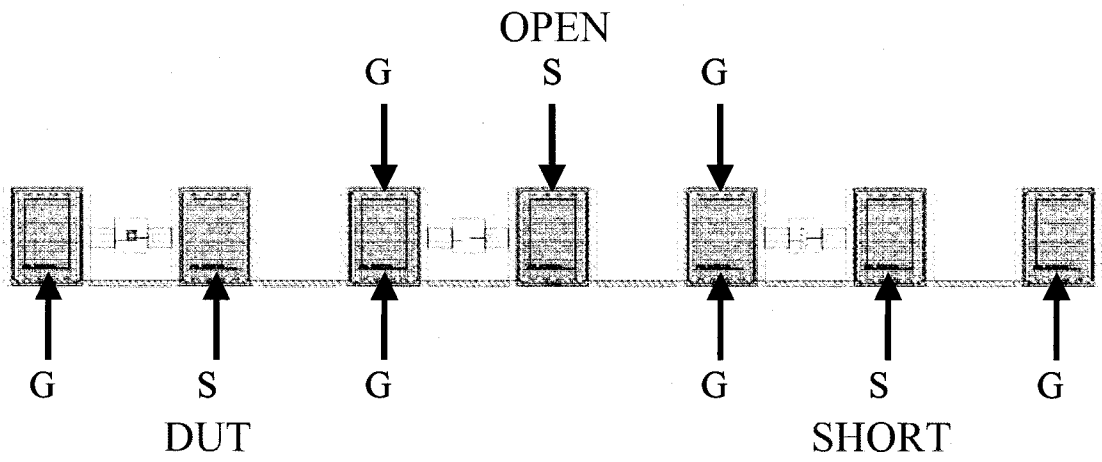


Figure 33 Annotated Layout of Inductor Test Structures

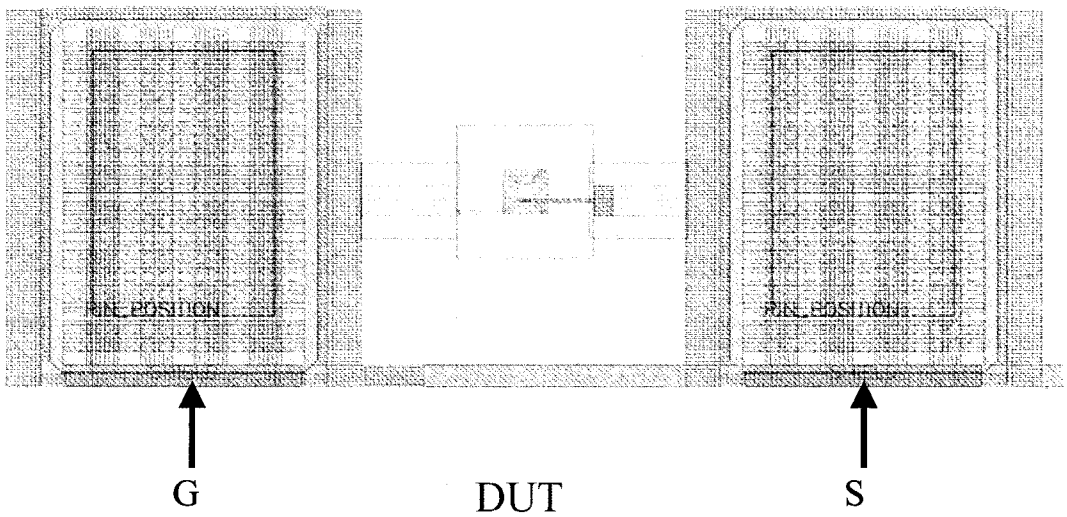


Figure 34 Annotated Layout of Inductor Test Structure (Zoom-In of DUT)

When taking VNA measurements, there are many parasitic factors within the test environment that influence measurements. These effects may come from the test cables, die probes, pads, and interconnect. With smaller devices, these parasitic effects have a

larger influence on measurements.

In order to limit these effects, first to the chip level, the VNA is calibrated to the tips of the die probes. The first step of this procedure is to use a calibration kit to calibrate the VNA to the cable ends. This involves attaching the highly accurate and precise components of the kit (short, open, thru, 50Ω load) to the cable ends, and taking measurements which are stored to the VNA memory. This then brings what is known as the "reference plane" to the cable ends (factors affecting measurements up to this point have then been subtracted). To bring the reference plane to the probe tips, a calibration substrate is used. Like the VNA calibration kit, the calibration substrate consists of a number of accurate and precise components, however, they are on a silicon substrate specifically designed for the physical dimensions of the die probes used. After landing the probes and taking measurements, the reference plane is then considered to be at the tips of probes.

In order to subtract, or de-embed, the parasitic effects of the inductor test structures, measurements of DUT, open, and short are taken. Figure 35 shows a model used for 2-port de-embedding, as described in [28]. By taking all three measurements, the Y and Z parasitic components can be subtracted, leaving just the measurement data for the DUT.

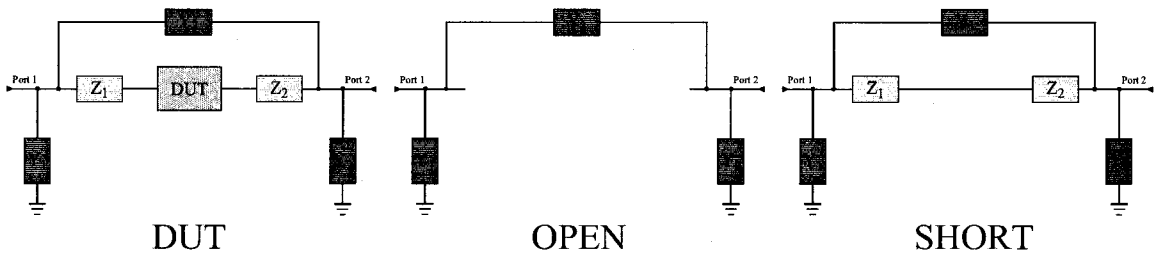


Figure 35 Model Showing Parasitic Components for 2-Port De-embedding

The above model and technique are for a 2-port characterization. As the constructed inductor test structures were for a 1-port characterization, the above model was modified. In order to do so, Port 2 of the model is shorted to ground, resulting in the model shown in Figure 36.

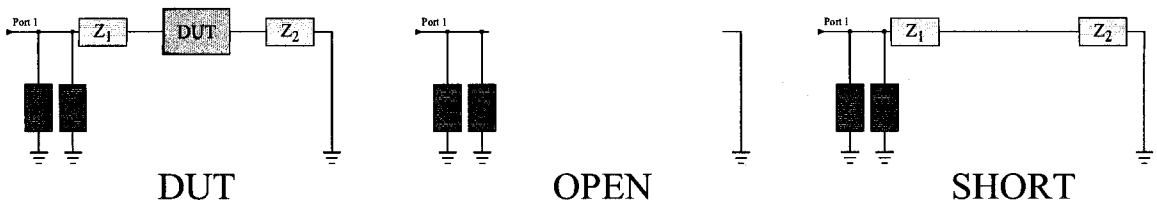


Figure 36 Model Showing Parasitic Components for 1-Port De-embedding

Using the above model, it can be seen that the parasitic components can be subtracted from the DUT measurement. By solving for the total admittance (Y_{total}) seen at Port 1 of the DUT structure and rearranging terms, the impedance of the DUT (Z_{DUT}) can be described by (9):

$$Z_{DUT} = \frac{1}{Y_{total} - Y_1 - Y_3} - Z_1 - Z_2 \tag{9}$$

By taking Y_{11} measurements for each test structure (Y_{total}, Y_{open}, Y_{short}), this de-embedded result can be realized according to (10):

$$Z_{DUT} = \frac{1}{Y_{total} - Y_{open}} - \frac{1}{Y_{short} - Y_{open}} \tag{10}$$

From Z_{DUT}, inductance and resistance versus frequency can be extracted, as shown in (11) and (12):

$$L_{IND} = \frac{\mathrm{Im}(Z_{DUT})}{2\pi f} \tag{11}$$

$$R_{IND} = \mathrm{Re}(Z_{DUT}) \tag{12}$$

6.1.3 Inductor Test Results

Shown in Figure 37 are the measured and simulated results of the inductor characterization. Given in the plots are inductance (top) and resistance (bottom) versus frequency. Four separate sets of test measurements were made in intervals of 5 GHz, from 100 MHz to 20 GHz. For each set, a new calibration (at VNA cables and die probe

tips) was performed. Given that the three intervals spanning 5 GHz to 20 GHz are continuous with one another, but not with the interval from 100 MHz to 5 GHz, it is assumed that something went with this interval either during calibration or during testing (such as a poor landing of the die probes).

Ignoring the 100 MHz – 5 GHz interval, the measurements agree well with simulation. The largest measured to simulated error in inductance is just 1%, and 14% for resistance.

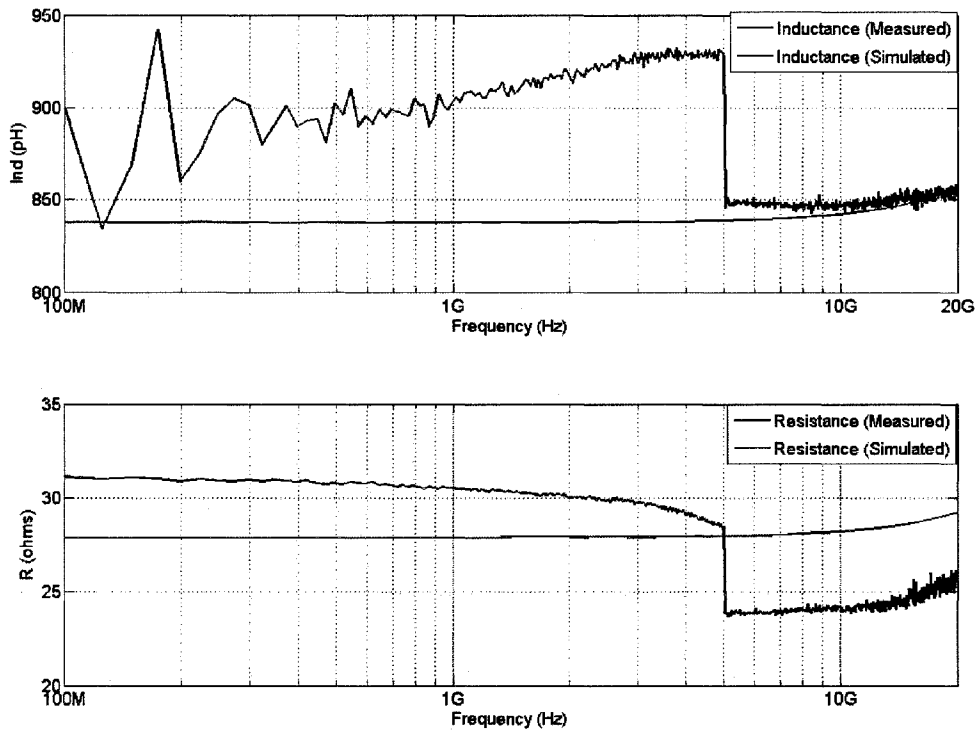


Figure 37 Measured Results of Inductor Characterization

6.2 Prototype Test Results

A die photo of the testchip protype is shown in Figure 38. Test measurements for the testchip were taken using two different methods (both using die probing):

1. Vector Network Analyzer (VNA)
2. Signal Generator / Spectrum Analyzer

The following two subsections present the results for each method. The biasing conditions that were used are given in Table 11 (same for both methods). These are the values that were set on the voltage supply equipments; on-chip values are not necessarily equivalent (discussed in Section 6.4).

Table 11 Bias Conditions for Testing

Voltage Supply	Voltage
VDD	1.5 V
VDD2	2.4 V
IBIAS	0.4 V
VRES	1.2 V
VCAP	1.2 V

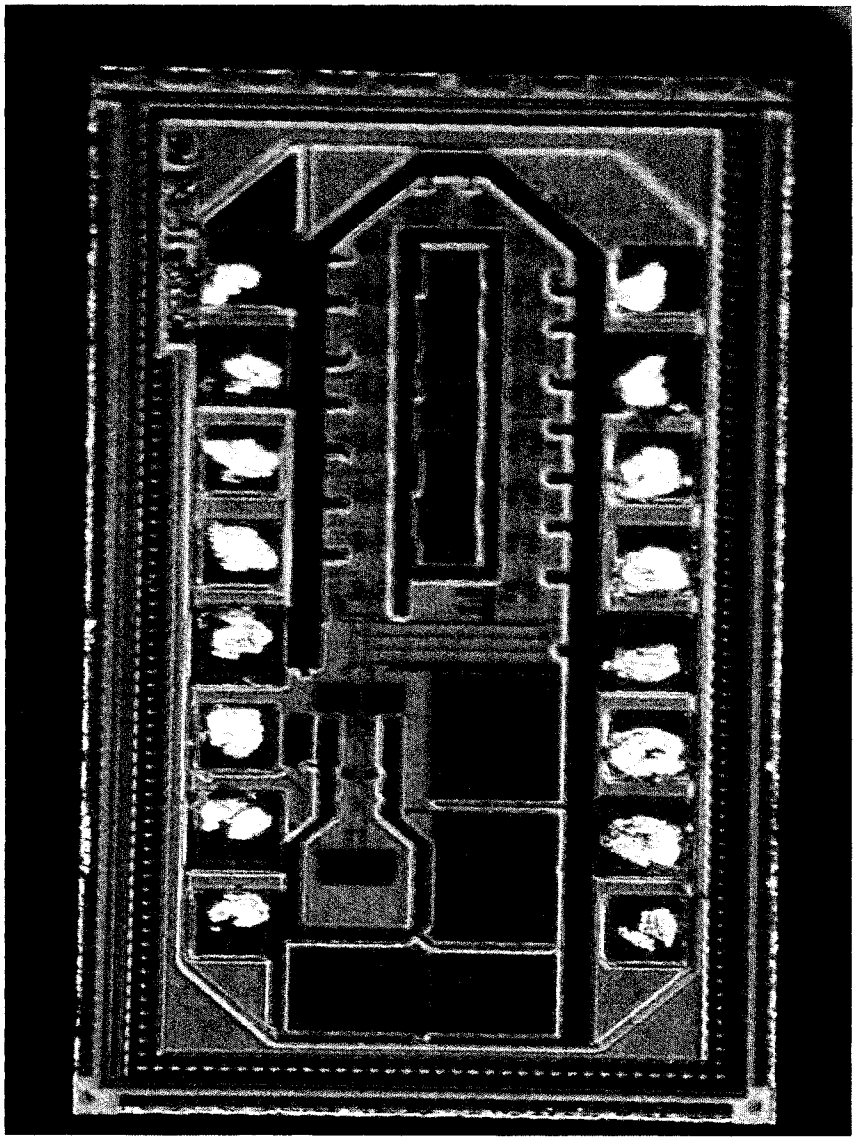


Figure 38 Prototype Die Photo

6.2.1 Test Results Using the VNA

Shown in Figure 39 and Figure 40 are the S_{21} measured results for the single delay cell and the tapped-delay-line, respectively. In each figure, the top plots represent the delay and reference path measurements (as well as the S_{12} measurement), and the bottom plot displays the de-embedded value, as well as the simulated value as given in Chapter 5.5. Similarly, Figure 41 and Figure 42 give the group delay measurements, de-embedded

values, and simulated values for the single delay cell and for the delay line. Measured and simulated values of S_{11} and S_{22} are shown in Figure 43 and Figure 44, for the single delay cell and the delay line.

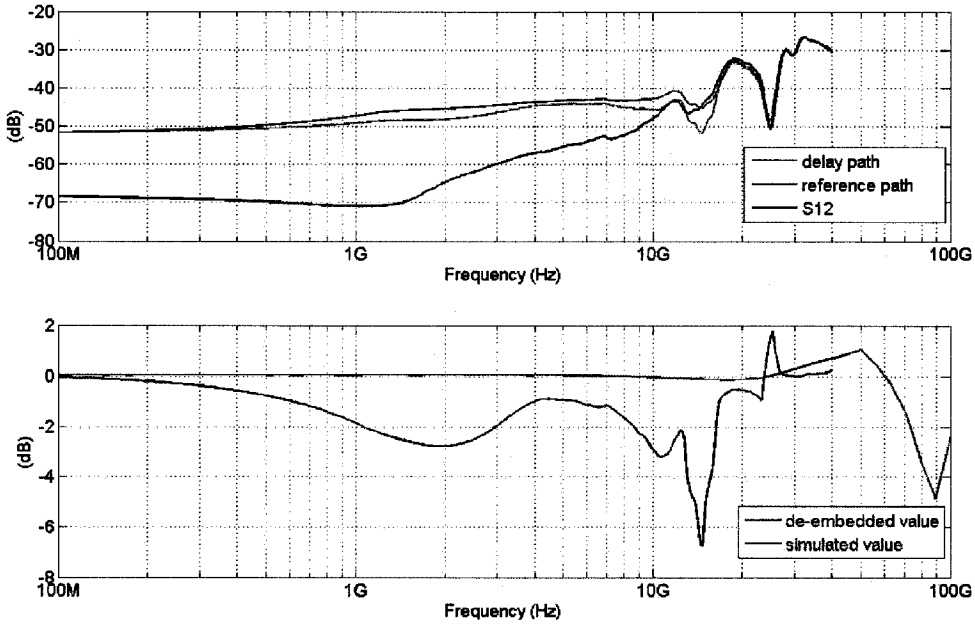


Figure 39 S_{21} Measurements for Single Delay Cell (VNA)

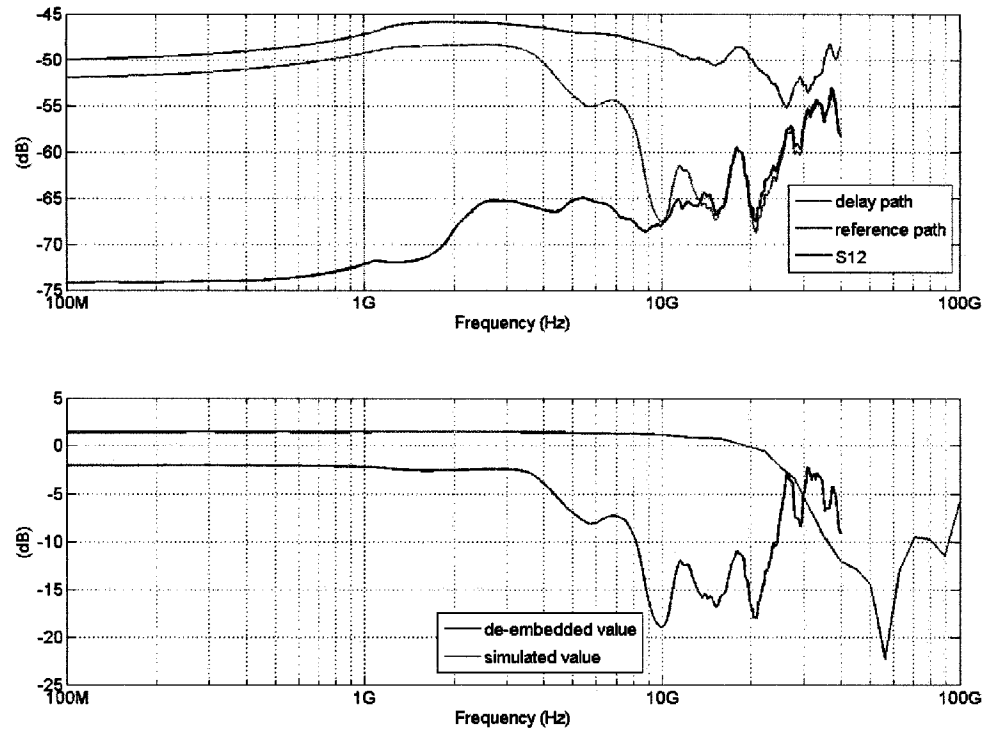


Figure 40 S_{21} Measurements for Delay Line (VNA)

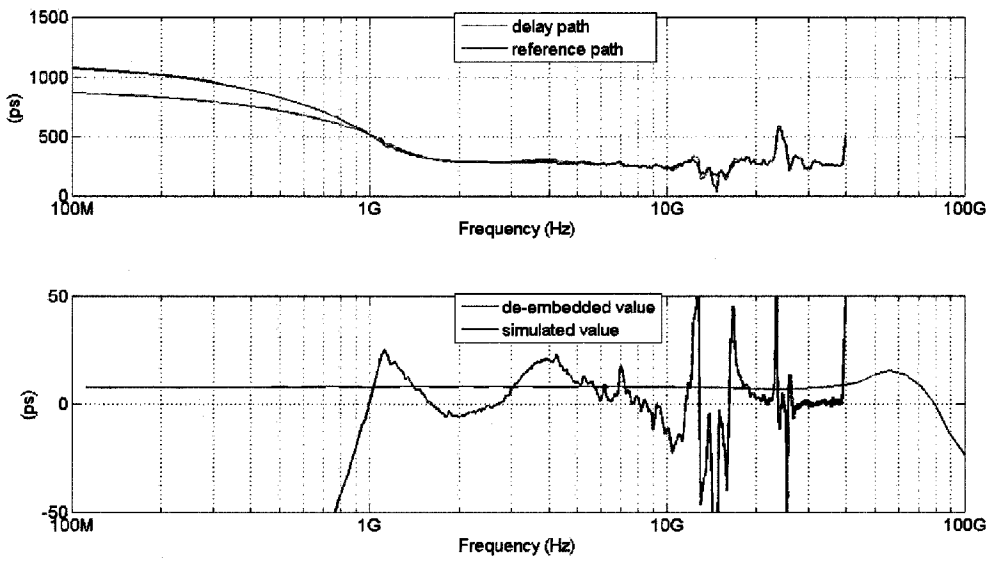


Figure 41 Group Delay Measurements for Single Delay (VNA)

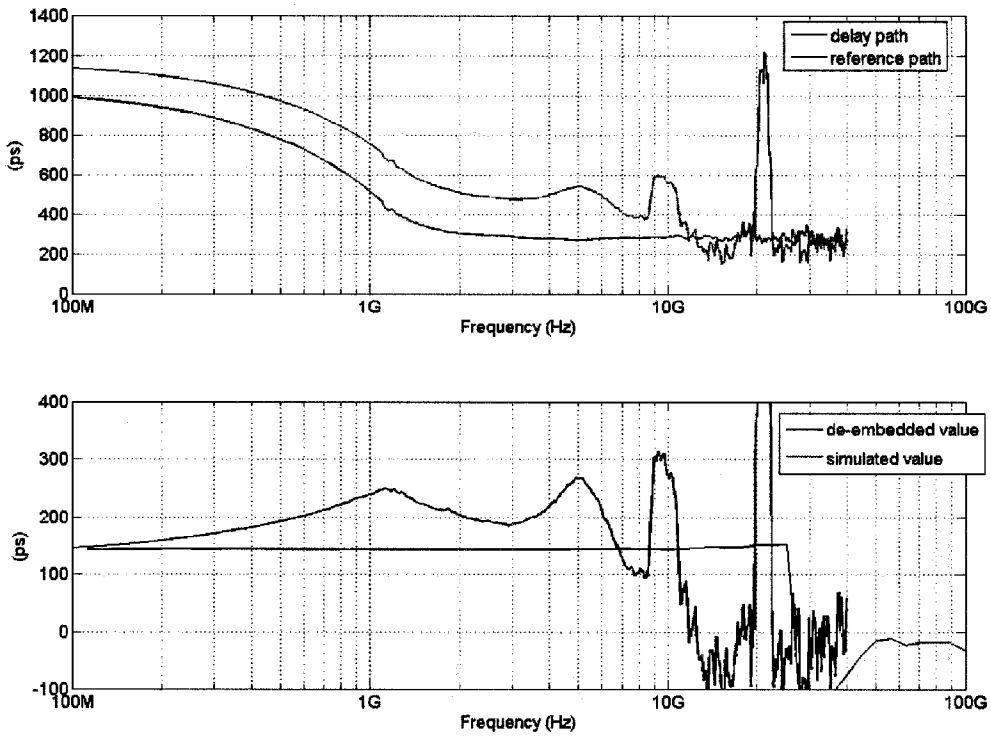


Figure 42 Group Delay Measurements for Delay Line (VNA)

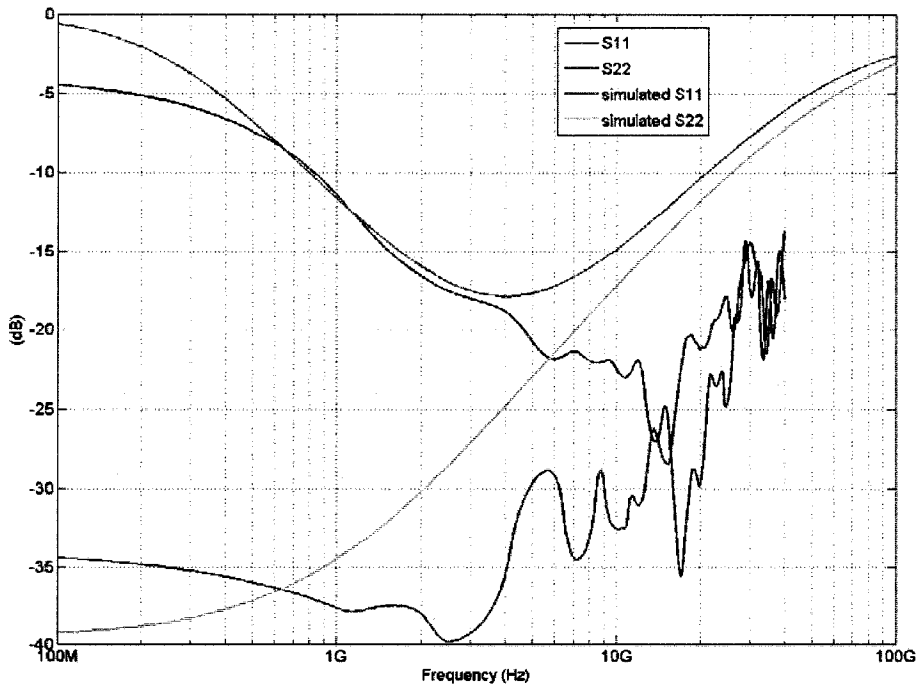


Figure 43 S_{11}/S_{22} Measurements for Single Delay (VNA)

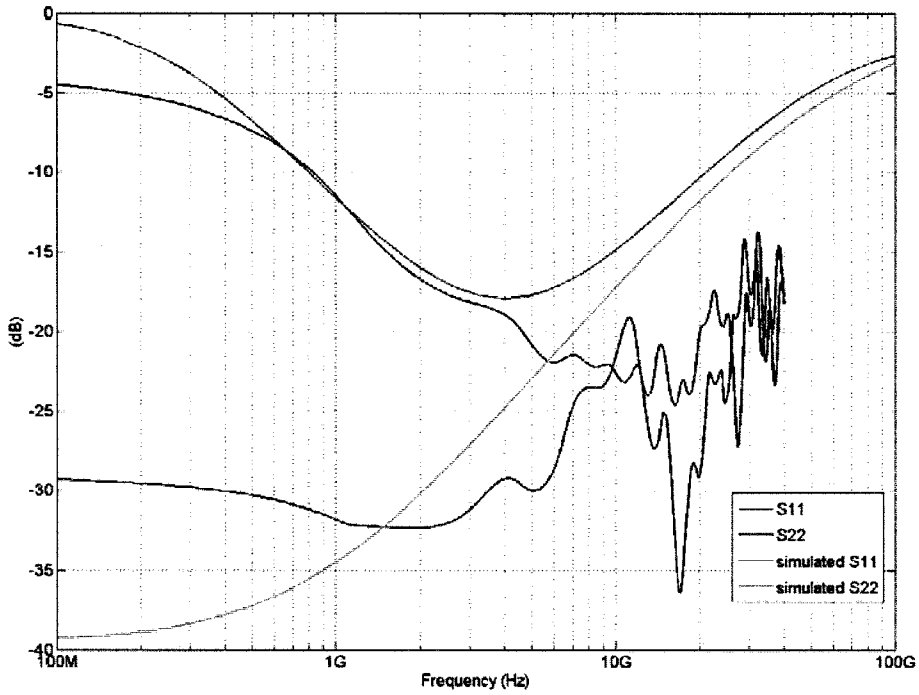


Figure 44 S_{11}/S_{22} Measurements for Delay Line (VNA)

6.2.2 Test Results Using the Signal Generator and Spectrum Analyzer

This chapter presents the measured results for which a signal generator applied the input signal (a 0 dBm input), and the output was measured using a spectrum analyzer. Measurements were recorded from the spectrum analyzer display (by hand), one frequency at a time (therefore the number of data points that could be measured was limited). The following plots show the results of the power gain; Figure 45 displays the results for the single delay cell, and Figure 46 displays the results for the tapped-delay-line. As was done with the VNA, measurements were recorded for the delay and reference path to result in a de-embedded value.

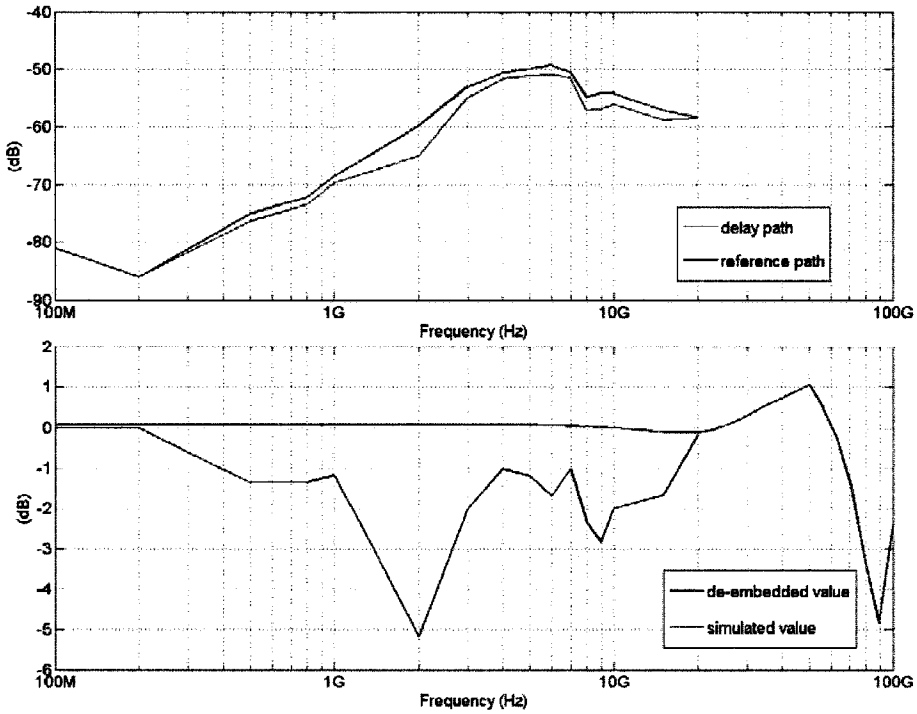


Figure 45 Power Gain Measurements for Single Delay (Signal Generator/Spectrum Analyzer)

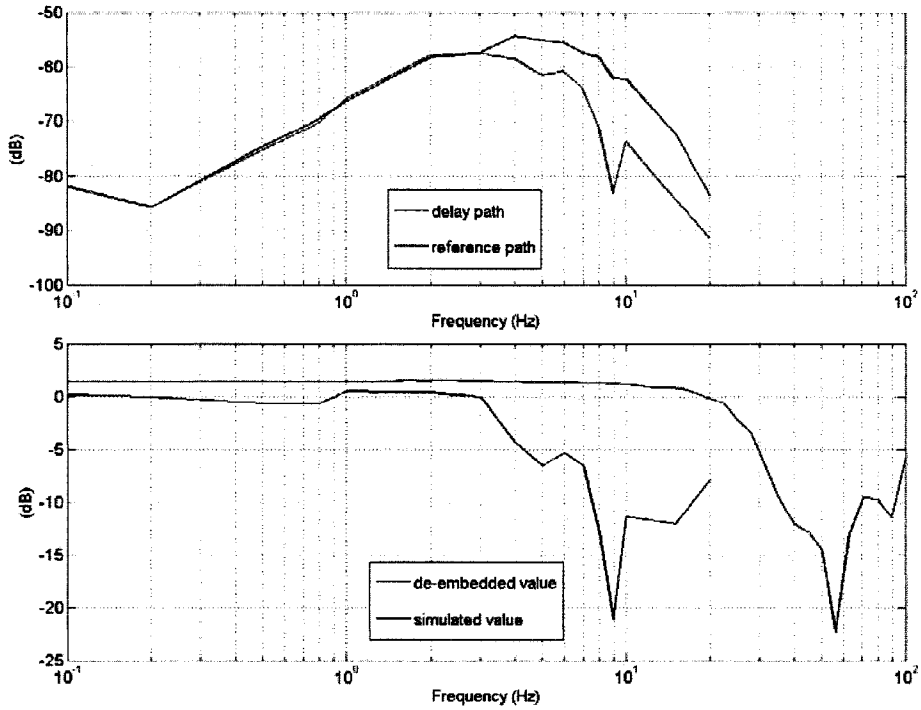


Figure 46 Power Gain Measurements for Delay Line (Signal Generator/Spectrum Analyzer)

6.3 Summary of Test Results

Presented in Table 12 is a summary of the test results. The simulated values of Section 5.5 are given, as well as the measured results using both the VNA and the signal generator with spectrum analyzer.

Table 12 Summary of Test Results

Measure	Single Cell / Delay Line	Simulated Value	Test Result	
			VNA	Signal Generator / Spectrum Analyzer
DC Gain	Single Cell	0.07 dB	0 dB	0 dB
	Delay Line	1.44 dB	- 2 dB	0 dB
Peaking	Single Cell	0.99 dB	None	None
	Delay Line	None	None	0.5 dB
Bandwidth (-3dB)	Single Cell	77.6 GHz	10 GHz	> 10 GHz ***
	Delay Line	24.0 GHz	4.5 GHz	3.5 GHz
Min/Max Delay (0-20 GHz)	Single Cell	6.83 / 8.02 ps	-21 / 25 ps *	
	Delay Line	144 / 152 ps	150 / 300 ps **	

* Within 1-10 GHz

** Within 0-10 GHz

*** Ignoring the notch at 2 GHz

6.4 Discussion

As can be seen from the previous subsections, there were a number of discrepancies between experimental and expected (simulated) results. Several factors have been identified which could lead to such differences. These factors include:

1. The on-chip current mirror for biasing all current sources had a floating source/bulk
2. Due to resistance in the test setup, on-chip supply voltages could not be verified
3. High power densities likely led to high operating temperatures and temperature gradients
4. Pattern fill could not be excluded from metals 1 to 5
5. There was too much attenuation in the signal path; as a result, crosstalk dominated at frequencies above 10 GHz
6. De-embedding involved taking a small difference from comparatively large

measurements; this resulted in poor measurement accuracy

7. It is suspected that the AC coupling capacitors between the input buffer and the tapped-delay-line may have failed (their oxides broke-down)

This section discusses these factors and how they are related to DC biasing, low-frequency results, high-frequency results, and the differences between single delay cell measurements and tapped-delay-line measurements. The simulation model is then altered based on these factors, and the updated simulation results are compared to the test measurements of the tapped-delay-line.

6.4.1 DC Biasing

One of the major sources which led to difficulties in recreating simulated conditions in the testing laboratory was a missing source/bulk connection. This was a diode-connected NMOS transistor, which acted as a current mirror to generate the VBIAS signal. This voltage is what set the values of all on-chip current sources (input buffer, delay cell, multiplexer/output driver). Although the source and bulk were tied together, they were floating rather than being tied to VSS. Before the prototype design was sent for fabrication, all required physical verification checking was performed and passed, including layout versus schematic (LVS). Obviously, LVS should not have passed due to the missing connection, and therefore the source of this problem was investigated. It was discovered that the chip guard ring, which is basically a wall of metal from substrate to top-metal that wraps around the perimeter of the chip, is what caused this problem. The chip guard ring uses a special type of substrate contact called 'contact bar'; it is the same material as a regular contact, but it is placed as one continuous contact around the entire chip. Due to an error in the LVS connectivity rules, it causes Assura to no longer differentiate between a connection to VSS and a connection to the substrate. Therefore, in the case of the current mirror, the source was connected to the bulk (substrate), and therefore LVS passed.

The result of this floating source/bulk is that there is approximately 500 Ω to 1 KΩ of resistance through the substrate to the closest VSS substrate connection (20 μm

away). In order to still be able to test, a voltage was applied to the IBIAS pad rather than a current. Although it allowed for measurements to be taken, this practice lacked both accuracy and precision. The effective gate voltage (V_{GS}-V_T) of current sources was designed to be very small in order to save voltage headroom. By applying a voltage instead of a current to IBIAS, variations in process, voltage, and temperature had a large effect on the current being sourced. Any variation from the nominal process meant the devices would not provide the same current as in simulation (for the same VBIAS). Perhaps the most problematic factor affecting current sources was temperature. Without changing anything in the test setup, relatively large fluctuations in on-chip current consumption could be observed over just a couple of minutes. In addition to affecting V_T and channel mobility, changes in temperature also affected V_{GS}. Due to resistance in the off-chip test setup (cables and die probes), the on-chip voltages of power supplies varied significantly with current. Applying a voltage from off-chip meant that its value was relative to the off-chip ground, not the on-chip ground (VSS). Therefore, even with a constant gate voltage applied, V_{GS} varied with current consumption.

Unfortunately, there wasn't a direct way to measure the on-chip voltage supplies (VDD, VDD2, and VSS). Due to the amount of current being consumed, if there was just 1 Ω of resistance in each of the VDD and VSS off-chip paths (cables and probes), the on-chip VDD-VSS headroom would be 0.7 V rather than 1.2 V. This problem, combined with the VBIAS controlled current sources, made it difficult to establish the proper DC biasing conditions. To aid in establishing the proper operating point, the VDC_OFFSET pad was connected to a voltmeter to measure the DC output voltage of the 9th delay cell in the tapped-delay-line. At proper DC operating conditions, this voltage is meant to be equal to 1.0 V. This voltage, along with I(VDD) and I(VDD2) were used to set VBIAS, VDD, and VDD2 in an attempt to get the DC biasing as close to what was designed for as possible. The final values used for testing were VDD = 1.5V, VDD2 = 2.4V, and VBIAS=0.4 V.

6.4.2 Low-Frequency Results

In addition to affecting current sources, changes in temperature had a significant impact

upon all other circuit elements. Figure 47 shows simulated S_{21} versus temperature for low-frequency (100 MHz), with nominal process and bias voltages, except that VRES is set to 1.2V. It can be seen that the de-embedded gain of the 18-tap delay line drops off by 4.25 dB for every 10° increase in temperature. The prototype had a relatively high power density, consuming 0.4 Watts in 1 mm^2 of chip space. Therefore, it is assumed that the average on-chip temperature would be much higher than the ambient temperature of the laboratory due to self-heating. For testing purposes, loose die were stuck to a glass slide with heated wax. Although wax and glass have very low thermal conductivities, they are not as low as air (0.25 W/m/°C for paraffin wax and 0.93 W/m/°C for glass, versus 0.025 W/m/°C for air). Therefore, it is expected that the main path of heat conduction was through the substrate, wax, and glass slide to the chuck of the die probing station. In retrospect, it would have been highly advantageous to have replaced the wax and glass slide with an apparatus that would act as a heat sink, and therefore lower the on-chip temperature.

In order to achieve a DC gain close to unity during testing, the value of VRES was increased from the nominal value of 0.5 V to the maximum value of 1.2 V (same as VDD). This effectively turns off the PMOS transistors in the delay cells, and gives the delay cells their maximum load resistance value. It is thought that this increased load was necessary due to increased temperature, which would lower the transconductance of the differential pair. From Figure 47, it can be seen that at a temperature of 104°, the de-embedded DC gain value of -2 dB would match that of the VNA measurements (Figure 40); similarly, at a temperature of 98°, the de-embedded DC gain value of 0 dB would match that of the Signal Generator with Spectrum Analyzer measurements (Figure 46).

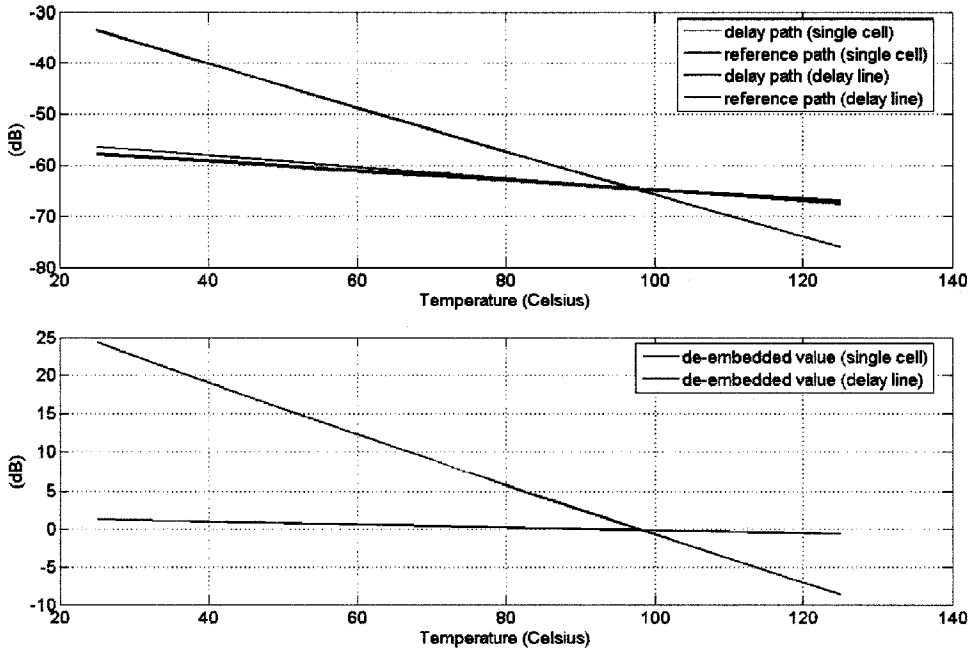


Figure 47 Simulated S_{21} versus Temperature for Low-Frequency (100 MHz) and Max VRES

Although it can be expected that the average temperature would have risen, it would not be uniform across the chip due to localized hot spots having higher than average power densities. For example, a single delay cell consumes 8 mW of power, and the buffer that serves as its tapped-load consumes 4.8 mW of power. However, the 1st and 18th delay cells have a multiplexer/output buffer stage, consuming 28.8 mW of power, adjacent to them in place of the simple tapped-load of the other cells. It is therefore expected that the local temperature would be higher for the 1st and 18th delay cells than other cells. Also, the 1st delay cell is next to the input buffer - the final stage of the input buffer has a power density of approximately 25.7 W/mm^2, versus 2.56 W/mm^2 for a delay cell. Not only would there be a difference in temperature between the first and last delay cells, but also between the first and last multiplexer/output driver circuits. This temperature gradient could explain why measurements of the two reference paths are so different. Figure 48 shows the S_{21} measurements of the reference paths for single cell and delay line de-embedding. At low-frequency, S_{21} of the delay line reference path was measured to be 2 dB lower, even though these paths are identical (with the exception of the transmission

line, which should actually make S_{21} of the delay line reference path 0.2 dB lower).

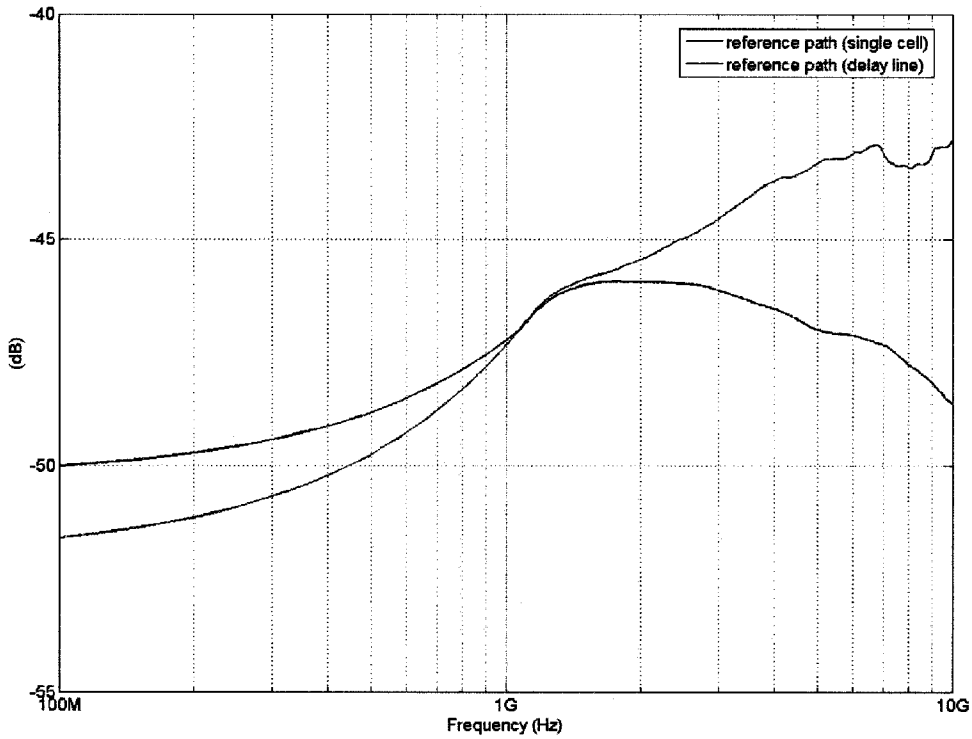


Figure 48 S_{21} Comparison of Reference Paths

6.4.3 High-Frequency Results

In order to ensure that a microchip will maintain its chemical mechanical planarization (CMP) integrity, a minimum degree of uniformity across all layers of its construction is necessary. This is done after a chip's layout is complete by filling extra space with pattern fill. In the case of the IBM 8RF-DM process, the pattern fill for metals 6, 7, and 8 are added by the designer, and the pattern fill for layers N+ (diffusion), polysilicon, and M1-M5 are added by the manufacturer. Typically, exclude layers are available to the designer to block pattern fill in areas that would be sensitive to the extra capacitance added. Originally, these exclude layers were added to all circuits and interconnect in the testchip's signal path. Unfortunately, just days before the tapeout deadline it was discovered that exclude layers, other than those for blocking N+ (diffusion) and polysilicon, were only available internally to IBM, and therefore they had to be removed.

The result was that M1-M5 pattern fill was added to all areas of the prototype during fabrication. This has the effect of dramatically increasing parasitic capacitance. Figure 49 is a picture taken under a microscope showing the pattern fill on metal 5. In the picture, the four stacked-inductors, the routing for the differential pair between the inductors, and the vertically-running signal lines can be seen. All of the small squares in the picture are metal 5 pattern fill. Given that the inductor track widths are 1.9 μm wide, it can be seen that the metal fill squares are placed quite close to the existing structures. Similar pattern fill was placed on the lower layers as well, but with smaller spacing. Shown in Figure 50 is a zoomed-in picture of the same delay cell.

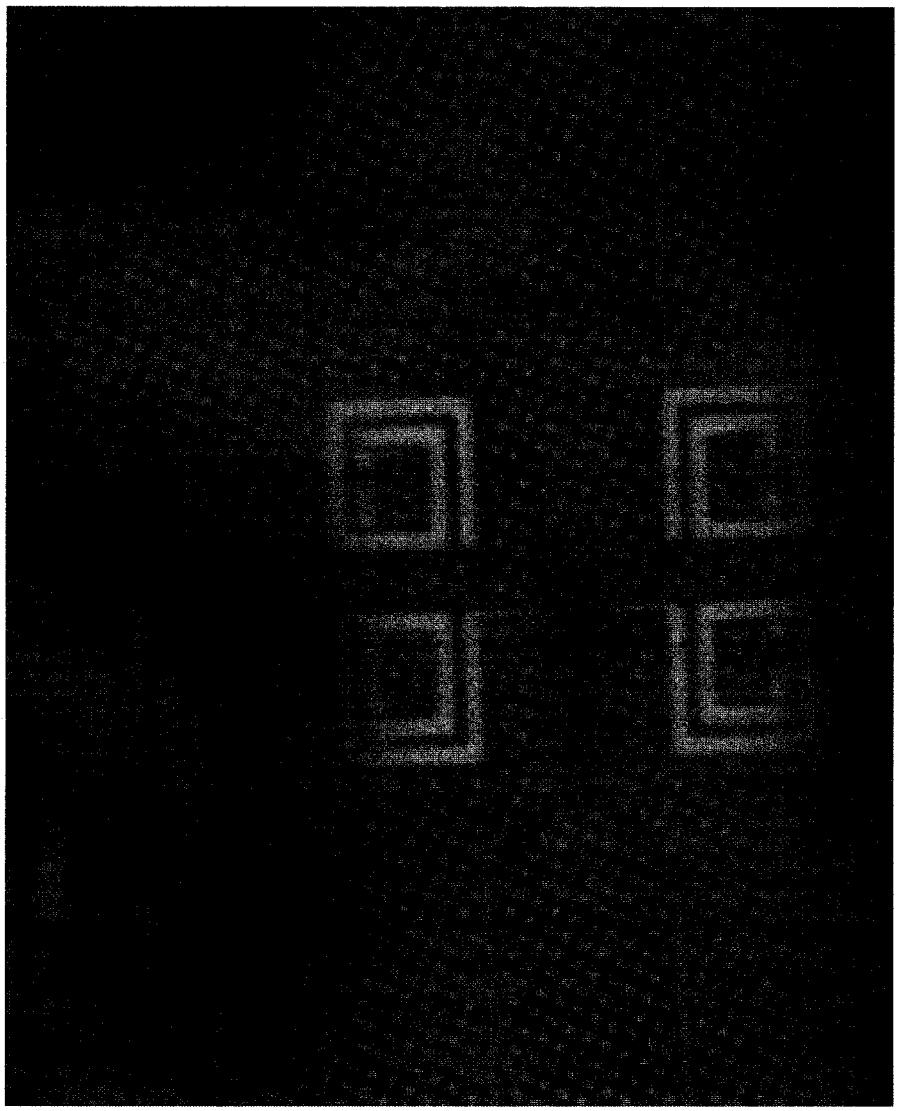


Figure 49 Picture of Metal 5 Pattern Fill in Delay Cell

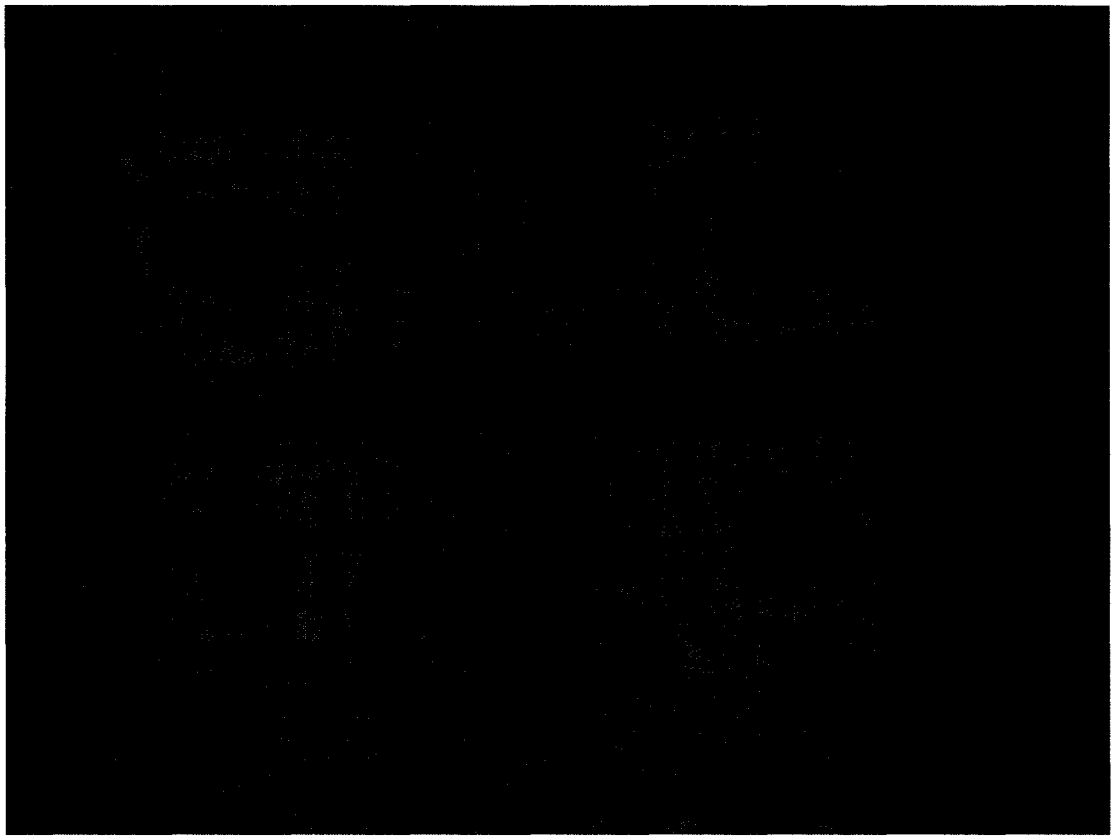


Figure 50 Picture of Metal 5 Pattern Fill in Delay Cell (Zoom-In)

Unfortunately, access to the post-pattern-filled layout could not be granted; however, the pattern fill layout design rules are released. Using a parallel-plate capacitance model for approximate values, it was calculated (depending on the coupling interconnect layers involved) that parasitic capacitance could increase by a multiplying factor varying between 1.65 and 4.0. When compared to the actual pattern fill, these numbers would be a pessimistic approximation, as the model used assumes that the metal fill blocks are placed in a straight line. Automated metal fill placement is typically staggered (across different layers and within the same plane), in order to reduce capacitance.

It is expected that this capacitance would have a dramatic effect on the inductors. As the inductors are four-level stacked-inductors, metal fill was placed on the outside and inside of all segments. It was also placed under the inductors on metal 1, which was purposely

left empty in order to reduce capacitance to the substrate (metal 2 was the bottom layer of the inductors). Not only does it add capacitance (to the substrate, and between metal segments), but it lowers inductance, increases losses due to eddy currents in metal segments and in the substrate, and lower self-resonant frequencies [29]. Due to the extra capacitance, the VCAP voltage (which controls the delay cell varactors) was set to 1.2V for test measurements. This has the effect of lowering capacitance in the cell by 6 fF.

Another problem that caused difficulties in testing is crosstalk. Due to the large amount of attenuation from input to outputs of the testchip, signal feed-through on a parallel path became a problem. This parallel path is capacitive in nature; therefore its effect becomes more significant with frequency. Beyond a certain frequency, the signal strength of the feed-through signal at the output becomes stronger than that of the on-chip signal path. In order to find these frequencies at which crosstalk dominates, S_{12} measurements were made and compared to the S_{21} de-embedding measurements, shown in Figure 39 and Figure 40 for the single delay cell and the tapped-delay-line, respectively. These S_{12} measurements are identical for reference and delay paths, and given that simulated S_{12} of the active signal paths was simulated to be much smaller, it can be assumed that the S_{12} measurements represent crosstalk. The point at which S_{12} becomes as strong as either S_{21} measurement (delay path or reference path) is the point at which crosstalk begins to dominate, and measurements beyond this frequency become invalid. For both the single delay cell and the delay line measurements, this frequency was found to be 10 GHz (the occurrence of the same frequency for both signal paths is just a coincidence).

6.4.4 Differences between VNA Measurements of Single Cell and Delay Line

When de-embedded test measurements are compared between the single delay cell and the 18-tap delay line, discrepancies can be seen. Values for the tapped-delay-line gain and group delay should be 18 times that of the single delay cell, but this is not the case. Shown in Figure 51 are plots of S_{21} and group delay, comparing the single cell measurements to the delay line measurements divided by 18 (measurements taken from VNA). From the plots it can be seen that the scaled delay line measurements (divided by

18) agree much more closely to simulated values than the single cell measurements. One obvious difference is the single cell S_{21} notch centered at 2 GHz is not seen in the delay line measurement. The S_{21} gain of the single cell rolls-off just before 10 GHz, whereas the delay measure does not. Given that 18 cascaded delay cells had a bandwidth of 4.5 GHz, it is expected that the bandwidth of a single cell would be well above 10 GHz. Comparing the group delay, it can be seen that the delay line measurement is much smoother, and is fairly close to the simulated value; the single cell measurement is very jagged, with values above and below zero.

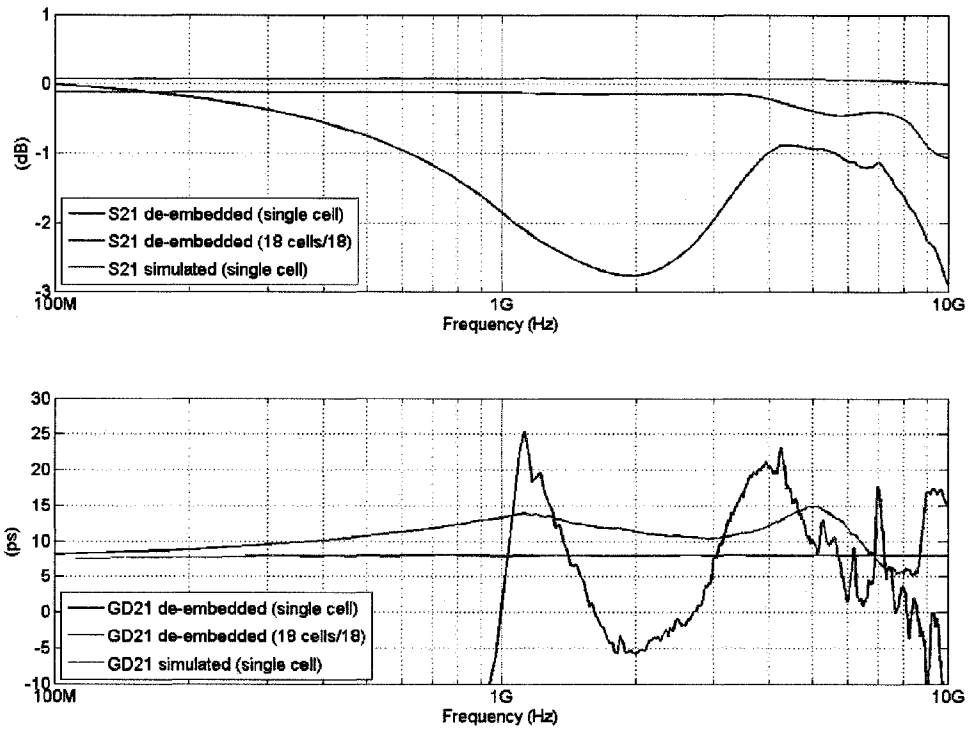


Figure 51 S_{21} and Group Delay Measurements: Comparing Single Cell to Delay Line Divided by 18

There are a few possible factors that may help to explain these differences. One possibility is that due to temperature and pattern fill effects (especially on the peaking inductors of the 2nd stage), the input buffer's conversion to a differential signal is much worse than was simulated in Section 5.2. The effect of the signal asymmetry would be seen at the output of the 1st multiplexer/output driver; the output is a single-ended signal, and the delay path has one extra inverting stage (the delay cell) more than the

reference path. If the (single cell) reference path and delay path outputs are treated as single-ended signals, the reference path output would predominantly be composed of the positive output of the input buffer, while the delay path output would be predominantly be composed of the negative output of the input buffer. Therefore, the notch at 2 GHz and the 10 GHz roll-off in the single cell de-embedded S_{21} result could be due to the difference in output signals at the input buffer. This would also largely affect group delay measurements.

The reason that this effect wouldn't be as pronounced in the delay line measurements is that the asymmetry in the differential signal gets smoothed over the 18 delay cells for the delay path measurement, and over the transmission line for the reference path measurement. Additionally, this delay path measurement contains 20 inverting stages from the input buffer, and the reference path measurement contains 2 inverting stages. As these are both even numbers of stages, if there was still a skew in the differential signals, both would predominantly be based upon the positive output of the input buffer.

Group delay measurements for the single cell and the delay line were given in Figure 41 and Figure 42. As with the S_{21} measurements, group delay was de-embedded by taking measurements of two paths, and taking the difference. Although the de-embedded result for the delay line was not ideal, it was at least fairly close to the expected result. The de-embedded result of the single delay cell does not resemble the expected value. The difference in the validity of these measurements is mainly due to the absolute values of the measurements taken. For the delay line, a reference value as high as 1000 ps was used to measure an expected value of 150 ps. Similarly, for the single delay cell a reference of 1000 ps was used, but to record an expected difference of just 8.33 ps. The difference is too small compared to the absolute measurement values. Further complicating reliability is that to record this data on the VNA, 40 measurements were taken and averaged, taking approximately 10-15 minutes. Over this time, temperature and current could shift considerably.

Another possible reason for the differences between single cell and delay line measurements is that the AC coupling MIM capacitors between the input buffer and the

delay line are suspected of having failed (oxides have broken-down, causing a large amount of leakage). Comparing the VNA S_{21} measurements (Figure 39 and Figure 40) and the signal generator/spectrum analyzer power gain measurements (Figure 45 and Figure 46), there is a significant difference in the slopes of the curves at low-frequency. S_{21} of the VNA is almost flat, while the power gain of the signal generator/spectrum analyzer slopes up steeply with frequency.

For these measurements, S_{21} is defined as incident output power divided by incident input power. The power gain using the signal generator/spectrum analyzer is defined by incident output power divided by the signal generator power that would be provided with a matched input. These measurements are only equivalent if input and output ports are matched. However, although the output of the prototype is matched, the input is not due to the AC coupling MIM that was placed before the 50Ω matching resistor. In the power gain measurements, the output power from the spectrum analyzer was measured and divided by an input power of 0 dBm. Due to the mismatched input, the actual input power from the signal generator is only a small fraction of this value at low frequencies. It should be noted that although the power gain measurements taken with the signal generator/spectrum analyzer are not an accurate at low frequency, the de-embedded results are (the error in input power is common for both paths).

Therefore, it is expected that the effect of the input AC coupling MIM capacitors would not be seen in the S_{21} measurements, but would be seen in the power gain measurements. However, the other set of AC coupling MIM capacitors (after the input buffer) should be seen in both S_{21} and power gain measurements. As there does not seem to be any evidence of AC coupling in S_{21}, but there is in S_{11} and in power gain measurements, it is thought that the AC coupling MIM capacitors before the input buffer are functioning correctly, but the AC coupling MIM capacitors after the input buffer have failed, or suffer from severe leakage. The cause of this failure is not known, as they should be operating within allowed voltage ranges. However, it may somehow be due to their connection to the high current 3rd input buffer stage, perhaps a transient issue during power-up, or an issue related to the high temperature that is expected in that area.

The failure of these MIM capacitors does not have any effect on the input buffer, but it does affect circuitry directly connected to the other side of the capacitors. The DC voltage at the output of the input buffer becomes the DC bias for the 1st delay cell, and the reference path buffer in each of the multiplexer/output driver circuits. This voltage was meant to be 1.0 V, but now becomes 1.27 V. This has the effect of increasing current in the 1st delay cell, and in the reference path buffers of the multiplexer/output driver circuits (due to finite output impedance of the current sources). Although current increases in the 1st delay cell, the increased gate voltage (and thus increased source voltage) pushes the differential pair transistors to the boundary between triode and saturation regions. This causes the transconductance (and therefore gain) to drop; it also dramatically reduces the input linear range, although this is a figure of merit that was not tested for. Simulation showed that this effect does not occur in the reference path buffer portion of the multiplexer/output driver circuits; although current increases slightly, the transconductance remains the same. In setting the DC bias voltages, the input buffer would also pass the DC offsets at its output to the inputs of the 1st delay cell and buffer circuits.

Another effect of the failed coupling capacitors is that their failed characteristics would not be identical. It is not likely that this would create any additional DC offset for the 1st delay cell or buffers, as these nodes would be higher impedance (due to high-resistance biasing resistors) than the leakage from the input buffer. However, at mid to high frequencies, when the capacitive impedance becomes comparable to the impedance due to leakage, offsets in signal levels could occur. The effects of the offsets would be the same as those discussed for the asymmetrical single-ended to differential signal conversion of the input buffer.

6.4.5 Updating the Simulation Model to Match Test Measurements

In order to demonstrate some of the topics discussed in this chapter, S-parameter simulations were performed in order to create a model that matches the VNA measurements for the tapped-delay-line. As the single-cell measurements are regarded as being invalid when compared to expected values (based on simulation and delay-line

measurements), only the delay-line is simulated and compared to measurements.

Changes made to simulation model:

- Temperature = 101° C
- VRES = 1.2 V (value used for testing)
- VCAP = 1.2 V (value used for testing)
- Extra capacitance added to delay cell (total of 7.5 fF/delay cell)
- 10 Ω resistors placed in parallel with AC coupling MIM capacitors at input buffer output to model oxide breakdown

The results of this simulation, along with the VNA S_{21} measurements for the 18-tap delay-line and are shown in Figure 52. Although the purpose of this simulation was to find a model which more closely resembled the measured results, the modifications made to the model are meant to give just an approximation. There are many possible variations which could have led to the results that were measured, including variations in variables that were not altered here, such as VDD, VDD2, IBIAS, process, temperature gradients, and DC offsets from the input buffer. An important factor that was ignored in the updated model was the effect of metal fill on the inductors (other than adding extra shunt capacitance). Due to the density and proximity of the metal fill, it is likely that the characteristics of the inductors would have changed substantially, and could be the dominant factor that altered high-frequency measurements.

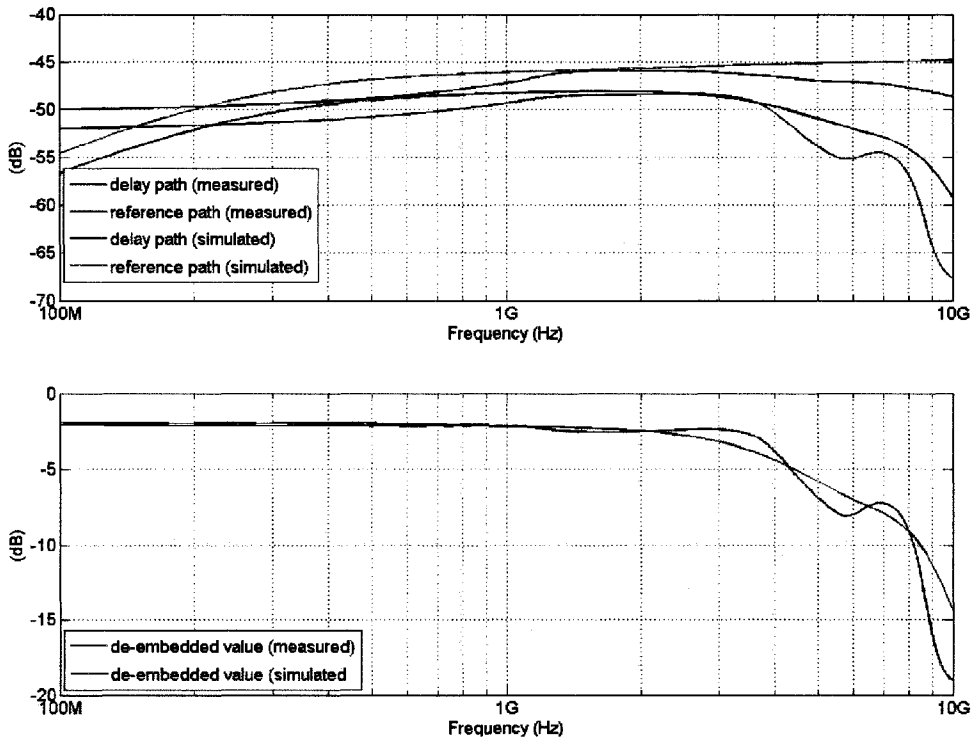


Figure 52 S_{21}: VNA Measurements versus Updated Simulation Results

Comparing to the original S_{21} reference path and delay path simulations of Figure 29, these simulations come much closer to approximating the measured low-frequency AC coupling effect. The original simulations showed an attenuation of 20 dB at 100 MHz due to coupling capacitors, versus 8 dB in the new simulation model, versus 4 dB in measurements. Due to the DC biasing being set by the input buffer, the 1st delay cell has a DC gain of -1.4 dB (-0.04 dB for the other delay cells). Therefore, the temperature for the simulation was reduced from 104° to 101° for the de-embedded DC gain to match. Cell capacitance was added to result in a 4.5 GHz bandwidth to match that of the de-embedded measured bandwidth.

Chapter 7 Conclusions

7.1 Conclusions from this Work

This work presents a delay cell for linear FFE operating at a data rate of 40 Gb/s. The delay cell uses compact stacked-inductors to achieve small silicon area and high bandwidth that can be maintained over many cascaded stages. Tuning capabilities were added to the delay cell, making it adaptable to variations in process, voltage, and temperature. The delay cell was designed and simulated in a CMOS 0.13 μm process. A prototype was created that used 18 of the delay cells cascaded with assumed multiplier loads to emulate the tapped-delay-line of an 18-tap FFE with T/3 tap spacing.

Test results of the prototype showed major discrepancies when compared to simulation results. Many of the factors that led to these differences were identified and discussed. Establishing the proper DC biasing during testing proved to be extremely difficult, due to the floating current mirror and the unknown voltages of on-chip power supplies. Self-heating in terms of average temperature and temperature gradients also affected testing. Due to a lack of voltage headroom for the delay cell current source, tuning capabilities did not meet specifications (as shown in corner simulations). Also, the prototype was designed such that each delay cell would have the same tuning voltages applied, making the delay-line tuning susceptible to temperature and process gradients.

The unavoidable placement of metal fill caused many problems related to the test results. It is expected to have significantly added parasitic capacitance to all signal lines and signal processing circuits. Metal fill was also placed inside, outside, and underneath the custom-designed stacked-inductors, resulting in more capacitance, increased eddy current induced losses, and lower inductance. These inductors were used in the delay cell, where it's thought they caused a reduction in bandwidth; similar inductors were also used in the input buffer, where it's thought that high-frequency offsets were created in the single-ended to differential conversion (in addition to reduced bandwidth). It was shown in the experimental results of Section 6.1 that when metal fill exclusion is used, the outlined method of inductor design and modeling yields very good agreement between simulation

and measurement.

Other problems were encountered with the de-embedding test methodology that was used. The combination of high attenuation in the de-embedding circuitry and close proximity of the input and output die probes caused crosstalk to dominate at frequencies above 10 GHz. This added to the difficulties in characterizing the single delay cell, which given all of the problems affecting high frequency operation, still likely had a bandwidth well above 10 GHz. The method of taking a small difference from large measurements of group delay proved to cause issues of precision. Not only did the use of this method amplify the finite accuracy that the VNA has in measuring the slope of phase change (group delay), but the measurements had to be averaged over long periods of time during which on-chip currents and temperature drifted.

Test results showed noticeable differences between the single delay cell and the 18-tap delay-line measurements. It is thought that this is at least partly due to high-frequency offsets in the differential output of the input buffer. Also, evidence was given to suggest that the MIM capacitors following the input buffer were blown (or severely leaking), causing the first delay cell (used for single cell characterization) to operate differently from the other delay cells.

These factors affecting the prototype testing were related to issues of fabrication, CAD software tools, and test circuitry and methodology, not to the delay cell design itself. Therefore, the measured results of the prototype do not serve to invalidate the delay cell as a useful building block of 40 Gb/s linear equalization.

7.2 Summary of Contributions

Contributions to the knowledge of serial data equalization were made through the presentation of a novel delay cell architecture for 40 Gb/s linear FFE. A combination of active and passive devices allowed the proposed architecture to possess many of the properties desirable for an FFE delay cell, such as small area, constant group delay versus frequency, unity-gain signal amplitude, no amplitude peaking, large delay-bandwidth product across many cascaded stages, relatively low power consumption (for an

active implementation), tuning capabilities, and the same DC bias level between input and output. Equations describing the amplitude, phase, and group delay response of the delay cell were provided. Additionally, simplified equations and design steps were provided to aid in the design of such a delay cell. It was demonstrated that 18 taps of a CMOS FFE delay-line could be implemented to provide 6 symbols of ISI coverage at a data rate of 40 Gb/s.

The delay cell also demonstrated how the use of compact stacked-inductors can be used to extend bandwidth, reduce power, or reduce area. Although this type of inductor has been around for many years, its use is still not widespread. The inductors that are provided in technology design kits are typically very large in size in order to reduce parasitic resistance. It was shown in this work that by using a low-Q (higher resistance) stacked-inductor, inductor area was reduced by 55 times when compared to the minimum size inductor from the design kit, having the same inductance value. This equates to a savings of 113,000 μm^2 per delay cell (the delay cell size in this work is just 3120 μm^2). This estimate of area savings includes the four inductors, and the spacing between inductors and to other devices (this spacing is calculated as 8 times the inductor turn spacing - the same ratio that was used in the delay cell layout).

7.3 Future Work

Future work would involve re-testing the loose die, but with the addition of a heat sink to allow for testing with junction temperatures close to room temperature. De-embedding could be improved by implementing another prototype in a BiCMOS process, allowing for the use of bipolar transistors to reduce attenuation in the de-embedding circuitry, while still using CMOS for the delay cell itself. For more agreeable measurements, choosing a process that allows for metal fill exclusion would also be necessary.

Design of a multiplier could allow for the construction of the entire FFE filter. A major design challenge of implementing an 18-tap FFE with a transversal filter architecture would be to achieve the required bandwidth at the summing node (see Figure 5). The possibility of using a traveling-wave architecture (see Figure 6) could be explored to ease

the difficulty in meeting the bandwidth specification, but at the cost of higher power consumption and larger area.

Improvements to the delay cell itself could also be explored. Shown in Figure 53 is one such improvement. This architecture includes the addition of two extra features not included in the delay cell of this work: extra series peaking inductors placed above the differential pair, and an additional tuning voltage vcap2 to tune extra varactors at the output. The additional inductors make the architecture similar to a high-frequency amplifier described in [26]. It allows for capacitance to become further distributed between the inductors, allowing the bandwidth to be extended. The addition of the vcap2 varactors was originally intended to be part of this work, but due to a limited number of pads on the prototype, the extra pad required could not be spared. The addition of these varactors adds an extra degree of freedom for high frequency tuning.

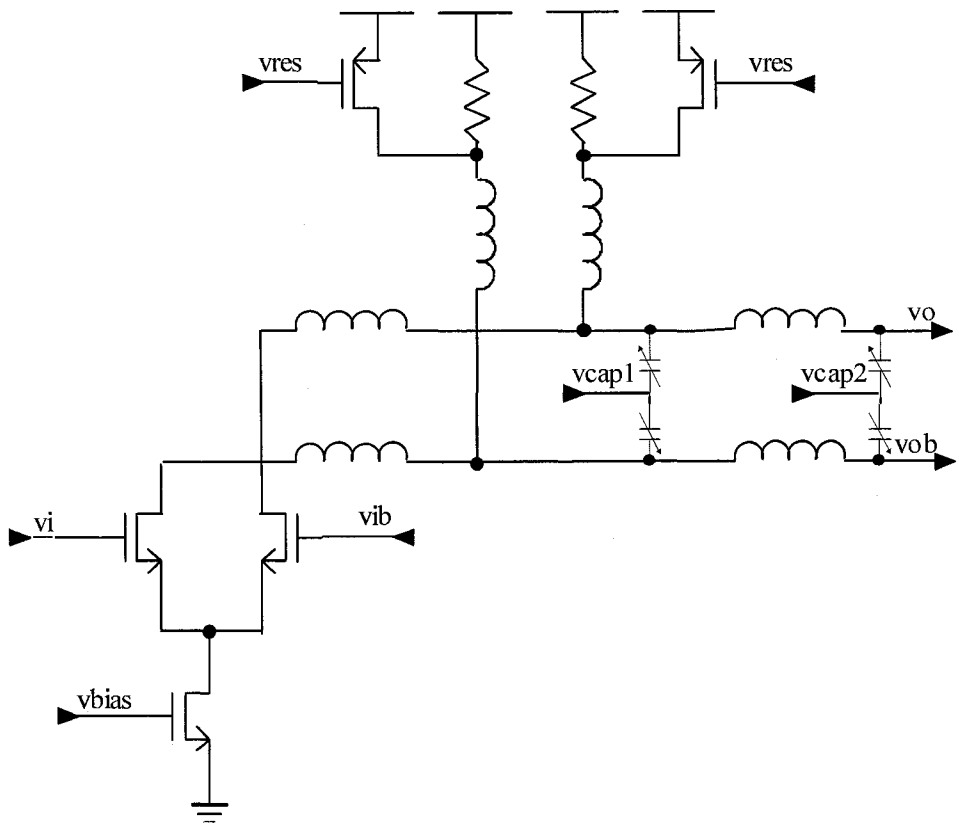


Figure 53 FFE Delay Cell with Shunt and Double-Series Peaking

Appendix A

The following is the technology file that was written for ASITIC, used to create the inductors used on the prototype. Due to the non-disclosure agreement of the technology, electrical and physical values have been removed (values replaced with "??"), but the overall structure is still shown.

```
; IBM 8RF_DM (0.13um CMOS) Technology file
; Travis Lovitt, January 2006

; based on the following construction:
;      - poly, M1, M2, M3, MQ, MG, LY, E1, MA
;      - BF on substrate (no pwell - low conductivity)

<chip>

      chipx = 256 ; dimensions of the chip in x direction
      chipy = 256 ; dimensions of the chip in y direction
      fftx =  512 ; x-fft size (must be a power of 2)
      ffty =  512 ; y-fft size
      TechFile = ibm_8rf_dm.tek
      TechPath = .
      freq = 10   ; frequency of operation
      eddy = 0

<layer> 0              ; substrate layer
      rho = ??         ; resistivity ohm-cm
      t   = ??         ; thickness um
        eps = ??       ; permitivity

<layer>     1                ; STI layer
      rho = ??
      t = ??
      eps = ??

<layer>     2                ; poly layer
      rho = ??
      t = ??
      eps = ??

<layer>     3                ; poly to M1 layer
      rho = ??
      t = ??
      eps = ??

<layer> 4              ; M1 oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 5              ; M1 to M2 oxide layer
      rho = ??
```

```
      t = ??
      eps = ??

<layer> 6                ; M2 oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 7                ; M2 to M3 oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 8                ; M3 oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 9                ; M3 to MQ oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 10               ; MQ oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 11               ; MQ to MG oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 12               ; MG oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 13               ; MG to LY oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 14               ; LY oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 15               ; LY to E1 oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 16               ; E1 oxide layer
      rho = ??
      t = ??
      eps = ??
```

```
<layer> 17              ; E1 to MA oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 18              ; MA oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 19              ; passivation oxide layer
      rho = ??
      t = ??
      eps = ??

<layer> 20              ; passivation nitride layer
      rho = ??
      t = ??
      eps = ??

<layer> 21              ; passivation polyimide layer
      rho = ??
      t = ??
      eps = ??

<layer> 22              ; air
      rho = ??
      t = ??
      eps = ??

<metal> 0               ; poly
        layer = 2       ; in which oxide layer
        rsh = ??        ; sheet resistance mOhm/sq
        t = ??          ; thickness
        d = 0                ; distance from bottom of layer
        name = poly
        color = orange

<metal> 1               ; M1
        layer = 4
        rsh = ??
        t = ??
        d = 0
        name = m1
        color = blue

<metal> 2               ;M2
        layer = 6
        rsh = ??
        t = ??
        d = 0
        name = m2
        color = cyan

<metal> 3
        layer = 8
```

```
        rsh = ??
        t = ??
        d = 0
        name = m3
        color = pink

<metal> 4               ; MQ
        layer = 10
        rsh = ??
        t = ??
        d = 0
        name = mq
        color = green

<metal> 5               ; MG
        layer = 12
        rsh = ??
        t = ??
        d = 0
        name = mg
        color = yellow

<metal> 6               ; LY
        layer = 14
        rsh = ??
        t = ??
        d = 0
        name = ly
        color = lightbrown

<metal> 7               ; E1
        layer = 16
        rsh = ??
        t = ??
        d = 0
        name = e1
        color = white

<metal> 8               ; MA
        layer = 18
        rsh = ??
        t = ??
        d = 0
        name = ma
        color = red

<via> 0                         ; poly to M1
        top = 1                 ; via connects up to this metal layer
        bottom = 0              ; via connects down to this metal layer
        r = ??                  ; resistance per via Ohm
      width = ??            ; width of via
        space = ??              ; min spacing between vias
        overplot1 = ??          ; min dist to bottom metal
        overplot2 = ??          ; min dist to top metal
        name = cont
        color = yellow
```

```
<via> 1                          ; M1 to M2
        top = 2                  ; via connects up to this metal layer
        bottom = 1               ; via connects down to this metal layer
        r = ??                   ; resistance per via Ohm
      width = ??         ; width of via
        space = ??               ; min spacing between vias
        overplot1 = ??           ; min dist to bottom metal
        overplot2 = ??           ; min dist to top metal
        name = v1
        color = lightbrown

<via> 2                          ; M2 to M3
        top = 3
        bottom = 2
        r = ??
        width = ??
        space = ??
        overplot1 = ??
        overplot2 = ??
        name = v2
        color = white

<via> 3                          ; M3 to MQ
        top = 4
        bottom = 3
        r = ??
        width = ??
        space = ??
        overplot1 = .01
        overplot2 = .01
        name = v1
        color = yellow

<via> 4                          ; MQ to MG
        top = 5
        bottom = 4
        r = ??
        width = ??
        space = ??
        overplot1 = ??
        overplot2 = ??
        name = vq
        color = purple

<via> 5                          ; MG to LY
        top = 6
        bottom = 5
        r = ??
        width = ??
        space = ??
        overplot1 = ??
        overplot2 = ??
        name = fy
        color = green

<via> 6                          ; LY to E1
        top = 7
```

```
        bottom = 6
        r = ??
        width = ??
        space = ??
        overplot1 = ??
        overplot2 = ??
        name = ft
        color = white

<via> 7                         ; E1 to MA
        top = 8
        bottom = 7
        r = ??
        width = ??
        space = ??
        overplot1 = ??
        overplot2 = ??
        name = f1
        color = red
```

Appendix B

The following is the inductor HSPICE optimization script that was used to curve fit the narrow band S-parameters to the unified broadband inductor model that was used in the delay cell.

```
*** L_292p_IBM.sp ***
* Travis Lovitt
* Mar/2006

* - SP parameters from Cadence
* - inductor '' used


.option acct nomod post=2
+ resmin = 1e-15
+ accurate

.net v(p2) vin rout=50 rin=50

vin p1  0 AC 1

L           p1    3       Ls
R           3       p2      Rs
Cox1        p1    1     Cox1
Cox2        p2    2     Cox1
Cs1     1           0       Cs1
Cs2     2           0       Cs2
Rs1     1       0       Rs1
Rs2     2       0       Rs2
Cp          p1      p2      Cp

.param
+ Ls  = OPT1(292p,2p,300p)
+ Rs  = OPT1(6.5,5,10)
+ Cox1      = OPT1(1f,1a,10f)
+ Cox2      = OPT1(1f,1a,10f)
+ Cs1 = OPT1(1f,1a,100f)
+ Cs2 = OPT1(1f,1a,100f)
+ Rs1 = OPT1(1K,100,100K)
+ Rs2 = OPT1(1K,100,100K)
+ Cp = OPT1(1f,1a,100f)

.AC data=measured optimize=opt1
+ results=comp1,comp2,comp3,comp4,comp5,comp6,comp7,comp8
+ model=converge
.model converge opt relin=1e-5 relout=1e-5 close=1 itropt=1000
cendif=0.01
.measure ac comp1 err1 par(s11m) s11(m)
.measure ac comp2 err1 par(s11p) s11(p)
.measure ac comp3 err1 par(s12m) s12(m)
.measure ac comp4 err1 par(s12p) s12(p)
.measure ac comp5 err1 par(s21m) s21(m)
```

```
.measure ac comp6 err1 par(s21p) s21(p)
.measure ac comp7 err1 par(s22m) s22(m)
.measure ac comp8 err1 par(s22p) s22(p)
.ac data=measured

.print z11(r) z11(i)
.print zin(1) zin(2)
.print par(s21m) par(s21p)
.print s21(m) s21(p)


.data measured
FREQ    s11m    s11p    s12m    s12p    s21m    s21p    s22m    s22p
100M  61.5m 1.4   939m  -0.106      939m  -0.106      61.5m 1.39
1G    63.3m 14    938m  -1.04 938m  -1.04 63.3m 14
10G   174m  58.2  921m  -9.91 921m  -9.91 173m  58.1
20G   311m  57.4  878m  -18.8 878m  -18.8 310m  57.2
40G   520m  46.9  767m  -33.4 767m  -33.4 520m  46.4
50G   599m  41.7  710m  -39.5 710m  -39.5 599m  41.1
.enddata
.param freq=1G,s11m = 0 , s11p = 0, s12m = 0, s12p = 0, s21m =0,
+s21p =0, s22m =0 , s22p = 0
.end
```

Appendix C

The following is a Matlab script that was used for de-embedding of inductor test structure measurements. The resultant plot is shown in Figure 37 of Section 6.1.3.

```
% cg_1004_ind_deembed_withSim.m
% ---------
% Travis Lovitt
% Nov 2005

% Summary
% -------
% File reads in S11/Z11/Y11-Parameter lab data for an inductor and it's
% de-embedding structures (open and short).  This de-embedding
% data is then used to mathematically remove open admittance and short
impedance from the inductor measurements.
% The inductance/resistance/quality factors are then
% calculated and plotted vs frequency.

clear all;
status = fclose('all');


% Location of raw measurement data
dir_ind = '/home/tlovitt/thesis/cg_1004_meas/ind_char/raw';
dir_ind_sim = '/home/tlovitt/thesis/cg_1004_meas/ind_char/sim_data';

% Measurements were split into 4 frequency ranges, each containing 201
linearily spaced frequencies:
freq1 = 50e6:(5e9-50e6)/200:5e9;
freq2 = 5.05e9:(10e9-5.05e9)/200:10e9;
freq3 = 10.05e9:(15e9-10.05e9)/200:15e9;
freq4 = 15.05e9:(20e9-15.05e9)/200:20e9;
freqs_50M_20G = [freq1 freq2 freq3 freq4];
freqs_50M_20G = freqs_50M_20G';

% Read-in S,Z,Y-params for IND/chip E7
S = [];Zre = [];Zim = [];Yre = [];Yim = [];
for n=[2 5 15 21]
    if n<10;
        FidS = fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'s.dat'));
        FidZre                                                          =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zre.dat'));
        FidZim                                                          =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zim.dat'));
        FidYre                                                          =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yre.dat'));
        FidYim                                                          =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yim.dat'));
    else
        FidS = fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'s.dat'));
        FidZre                                                          =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zre.dat'));
        FidZim                                                          =
```

```
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zim.dat'));
        FidYre                                                    =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yre.dat'));
        FidYim                                                    =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yim.dat'));
    end
    S_data =    fscanf(FidS,'%*g%*c %hg%*c %hg',[2 inf]);
    Zre_data =  fscanf(FidZre,'%*g%*c %hg%*c %*g',[1 inf]);
    Zim_data =  fscanf(FidZim,'%*g%*c %hg%*c %*g',[1 inf]);
    Yre_data =  fscanf(FidYre,'%*g%*c %hg%*c %*g',[1 inf]);
    Yim_data =  fscanf(FidYim,'%*g%*c %hg%*c %*g',[1 inf]);
    S = [S ; S_data'];
    Zre = [Zre ; Zre_data'];
    Zim = [Zim ; Zim_data'];
    Yre = [Yre ; Yre_data'];
    Yim = [Yim ; Yim_data'];
end
E7_IND = [freqs_50M_20G S Zre Zim Yre Yim];

% Read-in S,Z,Y-params for OPEN/chip E7
S = [];Zre = [];Zim = [];Yre = [];Yim = [];
for n=[11 6 16 22]
    if n<10;
        FidS = fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'s.dat'));
        FidZre                                                    =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zre.dat'));
        FidZim                                                    =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zim.dat'));
        FidYre                                                    =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yre.dat'));
        FidYim                                                    =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yim.dat'));
    else
        FidS = fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'s.dat'));
        FidZre                                                    =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zre.dat'));
        FidZim                                                    =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zim.dat'));
        FidYre                                                    =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yre.dat'));
        FidYim                                                    =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yim.dat'));
    end
    S_data =    fscanf(FidS,'%*g%*c %hg%*c %hg',[2 inf]);
    Zre_data =  fscanf(FidZre,'%*g%*c %hg%*c %*g',[1 inf]);
    Zim_data =  fscanf(FidZim,'%*g%*c %hg%*c %*g',[1 inf]);
    Yre_data =  fscanf(FidYre,'%*g%*c %hg%*c %*g',[1 inf]);
    Yim_data =  fscanf(FidYim,'%*g%*c %hg%*c %*g',[1 inf]);
    S = [S ; S_data'];
    Zre = [Zre ; Zre_data'];
    Zim = [Zim ; Zim_data'];
    Yre = [Yre ; Yre_data'];
    Yim = [Yim ; Yim_data'];
end
E7_OPEN = [freqs_50M_20G S Zre Zim Yre Yim];

%    Read-in    S,Z,Y-params    for    SHORT/chip E7
```

```
S = [];Zre = [];Zim = [];Yre = [];Yim = [];
for n=[12 7 17 23]
    if n<10;
        FidS = fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'s.dat'));
        FidZre =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zre.dat'));
        FidZim =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zim.dat'));
        FidYre =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yre.dat'));
        FidYim =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yim.dat'));
    else
        FidS = fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'s.dat'));
        FidZre =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zre.dat'));
        FidZim =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zim.dat'));
        FidYre =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yre.dat'));
        FidYim =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yim.dat'));
    end
    S_data =    fscanf(FidS,'%*g%*c %hg%*c %hg',[2 inf]);
    Zre_data =  fscanf(FidZre,'%*g%*c %hg%*c %*g',[1 inf]);
    Zim_data =  fscanf(FidZim,'%*g%*c %hg%*c %*g',[1 inf]);
    Yre_data =  fscanf(FidYre,'%*g%*c %hg%*c %*g',[1 inf]);
    Yim_data =  fscanf(FidYim,'%*g%*c %hg%*c %*g',[1 inf]);
    S = [S ; S_data'];
    Zre = [Zre ; Zre_data'];
    Zim = [Zim ; Zim_data'];
    Yre = [Yre ; Yre_data'];
    Yim = [Yim ; Yim_data'];
end
E7_SHORT = [freqs_50M_20G S Zre Zim Yre Yim];

% Read-in S,Z,Y-params for IND/chip E5
S = [];Zre = [];Zim = [];Yre = [];Yim = [];
for n=[3 8 18 24]
    if n<10;
        FidS = fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'s.dat'));
        FidZre =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zre.dat'));
        FidZim =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zim.dat'));
        FidYre =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yre.dat'));
        FidYim =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yim.dat'));
    else
        FidS = fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'s.dat'));
        FidZre =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zre.dat'));
        FidZim =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zim.dat'));
        FidYre =
```

```
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yre.dat'));
        FidYim                                                    =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yim.dat'));
    end
    S_data =    fscanf(FidS,'%*g%*c %hg%*c %hg',[2 inf]);
    Zre_data =  fscanf(FidZre,'%*g%*c %hg%*c %*g',[1 inf]);
    Zim_data =  fscanf(FidZim,'%*g%*c %hg%*c %*g',[1 inf]);
    Yre_data =  fscanf(FidYre,'%*g%*c %hg%*c %*g',[1 inf]);
    Yim_data =  fscanf(FidYim,'%*g%*c %hg%*c %*g',[1 inf]);
    S = [S ; S_data'];
    Zre = [Zre ; Zre_data'];
    Zim = [Zim ; Zim_data'];
    Yre = [Yre ; Yre_data'];
    Yim = [Yim ; Yim_data'];
end
E5_IND = [freqs_50M_20G S Zre Zim Yre Yim];

% Read-in S,Z,Y-params for OPEN/chip E5
S = [];Zre = [];Zim = [];Yre = [];Yim = [];
for n=[13 9 19 25]
    if n<10;
        FidS = fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'s.dat'));
        FidZre                                                    =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zre.dat'));
        FidZim                                                    =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zim.dat'));
        FidYre                                                    =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yre.dat'));
        FidYim                                                    =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yim.dat'));
    else
        FidS = fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'s.dat'));
        FidZre                                                    =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zre.dat'));
        FidZim                                                    =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zim.dat'));
        FidYre                                                    =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yre.dat'));
        FidYim                                                    =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yim.dat'));
    end
    S_data =    fscanf(FidS,'%*g%*c %hg%*c %hg',[2 inf]);
    Zre_data =  fscanf(FidZre,'%*g%*c %hg%*c %*g',[1 inf]);
    Zim_data =  fscanf(FidZim,'%*g%*c %hg%*c %*g',[1 inf]);
    Yre_data =  fscanf(FidYre,'%*g%*c %hg%*c %*g',[1 inf]);
    Yim_data =  fscanf(FidYim,'%*g%*c %hg%*c %*g',[1 inf]);
    S = [S ; S_data'];
    Zre = [Zre ; Zre_data'];
    Zim = [Zim ; Zim_data'];
    Yre = [Yre ; Yre_data'];
    Yim = [Yim ; Yim_data'];
end
E5_OPEN = [freqs_50M_20G S Zre Zim Yre Yim];

% Read-in S,Z,Y-params for SHORT/chip E5
S = [];Zre = [];Zim = [];Yre = [];Yim = [];
for n=[14 10 20 26]
```

```
    if n<10;
        FidS = fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'s.dat'));
        FidZre                                                          =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zre.dat'));
        FidZim                                                          =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'zim.dat'));
        FidYre                                                          =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yre.dat'));
        FidYim                                                          =
fopen(strcat(dir_ind,'/ind_meas_0',num2str(n),'yim.dat'));
    else
        FidS = fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'s.dat'));
        FidZre                                                          =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zre.dat'));
        FidZim                                                          =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'zim.dat'));
        FidYre                                                          =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yre.dat'));
        FidYim                                                          =
fopen(strcat(dir_ind,'/ind_meas_',num2str(n),'yim.dat'));
    end
    S_data =    fscanf(FidS,'%*g%*c %hg%*c %hg',[2 inf]);
    Zre_data =  fscanf(FidZre,'%*g%*c %hg%*c %*g',[1 inf]);
    Zim_data =  fscanf(FidZim,'%*g%*c %hg%*c %*g',[1 inf]);
    Yre_data =  fscanf(FidYre,'%*g%*c %hg%*c %*g',[1 inf]);
    Yim_data =  fscanf(FidYim,'%*g%*c %hg%*c %*g',[1 inf]);
    S = [S ; S_data'];
    Zre = [Zre ; Zre_data'];
    Zim = [Zim ; Zim_data'];
    Yre = [Yre ; Yre_data'];
    Yim = [Yim ; Yim_data'];
end
E5_SHORT = [freqs_50M_20G S Zre Zim Yre Yim];


%%% Read-in Simulation Data %%%
FidZre = fopen(strcat(dir_ind_sim,'/cg1004_Z11re_ind_sim_mod.dat'));
FidZim = fopen(strcat(dir_ind_sim,'/cg1004_Z11im_ind_sim_mod.dat'));

Zre_data_sim =  fscanf(FidZre,'%*g %hg',[1 inf]);
Zim_data_sim =  fscanf(FidZim,'%*g %hg',[1 inf]);
FidZim = fopen(strcat(dir_ind_sim,'/cg1004_Z11im_ind_sim_mod.dat'));
freqs_sim = fscanf(FidZim,'%g %*g',[1 inf]);



% Z11 Calculations - Deembed Inductor with OPEN/SHORT char
E7_Y11_IND = E7_IND(:,6)+E7_IND(:,7)*i;
E7_Y11_OPEN = E7_OPEN(:,6)+E7_OPEN(:,7)*i;
E7_Z11_SHORT = E7_SHORT(:,4)+E7_SHORT(:,5)*i;
E7_Z11_FINAL = 1./(E7_Y11_IND - E7_Y11_OPEN) - E7_Z11_SHORT;

E5_Y11_IND = E5_IND(:,6)+E5_IND(:,7)*i;
E5_Y11_OPEN = E5_OPEN(:,6)+E5_OPEN(:,7)*i;
E5_Z11_SHORT = E5_SHORT(:,4)+E5_SHORT(:,5)*i;
E5_Y11_SHORT                    =   E5_SHORT(:,6)+E5_SHORT(:,7)*i;
```

```
%E5_Z11_FINAL = 1./(E5_Y11_IND - E5_Y11_OPEN) - E5_Z11_SHORT;
E5_Z11_FINAL  =  1./(E5_Y11_IND  -  E5_Y11_OPEN)  -  1./(E5_Y11_SHORT  -
E5_Y11_OPEN);

% Solve for L, R, Q
E7_R = real(E7_Z11_FINAL);
E7_L = imag(E7_Z11_FINAL)./(2*pi*freqs_50M_20G);
E7_Q= abs(imag(E7_Z11_FINAL))/abs(real(E7_Z11_FINAL));

E5_R = real(E5_Z11_FINAL);
E5_L = imag(E5_Z11_FINAL)./(2*pi*freqs_50M_20G);
E5_Q= abs(imag(E5_Z11_FINAL))/abs(real(E5_Z11_FINAL));


% Solve for Simulation L, R, Q
R_sim = Zre_data_sim;
L_sim = Zim_data_sim./(2*pi*freqs_sim);
Q_sim = Zim_data_sim./Zre_data_sim;



% Plot L
figure(1);
subplot(211);
semilogx(freqs_50M_20G./1e9,E5_L/1e-12, 'r', 'linewidth', 2);
hold all;
semilogx(freqs_sim./1e9,L_sim/1e-12, 'b', 'linewidth', 2);
xlabel('Frequency (Hz)','FontSize',14);
ylabel('Ind (pH)','FontSize',14);
axis([0.1 20 800 950]);
grid;
legend('Inductance (Measured)', 'Inductance (Simulated)');
hold off;

% Plot R
 subplot(212)
 semilogx(freqs_50M_20G./1e9,E5_R, 'r', 'linewidth', 2);
 hold all;

 semilogx(freqs_sim./1e9,R_sim, 'b', 'linewidth', 2);
 xlabel('Frequency (Hz)','FontSize',14);
 ylabel('R (ohms)','FontSize',14);
 axis([0.1 20 20 35 ]);
 grid;
 legend('Resistance (Measured)', 'Resistance (Simulated)');
 hold off;
```

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