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A $\Sigma\cdot\Delta$ Frequency Discriminator Based Synthesizer

by

Walter T. Bax B. Eng.

A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfilment of the requirements for the degree of

Master of Engineering

**Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Carleton University
Ottawa, Canada**

December 1994

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A $\Sigma\Delta$ Frequency Discriminator Based Synthesizer

submitted by

Walter T. Bax B. Eng.

in partial fulfilment of the requirements for the degree of
Master of Engineering

Thesis Supervisor

Chair, Department of Electronics

Carleton University
December 1994

Abstract

The design and implementation of a new synthesizer architecture suitable for digital mobile radio applications is explored in this thesis. This architecture has several advantages over conventional high resolution fractional-N synthesizers currently used in these applications. The synthesizer is based on an oversampled $\Sigma\Delta$ frequency discriminator that directly converts the voltage-controlled oscillator (VCO) frequency to digital form. Further signal processing can then be performed digitally which eliminates many of the analog noise sources present in conventional fractional-N synthesizers.

Simulation models were developed to explore the effects of various parameters on the synthesizer phase noise and transient response. A discrete version of the synthesizer was realized and experimental testing validated the accuracy of the simulation models. Measured results show that the performance of this synthesizer architecture rivals that of conventional fractional-N synthesizers while being more suitable for monolithic integration.

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List of Symbols and Abbreviations

a_2	proportional gain
a_3	integral gain
AFC	automatic frequency control
AM	amplitude modulation
b	number of bits in comb filter
BiCMOS	bipolar and CMOS process
BW	PLL loop bandwidth
D/A	digital to analog converter
D	dynamic range of oversampled bitstream
DAS	direct analog synthesis
DDS	direct digital synthesis
DFT	discrete Fourier transform
DMD	dual-modulus divider
DSP	digital signal processing
ECL	emitter-coupled logic
FIR	finite impulse response
FLL	frequency-locked loop
FM	frequency modulation
FPGA	field-programmable gate array
GaAs	gallium arsenide
GMSK	gaussian mean shift keying
IF	intermediate frequency
IIR	infinite impulse response
k	comb filter order
K_B	Boltzman's constant

K_i	integrator gain
K_v	VCO sensitivity
$\mathcal{H}(f)$	single-sideband phase noise spectral density
N	decimation factor
n	divider modulus
OP-AMP	operational amplifier
PAL	programmable array logic
PCB	printed circuit board
PFD	phase-frequency detector
PLL	phase-locked loop
PM	phase modulation
QPSK	quadrature phase shift keying
RC	time constant
RF	radio frequency
$S_\phi(f)$	phase error spectral density
$\Sigma\Delta$	Sigma-Delta
S_n	noise power spectral density
SNR	signal to noise ratio
SR	slew rate
SSB	single sideband
S_v	frequency error spectral density
T	temperature
T_d	nominal divider output period
t_{PHL}	propagation delay from high to low
t_{PLH}	propagation delay from low to high
T_v	nominal VCO period
θ_e	phase error

UGBW	unity-gain bandwidth
VCO	voltage-controlled oscillator
VLSI	very large scale integration
Δv	D/A converter full-scale range
ω_n	PLL natural frequency
z^{-1}	discrete-time unit delay
ZOH	zero-order hold
ζ	PLL damping factor

Chapter 1

Introduction

The rapid growth in the use of personal communication devices operating in the gigahertz range has resulted in tremendous academic and industrial effort to develop technologies to fulfil the demanding specifications these systems require. Emerging technologies have steadily reduced the size and power requirements of these systems while increasing their operating frequencies to higher limits.

Current trends in communication standards favour digital modulation techniques (i.e. DECT etc.) over more conventional analog techniques (i.e. AMPS etc.). Digital communication techniques offer significant advantages in noise immunity and channel utilization efficiency. This provides the thrust for developing mobile digital radio transceivers that have the necessary performance while maintaining low power consumption and small size. Ongoing research has led to the development of various digital radio component architectures suitable for very large-scale integration (VLSI). In particular, research done on Sigma-Delta ($\Sigma\Delta$) fractional-N synthesizers provides partial motivation for this thesis [23].

This thesis examines a new synthesizer architecture proposed for digital mobile radio applications. This architecture has several advantages over the fractional-N type architectures currently used. The new synthesizer is based on an oversampled $\Sigma\Delta$ frequency discriminator in the feedback path which converts the frequency to digital form.

This results in a largely digital architecture that eliminates many of the analog noise sources that plague conventional fractional-N synthesizers.

1.1 Thesis Outline

An overview of frequency synthesis techniques is covered in Chapter 2. The suitability of each architecture for large-scale integration in mobile digital radio applications is discussed.

Chapter 3 introduces the new $\Sigma\Delta$ frequency discriminator based synthesizer architecture. Synthesizer component models are developed for use in simulations to predict the behaviour of the synthesizer.

Complete frequency-domain and time-domain synthesizer models are developed in Chapter 4. The models in conjunction with the synthesizer parameters are used to explore the effects these parameters have on the stability, transient response and phase noise of the synthesizer.

Detailed design considerations in the realization of the synthesizer architecture are studied in Chapter 5. The design parameters are identified to define the overall design space of the implementation. Additionally, experimental measurements are compared to analytical and simulated results to validate the models developed earlier.

Finally, some concluding remarks and recommendations for future research are presented in Chapter 6.

Chapter 2

Frequency Synthesizers for Mobile Applications

Channel selection in multi-channel radio receivers is achieved by using frequency synthesizers to mix the received signal down to an intermediate frequency (IF) for further processing. Many architectures are available when designing synthesizers, however the one chosen depends on the design requirements for the particular application. The important parameters of frequency synthesizers are tuning range, resolution, settling time, stability and spectral purity. However, specific applications add constraints to the size, power consumption, complexity and cost of the final synthesizer. In mobile communication systems, the emphasis is on the overall size and power consumption of the synthesizer in addition to its performance specifications.

There are many synthesizer architectures but they may be separated into the following major categories

- Direct analog synthesis
- Direct digital synthesis
- Indirect synthesis

The following sections describe these methods and their suitability for mobile communication applications.

2.1 Direct Analog Synthesis

Direct analog synthesis (DAS) directly translates a reference frequency using mixers, dividers, multipliers, switches and filters to produce an output frequency [1]. The typical DAS synthesizer shown in Figure 2.1 uses various combinations of these analog blocks along with multiple references to synthesize the desired frequencies.

Figure 2.1 Direct analog synthesis.

The frequency stability of DAS synthesizers suffers since they use multiple references and analog blocks which require careful calibration to ensure proper performance. The spectral purity of the output must also be controlled through band-pass filtering between various stages to reduce the harmonic content to acceptable levels. This degrades the switching speed of the synthesizer which is inversely proportional to the filter pass-bands.

Direct analog synthesis can produce synthesizers with high resolution through the use of multiple stages and reference frequencies. However, since only discrete analog blocks are used, the overall size and complexity grows quickly with higher frequency resolution and thus a DAS synthesizer quickly becomes unsuitable for mobile use.

2.2 Direct Digital Synthesis

Direct digital synthesis (DDS) generates a sinusoid by digital integration of the desired frequency at a higher clock rate. The accumulated phase is translated to a sinusoidal waveform via a table lookup and converted to an analog signal with a digital-to-analog (D/A) converter followed by a reconstruction filter [6].

Figure 2.2 Direct digital synthesis.

The phase accumulator in Figure 2.2 accepts an N-bit binary word representing the desired output frequency and produces a binary word indicating instantaneous phase. The instantaneous phase is mapped to instantaneous amplitude in the table lookup function. The frequency resolution of the DDS synthesizer is proportional to the rate of phase accumulation.

$$\Delta f = \frac{f_{clk}}{2^N} \quad (2.1)$$

Thus for a large input word size N , the resolution of the synthesizer becomes very small which is a desirable feature of DDS synthesizers. As the output frequency is increased, the number of samples per sinusoid decreases. Sampling theory states that at least two samples are required to reconstruct the output waveform so the maximum output frequency is limited by the clock frequency [5].

$$f_{max} = \frac{f_{clk}}{2} \quad (2.2)$$

Practically, the maximum output frequency is less than this to permit filtering of the image response which restricts the use of DDS synthesizers to lower frequency applications.

Since the input frequency word controls the rate of phase accumulation, and therefore the output frequency, it is possible to change the output frequency of the synthesizer as often as every clock cycle without affecting the phase continuity. This implies that DDS is suitable for applications which require various input modulation schemes (e.g. GMSK, QPSK etc) or frequency hopping in spread spectrum systems.

The spurious and phase noise performance of a DDS synthesizer is determined by the phase noise of the master clock as well as quantization noise introduced by the sine lookup table and the D/A converter. The close-in phase noise is governed by the oversampling ratio and results in very low phase noise for frequencies much less than $f_{clk}/2$. However, since DDS uses sampling, the output spectrum suffers from image frequencies as well as harmonics due to D/A converter non-linearities.

Direct digital synthesizers can be highly integrated since most of their architecture is digital leading to extremely small size. Their suitability for high frequency synthesis in mobile applications is questionable due to their high power consumption at high output frequencies. This is due to the Nyquist criterion which forces the clock frequency to be at least twice the output frequency necessitating the use of high speed technologies (e.g. ECL, GaAs etc.) that consume more power.

2.3 Indirect Synthesis

Indirect synthesis utilizes a tunable oscillator controlled by a phase-locked loop (PLL) or a frequency-locked loop (FLL) to generate an output frequency as shown in the single-loop synthesizer in Figure 2.3 [6].

Figure 2.3 Typical phase-locked loop block diagram.

This method of synthesis generates an output frequency dependant on the DC control voltage at the input to the voltage-controlled oscillator (VCO). The control voltage is derived from the error between a reference frequency and the VCO frequency. The corrective action of the loop forces the VCO to track the reference frequency or some multiple of it when a divider is present in the feedback path. Thus for a fixed reference frequency f_{ref} the divider modulus N determines the output frequency which is limited only by the maximum VCO frequency

$$f_{out} = Nf_{ref} \quad (2.3)$$

This imposes a minimum frequency resolution of f_{ref} for an integer divider modulus N . Higher frequency resolution requires a lower reference frequency with a subsequent increase in the divider modulus. However, an undesired side effect of this is that the overall phase noise at the output increases with the divider modulus thus limiting the minimum reference frequency.

The settling time of a PLL is inversely proportional to its loop bandwidth, therefore it would be advantageous to maximize the loop bandwidth for applications requiring a fast switching speed. However, the loop bandwidth also affects the stability of the loop and the phase noise at its output. These latter two parameters usually dominate so other methods to decrease the PLL settling time are used.

The spurious and phase noise response of a PLL is determined by the VCO characteristics, reference frequency and the loop components. The loop bandwidth has a large impact on the overall noise performance of the PLL. Outside the loop bandwidth spurious frequencies are suppressed by the low-pass action of the loop. Within the loop bandwidth, the phase noise dominated by the VCO close-in noise is suppressed.

Single-loop, integer-N PLL or FLL synthesizers are inherently simple structures and consume far less power than other synthesizer structures. It is possible to integrate some of the blocks to reduce their overall size even further [7]. However, these synthesizers are not capable of high frequency resolution with the low settling times required by current communication systems. Alternatives to these structures have been developed and are explored in the following sections.

2.3.1 Multi-Loop and Hybrid

The previous section on single-loop PLL's revealed the limited frequency resolution available without sacrificing the noise performance by lowering the reference frequency. One possible solution shown in Figure 2.4 is to use multiple loops and mix their outputs together in various combinations to produce the desired frequencies [3].

Figure 2.4 Multiple-loop PLL synthesizer.

This technique achieves high frequency resolution while still maintaining a fast switching speed and optimum noise performance. However, the overall complexity and power consumption of the synthesizer increases and it is unlikely with current technologies that an integrated solution is possible for mobile applications.

Synthesizers that combine the features of various synthesis methods are called hybrids [2]. Current hybrid architectures can consist of any combination of the basic architectures and usually exploit the best features of each method. Most hybrid structures use a DDS to generate an offset frequency in a PLL or drive the PLL directly by replacing its reference frequency. Since there are many hybrid and multi-loop PLL structures, their performance and characteristics are summarized in Table 2.1.

Table 2.1 Comparison of Hybrid Frequency Synthesizers [2].

Synthesizer	Multi-Loop PLL	DDS/DAS Hybrid	PLL with DDS frequency offset	PLL with DDS reference
Bandwidth	Large	>DDS	Large	Large
Frequency Resolution	Medium > 1KHz	Extremely fine < 0.01Hz	Extremely fine < 0.01Hz	Fine < 1Hz
Switching Time	Slow > 1ms	Very fast < 1 μ s	Fast < 100 μ s	Tradeoff vs. spurious noise
Spurious Noise	Good	Minimal close-in spurs	Minimal close-in spurs	Excellent over wide bandwidth
Phase Noise	Very good	Very good	Very good	Good
Circuitry	Complex	Moderate	Moderate	Simple

2.3.2 Fractional-N

In conventional integer-N PLL's, the minimum resolution was the reference frequency f_{ref} . Reducing f_{ref} results in a narrow loop bandwidth, inadequate phase noise

suppression and longer settling times [8]. In fractional-N synthesis, the divider modulus is periodically varied between n and $n+1$. The average value of the divider modulus N is

$$N = n + f \quad (2.4)$$

where n is the integer component and f is the fractional component. This technique has been shown to greatly increase the frequency resolution of the synthesizer without lowering the reference frequency [9]. One drawback to this method is that by varying the divider modulus, phase jitter is produced resulting in spurs at the synthesizer output. Many methods have been developed to combat this problem but most are a variation of the following techniques [10]

- phase interpolation
- jitter injection
- noise shaping

Phase interpolation extracts the current phase error component due to phase jitter in the divider from its modulus control. The instantaneous phase error is converted to analog and subtracted from the phase detector output which removes the spurious frequency components caused by divider phase jitter [9]. This architecture is shown in Figure 2.5 where the phase error is simply the current contents of the accumulator controlling the dual-modulus divider.

Figure 2.5 Phase jitter reduction using phase interpolation.

The performance of this method is largely dependent on the matching of the D/A converter gain with the phase detector gain and the synchronization of the phase error and compensation signal. Phase interpolation synthesis requires precision matching of analog components and is therefore unsuitable in many applications where high speed and low power are desired.

Fractional-N synthesizers generate phase jitter due to the periodic switching of the divider modulus. It has been shown that if the phase error is randomized, the periodicity will be destroyed and the phase error spurs will be reduced [4]. The jitter injection method takes advantage of this by randomizing the divider modulus control which spreads out the power in the phase error spurs. This will inherently raise the overall noise floor at the synthesizer output, but this is generally more desirable than discrete noise spurs. Jitter injection can be achieved with the architecture in Figure 2.6 which uses a random number generator to randomize the divider modulus control.

Figure 2.6 Block diagram of the random jitter injection method of phase jitter reduction.

Jitter injection is sometimes more favourable than phase interpolation since it attempts to control the phase error at its source rather than compensating for it later. Since the

randomization is generated using digital hardware, this method is less error prone than analog phase interpolation and is more suitable for monolithic integration. However, the noise power of the phase error spurs is reduced at the expense of raising the noise floor. This may not always be acceptable and some better forms of noise shaping are desirable to suppress the noise in the baseband even further.

Sigma-Delta ($\Sigma\Delta$) modulation is a noise shaping technique used to control the divider modulus. $\Sigma\Delta$ modulators generate a control sequence with an average density corresponding to the desired frequency, but in such a way that the inherent phase jitter is shifted away from baseband to higher frequencies. The basic first-order $\Sigma\Delta$ modulator block diagram is illustrated in Figure 2.7.

Figure 2.7 First-order $\Sigma\Delta$ modulator.

Analysis of the output bitstream of the $\Sigma\Delta$ modulator shows that the noise is suppressed in baseband and pushed to higher frequencies outside the PLL loop bandwidth [11]. The filtering action of the loop outside the loop bandwidth suppresses the overall noise to an acceptable level at the synthesizer output. The block diagram of the first-order $\Sigma\Delta$ modulator in Figure 2.7 can be easily implemented by recognizing that an accumulator is a simple realization of a first-order modulator [8]. Higher order $\Sigma\Delta$ modulators with superior noise shaping can be realized by cascading first-order modulators together as in Figure 2.8.

Figure 2.8 Digital third-order $\Sigma\Delta$ modulator realization.

Figure 2.8 shows an all digital realization which is suitable for monolithic implementation. The complexity of the circuit increases not only with the order of the modulator but also with the desired frequency resolution. This may significantly increase the power consumption of the modulator rendering it unsuitable for mobile applications.

2.4 Frequency Discriminator Based Synthesis

Synthesis techniques based on conventional frequency discriminators in the feedback path are inherently frequency-locked loops (FLL) and their use is restricted to certain applications where frequency is the controlled parameter. A very popular application is in automatic frequency control (AFC) used in almost every receiver design. In AFC circuits, an oscillator is forced to oscillate at a constant frequency through the use of closed-loop frequency control. A typical AFC circuit is shown in Figure 2.9 where a conventional analog balanced discriminator is used to sense the output frequency and generate an error signal to control the VCO.

Figure 2.9 Automatic frequency control using a balanced discriminator frequency-locked loop.

High quality signal generators make use of discriminator-based frequency-locked loops to lower the phase noise of the VCO used in the synthesizer. The technique uses one or more delay-line discriminators placed around the VCO to sense and control any frequency noise produced by the VCO [12]. A typical block diagram of a phase-locked loop (PLL) that incorporates a FLL is illustrated in Figure 2.10.

Figure 2.10 PLL using a frequency-locked loop to control VCO phase noise.

This architecture is similar to a conventional PLL but the effective VCO phase noise seen by the PLL is reduced by the frequency-locked loop. Frequency modulation (FM) of these synthesizers is more complex than conventional PLL's since any FM applied to the VCO input will be attenuated by the FLL loop gain. This problem is overcome by subtracting

the FM modulating signal from the error signal sensed by the frequency discriminator. This effectively leaves only the frequency noise generated by the VCO as an error signal which is subsequently corrected.

The use of frequency discriminators in frequency synthesis and control has been limited by the performance of the discriminators themselves. Most analog discriminators are non-linear circuits that suffer from offsets and non-linear conversion gain. The next section gives an overview of conventional analog discriminators and reveals their shortcomings. It also introduces a new oversampled digital frequency discriminator that forms the basis for a new synthesizer architecture explored in future chapters.

2.4.1 Frequency Discriminators

Frequency discriminators are used to demodulate angle modulated (FM or PM) carriers in receiver systems. The angle modulation may be the result of an intentional FM or PM signal or as a result of phase noise modulation. The output of a discriminator is an amplitude change that corresponds to a frequency change (FM to AM conversion) at its input. Consider an FM modulated carrier

$$\lambda_{fm}(t) = A \cos \left[2\pi f_c t + 2\pi k_f \int_0^t s(\tau) d\tau \right] \quad (2.5)$$

The conversion from FM to AM is accomplished by taking the time-derivative of the modulated carrier $\lambda_{fm}(t)$.

$$\frac{d\lambda_{fm}(t)}{dt} = -2\pi A [f_c + k_f s(t)] \sin \left[2\pi f_c t + 2\pi k_f \int_0^t s(\tau) d\tau \right] \quad (2.6)$$

Since the carrier frequency f_c is much greater than the maximum modulation frequency

$s(t)$, the derivative produces an output that is proportional to the modulating signal $s(t)$. The derivative of an FM signal can also be approximated by the difference between two adjacent signal samples.

$$\lambda_{fm}(t) - \lambda_{fm}(t - t_0) \approx t_0 \frac{d\lambda_{fm}}{dt} \quad (2.7)$$

There are many ways of implementing the derivative operation but the most popular methods are

- FM to AM conversion
- Phase shift discrimination

2.4.1.1 Analog Discriminators

Any tuned circuit (eg. band-pass filter) approximates the ideal differentiator over a small frequency range as shown in Figure 2.11.

Figure 2.11 Simple tuned circuit response used as a frequency discriminator.

A greater frequency discrimination range can be achieved by subtracting a shifted version of the tuned circuit response from itself [13]. With proper design, the even powers of the series expansion of the tuned circuit response are eliminated. This function is performed by the balanced discriminator circuit of Figure 2.12.

Figure 2.12 Balanced frequency discriminator.

Equation (2.7) approximates the derivative function by taking the difference between two adjacent samples of the FM signal. Since one sample is delayed in time (i.e. a phase shift), the discriminator can be implemented using a linear phase shift network in the delayed path as shown in Figure 2.13.

Figure 2.13 Phase shift frequency discriminator.

Ideally, the outputs from these analog frequency discriminator structures are a linear function of their input frequency. However, they all suffer from non-linear conversion gain and most exhibit DC offset problems (i.e. due to component tolerances etc.) that prevent them from giving an accurate analog measure of the absolute input frequency over a usable range.

2.4.1.2 Oversampled Digital Discriminators

The synthesizer architecture described in the following chapters uses a frequency discriminator in its feedback path to provide a digital measure of the VCO frequency. Since errors from the discriminator cannot be easily corrected, an accurate measure of the absolute frequency of the VCO is required. In addition, the output of the discriminator must be in digital form to interface with the rest of the synthesizer. The analog discriminator structures discussed previously would still require their output to be converted to digital form even if they produced an accurate analog measure of the VCO frequency. The $\Sigma\Delta$ discriminator described next is a unique alternative to the previous discriminator structures in that it combines frequency discrimination with analog to digital conversion.

The $\Sigma\Delta$ discriminator used in this synthesizer performs oversampled A/D conversion of the input frequency deviations of an angle modulated signal [14]. It generates a single-bit digital output whose density of ones is proportional to the instantaneous input frequency. Figure 2.14 shows the simplest form of the discriminator consisting of a dual-modulus divider (DMD) and a flip-flop connected in a loop.

Figure 2.14 First-order $\Sigma\text{-}\Delta$ frequency discriminator and timing diagram.

The principle of operation of this circuit is straightforward. The DMD divides the input frequency by n or $n+1$ depending on the value of the modulus control signal which in this case is the output bitstream $b(t)$. The phase of the divided-down frequency is compared to that of a reference frequency by means of the flip-flop. The output of the flip-flop indicates whether the phase of the divided-down frequency leads or lags the phase of the reference frequency. Thus the flip-flop's output is a one bit representation of the phase difference between the two signals, and is fed back to control the DMD. During steady-state operation, the modulus of the DMD is adjusted such that the phase of the divided-down frequency brackets that of the reference frequency. For an $n/(n+1)$ DMD and an output bitstream $b(t) \in \{0,1\}$, the average density of the bitstream is given by

$$\overline{b(t)} = \frac{1}{f_{ref}} (f_{in}(t) - nf_{ref}) \quad nf_{ref} < f_{in}(t) < (n+1)f_{ref} \quad (2.8)$$

The average bitstream density in Equation (2.8) is only valid over the discriminator input frequency range determined by the lower modulus n and the reference frequency f_{ref} .

Chapter 3

Analysis of a Frequency Discriminator Based Synthesizer

In the previous chapter, various synthesizer structures were reviewed to illustrate their characteristics and suitability for mobile applications. Synthesizers with high resolution and low physical complexity are most applicable since they offer the level of performance required for mobile use and are suitable for monolithic integration. Previously, the best method for mobile applications was $\Sigma\Delta$ fractional-N synthesis. The recent development of oversampled digital frequency discriminators makes a new synthesizer structure using the discriminator in the feedback path feasible [14].

The following sections describe the new architecture proposed in this thesis and develop analytical models to characterize the performance of the synthesizer.

3.1 Synthesizer Architecture

Figure 3.1 A $\Sigma\Delta$ frequency discriminator based synthesizer.

The new synthesizer structure in Figure 3.1 uses an oversampled $\Sigma\Delta$ frequency discriminator in the feedback path. The frequency discriminator combines the function of the dual-modulus divider and phase detector in a conventional fractional-N PLL. Additionally, the discriminator converts the analog input signal to digital form for further processing. This permits a greater portion of the synthesizer to be digital which offers a number of advantages over a conventional fractional-N synthesizer. A largely digital architecture is suitable for monolithic implementation without the need for additional tuning circuits found in many analog integrated implementations. Many analog noise sources are eliminated which reduces the overall noise at the synthesizer output. The frequency discriminator based structure also offers more flexibility in the processing of the signal. Through the use of digital signal processing (DSP), the loop dynamics can be adaptively controlled which results in synthesizer performance that is optimized under varying conditions. This is an important feature since many synthesizer designs without adaptive control, compromise their performance to meet the design specification under all conditions. DSP may also be used to adaptively cancel the spurious effects caused by incomplete noise shaping from the $\Sigma\Delta$ frequency discriminator output. These spurs appear

quite frequently in the radio frequency (RF) output spectrum of conventional fractional-N synthesizers and are caused by a similar mechanism in the $\Sigma\Delta$ modulator.

Operation of the synthesizer in Figure 3.1 is similar to conventional fractional-N synthesizers. A desired input frequency word is applied to the synthesizer and the VCO is forced to oscillate at that frequency through closed-loop control. Unlike conventional synthesizers, the reference frequency controls the discriminator such that the phase of the divided-down frequency brackets that of the reference frequency. The VCO becomes phase locked to an arbitrary reference phase determined by the initial conditions when the synthesizer acquires lock. Since the discriminator responds to the phase of the divided-down frequency, any phase drift of the VCO will cause a phase offset to exist. This phase offset implies a momentary deviation in frequency has occurred as shown in Figure 3.2.

Figure 3.2 Frequency perturbation caused by VCO phase error.

The frequency perturbation is converted to digital and fed back through the decimation filter. The resulting scaled VCO frequency is compared to the desired digital frequency word and an error signal is generated. The frequency error is integrated to produce an equivalent phase error and applied to a compensation block that forces the VCO to correct its phase to that of the reference phase.

3.2 $\Sigma\Delta$ Frequency Discriminator

The relationship between the input frequency f_{in} and the output bitstream is best described by developing models for the discriminator components and analyzing the response of the second-order discriminator used in this synthesizer.

3.2.1 Multi-Modulus Divider

Figure 3.3 Timing diagram of the multi-modulus divider.

From Figure 3.3, for a lower modulus of n and a bitstream b , the time to the k^{th} divider output which corresponds to the j^{th} VCO cycle is

$$t_{d,k} = t_{v,j} \quad \text{where} \quad j = \sum_{i=1}^k (n + b_i) \quad (3.1)$$

Here we define the time to the j^{th} VCO cycle to consist of a nominal time and a time

deviation corresponding to a change in the VCO frequency.

$$t_{v,j} = jT_v + \Delta t_{v,j} \quad (3.2)$$

Thus Equation (3.2) becomes

$$\begin{aligned} t_{d,k} &= jT_v + \Delta t_{v,j} \\ &= \sum_{i=1}^k (n+b_i)T_v + \Delta t_{v,k} \end{aligned} \quad (3.3)$$

where the time deviation of the VCO has been re-sampled at the divider output rate. In order to relate time to corresponding phase, define a negative phase difference where the current VCO phase lags its nominal phase as shown in Figure 3.4.

Figure 3.4 Lagging VCO results in a negative phase error with respect to its nominal phase.

This is consistent with PLL convention where a lagging VCO has a negative phase with respect to its nominal phase. Then the input phase difference can be defined as

$$\begin{aligned}
 \theta_{v,j} &= \frac{2\pi}{T_v} (jT_v - t_{v,j}) \\
 &= \frac{2\pi}{T_v} (-\Delta t_{v,j})
 \end{aligned} \tag{3.4}$$

Similarly, the phase difference at the divider output is

$$\begin{aligned}
 \theta_{d,k} &= \frac{2\pi}{T_d} (kT_d - t_{d,k}) \\
 &= \frac{2\pi}{T_d} (kT_d - \sum_{i=1}^k (n + b_i)T_v - \Delta t_{v,k})
 \end{aligned} \tag{3.5}$$

When the discriminator loop is locked, then the nominal input period T_v and the nominal divider output period T_d are related by the average divider modulus N .

$$\begin{aligned}
 T_d &= NT_v \\
 \text{where } N &= n + p_1 \\
 p_1 &= \left[\sum_{i=1}^k b_i \right] / k
 \end{aligned} \tag{3.6}$$

Then Equation (3.5) becomes

$$\theta_{d,k} = \frac{2\pi}{N} \left[Nk - \sum_{i=1}^k (n + b_i) - \frac{\Delta t_{v,k}}{T_v} \right] \tag{3.7}$$

Now letting $b=p_1+\Delta$ and substituting the expression for the input phase difference from Equation (3.4) gives the divider output phase difference

$$\theta_{d,k} = \frac{1}{N} \left[\theta_{v,k} - 2\pi \sum_{i=1}^k \Delta_i \right] \quad (3.8)$$

Equation (3.8) forms a basic model for the multi-modulus divider illustrated in Figure 3.5.

Figure 3.5 Block diagram of the multi-modulus divider model.

3.2.2 Quantizer

The linear model of the single-bit (i.e. 2 level) quantizer is based on the assumption that the signal activity in the system is sufficiently busy that the quantization noise can be viewed as uncorrelated with the signal. For second or higher order $\Sigma\Delta$ modulators this assumption is reasonable [11]. Thus the quantizer can be modelled as a unity gain element with additive quantization noise. Note that the gain of a single-bit quantizer is not defined and is arbitrarily set to one. If the quantization noise is assumed to be white with uniform distribution, it can be shown that its power spectral density is

$$S_{ni}(f) = \frac{\Delta^2}{12f_{ref}} \quad [Hz^2/Hz] \quad (3.9)$$

where Δ is the quantizer step size and f_{ref} the sampling frequency [11]. This leads to the model for the single-bit quantizer in Figure 3.6.

Figure 3.6 Linear single-bit quantizer model.

3.2.3 Second-Order $\Sigma\Delta$ Discriminator Model

The second-order discriminator used in the synthesizer has a single-loop architecture unlike previously reported structures [14]. A frequency-domain model for this second-order discriminator is based on the previously defined models of the multi-modulus divider and the quantizer and is shown in Figure 3.7.

Figure 3.7 Block diagram of the single-loop second-order discriminator.

Through manipulation of the blocks in Figure 3.7, it can be shown that this structure exhibits second-order noise shaping but with instantaneous frequency as the input

variable.

$$Y(z) = F_{in}(z) + E_n(z)(1 - z^{-1})^2 \quad (3.10)$$

In the time domain, the discriminator model consists of the equivalent difference equations of a second-order noise shaped modulator with frequency as the input variable.

3.3 Comb Decimation Filter

The use of a $\Sigma\Delta$ frequency discriminator to perform oversampled analog to digital conversion of the VCO frequency is desirable in discriminator-based synthesizers. This results in conversion at a high data rate similar to the oversampled conversion performed by conventional $\Sigma\Delta$ modulators on an analog voltage [11]. Therefore, the output rate of the bitstream must be reduced (i.e. decimated) and the number of bits of resolution must be increased. Previously, high-order finite impulse response (FIR) filters were used to decimate the oversampled bitstream to the Nyquist rate [15]. One of the problems with high-order FIR filters is that they may be very complex since they usually have many weighted taps. The tap coefficients are not usually integer powers of 2, so simple multiplication by bit shifting is not possible. Additionally, each tap has an associated delay which leads to instability of the closed-loop synthesizer structure. The FIR filter complexity and inherent delay render this type of decimation filter unsuitable for use in the synthesizer.

The filter chosen for use in the synthesizer is a simple multi-stage comb decimation filter shown in Figure 3.8. This type of filter is suitable for decimation to approximately four times the Nyquist rate and is much easier to realize than the high-order FIR filters described earlier.

Figure 3.8 Block diagram of the third-order comb filter.

Since the filtering requirements of the synthesizer are not as stringent as in other applications, these filters are attractive candidates for replacing the high order FIR filters since they have simple structures that introduce minimal delay [15]. From Figure 3.8, the discrete transfer function for a comb filter of order k and decimation factor N is

$$H(z) = \left[\sum_{i=0}^{N-1} z^{-i} \right]^k = \left[\frac{1 - z^{-N}}{1 - z^{-1}} \right]^k \quad (3.11)$$

Equation (3.11) indicates that the filter has a pole at $z=1$ which is not asymptotically stable and therefore may overflow. It can be proven that by using modulo arithmetic (i.e. wrap-around arithmetic) everywhere in the system, overflow is irrelevant. A sufficient condition for the filter to work correctly is to choose a modulus that is larger than

$$2^b \geq (N^k + 1)D \quad (3.12)$$

where b is the number of bits and D is the dynamic range of the input signal [16]. The dynamic range of the $\Sigma\Delta$ frequency discriminator is a single bit which implies that $D=1$.

Due to this limited dynamic range, modulo comb filters are very suitable for decimating single-bit oversampled $\Sigma\Delta$ bitstreams. If the modulo that satisfies Equation (3.12) is used throughout the filter, carry handling may simply be ignored which leads to a less complex realization.

A sufficient order for the filter is $k+1$ where k is the order of the $\Sigma\Delta$ frequency discriminator [17]. For the second-order frequency discriminator used in this synthesizer, a comb filter order $k=3$ provides sufficient attenuation of the quantization noise to limit the aliased noise power after decimation. The effect of aliasing can be shown by evaluating the frequency response of the comb filter around the unit circle.

$$H(e^{j2\pi f/f_{ref}}) = \left[\frac{1 - e^{-j2\pi f N/f_{ref}}}{1 - e^{-j2\pi f/f_{ref}}} \right]^k \quad (3.13)$$

The magnitude response of the comb filter shown in Figure 3.9 has zeros (i.e. notches) at integer multiples of the decimated rate. The noise power in a bandwidth around each notch is aliased into baseband due to the under-sampling action of the decimator.

Figure 3.9 Frequency response of a third-order comb filter.

The amount of attenuation at each notch is sufficient for decimation to approximately four times the Nyquist rate which in this case is defined by the synthesizer loop bandwidth.

The DC gain of the comb filter is N^k where N is the decimation factor and k is the filter order. This results in a high DC gain for the third-order filter used in this synthesizer which increases the signal resolution by

$$resolution = \log_2(N^k) \quad [bits] \quad (3.14)$$

This is a desirable feature of these filters since their DC gain contributes to the open-loop gain of the synthesizer.

The time-domain and frequency-domain models of the comb filter are developed from Equation (3.11) which can be separated into the recursive integrator section and the

differentiator section. Between these sections, a decimation occurs so the differentiators operate at the decimated rate f_{re}/N . Since the comb filter utilizes modulo arithmetic, the difference equations of the time-domain model must also employ modulo arithmetic to ensure a proper response.

3.4 FIR Filter

In the previous section, a multistage comb filter was used to decimate the oversampled bitstream to a lower rate while concurrently increasing the resolution. The attenuation of the out-of-band quantization noise is limited with these filters so additional filtering may be necessary to reduce the quantization noise. The problem with additional filtering stages is that they introduce more delay in the synthesizer loop which decreases the overall phase margin. Thus any additional stages must be designed carefully to maintain loop stability. Filter structures that are suitable for post-filtering the comb decimation filter output are short (i.e. minimal number of taps) FIR filters. These filters have a linear phase and for short lengths they introduce minimal additional delay. The realization of these FIR filters can greatly increase the circuit complexity unless constraints are imposed on the number of taps and tap coefficients [18]. Two filter structures shown in Figure 3.10 were chosen for implementation in the synthesizer.

Figure 3.10 Block diagram of a) a single stage FIR filter, b) a two stage FIR filter.

Both filters have simple structures since all their tap weights are 1 so no explicit multipliers are required. The transfer function of the filter in Figure 3.10a) is simply

$$H(z) = 1 + z^{-1} \quad (3.15)$$

while the filter in Figure 3.10b) is two cascaded sections of the same filter with a corresponding transfer function

$$H(z) = [1 + z^{-1}]^2 \quad (3.16)$$

Since the FIR filters occur after the comb decimation filter, they operate at the decimated rate f_{ref}/N . The magnitude response in Figure 3.11 shows that the single stage $1+z^{-1}$ filter has zeros at multiples of $\frac{1}{2}$ the sampling frequency and a DC gain of 2.

Figure 3.11 Frequency response of a single stage and two stage FIR filter.

This effectively attenuates the quantization noise while increasing the resolution by one bit. The two stage filter has zeros at multiples of $\frac{1}{2}$ the sampling frequency but a higher DC gain yielding 2 additional bits of resolution.

The time-domain expressions for the FIR filters are the equivalent difference equations derived from their respective transfer functions.

3.5 Digital Signal Processor

The digital signal processing (DSP) block can be divided into two sections. The first section compares the filtered discriminator signal to a digital reference frequency. The resulting frequency error signal is processed by the second section which also

controls the loop dynamics. The DSP block could potentially perform more advanced signal processing functions in addition to controlling the loop dynamics. An example is to adaptively filter the discriminator signal to cancel any residual frequency spurs arising from incomplete noise shaping. However, at this stage of the synthesizer development, only the loop compensation will be implemented. The type of loop compensation chosen uses proportional plus integral control of the phase error which makes the synthesizer a second-order structure. This implies an integration stage is necessary to convert the frequency error from the comparator to the equivalent phase error. The output from the DSP block is converted to analog and subsequently filtered to reduce the digital-to-analog (D/A) converter quantization noise. The extra pole introduced by the analog low-pass filter must be compensated for in the DSP block. The DSP block and D/A section with analog filter are shown in Figure 3.12.

Figure 3.12 Block diagram of the original DSP block with compensation for the analog filter pole.

An alternative to the previous controller structure is that of Figure 3.13. In this structure, one of the digital integrators is moved from the DSP block to after the D/A converter and implemented as an analog integrator. The low-pass characteristic of the integrator is effective for filtering the quantization noise of the frequency discriminator, thus the

additional low-pass filter of the structure in Figure 3.12 is not necessary. This reduces the complexity of the controller since the extra pole from the analog filter is removed. The frequency to phase conversion still occurs in the DSP section where the phase error θ_e is summed with a derivative term $\partial\theta_e$.

Figure 3.13 Block diagram of the simplified DSP block with analog integrator after the D/A converter.

The loop compensation network in the DSP block is analogous to the loop filter of a conventional phase-locked loop. The transfer function of the controller in the z -domain is

$$H(z) = a_2 + \frac{a_3}{1 - z^{-1}} \quad (3.17)$$

where a_2 is the proportional gain and a_3 the integral gain. Substituting $z=e^{j\omega T}$ in Equation (3.17) yields

$$H(e^{j\omega T}) = a_2 + \frac{a_3}{1 - e^{-j\omega T}} \quad (3.18)$$

This results in a non-linear equation which makes it difficult to solve for the various loop

parameters analytically. It is therefore desirable to linearize $H(z)$ by mapping it into the s-domain. The response of the integral term with $a_3=1$ shown in Figure 3.14 indicates that the digital integrator is linear for frequencies from DC to $f_{ref}/6$. Thus it can be replaced by an analog integrator with transfer function

$$H(s) = \frac{\pi f_{ref}}{3} \frac{1}{s} \quad (3.19)$$

Figure 3.14 Frequency response of a discrete-time integrator.

This relation holds as long as the bandwidth of the synthesizer is less than $f_{ref}/6$ where f_{ref} is the decimated sampling frequency. The mapping of the loop compensation network between the z-domain and the s-domain is expressed as

$$a_2 + \frac{a_3}{1 - z^{-1}} \leftrightarrow a_2 + \frac{(a_3 \pi f_{ref})/3N}{s} \quad f \leq \frac{f_{ref}}{6N} \quad (3.20)$$

where f_{ref}/N is the decimated sampling rate. The s-domain expression of Equation (3.20) is identical to a conventional PLL loop filter using an integrator with phase lead compensation [19].

The time-domain model of the digital signal processor (DSP) is derived from the discrete transfer function in Equation (3.17). Due to finite word size when implementing the DSP, it is necessary to restrict the value of some nodes to prevent internal overflow. This can be achieved through the use of saturation arithmetic at these nodes and this non-linear effect must be accounted for in the time-domain model to produce accurate simulation results.

3.6 Digital to Analog Converter

The digital to analog (D/A) converter interfaces the digital DSP section to the analog loop filter. From an analytical perspective, it represents the transition from the discrete-time domain to the continuous-time domain. An understanding of the D/A converter input and output signals is necessary to develop a model for it. In the digital domain, the signals can be considered as discrete time impulses occurring at the sampling rate. However, the D/A converter translates these discrete impulses to continuous time, discrete amplitude signals.

Figure 3.15 Zero-order hold function of the D/A converter.

Figure 3.15 illustrates the zero-order hold (ZOH) function of the D/A converter where each digital sample is held until the next one occurs. The D/A converter can be modelled as an ideal conversion gain converting digital numbers to a voltage followed by a ZOH function. This doesn't account for any non-linearities (e.g. offsets, integral, differential etc.) found in actual D/A converters but the model is sufficient for analysis of the synthesizer. The conversion gain is determined by the full-scale voltage range and the number of bits in the converter.

$$K_a = \frac{V_{fullscale}}{2^n} \quad [V/\#] \quad (3.21)$$

The normalized transfer function of a zero-order hold function assuming ideal impulses (i.e. delta functions) at its input is [20]

$$H(s) = \frac{1 - e^{-sT}}{sT} \quad (3.22)$$

Normalizing the transfer function so its DC gain is one ensures that its response matches that of the D/A converter. The normalized frequency response of the D/A converter in Figure 3.16 is a $\sin(x)/x$ function with zeros at integer multiples of the sampling clock

f_{ref}/N due to the ZOH function.

Figure 3.16 Normalized frequency response of a D/A converter.

Since the bandwidth of the synthesizer is much less than f_{ref}/N , the D/A converter essentially has a flat response and attenuation of the signal is negligible.

In the time domain, the D/A converter simply introduces a conversion gain from the digital input to a corresponding output voltage as indicated in Equation (3.21).

3.7 Analog Loop Filter

The analog integrator serves two functions in the synthesizer. First it performs the final integration making the synthesizer a second-order structure. Second, it filters the quantization noise from the frequency discriminator. Combining these two functions into

one block eliminates the need to compensate for the low-pass filter that would have been necessary after the D/A converter.

The integrator is modelled as an ideal linear integrator with output

$$v_o(t) = \frac{-1}{RC} \int v_i(t) dt \quad (3.23)$$

The constant term $-1/RC$ reflects the implementation of the function where the integrator time constant is set by RC and an inversion occurs that is compensated for in the DSP. Equation (3.23) represents the operation of the integrator in the time domain but it ignores the integration constant. In the frequency domain the integrator has a response

$$H(s) = \frac{-1}{RC} \frac{1}{s} \quad (3.24)$$

This corresponds to the frequency response shown in Figure 3.17 which illustrates the pole at DC with a slope of -20dB/dec.

Figure 3.17 Frequency response of the active integrator.

3.8 Voltage-Controlled Oscillator

There are two models used for the voltage-controlled oscillator (VCO). The noise analysis uses the VCO's actual phase noise characteristics to compute the phase noise contribution at the synthesizer output. Phase noise is discussed in a following chapter and will not be covered here. The linear frequency-domain analysis uses a simple linear model based on the following assumptions. If the modulation bandwidth of the VCO is assumed to be large, and over the tuning range the VCO sensitivity K_v remains constant, then the VCO can be modelled as a straight line with slope equal to K_v . The VCO transfer function in Figure 3.18 shows this characteristic with a DC tuning offset required to move the VCO centre frequency to the desired point.

Figure 3.18 Linearized VCO tuning characteristics.

The output frequency of the VCO can then be modelled as

$$\omega_o = K_{vco}(v_c + v_{off}) \quad [rad/s] \quad (3.25)$$

In most cases, the output phase of the PLL is the controlled parameter, thus the VCO performs an implied integration since its output is frequency. The equivalent block diagram for the linear frequency-domain model of the VCO is shown in Figure 3.19.

Figure 3.19 Linear VCO model with additive frequency offset voltage.

In the time domain, the VCO introduces a conversion gain that converts its input tuning voltage to an equivalent output frequency. Frequency is used as the output variable instead of a sinusoidal waveform to provide a convenient means of coupling to the frequency discriminator model which expects a frequency at its input.

Chapter 4

Simulation Results

Valuable insight into the predicted performance of the synthesizer can be obtained by developing complete open-loop and closed-loop simulation models using the functional models defined in Chapter 3. The use of these simulation models permits rapid exploration of the design space through modification of the synthesizer parameters. This reveals the effect these parameters have on the predicted loop stability, transient response and phase noise performance of the synthesizer.

4.1 Synthesizer Parameters

A synthesizer may be completely specified by the parameters defining its performance and characteristics. The following sections define the various parameters that characterize this synthesizer.

4.1.1 Bandwidth, Natural Frequency and Damping

Control theory allows one to describe the characteristics of any second-order loop using its bandwidth BW , natural frequency ω_n , and damping constant ζ . Although this synthesizer is unlike conventional PLL architectures, it may be described as a second-order system by recognizing the two integrators in the loop. The loop parameters are generally not independent which results in a compromise in performance. The target application of this synthesizer is primarily for frequency synthesis and as an FM modulator. This places constraints on the values of the synthesizer parameters.

Bandwidth (BW) is an important parameter which has a large influence on the overall performance of the synthesizer. A wide BW is desired for rapid acquisition and to stabilize short term jitter of the VCO [21]. This permits the synthesizer to be used in frequency hopping applications where the hopping rates are high. Frequency modulation is also possible with a wide BW . In this case the BW is chosen to be greater than the largest modulation frequency applied to the synthesizer's digital input. However, a wide BW may not be the best choice for optimal phase noise performance of the synthesizer due to other noise sources. There is an optimum loop BW that will minimize the phase noise at the output but choosing this will most likely compromise some other specification [22]. Another consequence of a wide BW in this synthesizer is that the phase margin is degraded leading to potential instability of the loop. This occurs because the loop BW approaches the decimated sampling rate f_{ref}/N where a rapid phase shift occurs due to the discrete-time architecture used in the synthesizer. With careful analysis of the performance specifications of the synthesizer, it is possible to choose a BW that provides an overall acceptable performance.

Since the loop compensation incorporates proportional plus integral control of the phase error, the choice of the natural frequency ω_n and the damping constant ζ may be made independent of each other [21]. This is accomplished by setting the gain of the proportional and integral terms in the DSP such that a sufficient phase margin exists to render the loop stable. Since the loop compensation network is digital, the proportional

and integral gains are quantized to a fixed number of bits which imposes a further constraint on the final values chosen for ω_n and ζ .

4.1.2 Frequency Resolution and Tuning Range

The tuning range of the synthesizer is limited by the input frequency range of the frequency discriminator. The frequency range of the second-order single-loop discriminator used in this synthesizer is from $(n+1)f_{ref}$ to $(n+2)f_{ref}$ where n is the lower modulus of the multi-modulus divider in the discriminator. This differs from the frequency range nf_{ref} to $(n+1)f_{ref}$ for the first-order discriminator described earlier, however both discriminators have an input frequency range equal to the reference frequency f_{ref} . Input frequencies above or below these limits will cause the discriminator to saturate resulting in a stream of ones or zeros at its output. This non-linear operation at frequencies below $(n+1)f_{ref}$ and above $(n+2)f_{ref}$ provide a frequency steering effect to pull the VCO back to the desired frequency. Extending the tuning range of the synthesizer can be accomplished by increasing the reference frequency to the limit imposed by the technology used to implement the discriminator. This also has beneficial effects on the noise shaping properties of the discriminator since increasing f_{ref} also increases the oversampling ratio. An alternative method to extend the tuning range is to extend the range of the divider moduli. This method has been successfully implemented in previous $\Sigma\Delta$ fractional-N synthesizers [23].

The frequency resolution of the synthesizer is determined by the number of frequency steps within its tuning range. The tuning range is simply f_{ref} but the number of frequency steps is determined by the synthesizer feedback path transfer function illustrated in Figure 4.1. The output of the discriminator is a quantized single-bit value representing the frequency of the VCO. This bitstream is decimated with a multi-stage comb filter to reduce the data rate and increase the resolution from a single bit to $\log_2(N^k)$ bits where N is the decimation ratio and k is the comb filter order. Further filtering is applied to the

comb filter output using single-stage FIR filters. These filters each have a DC gain of 2 which increases the frequency resolution by an additional bit for each stage. A final multiplication stage is used to increase the resolution by an additional 1 or 2 bits. The overall frequency resolution from all filter and gain stages becomes

$$\text{frequency resolution} = \frac{f_{ref}}{N^k K_{FIR} K_{mult}} \quad [Hz] \quad (4.1)$$

This corresponds to an input frequency word width of

$$\text{input frequency} = \lceil \log_2 (N^k K_{FIR} K_{mult}) \rceil \quad [bits] \quad (4.2)$$

From Equation (4.2) the frequency resolution is dependent on many parameters. However, some of these parameters also affect the noise performance and transient behaviour of the synthesizer so careful evaluation of their effect must be determined before choosing their values to set the frequency resolution.

4.1.3 Decimation Factor

One of the consequences of using an oversampled frequency discriminator in the synthesizer architecture is that eventually the data may have to be decimated to a more suitable rate for further signal processing. This is due to the limits on the processing speed of the DSP and the need to increase the resolution of the data from a single bit at a high rate to multiple bits at a lower rate. The decimation factor N is the difference between the oversampled rate and the resulting decimated rate and it influences a number of synthesizer parameters. The frequency resolution of the synthesizer is largely determined by the decimation factor. This results from the use of a third-order comb filter used to decimate the second-order noise-shaped bitstream from the discriminator.

From Equation (4.1), it follows that the frequency resolution is proportional to N^4 . There are limits to the maximum decimation factor N imposed by the comb filter and by the loop in general. The comb filter provides limited attenuation of the out-of-band quantization noise from the discriminator. If the decimation factor is too high, the amount of quantization noise power aliased into baseband will increase and degrade the signal to noise ratio (SNR) resulting in unacceptable synthesizer noise performance. The maximum amount of decimation using a multi-stage comb filter is limited to approximately four times the Nyquist rate defined by the loop bandwidth [15]. A more subtle stability problem exists within the loop itself for high values of N . This results from the discrete-time blocks in the synthesizer causing large phase shifts near the sampling frequency. Thus for a given loop bandwidth, there is a minimum sampling frequency (i.e. maximum decimation factor N) that still provides a sufficient phase margin to ensure loop stability.

4.2 Loop Stability

Stability is an important characteristic of any feedback control loop since instability results in oscillation and closed-loop control is lost. There are a number of ways of analyzing the stability of a time-invariant closed-loop system. If the transfer function of each block in the system is known, an analytical analysis of the open-loop poles and zeros can be done to determine if the system is stable. Often, the transfer function of the system is not known so this method is not possible. The PLL synthesizer described here is a mixed analog and digital system with time-variant sections in the DSP block. This introduces further difficulty in analyzing the stability of the PLL since the various methods assume a time-invariant system and are tailored for either a continuous-time or a discrete-time system. The time-variant characteristic of the PLL is evident only during transient conditions and is designed to prevent oscillation thus rendering the system stable. During steady-state conditions, the PLL is time-invariant and conventional stability analysis may be used. In a mixed analog and digital system, all the transfer

functions may be transformed into the continuous-time domain or discrete-time domain and subsequent pole/zero analysis can be applied. There are various transforms used to achieve this but they all distort the original transfer function to some degree. Another approach is to use Bode analysis which computes the magnitude and phase response of a system to determine if it is stable. The appealing characteristic of this method is that knowledge of the poles and zeros of the system are not necessary and mixed analog and digital systems can be easily analyzed. The Bode criterion for unconditional stability states that the open-loop gain must fall below unity (i.e. 0dB) before the phase shift reaches 180 degrees [21]. There are systems that are conditionally stable although they violate the Bode criterion [19]. In these cases, pole/zero analysis must be used to determine the exact conditions for stability.

Figure 4.1 Synthesizer closed-loop stability and phase noise model.

The Bode method is chosen to analyze the stability of the PLL synthesizer since it eliminates the problem of mixed continuous-time and discrete-time analysis of the poles and zeros of the system. The continuous-time and discrete-time models developed in Chapter 3 are used to construct the closed-loop model of the synthesizer shown in Figure

4.1. One exception is the model used for the discriminator which for stability analysis has been linearized. The reason for this is that the $\Sigma\Delta$ discriminator by definition is a non-linear unstable circuit and thus its average output value is used instead of its instantaneous output value. Since the discriminator input frequency range is from $(n+1)f_{ref}$ to $(n+2)f_{ref}$ and the average output bitstream value lies between zero and one, the linearized transfer function is expressed as

$$H(z) = \frac{1}{f_{ref}} \quad (n+1)f_{ref} < f < (n+2)f_{ref} \quad (4.3)$$

Although the synthesizer closed-loop model is made of continuous-time and discrete-time models, it is advantageous to map all models into the continuous-time domain in order to extract the various loop parameter relationships. In Chapter 3, the DSP block was transformed into the s-domain which remains valid as long as the bandwidth of the synthesizer is much less than the decimated sampling frequency f_{ref}/N . The resulting loop compensation transfer function is

$$H(s) = a_2 + \frac{(a_3\pi f_{ref})/3N}{s} \quad f \leq \frac{f_{ref}}{6N} \quad (4.4)$$

In a similar manner, the response of the loop (excluding the compensation network) can be mapped into the s-domain by noting that for frequencies within the loop BW, the loop appears as an integrator with a gain K' . This leads to the synthesizer open-loop transfer function

$$G(s) = \left[a_2 + \frac{(a_3\pi f_{ref})/3N}{s} \right] \frac{K'}{s} \quad f \leq \frac{f_{ref}}{6N} \quad (4.5)$$

Equation (4.5) reflects a second-order PLL with phase-lead compensation whose response

is shown in Figure 4.2.

Figure 4.2 Open-loop response of a second-order PLL with phase-lead compensation.

The relationship between the various loop parameters extracted from the PLL open-loop response $G(s)$ is

$$BW = \frac{a_2 K'}{2\pi} \quad [\text{Hz}] \quad (4.6)$$

$$\zeta = \sqrt{\frac{3N\pi(BW)^2}{K'f_{ref}a_3}} \quad (4.7)$$

$$a_2 = \frac{2\pi BW}{K'} \quad (4.8)$$

$$a_3 = \frac{3N\pi(BW)^2}{K' f_{ref} \zeta^2} \quad (4.9)$$

where BW is the loop bandwidth, ζ is the damping factor, a_2 is the proportional gain and a_3 is the integral gain. These parameters affect other loop characteristics but only their effect on loop stability is explored in this section.

The loop bandwidth is an important characteristic of a PLL and is easily adjusted by varying the open-loop gain K' as shown in Equation (4.6). This has no effect on the phase response of the PLL but it does change the available phase margin at the loop BW frequency (i.e. 0dB gain). As the loop BW increases, the available phase margin decreases until the PLL becomes unstable. This results in the open-loop response shown in Figure 4.3 where a rapid phase shift occurs as the BW approaches the decimated sampling frequency f_{ref}/N .

Figure 4.3 Open-loop response showing effect of bandwidth on loop stability.

If a wide bandwidth PLL is desired, the sampling frequency f_{ref} must be increased or the decimation factor N must be decreased to ensure loop stability. The upper limit on f_{ref} is determined by the technology used to implement the discriminator which operates at the oversampled rate. Varying the decimation factor also affects the noise performance and frequency resolution of the PLL which imposes constraints on its value. Since the values chosen for f_{ref} , N and BW depend on the technology used for implementation and the desired performance of the PLL, their choice is usually a compromise.

The damping factor ζ of this second-order PLL is affected by many parameters as shown in Equation (4.7). Parameters such as f_{ref} , N and BW are usually set by other synthesizer design constraints so the damping factor is determined by the ratio of the proportional and integral gains in the DSP block. The effect of varying ζ is to alter the phase margin at the 0dB gain frequency as shown in Figure 4.4.

Figure 4.4 Open-loop response showing effect of P/I gain ratio on loop damping factor.

Due to the finite resolution in the DSP block, the ratio of proportional gain to integral gain cannot be optimized but rather a ratio is chosen that provides a sufficient phase margin to ensure loop stability.

One of the parameters that has significant effect on the stability of the synthesizer is the accumulated delay around the loop. Delay causes a phase shift to occur which degrades the phase margin of a loop. In a mixed analog and digital PLL, delay is not a design parameter but rather a side-effect due to architecture implementation. The digital section of the synthesizer may introduce delay through pipelining and synchronizing circuits. This is usually necessary due to limitations in the speed of the technology used for implementation. Analog filters also introduce delay which causes unavoidable phase shift. The effects of delay introduced by the digital section on the stability of the loop is illustrated in Figure 4.5.

Figure 4.5 Open-loop response showing effect of digital delay on the loop stability.

The delay from analog filters is largely unavoidable but the digital delay can be minimized through careful implementation of the architecture. This may increase the complexity and the power consumption of the synthesizer so usually a compromise must be made.

4.3 Transient Response

The transient response of a synthesizer defines how the synthesizer will respond to any changes at its input. The current architecture of this synthesizer only permits a change in the digital input frequency which occurs during frequency hopping or frequency modulation. Acquisition is another highly non-linear phenomenon that is partially determined by the transient response of the synthesizer. In this section, the time-domain models developed in Chapter 3 are used to study the transient behaviour of the synthesizer.

Rigorous analysis of acquisition is difficult due to its non-linear behaviour so only a description of the acquisition process is presented here. During initial power-up, the synthesizer is out of lock and the VCO oscillates at an arbitrary frequency determined by the voltage at its tuning input. The key to acquiring lock is the presence of frequency steering in the loop. This is provided by the frequency discriminator which saturates with either a constant stream of ones or zeros when its frequency input is either above or below the valid input frequency range $(n+1)f_{ref}$ to $(n+2)f_{ref}$ respectively. When the decimated and filtered signal fed back from the discriminator is compared to the desired frequency, an error signal is generated that steers the VCO to the desired frequency and the loop acquires lock. Once the loop is locked, the discriminator monitors the phase of the VCO and provides corrective signals to compensate for any phase jitter. The discriminator can be compared to the phase-frequency detector (PFD) in a conventional PLL which provides an average frequency-steering error signal when the loop is out of lock and a subsequent compensating signal to correct for any VCO phase deviations.

After the loop acquires lock, its transient behaviour can be analyzed. The effect of various loop parameters on the transient response of the loop can be observed using the time-domain models developed in Chapter 3. Figure 4.6 shows a complete block diagram of the time-domain model used to simulate the transient response of the synthesizer. Since most of the synthesizer is discrete time, the transient simulation was performed in discrete time with sampling occurring at the discriminator oversampled rate f_{ref} . This method provides results with sufficient resolution, while maintaining a closed-loop simulation time much less than conventional techniques.

Figure 4.6 Time-domain synthesizer model used for transient analysis.

A common problem of any digital implementation of a closed-loop is the introduction of delays within the loop. Digital delays occur when pipelining is used to implement a function or as result of synchronizing circuits. There are also analog delays that exist within continuous-time filters and these are usually unavoidable. As explained earlier, delays degrade the phase margin of the loop and render the loop unstable if they are too large. The effect of delay in the time domain is shown in Figure 4.7 where the digital delay is varied in multiples of the clock period $1/f_{ref}$. The result of increased delay is an increase of oscillation before the frequency reaches steady-state. Since digital delay is constant over frequency, the response of the loop to a frequency step is

subsequently delayed by a corresponding amount. The effect of increased delay is similar to decreasing the damping factor of the loop. This is easily accomplished by varying the proportional to integral gain ratio in the DSP section.

Figure 4.7 Synthesizer transient response showing effect of digital delay on the loop stability.

Angle modulation and close channel spacing are possible if the synthesizer has a high frequency resolution. In this synthesizer the frequency resolution is determined by the DC gain in the feedback path since the frequency tuning range is constant. The type of decimation filter, the decimation factor N , the type of FIR filters and frequency scaling vary this gain and their combined effect determine the frequency resolution. The effect of frequency resolution on the transient response of the loop can be seen by observing the magnitude of the frequency error signal at the comparator output. When the resolution increases (i.e. through frequency scaling), the maximum error signal during a frequency step increases as well. This large error signal causes the DSP to saturate at a

constant value for a longer period before the transient decays. Since the DSP is followed by an analog integrator, the VCO will slew at a constant rate determined by its sensitivity K_v and the integrator time constant K_i as shown in Figure 4.8. The slew rate changes with frequency resolution since it is desirable to maintain a constant open-loop gain to keep the loop bandwidth the same. Thus as the frequency scaling is changed to vary the resolution, the overall loop gain is corrected by varying the analog integrator gain K_i .

Figure 4.8 Synthesizer transient response showing effect of frequency resolution on the slew rate.

4.4 Phase Noise

One of the most important parts of any synthesizer analysis is its phase noise performance. Noise sources that exist within the loop are all referred to the output of the VCO as phase noise and their noise contribution depends on their location and power.

In this synthesizer, there are three dominant noise sources

- frequency discriminator
- VCO
- analog loop filter

The following sections analyze each of these noise sources independently and their combined effect on the overall synthesizer phase noise.

4.4.1 Frequency Discriminator Phase Noise

The phase noise of the discriminator must be defined to determine its overall contribution to the synthesizer output phase noise. There are two methods of calculating the phase noise of the discriminator

- linear frequency domain
- non-linear time domain

The frequency-domain analysis is based on the linear discriminator model developed earlier, while the time-domain analysis uses the actual bitstream to compute the phase noise. Both methods are explored in the following section and their results are compared.

4.4.1.1 Linear Frequency-Domain Analysis

Using the linear model developed earlier, the output of the discriminator consists of the desired frequency and a frequency error due to quantization noise.

$$f_{out} = (n.f)f_{ref} + (1 - z^{-1})^2 f_{ref} E_n \quad (4.10)$$

where $(n.f)f_{ref}$ is the desired frequency and the remaining term is the frequency error. Defining $v(z)$ as the frequency error term and assuming a uniformly distributed error,

its power spectral density is

$$\begin{aligned}
 S_v(z) &= |(1 - z^{-1})^2 f_{ref}|^2 E_n \\
 &= |(1 - z^{-1})^2 f_{ref}|^2 1/12 f_{ref} \quad |Hz^2/Hz| \\
 &= |(1 - z^{-1})^4| f_{ref}/12
 \end{aligned} \tag{4.11}$$

Since phase error is the desired parameter, an integration must be performed. A rectangular integration in the z-domain yields

$$\Phi(z) = \left[\frac{2\pi}{f_{ref}(1 - z^{-1})} \right] v(z) \tag{4.12}$$

Thus the phase error spectral density is

$$\begin{aligned}
 S_\Phi(z) &= \left| \frac{2\pi}{f_{ref}(1 - z^{-1})} \right|^2 S_v(z) \\
 &= |(1 - z^{-1})|^2 \frac{(2\pi)^2}{12 f_{ref}} \quad |rad^2/Hz|
 \end{aligned} \tag{4.13}$$

Since the phase spectral density is two sided, the single-sideband (SSB) phase noise $\mathcal{L}(z)$ is

$$\mathcal{L}(z) = \frac{(2\pi)^2}{12 f_{ref}} |(1 - z^{-1})|^2 \quad |rad^2/Hz| \tag{4.14}$$

Converting this to phase noise power in a 1Hz bandwidth with respect to the carrier gives

$$\mathcal{L}(f)_{dBc} = 10 \log \left[\frac{(2\pi)^2}{12 f_{ref}} |(1 - e^{-j2\pi f T_{ref}})|^2 \right] \quad [dBc/Hz] \quad (4.15)$$

Equation (4.15) gives the phase noise spectral density in a form compatible with results obtained from experimental phase noise measurements.

4.4.1.2 Non-Linear Time-Domain Analysis

Time-domain phase noise analysis relies on the information embedded in the output bitstream of the discriminator. As defined earlier, the discriminator bitstream consists of the desired frequency and a frequency error. If the bitstream b is assumed to produce zeros or ones, then over a frequency range of f_{ref} the discriminator output is

$$\begin{aligned} f_{out,k} &= (n + \left(\sum_{i=1}^k b_i \right) / k) f_{ref} + v_k \\ &= (n.f) f_{ref} + v_k \end{aligned} \quad (4.16)$$

where the $(n.f)f_{ref}$ is the desired frequency. Subtracting the desired frequency from f_{out} isolates the frequency error v_k in the time domain. Since the frequency error spectrum is desired, multiple discrete Fourier transforms (DFT's) are used to compute an ensemble average of the bitstream in the frequency domain.

$$V(k) = \sum_{n=0}^{N-1} v(n) e^{-j(2\pi nk)/N} \quad (4.17)$$

After the appropriate scaling to account for windowing and various DFT sequence lengths, the frequency error spectral density S_e is computed with units of $(\text{Hz})^2/\text{Hz}$. A rectangular integration in the z -domain is required to convert from frequency to phase, thus the phase error spectral density becomes

$$S_\phi(z) = \left| \frac{2\pi}{f_{ref}(1 - z^{-1})} \right|^2 S_e(z) \quad [\text{rad}^2/\text{Hz}] \quad (4.18)$$

The phase error spectral density is one-sided, therefore the single-sideband phase noise $\mathcal{L}(f) = S_\phi(f)/2$. Converting this to phase noise spectral density with respect to the carrier power gives

$$\mathcal{L}(f)_{dBc} = 10 \log \left[\frac{S_\phi(f)}{2} \right] \quad [\text{dBc}/\text{Hz}] \quad (4.19)$$

This method of phase noise analysis is used to process the actual or simulated output of the discriminator by capturing the bitstream and post-processing it.

Figure 4.9 compares the results of the linear and non-linear discriminator phase noise analyses. The non-linear analysis gives a more accurate prediction of the phase noise since the model preserves the true non-linear behaviour of the discriminator.

Figure 4.9 Simulated frequency discriminator phase noise using linear and non-linear analyses.

4.4.2 VCO Phase Noise

Phase noise appearing at the VCO output is due to noise sources within the loop as well as noise generated by the VCO itself. It is desirable to characterize the VCO phase noise to predict its contribution to the total phase noise at the synthesizer output while under the influence of the loop. Since a discrete VCO is used in this synthesizer, the manufacturers specifications are used to characterize the VCO phase noise as shown in Figure 4.10. The phase noise is specified as the single-sideband (SSB) phase noise power with respect to the carrier power in a 1Hz bandwidth with units of dBc/Hz and is modelled as an additive noise source after the VCO.

Figure 4.10 Open-loop VCO phase noise.

The VCO phase noise power spectral density S_n can then be referred to the synthesizer output by calculating the transfer function from the noise source to the output.

$$\mathcal{L}(z) = |H(z)|^2 S_n(z) \quad [\text{dBc/Hz}] \quad (4.20)$$

From the block diagram in Figure 4.1, the output referred VCO phase noise becomes

$$\mathcal{L}(f)_{VCO} = \left| \frac{1}{1 + K(f)} \right|^2 S_n(f) \quad [\text{dBc/Hz}] \quad (4.21)$$

where $K(f)$ is the synthesizer open-loop gain. Figure 4.11 reveals the noise suppression of the loop within the loop bandwidth which reduces the VCO phase noise. Outside the loop bandwidth, the VCO phase noise has decreased to a level that is insignificant.

Figure 4.11 VCO closed-loop phase noise.

4.4.3 Analog Loop Filter Phase Noise

The analog loop filter implements the integration function in the synthesizer as well as the filtering of the D/A converter quantization noise. The filter is an active circuit which uses an operational amplifier (OP-AMP) as a gain block. The OP-AMP contains internal noise sources that must be accounted for in the calculation of phase noise. These noise sources are often specified as input referred equivalent noise voltage and noise current densities.

The noise voltage density is referred to the input of the filter as a voltage source at the inverting input as shown in Figure 4.12.

Figure 4.12 Noise voltage model of the analog loop filter.

Using the transfer function from the noise source to the OP-AMP output, $y_{o,v}$ is the output referred noise voltage density. If the input referred noise voltage density is V_n then the output noise voltage density is

$$V_{o,v}^2 = \left| \frac{(RC)s + 1}{(RC)s} \right|^2 V_n^2 \quad [V^2/Hz] \quad (4.22)$$

where RC is the integrator time constant.

The noise current density is also referred to the input of the OP-AMP and is modelled as a current source as illustrated in Figure 4.13.

Figure 4.13 Noise current model of the analog loop filter.

The output referred noise voltage density is calculated using the transfer function from the noise current source to the OP-AMP output yielding

$$V_{o,i}^2 = \left| \frac{1}{sC} \right|^2 I_n^2 \quad [V^2/Hz] \quad (4.23)$$

where a conversion gain from current to voltage has occurred.

Resistors in the loop filter contribute thermal noise that depends on their value. The noise voltage density of a resistor can be defined as

$$V_r = \sqrt{4K_B TR} \quad [V/\sqrt{Hz}] \quad (4.24)$$

where K_B is Boltzman's constant and T is the absolute temperature in degrees Kelvin [24]. The resistor thermal noise is modelled as a noise source in series with an ideal resistor and is depicted in Figure 4.14.

Figure 4.14 Resistor thermal noise model of the analog loop filter.

Similar to the OP-AMP noise sources, the output referred resistor thermal noise density derived from Figure 4.14 is

$$V_{o,r}^2 = \left| \frac{1}{(RC)s} \right|^2 V_r^2 \quad [V^2/Hz] \quad (4.25)$$

Since all noise sources in the loop filter are assumed to be uncorrelated, their respective noise powers may be summed to give the total noise power spectral density at the filter output.

$$V_{o,n}^2 = V_{o,v}^2 + V_{o,i}^2 + V_{o,r}^2 \quad [V^2/Hz] \quad (4.26)$$

This can be modelled as an additive noise source at the filter output as shown in Figure 4.15.

Figure 4.15 Total noise model of the analog loop filter.

4.4.4 Synthesizer Phase Noise

The total phase noise at the synthesizer output can be calculated from all the noise sources. Since each noise source is independent from all others, their power spectral densities can be summed to give the total noise power spectral density at the output [25]. Overlaying the independent output referred noise sources with the total synthesizer phase noise as in Figure 4.16, gives an indication of the dominant noise source at any given frequency.

Figure 4.16 Output referred synthesizer phase noise sources.

Since phase noise is an important PLL parameter, it is imperative to know the effect various PLL parameters have on the total phase noise. In this section, the effects that loop delay, bandwidth, damping factor and decimation factor have on the phase noise are explored.

In previous sections, delay in the loop has been shown to contribute to instability of the PLL. This was revealed as a decrease in the open-loop phase margin and excessive ringing in the transient response. Noise analysis uses the closed-loop response of the PLL to calculate the overall phase noise.

Figure 4.17 Synthesizer phase noise showing effect of digital delay in the loop.

Figure 4.17 shows that excessive delay in the loop causes instability and this results in the phase noise peaking at the loop bandwidth. If the delay is increased further, the loop will become completely unstable and lose lock. Loop delay is an undesirable side-effect of the implementation of the digital section and is also due to the phase shift in the analog filters of the synthesizer. In most cases the analog delay is unavoidable, but the digital delay should be minimized by optimizing the architecture of the digital section.

Bandwidth is a parameter that has a large influence on the phase noise and modulation capabilities of the synthesizer. A large bandwidth is desirable since VCO noise is suppressed within the loop bandwidth but adverse effects occur when the loop bandwidth is increased too far. When the loop bandwidth is increased, the open-loop

phase margin decreases which causes a decrease in loop stability. The effect on the phase noise shown in Figure 4.18 is a peaking near the loop bandwidth frequency

Figure 4.18 Synthesizer phase noise showing effect of loop bandwidth.

The response of the synthesizer to transients and its ability to phase lock to a reference has been shown to be partially dependent on the damping factor chosen. It also affects the overall stability of the loop by influencing the open-loop phase margin. The closed-loop response in Figure 4.19 indicates that the damping factor affects the phase noise in a manner similar to loop delay and bandwidth. This is indicated by the peaking of the phase noise near the loop bandwidth as the damping factor decreases.

Figure 4.19 Synthesizer phase noise showing effect of loop damping factor.

The decimation factor N predominantly sets the frequency resolution, but it has a subtle effect on the overall phase noise of the synthesizer. If the loop bandwidth is held constant as N is varied, then the open-loop phase response changes. This directly influences the phase margin and thus the stability of the loop. Previously, it was shown that the decimation factor has significant effect on the frequency resolution but although less pronounced, its effect on phase noise must still be considered when choosing N .

Chapter 5

Circuit Realization and Experimental Results

Realizing a design often represents an insurmountable task which is cluttered with technical details that delay the development of the final product. Technology issues frequently restrict the freedom in choosing specific design implementation paths. These issues must be resolved before any successful product can be realized. This chapter illustrates the design details used to realize a prototype synthesizer. Experimental test results of the synthesizer are also included to validate the theoretical analysis and simulation models developed earlier.

5.1 Design Parameters

Chapter 4 described the effect of the various synthesizer parameters on its features (i.e. resolution, tuning range etc.) and performance (i.e. phase noise, transient response etc.). This begins to define the design space that allows a working synthesizer to be constructed. The missing constraints result from the technology used to implement the synthesizer which frequently restricts the flexibility of the design the most.

The synthesizer was targeted for mobile personal communication applications where it could function as a local oscillator or as a modulator in transceivers.

This application clearly indicates the necessity for a design that is physically small and consumes little power.

The $\Sigma\Delta$ frequency discriminator is an oversampled, single-loop, second-order structure with a single-bit output bitstream. Higher order structures, although desirable, were not used since their stability becomes a problem that requires careful design to rectify. Implementation technology restrictions imposed limits on the maximum operational frequency of the discriminator, thus design parameters loosely targeted for analog cellular communications were chosen

- 860 to 870 MHz frequency tuning range
- 10MHz reference frequency

A second-order oversampled $\Sigma\Delta$ frequency discriminator requires a comb decimation filter of order $k=3$ to sufficiently filter the quantization noise [17]. This filter is suitable when decimating to approximately four times the Nyquist rate defined by the loop bandwidth. The decimation factor N also affects the frequency resolution and the stability of the synthesizer. Choosing a large value for N yields a high resolution but reduces the phase margin so a compromise must be made. In this design, a decimation factor $N=10$ was chosen to maximize the resolution while still providing a sufficient phase margin.

The comb filter contributes the most to frequency resolution since its DC gain is N^k . Additional resolution is provided by the FIR filter following the comb decimation filter and by scaling the signal. This gives a frequency resolution

$$resolution = \frac{f_{ref}}{N^k K_{FIR} K_{MULT}} \quad [Hz] \quad (5.1)$$

which corresponds to an input frequency word width

$$f_{in} = \lceil \log_2(N^k K_{FIR} K_{MULT}) \rceil \quad [bits] \quad (5.2)$$

The synthesizer bandwidth (BW) is an important parameter whose value is governed by the application. In modulators, a large modulation BW is necessary to permit the synthesizer to track the modulation signal adequately while for local oscillators a BW that minimizes phase noise is desired. Excessive BW also degrades the synthesizer phase margin imposing an upper limit on its value. Clearly, a compromise must be made when choosing a BW in most synthesizer designs such that sufficient modulation BW is available with adequate noise suppression. In this architecture, the BW is

$$BW = \frac{a_2 K'}{2\pi} \quad [Hz] \quad (5.3)$$

where K' is the loop gain and a_2 is the proportional gain of the synthesizer. A 50KHz BW was chosen in this implementation to provide a reasonable modulation BW with acceptable overall phase noise.

In this synthesizer architecture, the damping constant ζ is controlled independently from the natural frequency ω_n by varying the proportional and integral gains in the DSP block. The proportional gain a_2 and integral gain a_3 are restricted to integer powers of 2 to minimize the hardware implementation of the compensation network. In most cases, a damping factor of at least one is necessary to ensure stability of the synthesizer although values greater than two are not uncommon. The damping constant is defined as

$$\zeta = \sqrt{\frac{3N\pi(BW)^2}{K'f_{ref}a_3}} \quad (5.4)$$

where K' , f_{ref} and a_3 are the loop gain, oversampling frequency and integral gain respectively.

The transient response of the synthesizer is largely determined by the dynamic range of the digital to analog (D/A) converter. If the D/A converter range is small, the VCO will slew during input transients due to the constant D/A converter output being

integrated by the analog integrator. This in itself is not serious if the settling time is still acceptable but there is a minimum dynamic range that is determined by the steady-state operation of the synthesizer. Similar to conventional oversampled $\Sigma\Delta$ modulators, the $\Sigma\Delta$ frequency discriminator maintains a certain amount of small signal activity once its output has been decimated. This is due to the $\Sigma\Delta$ noise shaping action that occurs on the low-order bits. This small-signal activity must not be truncated in order to preserve the noise shaping so the D/A converter dynamic range must be large enough. The exact amount of steady-state small-signal activity is difficult to predict analytically, but simulations can reveal the dynamic range of the discriminator signal. Simulation results on this architecture indicate less than 8 bits of small-signal activity exists during steady-state operation. However, a 12 bit D/A converter was chosen to increase the slew rate of the synthesizer, thereby improving its transient response.

5.2 Circuit Realization

The entire synthesizer was realized on multiple printed circuit boards using various technologies (see Appendix A). This approach was used to permit rapid change of the design architecture to evaluate various methods of improving the performance and features of the synthesizer.

The frequency discriminator was realized using discrete components on a multi-layer printed circuit board (see Appendix C). Since the input frequency is near 1GHz, emitter coupled logic (ECL) is used throughout the circuit to achieve high switching speed and small propagation delays. Discrete ECL logic has high power consumption due to the low impedance interconnect between devices, however the power consumption can be drastically reduced by integrating all the ECL logic once the discriminator design is complete.

The digital hardware following the discriminator is implemented in one field programmable gate array (FPGA) which reduced the number of digital components

substantially (see Appendix B). Using FPGA's along with the appropriate design environment permits design changes to be implemented quickly.

The remaining analog hardware consists of the D/A converter, integrator and the RF section. Once again, discrete components are used to realize the analog section for flexibility. The RF section employs micro-strip techniques to provide proper matching between devices.

5.2.1 $\Sigma\Delta$ Frequency Discriminator

The frequency discriminator hardware is divided into sections which are described below. Together these sections realize the single-loop frequency discriminator model developed in Chapter 3.

5.2.1.1 Multi-Modulus Divider

The input to the multi-modulus divider is the VCO signal and thus it operates at the highest rate. This RF signal is AC coupled and differentially amplified to interface with the ECL divider differential input. It is imperative to use micro-strip transmission line techniques at the divider input to ensure proper impedance matching and correct operation.

The frequency discriminator used in this synthesizer is the single-loop design described earlier. The $(2-z^{-1})$ feedback block shown in the previous model (see Figure 3.7) is implemented in the divider shown in Figure 5.1 by controlling its lower 2 modulus control bits thus effectively performing the multiply by 2 operation.

Figure 5.1 Realization of the single-loop discriminator feedback function using the control inputs of the multi-modulus divider.

This implies that the divider is a multi-modulus structure which requires 2 modulus control bits to select from 1 of 4 divide moduli. The multi-modulus divider is a more complex structure than the simpler dual-modulus divider used in multi-loop discriminators but the single-loop discriminator performance justifies its use.

5.2.1.2 Phase-Frequency Detector

The frequency discriminator is a phase-controlled closed-loop circuit and thus it requires a phase-frequency detector (PFD) to initially steer the loop until locked and subsequently provide a measure of the phase error. The transfer characteristic of the PFD is shown in Figure 5.2. A differential ECL PFD with UP and DOWN outputs is used to interface with the divider output and the differential integrator. The ECL detector is only clocked at the 10MHz reference frequency but its fast switching speed minimizes the non-linear effects caused by its dead-zone.

2 of/de 2

PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

Figure 5.2 Phase-frequency detector transfer characteristic.

It is important to minimize the width of the dead-zone caused by the PFD detectors inability to generate the narrow UP and DOWN pulses. In the dead-zone, the PFD has no gain and the discriminator operates in open-loop mode. This causes short limit cycles (i.e. streams of zeros or ones) to occur in the output bitstream and degrades the discriminators quantization noise shaping. This problem can be eliminated by inducing a constant phase offset to prevent the PFD from operating in its dead-zone during locked conditions.

Figure 5.3 Constant phase offset resulting from the phase-frequency detector operating away from its dead-zone.

However, this results in a constant phase error between the divided-down input frequency and the reference frequency as illustrated in Figure 5.3. This constant phase error is minimized by introducing only enough phase offset to prevent the PFD from operating in its dead-zone.

5.2.1.3 Analog Integrator

The analog integrator converts the UP and DOWN pulses from the PFD into an analog voltage that is later quantized. It also implements the second integrator in the discriminator model thus making the discriminator a second-order structure. The integrator in Figure 5.4 is realized using an operational amplifier (OP-AMP) with differential inputs.

Figure 5.4 Active integrator with phase offset current injection.

The constant phase offset which shifts the PFD operation away from its dead-zone is produced by injecting a constant current into the OP-AMP's inverting input. This causes the integrator output to ramp towards the power supply rail. The action of the loop is to provide a continuous DOWN pulse which pulls the integrator output back towards 0V.

The inputs to the integrator are the low-active UP and DOWN pulses from the phase detector which are integrated differentially to produce an output voltage

$$v_o(t) = \frac{-1}{RC} \int [v_u(t) - v_d(t)] dt \quad (5.5)$$

Since the inputs to the integrator are pulses, the output will be a ramp in voltage with a slew rate (SR) determined by the differential input step size and the integrator time

constant RC .

$$SR = \frac{\Delta v}{RC} \quad [V/s] \quad (5.6)$$

The maximum differential input voltage is approximately 1V determined by the ECL logic levels. In order to prevent non-linear effects due to OP-AMP slewing, a constraint is put on the minimum integrator time constant RC . However, the unity gain bandwidth (UGBW) of the integrator should be greater than the input pulse rate defined by the reference frequency f_{ref} . This imposes an upper limit on the integrator time constant. Satisfying both these constraints requires an OP-AMP with a very high slew rate which leads to potential stability problems without careful design.

5.2.1.4 Quantizer

The voltage generated by the analog integrator represents the average phase error between the divided-down input frequency and the reference frequency. This voltage is quantized into a one-bit number and fed back to control the divider modulus.

Figure 5.5 Realization of the single-bit quantizer using an analog comparator and latch.

The quantizer shown in Figure 5.5 is implemented with an analog comparator and a transparent ECL latch. The comparator compares the input level to the 0V reference level and its output swings to an ECL high or low depending on which is greater. Once the comparator has settled, its output is latched. Since the comparator has a very high gain, some hysteresis is necessary to prevent it from oscillating. The hysteresis has a detrimental effect on the overall discriminator operation since it prevents the comparator from responding linearly to the analog input voltage from the integrator. This causes small limit cycles (i.e. streams of zeros or ones) to occur at the quantizer output and degrades the quantization noise shaping properties of the discriminator.

5.2.1.5 Timing Control

The overall timing of the discriminator is crucial to its correct operation. In this implementation, the timing signals are generated by ECL programmable array logic (PAL) devices. This reduced the total number of discrete logic devices and provided the flexibility for architecture modifications. Figure 5.6 shows a typical timing diagram for the discriminator in locked condition with various points marked for reference.

Figure 5.6 Single-loop $\Sigma\Delta$ frequency discriminator timing diagram.

The criteria for the discriminator to be stable requires that one delay occurs around the loop for every reference clock cycle. Analytically, this is represented by a z^{-1} delay somewhere in the loop. However, in the hardware, this delay is distributed throughout

the loop in $z^{-1/5}$ (i.e. 1/5 of a reference cycle) increments. The reason for this is that most digital logic has finite setup and hold times that must be met for correct operation. Additionally, the analog circuits have finite settling times before their outputs become stable. Thus the reference is a 50MHz clock that is divided into 5 phases (denoted by S_0 , S_1 and S_2 in Figure 5.6) to provide the fractional delays.

Points 1 and 2 show the constant phase offset resulting from shifting the phase detector operating region out of its dead-zone. This produces the DOWN pulses at point 3 causing the analog integrator to ramp up. During the period when DOWN is inactive (i.e. high), the offset current injected into the integrator causes its output to ramp down again thus maintaining a constant average value.

At point 4 the divider's terminal count is active and its modulus is adjusted depending on the current value of the divider modulus control inputs. It is imperative that the current modulus control inputs (P_0 and P_1) for the upcoming cycle are based on the previous value of the bitstream L_0 . This gives a total delay around the loop of one reference cycle which ensures correct operation of the discriminator. A change in the divider modulus causes the divider output edge at point 2 to shift with an average displacement from the reference edge at point 1 equal to the phase offset.

The rising edge of the reference at point 1 enables the comparator to sample the integrator output and this value is latched on the falling edge of LEN at point 5. The divider modulus control input (P_0 and P_1) is derived from the bitstream L_0 . Recall that the feedback path of the discriminator has a $(2-z^{-1})$ block. The gain of 2 is implemented by controlling the P_1 input to the divider which has a weighting of 2^1 . The negative z^{-1} term is simply an inverted version of the bitstream delayed by one reference clock cycle that controls the divider P_0 input. The divider modulus control signals derived from the latched comparator output are indicated by points 6 and 7.

5.2.2 Comb Decimation Filter

Direct implementation of the third-order comb filter described in Chapter 3 was chosen to simplify the hardware architecture by eliminating any multiplexing. There is a slightly higher complexity associated with this technique but it is acceptable for this application. Figure 5.7 shows the comb decimation filter architecture consisting of an oversampled infinite impulse response (IIR) section and a finite impulse response (FIR) section operating at the decimated rate. Since modulo arithmetic is used throughout the comb filter, a word width of

$$\lceil \log_2 (N^k + 1) \rceil \quad [bits] \quad (5.7)$$

is used to satisfy the constraints for proper filter operation [15].

Figure 5.7 Realization of the third-order comb decimation filter.

The integrators in the IIR section operate at the oversampled rate f_{rep} , therefore special techniques are used to reduce the propagation delay thereby increasing their

processing speed. High speed digital signal processing (DSP) circuits frequently employ pipelined architectures to reduce the effective propagation delay through each functional block. There is still an initial latency (i.e. delay) as the pipeline fills, but thereafter maximum processing throughput is achieved. Pipelining is not a viable solution whenever recursion (i.e. feedback) is necessary to implement a function due to the delay through the pipeline. Since the integrators in the comb filter are recursive, other techniques must be used to increase their respective processing speed, but pipelining is used between each integrator to increase the processing speed with minimal additional delay. Each integrator's speed may be increased by using carry look-ahead techniques to reduce the delay associated with the carry ripple between stages of the adder [26]. The advantage of carry look-ahead architectures becomes significant as the word width increases but their complexity increases rapidly. The approach used in designing the comb filter integrators is a combination of three 4-bit carry look-ahead adders cascaded to form a 12-bit integrator. This integrator architecture shown in Figure 5.8 results in an acceptable compromise of speed and complexity for this application.

Figure 5.8 Typical carry look-ahead architecture of the comb filter integrators.

The decimator is simply a register clocked at the decimated rate to effectively undersample the digital signal from the integrators by a factor of N . The decimator clock is derived from the oversampled clock to ensure synchronous operation.

Once the signal is decimated, the data rate is reduced to f_{ref}/N , so the speed requirements of the differentiators are relaxed. Standard ripple carry subtractors implement each differentiator for a low complexity realization. The propagation delay of each differentiator is small enough that three of them may be cascaded together without pipelining with an overall worst case propagation delay less than the decimated clock period N/f_{ref} .

5.2.3 FIR Filter

The architecture of the FIR filter following the comb decimation filter is very similar to the differentiator except an addition occurs instead of a subtraction. This simple architecture results from the necessity to use minimal tap FIR filter structures with integer power of 2 multiplier coefficients as explained in Chapter 4. The basic FIR filter structure implements the transfer function

$$H(z) = 1 + z^{-1} \quad (5.8)$$

and can be realized with a standard ripple carry adder since it operates at the decimated rate f_{ref}/N . The DC gain of the filter is 2, so an additional output bit is required to prevent overflow. These FIR filter structures may be cascaded to implement more complex transfer functions with only a width increase of one bit per stage and minimal additional delay.

5.2.4 Digital Signal Processor

Figure 5.9 Realization of the digital signal processing block and data synchronizer.

The digital signal processing block of Figure 5.9 is divided into a frequency comparison section and a loop compensation section.

The frequency comparator compares the decimated discriminator frequency to a reference frequency to produce an error frequency. The frequency error is simply the difference between the two frequencies and is realized using a signed arithmetic subtracter. Since the DSP block operates at the decimated rate f_{ref}/N , high speed is not necessary so a standard ripple carry subtracter is used to reduce the hardware complexity.

The loop compensation network in conjunction with the analog integrator provides proportional and integral control of the phase error as described in Chapter 3. The frequency error is converted to a corresponding phase error θ_e through an integration and summed with a derivative term $\partial\theta_e$. This is illustrated in Figure 5.9 where θ_e and $\partial\theta_e$ are scaled using multipliers with integer power of 2 coefficients for reduced complexity. The final integration occurs in the analog integrator (not part of the DSP) to give the phase error θ_e and the integral of phase error term $\int\theta_e$.

The output of the DSP block is converted to an analog correction signal through a D/A converter. It is important to prevent input range overflow in the D/A converter which would cause unstable synthesizer operation due to limit cycles. Thus it becomes necessary to use two's complement saturation arithmetic to prevent internal overflow of the nodes in the DSP block. This is especially important with digital integrators since they are inherently unstable and would otherwise overflow with a constant input. The saturating integrator and saturating adder both employ detection logic that senses if the current output would overflow or underflow preset limits. If these conditions exist then the output saturates at the preset value and prevents any limit cycles from occurring.

The quantization noise shaping of the frequency discriminator maintains a minimum level of small signal activity (i.e. active low-order bits) during steady-state operation which imposes constraints on the minimum internal node widths. Additionally, any gain stages (i.e. multipliers) increase the signal's dynamic range and therefore the width of the following node must increase accordingly. During steady-state operation, it is important to ensure that all nodes are wide enough to prevent them from overflowing (or saturating) which induces highly non-linear operation of the synthesizer [27]. Initial acquisition and frequency hopping cause large transients to occur and saturation of the DSP block is inevitable.

The entire DSP block in Figure 5.9 operates asynchronously to minimize delay and this introduces timing problems caused by data skew through the various stages. Unsynchronized data causes glitches at the DSP output and result in large spikes produced by the D/A converter since its inputs are unregistered (i.e. transparent). The data is synchronized through a register with enough delay to compensate for the DSP propagation delay. The synchronizer also serves as a translator to convert the two's complement output of the DSP to the offset binary input required by the D/A converter.

5.2.5 Digital to Analog Converter

The digital to analog (D/A) converter serves as an interface between the digital signal processing section and the analog section that follows. The synthesizer design parameters impose constraints on the minimum D/A resolution, full-scale output and whether a unipolar or bipolar output is required. This may be further complicated by additional problems encountered when trying to design the D/A converter circuitry. When high speed and high resolution are combined in the digital to analog conversion, certain design issues must be addressed to ensure satisfactory operation. In this synthesizer, the digital to analog conversion is realized using a high speed integrated D/A converter with twelve bits of resolution and bipolar outputs.

An important characteristic of any D/A converter is its output settling time. Fast settling is especially important in this case, since the analog integrator that follows the D/A converter continuously monitors its output. Any transients during switching appear as an undesired error signal in the forward path of the synthesizer. One method of reducing the settling time is to lower the output impedance of the converter and minimize parasitic capacitance at its output. This minimizes the time it takes for the output to settle at the expense of higher current due to the lower impedance. Limiting the output voltage range of the converter also reduces the settling time by minimizing the time during which the output is slewing to a new value. The slew rate is usually limited by the output current sources in the D/A converter. This has an added benefit, since a reduced output range also reduces the slew rate requirements of the analog integrator that follows the converter. In most cases, a compromise must be made to achieve fast settling with acceptable power consumption.

Data skew from unmatched digital inputs to the D/A converter generate glitches, where the output momentarily has an invalid value during switching. This glitch energy produces undesired spikes at the D/A converter output. Data skew is caused by both digital and analog phenomena and various methods can be used to reduce it. Data skew arising from the different propagation delays (i.e. t_{PHL} and t_{PLH}) in large

asynchronous digital circuits can effectively be reduced by synchronizing the parallel data. This reduces the data skew to that of the mismatch in the synchronizing circuit outputs. However, if the parallel data interfaces with printed circuit board (PCB) traces (or any other medium), then additional data skew may be introduced by transmission line effects. Proper transmission line techniques must be implemented to reduce reflection and ensure matching between the data lines. Even this may not be sufficient and a low-pass RC filter in the data lines may be used to introduce some passive delay to minimize the data skew. Figure 5.10 illustrates the use of these techniques to minimize data skew.

Figure 5.10 Off-chip data synchronization using passive filters.

Digital feed-through is a problem with any high speed converter that couples the noisy digital environment to the sensitive analog domain. It is impossible to completely isolate the spectral components of a high speed digital signal from the analog portions of a D/A converter, so inevitably these spectral components find their way onto the sensitive analog nodes. It is important to isolate the digital and analog sections of the converter as much as possible through the use of separate ground planes and careful consideration of the signal paths. Spectral components coupled through the digital data input lines may be reduced by passive RC filters in each line. However, it is important to not filter too many

harmonics, since this increases the switching time and may degrade the performance of the converter.

5.2.6 Analog Loop Filter

The analog integrator in conjunction with the digital zero in the DSP block forms the integrator with phase lead compensation network. It also filters the quantization noise from the D/A converter and provides additional loop gain for fine adjustment of the open-loop gain. The realization of the integrator must consider these factors in addition to the non-ideal effects of the hardware used to implement it.

The integrator is a single-ended active circuit using an OP-AMP for the gain stage. The input signal consists of a series of voltage steps from the D/A converter which change at the decimated clock rate and have a maximum range equal to the full-scale output of the converter. The time-domain response of the integrator is to produce a ramp in the direction set by the polarity of its input at a rate defined by the RC time constant.

$$v_o(t) = \frac{-1}{RC} \int v_i(t) dt \quad (5.9)$$

It is important to prevent non-linear operation due to OP-AMP slewing so its slew rate (SR) must exceed the limit set by the worst case input

$$SR = \frac{\Delta v/2}{RC} \quad [V/s] \quad (5.10)$$

where Δv is the full-scale output range of the D/A converter.

The integrator time constant RC is adjustable in this implementation to vary the open-loop gain which compensates for changes in the VCO's tuning sensitivity K_v . The

change in sensitivity is caused by the non-linear tuning characteristic of the VCO and component tolerances. The gain adjustment also permits the PLL bandwidth to be changed.

Since the D/A converter has a finite step size, it introduces quantization noise at its output. Fortunately, this quantization noise is shaped by the frequency discriminator such that most of the noise energy lies outside the PLL bandwidth and is subsequently filtered. However, residual noise remains and the analog integrator provides additional filtering to reduce the noise level.

During loop acquisition, a potential problem exists that the linearized models do not predict. Upon initial power-up of the synthesizer, it is possible for the integrator to saturate to the negative rail due to initial circuit conditions. Simulation indicates that the VCO would oscillate at its minimum frequency and the loop would eventually lock. Practically, many VCO's cease to oscillate when their tuning input is below 0V. This poses a serious problem in this synthesizer, since the frequency discriminator will produce either a stream of zeros or ones (i.e. $f_{\min}$ or $f_{\max}$) with no input signal. If a stream of ones occur, the PLL will erroneously produce an error signal to reduce the VCO frequency and the loop will never lock. The solution to this problem is to limit the maximum negative output of the integrator with the clamping circuit depicted in Figure 5.11.

Figure 5.11 Analog integrator with output voltage clamp.

If the integrator starts saturating toward the negative rail, the diode conducts and clamps the output voltage just below 0V which allows the VCO to continue to oscillate at its minimum frequency. The corrective action of the loop will eventually steer the VCO

back to the correct frequency and the loop will become locked.

5.2.7 Voltage-controlled Oscillator

The voltage-controlled oscillator (VCO) in this synthesizer implementation is a discrete version in a shielded package for improved phase noise performance. A commercially available VCO was used instead of developing a custom design because the emphasis of this research lies in the architecture of the synthesizer and not the VCO. The VCO drives the frequency discriminator in the feedback path and the surrounding circuitry (e.g. mixer, antenna etc.) so its output must be divided. Since the output frequency range of the synthesizer is near 1GHz, proper RF micro-strip design techniques are used to ensure proper impedance matching between devices. Additional gain stages are necessary to compensate for passively splitting the VCO power into two paths, and to provide sufficient power levels to drive the discriminator and the synthesizer output. A monolithic amplifier with sufficient gain and bandwidth was used to provide the additional gain.

5.3 Measured Results

Experimental testing of the synthesizer, provides a means of characterising its phase noise performance and transient response. The phase noise performance of a synthesizer limits the overall signal-to-noise ratio (SNR) of a frequency modulated receiver and has an influence on its sensitivity to strong interferers in adjacent channels. The synthesizer transient response reveals how well it recovers from external frequency steps. This characteristic is important in systems that use spread spectrum techniques which require the carrier to hop from frequency to frequency. It also provides an indication of the stability of the synthesizer.

The phase noise of the synthesizer was measured using industry standard phase noise measurement techniques (i.e. HP3048 phase noise measurement test setup). The frequency discriminator was also tested independently, to evaluate its open-loop phase noise performance. This was necessary since there is no loop suppression of the discriminator phase noise inside the PLL bandwidth, consequently, it becomes a significant contributor to the overall synthesizer phase noise.

The synthesizer transient response was measured using a frequency vs time interval analyzer with an externally controlled input frequency step. The input frequency step size was varied to permit the small signal and large signal transient behaviour of the synthesizer to be characterized.

The measured results are compared to the simulated results to validate the theoretical models used in the analysis section of Chapter 3.

5.3.1 Phase Noise

Open-loop testing of the frequency discriminator reveals its true phase noise shaping characteristics. The measured and simulated (non-linear method) phase noise of the discriminator is illustrated in Figure 5.12.

Figure 5.12 Measured and simulated frequency discriminator phase noise.

The measured phase noise corresponds to the simulated phase noise at offsets greater than 10KHz where the 20dB/decade phase noise shaping characteristic of the second-order discriminator is clearly visible. Near the carrier, the phase noise is not shaped and is essentially white with a density of -90dBc/Hz. This degradation in noise shaping is caused by non-linearities (e.g. offsets, parasitics etc.) in the discriminator implementation. Integrated versions of this discriminator should reduce these non-linearities and offer better phase noise performance. The overall effect of the degraded discriminator performance on the synthesizer phase noise is shown in Figure 5.13.

Figure 5.13 Synthesizer phase noise using measured and simulated discriminator phase noise.

The synthesizer close-in phase noise is clearly dominated by the discriminator phase noise in the measured case.

The synthesizer phase noise was measured at several carrier frequencies to give an indication of its performance over the tuning range. Figure 5.14 shows the measured phase noise at the synthesizer centre frequency.

Figure 5.14 Measured synthesizer phase noise at 865MHz.

Within the PLL bandwidth, the phase noise is essentially white with an average density of -90dBc/Hz. This differs from the simulated phase noise in Figure 5.13 where the close-in synthesizer phase noise is below -120dBc/Hz. The difference can be accounted for by the lack of noise shaping of the frequency discriminator at small offsets from the carrier frequency which was described earlier. Better synthesizer phase noise performance can be achieved by improving the discriminator performance.

The close-in spurs in Figure 5.14 are caused by power supply noise (i.e. power line frequency and harmonics) and external interference. Improvements can be made by using on-board supplies that are well regulated as opposed to laboratory power supplies. Frequency spurs at 1MHz and its harmonics are due to clock feed-through from the DSP section into the analog section. Some of this noise is directly coupled through the D/A converter as glitch energy and results from data skew at the D/A converter input. Cross-coupling of the digital switching noise into the analog section is also a source of these spurs and may be reduced through careful layout of the signal lines and control of

the digital and analog ground planes.

Figure 5.15 illustrates the phase noise at a carrier frequency that is a small offset (i.e. less than the PLL bandwidth) from the 865MHz centre frequency of the synthesizer.

Figure 5.15 Measured synthesizer phase noise at 865.01MHz.

In this case, there are additional spurs at twice the 10KHz frequency offset from the synthesizer centre frequency and its harmonics (i.e. 20KHz, 40KHz, 60KHz etc.). These spurs are caused by the frequency discriminator and reveal a potential problem with the second-order structure used in this implementation. Oversampled $\Sigma\Delta$ frequency discriminators (or $\Sigma\Delta$ modulators in general) employ noise shaping to shift most of the quantization noise away from baseband. However, lower order structures do not introduce enough randomization which causes discrete tones to exist [28]. These tones are caused by periodicity of the oversampled bitstream and result in discrete spurs in the frequency spectrum of the discriminator output. Higher order frequency discriminators further randomize this noise and provide better noise shaping characteristics, but it is difficult to design stable high-order structures. Alternatively, some form of spur cancellation could

be used to remove the spurs inherent to lower-order frequency discriminators.

Figure 5.16 Measured synthesizer phase noise at 862.54MHz.

Figure 5.17 Measured synthesizer phase noise at 867.42MHz.

Figures 5.16 and 5.17 show the phase noise of the synthesizer near both ends of its tuning range. At these carrier frequencies, the spurs caused by cyclostationary noise in the discriminator lie outside the PLL bandwidth and are subsequently suppressed by the loop.

5.3.2 Transient Response

Small signal transient behaviour exists when the input frequency modulation causes the synthesizer to operate in a linear fashion. Similar to many PLL architectures, this implies that the synthesizer must be able to track the input signal with little error. Figure 5.18 shows the measured and simulated transient response of the synthesizer for an input frequency step of 640KHz. This step size maintains small-signal behaviour evident by the overshoot and undershoot of the synthesizer transient response.

Figure 5.18 Measured and simulated synthesizer transient response with 640KHz frequency step.

Large signal operation occurs when the synthesizer operates in a non-linear mode. This occurs during acquisition after the synthesizer loses lock following an input transient. In this architecture, non-linear operation also occurs when the DSP section saturates due to large error signals. Figures 5.19 and 5.20 show the effects of non-linear operation during a large signal transient condition resulting from input frequency steps of 1.28MHz and 2.56MHz respectively. This is evident by the initial slewing of the frequency following the transient and is caused by the DSP saturating. Non-linear behaviour is also visible during the settling time which exhibits no undershoot.

Figure 5.19 Measured and simulated synthesizer transient response with 1.28MHz frequency step.

Figure 5.20 Measured and simulated synthesizer transient response with 2.56MHz frequency step.

Chapter 6

Conclusions

The growing popularity of digital mobile radio used in personal communication applications has led to the demand to develop technologies and novel architectures that meet these system requirements in a feasible manner. The innovative contribution of this thesis is the design, simulation and experimental characterization of a novel $\Sigma\Delta$ frequency discriminator based synthesizer architecture suitable for digital mobile radio.

A systematic review of previous synthesizer structures indicated that fractional-N architectures offered the high resolution without high complexity required for mobile digital radio applications. The synthesizer architecture presented in this thesis had several advantages over previous fractional-N architectures. It used a single-loop oversampled $\Sigma\Delta$ frequency discriminator in the feedback path to convert the VCO frequency to digital form. This resulted in a largely digital architecture that eliminated many of the analog noise sources that plagued conventional fractional-N synthesizers.

Detailed system and component simulation models were developed to provide insight on the predicted stability, transient response and phase noise performance of the synthesizer. Time-domain and frequency-domain analyses identified the effects of the synthesizer parameters on its performance and resulting architectural complexity. This provided boundaries on the design space when a practical synthesizer design was implemented for experimental testing.

This architecture is suitable for monolithic integration in a BiCMOS (bipolar and CMOS) process due to the large proportion of digital components. However, a discrete printed circuit board implementation was chosen to provide flexibility in rapid exploration of the synthesizer parameters. The use of a field-programmable gate array (FPGA) for the digital section proved invaluable when testing architectural design changes. Dynamic digital control of the loop parameters was possible through the conversion of the VCO frequency to digital form by the $\Sigma\Delta$ frequency discriminator. This differs from conventional fractional-N synthesizers where the loop parameters are controlled using analog techniques and are usually fixed.

Experimental measurement of the synthesizer phase noise demonstrated a level of -93dBc/Hz at a 10KHz offset. Initial simulations indicated a lower level limited by the analog loop filter of -122dBc/Hz at a 10KHz offset. Investigation revealed that the frequency discriminator provided inadequate noise shaping inside the PLL loop bandwidth and it was the limiting factor in the phase noise performance. Simulations using the measured discriminator phase noise predicted a synthesizer phase noise that correlates with the measured results.

The spurious performance of this synthesizer was better than -50dBc inside the PLL loop bandwidth. These spurs arise from the presence of cyclostationary phase noise due to incomplete $\Sigma\Delta$ noise shaping in the frequency discriminator. They are most prominent at frequencies that are a small offset (i.e. $<$ loop bandwidth) from the synthesizer centre frequency. Better randomization of the quantization noise can be achieved through higher order discriminator structures. Spurs outside the loop bandwidth can be attributed to reference clock feed-through from the digital section of the synthesizer and can be minimized through careful design of the D/A converter and signal interconnects.

Measurement of the transient response of the synthesizer was performed by modulating the digital input with various frequency step sizes. This provided a means to test both the small signal and large signal behaviour of the synthesizer. For small frequency steps (i.e. $<640\text{KHz}$), the loop remains locked and the DSP compensation network does not saturate. This resulted in a linear transient response with settling times $<35\mu\text{s}$ which corresponds with the simulated response. Large signal behaviour occurred when large frequency steps were used as input stimulus. This is characterized by the initial increased slew-rate limiting and the non-linear response (i.e. no frequency undershoot) of the synthesizer during settling. Settling times of $<50\mu\text{s}$ were observed for large frequency steps consistent with simulated results.

6.1 Future Research

The successful development of this synthesizer architecture opens up many areas for performance improvements and further research into new applications.

Improvements in the spurious response of the synthesizer can be achieved by implementing some form of adaptive spur cancellation scheme. This approach is viable since the spurs arising from incomplete noise shaping in the $\Sigma\Delta$ frequency discriminator are predictable and could be cancelled using DSP techniques.

Mobile digital radio applications demand small size and low power architectures, thus large scale integration in a BiCMOS process is a desirable approach. However, this introduces implementation issues that must be resolved before successful integrated circuits can be developed. The analog section of the architecture cannot be directly integrated without design changes since the noise requirements of the active circuits may not be met with most BiCMOS processes. One possible solution is to reduce the amount of active analog circuitry in the architecture. The analog integrator may be replaced by a passive RC filter which may reside off-chip depending on the desired time constant. This eliminates one OP-AMP at the expense of reduced noise suppression within the loop

bandwidth. Integrated voltage-controlled oscillators are the subject of current research and generally their performance is inferior to discrete oscillators due to their low-Q [29],[30]. Various D/A converter architectures that don't require precision laser trimming could be explored. Oversampled single-bit D/A converters may be a solution that can be readily integrated in a standard BiCMOS process.

The synthesizer used as a modulator is an area not explored in this thesis and open to further research. This synthesizer is well suited for digital modulation schemes (e.g. DECT, CT2 etc.) with modifications to the architecture. The specifications of digital modulation schemes generally have tight phase noise requirements and require large loop bandwidths. Achieving the phase noise performance usually requires a loop bandwidth that is less than that for modulation. However, modulation outside the loop bandwidth can be implemented by digitally pre-emphasizing the modulation signal to compensate for the PLL loop suppression.

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Appendix A

$\Sigma\Delta$ Frequency Discriminator Based Synthesizer Schematic

Appendix B

Field-Programmable Gate Array Schematic

Appendix C

$\Sigma\Delta$ Frequency Discriminator Schematic

END

3 1 - 0 5 - 9 5

FIN

The quantizer shown in Figure 5.5 is implemented with an analog comparator and a transparent ECL latch. The comparator compares the input level to the 0V reference level and its output swings to an ECL high or low depending on which is greater. Once the comparator has settled, its output is latched. Since the comparator has a very high gain, some hysteresis is necessary to prevent it from oscillating. The hysteresis has a detrimental effect on the overall discriminator operation since it prevents the comparator from responding linearly to the analog input voltage from the integrator. This causes small limit cycles (i.e. streams of zeros or ones) to occur at the quantizer output and degrades the quantization noise shaping properties of the discriminator.

5.2.1.5 Timing Control

The overall timing of the discriminator is crucial to its correct operation. In this implementation, the timing signals are generated by ECL programmable array logic (PAL) devices. This reduced the total number of discrete logic devices and provided the flexibility for architecture modifications. Figure 5.6 shows a typical timing diagram for the discriminator in locked condition with various points marked for reference.