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THE LIMITATIONS OF THE TRANSISTOR/
AS A HIGH-SPEED POWER SWITCH WITH
SPECIAL REFERENCE TO TUNED CLASS-D
AMPLIFIERS

by

Walter J. Chudobiak, B.Sc., M. Eng.

A thesis submitted to the Faculty of
Graduate Studies in partial fulfilment
of the requirements for the degree of
Doctor of Philosophy

Carleton University
Ottawa, Ontario
May, 1969

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ABSTRACT

This thesis considers two characteristics of large-area epitaxial and triple-diffused transistors which limit the efficiency and reliability of tuned Class-D power amplifiers:

- a) The thermal characteristics of a high-frequency saturating transistor switch.
- b) The static and dynamic collector-emitter saturation voltage characteristics.

Analogue simulations of devices having extended comb-like geometries along with thermographic examinations (temperature-sensitive phosphors) of actual devices are used to ascertain the thermal characteristics of large-area high-frequency switches. It is found that the emitter metallization resistance contributes to a non-uniform turn-off mechanism which may result in preferential heating of the region near the emitter contact.

The transport equations and charge-control concepts are applied in an analysis of a static conductivity-modulation mechanism occurring in the collector region of epitaxial and triple-diffused power transistors. This

results in an expression for collector-emitter saturation voltage as a function of terminal currents and device parameters. Also, an expression is derived which describes the current gain characteristics of saturated epitaxial and triple-diffused devices. The analysis is also used to illustrate the relationship between the emitter metallization resistance, collector charge storage, and the turn-off crowding mechanism experienced by high-frequency saturating transistor switches.

An analysis of a time-dependent collector conductivity modulation process is used to derive an expression which describes the repetition frequency dependence of the collector-emitter saturation voltage of an epitaxial (or triple-diffused) transistor switching a square wave of collector current. It is concluded that frequency-dependent edge-crowding mechanisms occur only at much higher frequencies than those considered in this study.

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LIST OF SYMBOLS

A	Effective collector area
A_{CB}	Collector-base junction area
C_1, C_2	Integration constants
D_n, D_p	Diffusion constants for electrons and holes in the collector region
f	Angular frequency
f_T	Transistor gain bandwidth product
E	Electric field strength
E_0	A constant parameter = 8000 volts/cm
E_{mB}	Maximum electric field strength at avalanche breakdown
h_{FE}	Grounded-emitter DC current gain
h_{FEO}	Grounded-emitter DC current gain for $V_{BC} = 0$
I_B	Base current amplitude
I_{BC}	Hole current flowing from base to collector
I_{BS}	Excess base current
I_C	Collector current
I_H	Emitter current level at which thermal resistance is measured
I_L	Current level at which base-emitter junction temperature is monitored.
J_B	Base current density
J_C	Collector current density
J_{Ca}	Collector current density at a point a.
J_{Cb}	Collector current density at a point b.
J_E	Emitter current density
J_n	Electron current density

LIST OF SYMBOLS (CONTINUED)

J_o	Reverse saturation current density
J_p	Hole current density
K	A constant which relates hole current in the high-resistivity collector region to the excess base current
k	Boltzmann's constant
L_e	Emitter stripe length
L_p	Hole diffusion length
M	A constant factor
N^+	Collector substrate impurity density
N	Net impurity density
N_d	Impurity density in the high-resistivity collector region
n,p	Injected carrier density in the collector region
n_i	Intrinsic carrier concentration
n_o, p_o	Equilibrium carrier densities in the collector region
P_{TON}	Average power dissipated by device during turn-on transitions
P_T	Rated collector power dissipation
P_{SAT}	Average power dissipated by device during ON time
P_{TOFF}	Average power dissipated by device during turn-off transition
P_1, P_2	Device power dissipation during thermal resistance measurement.
$P(O), P(W_c)$	Net minority carrier density in the collector region at x equals 0 and W_c .
Q_c	Total minority carrier charge stored in the collector

LIST OF SYMBOLS (CONTINUED)

q	Electron charge
q_a, q_b	Stored collector charge per unit length of emitter stripe at point a and point b.
R_B, R_{E1}	Discrete resistive elements in the composite-array transistor corresponding to base and emitter metallization resistance
R_{E2}	Emitter-ballasting resistance
S	Recombination velocity
T	Absolute temperature
T_1, T_2	Junction temperatures corresponding to device dissipation P_1 and P_2
V_B	The breakdown voltage of a one-sided pn junction with an impurity density N_d
V_{BC}	Terminal base-collector voltage
$V_{BC'}$	Potential drop across the base-collector junction
V_{BE}	Terminal base-emitter voltage
V_{CC}	Collector supply voltage
V_{CBO}	Collector-base breakdown voltage (emitter open)
V_{CE}	Collector-emitter voltage
V_{CEO}	Collector-emitter breakdown voltage (base open)
V_I	Potential drop across the region of the collector defined by $x_c < x < W_c$
V_P	Peak collector-emitter voltage amplitude during a turn-off transition
V_{SAT}	Collector-emitter saturation voltage
$\overline{V_{SAT}}$	Average collector-emitter saturation voltage during the ON time of a transistor switch
v	Velocity
v_m	Scatter-limited velocity

LIST OF SYMBOLS (CONTINUED)

W_b	Width of base region between boundaries of collector and emitter depletion layers
W_c	Width of lightly-doped collector region
W_e	Width of emitter diffusion stripe
W_1, W_2	Separation between base metallization stripes
x	Position in the collector region
x_c	The point removed from $x = 0$ at which $p = 0$.
x_{ca}, x_{cb}	x_c at the points a and b along the emitter stripe
x_{mb}	Depletion layer width for the avalanche breakdown voltage corresponding to the epitaxial layer resistivity
y	Spatial coordinate parallel with base and emitter stripes
z	Spatial coordinate normal to base and emitter stripes
α	Grounded-base current gain
β	Grounded-emitter DC current gain for $V_{BC} > 0$
γ	$\frac{J_{Cb}}{J_{Ca}}$
δ	$\frac{x_{ca}}{W_c}$
ϵ	Absolute permittivity
θ	Thermal resistance
μ_n, μ_p	Electron and hole mobilities
μ_{no}	Low-field electron mobility
ρ	Emitter metallization sheet resistance
ρ_B	Reciprocal of the average conductivity in the base region

LIST OF SYMBOLS (CONTINUED)

σ	A constant factor relating $V_{SAT}(t)$ and $V_{SAT}(0)$
τ	Minority carrier lifetime
τ_c	Effective minority carrier lifetime in the lightly-doped collector region
ψ	$\frac{qC_1\rho_B W_e}{4kT}$

CHAPTER 1

INTRODUCTION

1.1 Introduction

The theory and application of Class-D circuits have received considerable attention in the literature in recent years^{(1-6)*}. However, most of this attention has been directed towards the circuit aspects of the technique, while only limited attention has been given to the analysis of the semiconductor device characteristics which ultimately limit circuit efficiency and reliability^(4,6). These characteristics are the subject of this thesis. The characteristics concerned are introduced later in this chapter, following a brief review of the Class-D principle as related to tuned amplifiers.

1.2 A Review of the Class-D Principle

Baxandall⁽¹⁾ defined a Class-D circuit to be "one in which the angle of current flow in each active device is 180° , but in which substantially no voltage exists across the active device while it is conducting".

* For all such references, see the Bibliography.

There are two basic amplifier configurations to which this definition may be applied. In the first of these, the voltage-switching amplifier, a square wave of voltage generated by a circuit with an extremely low output impedance is fed to a series resonant circuit which recovers the sinusoid at the switching frequency⁽³⁾. Such a circuit is shown in Fig. 1.* With the polarities indicated, the transistors Q_1 and Q_2 are alternately saturated and cutoff, producing a square wave at the input to the series resonant circuit. The resultant circuit waveforms for a low switching frequency** are given in Fig. 1. Current, voltage, power, and efficiency relationships at a low switching frequency are given in Table I where it can be seen that collector efficiency approaches 100% if the collector-emitter saturation voltage is much less than the collector supply voltage.

In the other circuit configuration, the current-switching circuit, a square wave of current (instead of a voltage square wave) is fed to the output filter⁽³⁾. Such a circuit is shown in Fig. 2. A constant current supplied by the large inductor L_2 is fed to the parallel resonant circuit; the square wave of current results

* All figures appear after Appendix H.

** Frequencies at which power dissipated during switching transitions is small compared to power dissipated during saturation.

TABLE 1
Relationships for Tuned Class-D Power Amplifiers

	Voltage-Switch	Current-Switch
Output Voltage (RMS)	$\frac{\sqrt{2}}{\pi} (V_{CC} - 2V_{SAT})$	$\frac{\pi}{\sqrt{2}} (V_{CC} - V_{SAT})$
Output Power	$\frac{2}{\pi^2 R_L} (V_{CC} - 2V_{SAT})^2$	$\frac{\pi^2}{2R_L} (V_{CC} - V_{SAT})^2$
Input Current (DC)	$\frac{2}{\pi^2 R_L} (V_{CC} - 2V_{SAT})$	$\frac{\pi^2}{2R_L} (V_{CC} - V_{SAT})$
Input Power (DC)	$\frac{2V_{CC}}{\pi^2 R_L} (V_{CC} - 2V_{SAT})$	$\frac{\pi^2 V_{CC}}{2R_L} (V_{CC} - V_{SAT})$
Collector Efficiency	$\frac{V_{CC} - 2V_{SAT}}{V_{CC}}$	$\frac{V_{CC} - V_{SAT}}{V_{CC}}$

Note that with a given transistor type, design values of V_{CC} and R_L for the current-switch will differ from those used for the voltage-switch. Also note that the following power losses are ignored:

- 1) power loss during transistor cut-off
- 2) power loss due to nonideal tuning
- 3) power loss during switch transitions.

from the alternate saturation and cutoff of transistors Q_1 and Q_2 . The resultant low switching-frequency waveforms are shown in Fig. 2, while the current, voltage, power and efficiency relationships are also given in Table 1. Again it can be seen that collector efficiency approaches 100% if collector-emitter saturation voltage is much less than the collector supply voltage.

At high switching frequencies, the efficiency relationships given in Table 1 are not valid. Collector efficiency (and available output signal power) decreases steadily as switching frequency is increased because of a number of factors:

- 1) At high switching frequencies, the power dissipated by the active devices during switching transitions is not small compared with the amount of power dissipated when the devices are in saturation. Although the peak power dissipation during the switching transition may be constant over a wide range of switching frequencies, the average dissipation increases with frequency because of the increase in duty cycle.
- 2) The amount of power dissipation during the saturation time of the active devices also increases with switching frequency since the

collector-emitter saturation voltage is dependent on the repetition frequency^(7,8).

That is, the transient response of a transistor is such that the average saturation voltage increases as the signal period (or ON time) is decreased.

Class-D amplifier waveforms which exhibit pronounced device power dissipation during the switching transitions and the time dependence of collector-emitter saturation voltage are given in Figs. 3 and 4. The waveforms in Fig. 3 (voltage switch) illustrate an effect particularly noticeable at high switching frequencies; a spike of collector current which flows during the switching transitions as a consequence of device storage time being greater than device turn-on delay time^(4,6). With such current spikes, the power dissipation during the switching transitions is very high and, in fact, in many high-frequency voltage-switching applications, the larger portion of the net device dissipation occurs during the switching transitions.

It is evident that the switching transition loss in Fig. 4 (current switch) is somewhat lower because of the absence of spikes at the "base" of the sinusoidal waveform. Spikes of collector-emitter voltage can occur in an accurately tuned current-switching circuit, but only

if the transistor turn-off times are less than the turn-on times or if appreciable collector lead inductance exists^(4,6). In practice, however, the spikes can usually be avoided by providing sufficient base drive current to insure turn-off times which are greater than the turn-on times and by ^{many other} circuit layout techniques. The discontinuities in the rising and falling edges of the current waveforms in Fig. 4, are a result of the device turn-off times being much greater than the turn-on delay times. ①

Normally, the greater fraction of the device power dissipation in a current-switching circuit occurs when the device is in saturation. Since saturation voltage decays in the manner shown in Fig. 4, the average value of saturation voltage, and therefore device dissipation, increases with switching frequency. The average saturation voltage in the voltage-switching circuit also increases with frequency, but if a sinusoidal base drive current is used, the average saturation voltage is less than that in the current switching circuit since the peak collector current is not maintained during the entire conduction cycle. It should be mentioned that in this particular example (Fig. 3), the amplifier was driven with a square wave of base current, which accounts for the high saturation voltage⁽⁶⁾. Had a sinusoidal base drive been used, a much lower saturation voltage could have been realized.

1.3 Device Characteristics Studied in this Thesis

With reference to the factors discussed in the preceeding section, one may define several fundamental device characteristics which limit Class-D amplifier efficiency and reliability at high switching frequencies. The characteristics may be grouped under two headings:

A. Thermal Characteristics of the High-Speed Saturating Switch

The thermal behavior of a high-speed transistor switch dissipating power in the fashion shown in Figs. 3 and 4 (periodically applied power pulses with both pulse width and repetition period much less than the device thermal time constant) must be understood in order to assign a power rating to the device when used in Class-D applications.

B. Collector-Emitter Saturation Voltage Characteristics of the High-Speed Saturating Switch

The dependence of collector-emitter saturation voltage on collector current, base current, switching frequency, device structure, and device parameters must be established, in order to be able to select devices and to be able to tailor device drive waveforms so as to obtain (and indeed predict), the highest possible collector efficiency and output signal power in Class-D amplifier applications.

The device limitations considered in this thesis were originally encountered by the author while developing Class-D amplifiers capable of producing output signal powers of up to one kilowatt in the frequency range of 100 kHz to several Megahertz^(5,6). Silicon NPN epitaxial* and triple-diffused large-area transistors (collector-base junction areas typically greater than 0.05 cm^2) are commonly used in such applications, so particular emphasis is placed on devices of this nature in this thesis. Also, the device characteristics in a current-switching environment are stressed since this is the preferred circuit (because of its greater reliability and available output signal power) and is the arrangement most commonly used in high-power applications^(5,6).

The device models are required in a form which may be conveniently utilized by the circuit designer. Because of this, emphasis is placed on obtaining analytical or approximate analytic solutions for the differential equations used in the analysis. That is, numerical solutions of the differential equations are not attempted since it is felt that analytical solutions are more convenient for design purposes in that a digital computer is not required, and also, such results can be more readily incorporated into other related analyses.

* In this thesis, the term epitaxial refers to devices having a thin epitaxial layer in the collector, the emitter and base being diffused.

Moreover, applying this approach (which consists of placing emphasis on the simplest adequate representation of physical effects) to a complex physical problem enables one to retain some understanding of the mechanism being studied. Computer simulations of device operation are less attractive in this respect. Also, in the study of semiconductor devices, it is often true that discrepancies between the performance of a model and the actual device are not due to a basic error in the model itself, but rather, can be related to poorly defined model parameters. Unless a better definition of model parameters can be obtained, little is gained through the use of very accurate numerical techniques (i.e., computer simulation techniques) to solve the equations. *good point*

In developing the analysis and models in this thesis, attempts were made to relate the model parameters to familiar device parameters. For cases where this was not possible, techniques for determining the parameters are described.

1.4 Discussion of Existing Analyses

A. Thermal Effects

Various authors have described the thermal response of a transistor to periodically applied power pulses (see for example⁽⁹⁾). Also, device manufacturers

commonly specify safe operating areas for their transistors as a function of the time the device may operate with a particular collector current and voltage without incurring the risk of device failure. Both of these sources indicate that if the ON time of the power pulse and the repetition period are both very much less than the device thermal time constant, the peak junction temperature developed during the power pulse can be calculated by averaging the device power dissipation and applying a static analysis. However, in spite of the fact that the dissipation times (switching transitions) and repetition period of a high-frequency Class-D circuit are both generally much less than the transistor thermal device constant*, applying this technique to determine junction temperatures yields unreliable results; devices commonly fail even though the amount of average power dissipated by the device is less than the static rating defined by the manufacturer. It would appear that the fault with the existing analyses lies with the assumption that the same thermal equivalent circuit is valid over a very wide range of frequencies without regard to device geometry, base and collector waveforms, and other factors. Undoubtedly, for very-high-frequency switching of large-area devices, a redefinition of device thermal resistance is necessary.

* The device thermal time constant may be of the order of 1 msec., while the repetition period and transition times are commonly of the order of 1 μ sec. and 0.1 μ sec. respectively.

B. Collector-Emitter Saturation Voltage: Static Case

The static common-emitter saturation voltage of a transistor is commonly described in textbooks as being equal to the sum of the potential drops across the two forward-biased junctions plus additional, small stray terms. From an examination of the $V_{CE}-I_C$ characteristic curves of an alloy transistor (Fig. 5.a), it is apparent that such a definition is valid for alloy transistors. However, this description is not appropriate for epitaxial or triple-diffused large-area transistors. Typical $V_{CE}-I_C$ characteristic curves for epitaxial and triple-diffused transistors (Figs. 5.b and 5.c) normally exhibit a "two-stage" saturation curve which can easily extend to several volts. It would appear that the "stray terms" are dominating the saturation characteristics of the device.

Recently, a number of authors have acknowledged that conductivity modulation phenomena in the collector region govern the static saturation characteristics of transistors having lightly-doped collectors^(10,11,12). Qualitative discussions of these three papers are given in the paragraphs which follow.*

* The following additional paper was published after the completion of this thesis: L.E. Clark, "Characteristics of Two-region Saturation Phenomena", IEEE Trans. Electron Devices, Vol. ED-16, No. 1, pp. 113-116, January, 1969. Clark gives a solution for the minority carrier distribution in the collector region which is identical to that given by Beale et al⁽¹¹⁾. Also, he considered the effect of the base doping density on the two-stage saturation curve but failed to describe V_{SAT} as a function of collector current, base current, and device parameters.

Hahn⁽¹⁰⁾ was the first to report on this matter. In qualitative terms he related the shape of the saturation curve to the injection of minority carriers into the high-resistivity collector region. Also, he developed what he termed a semi-quantitative model which described the minority carrier distribution and field distribution in the high-resistivity collector region. However, he failed to refine his analysis to the point where an expression for collector-emitter saturation voltage in terms of collector current, base current and device parameters would result.

Beale and Slatter⁽¹¹⁾ have analyzed the minority carrier distribution in the lightly-doped collector region of a transistor operating in saturation. Their analysis is well suited for the calculation of total stored charge in the collector as a function of collector current level (for a defined collector-emitter saturation voltage) but it has a serious limitation in that the potential drop across the high-resistivity collector layer appears as a variable in the expression for minority carrier distribution. Because of this, and also because the minority carrier current in the collector was defined to be zero, their analysis cannot be extended to give collector-emitter saturation voltage as a function of collector current, base current, and relevant device parameters.

Larin's treatment of the topic in his recent book⁽¹²⁾ represents the most significant contribution to the literature (portions of the analysis presented in this thesis closely resemble Larin's but were, in fact, developed quite independently). There are, however, a number of shortcomings inherent in Larin's treatment. First, his analysis is not firmly founded upon fundamental semiconductor equations (such as the transport equations) and so is difficult to follow, at least in the initial steps. Second, his analysis was for a transistor having a wide, lightly-doped collector layer connected directly to an ohmic contact instead of to a heavily-doped substrate. Finally, he did not produce an expression which defined collector-emitter saturation voltage in terms of collector current, base current, and device parameters.

B. Collector-Emitter Saturation Voltage: Dynamic Case

A number of authors have suggested that the dependence of saturation voltage on the repetition frequency could be related to a crowding mechanism which effectively reduces the conducting area of the transistors^(7,8). Recently, Krishna et al⁽¹³⁾ presented an analysis of VHF transistor characteristics which demonstrated that saturation voltage increases because of

the inverse relationship between saturation resistance and conducting area. However, neither Krishna et al nor the other authors considered the conductivity modulation of the collector body resistance. But since the static saturation characteristics of epitaxial and triple-diffused structures are, in fact, dominated by this affect, it would appear that any treatment of the dependence of V_{SAT} on the repetition frequency should also include an analysis of time-dependent conductivity-modulation effects.

1.5 Approach Adopted in this Thesis

A. Thermal Characteristics of the High-Speed Saturating Switch

It was suggested in the previous section that the power rating of a high-frequency transistor switch should not be determined using a value for device thermal resistance given by one of the common DC measurement techniques⁽¹⁴⁾. In Chapter 2 of this thesis it is demonstrated that a crowding mechanism peculiar to the high-frequency transistor switch effectively reduces the area of the collector-base junction and so produces a non-uniform temperature distribution over the surface of the device. This effect can be interpreted as an increase in device thermal resistance. To establish the thermal characteristics of the high-frequency switch, one can

either measure the device thermal resistance at the switching frequency, or alternatively, describe the crowding mechanism and then use the DC thermal resistance to determine the temperature distribution over the surface of the device. The second of these procedures is developed in Chapter 2.

Also in Chapter 2, the relationship between the crowding mechanism and contact metallization resistance and contact arrangement for a transistor with a comb-like structure is demonstrated using an array of VHF small-area transistors interconnected to simulate a large-area device. A thermographic technique involving temperature-sensitive phosphors is used to observe temperature profile on the surface of transistor chips and to study the dependence of hot spot formation on device collector waveforms and base drive waveforms.

B. Collector-Emitter Saturation Voltage

The collector-emitter saturation voltage of epitaxial and triple-diffused transistors is related to the conductivity modulation of the high-resistivity collector layers inherent in such structures. Using the transport equations and charge-control concepts, the static collector-emitter saturation voltage is described

in Chapter 3, in terms of collector current, base current, and a number of device parameters. The analysis is extended to show that at low collector-emitter voltages, the falloff of current gain (h_{FE}) at high collector currents is largely due to conductivity modulation phenomena in the high-resistivity collector layer. Also, the analysis is used to demonstrate that the crowding mechanism discussed in Chapter 2 can ultimately be related to the conductivity modulation of the collector.

The static analysis of conductivity modulation is modified in Chapter 4 using a charge-control approach to give the time dependence of the collector-emitter saturation voltage for a transistor switching a square wave of collector current when driven by a square wave of base current. It is shown that for the frequencies considered in this thesis, the frequency dependence of collector-emitter saturation voltage can be related to a time-dependent conductivity modulation process in the collector region. Further, it is suggested that edge-crowding effects, the explanation normally given for the frequency dependence of collector-emitter saturation voltage, become significant only at frequencies greater than those considered in this study.

1.6 Statement of Original Work

Unless otherwise noted, all work reported in this thesis is original with the author.

CHAPTER 2

THERMAL CHARACTERISTICS

2.1 Introduction

Current crowding in transistors may result in the formation of hot spots and subsequent device failure even though the average device dissipation may be less than the rating assigned by the manufacturer. A current-crowding mechanism peculiar to the high-frequency saturating switch is described in qualitative terms in this chapter and it is shown that the mechanism can effectively reduce the power rating of the transistor.

A description is given of a thermographic technique which may be used to observe junction temperature distributions and also, an elementary thermal model is developed which may be used to predict the peak junction temperature in a high-frequency transistor switch. Particular attention is given to devices having a comb-like geometry since this is the structure most commonly employed in modern large-area transistors.

2.2 A Current-Crowding Mechanism

Large-area switching transistors which have failed catastrophically while operating in high-frequency Class-D

amplifiers ^{usually (always)} often exhibit a burned or damaged spot adjacent to the emitter contact. An example of such a device is shown in Fig. 6. Recently, this author⁽¹⁵⁾ described a crowding mechanism which could account for both the location of the damaged area and for the fact that device failure may occur for an average dissipation less than P_T . It was suggested that the crowding mechanism was the result of a successive reduction in the conducting area of the transistor occurring during the switching transitions from saturation to cutoff (see Fig. 7). With this reduction in conducting area, the region last extracted from the saturated state dissipates the bulk of the power loss incurred by the device during the turn-off transitions and is therefore preferentially heated. Very high junction temperatures may result even though the average device dissipation may be much less than P_T .

There are a number of basic factors which could contribute to the nonuniform turn-off mechanism portrayed in Fig. 7:

- a) The rate at which charge is removed during the turn-off transitions may not be uniform in all regions of the device.
- b) All regions of the device may not be saturated to the same degree during the ON time of the switch.

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- a) The rate at which charge is removed during the turn-off transitions may not be uniform in all regions of the device.
- b) All regions of the device may not be saturated to the same degree during the ON time of the switch.

It is subsequently shown in this thesis that the influence of the first factor is small and may be neglected for the purposes of this study. A discussion of the relationship between the crowding mechanism and the second factor is given in the paragraphs which follow.

For the purposes of this discussion, it is instructive to represent a saturated, large-area epitaxial (or triple-diffused) switching transistor by the two-element model shown in Fig. 8. Transistor Q_A corresponds to the region of the large-area device near the base contact while Q_B represents the region near the emitter contact. R_E and R_B correspond to the emitter and base metallization resistances.

Cave and Barnes⁽¹⁶⁾ have shown that the effect of the emitter metallization resistance is to produce a collector current density distribution which exhibits a minimum in the vicinity of the base contact and which increases along the emitter stripes to a maximum near the emitter contact.* Therefore, in the two-element model shown in Fig. 8, the collector current for element Q_B will be somewhat larger than that for Q_A .

* See Appendix A for an outline of the analysis given by Cave and Barnes.

DC potential probing along the base stripes of saturated transistors has shown that the potential drop along the length of a base stripe is normally very much less than the terminal collector-base voltage. Therefore, the terminal collector-base voltages for the two elements Q_A and Q_B are nearly equal. Because of this, the minority carrier conductivity modulation in the collector epitaxial layer of element Q_B will be more extensive than that for Q_A since Q_B is conducting a larger collector current.* Therefore, Q_B will have a longer turn-off time than Q_A since the storage time of an epitaxial device is normally defined by the time required to remove the injected minority carriers from the epitaxial collector layer⁽¹⁷⁾. The turn-off transition loci for the two elements Q_A and Q_B in the V_{CE} - I_C plane may resemble that shown in Fig. 9. It is evident from this illustration why the element Q_B (i.e., the region near the emitter contact) will be preferentially heated, particularly if an inductive load is present.

It should be mentioned that the above discussion does not apply to transistors having a heavily-doped collector since collector conductivity modulation effects

* The reader is referred to Chapter 3 for a detailed analysis of the relationship between conductivity modulation phenomena and the saturation characteristics of epitaxial and triple-diffused transistors.

are negligible in such devices. In fact, in the case of an alloy transistor, the area adjacent to the base contact is the more heavily saturated since the collector current density is least in that region. Therefore, one would expect the peak junction temperature in a high-frequency saturating alloy switch to occur in the region adjacent to the base contact (rather than near the emitter contact).

2.3 An Analogue of a Large-Area Transistor

Experimental confirmation of the effects of metallization resistance and contact arrangement on current crowding in large-area transistor switches may be obtained using the composite-array transistor shown in Fig. 10. The array consists of low-power epitaxial VHF transistors (2N2222) interconnected by the discrete resistive elements R_B , R_{E1} , and R_{E2} . These elements represent base stripe metallization resistance, emitter stripe metallization resistance, and emitter ballasting resistance (overlay structure), respectively. The individual transistors have closely matched switching characteristics (see Appendix B), and also, are thermally isolated from each other; thus, any variance between device temperatures may be attributed to the location in the array rather than to device nonuniformities.

A test arrangement of the form shown in Fig. 11 may be used to ascertain the thermal characteristics of the composite device. The drive signal amplitudes, V_1 and V_2 , are such that the device-under-test and the crowbar switch are alternately saturated and cutoff. Varying the delay time t_D enables one to determine the effect of power dissipation during the turn-off transition on the thermal profile. For example, with $t_D = 0$, the device-under-test dissipates power only while in the saturated state while for $t_D > 0$, the device dissipates power both while in saturation and also during the turn-off transition.

Measured temperatures profiles (case temperatures) of the composite device for various combinations of R_B , R_{E1} , R_{E2} , and contact arrangement are plotted in Fig. 12. The effect of power dissipation during the turn-off transition on the thermal profile of a large-area device being switched at a high frequency is evident from Fig. 12.a ($R_B > 0$, $R_{E1} > 0$, $R_{E2} = 0$). For $t_D > 0$ ($V_P = 30$ volts, $V_{CE0} = 45$ volts), there was pronounced heating of the area adjacent to the emitter contact, much more so than for $t_D = 0$. This is in agreement with the crowding mechanism described in the previous section.

The hot spot was shifted to the centre of the device and peak temperature reduced by making emitter

and base contacts on both ends of the composite device (Fig. 12.b, solid curve). A further improvement in temperature profile was realized by eliminating emitter metallization resistance from the device of Fig. 12.a (Fig. 12.b, dotted curve). This curve is of particular interest since it serves to demonstrate that the crowding mechanism is, in fact, a consequence of the emitter metallization resistance.

To simulate the characteristics of an overlay transistor with emitter ballasting, the circuit of Fig. 12.a was modified by the addition of one-ohm emitter resistances (R_{E2}). The emitter-ballasting resistors should in effect swamp the emitter metallization resistance and thereby ensure a uniform degree of saturation in all regions of the device. The uniform temperature profile given in Fig. 12.b (dashed curve) suggests that this does, in fact, happen. This clearly demonstrates the advantages of such structures in high-frequency saturating-switch applications. Large-area overlay power transistors ($A_{CB} > 0.05 \text{ cm}^2$) with emitter ballasting have recently become commercially available. However, at the time of writing, this author was unable to obtain samples for evaluation.

2.4 Thermal Profiles in Large-Area Transistor Switches

2.4.1 Thermographic Techniques

Schafft⁽¹⁸⁾ summarized the techniques which may be used to obtain thermal profiles in semiconductor de-

vices. Two of these methods are particularly well suited to the present application since both give rapid reproducible descriptions of temperature and are useful over a wide temperature range.* The most popular of the two methods is the scanning infrared plotter which is able to give quantitative, two-dimensional temperature determinations. However, scanning infrared plotters are extremely expensive and since one was not available for this study, the second approach was adopted. This method, temperature-sensitive phosphors, also gives two-dimensional temperature descriptions and has the added advantage of being very inexpensive and easy to apply^(19,20,21). Although the material is primarily intended for qualitative analysis, it is possible to apply a calibration procedure.

Temperature-sensitive phosphors (zinc-cadmium sulfide phosphors) fluoresce with a brilliance which is

* A third technique mentioned by Schafft is not well suited to this particular application since it is primarily intended for applications requiring very sensitive temperature resolution over a limited temperature range. However, for the sake of completeness, a brief description of the technique is given at this point. This method utilizes a material (cholesteric liquid crystals - "Liquid Crystals") which is applied in the form of a thin film to the device surface and which undergoes a series of color changes as the temperature is varied over specific short temperature ranges. Presently, material is commercially available which is useful from 0°C to 100°C, with a range of $\pm 1^\circ\text{C}$ to $\pm 7\frac{1}{2}^\circ\text{C}$ about any particular temperature in this interval.

inversely related to temperature when stimulated with near-ultraviolet radiation. Four different compositions are commercially available^{*}, each of which is temperature sensitive over a range of about 100°C. Using these four materials, it is possible to monitor temperatures in the range between 25°C and 400°C. However, the fluorescence of one of the phosphors (Radelin No. 3251) is temperature sensitive in the range 50°C to 150°C when stimulated with a high-power ultra-violet source^{**} and since this is the temperature range of interest for nondestructive device examinations, this one material alone is usually sufficient.

The phosphor is mixed with a light silicone oil (a material which does not fluoresce) and a thin coat is applied directly to the surface of the semiconductor die using a small brush (the manufacturer recommends a thickness of about one mil). To insure a uniform background color, it is often necessary to coat the device surface with a dark paint prior to the application of the oil-phosphor mixture. Where necessary, black water-based paints were used in this study.

* Manufactured by U.S. Radium Corp.

** A 100 watt, high-pressure mercury vapor lamp fitted with a 3660Å filter and placed at a distance of 10" was used in this study.

The temperature distribution which results when a large-area device is dissipating power can usually be viewed directly with the unaided eye, but a microscope-camera arrangement is convenient if a permanent record is desired. In such cases, a yellow filter (K2 filter) must be used to exclude reflected ultraviolet light from the camera.

The intensity of the luminescence encountered in this study was such that exposure times of one second or less were sufficient with 3000 or 10,000 ASA speed film.

Photographic film also provides a technique for quantitative work. The film may be calibrated by photographing the phosphor-coated surface of a calibrating mechanism such as a metal bar, the ends of which are maintained at known temperatures. Care must be taken to coat the calibrating mechanism with a phosphor thickness the same as that used for the work and to stimulate it with the same ultraviolet intensity. This calibration procedure requires photographic film having a wide tonal range or latitude (that is, sensitive over a wide range of brightness values). However, the microscope-camera equipment conveniently available to the author utilized Polaroid camera backs, and Polaroid film which exhibits

this property is not available. For this reason, it was not possible to provide a photograph of a calibrated mechanism which could be used by the reader to determine temperatures from the thermal profiles given in the thesis. Where required, the fluorescence brilliance of the semiconductor devices was compared visually with a calibrated bar and the temperature noted.

According to the manufacturer, temperature resolution of the order of 1°C (approximately 10% change of brightness per $^{\circ}\text{C}$) is possible with the phosphor. In the present study however, the maximum resolution appeared to be about 5°C (probably because of the photographic technique) and since this was sufficient, no attempt was made to attain the resolution defined by the supplier.

The only indication of the spatial resolution capabilities of the technique is given in Reference 19 where it is claimed that observations can be made on items of microscopic size under as high as 100 x magnification and also, by the manufacturer who specifies an average particle size of 9 microns. However, the resolution appeared to be adequate for the devices considered in this thesis and so no attempt was made to ascertain the ultimate capabilities of the technique.

2.4.2a Observed Temperature Distributions - Static Case

Before presenting a description of the temperature distributions in high-speed saturating switches, it is useful for purposes of comparison to briefly consider the temperature profiles exhibited by devices which are biased at some particular DC operating point.

A hot spot formation mechanism (static conditions) known as the Theory of Lateral Thermal Instability has been described extensively in qualitative terms in the literature^(22,23,24). This theory refers to a process whereby current builds up in one region of the transistor and decreases in the remaining area, resulting in a region of enhanced current density and temperature. The basic mechanism leading to the formation of a hot spot operates as follows (the discussion does not include avalanche effects). Consider a device with an initial slight nonuniformity of heat generation (or dissipation) in a small area of the device. The slightly higher local temperature in this area results in an increase in local base current density due to the negative temperature coefficient of the intrinsic base-emitter voltage. This in turn results in an increased local collector current density and therefore, additional heating of the area. The dependence of h_{FE} on collector current determines another contribution of increased collector current density

with increasing temperature since if the current gain increases with collector current, an additional power input arises. Also, the positive temperature coefficient of h_{FE} results in further enhanced collector current densities and therefore, additional dissipation with temperature. Because of the action of these three factors, the temperature of the incremental area rises while the temperature of the remaining area may decrease, particularly if the net collector current supplied to the device is maintained constant. The process continues and temperature and current build up locally until limited by the falloff of h_{FE} at high current densities and by the resistive drops in the various layers of the transistor (or by a change in state of the material, such as melting).

For a given device dissipation, the theory suggests that the likelihood of the formation of a hot spot is progressively reduced as the collector-supply current is increased since h_{FE} falls off at the higher collector currents and further, the resistive drops which have a stabilizing effect, increase with collector current. Also, it is possible to deduce from the theory which transistor structures are most susceptible to the formation of hot spots. For example, alloy transistors and

high-resistivity wide-base diffused transistors have a built-in safety factor in that at high current densities, conductivity modulation of the base causes a severe h_{FE} falloff preventing dangerous increases of local collector current density. Transistors with wide high-resistivity collector layers (such as most triple-diffused devices) also have a built-in safety factor by virtue of the resultant resistive drops. On the other hand, narrow-base epitaxial transistors are very susceptible to hot spot formation since these devices do not necessarily exhibit a rapid falloff of h_{FE} at high collector current densities and also, have a relatively low series collector resistance. However, the overlay epitaxial structure with emitter ballasting (the addition of emitter resistance in series with incremental areas) overcomes these limitations and is, in fact, the modern high-frequency transistor structure most immune to the formation of hot spots.

The preceding development assumed a slightly higher initial local temperature in some region of the device. For devices with a comb-like structure, the emitter metallization resistance is a factor which can contribute to the required initial nonuniform temperature distribution. Cave and Barnes⁽¹⁶⁾ have shown that

the effect of emitter metallization resistance is to produce a nonuniform collector current density distribution, density being maximum near the emitter contact at a point corresponding to the end of the base metallization stripe. One would therefore expect the peak device temperature to be observed in the region between the center line of the die and the tips of the base metallization stripes since collector current density (and hence power density) falls off rapidly beyond the tips of the base stripes. This is confirmed by the photographs in Fig. 13 of a large-area device dissipating 54 watts (DC) with a case temperature of 20°C (2N3265 - 125 watts, 90 volts, 25 Amp).^{*} Fig. 13.a depicts the brilliant fluorescence of the device at room temperature (no power dissipation) while Figs. 13.b, 13.c, and 13.d illustrate the thermal profiles in the device with collector currents and collector-emitter voltages of 18A-3V, 9A-6V, and 4.5A-12V respectively. It is apparent from the extinguishing of the fluorescence in the photographs that the susceptibility of the device to the formation of hot spots is enhanced as collector-emitter voltage is increased and collector current decreased (the darkest areas of the fluorescence indicate

* The parameters of the devices considered in this thesis are tabulated in Appendix C.

junction temperatures of approximately 60°C , 65°C and 70°C).^{*} No attempt was made to obtain photographs at still higher collector-emitter voltages since this entailed the risk of device failure (devices in short supply) and in any case, the results presented do indicate a trend and so confirm the Theory of Lateral Thermal Instability.

Further confirmation of the Theory of Lateral Thermal Instability was obtained by measuring the device thermal resistance using a technique described in Appendix D. The measurements were made over a range of operating conditions, but with device dissipation maintained relatively constant. The results, which appear in Fig. 13.e, confirm the theory to the extent that the degree of crowding is enhanced as the collector-emitter voltage is increased.

2.4.2b Observed Temperature Distributions and Qualitative Discussions - Dynamic Case

In this section, the phosphor is used in conjunction with the test circuit of Fig. 11 to determine the thermal characteristics of large-area epitaxial transis-

* It should be mentioned that the fluorescence of this particular phosphor becomes temperature sensitive only at temperatures greater than about 50°C . Because of this, the brilliance of the fluorescence in Fig. 13.a does not differ radically from that in the other photographs even though temperature differences of 40°C are involved.

tors operating as high-frequency saturating switches. Thermal profiles are given for three epitaxial transistors (2N3265, 2N3445, 2N3879) and it is shown that these devices represent three different degrees of crowding.

The dynamic thermal characteristics of triple-diffused transistors were not considered in this study since when switching near-rated currents, the saturation dissipation of a triple-diffused device is often much greater than the transition dissipation and so defines the thermal profile. Attempts to reduce the saturation loss by increasing the base drive* results in turn-off times which may be comparable to the switching period. The long turn-off time (both storage and rise time) normally precludes the use of triple-diffused device as high-speed, high-current switches⁽⁶⁾.

The fluorescence for a 2N3265 transistor dissipating power only while in saturation ($\overline{V_{SAT}} = 3.5$ volts, $I_C = 18$ Amp, $t_D = 0$) while being switch at frequency of 250 kHz is given in Fig. 14.a where it is evident that a fairly uniform temperature profile exists. Increasing the delay time t_D to give a peak collector emitter volt-

* The relationship between base drive level and saturation voltage is considered in Chapters 3 and 4.

age of 45 volts ($\overline{V}_{SAT} = 3.5$ volts, $I_C = 18$ Amp, $P_{SAT} = 25.2$ watts, $P_{TOFF} = 21.6$ watts) resulted in a slight dimming of the fluorescence, particularly in the region near the emitter contact (Fig. 14.b). The variation of the brilliance of the fluorescence over the surface of the device represents a temperature variation of about 20°C , with the slightly darker area near the emitter contact being the hottest (approximately 85°C). This is in agreement with the crowding theory advanced in Section 2.2. Again setting t_D equal to zero ($P_{TOFF} = 0$, $I_C = 18$ Amp) and increasing $\overline{V}_{SAT}$ to provide a net dissipation of 54 watts resulted in the thermal profile given in Fig. 14.c. Comparing Figs. 14.b and 14.c it is seen that the degree of crowding in the latter is less pronounced and is in fact similar to the static crowding experienced by the device when dissipating an equal amount of power at the same collector emitter voltage (Fig. 13.b). Increasing t_D to give a peak collector emitter voltage of 90 volts and decreasing I_C to nine amperes while maintaining a net power dissipation of 47 watts resulted in a thermal profile similar to that obtained for the 18 ampere, 45 volt example (Fig. 14.b). This suggests that the crowding effect of power dissipation during the turn-off transition is primarily power-dependent rather than voltage-dependent. It will be recalled that a device

biased at a DC operating point is susceptible to a hot spot formation mechanism which is largely voltage-dependent (see Section 2.4.2a).

We now consider the effect of increasing the switching frequency from 250 kHz to 500 kHz. With $I_C = 18$ amperes, $V_P = 45$ volts, and $P_{SAT} = P_{TOFF} = 32.4$ watts, a thermal profile resulted which indicated pronounced current crowding (Fig. 15.a). The quenching of the fluorescence in the region near the emitter contact represents a peak temperature of approximately 115°C , which is approximately 60°C higher than that near the base contact. It is instructive to compare this example with that of Fig. 14.b (250 kHz, $P_{SAT} = 25.2$ watts, $P_{TOFF} = 21.6$ watts) in which a peak temperature of 85°C and a minimum temperature of approximately 50°C was indicated. The comparison confirms that the effect of an increased switching rate is to enhance the average power density in the region near the emitter contact, the density in the region of the base contact remaining relatively unchanged, provided saturation voltage is maintained constant.

Changing the delay time t_D to increase the peak collector-emitter voltage from 45 volts to 55 volts had the effect of increasing the dissipation P_{TOFF} by about

7 watts and resulted in the impressive thermal profile shown in Fig. 15.b (peak temperature of approximately 135°C). Increasing the peak collector-emitter voltage still further to 90 volts (V_{CEO} specified by the manufacturer) and reducing collector current to 9 amperes resulted in the pronounced crowding shown in Fig. 15.c. One will recall that a similar combination of peak collector-emitter voltage and current at the lower switching frequency of 250 kHz produced a degree of crowding similar to that observed at lower collector-emitter voltages. It is suggested that avalanche effects are contributing to the crowding in the present example. A brief discussion of the relationships between avalanche effects, current densities, and crowding mechanisms is given in Section 2.4.3.

The 2N3445 (7.5 Amp, 60 volt, 115 watt) is a transistor which is much less susceptible to the crowding mechanism than is the 2N3265 transistor. Comparing geometries (Figs. 6 and 16.a), it is seen that the 2N3445 transistor has much shorter emitter stripes, partly because the device has a lower current rating and hence, a smaller area, but mainly because the emitter contact is placed along the centre line of the device instead along one side of the die. This has the effect of producing a

much more uniform degree of saturation over the extent of the emitter area of the device and hence, a more uniform turn-off process. A thermal profile is shown in Fig. 16.b for a 2N3445 transistor switching a collector current of 10 amperes at a frequency of 500 kHz with a peak collector-emitter voltage of 100 volts ($\overline{V_{SAT}} = 8$ volts). The photograph, which was made with high-contrast film (Polaroid 410), indicates a peak temperature of about 100°C which is only 20°C higher than the minimum junction temperature. It will be recalled that under similar conditions, the 2N3265 transistor exhibited pronounced crowding (Fig. 15.c) and a much higher peak junction temperature, in spite of the fact that it has much higher current and voltage ratings (as specified by the manufacturer).

The current crowding experienced by the 2N3879 transistor (Fig. 17.a) differs from that of the 2N3265 and 2N3445 transistors. This is evident from thermal profiles of the 2N3879 transistor operating under dynamic and static loading conditions (Figs. 17.b and 17.c). The fact that the peak junction temperatures in the two cases differ by only 10°C is most unusual and suggests that this device has an unusually high emitter metalli-

zation resistivity (see Section 3.3.7).^{*} This behavior is not typical of epitaxial power transistors and for this reason, further thermographic analysis of this device was not attempted. In any case, the device is conservatively rated by the manufacturer and is therefore capable of dissipating the rated P_T . For example, the manufacturer specifies the thermal resistance as $5^{\circ}\text{C}/\text{watt}$. However, measurements by this author (see Appendix D) indicated a value of the order of $3^{\circ}\text{C}/\text{watt}$. The extent to which the manufacturer has "derated" this device becomes even more apparent when a comparison is made with the 2N3445 transistor. The 2N3445 transistor has an emitter metallization area which is only 50% larger but the device is rated at 115 watts with a thermal resistance of $1.4^{\circ}\text{C}/\text{watt}$.

2.4.3 The Effects of Reverse Base Current Amplitude and Avalanche Mechanisms

It is well known that the second breakdown delay time^{**} of a transistor in the avalanche mode is extremely dependent on the amplitude of the reverse base current

* Because of film limitations, the peak junction temperatures cannot be ascertained from Figs. 17.b and 17.c.

** The interval which begins when the device first enters the avalanche mode and terminates when the collector emitter voltage collapses to a much lower value (second breakdown).

generated by the avalanche mechanism (see for example⁽²⁵⁾). This author has found that this delay time is also very dependent on the amplitude of the reverse base current which flows during the turn-off transition prior to the initiation of avalanche breakdown (the removal of stored base and collector charge). Since a large spike of reverse base current is required for fast switching speeds, it is of interest to establish what influence the spike amplitude has on the thermal profile of a device dissipating power during the turn-off transition (but with a peak collector-emitter voltage less than V_{CEO}). Thermal plots were obtained for a range of reverse base current amplitudes (for a number of devices) but no significant difference between the profiles could be detected. Therefore, it would appear that the spike amplitude may be increased at liberty to realize fast switching times without enhancing the likelihood of device failure.

Early⁽²⁶⁾, and more recently Poorter⁽²⁷⁾, have shown that at high current densities ($J_C > qN_d v_m$), the avalanche breakdown voltage of the collector-base junction of an epitaxial transistor varies inversely with the density of mobile carriers traversing the depletion region. It is conceivable that the turn-off crowding mechanism might yield current densities sufficiently high to reduce the device avalanche breakdown voltage.

This would initiate an additional crowding mechanism because of the negative resistance effect. That is, the collector current would tend to concentrate in the area of the device which first experienced breakdown. Subsequent destruction of the device might occur, even with average device dissipation much less than P_T . The pronounced crowding exhibited in Fig. 15.c is probably largely a result of this avalanche voltage-current density relationship. However, a number of 2N3265 transistors were driven briefly into avalanche breakdown during the turn-off transitions, and in some instances, the hot spot formed directly beneath the emitter contact. It is suggested that this might be attributed to the fact that the avalanche breakdown voltage of a device is inversely related to the resistance in the base circuit. Because of the distances involved, the resistance from a point in the base beneath the emitter contact to the tip of the base metallization stripe is larger than the resistance between points beneath the emitter stripes and the nearest base metallization stripe. Therefore, avalanche breakdown should first occur beneath the emitter contact, unless the collector current density elsewhere in the device is sufficient to effect a lower breakdown voltage.

The breakdown voltage-current density relationship was not considered further since crowding of the form shown in Fig. 15.c was not observed at voltages less than V_{CEO} (data sheet value) regardless of the current being switched. In any case, the switching transitions in current-switching Class-D circuits occur at relatively low voltages and so the breakdown voltage-current density relationship does not present practical limitations.

2.4.4 Crowding in Current-Switching and Voltage-Switching Class-D Applications

The transistor switches in a current-switching amplifier configuration are subjected to a dissipation loading somewhat different than those in a voltage-switching circuit. This has been discussed in detail by this author in a recent paper⁽⁶⁾ and is briefly reviewed here. Relatively speaking, the devices in a high-frequency voltage-switching circuit incur a high average power dissipation during the switching transitions (current spikes, Fig. 3), while the average transition dissipation for devices in the current-switching arrangement is somewhat lower. However, the dissipation during the ON time of the switch tends to be higher in the current-switching circuit than in the voltage-switch. In the

reference quoted, it was stated that although the current-switch collector efficiency is often lower because of the high average ON time dissipation, the circuit is generally capable of a greater output power than the voltage-switching configuration. The reason for this can be explained in terms of the crowding mechanism described in this thesis. That is, power dissipated during a turn-off transition results in higher junction temperatures than for an equivalent power dissipation during the ON time of a switch.

Thermal profiles of two 2N3879 transistors operating first in a voltage-switching amplifier and then in a current-switching amplifier, both at the same frequency (500 kHz) and with the same input power (150 watts), are given in Fig. 18 (the collector current and voltage waveforms corresponding to these profiles are given in Figs. 3 and 4). The voltage-switching circuit had a much lower collector efficiency (65% vs 75%) and also, as is clear from the photographs, the transistors in this circuit exhibited more pronounced crowding and higher peak junction temperatures than those in the current-switching configuration. This example clearly demonstrates the advantages of the current-switching circuit and also, the utility of the thermographic technique.

2.4.5 Current Crowding in Parallel Transistor Switches

The preceeding sections of this thesis have been devoted to considerations of crowding effects within individual devices. However, the theory of nonuniform turn-off also has relevance to arrays of transistors connected in parallel in high-speed switching applications.

To switch very high currents, it is often necessary to connect several transistors in parallel^(5,6). In such cases, it is common practice to provide each device with a small emitter feedback resistor to insure uniform current and power sharing between the devices. While this procedure provides adequate protection for transistors operating in the active mode, it does not insure uniform power dissipation between parallel-connected devices in a high-frequency, saturating-switch application. In a switching environment, the device turn-off times must be matched since failing this, the last element in the array to be turned off will dissipate the bulk of the total power loss incurred by the array during the turn-off transition. Although P_{TOFF} may be small in comparison with the power rating of the array, it may easily exceed the power rating of an individual element. The transistor switching times can be matched by first selecting devices with similar current gain

characteristics and then adjusting the base drive amplitude to the individual elements while monitoring individual device collector current waveforms. Alternatively, the matching can be realized by adjusting the base drives while monitoring device case temperatures with a sensitive thermometer.

2.5 A Method for Relating Power Dissipation and Peak Junction Temperature

In their discussion of the Theory of Lateral Thermal Instability (static case), Steffe and Le Gall⁽²³⁾ stated that the stability of the thermo-electric system of the device is not readily described mathematically since all factors giving rise to divergent local temperature characteristics are nonlinear functions, some of which are not accurately predictable by computation. The stability of the thermo-electric system of the high-speed saturating switch is surely even less amenable to mathematical description and so any model describing the system must be based on observed effects rather than on individual causes. Even then, it is difficult to formulate a model which is valid for devices of different geometry operating over a wide range of conditions. However, for instances where actual thermographic examination of the device under actual operating conditions is not

possible, access to a simple model which yields a realistic estimate of maximum device temperature is essential. An elementary model which is based on the observations in the previous sections and which can be applied to a device switching a square wave of collector current is described in this section.

The power dissipated by the device in a saturating switch can be taken to comprise three components:

- P_{TON} - power dissipation during turn-on transitions
- P_{SAT} - power dissipation while in saturation
- P_{TOFF} - power dissipated during turn-off transitions

From thermal plots similar to those given in the previous section, it is known that P_{TON} and P_{SAT} are normally dissipated fairly uniformly over the extent of the collector-base junction area. However, this is not the case for P_{TOFF} and as was demonstrated in the previous section, this results in a nonuniform temperature distribution on the surface of semiconductor die. The thermal profiles of the 2N3265 transistor appear to indicate that the major fraction of P_{TOFF} is dissipated by the region of the device adjacent to the emitter contact. The darkened areas (hot spots) in Figs. 15.a and

15.b appear to cover about one third of the total device area. It would therefore appear reasonable to suggest that for purposes of dissipating P_{TOFF} , the device has a thermal resistance which is three times as large as that which exists for dissipating P_{TON} and P_{SAT} . Therefore, for a first approximation, the peak junction temperature of a high-speed saturating switch may be described by an expression of the form

$$T_{MAX} = T_{CASE} + (P_{SAT} + P_{TON})\theta + MP_{TOFF}\theta \quad (2.1)$$

where M is a constant (equal to 3 for the 2N3265 transistor). Judging from the devices considered in this study, a value of M equal to three appears to be a valid worst-case estimate which may be applied when actual thermographic examination of the device is not possible. However, for devices such as the 2N3445 which exhibit only limited crowding, a value much less than three may be used.

Normally, a value for θ may be obtained from data sheets. However, it is suggested that the method given in Appendix D be used to determine the thermal resistance of the device since this enables one to measure θ at defined current and voltage levels.

For design purposes,* it is desirable to rewrite Eqn. 2.1 in terms of current, voltage and switching frequency. Such a representation would enable one to calculate the maximum collector current that could be switched for a given maximum junction temperature, peak collector-emitter voltage, switching frequency, and other parameters. P_{SAT} may be written in terms of current and device parameters by using Eqn. 4.7, an expression for the average saturation voltage during the ON time of a transistor switch (see Section 4.3). However, the device parameters in Eqn. 4.7 are also functions of temperature. Because of this, it is unlikely that Eqn. 2.1 can be presented in a form which would enable one to actually predict the peak collector current which may be switched for a given T_{MAX} . Therefore, Eqn. 2.1 may be used only for obtaining estimates of T_{MAX} for specified values of P_{SAT} , P_{TON} and P_{TOFF} .

It is suggested that T_{MAX} be limited to 150°C (or less). This should provide a safety margin against the shortcomings of the model.

Since avalanche effects were considered to be beyond the scope of this study, no attempt was made to develop a model which would accommodate operation in the avalanche mode. It is evident however, that the effect-

ive thermal resistance is considerably enhanced if the device is driven into avalanche breakdown (see Fig. 15.c). It would appear from the area of the hot spot in Fig. 15.c, that a tenfold increase in device thermal resistance might be assumed for a first approximation.

CHAPTER 3

COLLECTOR-EMITTER SATURATION VOLTAGE AND COLLECTOR CHARGE STORAGE - STATIC CASE

3.1 Introduction

The collector efficiency of a Class-D circuit is a sensitive function of the collector-emitter saturation voltage. Large-area triple-diffused and epitaxial transistors, the devices most commonly used in such applications, exhibit a collector-emitter saturation voltage which is large in comparison with that of an alloy device so it is essential that this aspect of device operation be thoroughly understood. A one-dimension analysis of conductivity modulation in the collector region is developed in this chapter using the transport equations and charge-control concepts and results in an expression for static collector-emitter saturation voltage in terms of collector current, base current, and device parameters. The analysis is extended to demonstrate that the falloff of device current gain at high current levels and low collector-emitter voltages should be interpreted in terms of saturation effects rather than in terms of base stretching and hot carrier phenomena. Also, the analysis is used to describe the charge distri-

bution responsible for the nonuniform discharge mechanism experienced by high-frequency switches.

3.2 Analysis

For purposes of this study, a collector doping profile of the form shown in Fig. 19 is assumed (impurity density on the base side of the collector-base junction much greater than that on the collector side).^{*} The analysis proceeds from the two transport equations and the requirement that total current be continuous:

$$J_n = q\mu_n E(n + n_o) + qD_n \frac{dn}{dx} \quad (3.1)$$

$$J_p = q\mu_p E(p + p_o) - qD_p \frac{dp}{dx} \quad (3.2)$$

$$J_C = J_n + J_p \quad (3.3)$$

where n and p represent injected carrier densities and n_o and p_o represent equilibrium densities. Eqns. 3.1, 3.2 and 3.3 are applied in two distinct cases:

$$a) \quad n \gg n_o = N_d, \quad p \gg p_o = \frac{n_1^2}{N_d}$$

* In this analysis, as throughout the thesis, a NPN structure is assumed.

$$b) \quad n \ll n_o, \quad p \ll p_o$$

Considering Case (a) and assuming quasi-neutrality ($p \approx n$) gives

$$J_n = q\mu_n E p + qD_n \frac{dp}{dx} \quad (3.4)$$

$$J_p = q\mu_p E p - qD_p \frac{dp}{dx} \quad (3.5)$$

Hole current is small in the high-resistivity collector region since W_c is much less than the carrier diffusion length and also, there is negligible hole flow through the $N_d N^+$ boundary, so Eqn. 3.5 can be reduced to

$$\mu_p E p = D_p \frac{dp}{dx} \quad (3.6)$$

An expression for E follows from the substitution of Eqns. 3.4 and 3.5 into Eqn. 3.3

$$E = \frac{J_c - q(D_n - D_p) \frac{dp}{dx}}{qp(\mu_n + \mu_p)} \quad (3.7)$$

Combining Eqns. 3.6 and 3.7 gives

$$\frac{dp}{dx} = \frac{J_c}{2qD_n} \quad (3.8)$$

and therefore

$$p(x) = \frac{J_C x}{2qD_n} + p(0). \quad (3.9)$$

When $n \ll N_d$ (Case (b)), Eqn. 3.1 can be simplified to

$$J_C = q\mu_n N_d E. \quad (3.10)$$

The regions in which Eqns. 3.8 and 3.10 are considered to be valid are defined by the coordinate x_c in Fig. 19. The location of this breakpoint is found from a consideration of recombination in the N_d region. The expression

$$I_{BC} = \frac{qA}{\tau_c} \int_0^{x_c} p(x) dx$$

represents the hole current from base to collector required to satisfy recombination in the N_d region (a constant, effective lifetime τ_c is assumed).

Again we consider two cases:

$$1) \quad x_c \leq W_c$$

$$2) \quad x_c > W_c$$

First, for $x_c \leq W_c$,

$$I_{BC} = -qx_c^2 \frac{A}{2\tau_c} \frac{dp}{dx}.$$

With the aid of Eqn. 3.8, x_c is found to be

$$x_c = \sqrt{\frac{-4\tau_c D_n I_{BC}}{I_C}} \quad (3.11)$$

where, in accordance with the sign convention of Fig. 19, I_C carries a negative sign.

The injected minority carrier density at the collector side of the collector-base junction is then given by

$$\begin{aligned} p(o) &= x_c \frac{dp}{dx} \\ &= -\frac{J_C}{q} \sqrt{\frac{-\tau_c I_{BC}}{D_n I_C}} \end{aligned} \quad (3.12)$$

The net minority carrier density at the same point is given by:

$$P(o) = \frac{n_i^2}{N_d} - \frac{J_C}{q} \sqrt{\frac{-\tau_c I_{BC}}{D_n I_C}} \quad (3.13)$$

For $x_c > W_c$,

$$I_{BC} = \frac{qAW_c}{2\tau_c} \{P(o) + P(W_c)\} - \frac{qAW_c n_i^2}{\tau_c N_d} + qAS \{P(W_c) - \frac{n_i^2}{N_d}\}$$

where the last term is representative of the recombination in the heavily-doped collector substrate. Expressing $P(o)$ in terms of $P(W_c)$

$$\begin{aligned}
 P(0) &= P(W_c) - W_c \frac{dp}{dx} \\
 &= P(W_c) - \frac{W_c J_C}{2qD_n}
 \end{aligned}$$

and solving for $P(W_c)$ gives

$$P(W_c) = \left\{ I_{BC} + \frac{I_C W_c^2}{4\tau_c D_n} \right\} \frac{\tau_c}{qA(W_c + S\tau_c)} + \frac{n_i^2}{N_d}. \quad (3.14)$$

For the case $x_c < W_c$, the collector-emitter saturation voltage is given by the sum of the integrals of the field expressions (Eqns. 3.7 and 3.10) and the potential drops across the forward-biased junctions:

$$\begin{aligned}
 V_{SAT} &= \int_0^{x_c} \left\{ \frac{J_C}{(q(\mu_n + \mu_p)p)} - \frac{(D_n - D_p)}{(\mu_n + \mu_p)p} \frac{dp}{dx} \right\} dx \\
 &\quad - \int_{x_c}^{W_c} \frac{J_C}{q\mu_n N_d} dx + V_{BE} - V_{BC}.
 \end{aligned}$$

Integrating and simplifying, Eqn. 3.15 results:

$$\begin{aligned}
 V_{SAT} &= V_{BE} - \frac{kT}{q} \ln \frac{N_d P(0)}{n_i^2} - \frac{kT}{q} \ln \left\{ \frac{J_C x_c}{2qD_n p(0)} + 1 \right\} \\
 &\quad - \frac{J_C (W_c - x_c)}{q\mu_n N_d}. \quad (3.15)
 \end{aligned}$$

For $x_c \geq W_c$, the last term in Eqn. 3.15 is dropped and x_c in the third term is changed to W_c .

Equation 3.15 may be simplified further since the contribution of the third term is normally less than 100 millivolts. This simplification was utilized in many of the calculations given in this thesis.

It should be noted that this analysis is based on the assumption that $n \ll N_d$ in the region $x_c < x < W_c$. This assumption places a limitation on the validity of the model since at current densities of the order of $qv_m N_d$, velocity saturation occurs and further increases in current density are accompanied by increases in carrier density rather than carrier velocity⁽²⁶⁾. That is, conduction in the region becomes space-charge-limited and the carrier density may approach or even exceed N_d . However, in the sections which follow, it is shown that the analysis is useful over a wide range of currents and fails only at very high current levels or in cases where the device experiences unusually pronounced current crowding. A simplified analysis of the space-charge-limited case is attempted in Section 3.3.7.

3.3 Applying the Analysis

A procedure for calculating the saturation characteristics of a device can best be described in terms of a flow chart. Such a chart is given in Fig. 20.

Although the analysis does not require a computer, the chart is presented in a form suitable for programming purposes.

The parameters which appear in the analysis are discussed in turn in the subsections which follow. Also, examples of the application of the analysis are given which demonstrate both the utility of the approach and the inherent limitations.

3.3.1 Collector Current Density J_C

The analysis presented in the previous section was developed assuming a uniform distribution of collector current density (that is, a one-dimensional analysis). It is necessary to qualify this assumption since Hauser⁽²⁸⁾ has demonstrated that the emitter (or collector) current density across the width of an emitter diffusion stripe may vary by a factor of two or more depending on the emitter current density and device geometry (emitter-edge crowding). Although Hauser's analysis does not account for conductivity modulation effects in the base region or include the dependence of current gain on emitter current density (that is, it does not allow for high-level-injection effects), it is at least "monotonically correct" for devices operating at very high current

densities since these two effects tend to compensate for each other. The general form of the current distribution described by Hauser is shown in Fig. 21 ($J_C(z)$), while the salient points of his analysis are reproduced in Appendix F.

In addition to the emitter-edge crowding described by Hauser, Cave and Barnes⁽¹⁶⁾ have shown that the collector current density also varies along the length of the emitter stripe (see Fig. 21, $J_C(y)$). Their analysis relates the current density variation along the emitter stripe to the resistivity of the emitter metallization (see Appendix A). However, as is discussed in a following section, this author has found that their analysis predicts a degree of crowding which is greater than that observed in practice and the explanation is offered that other effects in addition to emitter metallization resistivity must be included in any such analysis.

Rather than attempting to modify the analysis given by Cave and Barnes (and Hauser) and incorporating the results into the present study, this author chose to account for crowding phenomena by assuming that a uniform collector current density given by

$$J_C = \frac{I_C}{\text{area of emitter metallization}} = \frac{I_C}{A} \quad (3.16)$$

exists in the area defined by the emitter metallization. Current density is assumed to be equal to zero elsewhere (see Fig. 21). Since the collector-emitter saturation voltage characteristics of a device are ultimately defined by the region of the device having the highest collector current density, close agreement between calculated and observed collector-emitter saturation voltages will be obtained only if the density given by Eqn. 3.16 is approximately equal to the peak current density experienced by the device. It is reasoned that since the area of the emitter metallization is somewhat less than the area of the emitter diffusion, this technique of assigning current density will account for some crowding but, of course, will be valid over only a limited range. As is demonstrated later in this section, it has been found that realistic results may be obtained using this procedure for current densities at least as high as 150 Amp/cm². For calculations involving current densities greater than 150 Amp/cm², it may be necessary to modify the result given by Eqn. 3.16 by an experimentally-determined factor. It is suggested that progressively smaller areas be assumed until close agreement between calculated and observed saturation voltage is obtained.

The merits of this approach become evident when one considers the alternatives. For example, it is evident from the analyses given by Cave and Barnes and by Hauser, that an analytical solution of a two-dimensional current distribution problem is probably not achievable. Therefore, a two-dimensional analysis could be conducted only by resorting to a computer simulation of the device. A computer simulation is not only very complex and expensive, but also, is unattractive because of the loss of analytical representation of identifiable physical effects.

3.3.2 Current I_{BC}

The current I_{BC} represents the hole current from the base required to satisfy recombination in the collector region. For the purposes of this thesis, it is related to terminal currents and device parameters by the expression

$$I_{BC} = K(I_B + \frac{I_C}{h_{FEO}}), \quad (3.17)$$

where K is a constant < 1 .

Eqn. 3.17 bears a close resemblance to

$$I_{BS} = I_B + \frac{I_C}{h_{FEO}} \quad (3.18)$$

which represents the base current over and above that

required to maintain a transistor in the saturated state⁽²⁹⁾. In the case of a saturated alloy transistor, by far the greater portion of the current I_{BS} is required for the charging of the base region while only a small fraction is injected into the emitter or collector regions. However, this is not the case for triple-diffused and epitaxial devices since these structures have a lower inverse emitter efficiency* because the collector donor density N_d is less than the base impurity density. Since a detailed analytical description of the division of I_{BS} into its various components was considered to be beyond the scope of this study, the assumption was made that I_{BC} could be related to I_{BS} by a factor K . It is subsequently shown in this section that in spite of this assumption, close agreement between calculated and measured saturation characteristics is possible.

* The emitter efficiency with the roles of collector and emitter interchanged. A comparison of inverse alpha provides some indication of the relative magnitudes of the inverse emitter efficiencies for the two basic structures. This author has found that inverse alphas of 0.75 and 0.95 are typical of epitaxial and alloy power transistors respectively. It should be noted that the inverse emitter efficiency of a saturated epitaxial (or triple-diffused) device cannot be obtained from a routine analysis of diffusion currents resulting in inverse emitter efficiency as a function of a ratio of impurity densities (as for example, is the case for emitter efficiency of alloy devices⁽³⁰⁾), since the effect of the field established by the flow of majority carriers in the N_d region must be included.

The factor K may be determined using Eqn. 3.14 and a set of transistor $V_{CE} - I_C$ characteristic curves. The breakpoint separating the two segments of the two-stage saturation curve (Fig. 22) corresponds to the injected minority carrier density at the point W_c being equal to zero. Thus, K may be determined by representing I_{BC} by Eqn. 3.17 and setting the first term in Eqn. 3.14 equal to zero.

It should be mentioned that although Eqn. 3.17 enables one to accurately describe collector-emitter saturation voltage in terms of terminal currents and device parameters, the hole current which actually flows from the base to the collector in the device is not necessarily equal to I_{BC} . This is evident from a consideration of Fig. 21. Since an assumption was made that the collector current density distribution was uniform and equal in magnitude to the peak density which occurs in practice, the amount of stored collector charge given by the present analysis may be greater than that which is actually stored. I_{BC} is directly proportional to the amount of stored charge, and therefore, the predicted value of I_{BC} may also be greater than that which occurs in fact. This particular limitation of the study will not be overcome until a two-dimensional analysis is developed (see Section 3.3.1 for a brief discussion of the difficulties inherent in a two-dimensional analysis).

In addition to establishing the value of K , it is also necessary to define a value for h_{FE0} which will accurately describe the excess base current. Ideally, the device current gain should be experimentally determined using

$$h_{FE} = \frac{I_C}{I_B - I_{BS}} \quad \left| \quad V_{BC} > 0 \right. \quad (3.19)$$

but, of course, such a measurement is not possible. This hypothetical measurement should be made with the collector-base junction forward biased for a number of reasons. First, the base width (and volume) is enhanced when the collector-base bias is changed from reverse to forward because of the resultant change in depletion layer width. With an increase in base volume, the device current gain is degraded since a larger base current is then required to satisfy the recombination requirements. Also, with the collector-base junction forward biased, the charge carrier density in the base in the vicinity of the collector-base junction is enhanced. Since the carrier lifetime is inversely related to the carrier density (see for example⁽³¹⁾), lifetime in this region is decreased, again at the expense of device current gain. These two factors are particularly relevant to alloy

transistors since the base width of an alloy device is very dependent on the collector-base junction potential. Also, these devices have a high inverse emitter efficiency, and therefore the charge carrier density in the base region near the collector-base junction is considerably enhanced when the junction is forward biased. The influence of these two factors is minimized if the base impurity density is greater than that in the collector region adjacent to the junction, as is the case with epitaxial and triple-diffused transistors. Therefore, for the purposes of this thesis, it is suggested that an approximation for h_{FEO} be determined from the device $V_{CE} - I_C$ characteristic curves using the equation

$$h_{FEO} = \frac{I_C}{I_B} \quad \left| \quad V_{BC'} = 0 \right. \quad (3.20)$$

The locus of the points at which the measurement may be made is marked on the characteristic curves shown in Fig. 22. $V_{BC'}$ was estimated to be approximately equal to zero along the curve.

3.3.3 Mobility μ_n and Diffusion Constant D_n

The effect of temperature on collector-emitter saturation voltage is considered in this thesis and so

it is essential that the functional dependence of μ_n and D_n on temperature be described. Evans⁽³²⁾ and Morin and Maita⁽³³⁾ have shown that the temperature dependence of carrier mobility can be described by an expression of the form

$$\mu_n = CT^{-2.5} \quad (3.21)$$

where C is a constant approximately equal to 2×10^9 (assuming impurity densities less than 10^{15} atoms/cm³ and electric field strengths of the order of 10^3 volts/cm or less). If electric field strengths much greater than 10^3 volts/cm are anticipated, the relationship between mobility and field strength must be considered. Caughey and Thomas⁽³⁴⁾ have developed the following expression which provides a fit of the experimental dependence of carrier mobility on field strength:

$$\mu_n = \frac{\mu_{no}}{\sqrt{1 + \left(\frac{E}{E_0}\right)^2}} \quad (3.22)$$

where μ_{no} represents the low-field mobility (given by Eqn. 3.21) and E_0 equals 8000 volts/cm.

It is convenient to develop a general expression for collector-emitter saturation voltage which incorporates the field and temperature dependence of mobility as expressed by Eqn. 3.22. A substitution of Eqn. 3.22 in-

to Eqn. 3.10 gives

$$J_C = \frac{qN_d\mu_{no}E}{\sqrt{1 + \left(\frac{E}{E_0}\right)^2}}.$$

Solving for E and integrating with respect to x, the potential drop across the unmodulated, high-resistivity collector region is found to be:

$$V = - \frac{J_C(W_c - x_c)}{\sqrt{(q\mu_{no}N_d)^2 - \left(\frac{J_C}{E_0}\right)^2}}. \quad (3.23)$$

Therefore, by replacing the final term in Eqn. 3.15 with Eqn. 3.23, one obtains a general expression for collector-emitter saturation voltage which includes the field dependence of mobility:*

$$V_{SAT} = V_{BE} - \frac{kT}{q} \ln \frac{N_d P(o)}{n_i^2} - \frac{kT}{q} \ln \left\{ \frac{J_C x_c}{2qD_n p(o)} + 1 \right\} \\ - \frac{J_C(W_c - x_c)}{\sqrt{(q\mu_{no}N_d)^2 - \left(\frac{J_C}{E_0}\right)^2}}. \quad (3.24)$$

* Note that the validity of the assumption $n \ll N_d$ should be questioned in cases where the field dependence of mobility must be considered (see Section 3.4).

An expression which describes the temperature dependence of D_n may be developed from Eqn. 3.21 and the Einstein relation:

$$D_n = \frac{CkT^{-1.5}}{q} \quad (3.25)$$

The effect of field strength on D_n need not be considered since the field strength in the region $0 < x < x_c$ is normally much less than 10^3 volts/cm.

Carrier mobility μ_n and the diffusion constant D_n are also functions of doping levels and carrier densities⁽³⁴⁾. However, for the doping levels considered in this thesis ($N_d < 10^{15}$) mobility is not a sensitive function of doping density and so the mobility as given by Eqn. 3.21 (or 3.22) may be applied directly in the final term of Eqn. 3.15 (or 3.24).

At impurity densities of the order of 10^{16} atoms/cm³ an inverse relationship exists between impurity density and the diffusion constant D_n ⁽³⁴⁾. This dependence should perhaps have been included in the analysis since carrier densities of the order of 10^{16} are anticipated in the region $0 < x < x_c$. However D_n was assumed to be a constant in the analysis developed in Section 3.2 and, in spite of this, the results given

by Eqn. 3.15 agree well with those observed in practice. The fact that the saturation voltage as given by Eqn. 3.15 varies with the square root of D_n rather than directly may in part account for this agreement. Also, it is likely that carrier densities of the order of 10^{16} exist only in a small portion of the interval $0 < x < x_c$.

3.3.4 Collector Lifetime τ_c , Impurity Density N_d , and Width W_c

The variation with time of the open-circuit voltage of an initially forward-biased pn junction is dependent on the minority carrier lifetime (see Appendix E). It is shown in Appendix E that the effective lifetime of minority carriers in the lightly-doped collector region may therefore be determined from the slope of the collector-base junction open-circuit decay voltage.

The impurity density N_d may be determined from a capacitance-voltage measurement of the collector-base junction (see Appendix G).

It is shown in Appendix H that the static saturation voltage analysis given in this thesis enables one to determine W_c from the locus of the curve $V_{BC} = 0$ on the static $V_{CE} - I_C$ characteristic curves, provided N_d and A are known. It is also shown that W_c for a mesa

transistor may be determined from a measurement of the collector-base junction breakdown voltage.

3.3.5 Intrinsic Carrier Concentration n_i and the Recombination Velocity S

The intrinsic carrier concentration is given by the well-known expression:

$$n_i^2 = (15)(10^{32})T^3 e^{-\frac{1.21}{kT}}.$$

The recombination velocity S is a measure of the recombination rate in the heavily-doped collector substrate. The value of S is not critical since saturation voltage is not a sensitive function of this factor. One may obtain an estimate of the value of S by assuming that the transport of minority carriers in the collector substrate is primarily by diffusion, in which case

$$q \frac{D_p p(W_c)}{L} = q p(W_c) S,$$

where L represents the diffusion length of holes in the substrate. Hence,

$$S = \left(\frac{D_p}{\tau} \right)^{\frac{1}{2}}.$$

For the purpose of this thesis, the collector substrate impurity density and minority carrier lifetime were assumed to be 10^{20} atoms/cm³ and 10^{-8} sec respectively (this value for lifetime was used by Larin* for a heavily-doped emitter and was arbitrarily selected for calculations in this thesis).

3.3.6 Base-Emitter Junction Voltage V_{BE}

In this thesis, the terminal base-emitter voltage quoted by the manufacturer is used in the calculation of saturation voltage. It is realized that the terminal base-emitter potential includes ohmic drops in the extrinsic base region which do not contribute to the collector-emitter saturation voltage, but since Eqn. 3.15 provides neither for potential drops in the emitter and base bulk nor for lead resistance, an enhanced value for base-emitter junction voltage serves to improve the agreement between calculated and observed values of collector-emitter saturation voltage. Close agreement is possible since both the extrinsic base region potential drop and the other potential drops are small (normally less than 500 millivolts), and in any case, are of opposite polarity.

* F. Larin, "Radiation Effects in Semiconductor Devices"; New York, J. Wiley, 1968, pp. 25-28.

3.3.7 Results and Observations

A comparison is given in this section of the calculated and measured static collector-emitter saturation voltage characteristics of a 200 volt, 3.5 ampere, 80 watt, triple-diffused transistor (DTS 410), a 60 volt, 7.5 ampere, 115 watt epitaxial transistor (2N3445) and a 75 volt, 7.0 ampere, 35 watt epitaxial device (2N3879).*

A set of measured $V_{CE}-I_C$ characteristic curves for the high-voltage triple-diffused device (DTS 410) is given in Fig. 22 (junction temperature $\approx 35^\circ\text{C}$). Calculated saturation curves (Eqn. 3.15) for this device with junction temperatures of -40°C , $+35^\circ\text{C}$, and $+135^\circ\text{C}$ are given in Fig. 23 (device parameters are tabulated in Appendix C). The close agreement with observed characteristics may be taken as an indication of the validity (and utility) of the model.

For the purposes of these calculations, the temperature sensitivity of the parameters τ_c , μ_n , D_n and n_i were described by the expressions given in this thesis. However, measured values of h_{FE} were used

* The analysis was not applied to the 25 ampere epitaxial power transistor (2N3265) which was studied in Chapter 2 since a curve tracer capable of displaying the device characteristics at near-rated currents was not available.

since a valid analytical description of the temperature dependence of h_{FE} does not appear to be available in the literature.* The analysis revealed that the collector-emitter saturation voltage at the extremes of temperature is particularly sensitive to the parameters μ_n and h_{FE} and to a lesser extent, τ_c . Current gain h_{FE} and τ_c both increase with temperature, thus tending to reduce the collector-emitter saturation voltage (assuming I_C and I_B remain fixed while temperature is varied). However, μ_n varies inversely with temperature and so contributes to an increase of saturation voltage with temperature. The net effect of temperature can be described as follows: for a device operating within the second stage of the saturation characteristics and with base and collector currents maintained constant, collector-emitter saturation voltage decreases with temperature. However, it should be mentioned that at very low temperatures, h_{FE} is reduced considerably and hence the device operating point may shift from the saturated state

* The following paper was published after the completion of this thesis: D. Buchanan, "Investigation of current-gain temperature dependence in silicon transistors", IEEE Trans. Electron Devices, Vol. 16, No. 1, pp. 117-124, January, 1969. Buchanan conducted an interesting experimental study (by varying base and emitter doping levels) as well as a "piece-by-piece order-of-magnitude" analytical study of the effect of temperature on device current gain.

to the active mode with a resultant drastic increase in collector-emitter voltage (and conceivably, device failure occurring via second breakdown).

A set of measured $V_{CE}-I_C$ characteristic curves for the 60 volt, 7.5 ampere, 115 watt epitaxial transistor (2N3445) is shown in Fig. 24.a. In comparing these characteristics with those of the previous device, it is seen that the 2N3445 has a much lower saturation voltage (2 volts vs. 6.5 volts at $I_C = 2$ Amp), but it should be noted that the 2N3445 has a much higher collector current rating (7.5 Amp vs. 3.5 Amp) and so may exhibit a saturation voltage of the same order of that of the DTS 410 when the devices are passing their rated currents.

A calculated saturation curve of the 2N3445 transistor is shown in Fig. 24.b. Considerable difficulty was experienced in obtaining close agreement between calculated and observed curves for this device. In fact, a redefinition of the active transistor area (defined as the area of the emitter metallization in Section 3.3.1) was necessary to achieve the fit demonstrated in Fig. 24.b. The justification for the redefinition of device area becomes apparent upon a comparison of the metallization arrangements of the 2N3445 and

the DTS 410 transistors (Fig. 25.a). With the latter device, all portions of the emitter metallization are bounded by base metallization stripes of relatively constant separation (i.e., $W_1/W_2 \approx 1.2$). However, this is not the case for the 2N3445 where $W_1/W_2 \approx 3$. This suggests that for this device, the current density in the central-emitter area (enclosed by the rectangle in Fig. 25.a) will be relatively low in comparison with the density along the emitter stripes, in which case the central-emitter area should not be included in the determination of active transistor area. A thermal profile of the 2N3445, obtained when the transistor was biased at an operating point of $I_C = 6$ Amp, $V_{CE} = 13$ volts, confirmed that the power density (and hence, current density) in the central-emitter area was less than that along the emitter stripes (see Fig. 25.b). The reader may notice that in the thermal profile shown in Fig. 16.b (power dissipation in a high-frequency switch), the contrast in fluorescent brilliance between the central-emitter area and the emitter fingers appears to be less than that in Fig. 25.b. It is believed that avalanche effects in the dynamic case account for the power dissipation in the central-emitter region.

A set of V_{CE} - I_C characteristics curves for the 75 volt, 7 ampere, 35 watt epitaxial device (2N3879) is given in Fig. 26.a. In comparison with the saturation curves given for the two other examples, this device has a poorly-defined second stage; indeed, it is not possible to specify, with any degree of certainty, the point at which the second stage of the saturation curve terminates and the device enters the active mode. However, it is not apparent how an epitaxial transistor can be operating in the active mode and yet exhibit characteristic curves which indicate (by their slope) a static output impedance of several ohms. One must, therefore, conclude that for the device characteristics shown in Fig. 26.a, the second stage of the saturation curve extends at least to the upper-right-hand corner of the set of curves. As will be seen in Section 4.4, the dynamic saturation characteristics confirm the validity of this assumption. For analytical purposes, the locus of the point at which $V_{BC} = 0$ (i.e., the onset of saturation) was estimated and is shown marked on Fig. 26.a. A saturation curve calculated assuming a carrier mobility independent of field strength (Eqn. 3.15) is shown in Fig. 26.b. It is seen that agreement between theory and practice is poor, particularly at the higher values of collector current. To determine if this error could be related

to the field dependence of carrier mobility, the saturation voltage at a collector current of two amperes was calculated using Eqn. 3.24. This equation predicted a saturation voltage only sixteen millivolts greater than that given by Eqn. 3.15. In a further attempt to account for the error, the active transistor area was assumed to be one half of the area of the emitter metallization and the saturation voltage at two amperes recalculated, first assuming a constant carrier mobility and then with mobility as a function of electric field strength. The results of these calculations are also plotted in Fig. 26.b where it is seen that the calculated values agree reasonably well with each other and with the estimated value of saturation voltage. This suggests that a crowding mechanism is, in fact, responsible for the shape of the saturation curves.

An attempt was made to establish the reasons why this particular device exhibits such pronounced current crowding. DC potential probing along the emitter metallization of 2N3879 transistors indicated that this device has an emitter metallization of unusually-high resistivity. For example, with a collector current of three amperes, a potential drop of 200 millivolts was measured along the length of an emitter stripe (while the poten-

tial drop along a base stripe was of the order of 20 millivolts). For assumed base-emitter junction voltages of 600 millivolts and 780 millivolts at opposite ends of an emitter stripe, the theory of Cave and Barnes⁽¹⁶⁾ gives the ratio of collector current densities at the extreme ends of the emitter stripe as

$$\frac{e^{(30)(.78)} - 1}{e^{(30)(.60)} - 1} = e^{5.4} = 222$$

(for an assumed junction temperature of 125°C). Although a thermal profile of the device (Fig. 17.c) indicates a much smaller ratio of current densities (perhaps a ratio of 4 or 5), it is clear from the thermal profile that this crowding mechanism is most likely responsible for the peculiar saturation characteristics of this device. Until such time as the analysis given by Cave and Barnes is modified to include resistive drops elsewhere in the device, it will not be possible to describe the crowding mechanism analytically, and it will therefore be necessary to resort to thermographic techniques to obtain an estimate of the peak collector current density required for calculations of collector-emitter saturation voltage.

Attempts were made to reduce the emitter metallization resistance by bonding gold wires in parallel

with the existing metallization. It was found that the emitter and base metallization consisted of a thin layer of deposited aluminum which was covered with a thick layer of metal-filled paste. The entire surface of the device was coated with a layer of a clear plastic-like material (probably a silicone). Prior to the bonding of the gold wire, the plastic material and the metal-filled paste were removed by mechanical means and a thermal profile obtained ($V_{CE} = 10$ volts, $I_C = 3$ Amps). The thermal profile and the device $V_{CE}-I_C$ characteristics indicated that the crowding in the "modified" device was even more pronounced. It would seem that the metal paste not only reduces the emitter metallization resistance, but also, as does the plastic material, facilitates heat transfer over the surface of the semiconductor die.

The largest diameter gold wire which could be attached using the facilities available to the author (ball bonder) was 0.7 mil.* The current-carrying capa-

* Ball bonding of larger diameter wire, say 2.0 mil, necessitated heating the transistor header to such a high temperature (in order to attain the required temperature on the surface of the die) that the die became detached from the header. This difficulty could be overcome by using an ultrasonic wire bonder.

bility of 0.7 mil gold wire is limited and, in fact, the gold wires melted when the device characteristics were displayed on the curve tracer (2 amperes collector current). However, at a lower current, prior to the melting of the wire, the device exhibited a well-defined two-stage saturation characteristic.

3.4 Space-Charge-Limited Conduction

In the analysis of saturation voltage given in Section 3.2, the assumption was made that the injected carrier density n in the region $x_c < x < W_c$ was much less than the impurity density N_d . For transistors in which very high current densities occur, such as in the 2N3879, it is necessary to establish the limitations imposed by this assumption.

The flow of current in the interval $x_c < x < W_c$ is governed by the equation

$$J_C = q(n + N_d)\mu_n E = -q(n + N_d)v. \quad (3.26)$$

Incorporating the relation developed by Caughey and Thomas⁽³⁴⁾ which describes the carrier velocity variation with field strength, Eqn. 3.26 becomes

$$J_C = \frac{q(n + N_d)v_m E}{E_o \sqrt{1 + \left(\frac{E}{E_o}\right)^2}} \quad (3.27)$$

where $v_m = 1.1 \times 10^7$ cm/sec
and $E_0 = 8 \times 10^3$ volts/cm.

For carrier velocities less than about 10^7 cm/sec, increases in current density occur as a result of increases of carrier velocity. In such cases, $n \ll N_d$ (that is, neutrality exists) and Eqn. 3.27 may be simplified to

$$J_C = -qN_d v = \frac{qN_d v_m E}{E_0 \sqrt{1 + \left(\frac{E}{E_0}\right)^2}} \quad (3.28)$$

The resulting potential drop in the region $x_c < x < W_c$ may be obtained by solving Eqn. 3.28 for electric field strength and integrating with respect to x (see Section 3.3.3, Eqn. 3.23).

If the carrier velocity predicted by Eqn. 3.28 is of the order of 10^7 cm/sec (or greater) the assumption that $n \ll N_d$ may be invalid. In such cases, increases in current density occur as a result of increases in injected carrier density n since carrier velocity cannot exceed 1.1×10^7 cm/sec. If n is not small in comparison with N_d , a charge density given by

$$\frac{dE}{dx} = -\frac{q}{\epsilon} n \quad (3.29)$$

will exist in the region $x_c < x < W_c$. Eqns. 3.27 and 3.29 may be combined to yield a differential equation in terms of field strength:

$$\{\mu_{no} \epsilon E \frac{dE}{dx}\}^2 - 2q\mu_{no}^2 \epsilon E^2 \frac{dE}{dx} + E^2 \{q^2 \mu_{no}^2 N_d^2 - (\frac{J_C}{E_0})^2\} - J_C^2 = 0.$$

No attempt was made to obtain solutions for this equation since for the majority of the device considered in this thesis, peak collector current densities at near-rated collector currents were such that the assumption $n \ll N_d$ appeared to be valid. The only exception to this was the 2N3879 transistor which experiences an unusually high degree of crowding. An analysis which might prove to be useful in such special cases is described in the following paragraph.

Analytical solutions for field strength and potential in the collector region can be obtained if current density is sufficiently high that v equals v_m for all values of $x_c < x < W_c$ and a boundary condition is known. In such instances,

$$J_C = -q(n + N_d)v_m$$

and

$$\frac{dE}{dx} = -\frac{q}{\epsilon} n$$

and therefore

$$E = - \frac{qn}{\epsilon} (x - x_c) - E_o$$

(assuming $E(x_c) = - E_o$).

Integrating again with respect to x ,

$$V = \frac{q}{2\epsilon} \left(- \frac{J_c}{qv_m} - N_d \right) (x - x_c)^2 + E_o (x - x_c).$$

Because of the difficulty in ascertaining J_c and $E(x_c)$, no attempt was made to apply this analysis to the 2N3879 transistor.

3.5 Current Gain (h_{FE}) Falloff at High Current Densities

The h_{FE} characteristics of epitaxial and triple-diffused power transistors are commonly specified in data sheets as a function of collector current at a low, constant collector-emitter voltage, say two or three volts. It is seen in these plots that h_{FE} falls off drastically at the higher current levels. Larin⁽¹²⁾ and more recently this author⁽³⁵⁾ have suggested that the falloff of h_{FE} at high current densities could be related to the storage of minority charge carriers in the collector region. That is, the devices may be operating in saturation at the higher current levels.

An analysis which confirms this theory is developed in the following paragraphs by applying aspects of the saturation model first described in Section 3.2.

The saturation voltage of a device operating within the second stage of the saturation region is defined largely by the final term of Eqn. 3.15, that is,

$$V_I = - \frac{I_C(W_c - x_c)}{qN_d\mu_n A} \approx V_{SAT} + V_{BC'} - V_{BE}.$$

The variable x_c in the above equation is given by Eqn. 3.11 as

$$x_c = \sqrt{\frac{-4\tau_c D_n I_{BC}}{I_C}} = \sqrt{4\tau_c D_n K \left(\frac{1}{\beta} - \frac{1}{h_{FEO}} \right)}$$

where

$$\beta = \left. \frac{I_C}{I_B} \right|_{V_{BC'} > 0}.$$

Combining the above equations gives

$$V_I = - \frac{I_C \{ W_c - \sqrt{4\tau_c D_n K \left(\frac{1}{\beta} - \frac{1}{h_{FEO}} \right)} \}}{q\mu_n N_d A},$$

from which we obtain

$$\begin{aligned}
 \beta &= \frac{1}{\frac{1}{h_{FEO}} + \frac{1}{4\tau_c D_n K} \left\{ W_c + \frac{qN_d \mu_n A V_I}{I_C} \right\}^2} \\
 &= \frac{1}{\frac{1}{h_{FEO}} + \frac{1}{4\tau_c D_n K} \left\{ W_c + \frac{qN_d \mu_n A (V_{SAT} + V_{BC'} - V_{BE})}{I_C} \right\}^2}
 \end{aligned}
 \tag{3.30}$$

A comparison of the calculated and observed $\beta(I_C)$ characteristics of a high-voltage triple-diffused transistor (DTS 410) serves to confirm the validity of Eqn. 3.30. The measured current gain characteristics for this device are shown in Fig. 27 where it may be seen that current gain decreases steadily as collector current is increased. The falloff of current gain in Region A (collector-base junction reverse biased) can probably be attributed to three main factors. First, the falloff of emitter efficiency at high current densities. Second, an increase of base width which occurs as a result of the decreasing reverse bias on the collector-base junction. And finally, mobile charge carriers injected from the emitter tend to reduce the width of the base side of the collector-base junction depletion layers⁽³⁶⁾. It is suggested that the falloff of gain in Region B is primarily due to the injection of

holes from the base into the collector and to a lesser extent, to the falloff of emitter efficiency.

The $\beta(I_C)$ characteristics as described by Eqn. 3.30 are plotted in region B of Fig. 27 where it is seen that the equation does predict a rapid falloff of β . The fact that calculated and observed results are in close agreement would appear to confirm that the $\beta(I_C)$ characteristics are defined primarily by the injection of holes from the base into the collector rather than by the emitter efficiency (or other effects).

Eqn. 3.30 may ultimately prove to be useful for purposes of designing high current-high voltage transistors since it represents $\beta(I_C)$ as a function of N_d , W_c , A .

It is of interest to note that Beale et al.⁽¹¹⁾ and Larin⁽³⁷⁾ have shown that the falloff of f_T at high current densities should also be described in terms of the storage of minority carriers in the collector region. The merits of this approach become apparent after a brief consideration of the various theories which others have advanced^(38,39,40):

- 1) Kirk's⁽³⁸⁾ base-width-modulation interpretation of the f_T falloff for mesa

transistors is now generally acknowledged to be incorrect (see for example^(37,39)).

- 2) The analysis given by Van der Ziel and Agouridis⁽³⁹⁾ applies only to saturated transistors operating with collector current densities somewhat greater than $qv_m N_d$ (a hot-carrier model). The f_T falloff for the devices considered in this thesis occurs at much lower current densities.
- 3) The analysis given by Whittier and Tremere⁽⁴⁰⁾ assumes a reverse-biased collector-base junction. It is evident from the analysis given in this thesis that devices may be operating in saturation ($V_{BC} > 0$) even though the terminal collector emitter voltage may be of the order of five volts or greater.

The cutoff frequency f_T does not appear as a parameter in the analysis given in this thesis. For this reason, no attempt was made to extend the analyses given by Beale et al and Larin.

3.6 The Saturation Characteristics of Small-Area VHF Transistors

The two-stage saturation curve described in this thesis is generally evident from the curve-tracer dis-

plays of large-area triple-diffused and epitaxial power transistor characteristics. Low-voltage VHF epitaxial transistors normally do not exhibit a pronounced two-stage curve since these devices have a narrow collector epitaxial layer with a relatively high impurity concentration (in comparison with large-area power transistors). However, this author has found that for some VHF transistors types (for example, 2N2222), the occasional device does exhibit a clearly-discernable two-stage curve, and concurrent with this, a very high h_{FE} . It is suggested that these devices have a base diffusion depth much less than normal (resulting in a high current gain because of the narrow base width) and therefore a relatively wide collector epitaxial layer which results in the two-stage saturation curve.

VHF devices having a well defined two-stage saturation characteristic tend to exhibit prolonged storage and voltage rise times when operating in high-speed saturating switching circuits with base drive waveforms intended primarily for average-gain devices. For this reason, it is suggested that the static $V_{CE}-I_C$ characteristics of individual devices should be examined prior to their application in such circuits.

3.7 The Degree of Saturation and the Collector Current Density Distribution

The nonuniform distribution of stored charge which exists during the ON time of a saturated epitaxial (or triple-diffused) transistor was described in qualitative terms in Chapter 2. A quantitative analysis of the charge distribution is obtained in this section by extending the analysis given in Section 3.2.

In a previous section, it was mentioned that the potential gradient along the base metallization stripes is normally small in comparison with the terminal collector-base voltage. Therefore, the collector-base potential as measured between the collector terminal and any point on the base metallization is relatively constant. An expression for this potential is obtained from Eqn. 3.15:

$$V_{CB} = -V_{BC'} - \frac{kT}{q} \ln \left\{ \frac{J_C x_c}{2qD_n p(o)} + 1 \right\} - \frac{J_C (W_c - x_c)}{q\mu_n N_d} \quad (3.31)$$

For a device operating within the second stage of the saturation characteristics, the second term in Eqn. 3.31 is small in comparison with the other terms so the equation can be simplified to:

$$V_{CB} = -V_{BC} - \frac{J_C(W_c - x_c)}{q\mu_n N_d} \quad (3.32)$$

Since the potential V_{CB} is not a function of y (see Fig. 28.a), Eqn. 3.32 may be used to describe x_c as a function of y , provided $J_C(y)$ is known and V_{BC} is assumed to be a constant.

By applying this equation at any two points along the length of a base stripe we obtain

$$\frac{J_{Ca}(W_c - x_{ca})}{q\mu_n N_d} = \frac{J_{Cb}(W_c - x_{cb})}{q\mu_n N_d},$$

and therefore

$$x_{cb} = W_c \left\{ 1 - \frac{1}{\gamma} (1 - \delta) \right\} \quad (3.33)$$

where

$$\gamma = \frac{J_{Cb}}{J_{Ca}},$$

and

$$\delta = \frac{x_{ca}}{W_c}.$$

A ratio between the stored collector charge per unit length at points a and b follows from Eqns. 3.8 and 3.33:

$$\begin{aligned}
 \frac{q_b}{q_a} &= \frac{\frac{qAx_{cb}^2}{2} \left. \frac{dp}{dx} \right|_{y=b}}{\frac{qAx_{ca}^2}{2} \left. \frac{dp}{dx} \right|_{y=a}} \\
 &= \frac{x_{cb}^2}{x_{ca}^2} \frac{J_{Cb}}{J_{Ca}} \\
 &= \left\{ \frac{1}{\delta} - \frac{1}{\gamma} \left(\frac{1}{\delta} - 1 \right) \right\}^2 \gamma \quad . \quad (3.34)
 \end{aligned}$$

The relation between this ratio and γ is plotted in Fig. 28.b with δ as a parameter. From this graph, it is clear why the region near the emitter contact has a longer storage time than the area close to the base contact. For example, for assumed value of $\delta = 0.5$ and $\gamma = 0.9$, a ratio of charge densities of 0.71 is indicated.

CHAPTER 4

COLLECTOR-EMITTER SATURATION VOLTAGE - DYNAMIC CASE

4.1 Introduction

The charge-control approach developed in the previous chapter is extended in this chapter to demonstrate that for the repetition frequencies considered in this study, the frequency dependence of the collector-emitter saturation voltage of large-area epitaxial (and triple-diffused) transistors can be related to a time-dependent conductivity modulation phenomenon in the high-resistivity collector layer. Collector-emitter saturation voltage for a device switching a square wave of collector current is described in terms of collector current amplitude, base current, time, and device parameters. Since the analysis provides close agreement with observed device behavior, the conclusion is drawn that the increase in saturation voltage due to frequency-dependent crowding mechanisms^(7,8,13) occurs at much higher frequencies than those considered in this thesis.

4.2 Collector-Charge Storage and Saturation Voltage

Triple-diffused high-voltage transistors exhibit storage and collector voltage rise times which are very

sensitive to the amount of charge stored in the collector during the ON time of a switch. Both the storage and rise time increase with the amount of stored collector charge, presumably because of the time required to remove charge from the remote regions of the wide (50 - 100 μ), lightly-doped collector region. Therefore, a demonstration of the relationship between the repetition frequency dependence of saturation voltage and collector charge storage may be conveniently given by observing the collector voltage waveforms of a high-voltage triple-diffused transistor in a simple saturating switching circuit of the form shown in Fig. 29.a. By varying the ON time of the device, one obtains output voltage waveforms similar to those shown in Fig. 29.b. It is seen that as the ON time is increased, the turn-off time also increases (both storage time and rise time are enhanced), while the collector-emitter saturation voltage steadily decreases. In other words, at this switching frequency, the charging of the collector region is the time-dependent process which defines the repetition frequency dependence of the collector-emitter saturation voltage.

4.3 Analysis

In the previous chapter it was shown that the dominant component of the static collector-emitter

saturation voltage of an epitaxial (or triple-diffused) transistor may be described by an expression of the form

$$V = - \frac{J_C (W_c - x_c)}{q \mu_n N_d} . \quad (4.1)$$

Eqn. 4.1 may be used to describe the dynamic saturation characteristics of a transistor switching a square wave collector current if x_c is represented as a function of time. A relation between x_c and time follows from an assumption that the lightly-doped collector region may be represented by a one-lump charge-control model. The equation

$$i_{BC}(t) = \frac{dQ_C}{dt} + \frac{Q_C}{\tau_c} \quad (4.2)$$

describes the flow of minority carrier charge into the collector from the base. If the assumption is made that $i_{BC}(t)$ is a step function, the solution to Eqn. 4.2 is given by

$$Q_C(t) = I_{BC} \tau_c (1 - e^{-\frac{t}{\tau_c}}) . \quad (4.3)$$

Referring to Fig. 19 and applying Eqn. 3.8 we have

$$\begin{aligned}
Q_C(t) &= I_{BC} \tau_c (1 - e^{-\frac{t}{\tau_c}}) \\
&= \frac{qAx_c(t)}{2} \frac{dp}{dx} x_c(t) \\
&= - \frac{qx_c^2(t) I_C}{4qD_n}
\end{aligned}$$

and so

$$x_c(t) = \sqrt{-\frac{4D_n \tau_c I_{BC}}{I_C} (1 - e^{-\frac{t}{\tau_c}})}. \quad (4.4)$$

Therefore, the time dependence of collector-emitter saturation voltage is given by the expression

$$\begin{aligned}
V_{SAT}(t) &= -\frac{J_C}{q\mu_n N_d} \left\{ W_c - \sqrt{-\frac{4D_n \tau_c I_{BC}}{I_C} (1 - e^{-\frac{t}{\tau_c}})} \right\} \\
&\quad + V_{BE} - V_{BC}'. \quad (4.5)
\end{aligned}$$

For the purposes of this thesis, the term $V_{BE} - V_{BC}'$ was assumed to be a constant equal to 200 millivolts.

The average value of saturation voltage during the ON time of the switch may be required for efficiency calculations. Assuming an ON time equal to one-half of the signal period, the average saturation voltage is obtained from Eqn. 4.5 as follows:

$$\begin{aligned}
\overline{V_{SAT}} &= \frac{2}{T} \int_0^{\frac{T}{2}} \left\{ -\frac{J_C W_c}{q\mu_n N_d} + \frac{J_C}{q\mu_n N_d} \sqrt{-\frac{4D_n \tau_c I_{BC}}{I_C}} [1 - e^{-\frac{t}{\tau_c}}]^{\frac{1}{2}} \right\} dt \\
&\quad + V_{BE} - V_{BC}, \\
&= -\frac{J_C W_c}{q\mu_n N_d} + \frac{2J_C}{q\mu_n N_d T} \sqrt{-\frac{4D_n \tau_c I_{BC}}{I_C}} \int_0^{\frac{T}{2}} [1 - e^{-\frac{t}{\tau_c}}]^{\frac{1}{2}} dt \\
&\quad + V_{BE} - V_{BC}.
\end{aligned}$$

Using the substitution $x = e^{-\frac{t}{\tau_c}}$, the above integral may be evaluated and $\overline{V_{SAT}}$ found to be:

$$\begin{aligned}
\overline{V_{SAT}} &= -\frac{J_C W_c}{q\mu_n N_d} - \frac{2\tau_c J_C}{q\mu_n N_d T} \sqrt{-\frac{4D_n \tau_c I_{BC}}{I_C}} \\
&\quad \left\{ 2 \sqrt{1 - e^{-\frac{T}{2\tau_c}}} - \ln \left\{ \frac{\sqrt{1 - e^{-\frac{T}{2\tau_c}}} - 1}{\sqrt{1 - e^{-\frac{T}{2\tau_c}}} + 1} \right\} \right\} \\
&\quad + V_{BE} - V_{BC}. \tag{4.6}
\end{aligned}$$

$\overline{V_{SAT}}$ may be expressed as a linear function of J_C if the substitution $\beta = I_C/I_B$ is made:

$$\begin{aligned}
 \overline{V_{SAT}} = & - \frac{J_C W_c}{q \mu_n N_d} - \frac{2 \tau_c J_C}{q \mu_n N_d T} \sqrt{4 D_n \tau_c K \left(\frac{1}{\beta} - \frac{1}{h_{FEO}} \right)} \\
 & \left\{ 2 \sqrt{1 - e^{-\frac{T}{2 \tau_c}}} + \ln \left\{ \frac{\sqrt{1 - e^{-\frac{T}{2 \tau_c}}} - 1}{\sqrt{1 - e^{-\frac{T}{2 \tau_c}}} + 1} \right\} \right\} \\
 & + V_{BE} - V_{BC} \quad (4.7)
 \end{aligned}$$

For a given ON time, collector-emitter saturation voltage decays to a value which is some fraction of $V_{SAT}(0)$. One may derive an expression for a saturation voltage cutoff frequency if this fraction is represented as a parameter σ ($0 < \sigma < 1$), and if device ON time is assumed to be one-half of the signal period. From Eqn. 4.5,

$$- \frac{\sigma J_C W_c}{q \mu_n N_d} = - \frac{J_C}{q \mu_n N_d} \left\{ W_c - \sqrt{- \frac{4 D_n \tau_c I_{BC}}{I_C} (1 - e^{-\frac{T}{2 \tau_c}})} \right\}$$

and therefore

$$W_c (1 - \sigma) = \sqrt{4 D_n \tau_c K \left(\frac{1}{\beta} - \frac{1}{h_{FEO}} \right) (1 - e^{-\frac{T}{2 \tau_c}})}.$$

Solving for the signal period T gives:

$$T = 2\tau_c \ln \left\{ \frac{1}{1 - \frac{W_c^2(1 - \sigma)^2}{4D_n \tau_c K(\frac{1}{\beta} - \frac{1}{h_{FEO}})}} \right\} \quad (4.8)$$

or, in terms of switching frequency

$$\frac{1}{f} = 4\pi\tau_c \ln \left\{ \frac{1}{1 - \frac{W_c^2(1 - \sigma)^2}{4D_n \tau_c K(\frac{1}{\beta} - \frac{1}{h_{FEO}})}} \right\} \quad (4.9)$$

In the following sections it is shown that Eqns. 4.5 and 4.7 provide close agreement between theory and practice. Therefore, for the devices and frequencies considered in this thesis, one may draw the following conclusions. First, the basic conductivity modulation model is valid. Second, the charging of the lightly-doped collector region is adequately represented by a one-lump model. Third, the current I_{BC} can, in fact, be approximated by a step function. And finally, the effects of a frequency-dependent crowding mechanism may be neglected.

4.4 Applying the Analysis

In this section, a comparison is given of the theoretical and observed dynamic saturation characteristics

of the same three devices considered in Chapter 3 (DTS 410, 2N3445, 2N3879). The switching characteristics were studied using a test circuit similar to that shown in Fig. 11. Drive waveforms to the crowbar switch and to the device-under-test were such that the transistor entered saturation after a very brief excursion into the active region of operation.

Calculated and observed curves for the triple-diffused transistor (DTS 410) switching a collector current of two amperes are given in Fig. 30 where it can be seen that the results agree within $\pm 10\%$. Since close agreement was also obtained for the static characteristics of this device, it is felt that this further confirms the validity of the model.

It is of interest to note that the point at which V_{BC} , equals zero is clearly discernable on the observed waveform shown in Fig. 30. This suggests a technique which might be used to determine the locus of the curve $V_{BC} = 0$ for devices which exhibit poorly defined static saturation characteristics as a result of current-dependent crowding phenomena (see Section 3.3.7). This would enable one to obtain an estimate of the effective collector area for a given collector current.

Curves for the epitaxial transistor (2N3445) switching five amperes collector current with a moderate base drive (240 mA) are shown in Fig. 31.a. It is seen that the slopes of the calculated and observed curves are in close agreement, but the calculated value is consistently larger. This suggests that the basic model is correct, the error being due to a poor definition of model parameters. For example, decreasing W_c from 20μ to 16μ results in a near-perfect fit.

With an increased base drive (500 mA), somewhat closer agreement between theory and practice was obtained (Fig. 31.b). It will be recalled that when calculating the static characteristics of this device, improved agreement was also obtained at the lower collector-emitter voltages.

The response of the epitaxial transistor (2N3879) switching a collector current of 4.5 amperes was also calculated. To do so, it was necessary to obtain an estimate of the effective collector area since this device experiences pronounced current-dependent crowding (see Section 3.3.7). Using the technique described in this section, an area of $.00625 \text{ cm}^2$ was calculated and the response curve shown in Fig. 32 obtained. Although the agreement between theory and practice is inferior to that obtained for the DTS 410 transistor, it does tend

to confirm the validity of the model and is, of course, sufficient for design purposes.

It is instructive to compare the dynamic saturation characteristics of the 2N3879 and the 2N3445 transistors. Both devices have similar collector current and breakdown voltage ratings (as specified by the manufacturers). In fact, judging from the information supplied by the manufacturers, the only major difference between the electrical characteristics of the two devices (aside from power rating) is that the 2N3879 has a gain-bandwidth product of 60 MHz while that of the 2N3445 is only 20 MHz. At first thought, one therefore tends to predict that the performance of the 2N3879 transistor as a high-frequency switch would necessarily be superior to that of the 2N3445. However, the fact that the 2N3879 has a much higher average saturation voltage lends emphasis to the point that the parameters τ_c and effective collector area must also be compared since these parameters, rather than f_T , dominate the response of the device in the saturated mode. In practice, the short rise, fall, and base storage times afforded by a high f_T are of little value if the efficiency of the switch is defined by saturation voltage.

4.5 Applying the Saturation Voltage Analysis to Amplifier Design

An example of the performance of the 2N3879 transistor in a current-switching amplifier circuit was given in Chapter 2. Operating with a collector current of 5 amperes and a DC input power of 150 watts, the amplifier developed an output signal power of about 120 watts. The thirty watts dissipated by the transistors could be related to the high saturation voltage which is characteristic of the 2N3879 transistor. It is instructive to attempt to predict and compare the performance of the 2N3445 transistor under similar conditions since, as mentioned in the previous section, the data sheet specifications for the two devices are similar.

To obtain a prediction of amplifier efficiency at a given frequency and current level, one should normally calculate the average saturation voltage ($\overline{V_{SAT}}$) using Eqn. 4.7. For this initial calculation, it is suggested that a value of β equal to one-half of h_{FE0} be assumed.* Also, it should be noted that since $\overline{V_{SAT}}$ is a function

* It has been found in practice that this assumption provides a realistic compromise between average saturation voltage and device turn-off time. This type of approach must be adopted until such times as a realistic storage time model is developed.

of temperature-sensitive parameters such as μ_n and D_n , $\overline{V_{SAT}}$ must be determined using an elementary iterative procedure. Initially, the device power dissipation (or junction temperature) should be estimated and a value for $\overline{V_{SAT}}$ calculated. Using this value of $\overline{V_{SAT}}$, a second approximation of the junction temperature can be determined, after which $\overline{V_{SAT}}$ should be recalculated. The process should be repeated until convergence is obtained. However, for this particular example, the characteristics of the device can be obtained from Section 4.4. From Fig. 31.a it is seen that with a collector current of 5 amperes (and a β of $\approx 0.5 h_{FEO}$) the device has a $\overline{V_{SAT}}$ of about 3 volts at a frequency of 500 kHz. For a collector supply voltage of 30 volts and a $\overline{V_{SAT}}$ of 3 volts, a collector efficiency of 90% is predicted by the equations in Table 1.

It should be noted that the peak collector-emitter voltages* will be of the order of 85 volts, which is considerably higher than the 60 volt V_{CEO} specified by the device manufacturer. However, the V_{CEO} of the transistors used by the author were measured using a curve tracer and found to be typically of the order of 120 volts.

* $V = \pi (V_{CC} - V_{SAT})$.

The completed amplifier developed an output signal power of 134 watts with a collector efficiency of 85% which is only 5% less than that predicted. Of course, one would expect the observed efficiency to be lower since the calculations did not account for power dissipation during the switching transitions. The high collector efficiency suggests that the transistors are capable of a much higher output signal power, so a second amplifier operating with a collector supply voltage of 30 volts with a collector supply current of 10 amperes was designed. For an assumed h_{FEO} of 30, a $\overline{V_{SAT}}$ of 7 volts and a collector efficiency of 77% were calculated using Eqn. 4.7 and Table 1.*

Operating with a collector supply voltage of 31.5 volts and a collector supply current of 9.5 amperes, the amplifier developed an output signal power of 235 watts with a collector efficiency of 78%. Close agreement between calculated and measured collector efficiency was obtained in spite of the fact that the transition loss was neglected in the calculation because the assump-

* In Section 4.4 it was noted that improved agreement between calculated and observed saturation voltage could be obtained by using a value for W_c 20% less than that originally determined for the 2N3445 transistor using the method described in Appendix H. This reduced value was used in all calculations in this section.

tion was made that the $\overline{V_{SAT}}$ expressed by Eqn. 4.7 existed for a length of time equal to one-half of the signal period. However, from waveforms such as those shown in Fig. 4, it can be seen that if the base drive is sufficient, the two transistors tend to share the constant supply current for brief intervals, thus resulting in instantaneous saturation voltages during the intervals which are much less than those given by Eqn. 4.6. Therefore, in the present example, the power dissipated by the transistors while in saturation is somewhat less than $I_C \overline{V_{SAT}}$ (where $\overline{V_{SAT}}$ is given by Eqn. 4.7). However, the amount of power dissipated during the switching transitions was such that close agreement between predicted and measured collector efficiency was obtained.

It is evident that the 2N3445 transistor is capable of an even higher output signal power and at much higher switching frequencies. At higher switching frequencies, the power dissipation during switching transitions would be comparable to the dissipation during saturation and therefore, the observed collector efficiency would be considerably less than that predicted using the equation in Table 1. However, no attempt was made to ascertain the ultimate capabilities of this particular device since it is felt that the two design examples have demonstrated the general utility of the analyses given in this thesis.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Summation and Conclusions

Two fundamental characteristics of epitaxial and triple-diffused power transistors which limit collector efficiency and reliability of high-frequency Class-D amplifiers have been considered in this thesis:

- a) The thermal characteristics of the transistors when used as high-current saturating switches dissipating power both while in saturation and during switching transitions (power-pulse width and repetition period both very much less than the device thermal time constant).
- b) The static and dynamic collector-emitter saturation voltage characteristics of triple-diffused and epitaxial transistors.

It has been shown that a current-crowding mechanism peculiar to high-frequency switching applications may effectively reduce the power dissipation capabilities of large-area switching transistors. The thermal characteristics of high-frequency switches were studied with the aid of two experimental techniques:

- a) Thermographic examinations (temperature-sensitive phosphors).
- b) A simulation of a large-area transistor consisting of an array of VHF devices interconnected by resistive elements corresponding to metallization resistance.

Both of these sources indicated that the crowding mechanism could be related to a nonuniform distribution of collector current density which exists during the ON time of a transistor switch, largely as a result of the device emitter metallization resistance. An analysis of collector charge storage phenomena revealed that the portion of the device having the highest collector current density during the ON time of the switch is more heavily saturated than other regions of the device. Therefore, during the turn-off transitions, this portion of the device exhibits a longer turn-off time and therefore dissipates the bulk of the power loss incurred by the device during the turn-off transition. With such crowding, very high junction temperatures may result, even though the average device dissipation may be less than the power rating assigned by the manufacturer. Since the power loss incurred by the device during the turn-off transition is dissipated in a localized area, it

was concluded that calculations of the peak junction temperature resulting from this dissipation should be conducted using a value for device thermal resistance which reflects the degree of crowding experienced by the device. The extent to which crowding is occurring in the device may be conveniently ascertained by using temperature-sensitive phosphors to determine the thermal profile on the surface of the semiconductor die.

Judging from the performance of the composite large-area transistor and from the thermographic analysis of discrete large-area devices, it was concluded that overlay devices having emitter-ballasting resistors are relatively insensitive to the crowding mechanism while on the other hand, devices having an extended comb-like structure are particularly susceptible. Further, it was concluded that shortening the emitter stripes by placing the emitter contact along the centre line of the surface of the semiconductor die, rather than along one side, results in a device which is also relatively insensitive to the crowding mechanism.

Conductivity modulation phenomena in the collector region of epitaxial and triple-diffused transistors were shown to be responsible for both the peculiar collector-emitter saturation voltage characteristics exhibited by

these devices and also for the nonuniform turn-off mechanism discussed in the preceeding paragraphs. The transport equations and charge-control concepts were utilized in a one-dimensional analysis of minority carrier injection into the lightly-doped collector region, and this resulted in an expression for the static collector-emitter saturation voltage presented in terms of collector current, base current, and device parameters.

An analytical description (rather than a numerical solution) of collector-emitter saturation voltage was found to be possible only after the following assumptions had been made:

- a) The injected carrier density at a particular point in the lightly-doped collector region was either very much greater than the equilibrium density or very much less, depending on the location of the point with respect to the junction and to the collector substrate interface. That is, a portion of the collector region was considered to be heavily conductivity modulated, while the conductivity of the remaining portion was considered to be defined by the doping density. Different equations could then be solved in the

respective regions and appropriate boundary conditions applied.

- b) The injected hole current from the base to the collector was very much less than the electron current and also, could be related to the excess base current by an experimentally determined constant factor.
- c) Emitter-edge crowding and other two-dimensional effects could be accounted for by considering the collector current density to be finite and constant (for a given I_C) within the area defined by the emitter metallization and zero elsewhere.

Since close agreement was demonstrated between calculated and observed saturation characteristics, it was concluded that in spite of the assumptions made, the analysis is sufficiently accurate for purposes of device characterization for circuit application. Also, it was concluded that an accurate, numerical solution of the fundamental semiconductor equations would have been justified only if the analysis had been extended to include a realistic description of two-dimensional effects such as emitter-edge crowding.

From the analysis it was evident that the fall-off of current gain at high collector currents experienced by transistors having a lightly-doped collector should in some instances, be interpreted in terms of the saturation model described in this thesis rather than in terms of base stretching or hot electron effects.

By extending the analysis of conductivity modulation to include time-dependent effects, an expression was produced which described the collector-emitter saturation voltage of a transistor switching a square wave of collector current as a function of collector current, base current, time, and device parameters. That is, it was shown that for the devices and frequencies considered in this thesis, the dependence of collector-emitter saturation voltage on the repetition frequency is defined by a time-dependent conductivity-modulation process rather than by a frequency-dependent edge-crowding phenomenon.

The analysis of collector-emitter saturation voltage was found to be of considerable practical importance in that it facilitates the design of current-switching Class-D circuits to the extent that it enables one to predict the collector efficiency for a particular

combination of collector current, base drive current, and switching frequency.

5.2 Future Work

Both the electrical and thermal characteristics of a transistor switch operating in the ON state have been considered in this thesis, while only the thermal aspects of the switching transitions were considered. No attempt was made to provide an analysis of the device turn-on and turn-off times. However, since device turn-off times severely limit the frequency and power capabilities of high-voltage triple-diffused transistors operating in current-switching Class-D circuits⁽⁶⁾, it is suggested that further attention be given to the analysis of this characteristic. It is felt that the analysis of collector charge storage given in this thesis could be extended to provide an analytical description of the turn-off times for both epitaxial and triple-diffused devices. Both mesa and planar structures should be considered and an attempt made to establish the extent to which collector charge storage occurs in the sidewall region of planar devices. It is commonly assumed (see for example⁽⁴⁴⁾) that the absence of an aiding field in the sidewall region prolongs the turn-off time of a planar transistor. However, the absence

of an aiding field suggests that the collector potential in the sidewall region may be approximately equal to the device terminal collector voltage. It is evident therefore, that the sidewall region of a saturated planar device may actually be reversed biased, in which case the sidewall region will have little effect on the turn-off time. It would appear then, that a switching time analysis should demonstrate that under some drive conditions, the planar structure is capable of turn-off times comparable with those of a mesa structure.

The analysis of the frequency dependence of collector emitter-saturation could be extended to include the edge-crowding effects which undoubtedly occur at very-high frequencies. An attempt might be made to define a cutoff frequency above which edge-crowding phenomena dominate the saturation characteristics.

Attempts could be made to modify the existing analysis of the variation of emitter current density along the length of an emitter stripe⁽¹⁶⁾ and across the width of the stripe⁽²⁸⁾ to include phenomena associated with high-current operation. However, it should be noted that this would be a major undertaking and it is unlikely that analytical solutions are possible. A computer simulation will be complex (and expensive) unless good initial assumptions can be made.

The analysis given in this thesis was facilitated by the assumption that the hole current from the base to collector could be related to the excess base current by an experimentally-determined constant factor. Although this simplification was found to be acceptable for purposes of device characterization for circuit applications, it places a limitation on the utility of the analysis in that it precludes a prediction of device characteristics given doping profiles geometry and other design variables. Therefore, an analysis which would describe the dependence of this factor on device design variables and terminal currents should be attempted.

Finally, by incorporating the material presented in this thesis with the results of further work, an attempt could be made to define the basic compromises necessary in the design of transistors primarily intended for high-speed, high-current switching. The switching of tens of amperes in the megahertz range might be considered as a design goal.

APPENDIX A

THE EFFECT OF EMITTER METALLIZATION RESISTANCE ON THE COLLECTOR CURRENT DENSITY DISTRIBUTION

Cave and Barnes⁽¹⁶⁾ have related the collector current density distribution along the length of an emitter stripe (comb structure) to the potential drop along the emitter metallization. They assumed current distribution to be uniform across the width W_e of the stripe, that is, they did not account for nonuniform injected carrier flow into the base (from the emitter) arising from transverse base currents. With the whole base assumed to be an equipotential $V = 0$ and the potential drops in the bulk semiconductor material assumed to be negligible, they described the current flowing out of the emitter into the base through an element "dy" at any point y as

$$I_{eb} = J_o(e^{\frac{qV}{kT}} - 1)W_e dy \quad (A.1)$$

Therefore, with a current flow I along the metallization stripe

$$\frac{dI}{dy} = -W_e J_o(e^{\frac{qV}{kT}} - 1). \quad (A.2)$$

The potential gradient across the element dy is given by

$$\frac{dV}{dy} = - \frac{I\rho}{W_e} \quad (A.3)$$

where ρ is the sheet resistance.

From Eqns. A.2 and A.3 Caves and Barnes obtained

$$\frac{d^2V}{dy^2} - J_o \rho e^{\frac{qV}{kT}} = 0 \quad (A.4)$$

where $e^{\frac{qV}{kT}} \gg 1$.

Integrating Eqn. A.4 twice they found

$$V = \frac{kT}{q} \ln \left\{ \frac{C_1^2}{\frac{2qJ_o\rho}{kT} \cos^2 \frac{C_2}{2} [y - C_2]} \right\} .$$

The constant of integration C_2 can be evaluated if the assumption is made that there is no current flow along the stripe at the extreme end $y = L_e$. Therefore

$$\left. \frac{dV}{dy} \right|_{y=L_e} = 0 \quad \text{and} \quad C_2 = -L_e,$$

and

$$V = \frac{kT}{q} \ln \left\{ \frac{C_1^2}{\frac{2qJ_0\rho}{kT} \cos^2 \frac{C_1}{2} [y - L_e]} \right\} . \quad (A.5)$$

If the base current is neglected, the current along the emitter stripe at the point $y = 0$ is given by

$$I_T = - \frac{W_e}{\rho} \frac{dV}{dy} \Big|_{y=0}$$

where

$$I_T = \frac{I_C}{\text{number of emitter stripes}} .$$

Therefore, the constant C_1 may be determined from the following equation:

$$\frac{L_e \rho I_T}{2W_e} = \frac{C_1 L_e}{2} \tan \frac{C_1 L_e}{2} . \quad (A.6)$$

By applying the result given by Eqn. A.6 in Eqn. A.5, the collector current distribution may be determined from Eqn. A.1.

This author has conducted thermographic examinations of devices and has found that the variation in current density along the emitter stripe is generally less than that predicted by Eqn. A.1. It is suggested that an analysis which included the effect of potential

drops in the semiconductor bulk material would provide closer agreement with the observed current distribution.

APPENDIX B

MATCHING ELEMENTS FOR THE COMPOSITE-ARRAY TRANSISTOR

It is essential that any variance between element temperatures be attributable to device location in the array rather than to device nonuniformities. Therefore, the switching characteristics of the individual elements must be closely matched. The switching characteristics of the individual devices may be compared using a saturating switching circuit having a slightly inductive load, such as the arrangement shown in Fig. B.1 (an inductive load serves to enhance the power dissipation during the turn-off transitions). The drive frequency to the circuit and device currents should be such that the devices are operating under conditions similar to those anticipated in the array. Transistors with similar switching characteristics tend to share equally the net collector supply current during the turn-off transitions (equal turn-off times) and so will operate with similar case temperatures. Therefore, by comparing the case temperature of a transistor-under-test with that of a reference transistor, a set of devices with similar switching characteristics may be selected. In this study, devices which exhibited case

temperatures within $\pm 1^{\circ}\text{C}$ of the reference device were considered for use in the composite transistor. Further matching of the devices was accomplished using the composite array. The locations of the devices in the array were repeatedly interchanged until it was found that the thermal profile was independent of the relative location of the individual elements.

APPENDIX C

TABLE OF DEVICE PARAMETERS

DEVICE NUMBER	STRUCTURE	MANUFACTURER'S SPECIFICATIONS				MEASURED PARAMETERS					
		P _T WATTS	I _C AMPS	V _{CEO} VOLTS	f _T MHZ	N _A x10 ¹⁴	W _C μ	τ _C μSEC	A cm ²	A _{CB2} cm ²	K
2N3265	Epitaxial Mesa	125	25	90	20	4		4.4	.0619	.271	
2N3445	Epitaxial Annular	115	7.5	60	16	7.1	20	6	.0139	.1252	0.2
2N3879	Epitaxial Mesa	35	7	75	60	5.0	20	2	.0167	.0521	0.75
DTS 410	Triple-Diffused Mesa	80	3.5	200	4	3.9	82	13	.0382	.109	0.6

APPENDIX D

THERMAL RESISTANCE MEASUREMENTS
AT HIGH COLLECTOR CURRENTS

There are two basic methods which can be employed to measure the thermal resistance of a transistor, the constant junction temperature method and the constant reference temperature method⁽¹⁴⁾. The constant junction temperature method may be described as follows. A temperature-sensitive device parameter is monitored while the transistor is dissipating P_1 watts with the case temperature maintained at T_1 degrees. The device case temperature is then lowered (or increased) by a known amount and the device dissipation increased (or decreased) until the temperature-sensitive parameter indicates a junction temperature equal to the initial value. The thermal resistance can then be calculated using

$$\theta = \frac{T_2 - T_1}{P_2 - P_1}$$

where T_2 and T_1 represent the two case temperatures and P_2 and P_1 the power dissipated at these temperatures.

With the second technique, the constant reference temperature method, the temperature-sensitive parameter is measured as a function of temperature while the device is dissipating very little power, and a functional relationship is defined. Then, while maintaining a constant case temperature, the device is operated with a power dissipation P_1 and the junction temperature noted and then with a dissipation P_2 and junction temperature noted again. Thermal resistance can then be determined using the relationship

$$\theta = \frac{T_2 - T_1}{P_2 - P_1}$$

where T_2 and T_1 represent the junction temperatures corresponding to the device dissipations P_2 and P_1 .

The second of these methods is considered by this author to be the more practical since it is clearly more convenient to maintain the case temperature constant (using for example, an ice-water bath) while varying the junction temperature, then varying the case temperature while maintaining a fixed junction temperature.

The forward-biased voltage of either of the transistor junctions (measured while the device is conducting a very low current) and the current gain h_{FE}

(measured when the device is dissipating P_1 (or P_2) watts) are two temperature-sensitive parameters which are commonly used to monitor the junction temperature of silicon transistors. It is suggested that the junction voltage rather than current gain be monitored when measuring thermal resistance at high current levels because of the following reasons. When applying the constant reference temperature technique, the changing of the device dissipation from P_1 to P_2 watts is effected by altering the collector-base bias voltage, while the collector current is maintained constant. In order to limit the device dissipation to less than P_T , the measurements must be conducted at a low collector-emitter voltage. Under such conditions the device may be operating in saturation and h_{FE} will then be a function of collector-emitter voltage as well as temperature. Also, the temperature-sensitive parameter should be a sensitive function of the peak junction temperature attained while the device is dissipating P_1 (or P_2) watts. The current gain h_{FE} does not provide a direct indication of the maximum junction temperature but rather represents some average temperature. On the other hand, the forward-biased voltage of a pn junction has a negative temperature coefficient and therefore, the observed junction voltage is defined by the region of the junction

having the highest temperature. This is true, of course, only if ohmic drops can be neglected and therefore, the measurement should be made at low currents, say less than ten milliamps for the devices considered in this study. The use of the forward-biased junction voltage offers the added advantage in that the temperature coefficient of pn junction can be easily determined, either by measurement or from the literature^(42,43). For the purposes of this study, the coefficient was experimentally determined to be 1.8 millivolts per degree centigrade.

The arrangement shown in Fig. D.1 was used to determine the thermal resistance of the devices considered in this thesis (constant reference temperature). The switches S_1 , S_2 , and S_3 are normally in the positions shown and so the device power dissipation (P_1 or P_2) is given by

$$P = I_H V_{EB} + I_H V_{CB}.$$

Periodically, the switch positions are reversed for an interval which is much shorter than the device thermal time constant, and the base-emitter voltage is monitored while the junction is passing the low current I_L . It should be noted that the switch S_3 is closed when the

base-emitter voltage is monitored, and therefore the observed voltage is not a function of the voltage V_{CB} .

If thermal resistance measurements are to be made at near-rated current levels, the switching functions in Fig. D.1 must be performed by transistors, since relays (the devices most commonly used) are incapable of rapid switching of such high currents. A transistorized test circuit is shown in Fig. D.2. The amplitude of the 100 Hz drive signal is such that the switch positions are reversed for 5 μ sec intervals, during which the base-emitter voltage is measured.

The thermal resistance of each of the devices considered in this study was measured as a function of collector current. Device dissipation P_1 was maintained constant as the collector current was varied. The results for a typical device are shown in Fig. D.3. Beyond a certain collector current, thermal resistance increases, presumably because of current crowding along the length of the emitter stripes (Cave and Barnes⁽¹⁶⁾) and across the emitter stripes (Hauser⁽²⁸⁾). At lower current levels, it is seen that an inverse relation exists between thermal resistance and current level (see also Fig. 13.e). This can probably be explained in terms of the Theory of Lateral Thermal Instability (see

Section 2.4.2a). It is therefore evident that for application in Eqn. 2.1, the θ measurement should be made with the collector-emitter voltage approximately equal to $\overline{V_{SAT}}$ and I_H equal to the amplitude of the current to be switched.

With the exception of the high-voltage triple-diffused transistor DTS 410, the thermal resistance values which were measured at near-rated currents were equal to or less than those quoted by the device manufacturers. The minimum value of thermal resistance measured for the DTS 410 transistor was 0.9°C/watt while the manufacturer quoted 0.5°C/watt as a typical value. However, the transistor is capable of dissipating the rated P_T (80 watts) since it has a large emitter area ($A = 0.0382\text{ cm}^2$) and is mounted in a case generally used for transistors with power ratings of 100 watts or greater (TO-3).

APPENDIX E

COLLECTOR LIFETIME τ_c

Several authors have described techniques which may be used to determine the effective collector lifetime⁽⁴⁴⁻⁴⁶⁾. Larin⁽⁴⁶⁾ outlined a method which utilized the arrangement shown in Fig. E.1. With the switch S_1 closed, the collector-base junction of the device-under-test is forward biased, and a distribution of excess carriers is established in the lightly-doped collector region. By periodically opening the switch S_1 , the flow of current is interrupted and the resultant open-circuit voltage may be taken as a direct indication of the carrier concentration at the junction since

$$p(x = 0, t) = p_o e^{\frac{qV_{BC}(t)}{kT}} \quad (E.1)$$

According to Larin, if $W_c \gg L_p$, the time dependence of the carrier concentration at the junction may be described by

$$p(x = 0, t) = p(0, 0) e^{-\frac{2t}{\tau_c}} \quad (E.2)$$

where $p(0, 0)$ represents the carrier concentration on the collector side of the junction when the switch is first opened. Combining Eqns. E.1 and E.2 gives

$$\begin{aligned}
 p_o e^{\frac{qV_{BC}(t)}{kT}} &= p(0,0) e^{-\frac{2t}{\tau_c}} \\
 &= p_o e^{\frac{qV_{BC}(0)}{kT}} e^{-\frac{2t}{\tau_c}} \\
 &= p_o e^{\frac{q}{kT} \{V_{BC}(0) - \frac{kT}{q} \frac{2t}{\tau_c}\}}
 \end{aligned}$$

Therefore,

$$V_{BC}(t) = V_{BC}(0) - 2 \frac{kT}{q} \frac{t}{\tau_c} \quad (E.3)$$

from which it can be seen that the open-circuit voltage decays linearly with time and with a slope of approximately 50 millivolts per lifetime ($T = 25^\circ\text{C}$). The slope can be measured from an oscilloscope trace of the open-circuit voltage (see Fig. E.2).

Larin suggested that the open-circuit voltage for an epitaxial or triple-diffused transistor ($L_p > W_c$) was given by

$$V_{BC}(t) = V_{BC}(0) - 1.5 \frac{kT}{q} \frac{t}{\tau_{\text{eff}}} \quad (E.4)$$

where the factor of 1.5 could be related to the linear excess carrier distribution in the collector region.

He used the symbol τ_{eff} to indicate that the decay of

the open-circuit voltage is dependent on the lifetime in the collector substrate as well as on the epitaxial layer lifetime. However, τ_c was defined in this thesis as the carrier lifetime in the N_d layer and will therefore be somewhat greater than τ_{eff} . For this reason, the value of τ_c given by Eqn. E.3 was used in the calculations given in this thesis. A second measurement technique was used to confirm the validity of the result given by Eqn. E.3. According to Hoffmann and Schuster⁽⁴⁷⁾, if the excess charge is removed from an initially forward-biased diode by a large reverse current in an interval which is much less than the carrier lifetime, then the following holds true:

$$\tau = \frac{\text{stored charge}}{\text{diode forward bias current}} .$$

The stored charge may be determined from an oscilloscope trace of the diode reverse current. It was found that values of τ_c measured using this technique agreed within $\pm 15\%$ of those given by Eqn. E.3.

It should be noted that a poorly-defined τ_c does not necessarily result in poor agreement between calculated and observed saturation voltage characteristics. The reason for this is clear from a consideration of the procedure described in Section 3.3.2 for determining the

factor K which appears in the expression for I_{BC} (Eqn. 3.17). Applying this technique gives a value for K (and therefore I_{BC}) which is inversely proportional to τ_c . Therefore, the value of x_c given by Eqn. 3.11 is insensitive to errors in τ_c since τ_c is effectively cancelled.

The saturation voltage analysis given in this thesis assumes τ_c to be independent of the density of injected carriers in the collector region. Since it is known that τ_c is, in fact, dependent on the carrier concentration (see for example⁽³¹⁾), it is suggested that improved agreement between calculated and observed saturation characteristics will be obtained if the τ_c measurement is made with a value of $p(0,0)$ of the order of that anticipated in a saturated transistor.

Evans⁽³²⁾ found that the temperature dependence of the minority carrier lifetime in the base region of alloy PNP silicon transistors could be described by an expression of the form

$$\tau \propto e^{-\frac{0.055}{kT}} \quad (E.5)$$

Measurements conducted by this author indicated that Eqn. E.5 also correctly describes the temperature dependence of τ_c for epitaxial and triple-diffused silicon NPN transistors.

APPENDIX F

THE EFFECTS OF DISTRIBUTED BASE POTENTIAL
ON THE EMITTER CURRENT DENSITY DISTRIBUTION

Hauser⁽²⁸⁾ analyzed the effect of transverse base currents on the variation of emitter current density across the width of an emitter stripe of a planar transistor structure. The essential points of his analysis are outlined in this appendix.

The following assumptions are basic to Hauser's analysis:

- 1) The junctions are assumed parallel and planar.
- 2) Potential drops in the emitter region are negligible.
- 3) Surface recombination is negligible.
- 4) The conductivity of the base region is sufficiently high that conductivity modulation effects may be neglected.
- 5) α is assumed to be constant across the base region.
- 6) The conductivity of the extrinsic base region is assumed to be infinite.

Hauser considered the basic planar transistor structure shown in Fig. F.1.a. Because of assumption 6, the device may also be represented as shown in Fig. F.1.b.

The emitter current density is related to the emitter-base voltage $V(z)$ by the equation

$$J_E(z) = J_0 \left(e^{\frac{qV(z)}{kT}} - 1 \right). \quad (F.1)$$

With a transverse base current density $J_B(z)$ the emitter-base potential in the region $0 < z < \frac{W_e}{2}$ is given by

$$V(z) = V\left(\frac{W_e}{2}\right) - \int_{\frac{W_e}{2}}^z J_B(z) \rho_B dz \quad (F.2)$$

where, for a graded-base device, ρ_B is the reciprocal of the average conductivity in the base region⁽⁴⁸⁾.

The base current is given by

$$I_B(z) = 2W_b L_e J_B(z) = 2L_e \int_0^{\frac{W_e}{2}} (1-\alpha) J_E(z) dz. \quad (F.3)$$

Thus in the region $0 < z < \frac{W_e}{2}$,

$$\frac{dJ_B(z)}{dz} = \frac{1}{W_b} (1 - \alpha) J_E(z). \quad (F.4)$$

Applying Eqns. F.1 and F.2 in F.4 gives

$$\frac{dJ_B(z)}{dz} = \frac{J_0}{W_b} (1 - \alpha) \left\{ e^{\frac{q}{kT} \left[V\left(\frac{W_e}{2}\right) - \int_{\frac{W_e}{2}}^z \rho_B J_B(z) dz \right]} - 1 \right\}. \quad (F.5)$$

Differentiating Eqn. F.5 with respect to z gives

$$\frac{d^2 J_B(z)}{dz^2} = \frac{q J_0 \rho_B (1 - \alpha) J_B(z)}{W_b kT} e^{\frac{q}{kT} \left[V\left(\frac{W_e}{2}\right) - \int_{\frac{W_e}{2}}^z \rho_B J_B(z) dz \right]}. \quad (F.6)$$

With the aid of Eqn. F.5 the exponential term can be eliminated from Eqn. F.6:

$$\frac{d^2 J_B(z)}{dz^2} = \frac{q \rho_B J_B(z)}{kT} \left\{ \frac{dJ_B(z)}{dz} + \frac{J_0 (1 - \alpha)}{W_b} \right\} = 0. \quad (F.7)$$

If we assume $J_E(z) \gg J_0$, then from Eqn. F.4

$$\frac{dJ_B(z)}{dz} \gg \frac{1}{W_b} J_0 (1 - \alpha)$$

and so Eqn. F.7 reduces to

$$\frac{d^2 J_B(z)}{dz^2} + \frac{q\rho_B J_B(z)}{kT} \frac{dJ_B(z)}{dz} = 0 \quad (F.8)$$

The solution of Eqn. F.8 is given by

$$J_B(z) = C_1 \tan \left\{ \frac{C_1 q \rho_B C_2}{2kT} \left[1 - \frac{z}{C_2} \right] \right\}.$$

The constants of integration may be evaluated from the boundary conditions. For the structure shown in Fig.

F.1.b

$$J_B\left(\frac{W_e}{2}\right) = -J_B\left(-\frac{W_e}{2}\right)$$

which gives $C_2 = 0$, and therefore

$$J_B(z) = C_1 \tan \left\{ -\frac{C_1 q \rho_B z}{2kT} \right\} \quad (F.9)$$

Also, from

$$2W_b L_e J_B\left(\frac{W_e}{2}\right) = W_e L_e (1 - \alpha) \overline{J_E(z)}$$

we have

$$J_B\left(\frac{W_e}{2}\right) = \overline{J_E(z)} (1 - \alpha) \frac{W_e}{2W_b}$$

where $\overline{J_E(z)}$ denotes the average emitter current density over the extent of the emitter stripe.

Therefore, the constant C_1 may be determined from*

$$-\frac{\overline{J_E(z)}(1 - \alpha)W_e^2\rho_B q}{8 W_b kT} = \psi \tan \psi \quad (F.10)$$

$$\text{where } \psi = -\frac{qC_1\rho_B W_e}{4kT}.$$

Substituting Eqn. F.9 into Eqn. F.2 and performing the integration, one obtains

$$\begin{aligned} V(z) &= V\left(\frac{W_e}{2}\right) - \int_{\frac{W_e}{2}}^z \frac{4kT\psi\rho_B}{q\rho_B W_e} \left\{ \tan \frac{2\psi z}{W_e} \right\} dz \\ &= V\left(\frac{W_e}{2}\right) - \frac{2kT}{q} \ln \left\{ \frac{\cos \frac{2\psi z}{W_e}}{\cos \psi} \right\}. \end{aligned} \quad (F.11)$$

$J_E(z)$ is then obtained by substituting Eqn. F.11 into Eqn. F.1, which gives

* Eqn. F.10 corresponds to Eqn. 30 given by Hauser:

$$\frac{\overline{J_E(z)}W_e^2\rho_B q}{4 W_b^2 kT} = \psi \tan \psi \quad (30)$$

It would appear that Eqn. 30 contains a typographical error.

$$\begin{aligned}
J_E(z) &= J_o e^{\frac{q}{kT} \left\{ V\left(\frac{W_e}{2}\right) - \frac{2kT}{q} \ln \left\{ \frac{\cos \frac{2\psi z}{W_e}}{\cos \psi} \right\} \right\}} \\
&= J_E\left(\frac{W_e}{2}\right) \left\{ \frac{\cos \psi}{\cos \frac{2\psi z}{W_e}} \right\} \quad (F.12)
\end{aligned}$$

where the -1 term in Eqn. F.1 has been neglected.

A relationship between the average emitter current density $\overline{J_E(z)}$ and the maximum emitter current density $J_E\left(\frac{W_e}{2}\right)$ can be obtained as follows:

$$\overline{J_E(z)} = \frac{2}{W_e} \int_0^{\frac{W_e}{2}} J_E(z) dz.$$

Thus,

$$\overline{J_E(z)} = J_E\left(\frac{W_e}{2}\right) \frac{\sin \psi \cos \psi}{\psi} \quad (F.13)$$

Hauser applied the analysis to a device with a $\overline{J_E(z)}$ of 150 Amp/cm² and calculated a ratio $J_E\left(\frac{W_e}{2}\right)/J_E(o)$ of approximately 2.5. However, because of assumptions 4 and 5, the validity of the model at such current densities must be questioned. These two assumptions concern effects which tend to compensate each other, but the extent to which compensation occurs is unknown. For this reason, the model was not incorporated into the analysis given in this thesis.

APPENDIX G

COLLECTOR DOPING DENSITY N_d

Hilibrand and Gold⁽⁴⁹⁾ and Moll⁽⁵⁰⁾ have presented analyses of the capacitance-voltage characteristics of pn junctions with arbitrary impurity distributions which may be used to determine the collector impurity density N_d . Moll's treatment of the topic is outlined in this appendix.

Assume an increment of voltage δV applied to reverse-biased pn junction. With an increment of voltage δV , the field increment will be $\delta V/W$, where W is the width of the depletion region. The increment of charge is given by

$$\delta Q = \epsilon \delta E = \frac{\delta V \epsilon}{W}$$

and therefore

$$C = \frac{\delta Q}{\delta V} = \frac{\epsilon A}{W} \quad (G.1)$$

where A is the area of the junction (assumed to be constant). The rate of change of depletion capacitance with voltage is then given by

$$\frac{dC}{dV} = - \frac{\epsilon A}{W^2} \frac{dW}{dV} .$$

Again considering an increment of applied voltage δV , the factor $\frac{dW}{dV}$ is obtained as follows. For a net donor density of N_d on the n side of the depletion layer and a net acceptor density N_A on the p side, the increment of width δW is

$$\begin{aligned}\delta W &= \frac{\delta Q}{qN_d} + \frac{\delta Q}{qN_o} \\ &= \frac{\epsilon}{qW} \left(\frac{1}{N_d} + \frac{1}{N_a} \right) \delta V.\end{aligned}$$

Therefore,

$$\begin{aligned}\frac{dC}{dV} &= - \frac{\epsilon^2 A}{qW^3} \left(\frac{1}{N_d} + \frac{1}{N_a} \right) \\ &= - \frac{C^3}{q\epsilon A^2} \left(\frac{1}{N_d} + \frac{1}{N_a} \right)\end{aligned}$$

and

$$A^2 \frac{d}{dV} \left(\frac{1}{C^2} \right) = \frac{2\epsilon}{q} \left(\frac{1}{N_d} + \frac{1}{N_a} \right). \quad (G.2)$$

If the impurity concentration is much higher on the p side of the junction than on the n side, the penetration of the depletion layer into the n side will be very much larger than that into the p side and so Eqn. G.2 may be simplified to

$$A^2 \frac{d}{dV} \left(\frac{1}{C^2} \right) = \frac{2}{q\epsilon N_d}$$

and therefore

$$N_d = \frac{2}{q\epsilon A^2 \frac{d}{dV} \left(\frac{1}{C^2} \right)} . \quad (G.3)$$

A typical doping profile of an epitaxial power transistor is shown in Fig. G.1. The average impurity density in the base region is very much higher than that in the N_d collector region and therefore, if the reverse bias is sufficient, the error resulting from the one-sided junction approximation will be negligible. For the devices considered in this study, the CV measurements were made at reverse bias voltage levels which produced depletion layer widths of the order of $0.5 W_c$. It is believed that under such conditions, the one-side junction approximation error is small and also, the value of N_d so obtained represents a realistic average of the doping density in the high-resistivity collector region (it will be recalled that the analyses given in Chapters 3 and 4 assumed N_d to be a constant).

A low frequency RLC bridge (GR 1650-A) was used to obtain collector-base junction capacitance measurements at two bias voltages, V and $V + 5.0$ volts. The

capacitance-voltage curve in this range was approximated by a straight line segment and a quantity corresponding to the differential term in Eqn. G.3 calculated. The area of the collector-base junction was determined by optical means.

The collector-base junction of a mesa transistor is confined to a plane parallel with the surface of the semiconductor die and therefore, the capacitance-voltage characteristics of the collector-base junction can be described by a one-dimensional analysis such as that given by Moll. It is suggested that the error which results from an application of the one-dimensional analysis to planar or annular transistor structures will be small, provided the area of the portion of the collector-base junction which is parallel with the surface of the die is sufficiently large compared with the area of the base sidewalls to account for the high base doping (and collector doping in the case of annular devices) in the sidewall region. Of the transistors considered in this study, the only device which was not of the mesa variety was the 2N3445. However, since this is a large-area transistor and since an analytical treatment of the effect of sidewalls does not appear to be available in the literature, it was treated as a mesa device. The doping

density which was calculated using this procedure was of the order of that for electrically similar mesa transistors and so it was concluded that the contributing of the sidewall capacitance was, in fact, negligible.

APPENDIX H

MEASUREMENT OF COLLECTOR WIDTH W_c

The techniques described in Appendix G may be used to determine the width W_c of the high-resistivity collector region, provided avalanche breakdown does not occur for depletion layer widths less than W_c . The procedure consists of applying Eqn. G.3 to determine N_d at the collector edge of the depletion layer, and then solving for the width of the depletion region using Eqn. G.1. However, this technique was not applied in this study since very high reverse-bias voltages (greater than 100 volts) are necessary to deplete the N_d region of most power transistors. Measurements at such high voltages are not only inconvenient, but also, device failure may occur if the junction is inadvertently operated in the avalanche mode.

A second technique for determining W_c becomes apparent from a consideration of the collector-emitter saturation voltage model developed in this thesis. According to the model, the second stage of the saturation characteristic curve terminates at the point where $V_{BC} = 0$ (see Fig. 22). The collector-emitter voltage

along the locus of the curve $V_{BC} = 0$ is given by Eqn. 3.15 as

$$V_{CE} = - \frac{J_C W_c}{q \mu_n N_d} + V_{BE}. \quad (H.1)$$

For most devices, the $V_{BC} = 0$ curve at low current densities ($J_C < 50$ Amps/cm²) may be approximated by a straight line. Therefore, W_c may be determined from the slope of this curve, provided N_d , the effective collector area A , and V_{BE} are known quantities (normally, V_{BE} may be assumed to be a constant). This technique was adopted in this study, and found to be satisfactory. However, an alternative means of determining W_c is at times desirable, since the value given by Eqn. H.1 is subject to the errors in N_d and A .

A third method for determining W_c , which is applicable to mesa-epitaxial transistors, follows from Phillips⁽⁵¹⁾ analysis of the dependence of V_{CBO} on the factors W_c and N_d . If the base and the collector substrate doping densities can be considered to be very much greater than the doping density N_d , the collector field distribution for a reverse-biased collector-base junction will resemble that shown in Fig. H.1, where x_{mB} denotes the depletion layer width for the avalanche

breakdown voltage corresponding to the epitaxial layer resistivity. A linear variation of the field strength $E(x)$ in the collector region is shown since N_d was assumed to be constant in the epitaxial layer. The collector-base terminal voltage at breakdown (V_{CBO}) is equal to the shaded area beneath the field curve. By taking the ratio of this area to the area of the triangle (E_{mB} , 0, x_{mB}), one obtains the ratio of the breakdown voltage V_{CBO} to the epitaxial layer resistivity breakdown voltage V_B :

$$\frac{\frac{x_{mB}^2 N_d}{2} - \frac{(x_{mB} - W_c)^2 N_d}{2}}{\frac{x_{mB}^2 N_d}{2}} = \frac{V_{CBO}}{V_B}$$

and therefore,

$$W_c = x_{mB} - x_{mB} \sqrt{1 - \frac{V_{CBO}}{V_B}} \quad (H.2)$$

where

V_B = the breakdown voltage of one-sided pn junction with a doping density N_d .

x_{mB} = depletion layer width at V_B (both x_{mB} and V_B are generally available in textbooks such as Phillips⁽⁵¹⁾).

V_{CBO} = measured collector-base junction breakdown voltage.

Applying this technique to determine W_c is somewhat inconvenient because of the high voltages required (V_{CBO} typically greater than 300 volts). Moreover, it was found that with the devices considered in this study, the collector-base junctions generally exhibited a "soft" breakdown characteristic. That is, small increments of applied voltage were not accompanied by abrupt increases in avalanche current. Under such conditions, it is difficult to specify with any degree of certainty, the breakdown voltage V_{CBO} . However, for purposes of this study, V_{CBO} was arbitrarily defined as that voltage which resulted in a junction power dissipation of two watts. By applying this value of V_{CBO} in Eqn. H.2, a value for W_c was predicted which generally agreed well with that given by Eqn. H.1.

Fig. 1 Voltage-switching amplifier (low-frequency waveforms).

Fig. 3 High-frequency voltage-switching amplifier waveforms (V_{CE} : 10 volts/cm, I_C : 1 Amp/cm, t : 0.5 usec/cm).

Fig. 4 High-frequency current-switching amplifier waveforms (V_{CE} : 10 volts/cm, I_C : 1 Amp/cm, t : 0.5 usec/cm).

(a) Alloy 2N575

(b) Epitaxial 2N3445

(c) Triple-diffused DTS410

Fig. 5 Typical V_{CE} - I_C characteristics
(V_{CE} : 0.5 volts/cm, I_C : 200 mA/cm,
 I_B : 5 mA/step).

Fig. 6 Large-area epitaxial transistor (2N3265) with burned spot adjacent to emitter contact (x 12).

Fig. 7 The successive reduction of conducting transistor area during a turn-off transition.

Fig. 8 A two-element representation of a large-area transistor having a finite metallization resistance.

Fig. 9 Load curves for the elements Q_A and Q_B (Fig. 8) during a turn-off transition.

Fig. 10 Composite model of large-area switching transistor.

Fig. 11 Device test arrangement.

Fig. 12 Performance of the composite-array transistor ($f = 250 \text{ kHz}$, $I_c = 4 \text{ Amps}$);
 a) Temperature distribution with contacts as shown in Fig. 10,
 b) Effect of contact arrangement, R_{E1} , and R_{E2} ($t_D > 0$).

Fig. 13.a Phosphor-coated 2N3265 transistor fluorescing at room temperature.

Fig. 13.b Thermal profile for the 2N3265 transistor biased at an operating point of 18 amperes, 3 volts.

Fig. 13.c Thermal profile for the 2N3265 transistor biased at an operating point of 9 amperes, 6 volts.

Fig. 13.d Thermal profile for the 2N3265 transistor biased at an operating point of 4.5 amperes, 12 volts.

Fig. 13.e Thermal resistance of the 2N3265 transistor.

Fig. 14.a Thermal profile for the 2N3265 transistor ($f = 250$ KHz, $I_C = 18$ amperes, $V_{SAT} = 3.5$ volts, $V_p = 0$).

Fig. 14.b Thermal profile for the 2N3265 transistor ($f = 250$ KHz, $I_C = 18$ amperes, $V_{SAT} = 3.5$ volts, $V_p = 45$ volts).

Fig. 14.c Thermal profile for the 2N3265 transistor ($f=250$ KHz, $I_C=18$ amperes, $\bar{V}_{SAT}=6$ volts, $V_p=0$).

Fig. 15.a Thermal profile for the 2N3265 transistor ($f=500$ KHz, $I_C=18$ amperes, $V_p=45$ volts, $P_{SAT}=P_{TOFF}=32.4$ watts).

Fig. 15.b Thermal profile for the 2N3265 transistor ($f=500$ KHz, $I_C=18$ amperes, $V_p=55$ volts, $P_{SAT}=32.4$ watts, $P_{TOFF}=39.4$ watts).

Fig. 15.c Thermal profile for the 2N3265 transistor ($f = 500$ KHz, $I_C = 9$ amperes, $V_p = 90$ volts).

Fig. 16.a 2N3445 transistor (x 12).

Fig. 16.b Thermal profile for the 2N3445 transistor ($f = 500$ KHz, $I_C = 10$ amperes, $V_{SAT} = 8$ volts, $V_p = 100$ volts).

Fig. 17.a 2N3879 transistor (x 12).

Fig. 17.b Thermal profile for the 2N3879 transistor
($f = 500$ KHz, $I_C = 6.5$ amperes, $P_{SAT} = 12.5$ watts, $P_{TOFF} = 15.5$ watts, $V_p = 50$ volts).

Fig. 17.c Thermal profile for the 2N3879 transistor biased at an operating point of 3 amperes, 10 volts.

(a)

(b)

Fig. 18 Thermal profiles for the 2N3879 transistor operating in 150 watt, 500 KHz, Class-D amplifier circuits: a) voltage-switching circuit, b) current-switching circuit.

Fig. 19 Collector doping profile and net minority carrier density distribution in saturated NPN transistor.

Fig. 20 Suggested procedure for calculating V_{SAT} .

Fig. 21 Collector current density distribution in large-area transistors.

Fig. 22 V_{CE} - I_C characteristics of the high-voltage triple-diffused transistor DTS410 (V_{CE} : 1.0 volts/cm, I_C : 0.2 Amp/cm, I_B : 5 mA/step, $T \approx 35^\circ\text{C}$).

Fig. 23 Comparison of calculated and observed saturation curves of the DTS 410 transistor.

Fig. 24.a 2N3445 transistor V_{CE} - I_C
 characteristics (V_{CE} : 0.5volt/cm,
 I_C : 0.2 Amp/cm, I_B : 5 mA/step,
 $T \approx 35^\circ\text{C}$).

Fig. 24.b Comparison of the calculated and observed saturation characteristics of the 2N3445 transistor.

DTS410

2N3445

Fig. 25.a A comparison of the DTS410 transistor metallization with that of the 2N3445 transistor.

Fig. 25.b Thermal profile for the 2N3445 transistor biased at an operating point of 7 amperes, 7 volts.

Fig. 26.a $V_{CE} - I_g$ characteristics of the epitaxial transistor 2N3679 ($V_{CE} : 0.5$ volts/cm, $I_g : 0.2$ Amp/cm, $I_g : 5$ mA/step, $T \approx 35^\circ$).

Fig. 26.b A comparison of the calculated and observed saturation characteristics of the 2N3879 transistor.

Fig. 27 Current gain falloff at high collector currents.

Fig. 28 The degree of saturation as a function of the collector current density distribution; a) coordinate system, b) Eqn. 3.34.

(a)

(b)

Fig. 29 Illustrating the relationship between the frequency dependence of saturation voltage and collector charge storage: a) test circuit, b) resultant collector voltage waveforms ($V_{CE}: 10 \text{ volts/cm}$, $t: 0.2 \text{ usec/cm}$).

Fig. 30 Time dependence of saturation voltage for the DTS 410 transistor.

Fig. 31 The time dependence of saturation voltage for the 2N3445 transistor;
 a) medium base drive
 b) heavy base drive.

Fig. 32 Time dependence of saturation voltage for the 2N3879 transistor.

Fig. B.1 Test circuit for comparing switching characteristics.

Fig. D.1 Basic thermal resistance test arrangement.

Fig. D.2 Transistorized thermal resistance test circuit.

Fig. D.3 Thermal resistance as a function of collector current.

Fig. E.1 Circuit for measuring τ_c .

Fig. E.2 Base-collector open-circuit voltage decay.

Fig. F.1 (a) Planar transistor structure.
 (b) Idealized transistor structure.

Fig. G.1 A possible impurity profile for an epitaxial transistor.

Fig. H.1 Electric field distribution in collector region of epitaxial transistor at avalanche breakdown.

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