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**IMPLEMENTATION OF A TIMING RECOVERY CIRCUIT
FOR A MOBILE RADIO RECEIVER**

by

Tom M. Luk, B.A.Sc.

This thesis is submitted to the Faculty of Graduate Studies and
Research in partial fulfillment of the requirements for the
degree of

Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada
May, 1989

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ISBN 0-315-51182-6

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The undersigned recommend to the Faculty of Graduate Studies and Research the acceptance of the thesis:

**"IMPLEMENTATION OF A TIMING RECOVERY CIRCUIT
FOR A MOBILE RADIO RECEIVER"**

submitted by Tom M. Luk in partial fulfillment of the requirements
for the degree of Master of Engineering.

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Abstract

The purpose of this thesis is to design and implement the analog/digital baseband demodulator chips for a mobile 16 kb/s digital FM radio receiver within a university I.C. design environment. The analog circuits perform signal filtering, amplitude limiting, and integrate-and-dump filtering. The digital portion performs the task of clock-timing recovery from the received data. The clock-timing recovery circuit is based on a digital phase-locked loop which employs a Random Walk Filter. Due to the complexity of the system involved in this chip implementation, this thesis focuses on the implementation of the clock-timing recovery chip of the baseband demodulator; the analog circuits are designed by a fellow graduate student. It is also the goal of this thesis to present an I.C. design technique and methodology which is suitable to the resources available at Carleton University. The clock-timing recovery chips are designed using a 3-micron double-metal CMOS technology and each contains 1500 transistors. The chip area is 4.0 mm x 1.1 mm. The fabricated chips are tested to be fully functional. The measured results obtained from the clock-timing recovery chips clearly indicate the success of chip design following the proposed methodology, demonstrating its ability to generate "Work The First Time" designs.

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Glossary of Symbols and Abbreviations

APAR: auto-place-and-route

ASIC: application specific integrated circuit

BER: bit error rate

BPF: band-passed filter

CAD: computer-aided design

CIF: CALTECH intermediate form

CMC: Canadian Microelectronics Corporation

CMOS: complementary metal oxide silicon

DCO: digital-controlled oscillator

DPLL: digital phase-locked loop

GMSK: gaussian shifted keying

FM: frequency modulation

IC: integrated circuit

IF: intermodulation frequency

LSI: large scale integration

MRT: minimum resolution time

NRZ: no-return to zero

PD: phase detector

PLL: phase-locked loop

RWF: random walk filter

SNR: signal to noise ratio

TFM: Tamed frequency modulation

TRIO: Telecommunication Research Institute of Ontario

UHF: ultra high frequency

VHF: very high frequency

VLSI: very large scale integration

Chapter 1

INTRODUCTION

1.1 Thesis Motivation and Objectives

The transmission of data over VHF/UHF mobile channels has become increasingly important over the last few years. Mobile radio users such as couriers, police, taxis and emergency vehicles are now using data communication technology to access data bases and receive instructions in written forms. The net result is the growing demand for high-speed digital transmission to facilitate speech communication and high-speed data transmission. Mobile digital speech communication has motivated the development of bandwidth efficient modulation and speech coding techniques.

Narrow-band digital FM transmission techniques, such as tamed FM (TFM) [1], [2] and Gaussian baseband filtered minimum shift keying (GMSK) [3], have been reported to be applicable to mobile radio transmission [4], [5]. This type of digital FM has the following features:

- (i) constant envelope
- (ii) narrow-band spectrum
- (iii) good bit error rate (BER) vs. signal-to-noise ratio performance.

In recent years, there has been a growing interest in implementing digital mobile radio systems onto silicon to facilitate low power consumption and compactness, [6], [7], [8], [9]. Furthermore, developments in circuit design over the last few years have laid the foundation for realizing communication systems which require analog and digital functions on a single integrated circuit [10], [11]. Researchers at the Systems and Computer Engineering Department of Carleton University have involved in the development of high-speed mobile digital speech communication systems supported by the Telecommunication Research Institute of Ontario (TRIO). This research program has created opportunities for the Electronics Department of Carleton University to study the potential of integrating telecommunication systems, mobile radio systems in particular, into integrated circuits in a university design

environment. Although this thesis focuses on I.C. design for telecommunication applications, the ongoing I.C. design research activities at Carleton University are also of interest to other engineering/scientific applications, e.g. robotic research, cochlear implant research, etc. This thesis will demonstrate that Carleton University has the capability to implement mixed analog/digital LSI chips. Thus, researchers have the opportunities to miniaturize their analog/digital circuits onto a chip in a university environment.

The objective of this thesis is to implement the baseband data demodulator of a mobile radio receiver into a single integrated circuit (I.C.). The nominal data rate of the demodulator is 16 Kbits/s. The system consists of both analog and digital circuitries. The I.C. will be designed with Northern Telecom Ltd.'s 3- μ m double-level metal CMOS process through the Canadian Microelectronics Corp. (CMC). The baseband demodulator chip will be designed by a two-man team. One designer will concentrate on the design of the analog circuits while the other designer will design the digital circuits of the system. This thesis will focus on the design and implementation of the digital functions of the baseband demodulator chip, the timing recovery circuitry. An I.C. design methodology will be devised to implement mixed analog/digital system. The methodology will show great emphasis on high level system simulation and verification to achieve a chip design that shows full functionality in the first chip iteration. The success of this work has led to presentations at the Canadian Conference on VLSI (CCVLSI) at Halifax and the CMC workshop at Queen's University, Kingston.

1.2 Thesis Format

Chapter 2 will discuss the development of the I.C. design environment at Carleton University. A brief summary of I.C. design techniques and I.C. design methodology to implement the baseband demodulator will be described. The development of the standard-cells which are used in the design of the baseband demodulator chip will be presented. A description of the baseband demodulator system will be given in Chapter 3. A functional description of each functional block along with the high-level simulation results of the demodulator system will be presented. This provides a background for Chapter 4 in which the designs of the digital circuits and their layouts will be described. Chapter 5 will focus on the testing and characterization of the integrated circuits designed in this thesis work.

Chapter 6 then concludes the report by summarizing the work accomplished and suggesting areas of future work to improve the design of mixed analog/digital I.C.'s.

Chapter 2

I.C. DESIGN ENVIRONMENT

2.1 Introduction

This chapter discusses the development of an I.C. design environment at Carleton University using the resources provided by CMC. The chapter begins with a discussion of I.C. design techniques and the constraints considered in choosing the technique. The second section describes the I.C. design methodology that is suitable for the chosen design technique. This is followed by the implementation of the methodology using the available I.C. CAD tools. The final section presents the development of a standard-cell library. The library consists of over 50 logic cells and 20 analog cells.

2.2 I.C. Design Techniques

The commonly used I.C. design techniques are: full-custom, semi-custom standard-cells, gate array, and silicon compiler. The advantages and disadvantages of these techniques will be described in the following sub-sections. In the closing sub-section, one of these techniques will be selected for the implementation of the pilot project.

2.2.1 Full-Custom

The full-custom approach requires the longest design time when compared with the other design approaches. The layout is the most time consuming part of this technique because devices and interconnects are packed as closely as possible by hand. Everything is so closely packed that correction of errors is cumbersome and time consuming. In general, full-custom design involves subdividing the system into macrocells and laying out each macrocell to achieve certain performance goal with the lowest chip area. The full-custom technique is the oldest method of designing I.C. and today it is used in whole or in part to layout high volume chips, e.g. standard memory chips and microprocessor/microcomputer chips.

2.2.2 Semi-Custom Standard-Cell

The standard-cell I.C. design technique relies on a library of predefined logic/circuit cells. With few exceptions, every cell has the same height, though its width may be different. A typical standard-cell library consists of primitive cells such as inverter, NAND, and NOR gates, and macrocells such as D-type flip-flops and latches. A more extensive library may include macrocells and analog cells, e.g. up/down counter and op-amps. Although the preparation of a cell library takes time, the layout time of an application specific integrated circuit (ASIC) is greatly reduced.

An I.C. designer can call up specific cells, arrange them into parallel rows, and route the interconnects among the cells in the routing channel. A typical floor plan of a chip layout using standard-cells is shown in Fig. 2.1. Note that the power rails are arranged interdigitatedly. Control and clock signals can cross-over the power rails either by polysilicon underpass or by second level metalization depending on the I.C. fabrication technology.

The success of standard-cell design technique can be explained by its hiding of all design rules in the predefined cells except the clearance of the wiring in the routing channel. Thus, a chip layout which has all the design rules within the cell rows obeyed can be achieved. This technique reduces the design task to one optimization: minimizing the area of the routing channel. Given a well established standard-cell library, greater chip complexity can be realized while still maintain a high "First Time Success" rate and reduced design time. Although standard-cell design technique does not offer the highest circuit performance and circuit density as that of full-custom design, the advantages far outweigh the disadvantages.

2.2.3 Gate Array

A gate array is a chip on which pMOS and nMOS transistors are placed in a matrix form without connections. By connecting these transistors, a certain type of gate can be realized. Then by connecting these gates, a digital system can be implemented. Therefore, only the masks for connections and contacts have to be custom made. Also because only interconnections are considered in the I.C. layout, CAD tools can be used efficiently; thus greatly reduce the layout time. Gate array has the following disadvantages. The first disadvantage is the large chip size because large spacing must be provided for connections between adjacent columns and adjacent rows of transistors. The second disadvantage is the

Figure 2-1: Typical Standard-Cell Chip Floor Plan

possibilities of a high percentage of unused transistors depending on the particular system to be implemented onto a gate array chip. Another disadvantage is the trade-off in speed due to the fixed transistor sizes.

2.2.4 Silicon Compiler

The last method of I.C. design is the use of a silicon compiler. A silicon compiler design technique is based on writing a computer program which describes the system to do the I.C. designing. The compiler will take an input design specification at the system level and generate details at a lower level or the mask level. This design technique requires time to develop the silicon compiler. The choice of compiling level, computer language, and where the user/compiler feedback is established in the design cycle will affect the time required to develop the compiler.

2.2.5 Selection of I.C. Design Techniques

Taking into consideration the capability of I.C. design tools at Carleton University and the circuit complexity of the system to be implemented, one of these design techniques must be selected. The Metheus does support gate array designs. However, since Northern Telecom does not support gate array structure, there is no advantages in choosing the gate array design approach. The second technique considered is silicon compiler. At present, Carleton University does not have CAD tools that offer silicon compilation. Therefore, the two potential I.C. design techniques left are semi-custom standard-cell and full-custom methods.

In choosing between these two methods, some important factors have to be weighted:

- 1) the project to be implemented consists of analog and digital circuits
- 2) design time is restricted to approximately six months
- 3) high "First Time Success" rate is essential

For these reasons, an I.C. design technique that allows short design time and offers high "First Time Success" rate is desirable. These constraints rule out the full-custom design technique. Furthermore, after examining a number of articles, [11], [12], it is evident that semi-custom standard-cell design technique is most suitable for designing mixed analog/digital chips.

2.3 I.C. Design Methodology

I.C. design using standard-cells design technique has been very successful in recent years. Greater chip complexity can be achieved while still maintain a high "First Time Success" rate and reduced design time.

The methodology devised for the implementation of the mixed analog/digital system is a top-down standard-cell design approach with great emphasis on high-level system verification to achieve a more effective design. Top-down approach implies that one starts with the desired system to be implemented, decomposes it into functional blocks, and decomposes further to give more details at the lower level description, down to the geometric features of the masks. This methodology primarily consists of three stages:

Phase I: system and functional block description and high-level system verification

Phase II: circuit design with standard-cells and chip layout

Phase III: fabrication and testing

A flow chart of the top-down standard-cell design process is depicted in Fig. 2.2.

The design process begins with Phase I where key requirements relating to system specification and constraints relating to system performance are defined. This is followed by structure design where the system is decomposed into functional blocks, e.g. band-pass filter, phase-locked loop, integrate-and-dump filter, etc. Detailed description of each block's input/output requirements must be defined at this point in order to allow it to be interfaced with other blocks. A high-level simulator is then used to simulate the operation of the system. This allows the designer to firm up the structure design, the timing and the connectivity of the functional blocks. Functional block description and system simulation at this level involves the use of design languages, timing equations, propagation delays, and technology dependent parameters to verify and evaluate the system at this early stage.

Once the integrity of the system has been validated, one proceeds to Phase II where each functional block is designed and laid out using cells from the standard-cell library. An I.C. designer may choose to place and connect the cells either manually or automatically using a standard-cell auto-place-and-route (APAR) package provided that the cells are APAR compatible. The decision is based on the nature of the system (digital, analog, or mixed), the complexity of the system, and the design time allowed. At present the APAR package,

Figure 2-2: Top-Down I.C. Design Methodology

Chipsmith [13], of Carleton University has not yet been well set-up; and the system to be implemented consists of mixed analog/digital circuits. Therefore the pilot project will be laid out manually. Once the layout of each functional block has been completed, a physical layout extractor is used to create a simulation netlist. The functionality of each block can then be verified with either an electrical simulator or a switch-level simulator. Once the circuit design of each functional block has been validated, the system can be realized by connecting the functional block layouts. A layout extractor is used again to create a netlist to check the connections of the functional blocks. Once that has been verified, the design process then enters Phase III where a Caltech Intermediate Form (CIF) file is created from the layout and sent to the foundry to be fabricated. This completes the top-down standard-cell design methodology.

2.4 CAD Tools

This section gives a general overview of CAD workstations and discusses the I.C. design softwares that are used for the implementation of the pilot project.

VLSI research at Carleton University is supported by two classes of workstations: Metheus lambda 750 and SUN 3/60. The Metheus main CPU consists of two M68000 microprocessors. It has 8 Mb of main memory and two 33 Mb winchester disk drives. The 19-inch colour monitor has 1024x768 pixels and supports 8 million shades. The operating system of the Metheus is Berkeley UNIX 4.1. Peripherals include an HP7580 pen plotter and a Versatec V80 plotter.

The Metheus workstation has been well supported with a number of I.C. design softwares:

VALE: an I.C. mask level layout editor

PHLEX: a circuit extractor that translates a layout file into a circuit netlist

LEO45: a design rule checker

SPICE: an electrical simulator

Hg: a switch-level simulator

HLO: a logic simulator

Details of these softwares can be found in [14].

The I.C. design capability on the SUN 3/60 is discussed in the following. The main CPU of the SUN 3/60 consists of a 20 MHz M68020. It has 4 Mb of main memory and 575 Mb disk drive. Its 19-inch color monitor has 1152x900 pixels with 8 colour graphics planes.

At the time of chip implementation for this project, there are not many I.C. CAD softwares installed on the SUN workstation. It basically has two electrical simulators, SPICE [15], and HSPICE [17], and a logic/electrical simulator, SPLICE [18].

SPLICE Version 1.7 is a mixed-mode simulation program developed for the analysis of MOS circuits. Mixed-mode simulation allows the designer to choose the level of analysis best suited to each part of the circuit, with logic and electrical analyses performed concurrently. Electrical analysis is used where detailed timing information is essential; and logic analysis is used where first-order timing information and function verification is sufficient. The simulator is schematic based with a netlist input similar to SPICE. Some of the standard netlist circuit elements incorporated in SPLICE are: NAND, NOR, inverter, buffer, passgates, capacitors, resistors, MOS transistors, and voltage sources. Researchers at Carleton have made modifications to SPLICE so that additional circuit elements can be defined by the user. The additional elements are described using FORTRAN codes; and they can be used as part of a circuit netlist. For instance, a switched-capacitor filter can be described by difference equation using only a few lines of codes. Thus, by describing the behavior of functional blocks with programming languages, a complex system can now be simulated with greater efficiency. Thus SPLICE has been selected as the high-level simulator in Phase I of the design methodology to verify the structure of the system and the system timing.

SPICE Version 2G.1 is a popular general-purpose circuit simulation program for non-linear dc, nonlinear transient, and linear ac analyses. Circuits may contain resistors, capacitors, inductors, independent and dependent voltage/current sources, and the four most common semiconductor devices: diodes, BJT's, JFET's, and MOSFET's. HSPICE H8801 is a commercial version of SPICE simulator. HSPICE is a sophisticated electrical simulator intended for circuit designers who are already familiar with SPICE. HSPICE has additional features and options to SPICE; and it is more capable to converge to a solution for large circuits. In addition, HSPICE runs approximately three times faster than SPICE for the same circuit on identical workstation. HSPICE is selected as the electrical simulator used in Phase II of the design methodology when detailed and accurate voltage and timing

informations are needed.

In Phase II, a switch-level simulator is also required to verify the functionality of the digital chips' layouts performed for this project. The selected simulator is Hg of the Metheus workstation. Hg can be used to verify the operation of combinational logic, to check propagation time within a logic circuit, and to analyze complex sequential logic circuits. Simulation is performed by modeling the transistors by their "average channel resistance"; and transition delay is calculated based on the charge/discharge time of the load capacitor at the node under consideration. Thus a large digital circuits (1000 gates) can be readily simulated in much shorter time than SPICE/HSPICE. For the pilot project, Hg is used to verify the function and to simulate the performance of the digital phase-locked loop chips so that the chips will be functional for the first chip iteration.

At present the SUN 3/60 workstation does not support a mask level layout editor. Therefore all I.C. layout tasks are performed on the Metheus workstation using the layout editor VALE. The I.C. designer calls in the standard-cells from the cell library installed on Metheus and performs the required interconnects. Functional block layouts are created and they are saved as macrocells in the user's own file space. From these layouts, the required netlist to create simulation decks for SPICE/HSPICE and Hg can be extracted by using PHLEX. By running simulation on the layout, the designer can verify correct functionality as well as observe the effects on performance due to interconnect capacitance. Once the functionality of each block has been verified, the designer then uses LEO45 design rule checker to determine if the mask layers conform with the design rules.

Once the layout of the system has completed, a CIF file is created by using the command PHL2CIF on the Metheus. The CIF file is sent to CMC for implementation using the electronic mailing network.

2.5 Design of a Standard-Cell Library

Standard-cell I.C. design still represents the premier approach for designing quick turnaround I.C.. Standard-cells are more flexible to use, faster in speed, and more dense than gate array designs of comparable technology. Within the boundary of each standard-cell, it is a handcrafted design that can be optimized and fine tuned as desired. Also, cells can be added to the library whenever an application occurs that justify their design.

The basic structure of a standard-cell is shown in Fig. 2.3, [18], [19], [20]. Each cell has power (V_{dd}) and ground (V_{ss}) running horizontally through the cells. Therefore, by arranging cells in parallel rows, straight power and ground rails can be realized. The input and output signals of each cell are accessible either from the top or from the bottom of the cells. This arrangement allows a higher degree of freedom in placement and routing which results in a smaller chip size.

Figure 2-3: Standard-Cell Structure

When designing a standard-cell library, there are a number of considerations that can influence the design approach of the cells. These considerations include: design rules, speed requirements, density requirements, technology characteristics, and applications. At the very beginning of the library development, it is necessary to decide which of the above considerations are most important. This leads to decisions on the required cell height, grid space, and optimum beta ratio, $\beta = W_n/W_p$.

Fundamental decisions such as device sizes and beta ratios are made early in the cell development stage. The selection of beta ratio may take into account such parameters as power dissipation, propagation delay, noise immunity, and area. This issue has been examined extensively by [21], [22]. For the Northern Telecom (NT) CMOS3 technology, an effective beta ratio of 0.5 has been selected for the design of standard-cells. The layout of a gate using this ratio does not result in pMOS transistors occupying too much area and still provides good performance and adequate noise margin. A CMOS3 logic gate having an effective beta ratio of 0.5 has a noise margin of 1.2 V for $V_{dd}=5$ V. This fundamental parameter was maintained consistently throughout the cell design.

The physical design of the standard-cells library was made to be compatible with APAR packages. The advantage gained using this approach will permit the use of APAR tools when a specific design would benefit from it. APAR compatible cells require spacing of input/output pins to be a multiple of a predefined grid. A unit of a grid was defined as a spacing which would permit unrestricted placement of contacts (metal/poly-Si connections) at every grid point. For the NT CMOS3 technology, a grid spacing of $15\mu m$, as shown in Fig. 2.4, is necessary to satisfy the above requirements without violating any design rules. The dimensions given in Fig. 2.4 are specified using a $5\mu m$ scale for the minimum feature size. The design will be scaled down to 60% of the specified dimensions at NT prior to the fabrication of the masks.

The standard-cell height was determined after many layout attempts of the primitive cells (inverters, NANDs, NORs, etc). Results of these attempts varies between 6 and 8 grids. However, it was soon discovered that all-important D-type flip-flop (D-FF) was not well laid out using these height; that is, external interconnects are necessary. The D-FF layout was very compact when a 10 grid cell height was used, without any external interconnects. The drive capability of the inverter, NAND, and NOR gates were also increased with this increased height. The V_{dd} and V_{ss} rails were placed at the top and bottom of the cells with a width equal to that of a standard grid. A typical CMOS3 standard-cell structure is shown in Fig. 2.5. The layouts of a 2-input NAND gate and a D-Flip Flop are shown in Fig. 2.6 and Fig. 2.7, respectively.

The library consists of 50 logic cells and 4 input/output pad cells. All the CMOS3 standard-cells have been simulated with an electrical simulator, SPICE. The simulated results of the primitive cells are shown in Table 2.1. The cells have been documented and

Figure 2-4: Grid Spacing for NT CMOS3 Process

have been compiled in the Carleton CMOS3 Standard-Cell Manual. An excerpt from the manual, low-drive inverter CINV01, can be found in Appendix A.

CELL	simulated delay	
INVERTER	1.0	NS
2-INPUT NAND	1.4	NS
2-INPUT NOR	1.6	NS

note: load equal to one fanout

Table 2-1: Propagation Delay of CMOS3 Cells

Carleton University has helped to develop a $3\mu\text{m}$ single-metal standard-cell library, Canadian Semiconductor Design Association (CSDA) Standard-Cells. It is used as a reference since the CSDA cells are also laid out using $3\mu\text{m}$ design rules and the cell height (separation of Vdd and Vss rails) is also identical. Therefore, a direct comparison is justifiable. Table 2.2 tabulates the primitive cells widths of both CMOS3 and CSDA libraries. The CMOS3 cell widths are either the same or narrower than the CSDA cells.

Figure 2-5: Typical Standard-Cell Structure of the CMOS3 Library

2.6 Summary

A summary of possible I.C. design techniques has been presented. Based upon the constraints that exist within an university I.C. design environment, a semi-custom standard-cell design technique was chosen. An I.C. design methodology that is suitable with the chosen technique was devised. The proposed I.C. design methodology has great emphasis on high-level simulation/verification to achieve a high "First Time Success" rate. The details of the CAD tools used to implement the methodology were also presented. A description of the standard-cell development was also given. A standard-cell test chip consisting of primitive cells and flip-flops was fabricated so that testing and characterization of the cells and the process can be performed.

With the proposed design methodology and the available CAD tools, it appears that mixed analog/digital systems could be implemented successfully. A mixed analog/digital

Figure 2-6: Physical Layout of a 2-Input NAND Gate

Figure 2-7: Physical Layout of a D-Flip Flop

CELL	CMOS3	CSDA
INVERTER	27 um	27 um
2-INPUT NAND	36 um	36 um
2-INPUT NOR	36 um	36 um
2-INPUT XOR	72 um	82 um
D-FLIP FLOP	117 um	135 um
D-LATCH	63 um	81 um

note: same cell height for CMOS3 and CSDA cells

Table 2-2: Comparison of CMOS3 and CSDA Cell Widths

baseband demodulator was used as a test vehicle to demonstrate the effectiveness of the proposed methodology and the chosen CAD tools. The design of the demodulator will be discussed in Chapter 3 and 4. Chapter 5 will present the test results obtained from the fabricated chips.

Chapter 3

SYSTEM DESIGN

3.1 Introduction

The previous chapter described the I.C. design environment which has been developed at Carleton University and the design methodology that is suitable for standard-cell I.C. design. The proposed I.C. design methodology is used to integrate the mixed analog/digital baseband demodulator for a mobile radio receiver. The first section gives a general overview of a mobile radio system. Then the design requirements and constraints of the demodulator will be discussed. It is followed by functional block diagram description and high-level simulation of the timing recovery circuit of the demodulator. Finally the simulation of the baseband demodulator system is presented.

3.2 System Overview

Data has been transmitted over radio channel for many years. In recent years, however, there is a growing interest in, and demand for, high-speed digital transmission to facilitate speech communication and high-speed data transmission in the field of mobile radio. Examples of applications requiring such a service include: law enforcement services, taxi and other dispatch systems, and automatic vehicle location system. A block diagram of a mobile digital FM radio system is shown in Fig. 3.1. The data source could be a computer, a tele-typewriter or any other logic circuits. The data sink could be a printer, a video display, a computer, or logic circuitry. The figure also shows that noise is introduced in the radio frequency channel.

A block diagram representation of a FM receiver is shown in Fig. 3.2. The signal $x(t)$ at the input of the receiver IF filter can be written as

$$x(t) = \sqrt{2P} \cos(\omega_o t + \theta(t)) + \zeta(t) \quad (3.1)$$

Figure 3-1: Block Diagram of a Mobile Radio System

where P is the signal power, $\omega_o = 2\pi f_o$ is the center IF filter radian frequency, $\zeta(t)$ is the white Gaussian noise of one-sided spectral density N_o . The function $\theta(t)$ is the data phase after FM modulation given by

$$\theta(t) = 2\pi f_d \int_{-\infty}^t m(t) dt \quad (3.2)$$

where f_d is the frequency deviation, and $m(t)$ is the Manchester format equivalent of the NRZ data. The IF filter is assumed to have the low-pass equivalent transfer function $H(f)$ with corresponding impulse response $h(t) = F^{-1}[H(f)]$. The output $y(t)$ of the bandpass limiter following the IF filter can be expressed as

$$y(t) = \cos[\omega_o t + \phi(t) + \eta(t)] \quad (3.3)$$

where $\phi(t)$ is the filtered signal phase which is expressed as

$$\phi(t) = \tan^{-1} \frac{\int_{-\infty}^t h(t-\tau) \sin \theta(\tau) d\tau}{\int_{-\infty}^t h(t-\tau) \cos \theta(\tau) d\tau} \quad (3.4)$$

and $\eta(t)$ is the phase noise

$$\eta(t) = \tan^{-1} \frac{\xi(t)}{\sqrt{2\rho(t)} + \vartheta(t)}. \quad (3.5)$$

Here, $\xi(t)$ and $\vartheta(t)$ are independent Gaussian variables with zero means and unit variance and $\rho(t)$ is the time varying SNR given by

$$\rho(t) = \frac{E_b}{N_o T} \frac{a^2(t)}{\int_{-\infty}^{\infty} |H(f)|^2 df} \quad (3.6)$$

where $E_b = ST$ is the signal energy per bit and $a(t)$ is the filtered, normalized signal amplitude whose square is expressed as

$$a^2(t) = \left(\int_{-\infty}^t h(t-\tau) \sin \theta(\tau) d\tau \right)^2 + \left(\int_{-\infty}^t h(t-\tau) \cos \theta(\tau) d\tau \right)^2 \quad (3.7)$$

The probability density function of the phase noise is given by [35]

$$p(\eta) = \int_0^{\infty} \frac{x}{\pi} e^{-x^2 - \rho(t) - 2x\sqrt{\rho(t)} \cos \eta} dx ; \quad |\eta| < \pi \quad (3.8)$$

Figure 3-2: Block Diagram of a FM Receiver

Two of the most important problems in portable-mobile radio systems are power consumption and printed-circuit board area of the baseband modulator and demodulator sections. The objective of the pilot project is to implement the baseband demodulator of a mobile radio receiver onto a test chip. The baseband demodulator chip is developed toward single power supply, less power consumption, and fewer external parts.

The functional block diagram of the baseband demodulator is shown in Fig. 3.3. Each functional block represents a collection of circuitry that performs one or more tasks, and interfaces with other functional blocks to implement the desired system. The front-end of the demodulator contains a band-pass filter to reduce wideband noise thereby significantly improving the data error rates; and it is followed by a slicer which converts received Manchester coded signal to digital bit stream (A). The slicer removes amplitude noise, but phase fluctuations remain. Thus (A) is a replica of the transmitted bit stream perturbed with phase noise. A timing recovery circuit extracts an almost noiseless phase coherent clock waveform (B). The timing recovery circuit employs a phase-locked loop (PLL) to extract clock information from the Manchester bit stream. The Manchester bit stream (A) is "exclusive-NORed" with the local receiver clock (B) to produce a noisy NRZ bit stream (C). The phase noise on (A) and phase error of the local receiver clock (B) produce unwanted spikes at the border of each of NRZ bit period. The noisy NRZ bit stream enters the integrate-and-dump filter, producing waveform (D), which is strobed before each dump by the data strobe (E). The data sampler retains the output from each strobed sample to produce clean NRZ data (F).

Evolution in I.C. technology, particularly in CMOS, has made it possible to realize low power consumption analog and digital circuit elements on the same chip. The band-pass filter, slicer, and the integrate-and-dump filter were implemented with switched-capacitor circuits by a fellow graduate student [23]. This thesis will focus on the realization of the timing recovery circuit. The demodulator is to be operated at a data rate of 16 Kbits/s.

The freedom of the demodulator output from bit errors is closely related to the ability of the timing recovery circuit to correctly position the derived clock in order that the function of decoding, integrate-and-dump, and data strobing may be accomplished even when the incoming data stream is contaminated by noise. Several factors affecting bit error rates are:

- 1) Clock Acquisition and Tracking Range: The clock acquisition circuits should possess a

Figure 3-3: Block Diagram and Waveforms of a Baseband Demodulator

relatively wide capture range during acquisition and a narrow tracking range once locked. The narrow tracking range is permitted so that a lower tracking loop bandwidth can be used to maintain a mean bit clock frequency of 16.0000 KHz relatively immune to system noise. The tracking range is made commensurate with the stability of the transmitted data clock.

2) Derived Clock Lock Stability: The derived clock phase tracking circuits must track the expected mean phase of the incoming bit stream even though large phase noise excursions from the mean are present in the incoming data stream. In addition, the derived clock phase memory must be adequate to coast through deep fades lasting as long as 5 ms [24], during which time phase updating of the clock should be minimized.

3) Time Delay Distortion: If time delay in the band-pass filter is not constant over the signal emission band, the demodulated data zero crossings for dotting (101010 data sequence) and all-ones and all-zeros are offset in time relative to the zero crossings of the data clock. This situation is shown in Fig. 3.4 wherein the zero crossings for dotting occurs $10\text{ }\mu\text{s}$ early, whereas the zero crossing for all-zeros occurs $10\text{ }\mu\text{s}$ late. This early and late zero crossings condition makes it difficult to optimize the data strobe pulse position for data detection.

Figure 3-4: Zero Crossings of Band-Passed Signal

3.3 Timing Recovery Circuit

Timing recovery or bit synchronization is one of the most critical receiver function in synchronous communication systems. The baseband demodulator of a data receiver requires the existence of a digital clock, synchronized to the received data stream, to perform data demodulation task, to control the timing of the integrate-and-dump (I-and-D) filter, as well as the timing of the output data. Also, the receiver clock must be continuously adjusted in its frequency and phase to compensate for frequency drifts between the oscillators used in the transmitter and receiver clock circuits.

The timing recovery circuit is essentially a phase-locked loop (PLL) that tracks data transitions and based on some meaningful optimization criterion which determines the steady-state location of the timing instance. The PLL can either be implemented digitally or using analog circuits. An analog PLL circuit on chip is sensitive to temperature, component accuracy, and d.c. bias voltage drift [25], [26]. Thus, an analog PLL requires initial calibration (e.g. tuning the nominal frequency) and periodical adjustments (e.g. frequency offset due to component aging). A digital version of the PLL alleviates some of the problems associated with its analog counterpart because the loop performance of a DPLL is insensitive to temperature, supply voltage deviations, etc. Furthermore, continued progress in increasing performance, speed, reliability, and the reduction in size and cost of I.C. has resulted in strong interest in the implementation of the PLL in the digital domain [25]. Since the PLL chip is to be implemented within six months and it must work the first time, a digital version of PLL is chosen as the circuit to implement the timing recovery circuit.

The timing recovery circuit block diagram is shown in Fig. 3.5. This circuit is based upon the design for digital PLL (DPLL) given by Cessna and Levy [28]. This DPLL is made of five parts: a binary phase detector, a sequential loop filter, a local clock oscillator, a digital-controlled oscillator (DCO), and a divide-by L scaler. The characteristic of this type of loop is that the phase detector output is a binary signal. This signal is used to advance or retard the phase of a stable local clock oscillator by a discrete amount in such a direction as to bring the phase misalignment to a minimum. This type of DPLL is particularly suited for clock-timing recovery from received data because it performs as a transition tracking

loop as will be shown later in this chapter [27]. Also, when compared to a classical DPLL which requires an A/D converter, digital filters, and a D/A converter to implement, the simplicity of the DPLL in Fig. 3.5 makes it very attractive for "Work the First Time" chip implementation.

Figure 3-5: Timing Recovery Circuit Block Diagram

The functional behavior of each part of the DPLL is discussed in the following sections.

3.3.1 Binary Phase Detector

A binary phase detector determines phase misalignment between the received signal and the local clock; and provides corrective LAG or LEAD outputs which adjust the local clock phase to diminish phase error. Since the output of this type of phase detector is either LAG or LEAD, it is also referred as Binary Quantized Phase Detector. The technique of phase detection largely dependent on the format of the signal data. The operation of phase detection for square wave is first considered. Then a method to extract clock timing from the Manchester data signal is presented.

A method of tracking a square wave input is shown in Fig. 3.6. For each positive

transition of the input signal $s(t)$, a pulse is generated. As seen in Fig. 3.6, the pulses $p(t)$ contains a frequency component synchronous with the input. The pulses are compared with the local clock $u(t)$, and a decision is made as to whether the local clock lags or leads the incoming data transitions. As shown in Fig. 3.6, a pulse located in the "0" region of the local clock produces a LAG decision while a pulse in the "1" region generates a LEAD decision.

If the Manchester format is utilized, the incoming data signal can have transitions at the beginning and in the center of the bit period. For simplicity, a data rate of 16 KHz is assumed in the discussion. A modified circuit of Fig. 3.6, shown in Fig. 3.7, may be used to synchronize a PLL operating at twice the data rate frequency, 32 KHz. A divide-by-2 flip-flop is then used to obtain the 16 KHz receiver clock. The output of the divide-by-2 flip-flop could be ambiguous because the 16 KHz receiver clock could settle at the opposite phase, as depicted in Fig. 3.7 as $g(t)$, depending on the initial state of the flip-flop. This results in a faulty interpretation of the received data, because the start and the center of every bit period are erroneously exchanged.

To establish the correct phase of the recovered clock signal, it is necessary to extract the 8 KHz Fourier component of the Manchester bit stream [29]. That is to track the mid-bit transitions of each bit period. A method of extracting the 8 KHz component of the received bit stream is shown in Fig. 3.8. The edge detector generates a pulse for each transition of the bit stream, $s(t)$. Preceding every transmission of message, a dotting sequence (101010 data sequence) is sent for bit synchronization. Thus a pulse is generated in the center of each bit period, $p(t)$. The pulses are then compared with local 16 KHz clock, $u(t)$, to decide whether the local clock leads or lags the pulses, as discussed for the NRZ case. This dotting operation slaves the PLL's 16 KHz clock to the center of the bit period. Thus the phase of the 16 KHz receiver clock, $g(t)$, is well established. For each sequence of all-ones or all-zeros data, the phase detector produces one timing up-dating information. Nonetheless, no erroneous timing informations will be generated. This operation is summarized in Fig. 3.9.

3.3.2 Sequential Loop Filters

The outputs of the all digital phase detector discussed in the previous section can be used to control the DCO without any loop filtering. For bit synchronization, this is

Figure 3-6: Binary Phase Detector for Square Wave Input Signal

Figure 3-7: Modified Phase Detector for Manchester Coded Input Signal

Figure 3-8: Phase Detector for Manchester Coded Signal During Dotting Operation

Figure 3-9: PD Operation for All Zero's and All One's Sequence

not desirable, since the slightest phase error immediately affects the DCO. Many incorrect adjustments would be made that cause undesirable phase fluctuations. Although no loop filtering is strictly needed to obtain close-loop operation, it seems desirable to perform some filtering. The type of loop filter that is compatible with the Binary Quantized Phase Detector is the sequential loop filter. Its task is to statistically generate an ADD command or a DEL command based on the number of LAG and LEAD decisions output by the phase comparator. Two classes of sequential loop filters [28], are described in the following.

N-Before-M Filters:

The N-before-M filter, shown in Fig. 3.10, operates as follows. LAG and LEAD inputs are accumulated in registers of length N, while their sum is accumulated in the register of length M. Assume initially that all three counters are reset. The random sequence of binary inputs (LAG and LEAD) continues until one of two conditions is met. 1) If one of the N registers fills up before or simultaneous with the M register, then corresponding output is produced, all three counter are reset, and the cycle begins anew. 2) If the M counter fills up before either N counters, all three counters are reset, and no output is produced. The latter condition is most likely when phase misalignment is near zero, resulting in nearly equal number of inputs of each type.

Random Walk Filters

Another class of sequential loop filters producing similar performance as that of N-before-M filters is the random walk filter (RWF), shown in Fig. 3.11 [28]. This filter is named after the classical problem in probability theory, which exactly characterizes its operation. A random walk filter is made up of a bi-directional counter whose length is $2N+1$. In Fig. 3.11, the content of the counter is increased or decreased one by one for the command signal LAG and LEAD. When the contents of the counter reach $+N$ or $-N$, the corresponding ADD or DEL signal is produced. So at least N inputs are needed to produce the output signal, and the duration time between outputs is maximum when phase misalignment is near zero.

The N-before-M and RWF filters perform operations seems to be desirable, namely the filter output causes a phase correction, which has a higher probability of being correct than if corrections were made directly from phase detector outputs. Since both filters have similar performance, a decision needs to be made as to which filter is most appropriate for I.C. implementation. That is which filter consumes less area for the same performance.

Both sequential loop filters are normalized to have the same duration time between outputs when the probability of LAG and LEAD equal 0.5. Let duration time equals 36 phase detections. That is, it takes 36 phase detections to generate an output from the filter. For N-before-M filter, $N=8$ and $M=12$. For random walk filter, $N=6$. To implement the N-before-M filter with binary up-counters, it requires three counters: two 3-bit counters and one 4-bit counter. The random walk filter can be implemented with a 4-bit up-down-counter. The estimated gate count for the N-before-M filter requires 120 gates whereas the RWF requires 80 gates. Therefore, the random walk filter is selected as the sequential loop filter for I.C. implementation.

3.3.3 Digital-Controlled Oscillator

A digital-controlled oscillator (DCO) is basically a frequency source, with a phase correction capability. This device, shown in Fig. 3.12.a, makes discrete phase corrections corresponds to a voltage-controlled oscillator in conventional analog loop. This DCO is intended to operate in conjunction with those loop filters that generates ADD and DEL pulses. The operation of the DCO follows from the waveform shown in Fig. 3.12.b. In the absence of ADD or DEL pulses, the DCO divides the input fixed frequency by 2. Whenever an ADD pulse appears, a clock cycle is added by the internal logic of the DCO. A clock cycle is deleted on the other hand, whenever a DEL pulse appears. The output of the addition and subtraction circuitry is fed to a divide-by L scaler. Each cycle at the input to the divider represents a fraction of the output equals to $\Delta = 360^\circ/L$. Thus each loop filter output, by causing one pulse to be added or deleted, causes the DCO to be adjusted by $\pm\Delta$. Furthermore, the output frequency of the DCO can be controlled within a range governed by the maximum frequency of the ADD and DEL pulses.

Since the fixed frequency oscillator is not coherent with the signal source, it will not, in general, be possible by discrete adjustments of $\pm\Delta$, to bring the local clock in perfect alignment with the signal. The minimum value of phase misalignment is denoted by δ . Note that $|\delta| \leq \Delta/2$ since if this inequality does not hold, a shift in the phase of the local clock by integer multiple of Δ will bring about this condition, as shown in Fig. 3.13.

Several properties of the DPLL described above are summarized as follows. A more detail analysis can be found in [28], [30], [31].

Locking Range and Pull-In Time

Figure 3-12: Digital-Controlled Oscillator

Figure 3-13: Intrinsic Phase Error of the Digital PLL

The locking range of the DPLL using RWF is given by

$$f_{h0} = \frac{N}{T_c(NL - 1)} \quad (3.9)$$

$$f_{l0} = \frac{N}{T_c(NL + 1)} \quad (3.10)$$

$$B_0 = f_{h0} - f_{l0} = \frac{2N}{T_c(N^2L^2 - 1)} \doteq \frac{2f_0}{NL} \quad (3.11)$$

where $f_0 = 1/(T_cL)$ is the free running frequency, f_{h0} and f_{l0} are the upper and lower locking frequency limit, and B_0 is the locking range bandwidth.

The pull-in time of the DPLL in absence of noise can be estimated by

$$\varphi = \frac{K_\varphi T_c}{N} \quad (3.12)$$

where φ is the initial phase misalignment and K_φ is the number of phase detections required to shift the output phase from φ to 0.

The filtering network of the DPLL needs to be designed in such a way that the receiver clock will retain bit synchronization with the incoming data during fades up to 5 ms. On the other hand, mobile radios are push-to-talk terminals requiring fast signal acquisition. Subjective measurements indicate that lock-in time should not exceed 150 ms or 2400 bits at 16 kbits/s [9]. Thus the loop bandwidth of the DPLL is to be controllable externally as

suggested in [9], [32]. This is accomplished by changing the RWF parameter N . A signal-detection circuit at the output of the IF filter which indicates the presence or absence of signal may be used to control the DPLL bandwidth during operation. A realization of the signal-detection circuit can be found in [9]. For clock acquisition, a low $|N|$ (wide bandwidth) is selected to achieve a high-rate of clock phase correction. As soon as the presence of signal is detected, the loop bandwidth is narrowed; that is a large $|N|$ is selected to reduce phase jitter during tracking. It is this use of large N that permits the recovery circuit to ignore transients due to multipath. Since the minimum phase error is a function of L of the scaler, the DPLL design has also incorporated an option of $L=32$ or $L=64$. A complete functional block diagram of the timing recovery circuit is shown in Fig. 3.14.

After examining a number of papers [9], [24], a locking-range in excess of ± 50 Hz was suggested for the 16 Kbit/s condition. The crystal oscillator stability is $\pm 10^{-5}$, corresponding to a clock jitter of less than ± 0.16 Hz for the same condition. Therefore, a loop was designed to track this bandwidth. The parameter N was determined by solving equ. 3.11 for $L=32$. For the DPLL test chip, the value of N is 2 for acquisition and 128 for tracking, as suggested by [9].

$$N = 2$$

$$B_0 = 500 \text{ Hz}$$

$$N = 128$$

$$B_0 = 7.8 \text{ Hz}$$

3.4 High-level System Simulation

The purpose of high-level simulation is to obtain informations about the expected performance of a given system structure before detailed circuit design commences. The simulation and the modeling at this level involve the use of design languages, delays, and timing equations to describe the behavior of the circuit accurately. This enables the designer to firm up the integrity of the system at the early stages. The performance of the demodulator under consideration depends on the interaction of sampled-data analog circuits and digital circuits. Thus a program capable of simulating mixed sample-data and digital systems is required.

The high-level simulator used to simulate the baseband demodulator is SPLICE [16]. SPLICE is an event-driven simulator used for functional and electrical simulation. It has a fixed time step of calculation, the minimum resolvable time (MRT). The fixed time step can

- * for N = N1 (high-speed), DPLL C = 1
 for N = N2 (low-speed), DPLL C = 0

- # for L=32, freq. of master clock = 1.024 MHz
 for L=64, freq. of master clock = 2.048 MHz

Figure 3-14: Block Diagram of the Timing Recovery Circuit

be a fraction of the shortest clock period that might occur in a mixed analog/digital system. Thus a sample-data circuit operates at 512 KHz can derive its clock from a digital circuit clocking at 2.048 MHz. The event-driven nature of calculation allows both high-frequency digital and low-frequency sample-data calculations coexist very efficiently. The simulator is schematic based with a netlist input similar to SPICE [15]. Some of the standard netlist circuit elements incorporated in SPLICE are: NAND, NOR, inverter, buffer, passgates, capacitors, resistors, diodes, transistors, and voltage sources.

Researchers [33] at Carleton University have made modifications to SPLICE so that additional circuit elements can be defined by the user. The additional elements are described using RATFOR, a FORTRAN preprocessor language, compiled, and linked with the simulator as a subroutine. Once linked with the simulator, the elements can be used as part of a circuit netlist. Complex functional blocks can now be described by programming languages to create powerful circuit elements. In the following sections, the development of two user defined models are discussed. It is followed by high-level verification of the DPLL and the baseband demodulator designs using SPLICE.

In this section, a user defined model description for the phase detector (PD) and the random walk filter (RWF) of the DPLL is examined. Recall that the content of the bi-directional counter is incremented if a pulse appears in the "0" region of the local clock, and is decremented if a pulse locates in the "1" region. When the counter reaches one of the limits, $+N$ or $-N$, a corresponding ADD or DEL command signal is generated; and the counter resets to zero. The instruction flow chart of the PD and RWF model is shown in Fig. 3.15. Table 3.1 shows the FORTRAN model description and the invocation in SPLICE source deck. The dot tokens are instructions to the preprocessors while the functional description is recognized as normal FORTRAN codes. The RWF parameter N is available as an input parameter to the subroutine for the model, and is passed via the model card in the source deck. LAG/LEAD decisions are made once the positive-edge of the "edges" pulse is detected. It takes 31 lines of FORTRAN codes to describe the PD and RWF functional blocks. Although the PD and the RWF (bi-directional counter) could have been achieved using standard netlist logic elements in the source deck, it was more economical and time efficient to incorporate the circuits into a high-level digital model.

The switched-capacitor integrate-and-dump (I-and-D) filter, shown in Fig. 3.16.a, is chosen as an example to illustrate the modeling of a sample-data circuit. This circuit

Figure 3-15: Instruction Flow Chart of the PD and RWF SPLICE Model

```

%c ***** TABLE I *****
%c
%c FORTRAN Description of the PD and RWF
%c
%c .define lqmod2
%c .numinp 2
%c .numout 2
%c .begin
%c *****
%c      *phase detector and random walk filter
%c      *output a,b return to zero on negative edge of
%c      *input signal pulse
%c      *counter is reset on negative edge of input signal pulse
%c
%c *****
%c      *lvin1 = input signal pulse
%c      *lvin2 = local clock
%c      *lvop1 = ADD output
%c      *lvop2 = DEL output
%c
%c *****
%c      *par1 = parameter (N)
%c
%c *****
%c      integer state, pvin1, n
%c
%c ---->Initialization
%c      if(simtim.eq.0)then
%c          n=int(rnsm(pptr-1,))
%c          state=0
%c          pvin1=1
%c      endif
%c
%c ---->Detect Positive-Edge of Input Pulse
%c      if((lvin1.eq.2).and.(pvin1.ne.2))then
%c
%c ---->Increment content if local clk is "0"
%c          if(lvin2.eq.1)state=state+1
%c
%c ---->Decrement content if local clk is "1"
%c          if(lvin2.eq.2)state=state-1
%c          endif
%c          pvin1=lvin1
%c
%c ---->check if content equals +N
%c          if(state.eq.n)then
%c              if(lvin1.eq.2)then
%c                  lvop1=2
%c              else
%c                  state=0
%c                  lvop1=1
%c              endif
%c          else
%c              lvop1=1
%c          endif
%c
%c ---->check if content equals -N
%c          if(state.eq.-n)then
%c              if(lvin1.eq.2)then
%c                  lvop2=2
%c              else
%c                  state=C
%c                  lvop2=1
%c              endif
%c          else
%c              lvop2=1
%c
%c      endif
%c .end

```

Invocation of lqmod2 in SPLICE Source Deck

```

: .model (model name) lqmod: model=# parameters
: .model RWF lqmod: model=2 par1=2
: (instance name) outputs inputs (model name)
mod2 ADD DEL pulse local RWF

```

Table 3-1: FORTRAN Model Description of the PD and RWF

integrates the noisy NRZ signal and estimates the bit present when the data strobe is activated. Once the estimated data is strobed, the feedback capacitor is discharged and the integrating cycle is anew. The z-domain transfer function of the I-and-D filter during the integrating cycle is

$$H(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}} \quad (3.13)$$

The difference equation of the above transfer function is

$$V_{out}(t_n) = \frac{C_1}{C_2} V_{in}(t_n) + V_{out}(t_{n-1}) \quad (3.14)$$

The timing of integration with respect to ϕ_1 and ϕ_2 is shown in Fig. 3.16.b. Fig. 3.17 shows the instruction flow chart of the I-and-D filter, and the high-level language description of the model is shown in Table 3.2. The capacitor ratio C_1/C_2 is passed as a parameter in the subroutine. The difference equation, eq. 3.14, is evaluated when the positive-edge of the sampling clock input is detected. The digital data present at the output of the comparator is latched when the positive-edge of the data strobe pulse (ϕ_d) is sensed. At the same time $V_{out}(t_{n-1})$ is reset to zero. Fig. 3.18 shows the SPLICE simulation results of the I-and-D filtering action to recover clean NRZ data from the noisy NRZ input.

In this section, the SPLICE simulation of the digital PLL (DPLL) is discussed. Simulation is performed with the assumption that the input signal is a 101010... dotting sequence sent at a bit rate of 16 Kbits/s. Table 3.3 shows the source deck description of the complete DPLL. The added high-level models are accessed by the source deck in the same way as other models described previously. The input signal is sampled at a frequency equals to 32 times the data rate. This allows the edge detector outputs to be in synchronization with the local oscillator clock. Simulation results of the DPLL's tracking operation are shown in Fig. 3.19. The trace (edges) is the output of the transition edge detector. A pulse is generated for every transition of the input signal (in-sig). The simulation is performed having the receiver 16 KHz clock, rxclk, lags the pulses; the RWF counter length $N=2$, and the DCO scaler $L=32$. As depicted in Fig. 3.19, it takes two pulses to generate an ADD command. After a number of ADD command signals, the local clock locks on the input with a mean-absolute phase error $\leq \Delta/2 = 5.6^\circ$. That is the ADD and DEL commands are alternatively generated. A similar simulation with the local clock initially leads the input transitions is shown in Fig. 3.20. The simulation results verified the structure of the DPLL design.

Figure 3-16: Switched-Capacitor Integrated-and-Dump Filter

Next, the transient response of the DPLL to a phase step in the absence of noise is simulated. The initial content of the RWF is zero and the initial phase misalignment is 180° . The simulated results of phase error vs. the data transition count for ($N=2$ and $L=32$) and ($N=8$ and $L=32$) are shown in Fig.3.21. The number of transitions required to shift the output phase of the DPLL to zero from an initial phase, φ , can be approximated by eq. 3.12. Table 3.4 tabulates the simulated results and calculated results. The results are in perfect agreement with each other.

The performance of the demodulator is also simulated to validate the integrity of the system design. In order to simulate the demodulator faithfully, a high-level model that emulates the phase signal and noise component that appear at the output of the limiter-discriminator was required. Based upon the signal and noise characteristics, time domain models that generate phase signal with noise discretely in time were developed. The assumption made is that the signal channel noise is additive Gaussian and that the data and noise are statistically independent. Therefore the received carrier phase can be broken into

Figure 3-17: Instruction Flow Chart of the I-and-Dump Filter SPLICE Model

```

!c ***** TABLE II *****
!c
!c FORTRAN Description of the I-and-D Filter
!c With Comparator and Latch at the output.
!c
!define lgmod5
!numinp 3
!numout 1
!*begin
!c*****
!c *switched-capacitor integrator
!c *this model performs integrate & dump filtering
!c using an non-inverting integrator.
!c
!c*****
!c *lvin1 = sampling frequency input
!c *lvin2 = data strobe
!c *lvin3 = input signal
!c *lvop1 = hard-limited integrated signal
!c
!c*****
!c *par1 = c1/c2 capacitor ratio
!c
!c*****
! integer pvin1, pvin2, rxnrs
! real vol, vo0, k, latch
!c
!c---->Initialisation
! if(.simtim.eq.0)then
!   rxnrs=1
!   pvin1=1
!   pvin2=1
!   lvop1=1
!   vo0=0.0
!   k=rxnrs(pptr+1)
!   endif
!   time=real(s) *deltim
!   if(lvin3.eq.0) ut=-2.5
!   if(lvin3.eq.1) ut=+2.5
!c
!c---->Detect positive-edge of sampling freq input
! if((lvin1.eq.2).and.(pvin1.ne.2))then
!c
!c---->Evaluate the Difference Equation
!   vol=(k*input)+vo0
!c
!c---->V(tn-1)=V(tn)
!   vo0=vol
!   endif
!   pvin1=lvin1
!c
!c---->Detect positive-edge of strobe pulse
! if((lvin2.eq.2).and.(pvin2.ne.2))then
!   latch=vol
!   if(latch.ge.0.0)rxnrs=2
!   if(latch.lt.0.0)rxnrs=1
!   vo0=0.0
!   endif
!   pvin2=lvin2
!   lvop1=rxnrs
!end

```

Table 3-2: FORTRAN Model Description of the I-and-Dump Filter

Figure 3-18: SPLICE Simulation Results of the Integrated-and-Dump Filter

```

splice simulation of the digital-PLL (data rate (r) = 16kb/s)
;
; ***** TABLE III *****
;
; SPLICE Source Deck of the Digital PLL
;
;1 / (data rate) = 32 * (2 * mrt)
;phase comparison is done using estimated clk freq. at r/2.

;typical gates
.model dff1 lgmod: model-4 statin=1
.model dff2 lgmod: model-4 statin=1
.model dff3 lgmod: model-4 statin=1
.model del01 delay: delay=0.9765625us
.model buf01 buffer
.model inv01 inverter
.model nor01 nor
.model nan01 nand
.model nan02 nand
.model and01 and
.model xor01 xor
.model xnr01 xnor
.model zero lsrc: 0 0 0 1.953125us 0 0.9765625us 1.953125us
zer01 GND zero

;oscillator
.model osc01 lsrc: 0 1 0 2*mrt 0 mrt 2*mrt
.model osc01 lsrc: 0 1 0 1.953125us 0 0.9765625us 1.953125us

osc1 s1 osc01
buf1 osc s1 buf01

;transmitting clock
.model inclk lsrc: 0 1 0 62.5us 0us 30.2734375us 31.5us 61.5234375us 62.5us

txclk1 s2 inclk
buf2 inclk s2 buf01

.model div2 lgmod: model-8
blk8 insig inclk GND div2

;synchronized pos./neg. edge detector of input signal
dff1 x1 x1b osc insig dff1
del1 x1d x1 del01
dff2 x2 x2b osc x1d dff2
xnr1 edge x1b x2 xnr01

;zero-reset random-walk filter
.model xrwf lgmod: model-2 par1=2
blk2 ADD DEL gated dloclk xrwf

;digital voltage-controlled oscillator
.model dvco lgmod: model-3 par1=64 par2=0
blk3 loclk rxclk osc ADD DEL dvco
nan1 rxclkb rxclk rxclk nan01

;90 degree loclk delay
dff3 dloclk dloclkb rxclkb loclk dff3

;steering (windowing) circuit
nan2 k1 loclk edge nan02
inv1 gated k1 inv01

;phase difference calculator between txclk & rxclk
.model phase lgmod: model-6 par1=16000.
blk6 dummy rxclkb inclk osc phase

;1/(32*data rate) = 2*mrt
time 0.9765625us 2000us
.plot inclk insig edge rxclk rxclkb loclk dloclk gated ADD DEL

.stats

go
end

```

Table 3-3: Source Deck Description of the DPLL Circuit

Figure 3-19: SPLICE Simulation Results of the DPLL's Tracking Operation

Figure 3-20: SPLICE Simulation Results of the DPLL's Tracking Operation

Figure 3-21: SPLICE Simulation of Phase Error vs. Data Transition Count

**Pull-In Time for a 180 deg. Phase Step
(in number of transition count)**

N	L	pull-in time	
		calculated	simulated
2	32	16	16
8	32	128	128
32	32	512	512
128	32	2048	2048

Table 3-4: Simulated and Calculated Transition Counts

a data dependent term, called phase signal; and a noise dependent term, called phase noise.

The phase signal model is developed based on that only the two bits adjacent to the bit under consideration have any effects upon the bit [36]. Given a "0" for the bit under consideration, there are only four combinations that exists; 000, 001, 101, and 100. These 3-bits patterns are used to derive the Fourier series of $\sin\theta(t)$ and $\cos\theta(t)$ of eqn. 3.4. The phase noise is output discretely in time by generating the variates, $\xi(t)$ and $\vartheta(t)$ of eqn 3.5, that obeys the Gaussian distribution using the "inverse transformation method". The details of phase signal and phase noise models development can be found in Appendix B. Figure 3.22 shows a phase signal example of a random bit pattern. The same pattern with phase noise added is shown in Fig. 3.23.

The signal format used for performance evaluation of the baseband demodulator is shown in Fig. 3.24, [24]. The test pattern consists of the following sequence:

- 1) A 10-bit dotting sequence 1010101010 is required for bit synchronization acquisition. After the dotting sequence is terminated the phase of the local derived clock is updated by any 8 KHz component present in the data stream.
- 2) An 11-bit Barker sequence, 11100010010, for word synchronization is also required.
- 3) Pseudo-Noise sequence of length 1023 is transmitted repeatedly as the message.

Table 3.5 shows the complete source deck description for the demodulator. Figure 3.25 shows the connections of the custom models and logic elements to achieve the demodulator.

Figure 3-22: Random Bit Pattern Phase Signal without Phase Noise

Figure 3-23: Random Bit Pattern Phase Signal with Phase Noise

Figure 3-24: Test Signal Format for Performance Evaluation

A sample simulation run of the demodulator is shown in Fig. 3.26.

It was performed with a Gaussian IF filter, $BT=2$, $h=1$ and the signal-to-noise ratio, E_b/N_0 , is 15 dB where $h = 2\pi f_d T$, B is the bandwidth of the IF filter, T is the bit period, E_b is the signal energy per bit and N_0 denotes noise power spectral density. The data is sent synchronously with the transmitter clock, trace (txnrz). Trace (rdata) is the sliced Manchester coded signal which is to be "exclusive-NORed" with the receiver clock, rxclk. The decoded noisy NRZ data (nrz) is input to the I-and-D filter. The integrate-and-dump operation is depicted as trace (D). The clean NRZ data (NRZ) is output on the positive-edge of the receiver clock. Note the received data (NRZ) is the same as the transmitted data (txnrz). By comparing the waveforms of Fig. 3.26 with that of Fig. 3.3, the proposed structure of the demodulator meets the targetted system requirements described in section 3.2.

The bit-error rate (BER) performance of the demodulator was simulated to demonstrate the effectiveness of SPLICE in simulating VLSI analog/digital systems using user-defined models. The BER is obtained based on the number of errors present after 100,000 data bits has been sent under different signal-to-noise ratio. Each simulation run requires 3,200,000 minimum resolution time (MRT) steps and it takes 12 hours on a SUN3/60 workstation. The simulation is performed with $h = 1$ and $BT = 2$. The results of BER evaluation using SPLICE and theoretical BER [34] are shown in Fig. 3.27. The difference of the simulated values from the theoretical values is as small as 0.5 dB in E_b/N_0 at $BER = 10^{-3}$. The

```

splice simulation of the digital-PLL (data rate (r) = 16kb)
;
; ***** TABLE IV *****
;
; SPLICE Source Deck of the Demodulator
;
;1 / (data rate) = 32 * (2 * mrt)
;phase comparison is done using estimated clk freq. at r/2.

;typical gates
.model dff1 lgnd: model=4 statin=1
.model dff2 lgnd: model=4 statin=1
.model dff3 lgnd: model=4 statin=1
.model del01 delay: delay=0.9765625us
.model buf01 buffer
.model inv01 inverter
.model inv02 inverter
.model nor01 nor
.model and01 and
.model and02 and
.model and03 and
.model nor01 nor
.model nor02 nor
.model nor03 nor
.model nor04 nor
.model nor05 nor
.model nor06 nor
.model nor07 nor
.model nor08 nor
.model nor09 nor
.model nor10 nor
.model nor11 nor
.model nor12 nor
.model nor13 nor
.model nor14 nor
.model nor15 nor
.model nor16 nor
.model nor17 nor
.model nor18 nor
.model nor19 nor
.model nor20 nor
.model nor21 nor
.model nor22 nor
.model nor23 nor
.model nor24 nor
.model nor25 nor
.model nor26 nor
.model nor27 nor
.model nor28 nor
.model nor29 nor
.model nor30 nor
.model nor31 nor
.model nor32 nor
.model nor33 nor
.model nor34 nor
.model nor35 nor
.model nor36 nor
.model nor37 nor
.model nor38 nor
.model nor39 nor
.model nor40 nor
.model nor41 nor
.model nor42 nor
.model nor43 nor
.model nor44 nor
.model nor45 nor
.model nor46 nor
.model nor47 nor
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.model nor59 nor
.model nor60 nor
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.model nor67 nor
.model nor68 nor
.model nor69 nor
.model nor70 nor
.model nor71 nor
.model nor72 nor
.model nor73 nor
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.model nor75 nor
.model nor76 nor
.model nor77 nor
.model nor78 nor
.model nor79 nor
.model nor80 nor
.model nor81 nor
.model nor82 nor
.model nor83 nor
.model nor84 nor
.model nor85 nor
.model nor86 nor
.model nor87 nor
.model nor88 nor
.model nor89 nor
.model nor90 nor
.model nor91 nor
.model nor92 nor
.model nor93 nor
.model nor94 nor
.model nor95 nor
.model nor96 nor
.model nor97 nor
.model nor98 nor
.model nor99 nor
.model nor100 nor

;oscillator
.model osc01 lora: 0 1 0 2*mt 0 mrt 2*mt
.model osc02 lora: 0 1 0 1.953125us 0 0.9765625us 1.953125us

osc1 al osc01
buf1 osc al buf01

;transmitting clock
.model tclk lora: 0 1 0 62.5us 0us 30.2734375us 31.5us 61.5234375us 62.5us

tclk1 al tclk
buf2 tclk al buf01

;analog front-end of the receiver with pn-sequence generator.
.model front lgnd: model=1 par1=10 par2=28000. par3=4000 8
par4=0.5774 par5=0.5774 par6=1.
b1b1 tunc rdata rdata osc tclk front

;synchronized positive/negative edge detector of raw data
dff1 n1 n1b osc rdata dff1
del1 n1d n1 del01
dff2 n2 n2b osc n1d dff2
nrc1 edge n1b n2 nrc01

;zero-reset random-walk filter
.model rrwf lgnd: model=2 par1=8
b1b2 ADO DEL gated d1oclk rrwf

;digital voltage-controlled oscillator
.model dvco lgnd: model=3 par1=64 par2=0
b1b3 loclk rclk osc ADO DEL dvco
nan1 rclk rclk rclk rclk nan01

;90 degree refclk delay
dff3 d1oclk d1oclk rclk loclk dff3

;steering (windowing) circuit
nan2 h1 loclk edge nan02
inv1 gated h1 inv01

;manchester code decoder
nan3 rwnrs rdata rclk nan01

;integrate and dump filter
.model idf lgnd: model=5 par1=0.0375
b1b5 rwnrs osc rclk rwnrs idf

;bit error detector
.model ber lgnd: model=7 par1=2.9e-03
b1b7 tunc rdata edge loclk rclk rclk tunc rwnrs ber

;data strobe
del2 h1d rclk del01
inv2 h1d h1d inv02
and1 strobe h1d rclk and01

;1/(32*data rate) = 2*mt
time 0.9765625us 1000us
plot tunc rdata edge loclk rclk rclk d1oclk gated rwnrs rwnrs

state
go
end

```

Table 3-5: Source Deck Description of the Baseband Demodulator

Figure 3-25: SPLICE Models of the Baseband Demodulator

Figure 3-25: SPLICE Models of the Baseband Demodulator

Figure 3-26. Simulation of the Baseband Demodulator

disagreement is partly due to the inclusion of the receiver clock jitter and the non-constant time delay of the band-pass filter. Both factors were not considered in the Pawula's BER evaluations [34].

Figure 3-27: BER vs. SNR of the Baseband Demodulator

3.5 Summary

This chapter has presented the baseband demodulator system and the timing recovery circuit of the demodulator which was used as a pilot project for I.C. implementation. The reason for selecting this project is that it satisfies the requirements for mixed analog/digital system integration. Having introduced the demodulator to be implemented, the system configuration was finalized and system requirements were determined. From the high-level system requirements, a detailed functional block diagram of the system was determined. The integrity of the timing recovery circuit and the overall baseband demodulator had been verified with an high-level simulator, SPLICE. The following chapter will present the circuit design of the timing recovery circuit and the I.C. layout of the DPLL test chip and the baseband demodulator.

Chapter 4

CIRCUIT DESIGN AND LAYOUT

4.1 Introduction

The first three stages of the I.C. design methodology have been completed. The next step is the circuit design of each functional block of the timing recovery circuit. The design of the timing recovery circuit is based on a digital phase-locked loop (DPLL) circuit. Once the circuits have been designed and simulated, the DPLL chips floor plans and layouts may proceed. This is followed by verification and simulation of the DPLL chip layouts. Then, the analog circuit layouts and digital circuit layouts are integrated to realize the baseband demodulator. This will complete the implementation of the mixed analog/digital baseband demodulator and demonstrate the effectiveness of the I.C. design environment available at Carleton University.

4.2 Functional Block Design

This section will discuss the circuit design of the functional blocks in order to implement the DPLL of the timing recovery circuit. Functional block schematics will be presented along with simulation results in order to demonstrate the functionality of the circuits. The simulation results are obtained from a switch-level simulator called Hg which is available on the Metheus workstation.

4.2.1 Edge Detector

The function of this block is to sense the occurrence of polarity changes in the input signal. The input signal is sampled by the local oscillator so that the outputs of the edge detector would be in synchronization with the rest of the digital circuits. The sampled signal, $x_s(t)$, is delayed using a D-FF clocked by the local oscillator. Thus by exclusive ORing $x_s(t)$ and delayed $x_s(t)$, a pulse of a width equal to the local oscillator period is produced at all transitions of the input signal $x(t)$. The output of the XOR gate is labelled as "edges". A schematic for the hardware realization is shown in Fig. 4.1. Note that a

local buffer is inserted for the signal OSC to avoid race condition. An Hg simulation on the layout of this schematic is shown in Fig. 4.2. It clearly shows the correct functionality of the circuit block.

Figure 4-1: Edge Detector Schematic

Figure 4-2: Hg Simulation of the Edge Detector

4.2.2 Digital Controlled Oscillator

The digital controlled oscillator (DCO) is a frequency source whose phase can be controlled discretely by the random walk filter (RWF). The schematic of the DCO is shown in Fig. 4.3.a. This type of DCO is called increment-decrement (ID) controller. The operation of the ID controller follows the waveforms shown in Fig. 4.3.b. In the absence of ADD and DEL pulses, the ID controller divides the input frequency by a factor of 2. That is SW1 and SW3 are open and SW2 is closed. When ADD is "HIGH", SW1 is closed while SW2 and SW3 are open. The output of the controller is the inverted waveform of the input frequency. When DEL is "HIGH", SW3 is closed and the other switches are open. The output of the controller is set "LOW". The switches, SW1 to SW3, are realized with a pair of nMOS and pMOS transistors.

By synchronizing the ADD and DEL pulses from the RWF as shown in Fig. 4.3.b, the phase of the DCO output can be varied with a phase step $\Delta = 360^\circ/L$ where L is the parameter of the scaler at the output of the controller. The timing of the switches, SW1 to SW3, needs to be synchronized in such a way that no glitches are generated when the switches are turning ON and OFF. This condition is ensured by switching the switches during the instance that all the input nodes and the common output node are at the same logic state. The timing diagram of the DCO circuit is shown in Fig. 4.4.

It shows that the ADD/DEL pulse changes state when master clock, OSC, and the common output node of the switches are "LOW". This is accomplished by the D-FF delay to produce OSC (τ_{D-FF1}), the inverter delay to produce $\overline{OSC}$ (τ_{inv2}), and the D-FF delay to produce ADD or DEL pulses (τ_{D-FF2}). This timing scheme is physical layout sensitive because if, for example, $\tau_{inv1} = \tau_{D-FF1} + \tau_{inv2} + \tau_{D-FF2}$, the condition of all the nodes are at "LOW" state will not be satisfied. Therefore, special attention needs to be made on the loading of all signals during the physical layout of the DCO. An Hg simulation of the DCO layout is shown in Fig. 4.5.

For a layout insensitive timing scheme, a D-FF triggered by a clock at a frequency twice that of the master clock is placed at the common output node of the switches to retime the output signal. A schematic diagram and its corresponding waveform is shown in Fig. 4.6. Note that D-FF3 is triggered on the negative edge of inclk. This is when the output nodes of the switches is stable and free of glitches. Such layout insensitive circuit is necessary

(a)

RWF = Random Walk Filter

(b)

Figure 4-3: DCO Realization and its Waveforms

Figure 4-4: AC Timing Diagram of the DCO Circuit

Figure 4-5: Hg Simulation of the DCO Circuit

when the circuit is to be laid-out by an auto-place-and-route I.C. tool.

4.2.3 Phase Detector and Random Walk Filter

The phase detector (PD) determines whether the zero-crossings of the input signal, "edges", are leading or lagging the local 16 KHz clock. Random walk filter (RWF) is used to average out the number of LEAD and LAG decisions. The PD and the RWF are realized with a resettable 8-bit UP/DOWN counter as shown in Fig. 4-7. The local 16 KHz clock is fed to the U/D input of the counter. Depending on the logic state present at the U/D input, the contents of the counter change at the positive-edge of the "edges" pulses. The bit-cell schematics to implement an n-bit UP/DOWN counter are shown in Fig. 4-8.

Figure 4-7: PD and RWF Realization

An 8-bit decoder is used at the output of the 8-bit counter to detect the upper-limit, $+N$, and the lower limit, $-N$. The lock-in time of the DPLL is controllable as either high speed or low-speed as discussed in previous chapter. Therefore, four 8-bit decoders are required to detect $+N_1$, $+N_2$, $-N_1$, and $-N_2$ where $|N_1|$ is the limit for high-speed and $|N_2|$ is the limit for low-speed. Which outputs of the four decoders are to be used as the ADD and DEL command signals is controlled by setting DPLLC input "HIGH" for high speed and "LOW" for low-speed. To acquire more informations about the DPLL characteristics, two chips, TIMREC1 and TIMREC2, were designed with different N_1 's and N_2 's. TIMREC1 has $N_1=2$ and $N_2=127$; and TIMREC2 has $N_1=8$ and $N_2=32$. The 8 bit decoder addresses for $\pm N_1$ and $\pm N_2$ are:

Figure 4-6: Modified DCO Realization and its Waveforms

(a) Bit-Cell for the LSB of the Up/Down Counter

(b) Bit-Cell for the n-th bit for $n \geq 1$

(c) Connection of Bit-Cells to Realize an n th Bit U/D Counter

Figure 4-8: Bit-Cells of the Up/Down Counter

$+N1 = +2$	$A_7 A_6 \bar{A}_5 \bar{A}_4 A_3 \bar{A}_2 A_1 \bar{A}_0$
$-N1 = -2$	$A_7 A_6 A_5 A_4 A_3 A_2 A_1 \bar{A}_0$
$+N2 = +127$	$\bar{A}_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$
$-N2 = -127$	$A_7 \bar{A}_6 \bar{A}_5 \bar{A}_4 \bar{A}_3 \bar{A}_2 \bar{A}_1 \bar{A}_0$
$+N1 = +8$	$\bar{A}_7 \bar{A}_6 \bar{A}_5 \bar{A}_4 A_3 \bar{A}_2 A_1 \bar{A}_0$
$-N1 = -8$	$A_7 A_6 A_5 A_4 A_3 \bar{A}_2 \bar{A}_1 \bar{A}_0$
$+N2 = +32$	$\bar{A}_7 \bar{A}_6 A_5 \bar{A}_4 \bar{A}_3 \bar{A}_2 A_1 \bar{A}_0$
$-N2 = -32$	$A_7 A_6 A_5 \bar{A}_4 \bar{A}_3 \bar{A}_2 A_1 \bar{A}_0$

The 8-bit decoder is implemented with two 4-input NAND gates and one 2-input NOR gate. The combination of three gates are used instead of one 8-input AND gate is due to the fact that the three gates combination has a faster decoding speed than the 8-input AND gate. The decoding speed places a constraint on the maximum input frequency at which the DPLL is still able to phase-lock.

Recall that the outputs of the RWF, ADD and DEL pulses, need to be synchronized with the local oscillator clock, as shown in Fig. 4.3.b., so that pulse addition/subtraction of the DCO can operate correctly. Also if DPLLC was "LOW" initially and then set to "HIGH", the initial content of the counter $|N|$ could be greater than $N1$. Therefore, if DPLLC changes from 0 to 1, the counter should be reset to 0. This reset operation is not necessary for DPLLC going from 1 to 0 because $N1 < N2$. A complete schematic of the PD and RWF which performs the operations described above is shown in Fig. 4.9

An Hg simulation of the PD and RWF layout is shown in Fig. 4.10-11. The simulation was performed with $N=2$ and $L=32$. Figure 4.10 is for the case when "edges" lead the local clock. Figure 4.11 is for the case when "edges" lag the local clock. Note that the ADD and DEL pulses are generated as required in Fig. 4.4b; and the counter is reset to restart the cycle.

4.2.4 Divide-By L Scaler

Since the parameter L of the divide-by L scaler is of base-2, an n -bit binary counter can be used to realize the the scaler. The scaler can be implemented by either an n -stage ripple counter or an n -bit synchronous counter. Synchronous counters are distinguished from

Figure 4-9: Schematic of the PD and RWF Circuit

Figure 4-10: Hg Simulation of the PD and RWF Circuit

Figure 4-11: Hg Simulation of the PD and RWF Circuit

ripple counters in that clock pulses are applied to the "clock pulse" inputs of all flip-flops. The common clock triggers all the flip-flops simultaneously rather than one at a time in successive stages as in a ripple counter. This is advantageous for the DPLL design because excessive delay between the OSC signal and the 16 KHz clocks introduces additional phase error. Thus the synchronous counter realization for the divide-by L scaler was chosen. The bit-cell schematic of the counter is shown in Fig. 4.12. Since L is to be selectable as either 32 or 64, 6 bit-cells are thus required.

4.2.5 Data Strobe Generator and Data Sampler

The function of the data strobe generator is to generate a pulse at the start of each cycle of the local 16 KHz clock. This pulse is used as a triggering pulse for the D-FF to hold the estimated data present at the output of the integrate-and-dump circuit. This pulse is also used as a control signal for the integrate-and-dump circuit to restart its integrating cycle. The schematic of the data strobe generator and its corresponding waveform are shown in Fig. 4.13.

Figure 4-13: Data Strobe Generator

4.3 Layout of Digital Phase-Locked Loop Chips

Once all the functional block schematics of the DPLL have been designed and simulated, a rough area estimate can be made for the chip and a chip floor plan may be attempted.

For the LSB, $n = 0$, set $A(-1) = "1"$.

(a) Bit-Cell for the n-th Bit

(b) Connection of Bit-Cells to Realize an n-th Bit Counter

Figure 4-12: Bit-Cell of the Synchronous Binary Counter

Each functional block was designed and laid out using the Carleton CMOS3 Standard Cells. A physical layout extractor "phlex" was performed for each functional block to create a simulation netlist. Circuit simulations using Hg were then done on the layouts. Once the functional blocks were laid out and simulated, a floor plan for the DPLL chips could be made. At this stage, the buffering of critical signals is also considered.

When a CMOS gate is driving another nearby logic gate, there is little one can do to improve the delay other than sizing the transistors and manipulating the layout. However, for large fanout conditions in which small drive transistors must drive a very large capacitance, there is a need for circuit creativity. Under such situations, it is appropriate to put stages of buffering between the drive devices and the load [37]. When multiple loads are involved, multiple buffering can be used to optimize each path separately [38]. Both techniques are illustrated in Fig. 4.14.a and Fig. 4.14.b, respectively. The signals that will encounter heavy loading are OSC, the system clock, and "edges", the signal that drives the RWF. The signal OSC is distributed throughout the chip; and the technique of multiple buffering is employed for this signal. The buffering scheme for OSC is shown in Fig. 4.15. The signal "edges" has to drive the clock input of eight flip-flops of the 8-bit counter. Thus, high-power drivers are used to generate edges and edges signals.

Since two chips are to be designed, two layout schemes have been devised. TIMREC1 is laid out with all the functional blocks connected internal to the chip. TIMREC2 is laid out with the functional blocks to be connected external to the chip. This arrangement allows testing of each functional block in the event that one of the blocks fails to function. The floor plans for the timing recovery chips are shown in Fig. 4.16.

All the functional blocks, on chip buffers, and input/output pads are shown. Once the floor plan is completed, the interconnects among various functional blocks may be laid out, followed by the layout of interconnects between input/output pads and internal circuitry. Metal-2 is strictly used to connect pads to internal circuitry. Metal-1 is used to supply power to all functional blocks without encountering any metal or polysilicon underpasses. The layouts of TIMREC1 and TIMREC2 chips are shown in Fig. 4.17. Once the layout has been completed, the design is DRC'ed on the Metheus to ensure no layout rule violations exist.

Following chip layout, physical layout extraction was performed on the complete chip,

(a) Staged Buffering Scheme

(b) Multiple Buffering Scheme

Figure 4-14: Buffering for Large Fanouts Circuits

Figure 4-15: Buffering Scheme for OSC Signal

including the input/output pads, to verify the correctness of all interconnects. Hg simulation was also performed to predict the expected performance of the chips. Figure 4.18 shows the operation of the DPLL for the cases when the "edges" pulses lag and lead the local clock, "loc-clk". Note that it takes two "edges" pulses to generate an ADD or a DEL pulse; and an appropriate pulse is added or deleted at the output of the DCO.

Next, the maximum OSC frequency at which the chip can operate is predicted. The actual operating maximum frequency and the simulated maximum frequency will be compared to demonstrate the effectiveness of Hg to simulate the entire chip. The limiting factor is time delay to generate an AB or DB output following the positive-edge of the local oscillator clock (OSC). The timing of this operation is shown in Fig. 4.19. AB or DB must be low τ_{setup} sec. before the negative-edge of OSC, where τ_{setup} is the data setup time of the D-FFs. In order to generate ADD and DEL pulses, the following criterion must be satisfied,

$$\tau_{min} \geq \tau_{decode} + \tau_{setup}$$

Figure 4-16: Floor Plans of the Timing Recovery Chips

Figure 4-17: Layouts of the Timing Recovery Chips

Figure 4-18: Hg Simulation of the Timing Recovery Chip

From the Hg simulation, $\tau_{decode} \approx 85ns$. Since $\tau_{setup} \approx 10ns$, then

$$\tau_{min} \geq 100ns$$

conservatively. Therefore the maximum OSC frequency is 5 MHz or the maximum master clock frequency 10 MHz, and the expected maximum data rate at which the TIMREC chips can operate is ≈ 150 Kbits per second.

Once the overall chip simulation has been completed, the layout is converted to CIF using the command "phl2cif". The CIF file is then copied onto magnetic tape using "tar" command and sent to CMC so that its DRC tool, DRACULA, may perform on the chip. This is necessary because the DRC tool on Metheus does not check all the design rules. Once all errors were corrected, the final CIF file was sent to CMC for implementation. It took 3 to 4 months for the fabricated chips to return. Meanwhile test beds were designed awaiting the returning chips

4.4 Integration of the Baseband Demodulator Chip

The implementation of baseband demodulator primarily proceeds through two design

$\tau_{D\text{-FF}}$ = prop delay of D-FF
 τ_{decode} = prop delay of AB or DB from OSC
 $\tau_{\text{set-up}}$ = set-up time of the D-FF

Figure 4-19: AC Timing Diagram of AB and DB Generation

stages. First the digital timing recovery circuits and the analog circuits [23] were designed as separate chips. The chips were individually tested so that any design faults that existed could be readily located. Once the integrity of the circuit designs has been verified, the integration of digital and analog circuits then commences. Figure 4.20 shows a functional block diagram of the single chip demodulator.

The main circuits, such as BPF, slicer, I-and-D, data strobe generator, and timing recovery circuit are all implemented onto the chip. An effective testing scheme is required for achieving a testable chip. The partitioning testing technique [39] [40] is used as the testing method for the demodulator chip. This is a "Divide and Conquer" method in which the system is partitioned into two or more subcircuits so that it will be possible to test each subcircuit exhaustively. Access to embedded inputs and outputs of the subcircuits under test can be achieved by inserting multiplexers and connecting the embedded inputs/outputs of each circuits to I/O pads. The test circuit is indicated by a dotted line in Fig. 4.20. By applying "1" or "0" to the test pin, the BPF, slicer, I-and-D, and the timing recovery circuit can be tested individually. The multiplexer switches are realized with analog CMOS passgates.

The analog circuits of the demodulator are extremely sensitive to circuit noise. In particular by noise that is injected from the power-supply lines, ground, and clock lines. This is especially important when the I.C. contains both digital and analog circuits. The power supply and ground lines for digital and analog circuits are formed separately in order to protect analog signals from coupling noise which are induced from digital circuits. As shown in Fig. 4.21.a, the current through the common metalization resistance R_W is $i_a + i_d$ where $R_W = R_{W1} + R_{W2}$ and i_a and i_d are supply current for analog and digital circuits, respectively. Thus the voltage between node AB is $V_{AB} = V_{pad} - R_W(i_a + i_d)$. The current i_d contains large spikes due to the switching transient of digital circuits. The supply voltage of analog circuits are subjected to recurring voltage spikes. To reduce the effects of digital noise coupled through common resistance, star-connection and the use of separate power and ground pads, as shown in Fig. 4.21.b, are exercised in the layout.

Another important noise source is digital noise coupling from the substrate. P+ diffusion nodes of CMOS digital circuit, e.g. drains of pMOS transistors, may rise beyond the potential VDD during switching transients. Since the n-type substrate is biased at Vdd, a P+ diffusion at a potential higher than Vdd will inject minority carriers (holes) into the

Figure 4-20: Functional Block Diagram of the Demodulator Chip

R_{w1a} , R_{w1d} = metalization resistance from Vdd pad to analog and digital circuits, respectively
 R_{w2a} , R_{w2d} = metalization resistance from Vss pad to analog and digital circuits, respectively

Figure 4-21: Power Distribution for Mixed Analog/Digital I.C.

substrate. A guard structure which surrounds the analog circuits as shown in Fig. 4.22 helps to attenuate minority carriers from reaching the sensitive analog circuits. A collector guard structure which is based on the design of a lateral p-n-p transistor is shown in Fig. 4.23.a. The emitters are the digital P+ nodes which are likely to rise beyond Vdd. The P-well serves as the p-type collector. The n-substrate is the parasitic base of the lateral p-n-p transistor biased at Vdd. It is desirable to have the substrate biasing structure running in parallel with the P-well, as shown in Fig. 4.23.b, to keep the substrate biased solidly at Vdd potential. Thus minority carriers injected by the P+ emitter are intercepted by the P-well collector before they reach the analog circuits. The guard structure should also have many contacts connected to the substrate as well as the P-well to achieve an equal potential along the structure.

Figure 4-22: Analog Circuit Guard Ring Structure

The demodulator was laid out on a 30-pin pad-frame. The floor plan of the chip is shown in Fig. 4.24 and a plot of the layout is shown in Fig. 4.25. The chip area is 4.5 mm x 2.2 mm.

4.5 Summary

This chapter has presented the final stages of the I.C. design methodology, transforming

(a) Cross-Sectional View

(b) Top View

Figure 4-23: Guard Ring Structure

Figure 4-24: Floor Plan of the Demodulator Chip

2 of/de 2

MicroD

Figure 4-25: Layout of the Demodulator Chip

a functional block diagram to a chip layout. Two timing recovery chips, each has different loop parameters, were designed and implemented. The integration of analog and digital circuits has also been described.

Chapter 5

TEST RESULTS

5.1 Introduction

This chapter will discuss the test results obtained from the chips which were designed and fabricated during the course of the thesis work. In the first section, test results of the standard-cell test chip are presented. Results obtained from this chip will help to characterize the Northern Telecom's CMOS3 process. The second section will discuss the test results obtained from the timing recovery circuit chips.

5.2 Standard-Cell Test Chip Results

The goal of designing this chip is to verify the functionality of the primitive gates and input/output pads, and to compare the simulated propagation delays with those measured. Cells contained on the standard-cell test chip are: inverters, 2-input NANDs, 2-input NORs, D-FFs with reset, D-FFs with set and reset, pass-gates, 2-input XORs, 2-input XNORs, and Input/Output pads. Propagation delays of primitive logic gates (minimum size inverter, 2-input NAND, 2-input NOR) are obtained by connecting the gates in a ring oscillator structure as shown in Fig. 5.1.

The length of the ring oscillator is 25 inverting gates. Two identical rings of the same gate but with different fanouts are implemented to obtain propagation delays as a function of fanouts. The first ring has a fanout of one; and the second one has a fanout of five. Propagation delay is determined by

$$\tau_{delay} = \frac{1}{f_{osc}} \frac{1}{2} \frac{1}{25} \quad (5.1)$$

where f_{osc} is the oscillation frequency of the ring under test. Oscilloscope traces of the inverter, 2-input NAND, and 2-input NOR ring oscillator outputs are shown in Fig. 5.2.a, Fig. 5.2.b, and Fig. 5.2.c respectively. The oscilloscope traces appear to be contaminated

Two identical ring oscillators were designed for each gate type. The first ring does not have the capacitor "C" connected; the other one does. Capacitor "C" is equivalent to four fanout units.

Figure 5-1: Ring Oscillator Structure

with noise. This is due to the signal sampling circuitry of the oscilloscope which outputs data to the plotter.

The measured propagation delays are tabulated in Table 5.1. Figure 5.3 shows the simulated and measured propagation delays as a function of fanout for the primitive gates tested. Simulated propagation delay at one fanout has been normalized as one T_d unit in the graph. Ten standard-cell test chips were fabricated and tested. Based on the results obtained, the measured propagation delays are on the average 20% higher than the simulated results obtained from SPICE (LEVEL 2), and the deviation of the measured results among the ten chips tested varies by $\pm 10\%$ of the mean values.

Cell	Description	Fanout	Delay
CINV01	min. inverter	1	1.3 ns
CINV01	min. inverter	5	2.5 ns
CNAN02	2-input nand	1	1.6 ns
CNAN02	2-input nand	5	3.2 ns
CNOR02	2-input nor	1	1.9 ns
CNOR02	2-input nor	5	3.7 ns

1) the measured results are the average of the delays obtained from ten chips

2) $V_{dd} = 5V$

Table 5-1: Measured Propagation of Primitive Gates

The 20% difference between the simulated and measured results could be caused by the fact that the transistor models for simulation contain typical process values which are different from the actual values for the fabrication of the test chips. Another source of errors is in the estimation of routing capacitance at the output node of each gate. The edge capacitance of the routing was not included also. The $\pm 10\%$ deviation in the measured results between the ten test chips could be caused by variation in processing parameters

Figure 5-2: Oscilloscope Traces of the Ring Oscillators

Figure 5-3: Propagation Delays as a Function of Fanout

across the silicon wafer.

A 4-stage ripple counter as shown in Fig. 5.4 is used as the test circuit for the flip-flop cells. The counter is made up of JK-FF pre-cells and D-FF's. The CLK input is produced by a medium-power inverter cell (CINV03). The propagation delay is obtained by measuring the delay from A_0 to A_3 . Propagation delay from CLK input to Q is

$$\tau_{delay} = \frac{\text{Delay from } A_0 \text{ to } A_3}{3} \quad (5.2)$$

The estimated fanout of the Q output is 10. Two ripple counters were designed. The first counter was implemented using set/reset JK-FFs (CDFF04); and the second counter used reset JK-FFs (CDFF02). The set and reset inputs of the FFs were tested and found to be functional. The measured and simulated propagation delays are tabulated in Table 5.2. Both counters are operational at an input clock frequency of 25 MHz. Figure 5.5 shows the oscilloscope traces of the flip-flop A_0 output clocked by a 25 MHz input.

Figure 5-4: 4-Stage Ripple Counter

Other standard-cells which have been tested to be functional include exclusive-OR, exclusive-NOR, and passgates. Propagation delay (τ_{delay}) as a function of V_{dd} was also examined; and the results are shown in Table 5.3. The results indicate that τ_{delay} is inversely proportional to V_{dd} ; that is

$$\tau_{delay} \approx K \frac{1}{V_{dd}} \quad (5.3)$$

Measured and Simulated Propagation Delay (from CLK to Q) of D-FF

Cell	Description	Fanout	Delay (measured)	Delay (simulated)
CDFF02	D-FF w/ reset	10	7.2 ns	5.6 ns
CDFF04	D-FF w/ reset & set	10	8.1 ns	7.0 ns

1) the measured results are the average of the delays obtained from ten chips

2) $V_{dd} = 5V$

Table 5-2: Measured and Simulated Delays of D-FF

Figure 5-5: Oscilloscope Trace of Divide-by 2 Flip-flop

This is in agreement with the approximation for propagation delay given by [41] which states

$$\tau_{delay} \approx \frac{C_L}{V_{dd}} \left(\frac{1}{\beta_p} + \frac{1}{\beta_n} \right) \quad (5.4)$$

where C_L is the capacitance at the output and β_p and β_n are the transconductance gain of the pMOS and nMOS transistors respectively.

The ten standard-cell test chips were tested to be fully functional. Based on the above observations, the standard-cell designs proved to be successful and the cells display fairly

Vdd	delay	K = delay * Vdd
6.0 V	1.1 ns	6.6 V ns
5.5 V	1.2 ns	6.6 V ns
5.0 V	1.3 ns	6.5 V ns
4.5 V	1.4 ns	6.3 V ns
4.0 V	1.6 ns	6.4 V ns

Table 5-3: Propagation Delays of CINV01 as a Function of Vdd

good performance. The standard-cell test chip is a good indication that I.C. designs using the Carleton CMOS3 Standard-Cells have a very good chance of showing functionality.

5.3 Test Results of the Timing Recovery Chips

This section will discuss the test results obtained from the two timing recovery chips designed in Chapter 4. The chips are powered by a 5-V regulated power-supply. The timing recovery circuit's digital phase locked-loop (DPLL) parameters are as follows:

	TIMREC1	TIMREC2
L	32/64	32/64
N1	2	8
N2	127	32

Master Clock Frequency = 1.024 MHz for L = 32

Master Clock Frequency = 2.048 MHz for L = 64

Nominal DCO Free Running Frequency = 16 KHz

L is the divide-by L parameter of the digital controlled oscillator (DCO); and N1 and N2 are the lengths of the Random Walk Filter (RWF).

The bonding diagram and pin assignment of the timing recovery chips are outlined on Appendix C. The chips have been tested according to the following procedures.

5.3.1 DPLL Free Running Frequency f_o

The free running frequency of the DPLL is measured with the input signal pin connected to ground. That is, no phase correction commands are sent to the DCO. The test set-up is shown in Fig. 5.6. With the master clock frequency set at 1.024 MHz and L selected as 32, the free running frequency centers at 16.000 KHz. The same free running frequency was also observed for L=64 and master clock frequency=2.048 MHz. The spectrum of the DPLL's free running 16 KHz output is shown in Fig. 5.7.

Figure 5-7: Measured Spectral Density of Free-Running DPLL Output

5.3.2 Locking Range and Capture Range

The locking range is the range of frequencies, $(f_{lock(l)}, f_{lock(h)})$, over which the loop will remain lock. Usually the locking range is centered at the free running frequency; and the tracking bandwidth is defined as $f_{lock(h)} - f_{lock(l)}$. Capture range is the range of frequencies, $(f_{cap(l)}, f_{cap(h)})$, over which the loop can acquire lock. This range is also centered at the free running frequency; and the pull-in bandwidth is defined as $f_{cap(h)} - f_{cap(l)}$. The capture range can never exceed the locking range.

The test set-up for this experiment is shown in Fig. 5.8. A signal generator is applied to the DPLL's input pin. The locking range was measured by setting $f_1 = f_o$ initially, then slowly varying the input frequency f_1 and monitoring the upper and lower values of f_1 where

Frequency of master clock: 1.024 MHz for $L = 32$
 2.048 MHz for $L = 64$

L is the parameter of the divide-by- L scaler of the DCO

Figure 5-6: DPLL Free Running Frequency Test Set-Up

the system unlocks. In a similar way, the capture range was determined by first setting f_1 such that the loop is un-locked. Then f_1 was varied manually towards f_o . The upper and lower values of f_1 at which the system was locked were the upper and lower bounds of the capture range. Table 5.4 shows the measured and calculated tracking bandwidth and pull-in bandwidth for the DPLL designed.

N	L	Tracking (Hz)		Pull-in (Hz)	
		measured	calculated	measured	calculated
2	32	498	500	498	500
2	64	248	250	246	250
8	32	122	125	122	125
8	64	60	62	60	62
32	32	30	31	28	31
32	64	12	16	12	16
127	32	8	8	8	8
127	64	4	4	4	4

note: free running frequency is 16.000 KHz

Table 5-4: Tracking and Pull-in Bandwidths

The calculated values were obtained by the following equation:

$$B_o = \frac{2N}{T_c(N^2L^2 - 1)} \doteq \frac{2f_o}{NL} \quad (5.5)$$

where $f_o = 1/(T_cL)$ is the free running frequency. The difference between the calculated and measured results were $\leq 20\%$. The results also show that the tracking bandwidth equals the pull-in bandwidth for this particular type of DPLL; this is in agreement with the conclusion given in [31]. Since the tracking and pull-in bandwidth are equal, both will be referred to as tracking bandwidth. The results also indicate that the tracking bandwidth narrows as the RWF length (N) or the DCO scaler (L) increases.

5.3.3 Phase Jitter in the Presence of White Gaussian Noise

The unit in which jitter amplitudes are specified depends mainly on convenience and personal choices. Jitter amplitudes can be in units of absolute time, or in terms of parts of a unit interval expressed as a fraction or a percentage, or a phase in degrees. For example, a jitter amplitude of 0.01 ms of a 1 KHz timing signal is equivalent to a jitter amplitude of 0.01 unit interval, 1%, or 3.6° . The phase jitter in this thesis will be expressed in units of degrees.

The experimental set-up for timing jitter measurements is shown in Fig. 5.9

The input signal of the DPLL is assumed to be a 101010... binary Manchester sequence of 16.000 Kbits/s which is equivalent to a 8.000 KHz 50% duty cycle square wave. The square wave was contaminated with band-limited White Gaussian noise. The circuit for generating the square wave with noise is shown in Fig. 5.10. Figure 5.11 shows the spectrum of the input signal at different signal-to-noise ratios (E_b/N_o).

The measurement of the recovered clock mean-absolute phase jitter was carried out as follows:

- 1) The recovered clock is first "exclusive-ORed" with the reference 16 KHz signal, *refclk*.
- 2) The output of the XOR is low-passed filtered. The filtered output is a function of the mean phase jitter given by

$$V_n(t) = \frac{V_p}{\pi} \theta_n(t) \quad (5.6)$$

where V_p is the potential difference between the XOR logic levels and $\theta_n(t)$ is the mean-absolute phase jitter component.

The measured mean-absolute phase jitter as a function of E_b/N_o is shown in Fig. 5.12. The computed phase jitter for $N=2$ given by [30] is also shown for comparison. Note that, as E_b/N_o increases, the phase jitter approaches a constant value, approximately 5.6° for $L=32$ and 2.8° for $L=64$. This is explained by the intrinsic phase jitter of the DPLL discussed in Chapter 3,

$$| \text{phasejitter} |_{\min} = \frac{\Delta}{2} \quad (5.7)$$

where $\Delta = 360^\circ/L$. The results also indicate that the DPLL with $N=127$ has a better ability to suppress phase jitter than the one with $N=2$ at low E_b/N_o . The spectra of the recovered clock output for different loop parameters and E_b/N_o values are shown in Fig.

Frequency of master clock: 1.024 MHz for $L = 32$
2.048 MHz for $L = 64$

L is the parameter of the divide-by- L scaler of the DCO

Figure 5-9: Timing Phase Jitter Test Set-Up

$K = 16$ for master clock frequency 1.024 MHz
 $K = 32$ for master clock frequency 2.048 MHz

Figure 5-10: DPLL Test Input Signal Set-up

Figure 5-11: Spectrum of the Input Signal at Different SNR

5.13.a-f.

As expected, there is no significant changes in the shape of the spectra for $N=127$ as E_b/N_o decreases. However, for $N=2$, the noise components increase as E_b/N_o decreases. Also, the spectrum for $N=2$ at high E_b/N_o clearly displays the characteristics of a DPLL using a random walk filter (RWF). The frequency spikes about the free-running frequency is due to the filtering operation of the RWF and the discrete phase correction of the digital-controlled oscillator. Similar spikes can also be observed in the spectra for $N=127$. However, they are very closely spaced. Detailed description for the existence of these frequency spikes can be found in Appendix E.

5.3.4 Loop Transient Response to a Phase Step

In the absence of frequency offset, the loop response to a phase step is affected by the data transition counts, which is the number of LAG/LEAD decisions. In this section, the loop transient response to a phase step is examined. The experimental set-up is shown in Fig. 5.14.

The outputs from the HP8180A data generator are shown in Fig. 5.15. The output data is arranged in such a way that a 180° phase step is present at the start of each period T_p . Duration of the period T_p is made to be greater than the calculated pull-in time of the DPLL for a 180° phase step. The pull-in time is the transient time for a free-running loop to lock; and it can be estimated using the following equation:

$$\varphi = \frac{K_\varphi T_c}{N} \quad (5.8)$$

where φ is the initial phase misalignment and K_φ is the number of phase detections required to shift the output phase from φ to 0. The "exclusive-ORed" output was low-passed filtered to illustrate the diminishing phase error more clearly. The oscilloscope traces of the "exclusive-ORed" output and its filtered output for different loop parameters are shown in Fig. 5.16.a-d.

The pull-in time of the DPLL is the time for the filtered "exclusive-ORed" output to reach approximately zero volts. The calculated and measured pull-in times for 180° phase step are tabulated in Table 5.5. The results denote that the pull-in time is inversely proportional to the loop filter bandwidth because pull-in time decreases for small N and L .

Figure 5-12: Measured Mean-Absolute Phase Jitter of the DPLL

$N = 2, L = 32$
 $E_b / N_0 = 12\text{dB}$

a

$N = 2, L = 32$
 $E_b / N_0 = 24\text{ dB}$

b

$N = 2, L = 32$
 $E_b / N_0 = 65\text{ dB}$

c

Figure 5-13: Spectra of the Recoved Clock Output

d

$N = 127, L = 32$
 $E_b / N_0 = 12\text{dB}$

e

$N = 127, L = 32$
 $E_b / N_0 = 24\text{dB}$

f

$N = 127, L = 32$
 $E_b / N_0 = 65\text{dB}$

Frequency of master clock: 1.024 MHz for L = 32
2.048 MHz for L = 64

L is the parameter of the divide-by-L scaler of the DCO

Figure 5-14: Loop Transient Response to Phase Step Test Set-Up

Figure 5-15: Data Output from HP8180A for Transient Response Measurement

5.3.5 Timing Jitter in the Presence of Frequency Deviation

This section investigates the output phase jitter resulting from a difference in frequency between the input signal clock and the free running clock of the DPLL. The test set-up is shown in Fig. 5.17. The free running frequency, f_o , is fixed at 16 KHz and the input frequency, f_1 , is varied. Figure 5.18 shows a plot of the mean output phase jitter as a function of K where K is defined as

$$K = 2 \frac{f_o - f_1}{f_o}. \quad (5.9)$$

The two dotted-lines about the zero axis are the limits of the locking range of the DPLL.

5.3.6 Maximum Operating Clock Frequency

In section 4.3, the maximum clock frequency at which the chip can operate is predicted

(a) Loop Transient Response to a Phase Step
Initial Phase = 180 deg., $N = 2$, $L = 32$

(b) Loop Transient Response to a Phase Step
Initial Phase = 180 deg., $N = 2$, $L = 64$

Figure 5-16: Loop Transient Response to Phase Step

(c) Loop Transient Response to a Phase Step
Initial Phase = 180 deg., $N = 8$, $L = 32$

(d) Loop Transient Response to a Phase Step
Initial Phase = 180 deg., $N = 8$, $L = 64$

N	L	pull-in time	
		measured	calculated
2	32	2.0 ms	2.0 ms
2	64	4.1 ms	4.0 ms
8	32	8.2 ms	8.0 ms
8	64	16.2 ms	16.0 ms

Table 5-5: Pull-In Time for a 180 deg. Phase Step

using a switch-level simulator, Hg. Hg simulation results show that the maximum master clock frequency is 10 MHz.

The test set-up for maximum operating frequency is identical to that of the locking and capture range test set-up shown in Fig. 5.8. The test is performed with the input frequency to the DPLL, f_1 , equals to master clock frequency/32 or the free-running frequency, f_0 . The maximum master clock frequency at which the DPLL can operate is 8 MHz. That is, the DPLL can phase-lock to an input signal of 125 KHz. The Hg simulated maximum clock frequency is only 25% higher than the observed maximum clock frequency. This test has demonstrated that the Hg switch-level simulator gives very reliable simulation results of a chip's performance with an estimated 20 – 30% deviation from the actual results. The deviation is introduced because transistors are modeled as switches with corresponding "ON" resistance values. Also, the simulators underestimate the routing capacitance on the chip.

5.4 RWF-DPLL Applications

The results presented in the previous sections have demonstrated that the DPLL chips are fully functional. The results also show the change in the loop characteristics as the N-parameter of the RWF is varied. For low N-value, ($N=2$), the loop has wide tracking range, short pull-in time, and is capable to track reference signal of greater frequency deviation as compared to a loop with large N-value, ($N=127$). The observations listed above meet

Frequency of master clock: 1.024 MHz for $L = 32$
 2.048 MHz for $L = 64$
 L is the parameter of the divide-by- L scaler of the DCO

Figure 5-17: Timing Jitter due to Frequency Deviation Test Set-up

(a) Output Phase Jitter in the Presence of Freq. Deviation

(b) Output Phase Jitter in the Presence of Freq. Deviation

Figure 5-18: Output Phase jitter in the Presence of Frequency Deviation

the performance requirements of a loop that is suitable for lock acquisition as discussed in Chapter 3. For large N -value, the results display a loop that has narrow tracking bandwidth and low phase jitter at low E_b/N_o ratios. These characteristics describe a loop that is suitable to operate in the tracking mode. That is, a loop that suppresses phase transients during deep fading conditions. Thus, by detecting the absence and presence of received signals at the IF front-end, the loop characteristics can be changed by selecting small- N and large- N , respectively. During absence of received signal, the loop is operating in the acquisition mode so that it could lock onto the signal quickly once the signal is received. When the SNR of the received signal rises above a predefined threshold, the loop switches to the tracking mode. By that time the loop should have already locked onto the signal. If the SNR of the received signal drops below a predefined threshold for a certain length of time, thus indicating a loss of signal, the loop should switch to the acquisition mode in order to recover the signal. A method to implement the acquisition/tracking switching scheme can be found in [9].

The parameter L of the DCO should be selected base on the intrinsic mean-absolute phase jitter value of the loop that is acceptable to the system requirement. The intrinsic mean-absolute phase jitter is related to L by eqn. 5.7 shown in section 5.3.3.

5.5 Summary

The results obtained from the chips fabricated at Northern Telecom Ltd. through CMC were presented. The standard-cell test chip was tested and the standard-cells were found to be functional. A brief characterization of the CMOS3 process and the standard-cell library were presented. This chapter has also shown the success of designing complex digital I.C. using the methodology described in Chapter 2. The DPLL chips are found to be fully functional; and the measured results conform closely with the calculated results. The success of the chips has demonstrated the capability of the I.C. design environment to implement complex digital systems onto silicon.

The next chapter will summarize the design/implementation process of the DPLL chips carried out in the course of this thesis. Suggestions of future work will also be presented.

Chapter 6

CONCLUSIONS

6.1 Summary

The aim of this thesis is to design and implement the baseband demodulator of a mobile radio receiver onto a single I.C. Standard-cell design technique was chosen as the most suitable approach to design mixed analog/digital systems. The I.C. design was carried out based on a design methodology that would provide a high probability of success on the first iteration which was essential in I.C. design. The design methodology enables the designer to proceed in a step-by-step manner to accomplish the end product, a fully functional chip. The design method is particularly suited to the I.C. design CAD tools available at Carleton University.

High-level simulation and verification has been carried out for each of the functional blocks of the baseband demodulator. The structure of the system has also been simulated to verify the design of the system. In this design phase, the structure of the system and the input/output interfaces among the blocks were verified at the early stage of the design.

The functional blocks of the timing recovery circuit were designed using the Carleton CMOS3 Standard-Cell Library. The blocks were laid-out manually. A physical layout extractor was used to create simulation netlist from the layout so that an electrical simulation or a switch-level simulation could be performed on the layout. The layout of each functional block of the timing recovery circuit has been simulated and verified. In addition the layouts of the timing recovery chips, including the input/output pads, were simulated to verify the interconnects among the blocks and the pads. The timing recovery chips have been fabricated by Northern Telecom Ltd. through CMC.

Besides the timing recovery chips, a standard-cell test chip was also designed to characterize the performance of the Carleton CMOS3 standard-cells and to compare the simulated and measured results. The standard-cell test chip was also simulated to verify its design and layout.

The fabricated chips were tested upon receipt from CMC. Measured from the standard-cell test chip, the propagation delay of a standard inverter is 1.3 ns for a fanout of one with $V_{dd} = 5.0V$ and $V_{ss} = 0.0V$. The maximum toggling frequency of the D-FF is 25 MHz. The power dissipation of the primitive logic gates is $25\mu W/MHz$. All the circuitries on the standard-cell test chip were found to be functional.

For the two DPLL chips received from CMC, the tracking and pull-in bandwidths, phase jitter vs. input SNR, loop response to a phase step, and timing jitter in the presence of frequency deviation have been measured. The pull-in bandwidth is 500 Hz and the pull-in time is 2.0 ms when the DPLL is operating in the acquisition mode. The mean-absolute phase jitter of the DPLL in the tracking mode is 10 degrees at SNR=10dB. The experimental results conform closely with the theoretical/calculated results. The two DPLL chips designed were found to be fully functional and their performance met the design specifications. The good results also demonstrates the high probability of first time success of the design methodology proposed in Chapter 2.

An analog chip that contains the analog circuits of the baseband demodulator was designed by [23]. The circuits were designed with switched-capacitor techniques. This chip was also found to be fully functional and the tested results agreed with the simulated results.

The successful design of the 1500 transistors DPLL chips and the switched-capacitor analog chip designed by [23] indicate that if the design methodology is followed, complex mixed analog/digital systems can be integrated in the I.C. design environment of Carleton University.

6.2 Future Work

Now that the analog/digital functional blocks of the baseband demodulator have been successfully implemented, a mixed analog/digital baseband demodulator chip was implemented with the tested functional blocks. The design has been submitted to CMC for fabrication. Since the functional blocks were tested to be functional, the single chip design submitted will have a high probability of success.

Future work can be carried out in testing the single chip baseband demodulator. The bonding diagram and pin assignments are outlined in Appendix D.

Future work can also be performed in improving the BER of the demodulator by optimizing the filter specification of the band-pass filter. The BER performance is strongly influenced by the electrical characteristics of the BPF, the phase and frequency response of the filter. Thus the BER can be improved by selecting a higher order filter and/or filter type (Bessel instead of Butterworth).

Modifications can be made to the DPLL presented in this thesis to improve its tracking and acquisition behavior. Two additional phase comparators can be added along with an estimation-decision circuit to decide whether the DPLL should be either in acquisition or tracking mode. Details of this modified DPLL can be found in [42].

Since the standard-cell test chip has shown that the CMOS3 cells designed are fully functional and the successful timing recovery chip has demonstrated the effectiveness of the I.C. design methodology, Carleton University now has the fundamental components to implement VLSI chips. However, Carleton still requires further development in its I.C. design environment so that "WORK THE FIRST TIME" VLSI chips can be implemented successfully by a graduate student within six months, a typical master thesis research duration. Future work may be performed in setting up an auto-place-and-route I.C. package that supports the CMOS3 standard-cells developed during the course of this thesis. The new I.C. CAD tool, CADENCE tools, which Carleton has recently acquired, is a potential candidate for this project. Once the data base of the standard-cells is set-up on CADENCE, the designer is only required to enter the schematic of the system he wishes to implement using gate symbols that represent the cell and to simulate the design using performance parameters of the cells which are in the data base. The layout of the chip will be generated by CADENCE; and the design is then sent off to CMC for fabrication. Thus, the designer concentrates his work on designing and verifying his system; and leaves the error-prone layout work to the tools.

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Appendix A

Low-Drive Inverter

CARLETON VLVI
DESIGN CENTRE

CMOS3 LIBRARY

CINV01

DATE	1 MAY 1987	LOW POWER INVERTER
DIMENSIONS	45 X 14

TRUTH TABLE

IN	OUT
0	1
1	0

INPUT LOADING

NODE	IN
LOAD	1.0

DYNAMIC CHARACTERISTICS (INPUT R/T TIME = 3NS, VDD = 5.0 V @ 25C)

PARAMETER		FAN OUT LOAD = 1	FAN OUT LOAD = 10	UNIT
PROPAGATION DELAY (HL)	TPHL	0.6	1.7	NS
PROPAGATION DELAY (LH)	TPLH	1.3	3.5	NS
OUTPUT FALL TIME	TTRL	1.4	2.8	NS
OUTPUT RISE TIME	TTLH	1.9	6.6	NS

Appendix B

Filtered Phase Signal and Phase Noise Models

The development of the time domain simulation models for the phase signal and phase noise found in Manchester coded narrow-band digital FM with discriminator detection and a 2nd order low-pass filter is given in this appendix.

Filtered Phase Noise Development

Following Cartier, the assumption is made that only the two bits adjacent to the bit under consideration have any effect upon the bit since the transient response due to bits further away would have died out. Based on the above assumption, given a "0" for the bit under consideration, there are only four combinations which exist; 000, 001, 101, 100. These 3-bit patterns are used to derive the Fourier series of $\sin\theta(t)$ and $\cos\theta(t)$.

It has been shown that the optimum performance for Manchester coding is achieved with a time-bandwidth product $BT \approx 2$ and a deviation ratio ≈ 1 . These values are used to derive equations that describe the phase signal model.

Case I: All zeroes bit pattern "000"

In the case of "all zeroes" bit pattern, the data phase, $\theta(t)$, after FM demodulation is a triangular wave of a period T with zero mean value.

The Fourier Series of $\sin\theta(t)$ and $\cos\theta(t)$ are

$$\sin\theta(t) = \sum_{n=1}^{\infty} a_n \cos(2\pi n f_1 t) \quad (1)$$

and

$$\cos\theta(t) = A_o + \sum_{q=1}^{\infty} a_q \cos(2\pi q f_1 t) \quad (2)$$

where

$$a_n = \frac{4h}{\pi} \cos\left(\frac{\pi h}{2}\right) \frac{|\sin(\frac{n\pi}{2})|}{n^2 - h^2}$$

$$a_q = \frac{4h}{\pi} \sin\left(\frac{\pi h}{2}\right) \frac{|\cos(\frac{q\pi}{2})|}{q^2 - h^2}$$

$$A_o = \frac{\sin\left(\frac{\pi h}{2}\right)}{\frac{\pi h}{2}}$$

$$h = 2\pi f_d T \text{ and } f_1 = 1/T$$

Case II. Alternating "one-zero" bit pattern

In this case, the data phase signal, $\theta(t)$, after FM demodulation is a triangular wave of period $2T$ with zero mean value.

The Fourier series of $\sin\theta(t)$ and $\cos\theta(t)$ is the same as Case I with the exception of $f_1 = \frac{1}{2T}$.

Case III. "0011" bit pattern

Both the 001 and 100 bit patterns can be studied using the 0011 bit pattern.

The Fourier series of $\sin\theta(t)$ and $\cos\theta(t)$ are:

$$\sin\theta(t) = \sum_{n \text{ odd} > 0}^{\infty} a_n \sin(2\pi n f_1 t) \quad (3a)$$

$$\cos\theta(t) = A_o + \sum_{q \text{ even} > 0}^{\infty} a_q \cos(2\pi q f_1 t) \quad (3b)$$

where

$$a_n = \frac{4h}{\pi} \frac{4\cos\left(\frac{h\pi}{2}\right)\sin\left(\frac{n\pi}{2}\right)\cos\left(\frac{n\pi}{2}\right) - 2\sin\left(\frac{n\pi}{2}\right)}{n^2 - 4h^2}$$

$$a_q = -\frac{4h}{\pi} \frac{\sin\left(\frac{h\pi}{2}\right)\cos\left(\frac{q\pi}{2}\right)\cos\left(\frac{q\pi}{2}\right)}{q^2 - 4h^2}$$

$$A_o = \frac{\sin\left(\frac{h\pi}{2}\right)}{\frac{h\pi}{2}}$$

$$h = 2\pi f_d T \text{ and } f_1 = \frac{1}{4T}$$

The filtered phase signal may be well approximated by

$$\phi(t) = \tan^{-1} \frac{\sum_{n=1}^{\infty} (|H(nf_1)| a_n) \cos(2\pi n f_1 t + \angle H(nf_1))}{\sum_{q=1}^{\infty} (|H(qf_1)| a_q) \cos(2\pi q f_1 t + \angle H(qf_1)) + A_o |H(0)|} \quad (4)$$

for Case I and Case II; and for Case III

$$\phi(t) = \tan^{-1} \frac{\sum_{n=1}^{\infty} (|H(nf_1)| a_n) \sin(2\pi n f_1 t + \angle H(nf_1))}{\sum_{q=1}^{\infty} (|H(qf_1)| a_q) \cos(2\pi q f_1 t + \angle H(qf_1)) + A_0 |H(0)|} \quad (5)$$

By choosing an appropriate number of dominating Fourier coefficients, the filtered phase signal $\phi(t)$ may then be calculated in discrete time for each of the four bit patterns (000,001,101,100). The remaining four bit patterns (111,110,010,011) can be treated as (000,001,101,100) case with inverted phase.

Filtered Signal Phase Model Verification Results

Simulation results for the filtered phase signal at the output of the discriminator for cases I, II and III where "0" is the n^{th} bit under consideration is shown in Fig. B.1-4 (the IF filter used was a 2^{nd} order Gaussian filter).

It shows the waveform dependence on the number of Fourier coefficients. Figure B.5 shows the filtered phase signal waveform for an arbitrary Manchester coded data stream.

Figure B-5: Waveform of an Arbitrary Manchester Data Stream

It is therefore possible, for the purpose of time-domain simulations, to generate the filtered phase signal for Manchester coded data.

Figure B-1: Bit Pattern 000

Figure B-2: Bit Pattern 001

Figure B-3: Bit Pattern 101

Figure B-4: Bit Pattern 100

Phase Noise Model Development

The equation used to develop the noise model is given as

$$\eta(t) = \tan^{-1} \frac{\xi(t)}{\sqrt{2SNR} + \vartheta(t)}$$

which is similar to equation (5) with the exception that the SNR is assumed constant. where $\xi(t)$ and $\vartheta(t)$ are independent Gaussian variables with zero means, unit variance, and bandlimited to the IF bandwidth.

A Gaussian zero mean unity variance noise model has been developed and this model was used to generate the phase noise as follows. By generating noise at every $mrt=(1/32 T)$ in SPLICE, it gives a PSD bandlimited to $1/2mrt$, as shown in Fig. B.6, as opposed to the theoretical ∞ bandwidth.

Figure B-6: Zero-Mean Unit-Variance Noise Model Spectrum

The variance σ^2 is given as

$$\sigma_1^2 = B_{mrt} N_{01} \simeq 1.0$$

This noise is then passed through a LPF with a bandwidth equivalent to the IF bandwidth. The resulting PSD is shown in Fig. B.7.

The variance in this case is given as

$$\sigma_2^2 = B_{IF} N_{02} \neq 1.0$$

Figure B-7: Low-Passed Filtered Noise Spectrum

But what is required is a variance of unity which is not the case for Fig. B.7, so a scaling factor is needed to accomplish this. The scaling factor is determine as follows:

$$B_1 N_{o1} = B_2 N_{o2} = \sigma^2 \simeq 1.0$$

$$B_1 N_{o1} = B_2 N_{o2}$$

$$\frac{N_{o1}}{N_{o2}} = \frac{B_{IF}}{B_{mrt}}$$

where $B_{IF} = 1/T$ and $B_{mrt} = 1/(2t_s) \cdot t_s$ is the sampling rate.

$$N_{o2} = \frac{T}{2t_s} N_{o1}$$

Therefore, multiplying the output of the low-pass filter by a constant $T/2t_s$ will then give the required noise characteristics.

Appendix C

Timing Recovery Chips Bonding Diagram

CMC MULTIPROJECT BONDING DIAGRAM

RETIKLE CODE U26W

BRAND ID LABEL CV

OTHER IDENTIFICATION FEATURES _____

WAFER NUMBERS _____

DESIGN FILE REFERENCE TIMREC 1

PACKAGE	IDK40F1-192G	L10	C-493-175-35M
WIRE ALLOY	99% Al/1% Si	DIA.	.001"
	99% Al/1% Si	ELONG.	1.5 - 4%
			1.5 - 4%
		T.S.	14-16 gms
			18-22 gms
D/A PREFORM	ALLOY 98% Au/2% Si	RECOMMENDED SIZE	W/B METHOD U.S.

BONDING DIAGRAM

NOTES: 1. DIE ATTACH PAD SIZE: .400 X .400

2. ZERO GROUND

CIFZAP V1.2

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TIMREC1

PIN NUMBER	TYPE	DESCRIPTION
5	power	VSS
10	input (CMOS)	DPLLCB
11	power	VDD
16	input (CMOS)	MASTER CLOCK
17	output (CMOS)	OSC
18	output (CMOS)	MASTER CLK / 32
19	output (CMOS)	MASTER CLK / 64
20	input (CMOS)	U / DB OF U/D CNTR
21	input (CMOS)	Fa
22	output (CMOS)	Fa / 2
23	output (CMOS)	Fa / 4
24	input (CMOS)	selTRIG (set = 0)
25	input (CMOS)	INPUT
31	power	VSS
36	power	VDD

For L=32, connect (PIN18 to PIN21) and (PIN22 to PIN20)

For L=64, connect (PIN19 to PIN21) and (PIN22 to PIN20)

TIMREC2

PIN NUMBER	TYPE	DESCRIPTION
1	power	VDD
6	output (CMOS)	OSC
7	output (CMOS)	MASTER CLK / 64
8	output (CMOS)	MASTER CLK / 128
9	output (CMOS)	MASTER CLK / 256
10	input (CMOS)	Fa
11	input (CMOS)	U / DB OF U/D CNTR
12	input (CMOS)	selTRIG (set = 0)
13	output (CMOS)	WINDOW
14	output (CMOS)	EDGES
15	input (CMOS)	INPUT
20	power	VSS
21	output (CMOS)	TRIGBO
26	input (CMOS)	CLKB OF U/D CNTR
27	input (CMOS)	RESETB OF U/D CNTR
28	input (CMOS)	AtI
29	output (CMOS)	ADD+DEL
30	input (CMOS)	BuI
31	output (CMOS)	AtO
32	output (CMOS)	BrO
33	output (CMOS)	RESETB to U/D CNTR
34	output (CMOS)	resetB of DPLL reset
35	input (CMOS)	MASTER CLOCK
40	input (CMOS)	DPLLCB

For L=32, connect (PIN7 to PIN11) and (PIN7 to PIN10)

For L=64, connect (PIN8 to PIN11) and (PIN8 to PIN10)

Connect (PIN21 to PIN26), (PIN27 to PIN33), (PIN28 to PIN31),
and (PIN30 to PIN32)

Appendix D

Baseband Demodulator Chip Bonding Diagram

CIC MULTIPROJECT BONDING DIAGRAM

RETICLE CODE U292

BRAND ID LABEL TC3

OTHER IDENTIFICATION FEATURES CV040

WAFER NUMBERS _____

DESIGN FILE REFERENCE _____

PACKAGE		LID	
IDK40F1-192G		C-491-175-35M	
WIRE ALLOY	99% Al/1% Si	DIA.	.001"
	99% Al/1% Si		.00125"
ELONG.	1.5 - 4%	T.S.	14-16 pas
	1.5 - 4%		16-22 pas
D/A PREFORM	ALLOY 98% Au/2% Si	RECOMMENDED SIZE	W/B METHOD U.S.

BONDING DIAGRAM

NOTES: 1. DIE ATTACH PAD SIZE: .400 x .400

2. ZERO GROUND

CIFZAP V1.2

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PIN	TYPE	DESCRIPTION
1	ANALOG	LIMITER Vbias 1
2	ANALOG	LIMITER Vbias 2
3	power	DIGITAL VDD
6	CMOS (I)	DPLLCB
7	CMOS (I)	MASTER CLK
8	CMOS (O)	OSC
9		N / C
10	CMOS (O)	MASTER CLK / 64
11	CMOS (O)	MASTER CLK / 128
12	CMOS (I)	U / DB OF U/D CNTR
13	CMOS (I)	INPUT
14	power	DIGITAL VSS
15		N / C
18	ANALOG	Vbias 1 (OP-AMP)
19	ANALOG	Vbias 2 (OP-AMP)
20	ANALOG	Vbias 3 (OP-AMP)
21	ANALOG	Vbias 4 (OP-AMP)
22	ANALOG	ANALOG GND
23	power	ANALOG VDD
26	ANALOG	LP FILTER INPUT
27	ANALOG	LP FILTER OUTPUT
28	ANALOG	HP FILTER INPUT
29	ANALOG	HP FILTER OUTPUT
30	ANALOG	I / D INPUT
31	ANALOG	I / D OUTPUT
32	ANALOG	(PHI DUMP)
33	ANALOG	(PHI DUMP)B
34	ANALOG	SAMPLING CLOCK
35	ANALOG	LIMITER IN
38	CMOS (O)	LIMITER OUT
39	ANALOG	LIMITER Vref
40	power	ANALOG VSS

Appendix E

Detailed Analysis of the DPLL output Spectrum

In Fig. 5.13.c, the spectrum of the DPLL output for $N=2$ displays a presence of frequency spikes about the fundamental frequency, 16 KHz. Similar frequency spikes can also be observed in the spectrum for $N=127$. However, they are more closely spaced. The presence of these spikes are due to the operation of the digital filter, random-walk filter (RWF), and the operation of the digital-controlled oscillator (DCO). Detailed explanation of this class of DPLL can be found in section 3.3 of this thesis.

Having understood the operation of the DPLL, the output of the DPLL can then be examined. For simplicity, $N=2$ is chosen as the limit of the RWF and the loop is locked to the input signal.

When the loop is locked to the input signal, the minimum phase error is denoted by $\delta < \Delta/2$. where Δ is 360 degrees/ L and L is the scaler of the divide-by L .

Thus, the output of the DPLL is misaligned with the input signal with a phase error $< \Delta/2$. Since the DCO will advance or retard the local oscillator clock by Δ , the DPLL output will alternatively leads and then lags the input signal. Therefore, the phase detector will alternatively generate two LEAD pulses and then two LAG pulses (for $N=2$). This operation is depicted in the following diagram. The phase error has been exaggerated for easy observation.

The DPLL output contains three square wave signals of different period.

$$T1 = 1. / (\text{local oscillator frequency} / L) = 1. / 16 \text{ KHz}$$

$$T2 = T1 - a \quad \text{where } a = \Delta \times T1 / 360 \text{ deg.} = T1 / L$$

$$T3 = T1 + a$$

Thus, by analyzing the Fourier components of the above signal, one should arrive a spectrum which is identical to the ones displayed in Fig. 5.13.

As the signal to noise ratio (SNR) decreases, the pattern of T1 T2, and T3 becomes more random, unlike the pattern that is predictable as in the case of high SNR. This explain why the frequency spikes in Fig. 5.13.a,b were widened for low SNR.

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