Design, Analysis and Modeling of the Effect of the Phase Detector in Digital Phase-Locked Loops

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Abstract

The limitations and the effect of the performance of the binary phase detector on the overall performance of the digital phase-locked loop is the main focus of the research presented in this proposal. In the first part of the research, the gain limitation of the binary phase detector on the performance of the digital Bang-Bang phase-locked loop is investigated. Then to validate the concept that is explained and to improve the performance of the digital loop under the gain limitation, two schemes are explored and explained. In one scheme a random bit-stream which is noise-shaped using a software defined $\Sigma\Delta$ modulator is used to dither the reference and improve the performance and in the second scheme a Time-Amplifier is used to improve the digital loop performance by preventing the phase detector from operating in metastable region.

The second part of the research focuses on a novel multi-bit phase detector for high-speed applications where high-resolution performance is needed and the jitter budget is stringent. In this design a Transmission Delay Line is used to generate the delayed versions of the input clock. The performance of this phase detector is analyzed in detail using stochastic analysis.

In the second multi-bit phase detector a search algorithm is used to find

the closest delayed reference to the feedback clock. This scheme provides superior performance compared to the first scheme as its performance is not affected by the mismatch of the binary phase detectors used in the first scheme. The performance of the two design are compared and example of the performance in the loop is provided.

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Abbreviations

ADPLL All Digital Phase-Locked Loop

BBPLL Bang-Bang Phase-Locked Loop

BER Bit Error Rate

CDF Cumulative Distribution Function

CDR Clock and Data Recovery

CED Close Edge Detector

CML Current Mode Logic

CTDSA Cyclic Time Domain Successive Approximation

DAC Digital-to-Analog Converter

DCD Duty Cycle Distortion

DCO Digitally Controlled Oscillator

DLL Delay-Locked Loop

DNL Differential Non-Linearity

DTC Digital-to-Time Converter

INL Integral Non-Linearity

MUX Multiplexer

OSR Over Sampling Rate

PD Phase Detector

PDF Probability Density Function

PI Phase Interpolator

PLL Phase-Locked Loop

PVT Process Voltage and Temperature

SSC Spread Spectrum Clocking

TA Time Amplifier

TAPD Time-amplifier Assisted Phase Detector

TDC Time-to-Digital Converter

TDSA Time Domain Successive Approximation

TG Transmission Gate

VCO Voltage Controlled Oscillator

Chapter 1

Introduction

1.1 Why Digital Phase-Locked Loop?

With every new generation of the communication systems, the design challenges have kept increasing as the demand for speed increases while the power consumption and chip area has to be minimized. The communications systems include extensive digital signal processing which consume the majority of the power and area. Hence, the digital design indirectly dictates the process technology that is used to implement the system. As the need for digital signal processing grows, new technologies tend to accommodate dense digital circuits. These deep sub-micron technologies provide significant improvement in terms of speed, power and area. As a result, implementing the systems in sub-micron silicon technologies with nano-meter channel length such as 65nm, 32nm and beyond seems inevitable. Although these technologies prove to be very advantageous for digital circuit design, they put many constraints on analog circuit design. The challenges of designing analog cir-

cuitry are due to low power supply, high leakage, high threshold voltage which does not scale with the supply voltage and In Addition, the device random mismatch requires extra design effort to make sure the performance is not degraded. Since random mismatch is the result of physical imperfection during the process fabrication such as rough edges and impurities in the material, the sizing of this impurities could be comparable to the channel length of the sub-micron technologist, and hence their impact is greater in sub-micron technologies compared to long channel technologies. These factors drive analog designers to look for new ways of designing circuits to overcome the shortcomings of the sub-micron technologies.

One of the most important building blocks of any digital communication system is the phase-locked loop (PLL) that provides the system clock which makes transmitting and receiving the data possible. The conventional PLLs also known as analog PLLs have been used in almost all communication systems. Although these PLLs have excellent performance, designing them in new deep sub-micron technologies pose many challenges due to the characteristics of these technologies as mentioned above. For example, designing high complexity analog circuits such as charge pumps becomes more challenging. Also the use of large passive components in the loop filter of the PLLs, takes up a large area of the chip which can be costly or they require off-chip components which reduce the integration level of the chip.

In recent years All-Digital phase-locked loops (ADPLL) have raised interest in many applications such as wireline communications, Clock and Data Recovery (CDR), on-chip clock distribution and wireless communications due to their small area, better immunity to external noise, simplicity of the de-

sign, and portability and scalability with process technology. Also the digital nature of the loop eliminates the need for large on-chip and off-chip passive components which reduces the chip area significantly.

These properties of the ADPLLs have made these PLLs very attractive to the designers, however, the performance of the ADPLL typically falls short compared to the conventional analog PLLs. Hence, improvements at block level as well as system level must be undertaken while ensuring that requirement for phase noise, settling time, frequency lock range, phase resolution and power consumption are met.

Typically, calibration techniques are required to compensate for process, power-supply voltage, and temperature (PVT) variations and at the component level, each block must be designed for minimum non-ideality, mismatch and non-linearity.

The need to improve the performance of the ADPLLs has opened a new avenue in research both in industry and academia. The importance of these investigation lies in the fact that the present and the future communication systems are and will be implemented in deep sub-micron silicon process technologies with channel length as short as 14nm and beyond.

One of the most important properties of any PLL is the noise performance which is defined in form of phase noise. The noise performance of the PLL shows the ability of the PLL to reject the noise from internal device which are in form of thermal noise that modulates the output signal, and external noise which could be in form of jitter at reference clock and random noise or unwanted signal on the power supply. The noise performance of the ADPLLs is determined by the phase granularity and resolution, non-linearity in the

loop, and non-idealities of the loop components such as the phase detector (PD) and the oscillator. The objective of this research is to explore new design techniques to improve the ADPLL performance while maintaining its excellent qualities and advantages. The main focus will be on improving the noise performance of the high-speed ADPLLs by employing new techniques both at the system level and at the component level.

1.2 Motivation and Contributions

As mentioned in the previous section, portability and scalability of the digital PLL are the main factors for the growing interest in them. The objective of this research was to find new and innovative ways to improve the noise performance of the ADPLLs to make them suitable for high-speed wireline applications that require very low output jitter while considering the simplicity of the design.

The target application, high speed wireline communication requires integer PLL with a reference clock of 300MHz and output clock of 10GHz and 20GHz (in two different loops). On the output jitter, the target was to achieve an rms jitter of sub-picosecond.

Due to the limitations of the Time-to-Digital Converter (TDC) based phase detector, such as large variations of resolution over PVT, requiring complex calibration techniques and high power consumption, the TDC base PLL was not the best choice for the application. On the other hand, the Bang-Bang PLL characteristics made it a suitable candidate for this project due to its robust performance over PVT, simplicity of the design and com-

patibility with integer PLLs.

As one of the most important blocks of the Bang-Bang digital loop, the phase detector plays an important role in determining the performance of the ADPLL. Hence, the first part of this research is focused on the performance of the phase detector and its limitations that might affect the overall performance of the ADPLL.

The investigation of the phase detector showed that the gain reduction of the phase detector under certain condition can degrade the performance of the loop. Since the phase detector of the Bang-Bang PLL (BBPLL) operates at the edge of the clock, if the time difference between the two edges of the clock are narrow such that the timing requirements, hold time and setup time, are violated, the gain of the phase detector is significantly reduced which in part results in hysteresis in the loop and increased deterministic jitter of the output clock.

The results of this investigation led to a contribution published in IEEE Transactions on Circuits and Systems, [1]. In this article, the behavior of the phase detector in the digital loop was modeled and closed form equations were derived to predict the behavior of the loop based on the characteristics of the phase detector. The analysis of the loop behavior and the equations provided, give the designers a tool to predict the location of the spurious tones that are result of the repetitive pattern in the control signal of the Digitally Controlled Oscillator (DCO) and the excessive jitter generated by the loop due to the limitations of the phase detector.

To improve the performance of the BBPLL due to the phase detector limitations, two techniques were investigated. In the first technique, a software

generated random bit stream was used as the reference for the ADPLL. In this technique the bit stream was generated as the output of an “ $n - th$ ” order $\Sigma\Delta$ modulator carrying the noise-shaping characteristics of the modulator which helped reducing the inband noise. Using the bit stream helps to reduce the spurious tones by dithering the reference and breaking the cyclic patterns in the control signal. This work is published in IEEE Electronics Letters Journal, [2].

In the second technique, a Time-Amplifier (TA) is employed to improve the performance of the phase detector by increasing the time difference between the input clocks and preventing the phase detector to enter the metastable region which results in hysteresis and degrades the performance of the PLL.

In the second part of the research, a multi-bit phase detector is proposed that employs a new technique to improve the resolution of a “TDC-like” phase detector. The aim of this project was to design and implement a fine-resolution multi-bit phase detector which alleviates the limitations of the TDC such as dependency on PVT and requirement for complex calibration schemes. In this technique a transmission line is used to provide a fine delay between adjacent taps that are used as input clock of the phase detector. This part of the research is divided into two sections. In the first section a flash transmission delay line based phase detector is designed where the same number of arbiters, as the number of the taps of the transmission line are used to generate a digital code that contains the phase error information between the reference clock and the feedback clock. An extensive performance analysis using stochastic methods is done on the performance of the flash

phase detector and design challenges and trades off are shown.

In the second part, a new approach is proposed which improves the trade-offs of the flash phase detector in achieving the design target. In this method, a search algorithm is employed to eliminate the need for more than one arbiter in the loop by finding the closest reference edge, from the transmission line taps, to the feedback clock. The loop is designed in 28nm SOI CMOS technology and the performance of the new phase detector shows improvement compared to the first method.

1.3 Outline

This thesis is organized as follows:

Chapter 2 provides an overview on All-Digital PLLs including TDC based and BBPLLs and the state of the art research in this area is discussed in this chapter.

The effect of the phase detector limitations on the performance of the digital loop is shown and analyzed in Chapter 3. In this chapter several equations are derived which can be used to predict the spurious tones and the extra jitter in the loop due to the phase detector limitations. A new model for the BBPLL is also introduced that includes the effect of hysteresis of the phase detector on the loop performance.

In Chapter 4, Section 1 discusses briefly about design of the digital PLL considering jitter budgeting. The next two sections, show the techniques explored and employed to improve the performance of the digital PLL: in Section 2 the random bit stream is used to dither the reference clock in order

to reduce the spurious tones at the output and in Section 3, a Time-Amplifier is used to increase the resolution of the binary phase detector which in return improves the performance of the digital PLL.

Chapter 5 describes the new multi-bit flash transmission line based phase detector. In the chapter the transmission line is modeled and characterized to be used as a delay element and the design of the arbiters that are used as binary phase detector is shown.

The performance of the multi-bit flash phase detector is analyzed in Chapter 6. Stochastic analysis is used to determine the gain of the phase detector as well as its monotonicity and linearity. At the end of the chapter the design for high yield is explored and design challenges, limitations and trade-offs are shown.

In Chapter 7, the searched based multi-bit transmission line phase detector is introduced and its performance is shown. Section 7.5 shows the multi-bit phase detector in a digital loop. While the main focus is the design and performance of the phase detector, the loop is used to make a practical work frame for the phase detector. The digital loop is designed and implemented in 28nm SOI CMOS technology and the measured results are provided in this chapter.

Chapter 8, concludes the thesis and outlines the future work based on the research done in this thesis.

Chapter 2

Review of All-Digital Phase-Locked Loops

The early digital PLLs appeared in early 70's [3] - [6], however it was not until early 2000' that ADPLLs were used in industrial products [7] and [8]. ADPLLs, in general, fall into two categories depending on the type of the phase detector. Time-to-Digital converter based ADPLLs are mostly used as fractional PLLs in wireless applications and binary phase detector based, also known as BangBang PLLs have found use in wireline and clocking applications mainly as integer PLLs.

2.1 Time-to-Digital Converter based DPLL

In TDC based PLLs, the phase-frequency detector and the charge pump of the conventional PLL is replaced by a TDC as shown in Figure 2.1. The reference clock is sampled by the output clock and a series of its delayed

Figure 2.1: Block diagram of the TDC base digital PLL.

clocks as shown in Figure 2.2. Then the output code is passed through the loop filter that generates a digital code that controls the DCO. This method provides a simple way of digitizing the time/phase information. The generated code is then compared to a frequency code word in the loop, and the phase/frequency error generated by the comparison and integrated by the digital loop filter. The output of the filter controls the loop oscillator. Depending on the oscillator, either a Digital-to-Analog converter (DAC) is used or the implementation of the digital oscillator allows the use of the digital output of the filter digitally. The TDC loop eliminates the use of frequency dividers in the loop if the output frequency is reasonably low.

The accuracy of the conversion, hence the performance, depends strongly on the process technology as well as voltage and temperature variations. The time resolution of the TDC is determined by the minimum gate delay of the process technology. The large quantization error of the TDC can lead to low phase resolution and spurious output which may not be acceptable for many applications. In order to improve the performance of the TDC PLLs, several techniques have been introduced by academic and industrial research groups.

Phase interpolation is one of the techniques used to reduce the time reso-

Figure 2.2: Time-to-Digital Converter.

lution to less than a gate delay. In [9] and [10] phase interpolation is done by using extra circuitry and in [11], using both rising and falling edges to sample the reference clock has helped to increase the time resolution. In [12] and [13], time amplification technique is employed to achieve a finer resolution in the TDC. In this technique, the timing residue is amplified so that it can be further sampled to generate a digital code which represents the fine resolution error. Although these techniques show overall improvement in reducing the phase noise and spurs of the output, often the employed error reduction techniques, PVT calibration and mismatch cancellation add considerable amount of extra circuitry to the initial design which makes the design very complex

and challenging. Any added circuitry not only adds to the complexity but also introduces extra non-idealities in the form of non-linearity, phase noise and power dissipation to the design. Also TDC ADPLLs seem to be more suitable for low-speed applications.

2.2 Bang-Bang PLLs

Another major category of digital PLLs is Bang-Bang PLL which uses a binary phase detector. This phase detector provides 1-bit of phase information on the rising(falling) edge of the reference clock. The phase detector output indicates whether the feedback clock leads or lags the reference clock. The binary operation of the phase detector speeds up the phase detection hence speeds up the overall operation of the PLL, however, it introduces hard non-linearity into the system. BBPLLs have been conventionally used in clock and data recovery circuits, however, in recent years the advantages of the BBPLLs have made them suitable candidates for high-speed frequency synthesizers as well. The simplicity of the design is one of the main advantages of the BBPLLs which makes them more suitable for high frequency applications.

In CDRs, the Alexander (Bang-Bang) phase detector,[20] , shown in Figure 2.3, is commonly used to detect the phase information and to use it to recover the clock from incoming data. As shown in the Figure the reference of the CDR loop is the incoming data. The Alexander phase detector uses two data samples and one edge sample to extract early/late phase information.

Unlike in CDRs, for PLL applications, the reference is an external clean

Figure 2.3: Alexander (Bang-Bang) phase detector.

clock, e.g. a crystal oscillator, instead of incoming data. In high-speed application, often a single D-flip flop is used as the phase detector which only uses edge sample to lock the clock. Even though Alexander phase detector and a simple flip flop both have the same binary transfer function, they differ in the number of samples they use for phase error detection. The transfer function of the binary phase detector is shown in Figure 2.4.

Figure 2.4: Output of the Binary phase detector.

Due to the non-linear behavior of the phase detector, the analysis of the performance of the BBPLL proves to be more challenging comparing to the conventional PLL and has been subject to research on digital PLLs [14] - [15]. One of the main properties of BBPLL is the “locked” behavior. When locked, unlike in conventional PLLs, the output of the binary phase detector alternates between +1 and -1. Due to this “bang-bang” behavior, the loop oscillator is over-driven in one cycle and under-driven in the next cycle, yet the average frequency remains constant. This toggling results in intrinsic deterministic jitter. This jitter also poses a trade-off with the bandwidth of the loop.

In most applications a wide bandwidth is desired in order to suppress the out-of-band phase noise dominated by the loop oscillator. However, in the BBPLL, wider bandwidth translates to higher self generated jitter. Both bandwidth and jitter are inversely determined by the proportional gain of the loop filter and hence improving one degrades the other one. To reduce the intrinsic jitter of the BBPLL, some researchers adopted a re-configurable digital loop filter to reduce the proportional gain after the loop is initially

locked with a higher gain to reduce the jitter [17]. This also reduced the locking time. Although the noise is reduced, the frequency range of this PLL is fairly narrow. This method has been modified in [18] for a wider frequency range operation at the expense of phase noise by counting the number of consecutive leads and lags and modifying the loop gain accordingly.

The non-linear dynamics of the BBPLL contribute to non-ideal behavior of the loop. In particular, the presence of the limit cycles and spurs at the output, limit the performance of the BBPLL. The limit cycles are the periodic or quasi-periodic signals happening in DCO control signal which generate spurious output. This issue is also well known in other non-linear system such as $\Delta\Sigma$ modulators and has been studied and analyzed in the literature. The loop delay has been studied in [19] as a factor contributing to the occurrence of limit cycles. Although the gain of the binary phase detector is assumed to have a two-level step-like transfer function as shown in Figure 2.4, in practice the transition between the two levels has a finite slope causing a reduction in the gain of the phase detector and a change in the loop dynamics. This reduced gain of the phase detector also translates into limit cycles.

2.2.1 First Order Bang-Bang BPLL

The output of the phase detector is the sign of the time difference between reference clock and output clock; $\Delta t = t_{ref} - t_{output}$. As in Figure 2.4, the phase error mapping is as follow:

(a)

(b)

Figure 2.5: (a) Block diagram and (b) z-domain model of the first order BBPLL.

$$\varepsilon(\Delta t) = \begin{cases} +1 & \Delta t \geq 0 \\ -1 & \Delta t < 0 \end{cases} \quad (2.1)$$

Depending on whether output clock leads or lags the reference clock, the output of the phase detector is either +1 or -1. The phase detector only determines the direction of the phase correction and there is no information on the value of the phase error.

To clarify the behavior of the lock state, a first order BBPLL is shown in Figure 2.5. The first order BBPLL consists of the binary phase detector,

Figure 2.6: Simulated output of the first order BBPLL in response to a frequency ramp.

a loop filter which is proportional gain stage and an oscillator. The phase domain analysis of the first order loop is done in [21].

Since the phase detector output is either +1 or -1, in lock state, the frequency of the oscillator is:

$$f_{vco} = f_{nom} + \varepsilon(\Delta t)NK_pK_{vco} \quad , \varepsilon(\Delta t) = \pm 1 \quad (2.2)$$

where K_p is the attenuation factor of the proportional path (often called proportional gain), K_{vco} is the frequency gain of the oscillator, N is the frequency division and $\varepsilon(\Delta t)$ is the sign of the phase error between the reference and feedback clock.

It can be said that at each clock cycle, the oscillator is driven to one of

Figure 2.7: Output spectrum of a first order BBPLL.

the above frequencies and this is where the “Bang-Bang” name came from. As long as the frequency step is smaller than $2NK_pK_{vco}$ the PLL is locked and the oscillator frequency keeps toggling between the two frequencies. The response of a first order BBPLL to a frequency ramp is shown in Figure 2.6 which clearly shows the above statement. In lock, the average frequency is exactly as the input frequency, hence the output is synchronized with the reference clock. However, the oscillator is modulated by the two higher and lower control values hence it can be observed that, the output spectrum consists of two spurs along with the main tone as shown in Figure 2.7.

From (2.2) it can be seen that the peak-peak jitter in seconds, generated by the loop is,[21], assuming $N = 1$:

$$J_{pp} = \frac{4\pi K_P K_{vco}}{f_{nom}} \quad (2.3)$$

Figure 2.8: Block diagram of the second order BBPLL.

This jitter is due to the constant toggling of the oscillator in lock and is deterministic.

2.2.2 Second Order Bang-Bang BPLL

The second order BBPLL extends the frequency range of the BBPLL by employing an integral path to the loop filter as shown in Figure 2.8. The proportional path indeed takes care of the phase locking while integral path takes care of the frequency locking, [21]. Unlike the conventional PLLs where the analysis is often done in phase domain, in Bang-Bang PLLs, time domain analysis can be easily used since the loop is governed by hard non-linearity. The time domain analysis is adopted in most previously published work and in the present also the time domain equations are used to analyze the Bang-Bang PLL. For a delay-free second order Bang-Bang, the time-domain set of equations introduced in [22], are as below:

$$\left\{ \begin{array}{l} T_{vk} = T_{v0} + v_k K_T \\ \Delta t_k = \Delta t_{k-1} + T_r - N T_{vk} \\ v_k = K_p \varepsilon(\Delta t_k) + K_i \omega_k \\ \omega_k = \omega_{k-1} + \varepsilon(\Delta t_k) \\ K_T = -K_v T_{v0}^2 \end{array} \right. \quad (2.4)$$

where T_{v0} and T_{vk} are the period of the oscillator at initial time and k^{th} clock cycle, T_r is the period of the reference clock, N is the frequency division, v_k is the oscillator control signal at k^{th} clock cycle, ω_k is the output of the filter accumulator at k^{th} clock cycle, K_{vco} is the frequency gain of the oscillator and K_T is the period gain of the oscillator.

Similar to the 1st order loop, in the 2nd order loop locking happens when the phase error between the reference and the output clock is inside a bounded phase plane. The boundary of the phase plane is determined by the dynamics of the loop which are determined by the loop parameters such as loop filter and frequency gain of the oscillator. The deterministic jitter of the 2nd order loop in ideal conditions where $D = 0$, is as:

$$J_{pp} = 2N K_P K_T \quad (2.5)$$

This is due to the fact that the phase locking is controlled by the proportional path and in ideal conditions integral path should not contribute to any phase change in lock state. This however does not hold if the loop has internal delay. If the loop has D clock cycles of delay which is affecting both proportional and integral paths, the peak-to-peak jitter is increased significantly. In [22] an extensive analysis is done on the loop with internal delay, $D \neq 0$, and the

peak-to-peak jitter is given by:

$$J_{pp} = NK_p K_T [2(1 + D) + (1 + D)K_i/K_p + (1 + D)^3(K_i/K_p)^2 + O((K_i/K_p)^3)] \quad (2.6)$$

Although the phase trajectory in the ideal 2nd order is bounded to two values, similar to jitter, the loop delay increases the boundary of the phase trajectory. This analysis is also shown in [22] and in the present work, similar methods are used to investigate and analyze the loop behavior under non-idealities of the phase detector. The details of the analysis is shown in Chapter 3.

As in all second order feedback loops, the stability of the loop has to be carefully analyzed. In bang-Bang loops the stability of the PLL is mainly dependent on the loop filter parameters, K_p and K_i . To ensure stability the integral gain has to be much smaller than the proportional gain such that the timing update of the integral path is insignificant compared to the timing update of the proportional path. However similar to jitter, the loop delay is another parameter in the stability of the loop. In [22] the condition for an stable loop is given by:

$$\frac{K_i}{K_p} < \frac{2}{2D + 1} \quad (2.7)$$

where D is the loop delay in clock cycles.

As mentioned above the non-linear behavior of the loop results in the limit cycles. This condition dictates limitations on the performance of the loop in terms of generated jitter and output spurs. The limit cycles are characterized by their radius expressed in number of clock cycles. As the radius increases, the loop jitter performance degrades. Limit cycles can result from different sources in the loop and thus several studies focus on finding the sources of

limit cycles and designing for minimizing their impact [14], [16], [22] and [23]. A statistical description of the effect of metastability in a Bang-Bang phase detector on jitter is given in [14]. In this work, metastability manifests itself as a reduced gain at zero-crossing, hence a linear model for the phase detector transfer function in an analog loop is given and the generated jitter due to phase detector gain limitation is calculated. In [16] and [23], the resolution of the DCO, or the phase granularity, is assumed to be the main source affecting limit cycles in the loop. In [16], the loop is modeled utilizing $\Delta\Sigma$ methodology to include quantization noise of the DCO to predict the limit cycles by the number of phase jumps that happens to guarantee a stable lock. An analytic solution to design for minimum jitter and unwanted tones due to DCO resolution is given in [23]. In [22], a time-domain based analysis of the non-linear behavior of the loop is introduced and the loop is analyzed in the presence of delay. The delay is assumed to be an inherent delay caused by the digital implementation of the loop, and the relation between the loop delay and limit cycles is extensively studied.

2.3 Summary

In this chapter the two categories of digital PLLs were explored. In the first section, TDC based PLL was shown and some of the state of the art work was reviewed. The next section was dedicated to Bang-Bang PLLs which are the more suitable architecture for the target application of this research. A short review of the literature was also provided in this chapter. In the next chapter, a new analysis on the effect of phase detector limitations on

the performance of the BBPLL is done. The time-domain equations shown in Section 2.2.2 are used to derive new equations that model the loop with phase detector limitations.

Chapter 3

Effect of Phase Detector

Hysteresis on the Performance of the Digital Bang-Bang PLL

In this chapter, the phase detector is investigated as a source of increased jitter and spurious tones at the output of the BBPLL. Since the phase detector samples the phase information at the edge of the clock, as the BBPLL approaches the lock state, edges of the reference and feedback clocks are getting closer and this may result in violating the timing properties of the phase detector. Depending on the flip flop and the dynamics of the loop, the flip flop may enter metastable region and the hysteresis degrades the performance of the loop. In this chapter the effect of the hysteresis of the phase detector on the performance of the loop is investigated and a new model for the BBPLL is introduced that includes the effect of hysteresis of the phase detector on the performance of the loop. The results of this investigation is published in

[1].

3.1 Effect of Phase Detector Gain Limitation on Bang-Bang BPLL Performance

Often a single flip flop is used as phase detector in BBPLLs. One of the limitations of the flip flops is the gain reduction which manifests itself as failure due to metastability [14]. If the timing margin of the flip flop, t_{set} or t_{hold} , is violated, the gain of the flip flop is reduced which means the output does not fully charge or discharge to its final value. As a result the expected transition fails and the output stays in an ambiguous state. Due to noise the output cannot stay in metastable region for long and eventually it flips to one of the stable regions. However due to low gain often the output returns back to its original state [24]. In this situation, the flip flop exhibits hysteresis. In this section an investigation of the effect of the hysteresis in PD on the digital loop is performed.

3.1.1 Limit-Cycles in Bang-Bang PLL Loop with Non-ideal Phase Detector

Figure 3.1 shows a discrete model of the BBPLL. The digital implementation of these PLLs often introduces extra delay in the loop which is shown here by D in number of clock cycles. This intrinsic delay degrades the performance, hence careful design is necessary to keep this delay as low as possible [22]. In lock state, the loop is minimizing the phase error to zero, meaning, the

Figure 3.1: Model of the second order BBPLL.

two input edges are very close to each other. To analyze the loop, the time domain equations are re-written as in (3.1), where k denotes the iteration index in terms of number of reference clock cycles from the initial clock cycle of 0, T_{v0} denotes the initial period of the oscillator and T_{vk} is the period of the oscillator after k clock cycles. T_r is the period of the reference clock, assuming it is a jitter free signal. K_p and K_i are the loop filter proportional and integral path gains, respectively. v_k is the output of the loop filter and ω_k is the output of the loop integrator at k_{th} clock cycle. K_v is the oscillator frequency gain which is converted to period gain, K_T , and N is the frequency division ratio. The $sgn(\Delta t)$ is the sign of the error and is defined in (2.1). Since frequency and period of the signal change in opposite directions, the period gain of the oscillator has a negative sign with respect to the frequency gain. This loop is assumed to have an inherent delay equal to D reference clock cycles, which affects both the proportional and the integral path. Since we are interested in the locked behavior, it is assumed that the loop is frequency locked at the k_{th} clock cycle, $NT_{vk} = T_r$.

Figure 3.2: Transfer function of the phase detector under hysteresis.

$$\left\{ \begin{array}{l} T_{vk} = T_{v0} + v_k K_T \\ \Delta t_k = \Delta t_{k-1} + T_r - N T_{vk} \\ v_k = K_p \text{sgn}(\Delta t_{k-D}) + K_i \omega_{k-D} \\ \omega_k = \omega_{k-1} + \text{sgn}(\Delta t_k) \\ K_T = -K_v T_{v0}^2 \end{array} \right. \quad (3.1)$$

For the loop to phase lock, it is necessary to have the same number of iterations in the positive direction as in the negative direction. The set of equations in (3.1) do not consider the condition where there is hysteresis in the loop.

If PD enters the metastable region due to timing violation, the output transition does not happen and it leads to hysteresis as shown in Figure 3.2. In this case, the phase error deviates from the ideal consecutive +1 and -1 and the loop behavior is similar to that of a loop with an internal delay, causing the loop to have limit cycles (orbits) with radius greater than 1. The

Figure 3.3: Example of the phase trajectory of a BBPLL, circles: delay-free ($D = 0$) with non-ideal phase detector, $\sigma \neq 0$, solid line: arbitrary delay ($D \neq 0$) and an ideal phase detector, $\sigma = 0$.

spur location and generated jitter are directly proportional to the radius of the limit cycle. In the following sections, it is shown how the length of the hysteresis, measured in units of time, affects the behavior of the loop jitter and location of the spurs. To analyze the behavior, we have to find the relation between the radius of the orbit and hysteresis, denoted by σ (Figure 3.2).

Figure 3.3 shows examples of the orbits when the loop is locked. In this plot x-axis shows the time difference between the two edges of the clock, Δt , and y-axis shows the output of the accumulator. Assume at initial cycle, k , Δt_k is positive and close to zero. The accumulator value at the initial cycle

is ω_0 . In a hysteresis-free loop, the following is true for a sign transition at the output of the phase detector:

$$\begin{cases} \Delta t_k \geq 0 \\ \Delta t_{k+1} < 0 \end{cases} \quad (3.2)$$

That is, assuming if at k^{th} clock cycle the reference clock is leading the feedback clock, then the timing difference between the two clocks is positive and if at $k+1^{th}$ cycle a transition happens, then the feedback clock leads the reference clock and the difference between the two clock edges is negative. In this loop it is assumed that the loop has an arbitrary number of clock cycles delay, $D \neq 0$. The presence of hysteresis however, adds another timing condition to the loop for a transition, as follow:

$$\begin{cases} \Delta t_k > 0 \\ \Delta t_{k+1} < 0 \\ \Delta t_{k+n} \geq -\sigma \quad n \geq 1 \end{cases} \quad (3.3)$$

Assuming $D = 0$, from (3.1), the timing update is:

$$\Delta t_{update_k} = \Delta t_k - \Delta t_{k-1} = -NK_T \left(K_p \text{sgn}(\Delta t_k) + K_i \sum_{i=0}^k \text{sgn}(\Delta t_i) \right) \quad (3.4)$$

At each cycle, the phase timing error is changed by Δt_{update} . Assuming T_r is constant, if $|\Delta t_{update}| < \sigma$, $n > 1$ number of cycles is required so that the condition in (3.3) is satisfied.

As shown in Figure 3.2, during the hysteresis, the output of the phase detector remains the same and the timing error is accumulated in the oscillator. This accumulation changes the phase trajectory of the loop compared to a hysteresis-free loop. Figure 3.3 shows the phase trajectory of a loop with

$\sigma \neq 0$ (circles) in comparison with a hysteresis-free loop (solid line). For the same loop parameters, the accumulator keeps increasing (decreasing) depending on the previous state; hence the timing error keeps increasing until $|\Delta t| \geq \sigma$. This directly translates into additional delay in the loop which increases the radius of the limit cycle as well as the jitter. Once the transition condition is met, the phase detector output toggles and the loop remains in the reverse direction for the same number of cycles as the previous direction.

Considering this behavior, the equations governing the loop are summarized in (3.5) and (3.6).

$$\left\{ \begin{array}{lll} \omega_0 & , & \text{sgn}(\Delta t_0) = +1 \quad \text{for } k = 0 \\ \omega_R = \omega_0 + R & , & \text{sgn}(\Delta t_k) = +1 \quad \text{for } 0 \leq k \leq R \\ \omega_{2R} = \omega_0 & , & \text{sgn}(\Delta t_k) = -1 \quad \text{for } R < k \leq 2R \\ \omega_{3R} = \omega_0 - R & , & \text{sgn}(\Delta t_k) = -1 \quad \text{for } 2R < k \leq 3R \\ \omega_{4R} = \omega_0 & , & \text{sgn}(\Delta t_k) = +1 \quad \text{for } 3R < k \leq 4R \end{array} \right. \quad (3.5)$$

$$\left\{ \begin{array}{ll} \Delta t_0 \approx 0 & k = 0 \\ \Delta t_R = \Delta t_0 + K_T N \left(K_i \sum_{i=1}^R (\omega_0 + i) + K_p R \right) \geq \sigma & 0 \leq k \leq R \\ \Delta t_{2R} = \Delta t_0 + K_T N \left(K_i \sum_{i=1}^R (2\omega_0 + R) \right) & R < k \leq 2R \\ \Delta t_{3R} = \Delta t_0 + K_T N \left(K_i \sum_{i=1}^R (3\omega_0 + R - i) - K_p R \right) & 2R < k \leq 3R \\ \Delta t_{4R} = \Delta t_0 + K_T N \left(K_i \sum_{i=1}^R (4\omega_0) \right) & 3R < k \leq 4R \end{array} \right. \quad (3.6)$$

Equation (3.5) shows the value of the accumulator, ω_k , and the sign of the error, $\text{sgn}(\Delta t_k)$, at any given time, t_k and (3.6) shows the timing error for the same time points. In the first analysis, it is assumed that the loop is delay

free, $D = 0$, to emphasize the behavior of the phase detector non-idealities on the performance of the PLL. In practice, this is the case where the loop delay has little impact on the operation, e.g., when the bandwidth of the PLL is small enough. At initial cycle, $k = 0$, we assume the accumulator value is ω_0 and the timing error is $\Delta t_0 \approx 0$. It is expected that a transition to happen in the next clock cycle, however, as mentioned, the sign of the error stays the same till $\Delta t_k \leq -\sigma$. If the phase trajectory plane is divided into 4 sections, two of the sections should have positive sign and two should have negative sign. Also the two sections with the same sign should be consecutive to form an orbit. In the case shown in Figure 3.3, the second and the third sections have negative sign and the first and the forth sections have positive sign.

To validate (3.5) and (3.6), a MATLAB model based on the set of equations in (3.1) is implemented. In this model the timing margin of the phase detector is modeled as hysteresis with condition as in (3.3). This means, a transition happens only if the timing error is greater than the timing margin of the phase detector, σ . From the model it is observed that the radius of the loop increases by increasing σ and by reducing the proportional gain, K_p . The radius R is defined as the number of cycles needed till the phase detector timing conditions are met and the transition happens. Figure 3.4 (a) shows the dependency of the radius, R , versus K_p and σ , obtained from the model simulation. In this simulation, $f_{ref} = 312.5MHz$, $f_{out} = 2.5GHz$, $K_v = 250MHz/V$ and $N = 8$. To ensure the stability of the loop, $K_i = K_p/4$ and $D = 0$.

Using the set of equations shown in (3.5) and (3.6), after some algebraic simplifications, the radius of the limit cycle can be derived as:

Figure 3.4: Radius of the limit cycle over K_p and σ from, (a) MATLAB model, (b) closed form equation for R , (3.7).

$$R \cong \lceil \frac{\sigma}{NK_T K_p} \rceil \quad (3.7)$$

Figure 3.4 (b) shows the calculated radius versus K_p and σ . Since the stability of the loop requires $K_i \ll K_p$, the timing update due to the proportional path dominates the total update at each cycle and as a result (3.7) gives a very good estimate of the radius of the loop. This can be seen in the plots of Figure 3.4.

Jitter Performance of the Bang-Bang PLL with $\sigma \neq 0$

In (3.5) and (3.6), it is assumed at the initial iteration, $k = 0$, the value of the accumulator to be ω_0 . To obtain the loop jitter, Δt_{max} , the value of ω_0 has to be calculated for the specific orbit as a function of the loop parameters. From (3.5) and (3.6), it takes $R - \omega_0$ iterations so that $\Delta t_R \geq \sigma$ from $\Delta t_0 \approx 0$. By solving for Δt_R in the equation and assuming $K_p \gg K_i$, ω_0 is obtained as:

$$\omega_0 = -\alpha + \sqrt{(\alpha + R)^2 - \frac{2\sigma}{NK_T K_i}} + 1 \quad (3.8)$$

where,

$$\alpha = \frac{K_p}{K_i} \quad (3.9)$$

Once the initial value of the accumulator is known, the timing performance of the loop can be determined. Even after the timing error has reached the timing margin of the PD, the jitter keeps increasing for a while because of the slow update in the integral path compared to the fast update in the proportional path. The ratio between K_p and K_i , α , determines the amount of additional jitter. Depending on α , there are two cases for jitter calculation:

- *Case 1 : $\alpha > R$*

This condition suggests that K_p is much larger than K_i . In this case, the slow timing update of the integral path has little effect on the extra jitter; hence maximum jitter happens with one delay cycle at $(R + 1)th$ cycle from the initial cycle. Using (3.5) and (3.6) the jitter is:

$$\Delta t_{max} = K_T N \left[\frac{K_i (R(R+1) - \omega_0(\omega_0+1) - 2)}{2} + K_p (R - \omega_0 + 1) \right] \quad (3.10)$$

For reasonably small K_p and K_T , the maximum jitter occurs at the peak of the orbit and Δt_{max} can be very well approximated as σ .

- *Case 2 : $\alpha \leq R$*

For a case with large R when K_p and K_i are close to each other, both integral and proportional paths contribute to the timing update; however, they have opposite contributions due to the accumulated value in the integral path. Hence the jitter is at maximum when the two paths contribute equally to the timing update. Equivalently, the accumulator value has to reach α . For this case, jitter is:

$$\Delta t_{max} = \Delta t_R + K_T N \left[\frac{K_i (R(R-1) - \alpha^2)}{2} - K_p (R - \alpha) \right] \quad (3.11)$$

where Δt_R is:

$$\Delta t_R = \Delta t_0 + K_T N \left[\frac{K_i (R - \omega_0 - 1)(R + \omega_0)}{2} + K_p (R - \omega_0) \right] \approx \sigma \quad (3.12)$$

For a fixed K_p and K_i , the radius of the limit cycle and the jitter versus the phase detector timing margin, σ , are shown in Figure 3.5. In this figure $K_p = 2^{-12}$ and $K_i = 2^{-14}$, where the MATLAB model (circles) and the closed form equations (solid) are compared.

To give an overview of the dependency of the loop performance on K_p and σ , the loop jitter due to limit cycle is plotted in Figure 3.6, where the results of MATLAB model and the closed form equation are shown in part (a) and

Figure 3.5: (a) Radius of the limit cycle, MATLAB model (circles), calculated (solid) and (b) excessive jitter, MATLAB model (circles), calculated (solid), vs. σ for a loop with $K_p = 2^{-12}$ and $K_i = 2^{-14}$.

(b). In this plots $K_i = 2^{-14}$. From Figure 3.4 and Figure 3.6 it is seen that for large σ , the loop performance degrades as K_p reduces. For large K_p , the jitter changes linearly with K_p . This means that the timing update is large enough that the hysteresis of the PD does not affect the jitter. However, for smaller K_p , if the phase detector exhibits hysteresis, it results in more jitter. Hence for an optimized jitter performance it is necessary to evaluate the behavior of the PD. In Figure 3.7, loop jitter is plotted for a loop with $\sigma = 0$ (no hysteresis) and $\sigma = 2.5ps$. The plots clearly show the increased jitter for small K_p . Figure 3.7 shows the effect of K_i on jitter. In plot (a) K_i is kept constant and in plot (b) its ratio to K_p is kept as 4. It is observed

Figure 3.6: Loop jitter, (a) MATLAB model, (b) closed form equation, over K_p and σ .

that reducing K_i results in lower generated jitter but it increases the locking time, hence it is beneficial to keep the integral gain low.

The effect of the random jitter of the reference clock on the performance of the loop has been discussed in previous works such as in [23]. Figure 3.8 shows the loop jitter over K_p for various cases considering input random jitter, $J(\text{rms})$, and phase detector hysteresis. In these simulations a random jitter with RMS value of 0.51ps is added to the reference clock. The results show that in the presence of noise there is also an optimum loop filter gain which gives the lowest jitter, however, the presence of hysteresis dominates the jitter generation especially if K_p is small. However, if the random noise is larger than the hysteresis, overall noise performance is dominated by the noise. In these simulations, the intrinsic delay $D = 1$ and the integral gain

Figure 3.7: Comparison of the jitter generated by the loop with $\sigma = 0$ (circles) and $\sigma = 2.5\text{ps}$ over K_p , where (a) $K_i = 2^{-14}$ and (b) $K_i = \frac{K_p}{4}$.

$K_i = 2^{-14}$. Note that the jitter (Δt) is measured at the input of the loop as the difference between the two inputs of the phase detector.

3.1.2 Implementation of Bang-Bang PLL

To validate the analysis, a Bang-Bang loop is designed using a 32-nm CMOS technology where a flip-flop is used as the phase detector and the results are compared with the MATLAB model. In the circuit level simulations, a behavioral VCO is used which is controlled by a 12-bit behavioral DAC, providing high resolution to avoid the effect of the oscillator quantization on the performance. In these simulations, the phase detector timing margin, σ , is 1.7 ps. Figure 3.9 shows the orbits of the simulated and modeled loop in

Figure 3.8: Comparison of the loop jitter for various cases considering noise and hysteresis over K_p , where $D = 1$ and $K_i = 2^{-14}$.

two cases with different K_p values and constant σ and K_i . As can be seen for the same hysteresis amplitude, lower proportional gain results in higher jitter which contradicts the ideal, hysteresis-free loop. It should be noted that the jitter mentioned here is deterministic jitter, generated by the loop dynamics.

3.2 Spurious Tones in Bang-Bang PLLs

The radius of the limit cycles determines the frequency of the main spurious tones. In an ideal loop, spurs are located at $\pm \frac{f_{ref}}{2}$ away from the fundamental tone since at each reference clock cycle the output of the phase detector

Figure 3.9: Comparison between circuit level simulation (thin light lines) and MATLAB model (thick line) for a loop with $\sigma = 1.7ps$, $K_i = 2^{-14}$ and (a) $K_p = 2^{-12}$, (b) $K_p = 2^{-10}$.

toggles, meaning the oscillator is modulated at half rate of the reference clock. As the radius of the limit cycle increases, the frequency of the modulation reduces, which moves the spur tones closer to the output. For the loop with limit cycles having a radius of R cycles, the spur tones are located at:

$$f_{spur} = \pm \frac{f_{ref}}{2R} \quad (3.13)$$

Figure 3.10 shows the frequency of the spur tone normalized to the reference frequency for two values of proportional gain versus the phase detector timing margin.

These plots, obtained from the MATLAB model, show the dependency of the spur location to the radius of the limit cycle as in (3.13). As expected, the

Figure 3.10: Normalized spurious tone over σ for the loop with $K_p = 2^{-9}$ (diamond) and $K_p = 2^{-12}$ (cross).

performance degradation increases as K_p is decreased. This can be seen from the results for $K_p = 2^{-9}$ (diamond) and $K_p = 2^{-12}$ (cross). In Figure 3.11 the power level of the main spur tone is compared for $K_p = 2^{-9}$ (diamond) and $K_p = 2^{-12}$ (cross) over σ . As expected, larger limit cycles generate stronger spur tones that are closer to the fundamental with respect to the reference frequency. Hence, when designing the loop, it is necessary to optimize the parameters and circuit blocks for limit cycles with minimum radius.

To compare these results with the circuit level simulation, the loop with $K_p = 2^{-12}$ and $K_i = 2^{-14}$, is simulated in 32-nm CMOS technology. The spectrum of the oscillator control signal, v , of the simulated and model PLL are shown in Figure 3.12 top and bottom, respectively. From (3.7), assuming

Figure 3.11: Power of the spurious tone over σ for the loop with $K_p = 2^{-9}$ (diamond) and $K_p = 2^{-12}$ (cross).

$NK_T = 320ps$ and $\sigma = 1.7ps$, the radius of the limit cycle is calculated as $R = 22$ which is equal to the loop simulation seen in Figure 3.9 (a). In this case, the reference frequency is 312MHz. From (3.13), the spur tone is located at:

$$f_{spur} = \frac{312 \text{ MHz}}{44} = 7\text{MHz} \quad (3.14)$$

which is very close to the result of 6MHz obtained from the circuit simulations. To compare the MATLAB model with circuit simulation, the timing margin of the phase detector is extracted from Cadence simulations and used in MATLAB model. Since the timing resolution is in the order of less than a picosecond, the simulation setup can affect the accuracy of measuring , hence

Figure 3.12: Spectrum of the oscillator control signal, v , (top) circuit level simulation, (bottom) MATLAB model

some small discrepancy between Cadence simulation and model is expected.

3.3 Modeling Bang-Bang PLLs with Non-ideal Phase Detector

In this section we introduce a new model for the Bang-Bang PLL which includes the effect of the phase detector hysteresis. This model is of advantage when designing the loop by predicting the frequency of the spurs and the deterministic jitter.

3.3.1 Bang-Bang PLL model

In the previous section, the radius of the limit cycle and excessive jitter of the loop are evaluated and the closed form equations are derived. These equations give necessary information to model the loop.

Based on the analysis, it can be said that the loop with hysteresis exhibits similar behavior as a type I BBPLL, where the delay is affecting both integral and proportional paths, as shown in Figure 3.1. However, here the delay due to phase detector hysteresis has a larger impact on the loop performance compared to the implementation delay as shown in [22]. In this model we define this delay by M clock cycles at the output of the phase detector.

If at initial cycle, $k = 0$, we assume ω_0 for the value of the accumulator, the extra cycles, or the delay, can be estimated as:

$$M \approx R - \omega_0 \quad (3.15)$$

Figure 3.13: Model of the BBPLL with a non-ideal phase detector.

From (3.7) and (3.8), it is seen that M , depends on the phase detector timing margin σ and the loop filter gains, K_i and K_p . The BBPLL model with non-ideal phase detector is shown in Figure 3.13. Equation (3.15) holds only for $K_p \gg K_i$. If they become close to one another, the loop is at the edge of instability and the behavior of the loop becomes difficult to predict.

Also extra delay in the loop reduces the phase margin of the PLL, meaning that for excessive loop delay the PLL can become unstable. So the loop delay should be kept to the minimum not only for jitter performance but also for stability reasons [22].

For the example loop with $\sigma = 1.7ps$, $K_p = 2^{-11}$ and $K_i = 2^{-14}$, (3.7) and (3.8) result in $R = 11$ and $\omega_0 = 6$; and the delay is calculated as $M = 5$, as defined by (3.15). Figure 3.14 shows the performance of the simulated loop in comparison with that of the model.

Since the model introduces a delay in the loop, it can cause the loop to approach the unstable region where the loop behavior can be unpredictable. Although equations (3.7) to (3.15) are still valid, the model can give incorrect results depending on σ and K_p . From extensive simulation, the calculated number of delay cycles, M , and the model are valid as long as (3.16) holds.

Figure 3.14: Comparison of the circuit level simulation of the loop performance of the circuit (thin grey lines) with the model (circles) for $\sigma = 1.7ps$, $K_p = 2^{-11}$ and $K_i = 2^{-14}$.

$$\frac{\sigma}{NTK_T K_p} < \frac{K_p}{K_i} \quad (3.16)$$

An example of the valid range for the case where $K_i = \frac{K_p}{6}$ is shown in Figure 3.15 with cross symbols.

3.3.2 Loop with Internal Delay, $D \neq 0$

Depending on the location of the delay, two types of BBPLL are introduced in [22]. If the delay affects both integral and proportional paths, the BBPLL

Figure 3.15: Loop parameters, σ and K_p range for valid prediction of M where $K_i = \frac{K_p}{6}$.

is defined as *type-I* and if the delay affects only the integral path, it is called *type-II*.

In practice, it is beneficial to design the loop such that only the integral path is affected by the delay as the performance degradation is less severe. However, the delay generated by the phase detector affects both integral and proportional paths, hence, it dominates the performance degradation. Without going through the detail of analysis; here, the model in Figure 3.13 is used to show the effect of the phase detector gain limitation on the loop with an internal delay.

Figure 3.16 shows a comparison of type-I and type-II BBPLL performance

Figure 3.16: Comparison of type-I and type-II BBPLL with $D = 2$ for $\sigma = 0$ and $\sigma = 1.7ps$. The delay-free loop result is shown as reference (cross). Note that type I and type II are identical if $D = 0$.

with or without the internal delay and ideal and non-ideal phase detector. The loop filter parameters are $K_p = 2^{-11}$ and $K_i = 2^{-14}$ for all cases. In this plot, the simulation results of the loops for $\sigma = 0$ and $\sigma = 1.7ps$ are compared.

Although type-II BBPLL shows a superior performance in a loop with internal delay, its performance degrades more severely with a non-ideal phase detector compared to type-I PLL. This is due to transformation of type-II to type-I when the phase detector introduces extra delay in the loop. However the type-II PLL still has better absolute performance, so careful design has to be considered to keep the proportional path delay free.

Beside the increased jitter and closer spur tones, the loop delay can push the loop to instability, depending on the ratio of proportional to integral gains. Hence another reason of the importance of analyzing the phase detector hysteresis is to determine the minimum ratio of the proportional to the integral gain which prevents the loop from becoming unstable.

3.4 Summary

In this chapter the effect of the hysteresis of the phase detector on the performance of the phase detector was investigated and based on the analysis a set of equations were derived that can be used to predict the frequency of the spurious tones and the deterministic jitter added due to the phase detector non-ideality and a model for the BBPLL loop is provided that considers this effect. The material of this chapter is published in [1].

Chapter 4

Improving the Performance of the Bang-Bang PLL Due to Phase Detector Limitations

When budgeting for jitter and spurs, the loop has to be optimized for minimum inherent jitter generated by the loop and for the minimum effect of the PD on jitter. From the previous analysis, it was shown that smaller proportional and integral gain generates lower jitter; however, the loop stays in the same state longer if the PD has a low timing resolution which may override the advantage of having low proportional gain.

In this chapter, the jitter budgeting methodology is briefly discussed, focusing on the effect of the phase detector limitations then two techniques are investigated that aim to improve the performance of the PLL by reducing the spurious tones at the output. In the first technique a random bit stream is generated to dither the reference clock and in the second technique, a

Time-Amplifier (TA) is employed to increase the resolution of the PD.

4.1 Example of Jitter Budgeting Methodology

The evaluation of the Bang-Bang loop performance in the previous chapter provides insight for designing the loop for a given jitter budget. When designing the digital BBPLL, both random and deterministic jitter have to be considered. The random jitter performance evaluation follows similar methods discussed in [15], [21] and [25]. A linearized model of the Bang-Bang phase detector is used to facilitate the linear analysis of the loop. The linear gain of the phase detector is estimated as in (4.1), assuming the jitter has a Gaussian distribution [15],

$$K_{PD} = \frac{1}{\sqrt{2\pi}\phi_{in}} \quad (4.1)$$

where, ϕ_{in} is the rms jitter on the reference clock. The Jitter transfer function of the conventional analog Bang-Bang PLL is shown in [26]. This equation can be used to optimize the bandwidth of the loop for jitter performance. Assuming the phase noise of the oscillator meets the out-of-band jitter profile, the proportional and integral gain of the loop, K_p and K_i , are selected for the bandwidth that minimizes the jitter without compromising stability of the loop. The loop optimization is extensively studied in [15].

Once the parameters of the loop are determined, the loop has to be evaluated for maximum allowed timing margin of the phase detector, σ , for the given jitter profile. The model introduced in Chapter 3 can be used to map

the frequency and the power of the spurs. Comparing the jitter profile and spur tone map gives an upper bound for σ which provides a guideline for designing the phase detector.

As a practical example, assume a BBPLL is designed for a high speed CDR application with signal rate of $40Gbps$ and a reference clock of $300MHz$ and an acceptable bit error rate of 10^{-12} . The total jitter, TJ is:

$$T_J = 2 \times Q_{BER} \times RJ(RMS) + DJ(Peak - Peak) \quad (4.2)$$

where RJ is the random jitter and DJ is the deterministic jitter and Q_{BER} is a factor that depends on the target Bit Error Rate (BER). For a system with $BER = 10^{-12}$, $Q_{BER} = 7.05$ which means the the total random jitter, RJ has a weight of 14 compared to deterministic jitter, [27], [28] .

In most standards the acceptable jitter values are as $T_J = 0.32UI$, $RJ = 0.15UI$ and $DJ = 0.17UI$. The random jitter of the BBPLL is dominated by the DCO which requires a phase noise that meets the above specifications. For a given DCO with period gain $K_T = 2.5ps$, and PD with gain as in (4.1) with $\phi_{in} = 3ps$, assuming the input jitter on the reference is greater than the jitter generated by the loop, $(D+1)K_pNK_T$ [22]. Designing for a 1MHz bandwidth leads to a loop filter proportional gain $K_p = 2^{10}$. In a good design the ratio between K_i and K_P is kept large for assuring the stability. This also facilitates the assumption of a first order PLL.

From the specification, the maximum DJ is about $4.25ps$. This budget should include jitter coming from all sources such as loop delay, as well as delay due to hysteresis. Hence, to leave enough margin, the hysteresis jitter should be limited to $2ps$. Assuming $\alpha = \frac{K_p}{K_i} = 16$, solving (3.10) (3.12)

Figure 4.1: Jitter over hysteresis for $\alpha = \frac{K_p}{K_i} = 16$.

gives the maximum allowed hysteresis of PD. Since α is large and K_p and K_i are small, we can safely estimate the jitter as σ , the timing jitter of the PD. MATLAB is used to solve the equations numerically and a plot of the jitter versus σ is shown in Figure 4.1, which supports our estimation. Based on the maximum allowable DJ, the hysteresis cannot be larger than $1ps$. Figure 4.2 shows the jitter with maximum allowable σ . Since the reference noise impact the jitter performance, the jitter with added noise is also shown in dashed line. It is assumed that $D = 1$.

4.2 Spur Reduction in Bang-Bang PLLs Using a Programmable Bit-Stream

In this section, *Spread Spectrum Clocking* (SSC) technique is used to improve the performance of the BBPLL. In SSC technique, a random signal, i.e.

Figure 4.2: Input jitter of the example design, thick solid line: without reference noise, dash line: with reference noise.

white noise, is used to dither the main signal for an improved spectrum. This technique is widely used in fractional PLLs by using a $\Sigma\Delta$ modulator to randomize the frequency division to prevent a periodic pattern that causes the spurious tones at the output. Similarly in BBPLLs this technique is used to improve the performance by breaking the reaping patterns that cause spurious output. Unlike conventional PLLs, the bandwidth of the BBPLL is inversely proportional to the input jitter since the gain of the binary phase detector is inversely proportional to the input jitter, [14], [31]. In [29] a controlled amount of jitter is added to the reference clock to take advantage of the inverse proportional relation between the gain of the BBPD and the input jitter. To prevent the noise level from increasing due to the input jitter,

a $\Sigma\Delta$ modulator is used to shape the noise at the input of the BBPLL. [30] uses a noise shaped short period pattern to randomize a TDC based ADPLL to smooth out the output spectrum. These two techniques are used in the present work to achieve a versatile and portable design that improves the performance of the BBPLL.

4.2.1 Generating a Noise-Shaped Random Bit-Stream

In the present work a similar technique is used to smooth out the spectrum of the output and to reduce the spurious tones by using a random bit-stream as the reference of the BBPLL. The unique feature of this work is the method that is used to generate the random bits. In the proposed technique, a software based $\Sigma\Delta$ modulator is designed that uses the reference clock to generate the output bit-stream using a Digital-to-Time Converter (DTC)[32]. The bit-stream then can be used as the input to the ASIC using any standard interface such as JTAG. This technique allows for easy re-designing of the bit-stream for a new application without any hardware overhead since the software designed $\Sigma\Delta$ modulator can be re-designed to any order for required noise shaping.

Since the bit-stream is used as the reference, the average frequency of the random stream should be exactly the same as the frequency of the reference clock. Since the BBPLL has a low-pass transfer function, the quantization noise of the modulator which is shaped to higher frequencies compared to reference is filtered and hence the noise floor of the output is not raised significantly due to randomization.

Figure 4.3 (a) shows the operation of the DTC where the input amplitude

Figure 4.3: (a)The Digital-to-Time Converter, (b) block diagram and transfer function of the PLL with random reference using $\Sigma\Delta$ modulator and DTC.

of the signal is converted to a time-domain signal and Figure 4.3 (b) shows the principal of the operation of the input dithering in PLLs. As can be seen, a $\Sigma\Delta$ modulator is used to generate a random output signal from the reference. Then the output of the modulator is collected by the DTC and mapped to a time-domain signal. An example of mapping is as follow [32]:

$$\Sigma\Delta\text{output} = \begin{cases} '0' \\ '1' \end{cases} \rightarrow \text{DTC output} = \begin{cases} '1100' \\ '0110' \end{cases} \quad (4.3)$$

The input signal is band-limited so that a high over-sampling ratio (OSR) can be used for the modulator. The advantage of the $\Sigma\Delta$ modulator is its noise shaping ability, where for the same noise power the noise density shows a high-pass behavior. This shaped noise however, should be filtered out to prevent injection of the excessive noise to the loop. In this application, since the PLL has a low-pass characteristics, it also filters the shaped noise and an extra filtering step is not needed. This process can be seen in Figure 4.3 (b) where the transfer function of the PLL with a randomized reference using a $\Sigma\Delta$ modulator and a DTC is shown at the bottom of the graph.

4.2.2 Random Bit-Stream in Bang-Bang PLL

Figure 4.4 shows the top level block diagram of the BBPLL with a random bit-stream reference. In this architecture a secondary loop is used for fast frequency acquisition which consists of an up-down counter with an accumulator. This loop is involved only during the frequency locking and the fine resolution frequency and phase locking is reached by the Bang-Bang loop with random reference. The random bit-stream that is generated in software is stored in external or internal memory and is used as the reference in a recursive manner.

Figure 4.5 (a) shows the output spectrum of the conventional BBPLL in comparison with that of the same BBPLL with random bit-stream reference, generated by a 4th order $\Sigma\Delta$ modulator shown in Figure 4.5 (b). As can be seen, in the BBPLL with random reference, the main spurious tone is located at higher frequency, 130MHz, compared to 50MHz in conventional BBPLL and has a lower power. In the BBPLL with random reference, the

Figure 4.4: The block diagram of the BBPLL with random bit-stream reference.

noise floor is higher which is due to inherit noise of the $\Sigma\Delta$ modulator which is not filtered by the PLL.

4.3 Increasing the Resolution of Bang-Bang PD using Time-Amplifier

In this section a Time-Amplifier is designed to help increasing the BBPD. Then the effect of the PD with TA is shown in a designed digital Bang-Bang PLL.

Figure 4.5: (a) output spectrum of the conventional BBPLL, (b) output spectrum of the BBPLL with random bit-stream reference.

4.3.1 Time-Amplifier Assisted Phase Detector

The time-amplifier is introduced in [34] and its modified design is used in different applications. [35] describes the time amplification concept and introduces a CMOS design based on differential pair schematic which is later on used to for high resolution timing measurement in [36]. In [12] the time-amplifier is used in a coarse-fine TDC structure to improve the resolution of the fine TDC. The schematic and timing diagram of the time-amplifier is used from [12] which is shown in Figure 4.6. The TA consists of two RS latches that are driven by two inputs, each seeing one input and a delayed version of the other input. Both latches are loaded with large capacitors for given TA gain. The gain of the TA depends on the load capacitor, delay at the input and g_m of the gates [12]. The symmetrical schematic of the TA ensures that the clock that arrives first, loads the capacitor of the latch that

Figure 4.6: Schematic and timing diagram of the time-amplifier, [12].

is connected by the shortest path and as soon as the load is charged it resets the other latch.

In this work, the TA is used to increase the resolution of the Bang-Bang phase detector in order to reduce the spurious tones at the output of the BBPLL. The aim of the TA in this work is to increase the distance between the two clock edges near the zero crossing. Unlike in the TDC that the value of the phase error is important, in the BBPD, as long as the order of the edges in terms of arrival time is conserved, the actual distance between the

edges is not important. This eliminates any required calibration or decoding process that is necessary in the TDC.

The TA operates by extending the duty cycle of the input signals. This can pose limitations when employing the TA. If the application is sensitive to duty cycle distortion (DCD), DCD correction circuitry is necessary which can add hardware overhead and can be challenging due to the large amount of distortion if the gain is high. In Bang-Bang PD application, the phase detector works with the edge and is not sensitive to duty cycle which is an advantage. However, if the gain is high and if the TA is always operating, there is a high risk that due to DCD, the clock edges can be lost which can have significant impact on the operation of the PD and the loop. To alleviate this issue a “Close Edge Detector” (CED) circuit is designed to prevent the TA from operating when the edges have a large distance between them. The schematic of the CED is shown in Figure 4.7. The delay in the Early/Late clock paths is several times larger than the timing resolution of the PD to make sure the range is fully covered. If the edges are far apart, both inputs go through a few gates that is similar to the delay of the TA. When the edges of the clocks fall into the operating range of the TA, the TA is enabled by CED and extends the edges. The block diagram of the TA assisted phase detector (TAPD) is shown in Figure 4.8.

4.3.2 Design and Implementation of Time-Amplifier Assisted Phase Detector

The TAPD is designed and implemented in 130nm BiCMOS technology, using only CMOS transistors. The TA is a custom designed circuit while

Figure 4.9: Transient simulation of TAPD with $C_{load} = 130 fF$.

In the first design an edge distance of $-350p < \Delta t_{in} < 350ps$ was targeted. The load capacitor was around $130 fF$. An example of transient waveforms of the input and output of the TAPD is shown in Figure 4.9 in this design the TA gain is, $A_{TA} \approx 2$. The operating range later was reduced to $\Delta t_{in} = \pm 120ps$ due to large DCD. The transfer function of the TA as in output time versus input time is shown in Figure 4.10.

Figure 4.10: Simulated transfer function of the TA.

Figure 4.11: Layout of the TAPD.

The layout of the TAPD is done symmetrically as shown in Figure 4.11 to ensure the best performance. The implemented chip consisted of the TAPD and a regular binary phase detector connected to the same inputs as TAPD. The layout of the chip is shown in Figure 4.12.

Figure 4.12: Layout of the fabricated TAPD chip.

Figure 4.13: Transient measurement of the TA for Δt_{in} (a) 100ps and (b) 150ps.

4.3.3 TAPD Chip Measurement

In the first test the two inputs have a delay between them and at the output the output of the TA is observed. In this test CED is activated. The transient measurement of the output of the TA is shown in Figure 4.13, where (a) shows the measurement for $\Delta t_{in} = 100ps$ and (b) for $\Delta t_{in} = 150ps$. As can be seen, in case (a) since Δt_{in} is within the range of CED timing, the TA is activated and the output time, Δt_{out} is increased to 196ps. In case (b) the input time is outside of the range of CED, hence the TA is disabled and the two outputs only go through a delay without any further change. As can be seen the output time is measured at 152ps which is the same as the input time.

By changing the delay, the transfer function of the TA is obtained which is shown in Figure 4.14. In this graph the delay from the interconnects is de-embedded from the measured output time and the measured transfer function is compared to that of simulated transfer function. The measured

Figure 4.14: Measured transfer function of the TA compared with simulation.

gain of the TA is $A_{TA} \approx 1.6$ and the the TA is active when the edges are roughly at $\pm 115ps$. When the delay between the edges is more than the activation range, the outputs are passed through a delay and to the output. That is seen on the graph by a dip followed by a linear transfer function. The delay is $\approx 350ps$ which is implemented by passive gates.

To compare the performance of the TAPD with the performance of a conventional binary PD, the two inputs are set to have a small frequency difference, Δf , and the transient measurement was run while observing the outputs of the TAPD and PD. Figure 4.15 shows the simplified measurement setup. The small frequency offset between the two inputs ensures that the edges of the two clocks are getting close and eventually pass each other. When the edges are close, the TA is activated and the distance between the edges is extended. The output of the conventional PD and TAPD is then

Figure 4.15: Simplified measurement setup of TAPD.

observed for the time that toggling happens. This happens when the edges of the input clocks pass each other, hence the output of each phase detector changes state or toggles. From Bang-Bang PD it can be viewed as the early and late clocks have changed position.

The objective of this test is to determine which phase detector toggles first. This indicates that the corresponding phase detector has a higher resolution and can make a faster decision compared to the other phase detector. In other word, this shows the margin of the input timing requirements that avoids metastability. The measured output of the TAPD and PD under this test is shown in Figure 4.16. As can be seen, for the same input, the output of the TAPD toggles $130ns$ earlier than PD which equals 39 cycles for this measurement at input frequency of $300MHz$.

Although this test shows that the TAPD has a better resolution compared to a conventional PD, the absolute improvement depends on the testing setup, meaning how fast the edges pass each other which depends on Δf .

Figure 4.16: Measured output of the TAPD compared with output of PD when the edges are crossing.

4.3.4 TAPD in Digital Loop

The TAPD designed and measured in the previous chapter was to prove the concept of the performance improvement by using a time-amplifier in the binary phase detector. In this section the same concept is used to show the performance improvement in the digital loop. The TAPD and the rest of the digital PLL are designed and simulated in 32nm CMOS technology.

The TA designed in CMOS technology has a linear gain of $A_{TA} = 20$ around zero crossing covering $\pm 10ps$ and non-linear higher gain covering up to $\pm 25ps$. The simulated transfer function of the TAPD is shown in Figure 4.17.

Figure 4.18 shows the block diagram of the digital BBPLL including TAPD as phase detector. The digital circuitry is designed using standard library cells and the oscillator is a behavioral model. A 12-bit Digital-to-Analog Converter is used to convert the output of the filter to an analog

Figure 4.17: Simulated transfer function of TAPD designed in 32nm CMOS technology.

value for the VCO.

The loop is designed for $F_{VCO} = 2.5GHz$ and $F_{REF} = 312.5MHz$ which means $N = 8$. The delay throughout the loop is about 1 cycle, so it is assumed that $D = 1$. The remaining of the parameters are as in (4.4).

Figure 4.18: Block diagram of the digital BBPLL with TAPD.

$$\left\{ \begin{array}{l} K_p = 2^{-10} \\ K_i = 2^{-12} \rightarrow K_{ieff} = \frac{K_i}{2^4} \\ K_{vco} = 200 \frac{MHz}{V} \\ K_{DCO} = \frac{K_{VCO}}{2^{12}} \approx 50 \frac{KHz}{LSB} \\ K_T = -K_{VCO} T^2_{VCO} = -32 \frac{ps}{V} \end{array} \right. \quad (4.4)$$

Assuming uniform distribution and ideal PD, K_{PD} is:

$$K_{PD} = \frac{1}{\sigma_{PD}} \quad (4.5)$$

where σ_{PD} is defined as:

$$\sigma_{PD} = \frac{(D+1)K_P N K_T}{\sqrt{3}} = 445 fs \quad (4.6)$$

The transfer function of the BBPLL for the above parameters is shown in Figure 4.19. The loop has a bandwidth of $258 kHz$.

The main interest of employing TAPD in the BBPLL is to reduce the spurious tone at the output which is related to the resolution of the phase detector. In the circuit, a Current Mode Logic (CML) flip-flop is used as a regular binary phase detector. This flip-flop has timing margin of $t_{margin} = 1.7ps$. From (3.7), the radius of the limit cycle generated due to PD resolution is:

$$R = \lceil \frac{t_{margin}}{N K_p K_T} \rceil = \lceil \frac{1.7ps}{8 \times 2^{-10} \times 32ps} \rceil = 7 \quad (4.7)$$

and hence the main spurious tones should be located at:

Figure 4.19: Transfer function of the BBPLL with parameters as in 4.4 and an ideal phase detector, (top) open loop gain, (bottom) closed loop gain.

$$f_{spur} = \pm \frac{F_{REF}}{2R} = \pm 22.3 MHz \quad (4.8)$$

The additional delay in number of cycles caused by PD resolution can be calculated from (3.8) and (3.15) which results in $M = 6$. As a result the loop bandwidth is reduced as shown in Figure 4.20 (top). As can be seen the bandwidth is reduced to 88 kHz. In the linearized model the gain of the phase detector is defined as in (4.5) where:

$$\sigma_{PD} = 2t_{margin}/\sqrt{12} \quad (4.9)$$

By using the above value for phase detector gain then the two models merged as shown in 4.20 (bottom). The model including additional delay however, provides information on spurious tones as well.

Figure 4.20: Transfer function of the BBPLL with (top) additional loop delay of $M=6$ cycles and (bottom) with linearized model of PD with $\sigma_{PD} = 2t_{margin}/\sqrt{12}$.

Figure 4.21: Spectrum of the VCO for the loop with (a) PD and (b) TAPD.

The loop is simulated with both PD and TAPD. The spectrum of the VCO clock is shown in Figure 4.21 (a) for the loop with PD and Figure 4.21(b) with TAPD. Comparing f_{spur} from (3.13) and Figure 4.21 (a) shows close estimation from calculation. As can be seen from both graphs, the TAPD results has the spurious tone 3 times further away from the fundamental compared to PD tones and has less power. Also, since location of the spurs and the deterministic jitter both relate to the radius of the limit cycle, from (3.13), the radius of the limit cycle in TAPD loop can be calculated as:

$$R = \frac{F_{REF}}{2f_{spur}} = \frac{312MHz}{2 \times 78MHz} = 2 \quad (4.10)$$

then from (3.7) the resolution of the TAPD is obtained as:

$$t_{margin} = RNK_TK_p = 512fs \quad (4.11)$$

The analysis above shows that the resolution of the PD is improved by 3.3 times by using a time amplifier.

Another point to note here is that the delay in the loop causes bandwidth reduction as seen in Figure 4.20. In the linear analysis the bandwidth of the loop depends inversely on the timing margin of the phase detector as shown in (4.5). We saw that employing the time amplifier reduces the delay in the loop by reducing the timing margin of the phase detector. Similarly this can be viewed in the linearized model by increased loop bandwidth due to increased gain of the phase detector. The bandwidth of the BBPLL based on the linearized model is, [37]:

$$\omega_u = \frac{NK_pK_T}{T_rt_{margin}} \quad (4.12)$$

where T_r is the period of the reference clock. This expression shows that the reducing timing margin of the phase detector increases the bandwidth of the loop. Also assuming time amplifier is not used, achieving the same bandwidth when the timing margin of the phase detector is high, requires increase of either K_p or K_T which neither one is preferable since increasing either one results in increasing the output jitter.

4.4 Summary

In the first section a brief jitter budgeting for the digital PLLs was explained. This methodology helps with including all the possible sources of error in cal-

culations and making the necessary modifications to meet the jitter target. In the last two sections of this chapter two techniques to improve the performance of the digital BBPLL by improving the resolution of the phase detector was introduced. In the first technique, dithering is used to randomize the phase error detection in order to break the repetitive patterns present on the oscillator control signal. In this technique software is used to generate a bit stream which was shaped by a $\Sigma\Delta$ modulator was used instead of the reference clock. In the second technique, a time-amplifier was used to increase the resolution of the phase detector by increasing the time difference between the edges of the reference clock and the output clock which prevents the phase detector from operating in metastable region.

Chapter 5

Multi-bit High-Resolution Transmission Line Based Phase Detector

In some applications in which the linear phase detector is preferred or required, such as fractional frequency synthesizers, the Bang-Bang PLL is not useful and TDC-based phase detectors are the preferred choice. However as mentioned in Chapter 2, the conventional TDC phase detectors pose several limitations such as limited phase error resolution depending on the technology and PVT dependent variations in performance which leads to the need for complicated and power hungry calibration schemes. In this chapter, a novel multi-bit phase detector is introduced that provides high timing resolution which is independent of the process variations. This phase detector is designed to be used in high-speed applications where jitter budgeting is very stringent. The design is implemented in 28nm CMOS-SOI technology.

Figure 5.1: Transmission Delay Line based phase detector.

5.1 Architecture of the Transmission Delay Line Based Phase Detector

Figure 5.1 shows the architecture of the Transmission Delay Line (TDL) based phase detector. Similar to the TDC based phase detector, the reference clock is passed through a chain of delay elements and the output of each delay element is compared with the feedback clock using a binary phase detector and the output is a digital code which contains phase error information between the two clocks. The delayed version of the reference clock in TDL based phase detector is generated using a transmission line where the delayed version of the clock is taken from various taps of the line, as shown in the Figure. An example of the output of the phase detector is shown in Figure 5.2. Similar to the Bang-Bang phase detector, each binary phase detector determines if the feedback clock is leading or lagging the corresponding delayed reference clock. Since the delay between the two taps of the transmission line is small, these comparators have to be able to make a decision when the edges of the two clocks are very close. Even though a flip flop can

Figure 5.2: Output of the TDL phase detector.

be used as a phase comparator, in this application however, the speed of the operation of the flip flop is not fast enough to make a correct decision. As explained in Chapter 3, a flip flop can enter into the metastable region if the clock edges are close, hence in designing the phase comparator for TDL, a primary consideration is that the timing threshold of the comparator should be much smaller than the resolution of the TDL. The design for fast operation requires the use of small devices which in part poses another challenge which is the timing mismatch offset of the comparators that can degrade the performance of the phase detector. The design of a fast phase comparator, or an arbiter, will be discussed in later sections of this chapter and the detailed

Figure 5.3: Transmission line based delay line.

analysis of the effect of the mismatch of the arbiters on the performance of the phase detector is studied in Chapter 6.

5.2 Transmission Delay Line

Figure 5.3 shows how a transmission line is used to provide different phases of the input clock. This technique is useful for applications that require fine timing resolution at the cost of die area. Another advantage of the TDL phase detector compared to the TDC is that the arrival time of the signal to each tap is independent from variation of the buffers or arbiters whereas in the TDC the arrival time of the signal depends on the delay variation of all

the delay elements before the tap.

The range of the TDL operation, in the sense of the timing coverage, depends on the frequency of operation, design technology and the available silicon area. Another advantage of the TDL based phase detector is that since the delayed clocks are generated only by metal interconnects, the PVT variation of the delay is far more stable compared to the delay line generated by active components.

There are two main concerns when designing the TDL, the termination and the input drive. If the transmission line is not properly terminated, each delayed signal, reflects back and creates significant phase shift in the transmission line to the point that the order of the delayed signal could become completely random. This will cause the phase detector to generate wrong phase error which can increase the total jitter in the PLL.

Since each tap of the transmission line is connected to a binary phase detector, the input driver should be able to drive the phase detectors without excessive increase of the rise/fall time of the input clock. If the transmission line is terminated, the resistor is also loading the driver.

When the transmission line is terminated, a path from supply to the ground is generated that draws a constant current. So when designing the transmission line, minimizing this current should be considered. Since the transmission line can be matched to any arbitrary impedance, the width of the line is selected as narrow as possible to increase the impedance and hence to reduce the static current.

5.2.1 Modelling of the Transmission Line as a Delay Line

The transmission line is designed in an 8-metal technology as a microstripline, where the first metal layer is used as the ground shield and the last copper metal layer is used for the microstripline. For this specific design the available die area allowed 0.5mm in length. The frequency of operation is specified at $312MHz$ and the width of the transmission line is selected as minimum as possible to provide a high impedance line. To accommodate the 0.5mm line in the given area and to achieve a high impedance, an octagonal shape was chosen for the line as shown in Figure 5.3 with minimum possible width of $w_{TL} = 1\mu m$. For $w_{TL} = 1\mu m$, $\frac{w_{TL}}{h} = 0.22$ where h is the substrate thickness and the relative permittivity, $\epsilon_r = 4.3$, the line characteristics are as follow [38]:

$$\begin{aligned} q &\approx 0.575 \\ \epsilon_{eff} &= 1 + q \cdot (\epsilon_r - 1) = 1 + 0.575 \times 3.3 = 2.9 \end{aligned} \tag{5.1}$$

The impedance of a line is:

$$Z_o = \frac{Z_{o1}}{\sqrt{\epsilon_{eff}}} = \frac{210\Omega}{\sqrt{2.9}} \approx 123\Omega \tag{5.2}$$

The unit value of lumped components of the TL are obtained as in (5.3) and the lumped model is shown in Figure 5.4.

$$\begin{aligned}
v_p &= \frac{c}{\sqrt{\epsilon_{eff}}} = \frac{8 \times 10^8}{\sqrt{2.9}} = 1.76 \times 10^8 \frac{m}{s} \\
\bar{L} &= \frac{Z_o}{v_p} = \frac{123}{1.76 \times 10^8} = 700 \frac{nH}{m} \rightarrow L = 350 pH \\
\bar{C} &= \frac{1}{Z_o v_p} = \frac{1}{118 \times 1.6 \times 10^8} = 46 \frac{pF}{m} \rightarrow C = 23 fF \\
R &= R_s \cdot \frac{l_{TL}}{w_{TL}} = 0.025 \cdot \frac{500}{1} = 12.5 \Omega
\end{aligned} \tag{5.3}$$

Figure 5.4: A simple model of a section of the microstripline.

At this frequency the wavelength is:

$$\lambda_{eff} = \frac{v_p}{f} \left(\frac{ms^{-1}}{Hz} \right) = \frac{1.76 \times 10^8}{312 \times 10^6} \approx 0.5637m \tag{5.4}$$

So the delay through $0.5mm$ of transmission line is:

$$t_{delay} = \frac{l_{TL}}{f \times \lambda_{eff}} = \frac{0.5 \times 10^{-3}}{312 \times 10^6 \times 0.5637} \approx 2.84ps \tag{5.5}$$

For this transmission line the total delay is $2.84ps$ and depending on the application the number of taps can be selected at a linear distance from each other. In this design, 32 taps are placed with $15\mu m$ spacing. This spacing provides $92fs$ of delay between each two taps.

The model is scaled to the length of the individual strips for simple simulation since using the EM simulators with an n-port structure can be complicated. The microstripline is also modeled by EMX, a commercial 3-D

electromagnetic simulator and modeler. The comparison of the cascaded calculated model of the TL and the model generated by EMX is shown in Figure 5.5.

Figure 5.5: Comparison between calculated impedance and EMX model of the transmission line.

To ensure that the reflection coefficient, Γ , is minimized, the transmission line has a resistive termination by $R_T = 140\Omega$. R_T is slightly bigger than the line impedance, this is done to reduce the current through the transmission line and R_T while keeping Γ small.

The transient simulation result of the unloaded EMX model of the transmission line with a few pins tapped out as sample is shown in Figure 5.6. As

Figure 5.6: Transient simulation result of the EMX model of the transmission line.

can be seen the total delay of the transmission line is about 2.9ps .

One of the limitations of the transmission line when used with a sharp square wave is that the behavior of the transmission line differs for the harmonics of the main tone of the signal and it can have significant impact on the performance of the phase detector. On one side, the sharp edges are preferred for fast decision making and on the other hand, the different phases coming out of the transmission line could be random and this issue is magni-

Figure 5.7: Behavior of the transmission line when excited by a sharp square wave.

fied if the signals are reflected. An example of the “inverted random phases” is shown in Figure 5.7.

Each of the taps of the transmission delay line is connected to a phase comparator that decides which input signal has arrived earlier. When the transmission line is loaded by the comparators, the characteristics, such as the total delay and its timing resolution are changed. Hence a few iterations of design and modeling are needed for the desired performance. Loading the transmission line helps with a more unified characteristics as the edges are

Figure 5.8: Schematic of the arbiter used as a phase comparator.

smoothed out. In the next section designing of the phase comparators is described.

5.3 Design of the Arbiter as Phase Comparator

The arbiter was introduced in [39] where it was used for fine resolution time measurement. The arbiter acts as an edge comparator, indicating which input has arrived earlier. The schematic shown in Figure 5.8 is a modified schematic of the arbiter used in [40]. The operation of the arbiter follows that of the StrongARM latch, introduced in [41]. The difference between the strongARM latch and the arbiter as designed here is that the arbiter does not have a separate clock. The *OR* gate here facilitates the pre-charge phase. Assuming both inputs are low. As long as the two inputs remain low the two outputs, *Out1* and *Out2* are pre-charged to VDD by P3 and P4. If one

Figure 5.9: Output of the arbiter, nodes *Out1* and *Out2*, shown for different input timing.

of the inputs, assuming *In1*, goes to high at time t_1 , then P3 and P4 are turned off and N3 is turned on which starts to discharge node *Out1*. This phase of the operation can be considered as the “amplification” phase. In this phase, the gain of the positive feedback determines the performance and the resolution of the arbiter. Assuming the time it takes to fully discharge node *Out1* is $t_{dischrg}$, if the second input, here *In2*, goes from low to high at t_2 such that $t_2 \ll t_{dischrg}$, then node *Out1* is not fully discharged before N2 and hence N4 is turned on. In this case the gain of the NMOS cross-coupled pair may not be strong enough to turn on the PMOS cross-coupled pair and since N2 is turned on too, node *Out2* starts to discharge as well and the two output become the same. In other words, the latch can enter the metastable region. Eventually the outputs settle to a stable state but due to low gain it takes longer, which can be problematic for the following circuitry. This

Figure 5.10: Arbiter with samplers.

behavior is shown in Figure 5.9. The plot shows the output of the arbiter where one clock edge is kept constant and the other clock edge is swept such that $0 \leq \Delta t \leq 1ps$, where Δt is the delay between the two clocks. As can be seen, depending on the delay between the two clocks, the settling time of the output differs. For small delay the two outputs stay equal which indicates a decision cannot be made at that point and the result is not reliable.

The mechanism explained above determines the timing resolution of the arbiter. Following the discussion in Chapter 3, the timing resolution of the binary phase detector affects the performance of the digital loop by increasing the delay and hence increasing the accumulated jitter. The advantage of the arbiter over a conventional latch is that the arbiter can be designed for very fast operation which results in a superior performance over a conventional binary phase detector in the loop.

Since the output toggles between high and low logic and it is desired to have a constant level at the output, similar to latch, the arbiter should be followed by a sampling block such as a flip flop or an RS latch. The top level schematic is shown in Figure 5.10. The output of the arbiter for a moving

Figure 5.11: Output of the arbiter when one input clock is swept with respect to the other one.

clock with respect to the other one is shown in Figure 5.11. In this simulation, the period of the input clocks differ by $1ns$, in $100ns$, so when simulation is running for long time the clock edges surpass each other and the output of the arbiter is changed. The schematic of the arbiter with transistor sizing for the above simulation is shown in Figure 5.12.

5.3.1 Flash Transmission Delay Line Based Phase Detector

The transmission delay line, described in Section 5.2, and the arbiter are used to design a 32-bit flash TDL based PD. Each tap of the TDL is connected to one of the inputs of an arbiter and the other input is connected to the second input of the arbiters. To ensure the layout routing does not affect the performance, in designing the layout it should be taken into account that the

Figure 5.12: Schematic of the arbiter with transistor sizing.

interconnects have similar length so that the delay between the taps of the transmission line remains the same for all taps. This is the main reason for choosing an octagonal shape for the TDL as shown in Figure 5.13. Similarly the second clock is connected to the center of the TDL and is distributed evenly to arbiters.

The TDL phase detector has a timing coverage of t_r which is equal to the transmission line propagation delay. If the time difference between the two input clocks is greater than t_r , then TDL operates as a Bang-Bang phase detector with all bits at +1 or -1. If the time difference between the edges of the two input clocks is smaller than t_r , then ideally the output of the phase detector is as shown in Figure 5.2 with only one transition occurring. One advantage of the flash TDL phase detector over conventional Bang-Bang phase detector is that the output consists of N arbiters producing an N-bit output code. If the edge of the clocks are close to each other such that

Figure 5.13: Layout of the flash phase detector with TDL shown as dark octagonal line connected to the arbiters.

the timing requirement of the arbiter is violated, only one output is affected which results in an error with a resolution of $1/N$. However if the same happens in a Bang-Bang loop, since the phase error has only one bit, the error impact is bigger than in the flash TDL loop. In reality noise and timing mismatch of the arbiters give rise to limitations in the performance. As a general rule, a transition happens if $\Delta_t \gg n + t_{os}$ where Δ_t is the resolution of the TDL. In the next chapter the performance of the flash TDL phase

detector is analytically investigated for the effect of the timing mismatch on the performance of the phase detector.

5.4 Summary

In this chapter a new multi-bit phase detector based on transmission delay line was introduced and design of the arbiters used as phase comparator was explored. The TDL PD is intended to replace the TDC in digital phase locked loop which require high resolution.

Chapter 6

Performance of the Flash Transmission Delay Line Phase Detector

The Performance of the TDL phase detector directly affects the performance of the PLL in defining properties such as gain, bandwidth and settling time. Two of the most important performance merits of the TDL are its gain, which is related to the resolution of the TDL and its monotonicity and linearity. In this chapter, stochastic analysis is used to analyze the performance of the TDL PD.

6.1 Gain of the TDL Phase Detector

To obtain the gain first the timing resolution of the phase detector has to be determined. The resolution of the line, T_{res} , is equal to the delay between

the two adjacent taps of the transmission line as defined below:

$$T_{res-ideal} = t_n - t_{n-1} = \Delta_t \quad (6.1)$$

As shown in previous chapter, the delay between the two taps depends on the length of the line between them. However, since each tap is connected to an arbiter, the effective resolution of the line is affected by the timing mismatch of the arbiters.

Assuming the timing mismatch of the arbiters has a Gaussian distribution with standard deviation of σ_n , the resolution deviates from (6.1) as shown below:

$$T_{res} = (t_n + n_n) - (t_{n-1} + n_{n+1}) = \Delta_t + n_{tot} \quad (6.2)$$

where n is a positive or negative error corresponding to the timing mismatch of the arbiters. As shown in Figure 6.1, since both edges follow a Gaussian distribution and are uncorrelated events, hence the difference of the edges is also a Gaussian distribution defined as in (6.3), with a mean value of $t_n - t_{n-1} = \Delta_t$ and standard deviation of $\sqrt{2}\sigma_n$ and the probability density function (PDF) of $f_t(t)$ as in (6.4) where t is a random variable.

$$\begin{cases} N_{t_{n-1}} = N(t_{n-1}, \sigma_n^2) \\ N_{t_n} = N(t_n, \sigma_n^2) \\ N_{T_{res}} = N_{t_n} - N_{t_{n-1}} = N(\Delta_t, 2\sigma_n^2) \end{cases} \quad (6.3)$$

$$Dist.T_{res}(t) = \frac{1}{2\sigma_n\sqrt{\pi}} e^{\frac{-(t-\Delta_t)^2}{4\sigma_n^2}} \quad (6.4)$$

In Figure 6.2 the distribution of T_{res} , as the difference between two adjacent taps, for low and high σ_n is shown.

Figure 6.1: Effect of the timing mismatch of the arbiters on the delay of the line

Figure 6.2: Normal distribution of T_{res} for (a) $\sigma_n = 0.4\Delta_t$ and (b) $\sigma_n = 0.8\Delta_t$.

With T_{res} following a distribution as shown above the effective resolution can be defined as:

$$T_{ref-eff} = T_{res} + 2x \cdot \sqrt{2}\sigma_n \quad (6.5)$$

where x can be defined based on accuracy and yield needed for the application. In most applications x is defined between 3 and 6 for a high yield.

The gain of the TDL phase detector is defined similar to that of TDC phase detector as:

$$G_{TDL} = \frac{1}{T_{res-eff}} \quad (6.6)$$

Figure 6.3: Output code of the TDL for (a) $\sigma_n = 0.4\Delta_t$ and (b) $\sigma_n = 0.8\Delta_t$ compared with ideal code (thick black).

Depending on the coming edge and σ_n the resolution of the TDL is changing. As σ_n increases the resolution reduces which means the gain of TDC is reduced. Figure 6.3 shows the comparison of the output code of the TDL over input time for two distribution with $\sigma_n = 0.4\Delta_t$ and $\sigma_n = 0.8\Delta_t$. For these simulations a MATLAB model of the flash based phase detector is used where the input time is passed over the range of the phase detector and assuming the timing mismatch with standard deviation of σ_n affecting the timing. Each code is simulated 500 times.

In [39] and [42], the random mismatch of the arbiters is used to design a high-resolution TDC by using stochastic technique. In these works, N arbiters are connected to two input signals in parallel and assuming the slope of the signals remains constant, the result is a unique TDC level due to the mismatch of the arbiters. With N arbiters, an M -bit TDC phase detector is created such that $N = 2^M - 1$, [42]. In this case, TDC resolution depends on the number of arbiters and σ_n which is the standard deviation of the timing mismatch of the arbiters.

In an ideal phase detector the transition from one code to the next has a slope of infinity, creating a “stair case” transfer function. In real situation however, the slope of the transition reduces due to the spread of the code. The slope of the transition is equal to the cumulative distribution function (CDF) of the distribution of the transmission line resolution, shown in (6.4).

6.2 Monotonicity of the Output Code of the TDL Phase Detector

Another problem that rises in the presence of the mismatch is the occurrence of “bubbles”, meaning the output code has more than one transition, as shown in Figure 6.4. This problem affects the monotonicity of the flash TDC in a similar way as in flash ADCs. Since the resolution follows a normal distribution as shown in Figure 6.2 (a), the probability of the presence of the bubble increases as the tails of the adjacent distributions overlap. As shown in Figure 6.2 (b), for higher σ the tail of the distribution can spill over several taps, making the probability of detecting a wrong phase error very high. Assuming in Figure 6.5, the total number of taps is N for a given transmission line with resolution of $T_{res} = \Delta_t$ and assuming that the probability of a correct transition from “1” to “0”, $P(10)$, is defined as, [39]:

$$P(10)_{ij} = P(t_i + n_i < t < t_j + n_j) \quad (6.7)$$

This implies:

Figure 6.4: Existence of the bubble in the output code.

Figure 6.5: A transition happening at $t_i < t < t_j$.

$$\begin{cases} \forall \quad t_{ii} < t_i \quad t_{ii} + n_{ii} < t \quad \text{and} \\ \forall \quad t_{jj} > t_j \quad t_{jj} + n_{jj} > t \end{cases} \quad (6.8)$$

where n_{ii} denotes the timing noise due to the mismatch of the arbiter connected to the ii -th tap. Since the mismatch in devices is time invariant and has a Gaussian distribution, hence the noise that is denoted here is also time-invariant and follows a Gaussian distribution.

A bubble happens if the condition in (6.8) is not met. Assuming the incoming clock edge is at time t and it falls between taps i and j such that $t_i < t < t_j$. The probability that the bubble happen is as follows, assuming

n_i and n_j are the timing noise due to the mismatch:

$$\left\{ \begin{array}{ll} \text{if } t_i + n_i > t \text{ and } t_j + n_j > t \rightarrow \text{no bubble, no transition at } t_{ij} \\ \text{if } t_i + n_i < t \text{ and } t_j + n_j > t \rightarrow \text{no bubble, transition at } t_{ij} \\ \text{if } t_i + n_i > t \text{ and } t_j + n_j < t \rightarrow \text{bubble} \\ \text{if } t_i + n_i < t \text{ and } t_j + n_j < t \rightarrow \text{no bubble, no transition at } t_{ij} \end{array} \right. \quad (6.9)$$

From above, it can be seen that only one condition results in the bubble. Although other conditions may result in a wrong or skewed transition, they do not necessarily imply the existence of the bubble. In this case, the probability of the bubble, $P(01)_{ij}$ can be written as:

$$\begin{aligned} P(01)_{i,j} &= P[t_i + n_i > t \text{ \&\& } t_j + n_j < t] = P[t_i + n_i > t] \cdot P[t_j + n_j < t] \\ &= P[i \cdot \Delta_t + n_i > t] \cdot P[j \cdot \Delta_t + n_j < t] = [1 - \Phi_i(t)] \cdot \Phi_j(t) \end{aligned} \quad (6.10)$$

where $\Phi(x)$ denotes the cumulative distribution function, CDF, of x as:

$$\Phi_n(x) = \frac{1}{2} [1 + \text{erf}(\frac{x - \mu}{\sigma\sqrt{2}})] \quad (6.11)$$

with error function, $\text{erf}(x)$, defined as:

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt \quad (6.12)$$

Assuming, $n_x \in N(0, \sigma_n^2)$, equation (6.10) can be written as:

$$P(01)_{i,j} = \frac{1}{4} (1 - \text{erf}(\frac{t - i \cdot \Delta_t}{\sigma_n \sqrt{2}})) \cdot (1 + \text{erf}(\frac{t - j \cdot \Delta_t}{\sigma_n \sqrt{2}})) \quad (6.13)$$

It should be noted that a wrong decision at the first and the last tap does not result in a bubble, rather, it shifts the decision (the output code).

The bubble happens only if the second taps make a wrong decision while the first tap also makes a wrong decision. Since the probability that a bubble happens before or at the beginning of the TDL range, is insignificant and has small effect on the overall performance, for a close estimation, these probabilities can be ignored. Hence, the first and the last taps' probability are not included in the calculation of the bubble probability. With this estimation the probability of the bubbles of the taps where, $x \neq i, j$, is

$$\begin{aligned} P(01)_{|x \neq i, j} &= 1 - P(10) = 1 - [P(t_1 + n_1 < t).P(t_2 + n_2 < t). \\ &\dots P(t_{i-1} + n_{i-1} < t).P(t_{j+1} + n_{j+1} > t). \\ &\dots P(t_{N-2} + n_{N-2} > t).P(t_{N-1} + n_{N-1} > t)] \end{aligned} \quad (6.14)$$

If the time intervals are written in Δ_t and assuming $t_0 = 0$ for simplicity, (6.14) can be written as:

$$\begin{aligned} P(01)_{|x \neq i, j} &= 1 - \{P(\Delta_t + n_1 < t) \cdot P(2\Delta_t + n_2 < t) \dots \\ &\cdot P((i-1)\Delta_t + n_{i-1} < t) \cdot [1 - P((j+1)\Delta_t + n_{j+1} < t)] \dots \\ &\cdot [1 - P((N-2)\Delta_t + n_{N-2} < t)] \cdot [1 - P((N-1)\Delta_t + n_{N-1} < t)]\} \end{aligned} \quad (6.15)$$

and using the CDF,

$$P(01)_{|x \neq i, j} = 1 - \frac{1}{2^{N-3}} \cdot \prod_{x=1}^{i-1} (1 + \text{erf}(\frac{t - x\Delta_t}{\sigma_n \sqrt{2}})) \cdot \prod_{x=j+1}^{N-1} (1 - \text{erf}(\frac{t - x\Delta_t}{\sigma_n \sqrt{2}})) \quad (6.16)$$

where,

$$i \cdot \Delta_t < t < j \cdot \Delta_t \quad (6.17)$$

The final bubble probability is:

$$P(01)_{|bubble} = P(01)_{|x \neq i,j} \cdot P(01)_{|i,j} \quad (6.18)$$

As shown in (6.16), the probability of a bubble depends on the number of the taps, N , the delay between the taps (TDL resolution), Δ_t , and standard deviation of the noise distribution, σ_n .

For higher accuracy, the probability of the bubbles at the edge of the TDL range should be included in (6.18) as follow:

$$\begin{cases} \forall \quad t < t_0 & P(10)_{|x < t_0} = 1 - \Phi_x(t) \\ t = t_0 & P(01)_{|t_0} = 1 - \Phi_x(t) \\ t = t_1 = \Delta_t & P(01)_{|t_1} = \Phi_x(t) \end{cases} \quad (6.19)$$

and

$$\begin{cases} \forall \quad t > t_N & P(10)_{|x > t_N} = \Phi_x(t) \\ t = t_{N-1} = (N-1)\Delta_t & P(01)_{|t_{N-1}} = 1 - \Phi_x(t) \\ t = t_N = N\Delta_t & P(01)_{|t_N} = \Phi_x(t) \end{cases} \quad (6.20)$$

and the probability of the bubble outside of the TDL range is:

$$P(01)_{tail} = [1 - P(10)_{|x < t_0}] \cdot P(01)_{|t_0} \cdot P(01)_{|t_1} \cdot [1 - P(10)_{|x > t_N}] \cdot P(01)_{|t_{N-1}} \cdot P(01)_{|t_N} \quad (6.21)$$

The total probability of the bubble including is:

$$P(01)_{|bubble-tail} = P(01)_{|x \neq i,j} \cdot P(01)_{|i,j} \cdot P(01)_{tail} \quad (6.22)$$

Figure 6.6: Probability of the bubble using equation, (6.22) (black) and (6.18) (magenta) for $\sigma_n = 0.4\Delta_t$ (top) and $\sigma_n = 0.8\Delta_t$ (bottom). The two method merge as can be seen except for the skirt of the probability curve.

A comparison of the probability obtained from (6.18) and (6.22) is shown in Figure 6.6 in magenta and black lines respectively. In the figure the probability is shown for two values of σ_n , as top: $\sigma_n = 0.4\Delta_t$ and bottom: $\sigma_n = 0.8\Delta_t$. It can be seen in the figure that the difference between the two equations only affects the tail where it is more spread using (6.22) compared to (6.18). The two equations match within the TDL range. Hence the estimated probability as in (6.18) can be safely used for performance evaluation.

Another property that is observed from Figure 6.6 is the shape of the probability. Considering the ratio of σ_n and Δ_t , for large σ_n , the probability

Figure 6.7: Probability of the bubble, (black) MATLAB random simulation (10000 runs) , (magenta) analytic results using (6.18) for $\sigma_n = 0.8\Delta_t$.

of the bubble increases as the transition time gets closer to the taps. This is due to the spread of the distribution which increases the probability of “exchanged” taps. However for small σ_n , the probability of the bubble is higher between the two taps since the distribution is narrow hence the chance of the bubble at the taps where the transition happens is small.

To show the validity of the analysis, MATLAB is used to generate a random mismatch with normal distribution $N(t_x, \sigma_n^2)$ where t_x is the time at each tap and σ_n is the standard deviation of the distribution of the mismatch. Figure 6.7 shows MATLAB simulation result, shown in black, compared with the result obtained from (6.18), shown in magenta. For this simulation, $\sigma_n = 0.8\Delta_t$. In this graph, the taps are located at $0.1x$ and as can be seen, the probability of the bubble increases as the transition time gets closer to

Figure 6.8: The probability of more than one bubble in the code, compared to the probability of a single bubble for $\sigma_n = 0.8\Delta_t$.

the taps.

The above analysis is done for existence of a single bubble in the code. However there is also the possibility of multiple bubbles in the code. Using MATLAB simulation, the probability of multiple bubbles is observed and an example is shown in Figure 6.8 for $\sigma_n = 0.8\Delta_t$. As can be seen, the probability of multiple bubbles is very small compared to only one bubble, hence, the overall performance can be closely estimated by the probability of a single bubble.

Assuming a single bubble, the mean of the probability of the bubble versus σ_n/Δ_t is shown in Figure 6.9. The mean can be used for fast estimation of the

Figure 6.9: Mean of the bubble probability over $\frac{\sigma_n}{\Delta_t}$.

probability since the ripple has a small amplitude around the mean. Using curve fitting techniques, the probability for this case is fitted to a polynomial as follow:

$$P(01)_{Mean-est} = -0.2229\left(\frac{\sigma_n}{\Delta_t}\right)^3 + 0.7464\left(\frac{\sigma_n}{\Delta_t}\right)^2 - 0.3174\left(\frac{\sigma_n}{\Delta_t}\right) + 0.0315 \quad (6.23)$$

6.3 Linearity of the Phase Detector

The linearity of the TDL is measured by the standard factors such as Differential Non-Linearity (DNL) and Integral Non-Linearity (INL). These factors show how the performance of the TDL deviates from ideal performance due to mismatch. They are also important as measures of estimating silicon yield in the production.

6.3.1 Differential Non-Linearity

Similar to TDC, the DLN is defined as, [43]:

$$DNL = \frac{t_{n(eff)} - t_{n-1(eff)} - \Delta_t}{\Delta_t} \quad (6.24)$$

Assuming the timing mismatch of the arbiters and same as in (6.2), we have:

$$t_{n(eff)} - t_{n-1(eff)} = t_n + n_n - (t_{n-1} + n_{n-1}) = \Delta_t + n_{tot} \quad (6.25)$$

where Δ_t is the delay between the two taps of the TDL and n_{tot} is the total timing noise due to the mismatch of the arbiters. Then the DNL can be written as:

$$DNL = \frac{\Delta_t + n_{tot} - \Delta_t}{\Delta_t} = \frac{n_{tot}}{\Delta_t} \quad (6.26)$$

where $n_{tot} \in N(0, 2\sigma_n^2)$. This equation shows that the DNL directly relates to σ_n and the resolution of the TDL. As it is accepted in the industry, the DNL should be limited to $\pm 0.5LSB$. Hence,

$$-\frac{1}{2} \leq \frac{n_{tot}}{\Delta_t} \leq \frac{1}{2} \quad (6.27)$$

and the probability that n_{tot} falls into the limit is:

$$P(DNL) = P\left(-\frac{\Delta_t}{2} \leq n_{tot} \leq \frac{\Delta_t}{2}\right) = \int_{-\frac{\Delta_t}{2}}^{\frac{\Delta_t}{2}} \frac{1}{\sqrt{2\pi}\sigma_n} e^{-\frac{t^2}{2\sigma_n^2}} dt \quad (6.28)$$

Defining, $x = \frac{t}{\sqrt{2}\sigma_n}$ and $\sigma_n' = \sqrt{2}\sigma_n$,

$$P(DNL) = \int_{-\frac{\Delta_t}{2\sqrt{2}\sigma_n}}^{\frac{\Delta_t}{2\sqrt{2}\sigma_n}} \frac{1}{\sqrt{\pi}} e^{-x^2} dx = erf\left(\frac{\Delta_t}{4\sigma_n}\right) \quad (6.29)$$

P(x)	x
0.8000	0.9062
0.8200	0.9481
0.8400	0.9935
0.8600	1.0435
0.8800	1.0994
0.9000	1.1631
0.9200	1.2379
0.9400	1.3299
0.9600	1.4522
0.9800	1.6450
1.0000	Inf

Table 6.1: Inverse error function values for given probability.

Since the interest is to design the circuitry such that the DNL stays limited to $\pm 0.5LSB$, (6.29) can be used to obtain the maximum allowable σ_n for a given requirement using inverse error function, $erf^{-1}(x)$, which is available in most probability books. Examples of values of x for the given probability, $P(x)$ is shown in Table 6.1.

Assuming the required probability for $DNL \leq \pm 0.5LSB$ is $P(DNL) \geq 0.9$, from Table 6.1, $x \geq 1.1631$, which gives σ_n equal to:

$$x = \frac{\Delta_t}{4\sigma_n} \geq 1.1631 \rightarrow \sigma_n \leq 0.215\Delta_t \quad (6.30)$$

Assuming $\Delta_t = 0.1(ps)$, for $\sigma_n \leq 0.0215(ps)$ the probability of $DNL \leq$

Figure 6.10: DNL of the TDL PD with $\sigma_n = 0.15\Delta_t$ (top) and $\sigma_n = 0.25\Delta_t$ (bottom) over 1000 runs.

$\pm 0.5LSB$ is higher than 0.9. In Figure 6.10, the simulated DNL of the TDL for two values of σ_n as, $\sigma_n = 0.15\Delta_t$ (top) and $\sigma = 0.25\Delta_t$ (bottom) are shown. As can be seen in the top graph the DNL is closer to $\pm 0.5LSB$ where the probability in this case is well above 0.9 while the probability of the second simulation is about 0.85 which is also observed from the graph. These results are from 1000 runs of simulations.

The DNL is simulated over various σ/Δ_t and the result is shown in Figure 6.11, top. In this graph the simulated curve is compared to calculated curve using (6.29). Both graphs are matched which shows the validity of the equation.

Figure 6.11 (bottom) shows the probability of the DNL, zoomed for

Figure 6.11: (Top) Simulated probability of DNL (solid line) versus calculated probability (circles) over σ_n / Δ_t , (Bottom) zoomed probability of DNL σ_n / Δ_t .

high values to give an estimation of σ/Δ_t for 3σ , $P(-0.5LSB \leq DNL \leq +0.5LSB) \geq 0.997$, which from the graph, is achieved when $\sigma \leq 0.1\Delta_t$.

Design for High Yield

To achieve a high yield, it is important to design for small σ_n . This is especially critical for high resolution TDLs. When designing for high yield, it should be considered that the maximum DNL of each code stays below $0.5LSB$. Hence, the probability of an N-code phase detector is:

$$P(DNL_{codeword}) = P^N(DNL) = erf^N\left(\frac{\Delta_t}{4\sigma_n}\right) \quad (6.31)$$

where N is the number of the taps. This implies that more taps results in lower probability of DNL smaller than $0.5LSB$. To show the codeword probability and its dependency on N , a simulation is run for phase detectors with $N = 16$, $N = 32$ and $N = 64$ taps and the results are shown in Figure 6.12, top. The simulated graphs are compared with the calculated probability using, (6.31). Each simulation is ran 1000 times.

In the zoomed graph shown in 6.12, bottom, it can be seen that for $\sigma_n < 0.09\Delta_t$, the probability of the codeword meets yield of higher than 3σ .

6.3.2 Integral Non-Linearity

In this section the INL of the TDL phase detector is explored. By definition, the INL is the deviation of the output code from a straight line. Here the raw INL is defined as:

$$INL_{raw}(c_n) = \frac{t_n - n\Delta_t}{\Delta_t} \quad (6.32)$$

Figure 6.12: (Top) Simulated probability of DNL of the code word for TDL with $N=16$ (cross), $N=32$ (solid) and $N=64$ (dot) compared with theoretical calculation using (6.31), (Bottom) zoomed probability of DNL of the code word for high yield.

where, c_n is the $n - th$ element of the output code. In practice, there are several ways of defining a straight line as a reference, for example the reference line can be defined by connecting the end points or can be defined by a line that results in the best fit, [44]. Then the actual code is compensated for the offset and gain error such that an input time corresponding to code “0” always produces a “0”. Using endpoints in a TDL with N taps, the gain error, G_{error} is obtained as, [43], [44]:

$$G_{error} = \frac{t_N - t_0}{\Delta_t} - (N - 1) \quad (6.33)$$

where,

$$t_N = t_0 + (N - 1)\Delta_t + n_N \quad (6.34)$$

and n_N is the error due to noise due to mismatch at tap N . Placing t_N in (6.33) gives:

$$G_{error} = \frac{(N - 1)\Delta_t + n_0 + n_N}{\Delta_t} - (N - 1) = \frac{n_0 + n_N}{\Delta_t} \quad (6.35)$$

Each tap then is compensated for the gain error and scaled by the LSB as:

$$c'_n = \frac{t_n}{\Delta_t} + \left(\frac{n - 1}{N - 1}\right)G_{error} \quad (6.36)$$

where c'_n denotes the $n - th$ element of the code. It should be noted that unlike TDC, where the arrival time of the signal to each tap depends on the delay variation of the previous delay elements, here the arrival time is constant and only depends on the characteristics of the transmission line, given that the line is terminated to avoid reflections it can be assumed that the arrival time is independent from PVT and is constant. Hence, the INL

Figure 6.13: Simulated INL of the TDL for $\sigma_n = 0.15\Delta_t$ (top) and $\sigma_n = 0.25\Delta_t$.

analysis here only takes into account the error due to the timing mismatch of the arbiters. The final (compensated) $INL(c_n)$ is then defined as:

$$INL(c_n) = \acute{c}_n - c_n \quad (6.37)$$

Using (6.32), the INL of TDL for $\sigma_n = 0.15\Delta_t$ and $\sigma_n = 0.25\Delta_t$ is simulated and the results are shown in Figure 6.13. As can be seen, similar to DNL, small σ_n results in high probability of INL close to $\pm 0.5LSB$. From the same analysis as DNL, for $P(INL) < 0.5LSB$ is obtained as:

$$P(INL) = \int_{-\frac{\Delta_t}{2\sqrt{2}\sigma_n}}^{\frac{\Delta_t}{2\sqrt{2}\sigma_n}} \frac{1}{\sqrt{\pi}} e^{-x^2} dx = erf\left(\frac{\Delta_t}{2\sqrt{2}\sigma_n}\right) \quad (6.38)$$

Figure 6.14: Simulated probability of INL compared with theoretical probability, over σ_n/Δ_t for $N = 16$, $N = 32$, $N = 64$.

and the probability of INL for the codeword is:

$$P(INL_{codeword}) = P^N(INL) = \text{erf}^N\left(\frac{\Delta_t}{2\sqrt{2}\sigma_n}\right) \quad (6.39)$$

where, N is the number of taps.

Comparing (6.39) and (6.31) indicates that the acceptable range of σ_n is determined by the DNL probability, at which INL is guaranteed to be bounded by $0.5LSB$ as it has a higher probability compared to DNL. The simulated probabilities of the INL over σ_n/Δ_t for $N = 16$, $N = 32$ and $N = 64$ are shown in Figure 6.14 where they are also compared with calculated probability using (6.39).

6.4 Design Challenges and Considerations

In previous sections it was shown that the performance of the TDL phase detector is highly dependent on the timing mismatch offset of the arbiters and the main design challenge is to reduce the mismatch. On the other hand, since the TDL resolution is very high, it is equally important that the arbiter is able to make a decision within the target resolution, Δ_t . This means it has to be designed for high-speed operation. The above requirements can pose a trade-off as one requires large transistors to reduce the mismatch and the other requires small transistors for fast operation.

As it is accepted in the industry, the standard deviation of the threshold voltage offset, σ_v , is defined as, [45]:

$$\sigma_v = \frac{A_v}{\sqrt{WL}} \quad (6.40)$$

where A_v is a technology dependent constant and is provided by the process technology foundry. In this application however, the timing mismatch is what determines the performance of the arbiter. The timing offset can be viewed as the time that the input signal edge is high (low) enough to pass the threshold voltage. The timing mismatch also depends on the slope of the input signal and it is defined as[42]:

$$\sigma_t = \frac{\sigma_v}{S_v} = \frac{A_v}{S_v \sqrt{WL}} = \frac{A_t}{\sqrt{WL}} \quad (6.41)$$

where σ_t is the standard deviation of the timing mismatch and S_v is the slope of the signal. This dependency of the timing mismatch offset on the voltage mismatch offset and the slope of the input is shown in Figure 6.15.

Figure 6.15: Dependency of the timing mismatch offset on the voltage mismatch offset and slope of the signal.

From above, it is seen that to reduce the timing offset, the input signals should have a sharp rising and falling edges and large buffers are needed to avoid slow rate reduction.

In the 28nm CMOS technology that was used, the mismatch offset factor is:

$$A_v \approx 3.6mV \cdot \mu m \quad (6.42)$$

and as an example, assuming $S_v = 450mV/ps$, then,

$$A_t = \frac{A_v}{S_v} = 8fs \cdot \mu m \quad (6.43)$$

In the arbiter shown in Figure 5.8, the input referred offset is dominated by the input pair, N1 and N2 since in operation, the circuit is reduced to a cascode amplifier with active load, hence the effect of the offset of the

cross-coupled N3 and N4 is insignificant and the offset of the cross coupled P1 and P2 is divided by the gain of the amplifier when referred back to the input. The contribution from switching transistors, P3 and P4 is also insignificant because they are on only at the precharge phase [46]. Hence the input referred offset of the arbiter is:

$$\sigma_{t-arb}^2 \approx \sigma_{N1}^2 + \left(\frac{gm_{P2}}{gm_{N1}}\right)^2 \sigma_{P2}^2 \quad (6.44)$$

Assuming, $\mu_N = 2.5\mu_P$,

$$\sigma_{t-arbiter}^2 = \frac{A_{vN}^2}{S_v^2 W_{N1} L} + 2.5 \left(\frac{W_{P2}}{W_{N1}}\right) \frac{A_{vP}^2}{S_v^2 W_{P2} L} \quad (6.45)$$

The above equation shows that the sizing of the PMOS does not affect the offset due to the circuit topology.

In the previous sections, it was shown that the best performance of the TDL is achieved when the timing mismatch is about 10% of the resolution of the TDL. Assuming the resolution is $\Delta_t = 150fs$, for 15fs of mismatch the sizing of the transistors is as below for $A_{vP} = 1.1A_{vN}$ and $S_v = 450mV/ps$:

$$\frac{2A_{vN}}{S_v \sqrt{WL}} = \frac{16fs \cdot \mu m}{\sqrt{WL}} \leq 15fs \rightarrow WL \geq 1.13(\mu m)^2 \quad (6.46)$$

If $L = 30nm$,

$$W \geq 38\mu m \quad (6.47)$$

The size of the transistor shows that the above assumptions do not result in a practical circuit design. Besides the excessive die area needed for the arbiters, the large devices prevent the arbiter from detecting a transition

within the resolution of the TDL which is around $100fs$ to $150fs$ depending on the loading of the line. Another problem with large devices is the loading of the transmission line which can create large delays and reduction of the resolution of the TDL. One way of improving the timing offset is to increase the channel length, L . However this is not preferred in high speed applications.

In the previous sections, it was shown that for a high yield the mismatch of the arbiters, denoted by σ_n should be within 10% of the TDL resolution, Δ_t . Assuming, $\Delta_t = 150fs$, to achieve $\sigma_n \approx 15fs$ and assuming $A_v = 3.6mV/\mu m$ and $S = 1.8ps/0.8V \approx 450mV/ps$, then by using equation (6.45), the timing offset of the arbiter based on the width of the input pair NMOS with the minimum length of $l = 30nm$ is as shown in Figure 6.16. On the same plot, the Monte Carlo simulation result of the timing offset of the two arbiters with different sizing and the same signal condition is plotted for a comparison between theory and simulation.

The size of the transistor shows that the above assumptions do not result in a practical circuit design in terms of the size and speed. As mentioned above the arbiter has to be able to make a correct decision within the resolution of the TDL. The large size obtained from above calculations prevent the arbiter from making a transition in less than $150fs$. Hence either the resolution has to be increased or the yield requirement should be relaxed for more practical design. Another way of improving the timing offset is to increase the channel length, L . However this is not preferred in high speed applications.

The TDL phase detector was simulated with two different sizing of the

Figure 6.16: Timing offset of the arbiter vs. width of N1 in 28nm CMOS technology for $S_v = 450mV/ps$ and $l = 30nm$.

Figure 6.17: Flash TDL phase detector example of code spread for Case1-small devices and Case2-large devices.

Device	Case 1	Case 2
$W_{N1,N2}$	$0.4\mu m$	$2.4\mu m$
$W_{N3,N4}$	$0.4\mu m$	$1.6\mu m$
$W_{P1,P2}$	$0.3\mu m$	$0.6\mu m$
$W_{P3,P4}$	$0.6\mu m$	$0.6\mu m$
Output code mean	16.86	17.36
Output code STD	2.39	0.637

Table 6.2: Flash TDL phase detector Monte Carlo simulation result for different sizing of the arbiter.

arbiter. The sizing for the two cases and the simulation results are summarized in Table 6.2. In these simulations 300 Monte Carlo simulations were run while the input was kept unchanged. This simulation shows the spread of the output code due to the mismatch of the arbiter. From the result it can be seen that with small arbiter the performance is significantly degraded as the output code is spread over more than two codes. In the second case the spread is improved however it is still more than the target for a high yield. The histogram of the simulation results is shown in Figure 6.17.

To show how the spread of the output affects the performance of the TDL another simulation is run in which, the delay between the two input clocks of the TDL is changed by $t_{res}/20$ manually and at each phase 100 Monte Carlo simulations are performed. Then the output-code is averaged over the 100 simulations. For an ideal phase detector, moving from one code to the next is a sharp transition, but the slope of moving from one code to the next gets slower as the mismatch increases. The simulation result of the flash TDL

Figure 6.18: Monte Carlo simulation result showing the spread of one output code in Flash TDL PD compared to ideal(typical) code.

phase detector is shown in Figure 6.18. These simulations are performed with the arbiter sizing of Case 2. In previous analysis it was shown that the transition from one code to the next follows a normal distribution and the slope of the transition is equivalent to the CDF of the distribution. To show the validity of this assumption, the CDF of a normal distribution with σ obtained from Monte Carlo simulation shown in Figure 6.17, Case 2, is plotted together with the code transition shown in Figure 6.18. As can be seen the theoretical and simulated plots follow very closely.

Also for a high yield, σ of the distribution should be within 10% of the resolution of the transmission line. The design shown above does not meet

the high yield requirements, hence better techniques are needed to improve the performance of the phase detector.

In the next chapter another approach is taken to improve the performance of the TDL by reducing the offset of the first stage of circuitry that decides the phase error.

6.5 Summary

In this chapter the performance of the flash transmission delay line phase detector was analyzed using stochastic methods, where the gain, monotonicity and linearity of the TDL PD was evaluated by the probability of the random variable defined by the timing mismatch of the arbiters. At the end of the chapter the design challenges were described and the performance of the flash TDL phase detector was shown by various simulations.

Chapter 7

Successive Approximation Search Based Transmission Delay Line Phase Detector

In the previous chapter it was shown that the performance of the TDL PD depends on the timing mismatch offset of the arbiters and for a fine resolution TDL it is critical to keep offset much lower than the ideal resolution of the TDL which is determined by the distance of the taps. Achieving a low timing offset in arbiters however, poses challenges as the trade-off between size and speed. For low offset, the size of the transistors should be large while this reduces the arbiter ability to make a decision within the target resolution.

In this chapter, a new approach is introduced to overcome this issue by isolating the arbiter from the TDL and employing a search base technique to find the right output code.

7.1 Time Domain Successive Approximation

The successive approximation technique has been used in ADCs. In this technique the reference voltage is adjusted in a binary manner based on the search result. The Time Domain Successive Approximation (TDSA) while very similar to voltage domain in algorithm, has more limitations due to inability of reverting the time back. Indeed, the only possible way to search is by means of increasing the delay in an algorithmic basis.

The TDSA is previously used in [47] and [48]. In [47], two loops with digital-to-time converters are used to adjust the delay between the two time instances until the difference is solved. In this method a triggering pulse is propagated in each loop until the phase has reached the timing resolution. In each cycle the early clock is delayed and at each search step, the delay is halved. Since there are two loops, the phase error is very sensitive to the mismatch between the two loops. Hence after each timing convergence the two channels are swapped and the Cyclic Time Domain Successive Approximation(CTDSA) based TDC is calibrated.

In order to reduce long conversion latency in CTDSA due to adjusting the delay in both signals and the need for two DTCs, [48] proposes another search based scheme in which the delay adjustment is done only on one of the inputs, depending on the lead or lag, while a fixed delay, equal to half of the delay adjustment, is added to the other input regardless of phase lead or lag. In this scheme, called Decision-Select Successive Approximation, although the long latency of decision making is improved, due to use of many delay elements in the chain, complicated calibration scheme is required for accurate decision making. In this method a chain of 1-bit TDCs are used

and each TDC consists of several block with delay and mismatch that have to be compensated.

In this research the goal is to take advantage of the TDSA to achieve high resolution TDL based phase detector while maintaining a low complexity and low power architecture design.

7.2 Architecture of the Proposed Search Based TDL PD

The main motivation for the new architecture is to alleviate the large timing offset of the arbiter from the phase error decision making. In the new architecture, each tap of the transmission line is connected to a transmission gate (TG) switch instead of an arbiter. The transmission gate switches have much smaller timing offset compared to the arbiter and this is the main advantage of using them as the first stage of the phase detector. A search and select algorithm determines which switch is on at any given time while the rest of the switches are off. The output of the switches are all connected to an arbiter which is the phase detector comparator.

In this section, first the timing offset of the transmission gate switches is analyzed and compared to that of the arbiter and then the architecture and design of the new phase detector is shown in the following sections.

7.2.1 Mismatch Offset of the Transmission Gate Switch

The advantage of using switches instead of arbiters as the first stage is that the switches have much smaller timing offset compared to the arbiters. As seen in Figure 5.8, the signal path is from the NMOS gate to drain which is directly affected by the variation of the threshold voltage and from (6.44), there are two active devices that contribute to the offset. In the switches however, the signal path is through source and drain which are less affected by the variation of the threshold voltage which is the main cause of offset in transistors.

For each transistor in the transmission gate, the on resistance, R_{ON} , is:

$$R_{ON} = \frac{1}{\mu c_{ox} \frac{W}{L} (v_{gs} - v_{th})} \quad (7.1)$$

Although c_{ox} also contributes to the offset, here, the two main parameters contributing to the offset, μ and v_{th} are considered. The variation of the resistance due to the two parameters is:

$$\Delta R_{ON} = \frac{\Delta v_{th}}{\mu c_{ox} \frac{W}{L} (v_{gs} - v_{th})^2} + \frac{\Delta \mu}{\mu^2 c_{ox} \frac{W}{L} (v_{gs} - v_{th})} \quad (7.2)$$

The above equation shows that the variation of R_{ON} is much smaller than the variation of the current due to v_{th} and μ as shown in (7.3). This is considered when the transistor is used in a non-switch mode.

$$\Delta I = \mu c_{ox} \frac{W}{L} (v_{gs} - v_{th}) \Delta v_{th} + \frac{1}{2} c_{ox} \frac{W}{L} (v_{gs} - v_{th})^2 \Delta \mu \quad (7.3)$$

Although in this scheme the requirement for the timing offset is more relaxed compared to flash TDL phase detector, it is still beneficial to keep

Figure 7.1: Schematic of the transmission gate switch.

the offset small to avoid ambiguity in the decision making. The target σ_t of the TG is below 10% of the resolution of the TDL, Δ_t , for assurance of the performance.

Figure 7.2: Timing mismatch of the transmission gate switch at 25°C and 110°C.

Figure 7.1 shows the schematic and sizing of the transmission gate. In this switch both NMOS and PMOS are sized the same for better mismatch. The timing offset of the switch is shown in Figure 7.2 at 25°C and 110°C. The results are obtained from 500 Monte Carlo simulation at the two mentioned temperatures. At room temperature the timing offset of the switch is 8fs

Figure 7.3: Simplified block diagram of the search based TDL PD.

but it degrades to $19fs$ at hot temperature. Although larger size can reduce the offset, the sizing is kept as shown in the schematic figure for reasonable propagation delay.

7.2.2 Top Level Architecture

Figure 7.3 shows the simplified block diagram of the search based TDL phase detector. In this architecture a tapped transmission line provides 32 phases of the reference clock and the closest delayed reference to the feedback clock is selected at the end of the search step. The “select” logic controls the multiplexer based on the arbiter output which makes the decision on which clock is early or late.

In this scheme, first the *select* bits of the multiplexer are set to the mid

tap of the TDL by setting the MSB of the *select* bits to ‘1’ while keeping the rest of the bits ‘0’. The first tap could be chosen at any arbitrary tap, however for a binary search the mid tap facilitates an easier search. In the next step, based on the output of the arbiter, the *select* bit is either kept as ‘1’ or is set to ‘0’. The arbiter is the comparator or the main early/late phase detector of the loop and its output sets the direction of the search.

In the next step the second MSB is set to ‘1’ and again based on the arbiter output, either the decision is kept or it is reversed. This procedure is repeated until every bit of the *MUX – select* is set. At the end of the search, the output which is the pointer to the closest tap of the TDL to the feedback clock, is re-timed by a sampling clock and the phase information is used. When used in the digital loop, the frequency of the loop oscillator is kept unchanged to avoid corruption in the phase error detection and only at the end of the search, the frequency/phase of the oscillator is updated and adjusted.

The flow chart of the time domain successive approximation algorithm is shown in Figure 7.4. As was previously mentioned, in this design the TDL provides 32 taps, hence the *MUX – select* has 5 bits. An example of the timing diagram of the phase detector is shown in Figure 7.5. As can be seen at the end of the search, the phase detector output shows which tap is the closest to the feedback clock. In the example, the closest TDL tap is the 7th tap and since the feedback clock is leading the reference clock, the phase error information indicates that the feedback clock should be delayed equal to 7 taps for the minimum phase error.

This architecture as it is presented here has the limitation of providing

Figure 7.4: The flow chart of the time domain successive approximation process.

Figure 7.5: An example of timing diagram of the search based TDL phase detector.

the phase information only in one direction since time can not be delayed or reverted back. Hence, from digital loop point of view, if the feedback clock is lagging, the output of the TDL phase detector is the same as a coarse Bang-Bang phase detector and the fine phase error detection only occurs when the feedback clock is leading the reference clock. This limitation can be improved in several ways. For example, another TDL can be used to provide delayed edges of the feedback clock. In this case, when the feedback clock is lagging the phase information can be obtained from feedback TDL and when the feedback clock is leading, the phase information can be obtained from reference TDL. This method however, increases the die area. Another way is to use the mid-tap output of the TDL as the reference clock for the rest of the digital loop. In this method a bi-directional phase information is generated at no area cost. This however, will cause a constant phase offset

Figure 7.6: The schematic of the search based TDL phase detector.

which can be calibrated later on. The second method is adopted here.

7.3 Design of the Building Blocks of the Search Based Phase Detector

The schematic of the search based TDL phase detector is shown in Figure 7.6. The main building blocks of the phase detector are the TDL, the *MUX – SELECT* block, a 32-to-1 transmission gate multiplexer (MUX) and an arbiter or comparator. During the search, *MUX – SELECT* selects one of

the taps as the input of the arbiter and the arbiter decides the direction of the search at the next step.

The design of the TDL and the arbiter is kept the same as described in Chapter 5. For fast operation the sizing of the arbiter is small. Although the small sizing leads to a large timing offset, since there is only one arbiter in the loop, it does not degrade the performance as analyzed in Chapter 6. In this case the timing offset results in a static phase error which can be calibrated.

Compared to the arbiter, the transmission gate is designed with larger transistors to achieve a low timing offset. The offset of the transmission gate switch is as shown in Figure 7.2 with the spread of $\sigma_t = 8fs$ over process corners at room temperature and $\sigma_t = 19fs$ at $110^\circ C$. If the size of the switch is doubled, the worst case offset (at hot) is reduced to $\sigma_t = 10.14fs$ which is roughly 10% of the resolution of the TDL. For the first design however, the size is kept as the original design shown in Section 7.2.1 for low propagation delay through the switch.

In the following sections the design of each block is provided in detail. These blocks are designed using the standard digital library cells provided by the technology provider.

7.3.1 MUX-SELECT Logic

The simplified block diagram of the *MUX – SELECT* logic is shown in Figure 7.7. This block consists of a 5-phase clock generator, clock re-timer and N decision select unit (search unit) for N bits of output. In this block careful design has been considered to ensure that the timing of the clocks

Figure 7.7: Block diagram of the MUX-SELECT logic block.

and the search output are valid over process corners and temperature. This is achieved by placing appropriate delay cells to make sure there is enough timing margin for sampling the output and to reset the blocks for the next search process.

Since the search algorithm takes N clock cycles to complete, for an N -bit output, N clocks with frequency of f_{REF}/N are required such that each clock is high only for half of the reference clock and is low for the rest of its period. For this design, a 3-bit counter is used to generate 5 phases of the clock with frequency of $f_{REF}/5$ as shown in Figure 7.8. The clock phases are marked by CLKOUT. Each phase starts at the rising edge of the reference clock and stays high for half of the period of the reference clock.

Figure 7.9 shows the search unit block. As mentioned above, the phase detector consists of N search units for N bits of output. These units share the PD input which is connected to the output of the arbiter and each CLKOUT clock is connected to one of the search units.

In this block at the rising edge of the clock the output is set to 1 and at the falling edge of the clock the output of the phase detector is sampled

Figure 7.8: Block diagram and timing diagram of the search 5-phase clock generation.

Figure 7.9: Block diagram of the search unit.

and selected by the MUX. When the CLKOUT is high, the initial phase of the search starts by setting the corresponding bit of the *MUX-SELECT* bit to 1. The decision takes place at the falling edge of the CLKOUT and it is kept until the search is completed. The counter of the clock generator and the search unit flip flop is reset when the search is completed and the process starts over at the next search step.

An example of the output code of the search based phase detector is shown in Figure 7.10. As can be seen the new search starts at the middle code, 16

Figure 7.10: Simulated example of the output code of the search based TDL phase detector.

(decimal), and stops at an appropriate value. The reference frequency in this simulation is $300MHz$, hence each search step takes $16.67ns$ to finish, meaning the phase detector data is ready at $60MHz$.

Timing Design and Adjustments

The search based phase detector is designed with two clock generation blocks. In the first design as was shown in the previous section, the search clock is on for half cycle of the input clock and the search result is ready after 5 clock cycles. In this design at the beginning of the search the MSB search unit is set to '1' while all other search units are set to '0'. This guarantees

Figure 7.11: The timing diagram of two design of the search based phase detector.

that the search result is ready after 5 clock cycles. In the second design, the 5 search clock phases are high for one cycle of the input clock, then all the search units are reset and in the next cycle the search starts by setting the MSB search unit to ‘1’. In this scheme the search result is ready after 6 clock cycles. The advantage of the first design is that it results in smaller delay in the loop while the second design guarantees more robust timing constraints. The timing diagram of both designs are shown in Figure 7.11.

The two designs are done in two different process technology. The first design has been fabricated while the second design is used for simulation results.

7.4 Performance of the Search Based TDL Phase Detector

Figure 7.10 shows an example of the output of the search based phase detector. In this figure the search process of the phase starts at the middle code

Figure 7.12: Output of the search based phase detector from 300 Monte Carlo simulation runs, (a) the search output, (b) histogram of the output code.

and ends at the code which gives the minimum error.

As it was shown in Figure 7.2, the timing mismatch of the transmission gates is much smaller than that of the arbiter which was studied in Chapter 6. Hence it is expected that the search based phase detector performance to be less dependent on the process variations which causes mismatch. Similar to the previous chapter, statistical data is needed to determine the performance of the search based phase detector. Figure 7.12 (a) shows the output of the search based phase detector for 300 Monte Carlo simulation runs. A point to make here is that most of the discrepancy in the output happens at the end of search when the error is minimized by the search and the edges of the clocks are close. In this region mismatch affects the code more severely compared to the case that the edges are far apart and beyond the timing offset. The corresponding histogram of the output code is shown in Figure 7.12 (b) . In

this simulation the delay between the two clocks is kept unchanged and the objective of the simulation is to see what is the spread of the output code over process corners which reflects the effect of the mismatch. For the same arbiter used in both flash and search based, the spread has improved from about $0.68 \times \text{Code}$ to $0.48 \times \text{Code}$.

In the search based phase detector, the mismatch is caused mainly by the buffers after the transmission gates and the arbiter while the switches are not contributing significantly to the mismatch. Further improvement of the spread is possible by increasing the size of the buffers. However this will affect resolution of the transmission line by extra capacitive loading.

7.5 Search Based Phase Detector in the Digital Loop

The top level block diagram of the digital loop is shown in Figure 7.13. The search based TDL phase detector is used as the phase detector of a 1st order digital loop which was designed and implemented in 28nm SOI CMOS technology using Cadence. The digital loop used in this chapter is property of Ciena Inc and is used here solely to provide a platform for the phase detector and show the functionality of the phase detector. Hence the design of the loop is not discussed in detail.

The digital loop consists of the search based TDL phase detector, a digital filter which is an integrator with a gain of K_i , a phase interpolator (PI) and a frequency divider. The PI gets an external clock locked to the target frequency and since the loop is a 1st order, it can be considered as a delay-

Figure 7.13: Top level block diagram of the digital DLL with search based TDL phase detector.

locked loop (DLL) since the PI can only change the phase of the input clock to lock it to the reference clock.

For the simulations the loop was also designed in the same technology. The phase detector was designed by the author as explained previously. Also, the accumulator was also designed by the author using standard digital library cells. The phase interpolator and the frequency divider was borrowed from the existing design which was done by other team members. The fabricated chip, however, is designed by other members of the team except for the search-based phase detector which is designed by the author at schematic and layout level. The layout of the phase detector is shown in Figure 7.14.

In Figure 7.15, a transient simulation result of the loop is shown which shows the loop in lock state. The top plot shows the output of the phase detector and the bottom plot shows the output of the loop filter. It should be noted that the top plot shows only the final search result at the end of the search cycle. As the loop approaches lock, the search result stays at '0',

Figure 7.14: Layout of the search based TDL phase detector.

Figure 7.15: Simulated output of the digital loop with search based TDL phase detector, (top) output of the phase detector, (bottom) output of the accumulator.

which indicates that the clocks are coinciding to the resolution of the TDL or are at the minimum phase from each other. Similarly the bottom plot shows the incremental increase of the integrator output until the loop is locked. In this simulation the reference clock is at $300MHz$, PI external clock is at $10GHz$ and $K_i = 2^{-10}$.

7.5.1 Measurement Results

The digital loop shown above was fabricated as a part of a large system. The measurement is done by a third party and only a limited number of

Figure 7.16: Measured output of the search based phase detector.

measurements have been done at this point, including the search based phase detector output and the loop phase noise measurement.

The measured output of the phase detector is shown in Figure 7.16. In this measurement the digital loop is driven such that the reference clock and the feedback clock have a small delay. This ensures that the phase error between the two clocks is in the range of the transmission delay line of the phase detector, otherwise the output of the phase detector is saturated either to all zeros or all ones. In the figure a few examples of the search steps can be seen. In these measurements a lagging feedback clock is passing the edge of the reference clock and vice versa. When the feedback clock is lagging the

output of the phase detector is saturated to all ones, or code '31'. When the clock is passing the reference clock, depending on how fast the transition happens, the output of the phase detector has different levels until the clock is passed and the output is saturated to all zeros, or code '0'. It should be noted that the output of the phase detector is the final value at the end of the search cycle and the intermittent search steps are not shown. Static measuring of the search based phase detector is very challenging due to the dynamic nature of the search algorithm and also to the small timing window of the TDL. Hence the above measurement is a way to make sure that the phase detector is working properly and is responsive to the input phase error.

The second measurement shown in Figure 7.17 shows the phase noise of the digital loop. In this measurement the external clock of the phase interpolator is frequency locked to the reference clock while the 1st order loop is used to lock the phase. The phase noise shown in the plot is measured at the input of the phase detector. The reference frequency is 312.5MHz and the integral gain is set to 0.035.

In the plot it is seen that the carrier frequency is at twice that of the reference, this is because a divide by 2 stage is implemented inside the phase detector block which is not accessible from outside. Hence the true phase noise at the input should be considered 6dB lower than what is shown in the plot.

This measurement ensures that the digital loop with new phase detector is locked and stable. The expected phase noise of the loop is lower than what has been measured. This could be due to several factors such as reference phase noise. Another reason could be that the resolution of the TDL is lower

Figure 7.17: Measured phase noise of the digital loop with search based phase detector

than its target due to loading and uncounted parasitics. This could directly increase the phase noise.

The thorough analysis of the measured results are beyond the scope of this work since the loop is designed for a specific application and access to the system information, design environment and more measurement is not possible. The above measurements are used to validate the functionality of the search based phase detector.

7.6 Summary

In this chapter a novel multi-bit phase detector was introduced that uses time-domain successive approximation technique to minimize the phase error between the two input clocks. The design details and the performance of the search based phase detector was shown and as an example the behavior of a 1st order loop that uses the search based phase detector was shown.

Chapter 8

Conclusion

8.1 Summary

This focus of this thesis was on phase detectors, their performance and the effect of their non-idealities on the performance of digital PLLs. The thesis covered two main categories of the phase detectors. In the first part, the performance of the Bang-Bang phase detector and its effect on the digital BBPLL was investigated and in the second part two new multi-bit phase detectors were introduced that are suitable for applications that require linear phase detectors. The detail of the chapters of the thesis is as follow:

The first chapter covered the introduction of the work and the motivation behind the research. In the second chapter the background of the DPLLs including the type of the DPLL, their architecture, the application and the limitation of each type was reviewed. In Chapter 3, a new analysis was done on the effect of the gain limitation and hysteresis of the phase detector on the performance of the Bang-Bang DPLL in extensive detail. Based on this

analysis, techniques were developed that predict the excessive deterministic jitter and the frequency of the main spurious tone at the output of the BBPLL. These techniques can be used for jitter budgeting when designing the loop.

Since the phase detector poses limitations on the performance of the BBPLL, in Chapter 4, two techniques were introduced that improve the performance of the BBPLL by modifying the loop at the system level and also at the block level. In system level improvement, a software based $\Sigma\Delta$ modulator was used to generate a random bit-stream which replaced the reference clock of the loop. This technique introduces dithering in the loop which helps to reduce the spurious tones at the output. In the block level technique, a time-amplifier was used to increase the timing margin of the conventional binary phase detector which prevented the phase detector gain from operating in the metastable region and improving the performance of the loop by pushing the spurious tones further away from the fundamental.

In Chapter 5 a new phase detector is introduced that uses a transmission line to generate the delayed version of the input clock. Unlike in TDC, in TDL phase detector the delay does not depend on the gate delay which is limited by the process technology and is robust against process and temperature variations. The TDL phase detector is used to design a flash based phase detector using arbiters as binary phase detectors.

In Chapter 6 the detailed analysis of the flash TDL based phase detector using stochastic analysis was described which covered gain, resolution and the linearity of the phase detector. Based on the analysis, conditions for designing for reliable and high yield phase detector was shown and design

challenges and trade-offs were reviewed.

Chapter 7 introduces a novel search based phase detector that uses the transmission line as delay element and employs a time-domain successive approximation technique for phase error detection. The design details and performance of the phase detector was shown. A 1st order digital loop was constructed that utilizes the search based TDL phase detector and simulation and measured results of the loop were provided.

8.2 Contributions

The detailed analysis of the effect of the hysteresis of the phase detector, explained in Chapter 3 is published in IEEE Transactions on Circuits and Systems, [1]. In this paper, the behavior of the phase detector in the digital loop and closed form equations predicting the behavior of the loop based on the characteristics of the phase detector are shown. Also a new model for BBPLL is introduced which includes the limitations of the phase detector.

The system level technique that was used to improve the performance of the BBPLL, described in Section 1 of Chapter 4, which employs a software based random bit-stream for reference to dither the input of the BBPLL is published in IEEE Electronics Letters Journal, [2].

In the second technique, a Time-Amplifier is employed to improve the performance of the phase detector by increasing the time difference between the input clocks and preventing the phase detector to enter the metastable region which results in hysteresis and degrades the performance of the PLL.

A multi-bit phase detector is proposed that employs a new technique to

improve the resolution of a “TDC-like” phase detector. In this technique a transmission line is used to provide a fine delay between adjacent taps that are used as input clock of the phase detector. An extensive performance analysis using stochastic methods is done on the performance of the flash phase detector and design challenges and trades off are shown.

In the second design, time domain search algorithm along with a transmission delay line to provide a fine-resolution phase detector that is suitable for high-speed applications that require low jitter. A first order digital loop using this phase detector is designed and fabricated in 28nm SOI CMOS technology.

8.3 Future Work

For future work, since several new techniques have been introduced in this thesis, there are many avenues for further improvements of the design and more chip implementation. In Chapter 4, the time amplifier technique was used. Although the time amplifier is implemented and measured but a complete BBPLL chip will show the improvement from a top level perspective.

Also based on the analysis done in Chapter 6, design improvements can be done on different blocks of the TDL based phase detector. The arbiters can be designed for better mismatch and also techniques for calibration can be introduced to improve the performance of the TDL based phase detector.

Based on the results obtained from the search based phase detector, introduced in Chapter 7, this technique can be used for high-resolution, fast and accurate phase detectors that can be used in high speed applications.

Calibration techniques can be employed for a robust, high-yield design. This new design, shows promising performance over conventional TDC phase detector. The design and its performance analysis has a potential for extra publications depending on availability of more measurements.

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