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CMOS High Q-enhanced Filters for Radio Receivers

by

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B.A.Sc. (Electrical Engineering)

A thesis submitted to the
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in partial fulfillment of
the requirements for the degree of

Master of Applied Science

in

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**CMOS High Q-enhanced Filters
for Radio Receivers**

submitted by

Chris DeVries, B. Eng.

in partial fulfillment of the requirements for
the degree of Master of Applied Science

Thesis Supervisor

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April, 2002

Abstract

Q-enhanced LC filters are presented as an alternative to off-chip filters in a High-IF type heterodyne receiver. The dynamic range limitations of this type of filter are analyzed and a closed form expression is given for the dynamic range given circuit parameters and operating Q. Test chips are implemented that include both on and off-chip inductors to obtain filters in the frequency range of 500 MHz and 2.4 GHz. The test chips use resistive degeneration to improve the linear range of the filter. Direct digital tuning of the filters is investigated and a test system is created to test the tuning capabilities. A dynamic range of over 40 dB is accomplished with a Q of 650, operating at 500 MHz using off-chip inductors. A dynamic range of over 30 dB is accomplished with a Q of 530, operating at 2.4 GHz using on-chip inductors.

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List of Abbreviations

ADC	Analog to Digital Converter
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital to Analog Converter
dB	decibel
dBc	decibels with respect to the carrier
dBm	milli-decibel (decibels with respect to 1 mW)
GPIO	General Purpose Interface Bus
GPS	Global Positioning System
IC	Integrated Circuit
IF	Intermediate Frequency
IP2	Second Order Inter-modulation Product
IP3	Third Order Inter-modulation Product
LAN	Local Area Network
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
mS	milli-Seimens ($1/1\text{k}\Omega$)
NF	Noise Figure
PAN	Personal Area Network
Q	Quality Factor
Q_0	Un-enhanced Quality Factor
RF	Radio Frequency
SAW	Surface Acoustic Wave
SNR	Signal to Noise Ratio
SOC	System On a Chip
VCO	Voltage Controlled Oscillator

1 Introduction

The proliferation of wireless devices in the past 10 years has pushed wireless designers to search for cheaper, lower power solutions. A large part of this push has been toward a fully integrated radio transceiver where all components of the radio after the antenna are integrated onto one Integrated Circuit (IC). The major reason for the desire for a single chip radio is to reduce the system cost by eliminating expensive off-chip components. Another reason is to reduce the overall system power by eliminating the need for driving analog signals off-chip where large parasitic elements require higher power output.

Analog filters, used to select the desired signal from a wide spectrum of radio signals are very expensive if implemented as off-chip components. For example, Analog Devices Inc. introduced a 900 MHz RF transceiver chip in 1998 called the AD6190. At the time it represented an RF transceiver with a high level of integration. Even so, the analog filtering for the receiver was implemented entirely off-chip. The application circuit, as shown in the AD6190 datasheet is illustrated below in Figure 1.1.

Figure 1.1: Block Diagram of AD6190, © Analog Devices Inc.

The AD6190 requires two ceramic filters at 10.7 MHz, as shown in the block diagram and a 900 MHz filter labeled as 'ANT FILTER'. The filters cost about 0.60 US \$ each in large quantities, whereas the device itself was priced at under 5 US \$ in large quantities. The filters add approximately 25 % to the cost of the receiver. As can be seen from this example, it is desirable to integrate the filters with the receiver into one IC. Unfortunately, the filter is a very difficult part of the receiver to implement on-chip because of the low quality and performance of active, integrated filters [1]. Current solutions for on-chip RF receivers use alternative architectures compared to the traditional super-heterodyne receiver in order to alleviate the problem of on-chip filtering. The downside of these architectures is that they cannot obtain the same selectivity of the super-heterodyne receiver, as will be described in Section 2.1.

This thesis presents high Q-enhanced filters as a filtering alternative for RF receiver applications. The Quality factor (Q) of a filter is a measure of how narrow the selection band is compared to the center frequency. Most integrated filters are limited to lower frequencies for the required selectivity and Q of RF receivers. The Q-enhanced filter allows higher frequency filtering and therefore the use of the super-heterodyne architecture. This thesis explores the capabilities and limitations of Q-enhancement. Test circuitry has been implemented to demonstrate Q-enhanced filter performance in CMOS (Complementary Metal Oxide Semiconductor) technology.

CMOS is emerging as a highly desirable technology for RF integration [2]. CMOS is used extensively for digital ICs. The bulk of ICs today are fabricated in CMOS, resulting in a relatively inexpensive, easily available technology. System on a chip (SOC) integration has enabled many more functions to be implemented onto the same IC in order to reduce cost. This often forces analog and RF circuitry to be designed in CMOS where the larger amount of digital circuitry benefits from a higher transistor density and therefore lower cost.

In digital circuitry, MOS transistors have a major advantage over bipolar transistors in that they dissipate power only when the circuit switches from one state to another. MOS transistors are traditionally slower and noisier and require more power to obtain the same signal gain. For this reason they are considered inferior compared to bipolar transistors for analog circuitry [3]. However, scaling of CMOS technology to smaller and smaller geometries has increased the speed capabilities to a point where it is possible to use CMOS at RF frequencies that have traditionally employed bipolar devices [4]. This, as

well as SOC pressures has caused CMOS to be the technology of choice for many RF circuit designers.

The Q-enhanced filter is a simple circuit implemented in CMOS technology. The circuitry scales easily with smaller geometries of CMOS and lower supply voltages. For this reason, and to allow demonstration of the ability for SOC integration, the CMOS Q-enhanced filter is presented here as a solution for on-chip filtering for RF applications.

Section 2 of this thesis provides a background for the use of filters in radio receivers. First, an overview of integrated receiver architectures is covered in Section 2.1. Second, an explanation of the derivation for filtering requirements in a receiver is explained in Section 2.2. Section 2.3 gives an overview of different filter types and finally, Section 2.4 introduces the concept of filter tuning.

The basic design of a Q-enhanced filter is covered in Section 3. Derivations relating to the evaluation of the noise and dynamic range analysis of the filter are covered in this section. The layout and circuit design parameters for test filters are described in detail.

Section 4 contains simulation and test results for the test chips. In many cases results are correlated with theory derived earlier. A detailed description of the prototype filter tuning system is described in this section.

Section 5 contains the conclusions and a summary of the contributions of this thesis, while Section 6 outlines some recommendations for further research.

2 Background

Filtering is an essential component of any radio receiver. The incoming spectrum of signals to a receiver is normally comprised of many different signal bands that could have components from various sources, sometimes very close together [4]. An incoming signal spectrum may look something like that seen in Figure 2.1.

Figure 2.1: Example of Incoming Signal Spectrum

It is important for a given receiver to have enough sensitivity to be able to receive the desired signal in the presence of noise and interference. An example of this specification is a minimum input level of -70 dBm for Bluetooth [6]. This means that the receiver must detect signals as low as -70 dBm in power. With a load impedance of 50 Ohms, this is equal to a voltage of 70.7 μ V. As well as having this sensitivity, the receiver must have a certain minimum selectivity at the same time. This means that the receiver must be able to receive a signal in the desired channel in the presents of nearby, unwanted signals or interferers. The method in which a radio receiver removes these interferers before demodulation of the desired signals is outlined below.

2.1 Radio Receiver Architectures

Receiver architectures have developed over the last century to accommodate the necessary selectivity and sensitivity of wireless communications. The Super-heterodyne

receiver was introduced in 1918 [7]. Since then modifications have been made to make it integrated and lower power. For modern receivers, the architecture has been modified to allow integration of the analog filters.

Super-heterodyne

The word 'heterodyne' itself means two signals of different frequencies combined to produce the sum and difference of the original frequencies. This is commonly referred to as 'mixing' the two signals. The filter Q required to obtain the proper selectivity is extremely high at Radio Frequencies (Q is the ratio of center frequency to bandwidth of a filter). By using the super-heterodyne architecture, the frequency is shifted down so that it can be further filtered (at a lower Q) before final demodulation. Figure 2.2 shows a typical modern super-heterodyne receiver [1].

Figure 2.2: Typical Super-heterodyne Receiver

A super-heterodyne receiver is one that uses a Local Oscillator (LO) to mix the desired signal band down to an Intermediate Frequency (IF) to facilitate amplification and rejection of the unwanted signals [4]. The first stage of the receiver is a band select or Radio Frequency (RF) Filter. It provides attenuation of large interferers from other signal bands and reduces the required dynamic range of the input stage. The Low Noise Amplifier (LNA) maintains the noise performance of the receiver by amplifying the signal before noisier stages of the receiver. A side effect of the mixing process produces the need for the image reject filter [2]. The act of mixing two sinusoidal signals together

produces a component at the difference of the two frequencies. For a given LO, there are two distinct frequencies which will generate the same lower frequency difference. In the super-heterodyne filter, this results in an image channel where interferers can potentially be mixed down on top of the desired channel. The image reject filter attenuates signals at this image frequency in order to remedy this problem. The IF Amplifier is often implemented as a variable gain amplifier so that the incoming signal level can be adjusted before being filtered by the IF filter. The IF filter provides the channel selection of the receiver and has a much narrower bandwidth than the RF filter.

There is a tradeoff between choosing a high IF versus a low IF [4]. To obtain the required selectivity, it is desirable to have the IF as low as possible. This way a filter with a realizable Q can be used to perform the channel selection. The problem with this method is that the image frequency is then very close to the desired channel and therefore the image reject filter is more difficult to implement. In traditional super-heterodyne receivers there are often two stages of down conversion or mixing to alleviate this problem. The first IF is quite high so that image rejection is not a problem. The image for the second down conversion can then be filtered in the channel select filter of the first IF. The final channel select filter is then done at the lower, second IF.

The dual IF receiver is difficult to implement in a fully integrated chip because of the large number of filters required and the requirement of two LO signals. Modifications to this architecture have been developed that solve this problem while obtaining the necessary performance. They each have different benefits and requirements for filtering.

Low IF

The low IF receiver is a modification of the traditional super-heterodyne receiver. The IF is set to such a low frequency that the signal can be directly sampled or demodulated with

relatively inexpensive baseband (low frequency) processing. The benefit of this is that a high order filter can be implemented using low frequency IC filtering techniques such as G_m -C or switched capacitor filters. It also limits the receiver to only one IF stage so that only one mixing stage, Voltage Controlled Oscillator (VCO) and Phase Locked Loop (PLL) is necessary. The downside is that the image frequency of the low IF receiver is very close (typically less than 5 MHz) to the desired signal. The result is that it is insufficient to simply implement an image reject filter before the mixer. Instead, an image reject mixer and notch filter is commonly used. This type of mixer is also sometimes called a quadrature mixer because the signal is mixed using two different LO signals which are offset by 90° , as shown in Figure 2.3.

Figure 2.3: Image Reject Mixer and IF Stage

The entire IF stage is duplicated in what is called the I and Q paths. In this example, the signal is then sampled using an Analog to Digital Converter (ADC). The two different paths in the IF stage are out of phase by 90° and it can be shown that when these two signals are added together in the digital domain, the signals at the image frequency will be cancelled out [8].

The downside to the image reject filter is that in order to work properly, the I and Q signal paths must be matched very closely. This requires sophisticated tuning mechanisms on the LO generation circuitry and the notch and IF filters. In addition, the duplication of the entire IF stage, including the ADC causes a large increase in power consumption in the receiver.

Direct Conversion

The direct conversion or homodyne receiver results when the low IF idea is extended further. The direct conversion receiver, sometimes called the Zero-IF receiver, converts the modulated signal directly to DC. The benefit of this architecture is that there is again only one conversion stage and no image frequency to deal with. The disadvantage of this technique is $1/f$ noise in the low frequency signal processing, DC offsets, LO isolation and low second order inter-modulation product (IP2) [3]. The direct conversion receiver also needs a quadrature mixer to differentiate between the negative and positive frequency components of the signal. This type of receiver has been limited in the past to applications where there is no signal component at DC such as Frequency Shift Keying (FSK) [9].

High IF

The traditional super-heterodyne structure is still very appealing if the necessary filtering can be done on-chip. Q-enhanced filtering techniques can provide mid to high frequency filtering on-chip, allowing the integration of this type of architecture. As described above, using a high IF alleviates the problem of the image frequency. Although this has proven difficult to implement in the past, with improved ADC performance it is conceivable to implement the IF at a higher frequency and then sub-sample directly to a second IF. This type of receiver would look like Figure 2.2 with a sub-sampling ADC

replacing the further mixing stages. The final demodulation and any further filtering would be carried out in the digital base-band processor.

The key to a fully integrated, high IF receiver is the implementation of high Q filters on chip. The IF filter must provide the necessary selectivity before the signal is sampled by the ADC. This criterion will be set by the interference specifications of the band of interest, as outlined in the next section.

2.2 General Filter Requirements

The requirements for filtering of the incoming RF signal depend primarily on the specifications of the particular band of interest. A typical band requirement such as Bluetooth or GSM [6],[10], will require that the desired signal is received in the presence of strong, nearby interfering signals. A typical spectrum is shown in Figure 2.4:

Figure 2.4: Worst Case RF Input Spectrum (Bathtub curve)

This bathtub curve is a representation of the interference specifications for Bluetooth [6]. At the center of the graph is the desired signal at the minimum level required to be resolved by the receiver. The correct demodulation of the desired signal will require a certain amount of Signal to Noise Ratio (SNR) that depends on the type of modulation scheme. In the case of Bluetooth, a desired SNR of 10 dB implies that the minimum signal detected must be -80 dBm. The bar at the center of the plot shows the desired SNR for the received signal. The remainder of the plot shows the maximum possible interfering signal at a given offset. At an offset of 2 MHz it is possible to have an interferer that is 30 dB higher than the desired signal and at 3 MHz offset, the interferer can be 40 dB higher. For the entire Bluetooth band, it is possible to have interferers 40 dB higher than the desired signal. The out of band interferers that are 100 MHz away can be 60 dB greater than the desired signal.

In order for the base-band demodulation to operate correctly, the desired channel must be amplified to a level that can be detected by the base-band conversion circuitry and the interfering signals must be attenuated to a level that will not interfere with the final data conversion. The necessary dynamic range of a given stage in the receiver will depend on the amount of filtering and gain in the previous stages. The following discussion will look at the effects of filtering at different stages in the receiver.

The first stage of the receiver will have to receive the minimum signal without inducing non-linearities. From Figure 2.4 the dynamic range requirement will be greater than 70 dB. This is exceedingly difficult to achieve for an active integrated filter with high Q. In reality, there is some filtering off-chip in every receiver implementation. This can take the form of the response of the input antenna and matching circuit and in many cases

includes a passive, wide-band pre-select filter (e.g. ceramic or Surface Acoustic Wave - SAW). This serves the function of filtering out very large interferers that have a large frequency offset from the desired frequency. Assuming these out of band interferers are sufficiently attenuated, the in-band section of Figure 2.4 remains.

If the final demodulation is done after an Analog to Digital Converter, the ADC will be the final analog stage of concern for dynamic range, provided that previous stages have the same dynamic range capability or better. This is normally the case since the ADC will be designed for the minimum requirements to save on power and chip area. Further filtering can be done in the digital domain, however the ADC must meet the post-filtering dynamic range requirements of the specifications. An ADC has a dynamic range of approximately $6 \times n$ dB, where n is the effective number of bits in the ADC [11]. Since the signal itself has a required SNR in order to be demodulated correctly the dynamic range must be even higher. The required number of bits, n of the ADC will be:

$$n = \frac{(P_{\text{int}} + SNR_{\text{out-min}})}{6} \quad (2.1)$$

where P_{int} is the maximum power of the interferers and SNR_{out} is the signal to noise after the ADC, both in dB. Ideally, n is minimized thereby reducing the complexity and power requirements of the ADC. From the example of Figure 2.4 one can see that if there were no further filtering of the input spectrum, the total interference power would be:

$$P_{\text{int}} = 40\text{dBc} + 10\log(m) \quad (2.2)$$

where m is the number of channels within the incoming signal band that have not been attenuated by the pre-filtering and dBc is a measure of dB with respect to the carrier. Note that the power of the closest interference has been neglected as it consists of only two channels 10 dB lower than the rest. The entire band for Bluetooth is composed of 80

channels with 1 MHz spacing. It is unreasonable to assume that all 80 channels will have interfering signals at the same time, so a reasonable number of interfering channels of 5 is assumed. This means that the interfering power is approximately 47 dBc and a minimum of 10 effective bits is required in the ADC (for a SNR_{out} of 11 dB). Due to other sources of noise and to account for other design variations, an ADC of at least 12 bits would likely be required. An ADC of this size with an input bandwidth of 2.4 GHz is exceedingly difficult to build and has large silicon area and power consumption.

To reduce the ADC requirements, the signal is filtered before it is presented to the ADC. By overlaying the filter function on the bathtub curve the effect of RF filtering on the dynamic range requirements of the subsequent stages can be seen. Figure 2.5 shows the effects of a second order RF filter centered at 2.4 GHz with a Q of 500.

Figure 2.5: Bathtub Curve Modified by Second Order RF Filter

The worst case (inside edge of the 40 dB specification) of the bathtub curve is reduced by approximately 5 dB and interferers falling further out are attenuated even further. The P_{int} is now reduced significantly to approximately 38 dBc. This would require an ADC with a dynamic range of 49 dB or at least 9 bits. The ADC would still be difficult to design because of the large input bandwidth required. In addition, the dynamic range requirements of the filter itself are difficult to achieve. Implementing an on-chip filter with a Q of 500 and dynamic range of 49 dB at RF frequencies is difficult.

Down converting or mixing of the desired signal channel allows the filter to be implemented at a lower frequency. This has the effect of increasing the rejection seen by the interferers with a similar filter Q as the RF filter case. Figure 2.6 shows an example of a filter implemented at an IF of 500 MHz with a Q of 500. The resulting specification on the filter's dynamic range is drastically reduced as well as the requirements for the ADC.

Figure 2.6: Bathtub Curve after IF Filtering

The IF filter reduces the worst-case interferer by 17 dB and after the filter, the level of P_{int} is 26 dBc. Theoretically, this would only require an ADC with 5 effective bits and the input bandwidth required is 500 MHz. This type of ADC is more reasonable for a low power receiver application.

2.3 Filter Types

Filtering can take many different forms. Depending on the frequency and shaping requirements, filters can be implemented in off-chip in the form of discrete LC (Inductor-Capacitor), ceramic or SAW (Surface Acoustic Wave) filters or on-chip in the form of active filtering. In general, off-chip filtering is superior in terms of dynamic range but is more costly than on-chip filtering. Figure 2.7 shows various types of filter architectures that will be discussed below.

Figure 2.7: Summary of Filter Types

Passive Filters

Passive filters are used extensively in radio design [1]. Their dynamic range is very high (> 100 dB) and it is possible to implement high order filtering functions. Discrete inductors and capacitors are often used to match the impedance of the RF input to that of the antenna to maximize the input power. Passive LC matching can serve as an off-chip filter. The Q of off-chip inductors is in the range of 20 to 50, which is not high enough to get a narrow band selection using only the matching network. In general, a SAW or ceramic filter is needed to provide the necessary out of band rejection of interfering signals. The drawback of such filters is that they are fixed at one frequency and are expensive. To provide the necessary filtering of interferers it is more desirable to have a cheaper, tunable filter. It is especially attractive if this filter can be integrated on-chip with the rest of the receiver.

Active RC Filters

An active filter can be implemented by replacing the inductors used in the passive LC prototype with an active circuit [12]. There is also potential for the signal to be amplified

in the filter with the use of the active circuit. Active RC filters make use of the op-amp (operational amplifier) as a building block. Standard integrators and feedback amplifiers can be combined to create complex filter functions. The advantage of this type of filter is that it uses only resistors, capacitors and op-amps. A drawback is that resistors take up a large amount of silicon. In addition, it is difficult to make resistors and capacitors match without trimming, although a scheme has been suggested that allow for tuning using a binary-switched array of capacitors and digital control [13]. As well, the use of op-amps limits the frequency range and linearity of the filters.

MOSFET-C Filters

To alleviate the problem of fabricating integrated resistors, MOSFET-C filters replace them with a FET transistor operating in the triode region [14]. The transistor is much smaller and can be used for higher resistance values. One of the main problems with this solution is that the triode transistor is non-linear. To reduce this problem a fully differential circuit topology can be used. There is still a problem with resistor (transistors in the triode region) and capacitor matching which often requires complicated tuning or trimming of components.

Switched Capacitor Filters (Switch-Cap Filters)

Switch-Cap Filters are discrete time filters that make use of switches and capacitors to replace the resistors needed in the active RC network. The signal is sampled and stored on capacitors using two or more clock phases. The benefit of this type of filter is that only capacitors, switches and op-amps are required and the transfer function parameters are only dependent upon capacitor ratios. These ratios tend to be much more accurate than resistor or capacitor absolute values. Aliasing occurs at multiples of the clock frequency, limiting the operating frequency as described by the Nyquist criteria [11].

Issues associated with sampling circuits such as charge injection and kT/C noise (noise due to switch resistance) and sampling jitter are all present in switch-cap filters.

G_m -C Filters

Transconductance-C or G_m -C filters, like the switch-cap filters, use only capacitors and active components. G_m -C filters are continuous time and are only limited in frequency by the response of the transconductor and feedback networks. They can reach frequency ranges into the hundreds of megahertz. This type of filters can be used to create high order structures within a widely tunable frequency range.

The two pole bi-quadratic filter, which is the building block for the G_m -C filter, is made up of four transconductors. Higher order filters generally employ several of these 'bi-quads'. The absolute tolerance of on-chip capacitors and device transconductances are very high so the G_m -C filter normally requires sophisticated tuning techniques. This can take the form of a second, identical "master" filter or VCO [14].

It is difficult to achieve a dynamic range of greater than 50 dB for the G_m -C filter because of the open loop operation of the basic G_m -C integrator [15].

Q-enhanced LC Filters

Passive LC filters can be implemented in an IC using spiral, planar inductors and parallel plate capacitors [16]. A major limitation of this approach is that the integrated inductors suffer from very low Q values (~ 5), which means that a band-pass filter would have a bandwidth of only 20% of the center frequency. Active components can be used to compensate for the losses in the inductor. These filters are commonly referred to as Q-enhanced LC filter. The bi-quad for the Q-enhanced filter is relatively simple, employing only two transconductors. One transconductor is used for the input and the other to make up the inductor compensation or negative resistance. A major advantage of Q-enhanced

filters is that it is possible to design a Q-enhanced filter for higher frequency operation and lower power than the equivalent G_m -C filter [17].

The Q-enhanced filter is limited primarily to low order, all-pole filters. Although 4-pole filters have been reported [18], most implementations have dealt only with the simple 2-pole version. It is possible to cascade multiple two-pole sections [1] but this is generally limited to only a few stages.

Another major benefit of the two pole Q-enhanced filter is its ability to be tuned to very high operating Q's. This can be seen by a comparison with an equivalent G_m -C bi-quad filter section.

Figure 2.8: G_m -C Bi-quad

The G_m -C implementation is shown in Figure 2.8. The input transconductance, g_{mi} converts the input voltage to a current (Note: this same transconductor is used in the Q-enhanced filter with the same performance criteria, as will be shown later.) The two identical transconductors, labeled g_m form a gyrator that replaces the inductor of the passive LC implementation. By itself, the gyrator would oscillate so the lossy transconductance g_{mQ} is added to set a finite Q for the bi-quad. The center frequency and Q for this two-pole filter are given by [19]:

$$\omega_0 = \frac{g_m}{C} \text{ and } Q = \frac{\omega_0 C}{g_{mQ}} = \frac{g_m}{g_{mQ}} \quad (2.3)$$

To minimize power consumption the transconductances are set as low as possible. This also means choosing C to be as small as possible, but C must be larger than the parasitic capacitances in the filter so that non-linear device capacitance does not dominate. For example, with an operating frequency of 1.5 GHz, if a capacitance of 1pF is chosen, a g_m of 9 mS is required. This is reasonable, but tuning will be required to maintain this frequency over process variations. In addition, to obtain a very high operating Q (e.g. 500 - 1000), it is necessary to tune the transconductance g_{mQ} to a level that is Q times lower than g_m .

In comparison, the Q -enhanced filter replaces the gyrator and lossy transconductor with a real inductor and enhancement transconductor. One transconductor is tuned to cancel out the losses in the inductor. Using the example above and assuming an on-chip inductor of 5 nH has a Q of 5, the enhancement transconductor required is only 4 mS. Note that this replaces the two transconductors of 9 mS of the G_m - C filter. Kuhn [1] performed a more thorough power versus dynamic range analysis showing the potential power savings of a Q -enhanced filter.

The Q -enhanced filter poses a very feasible solution for on-chip, low power filtering. The possibility of implementing a band-pass filter at RF frequencies is limited only by the attainable dynamic range of the filter and the f_T of the devices used.

2.4 Filter Tuning

Any filter implementation will have a transfer function that varies with tolerances on the components that make up the filter. In some cases, it is possible to obtain the required accuracy for a given application by choosing filter components with the correct values

and tolerances. For example, if a switched-capacitor filter is used, the transfer function depends primarily on the ratio of capacitances in the circuit and these can have tolerances of less than 0.2 % [19], which could be sufficient for some applications. For many integrated filters, the components of the filter have tolerances that give unacceptable variance in the filter performance. In this case, tuning of some type is required to ensure the filter will operate as designed.

Tuning can be done manually or automatically. A manual tuning scheme involves measurement of the filter performance and adjusting the filter components until the desired specifications are met [19]. This can take the form of a digital calibration or a physical change of the circuit, such as laser-trimmed resistors. The downside of manual tuning is that it adds an expensive step to the manufacturing process and makes the filter less flexible. Manual tuning also does not allow the filter to accommodate circuit changes that may occur during operation, such as temperature changes.

To accomplish automatic tuning, circuitry is designed that is able to measure the filter performance and adjust it to specifications when the chip is operating. This is traditionally accomplished using analog circuitry that “locks” the filter into place [15],[18],[19]. This type of loop locking is very similar to that of a Phase Locked Loop (PLL). Figure 2.9 shows typical block diagrams of automatic Q and frequency tuning. In both cases a master filter or VCO is used to perform the tuning measurement and the resulting control signal is used to tune the slave filter. The slave filter is the main filter that operates on the input signal.

Figure 2.9: Typical Implementation of Automatic Tuning

The example above shows a master-slave tuning scheme. The drawback of the master-slave architecture is that extra circuitry is needed to implement a filter and during operation of the tuning circuitry, the power consumption is increased. As well, the accuracy of the tuning depends on the matching between the master and slave filters. For a high Q LC filter, matching tolerances make it difficult to implement the master-slave architecture. For example, at a Q of 500 and a center frequency of 500 MHz, the maximum frequency deviation between master and slave has to be on the order of 0.1 % (less than half the filter bandwidth). This would require the inductor and capacitor matching to vary by no more than 0.2 %, which is difficult to achieve.

Another option for tuning of a filter is to use direct tuning. This involves measuring the filter parameters directly from the slave filter without the use of an extra master filter.

Figure 2.10 shows an example of a direct tuning scheme. Direct tuning requires a switch at the input of the filter to switch the input signal off during tuning. Registers or lock-in amplifiers hold the tuned control voltages during the operation of the filter.

Figure 2.10: Example of Direct Tuning

The drawback of this type of implementation is that a tuning cycle is required, in which the filter cannot be used. For many applications, this is a feasible solution [20].

3 Q-enhanced LC Filter Design

3.1 Basic Circuit Description

The second order Q-enhanced filter consists of a gain stage, a real LC tank circuit and negative resistance (or Q-enhancement) circuit. The simplified circuit diagram, representing a single ended circuit, is shown in Figure 3.1 where g_0 is the equivalent parallel conductance due to losses in the circuit. These losses are dominated by the losses in the inductor for most practical cases. Note that this is an approximation because the inductor losses are actually in series with the inductor. This approximation is quite good for a narrow band Q-enhanced filter. For a wideband filter, the equivalent g_0 would change slightly with frequency. In Q-enhanced filters, a narrow band of signals is being filtered so the approximation is valid.

Figure 3.1: AC equivalent of Q-enhanced Filter

The input transconductance is denoted by g_{m1} and the Q-enhancement is g_m . The transfer function for such a circuit can be shown to be [16]:

$$H(s) = \frac{\frac{g_{m1}}{C} s}{s^2 + \frac{g_0 - g_m}{C} s + \frac{1}{CL}} \quad (3.1)$$

This can also be expressed as:

that obtains the maximum possible dynamic range, the input transconductance is designed for low noise. A lower power solution can be considered for a filter that is not used in the first stage.

Enhancement Transconductor

The enhancement transconductor is composed of transistors $M_{3a,b}$ and M_4 and resistor R_1 . The transconductor is a basic differential pair with resistive degeneration. By connecting the transconductor in a positive feedback mode, it becomes a negative conductance. The voltage at the current source to the enhancement transconductor, V_Q , controls the Q of the filter. Degeneration resistor R_1 and transistor M_4 are included in the transconductor to improve the linear range of the filter. M_4 operates in the triode region as a resistor and is included to allow the amount of degeneration to be varied to find an optimum balance between dynamic range and power consumption. The high Q operation depends on a difference of $g_0 - g_m$, the gain is very sensitive to changes in the g_m of this transconductor. This will be analyzed in detail below. The resistor R_1 as well as the transistor M_4 forms the degeneration. It can be shown that the overall transconductance, G_m with degeneration is [3]:

$$G_m = \frac{g_m}{1 + g_m R} \quad (3.4)$$

Where g_m is the overall transconductance of the transistors M_{3a} and M_{3b} , and R is the total degeneration resistance. Here it can be seen that the transconductance has been reduced by the feedback term $(1 + g_m R)$. Also, the maximum G_m is limited to $1/R$. This means that the degeneration resistance cannot be set higher than the equivalent losses in the tank circuit ($1/g_0$) or high Q operation will not be possible. For some applications, it may be desirable to change the linearity of the transconductor for different operating conditions.

A lower resistance would mean less power required to reach a given Q . Having M_4 as a variable resistor allows this flexibility. The Q of the filter is controlled by the voltage at the current source to the enhancement transconductor, V_Q . This current source is split into two parts, with the degeneration between the two sections so that a DC voltage drop is not seen across R_1 .

Tank Circuit

The tank circuit of the filter is comprised of a real inductor and a varactor. To accommodate lower frequency operation (100 - 900 MHz), the inductors and varactors are placed off-chip. For higher frequency operation (1 - 2.5 GHz) the tank circuit is fully integrated using on-chip, spiral inductors.

Output Driver / Bias Circuitry

The remaining on-chip components are bias circuitry (not shown in Figure 3.2) and output drivers. The entire filter schematic along with relevant off-chip biasing is shown in Figure 3.3. The output drivers are implemented as single-ended, resistively biased source followers. The second stage is biased off-chip to allow flexibility in the resistive biasing. This helps to perform impedance matching and gives the possibility of using the second stage as a common source if necessary. The input transconductor (LNA) is biased using two matched current sources that are set off-chip using a potentiometer. Inductor degeneration is implemented on-chip in the LNA to improve input matching capabilities at high frequencies. Below 1.5 GHz this 4 nH inductor has little effect.

Off-chip RF baluns are used to convert to and from differential signal at the input and output of the filter respectively. The input bias of the LNA is provided through a current mirror and off-chip current source. Matching components are used to interface the filter to a 50 Ohm test setup.

3.2 Noise

The noise floor (minimum detectable signal) of a band-pass filter used in a receiver is not as important if the filter is used after several gain stages (such as an IF filter placed after the LNA and mixer.) In the case of an RF filter, the noise figure is extremely important, especially if the filter is the first component the input signal experiences. In this case, the input transconductance can be the LNA. Detailed analysis of different LNA structures and design procedures has been covered previously [2],[4].

A simplified approach to analyzing the noise of the Q-enhanced filter can be used if the noise figure is not of primary concern and at low RF frequencies (as is the case for an IF filter). For this case, the simplified noise model of the MOS transistor in Figure 3.4 applies [11].

Figure 3.4: Simplified MOS noise model

The noise quantities in Figure 3.4 can be defined as follows:

$$\begin{aligned} v_n^2 &= \frac{K}{WLC_{ox}f} \\ i_n^2 &= 4kT\left(\frac{2}{3}\right)g_m \end{aligned} \quad (3.5)$$

Where v_n represents $1/f$ noise in the transistor and i_n results from the thermal noise in the channel of the transistor. The $1/f$ noise can be ignored for the linear noise analysis because the filter frequency of operation is quite high. Note that the $1/f$ noise in the current source of the filter causes a non-linear noise phenomena which can degrade the filter performance.

For a differential transconductor, the noise of the two transistors will add because they are uncorrelated. The noise in a general transconductor can be approximated with [21]:

$$i_n^2 = 4kTFg_m \quad (3.6)$$

Where F is a factor accounting for the specific implementation of the transconductor and is usually between 1 and 2.

In the Q-enhanced filter there are two transconductors that add noise to the signal: the input transconductance g_{mi} and the enhancement transconductor, g_m . As well, the inductor adds a thermal noise equivalent to its resistive losses. The total noise current entering the tank circuit is then:

$$i_{nt}^2 = 4kT(F_i g_{mi} + F g_m + R) \quad (3.7)$$

For high Q operation the value of g_m is set almost equal to the losses in the tank (g_0) and these losses are approximately $1/R$. This means equation 3.7 can be approximated with:

$$i_{nt}^2 = 4kT(F_i g_{mi} + (F + 1)g_m) \quad (3.8)$$

An example will illustrate the relative sizes of the quantities above. If an off-chip inductor of 10 nH with a Q_0 of 20 is used to filter at 500 MHz with a Q of 500, g_0 and therefore g_m is approximately $1/630$ Siemens or 1.59 mS. The mid-band gain seen by the filter is set by the equivalent tank impedance or operating Q as:

$$A(\omega_0) = g_{mi} \cdot Q\omega_0 L = g_{mi} \cdot 15.7k\Omega \quad (3.9)$$

If a mid-band gain of 40 dB is desired, a g_{mi} of 6.37 mS is required. This would mean that the input transconductance is the dominant noise source for the filter (approximately 75 %.) If the mid-band gain is set to unity, the g_{mi} is much lower than the enhancement transconductor and can be neglected for noise calculations.

3.3 *Dynamic Range*

As seen in section 2.2, the dynamic range is a critical aspect of the bandpass filter. It determines whether a filter can be used for a given interference specifications. Dynamic range can be defined as:

$$DR = \frac{P_{\max}}{P_{\min}} \quad (3.10)$$

Where $P_{\max}$ is the maximum power defined by a criterion such as 1 dB compression and $P_{\min}$ is the minimum power level detectable or the noise floor of the filter. As seen in the previous section, the contribution to noise depends on the design of the two transconductances, g_{mi} and g_m . Previously, the dynamic range for a Q-enhanced filter was shown to be [1],[26],[27],[29]:

$$DR = \frac{V_{\max}^2 C}{kT(F+1)} \cdot \frac{Q_0}{Q} \quad (3.11)$$

The assumption here has been made that the mid-band gain is set to unity so the input transconductance is ignored and the g_m is equated to Q_0 (as shown in Section 3.2). Although high mid-band gain may actually be desired, the analysis is first done using the assumptions of equation 3.11 so that a comparison with previously reported dynamic range relationships can be made.

The term $V_{\max}$ is a measure of the maximum output voltage before the circuit reaches 1 dB compression point. The assumption here is that this is some voltage level determined only by the circuit architecture chosen. A critical factor, not considered in the above expression, is that the term $V_{\max}$ is actually dependent of the enhanced Q of the filter. This will be shown in the following derivation.

The gain of the filter at the center frequency is proportional to the Q of the filter, which can be seen from equation 3.2. In the Q enhanced filter, the dynamic range of the circuit

is limited by the Q enhancement for practical implementations (i.e. where $Q \gg Q_0$). A small amount of non-linearity in this circuit will cause the Q, and thus the gain, to decrease rapidly.

As the output signal is increased, it causes a slight non-linearity and reduces the effective g_m of the circuit. We can define the change due to non-linearity as Δg_m . This change in the transconductance of the Q enhancement circuit is a reduction so Δg_m is defined to be a positive number. Normally the 1dB compression point is used to measure the linear range of a filter. This is expressed as the small signal gain divided by the gain at the 1 dB compression point. For the purpose of this derivation, this compression ratio will be defined as x . Also, the change in g_m that will give this ratio is defined here as $\Delta g_{m,max}$, as shown below:

$$\frac{Q(\Delta g_m = 0)}{Q(\Delta g_m = \Delta g_{m,max})} = x \quad (3.12)$$

Taking the expression for Q from equation 3.3, we obtain an expression for this ratio as follows:

$$\frac{(g_0 - g_m) - \Delta g_{m,max}}{g_0 - g_m} = x \quad (3.13)$$

The maximum Δg_m before reaching the gain compression ratio is given by:

$$\Delta g_{m,max} = (1 - x) \cdot (g_0 - g_m) \quad (3.14)$$

Combining equation 3.3 and equation 3.14:

$$\Delta g_{m,max} = (1 - x) \cdot \frac{\omega_0 C}{Q} \quad (3.15)$$

Note that the larger the enhanced Q, the smaller the maximum change in g_m . This equation gives insight into what happens when the Q of the filter is increased. Independent of the transconductor implementation, the allowable non-linearities seen in

g_m will vary inversely with the enhanced Q. For a given transconductor, there is a relationship between $\Delta g_{m,max}$ and the maximum output voltage, V_{max} . Obtaining this relationship in a closed form can provide a more accurate expression of dynamic range as a function of Q enhancement.

For the simple case of a differential pair, as shown in Figure 3.2, the derivation of this relationship is somewhat involved. It begins with a look at the voltage to current relationship of the differential transistors $M3_a$ and $M3_b$.

Taking the voltage loop from V_+ to V_- (assuming R_1 is 0):

$$V_+ - V_{GS1} + V_{GS2} - V_- = 0 \quad (3.16)$$

Using the following substitutions:

$$V = V_{ID} = V_+ - V_- \quad (3.17)$$

$$V_{GS} = \sqrt{\frac{I_D}{K_N}} + V_{TN} \quad (3.18)$$

Then:

$$V = \sqrt{\frac{I_{D1}}{K_N}} - \sqrt{\frac{I_{D2}}{K_N}} \quad (3.19)$$

Also, one can define the two DC currents as $(I_B + I)/2$ and $(I_B - I)/2$ where I_B is the total tail current and I is the output differential current to obtain:

$$V\sqrt{2K_N} = \sqrt{I_B + I} - \sqrt{I_B - I} \quad (3.20)$$

Recognize that:

$$g_m = 2\sqrt{I_D K_N} = \sqrt{2I_B K_N} \quad (3.21)$$

With gain compression, there is an effective reduction in the g_m . The average g_m is the ratio of the large signal output current I to the input voltage V . This large signal g_m will be defined as $g_{m,LS}$.

Dividing both sides of equation 3.20 by I gives:

$$\frac{V}{I} \sqrt{2K_N} = \frac{\sqrt{I_B + I} - \sqrt{I_B - I}}{I} \quad (3.22)$$

Now using the definition of $g_{m,LS}$ results in:

$$g_{m,LS} = \frac{I}{V} = \frac{I \sqrt{2K_N}}{\sqrt{I_B + I} - \sqrt{I_B - I}} = \sqrt{2I_B K_N} \frac{\frac{I}{I_B}}{\sqrt{1 + \frac{I}{I_B}} - \sqrt{1 - \frac{I}{I_B}}} \quad (3.23)$$

Δg_m can be expressed as follows:

$$\Delta g_m = g_m - g_{m,LS} = \sqrt{2I_B K_N} \left(1 - \frac{y}{\sqrt{1+y} - \sqrt{1-y}} \right) \quad (3.24)$$

where $y = I/I_B$. Note that as y approaches 0, this equation also approaches 0 (a limit using Hôpital's rule is necessary to show this [30]). Equation 3.24 expresses the change in g_m with respect to the amplitude of the current at the transconductor output. To obtain a relationship with respect to the voltage input, equation 3.20 can be solved as follows [22]:

$$\frac{I}{I_B} = z \sqrt{1 - \frac{z^2}{4}}, \quad -\sqrt{2} \leq z \leq \sqrt{2} \quad (3.25)$$

where

$$z = \sqrt{\frac{2K_N}{I_B}} \cdot V \quad (3.26)$$

Combining equations 3.24, 3.25 and 3.26 gives Δg_m as a function of z (and thus input voltage).

$$\Delta g_m = \sqrt{2I_B K_N} \left(1 - \frac{z \sqrt{1 - \frac{z^2}{4}}}{\sqrt{1 + z \sqrt{1 - \frac{z^2}{4}}} - \sqrt{1 - z \sqrt{1 - \frac{z^2}{4}}}} \right) \quad (3.27)$$

The function is complicated and does not provide much insight on it's own. A Taylor series expansion of the function is given by:

$$\Delta g_m = \sqrt{2I_B K_N} \left(\frac{1}{8} z^2 + \frac{1}{128} z^4 + \frac{1}{1024} z^6 \dots \right) \quad (3.28)$$

This series is almost exact for the range of validity (i.e. $y = \pm(I/I_B)$ or maximum current swing). Taking only the z^2 term gives a function that is off by approximately 10 % at the extremes and 2.5 % for practical compression ranges. Using this simplification and equation 3.21 and 3.26 gives:

$$\Delta g_m = \frac{K_N^2}{4g_m} \cdot V^2 \quad (3.29)$$

It should also be noted that when there is Q enhancement, the value of g_m is very close to the value of g_0 :

$$g_m \approx g_0 = \frac{1}{\omega_0 L \cdot Q_0} \quad (3.30)$$

Combining equations 3.29 and 3.30 gives:

$$V = \sqrt{\frac{4\Delta g_m}{K_N^2 Q_0 \omega_0 L}} \quad (3.31)$$

Now combining the maximum g_m derived in equation 3.15, results in an expression for the maximum allowable input voltage:

$$V_{\max} = \frac{2}{K_N} \sqrt{\frac{C(x-1)}{LQ_0Q}} \quad (3.32)$$

The result shows that when Q is increased, the voltage at which compression is reached decreases. This has a major impact on the performance of Q enhanced filters. Another important point here is that a larger Q_0 also decreases the maximum voltage. This has not been considered in previous derivations.

The original dynamic range equation can be modified by substituting equation 3.32 into equation 3.11 as follows:

$$DR = \frac{4C^2(x-1)}{K_N^2 LkT(F+1)Q^2} \quad (3.33)$$

Using a 1 dB compression ($x = 1.122$):

$$DR = \frac{0.488C^2}{K_n^2 LkT(F+1)Q^2} \quad (3.34)$$

Two major differences between equation 3.11 and 3.34 are of interest. First, the dynamic range now varies with the inverse of Q^2 . This shows the importance of the transconductor design in the overall dynamic range. The dependence on Q can be reduced if the dependence of g_m versus the maximum tank voltage is reduced. Second, the dependence of the dynamic range versus Q_0 has effectively disappeared. This can be explained by the fact that although a lower Q_0 leads to a larger noise current, this is cancelled by the fact that the resulting higher g_m required for enhancement increases V_{max} (equation 3.29.)

From to the original noise equation (3.8), note that the noise effects of g_{mi} were neglected because the mid-band gain was assumed to be unity. If a desired mid-band gain of 40 dB is used, it is the effect of the enhancement transconductor, g_m that can be neglected. This would cause the result from equation (3.34) to have the following form:

$$DR \propto \frac{1}{Q_0 Q^2} \quad (3.35)$$

This implies that by increasing the losses in the tank we can actually increase the dynamic range of the filter. This is only true up to the point where the noise due to g_m is significant (i.e. as large as the noise due to g_{mi}).

3.4 Layout / Circuit Design

Test chips were fabricated in a 0.18 μ m CMOS, standard digital process through CMC (Canadian Microelectronics Corporation). The circuit design and layout of the various components is described below. Table 3.1 shows the sizing of all integrated transistors in the design of Figure 3.3.

Table 3.1: Transistor Sizing

Transistor	Width (μm)	Number of Fingers	Total Width (μm)	Length (μm)
M_1	2.5	30	75	0.18
M_2	2.5	30	75	0.18
M_3	6	16	96	0.22
M_4	6	16	96	0.22
M_5	10	40	400	0.5
M_6	20	8	160	0.2
M_7	4	4	16	0.25
M_8	10	7	70	0.25
M_c	5	16	80	1

Tank Circuit

The testchip includes filters with both on-chip and off-chip tank circuits to be tested, allowing for various different frequency bands. The fully integrated version includes on-chip spiral inductors and MOS varactors. It is intended for operation at frequencies from 1.5 – 2.4 GHz. The layout for the on-chip tank circuit is shown in Figure 3.5.

Figure 3.5: Layout of On-chip Tank Circuit

The varactors are sized to allow for approximately 10 % frequency tunability. The varactors used are MOS capacitors (M_c) in inversion mode. This type of varactor provides a wide tuning range with a moderate Q and is very easily implemented in a CMOS process [23]. Through simulation, it was found that a transistor sized at a W/L ratio of 80/1 gave a capacitance that range from 0.7 pF down to 50 fF with an applied V_f of 0 to 1.8 Volts. Extra capacitors were placed in parallel with the varactors using 6 metal layers. Laser fuses used with the capacitors allow different frequency bands to be tested. The inductors were intended to be approximately 4.2 nH, but due to a layout and inductor simulation error, the realized inductance was approximately 6 nH. This resulted in a maximum frequency of 1.7 GHz. To facilitate the testing of this filter at 2.4 GHz, a FIB (Focused Ion Beam) was performed to reduce the overall inductance of the tank circuit by shorting the outermost loop. A resulting micro-photograph is shown in Figure 3.6.

Figure 3.6: Micro-photograph of FIB

The result of the FIB modification is that the inductor Q is lowered. The tungsten short, seen in Figure 3.6 is $10\text{ }\mu\text{m}$ wide and about $2\text{ }\mu\text{m}$ long between connections, which gives an added resistance of approximately 40 ohms. In addition, the unused loop of the inductor will induce losses through coupling with the inner loops. This has the effect of requiring a larger g_m to achieve high Q operation. As outline in Section 3.3, this can have a positive effect on the dynamic range if the noise from the input stage dominates.

The off-chip version has pins for the tank circuit connection. The tank circuit in this case is composed of standard surface mount inductors and hyper-abrupt varactor diodes (Philips part #BB131). The high frequency range of the off-chip version is limited only by the parasitic elements of the package. The package used for this test-chip is a 24 pin ceramic flap package (CFP) which is intended for use up to 2 GHz. However, since the bond-wire inductance is over 1 nH , the off-chip operating frequency is limited to approximately 750 MHz. This could be improved by the use of on-chip varactors instead

of off-chip varactor diodes. This would cause the bond-wire inductance to be added to the tank inductance, allowing operating frequencies over 1 GHz.

The low frequency is limited by the parasitic capacitance of a large off-chip inductor. When this capacitance is large, it causes the dominant center frequency of the filter to be determined by the bond-wire inductance. The lowest frequency possible for the off-chip filter is approximately 110 MHz.

Input Transconductor

The low noise input stage was based on a previous design [24]. The device sizing and bias levels are the same but the layout and bias circuitry was changed to allow integration in the filter test chip. Inductor degeneration is a typical design method for obtaining good matching and low noise figure in CMOS LNA design [7]. The inductor used is a 6nH, center-tapped inductor with the current supply split across the inductor to avoid DC power loss in the inductor. The inductor is effective at higher frequencies (1.5 – 2.4 GHz) but at lower frequencies is ineffective. The same inductor used for the tank circuit was used for the inductive degeneration (approximately 3nH per side). For the off-chip (low frequency) tank version, the input match was attained easily using standard surface mount components. The split current supplies (M_6) are laid out using a common centroid method to provide good matching. To allow flexible biasing possibilities, the current mirror for the current supply is supplied off-chip. The layout of the input transconductance is shown in Figure 3.7.

Figure 3.7: Layout of Input Transconductance

Enhancement Transconductance

The enhancement transconductor is shown in Figure 3.8. The bias current for this differential pair will be determined by the required g_m . As discussed in section 3.1, this will be approximately equal to the losses in the tank circuit which can range from a few hundred Ohms for on-chip inductors to 2 – 3 kOhms for off-chip inductors. A large transistor M_3 is desirable to lower the current required to obtain this g_m , but as the transistor size is increased, the dynamic range is adversely affected as shown in equation 3.34. In addition, the parasitic capacitance of the transistors should be small compared to the tank circuit varactor to ensure the designed tuning range is maintained. The transistor M_3 is sized with a total W/L ratio of 96/0.22 to allow for a reasonable amount of current to obtain the required g_m .

The first set of test chips produced had only resistive degeneration with options from 0 to 700 Ohms. Initial testing showed that for resistances less than 700 Ohms, there was a negligible effect on the linearity and therefore the required current of the transconductor. The reason for this is that a resistor of this size has a insignificant effect on the overall transconductance given by equation 3.4.

A second test chip was then fabricated with degeneration comprised of the real and active resistors. The maximum size of the transistor is determined by equation 3.4 and depends on the size of the losses in the tank circuit. To accommodate a range of values, several resistors were placed in parallel allowing resistances from 700 Ohm to 1.5 kOhm to be tested. The variable resistor needs to be sized so that the minimum 'on resistance' is less than the resistive degeneration. By designing M_4 so that the 'on resistance' is lower than 700 Ohms allows the degeneration to be switched off. If M_4 is too large, the parasitic capacitance can cause the effective impedance across the degeneration resistor to be too low, even when M_4 is off. For this reason, M_4 is sized just large enough with a W/L of 96/0.22.

The current source is split up into two sections across the degeneration to avoid having a DC voltage drop across the resistors. The current source transistors (M_6) are sized as large as possible to minimize the effect of $1/f$ noise on the transconductor [25]. M_6 must remain in the saturation region so that high output impedance is maintained for the current source. M_6 is sized at a W/L of 160/0.2 per side, giving a total of 320/0.2 for the entire current source.

The current source is laid out in a common centroid fashion to ensure both halves (M_{6a} and M_{6b}) match. The transconductor is also laid out in common centroid. Laser fuses are

used extensively to allow for modifications in the size of the transistors and especially the amount of degeneration.

Figure 3.8: Enhancement Transconductor

4 Simulation and Experimental Results

Results are presented here for the integrated Q-enhanced filter that was fabricated to demonstrate the usefulness and potential of this design. Results are shown for both a low frequency (500 MHz) filter and a high frequency (2.4 GHz.) The test setup used for measured results is shown in Figure 4.1.

Figure 4.1: Photo of Test Setup

4.1 Noise

The filter design was simulated to determine its noise performance. To perform the simulation, the input was set using a 50 Ohm source impedance with ideal matching components and a transformer. This is similar to the test setup used to test the filter (Figure 4.1) with the exception that losses in the input matching and package parasitics are not modeled here. The noise in the simulation is the noise only due to integrated devices (i.e. the transconductors and inductors.) Figure 4.2 and Figure 4.3 show the results of the noise simulation for the IF and RF filter respectively.

Figure 4.2: Simulated Noise Figure for IF Filter

Figure 4.3: Simulated Noise Figure for RF Filter

The noise figure is minimized when the current supply to the input transconductor is high. Since it is not necessary that the filter input stage be used as an LNA in the case of the IF filter, the filter was also simulated for lower bias currents in the input stage to determine the effect on the noise figure. In each case, a Q of approximately 500 was used and the input was matched as above. Table 4.1 shows the summary of these simulations.

Table 4.1: Summary of Simulated Noise Figure for IF Filter

Input I_{bias}	Q	f_c	Noise Figure (dB)
2 mA	540	556.8 MHz	1.75
600 μ A	543	561.2 MHz	2.60
200 μ A	527	562.4 MHz	4.65
100 μ A	531	562.6 MHz	6.75

Using the test setup, the noise figure was found for both filters. The noise figure is tested for various bias currents as shown below in Table 4.2.

Table 4.2: Test Results for Noise Figure

Input I_{bias}	IF filter Noise Figure (dB)	RF filter Noise Figure (dB)
2 mA	1.9	3.8
1.5 mA	1.7	3.9
1 mA	2.3	4.9
500 μ A	2.8	-
400 μ A	3.4	-
300 μ A	4.5	-
200 μ A	5.8	-
100 μ A	9.8	-

The baluns used on the test board (see Figure 3.3) for the IF filter were M/A-COM part # ETC4-1-75 which have a typical loss of approximately 0.5 dB at 500 MHz. For the 2.4 GHz RF filter, M/A-COM part # ETC1.6-4-2-3 was used and has a maximum loss of 3 dB up to 2500 MHz. For the IF filter, the results have been corrected for a 0.5 dB loss in the balun and 0.5 dB loss in the connector, matching network and package combined. The correction of the 2.4 GHz filter is 6 dB, comprised of the loss from the balun and the much higher losses of the package and matching circuitry. The package used for the test chips is rated up to 2 GHz, meaning that losses at 2.4 GHz can be appreciable.

The results from simulation for the IF filter agree with the measured results in both value and the dependence on the input supply current. The IF filter shows little degradation after reducing the input transconductor current to 500 μ A. Simulation for the RF filter noise figure is less accurate, due mainly to the fact that transistor models used do not include high frequency effects and the lack of modeling of the packaging and off-chip matching components used. A more accurate analysis of the noise figure possible with this configuration in 0.18 μ m CMOS is available in [24].

4.2 Voltage / Power Gain

The power gain of the filter is highly dependent on the impedance transformations at the input and output of the filter. In the test setup, the filter is matched at the input to 50 Ohms using a balun and off-chip, passive matching components. At the output, on-chip source followers and an off-chip balun and matching components provide a match to 50 Ohms. In a fully integrated receiver the proper power gain could be added to convert to the impedance of the next stage. For example, this could be a sampling circuit for an ADC.

The power gain for the filter was simulated using the same circuit used to find the noise figure (input and output matched with ideal elements.) The power gain includes gain due to the filter and gain from the source followers. Voltage gain was also analyzed, since it is useful to know on-chip signal voltages. The output voltage used to find this gain is the node across the tank circuit. The voltage and power gain was simulated using an operating Q of 540 for the IF filter and is shown in Figure 4.4. Figure 4.5 shows the same plot for the RF filter with a Q of 534. Biasing for the IF filter is at 600 μ A and 2 mA for the RF filter.

Figure 4.4: Voltage and Power Gain for the IF filter

Figure 4.5: Voltage and Power Gain for RF filter

Table 4.3 : Simulated Gain for IF and RF filters

Filter and Operating Q	Voltage Gain	Power Gain
IF Filter	63 dB	48 dB
RF Filter	63 dB	47 dB

The voltage and power gain differ by approximately 15 dB. This is due to the voltage loss of 6 dB in the source followers and the voltage loss by the step-down transformer and matching circuitry. The inductive degeneration has the effect of lowering the input transconductance (g_{mi}) that is higher for the RF filter than for the IF filter. This is offset by the fact that the IF filter has a lower bias current (600 μ A). The inductance has little effect on the IF filter because of its lower frequency of operation. The measured voltage and power gain for the two filter implementations are shown in Table 4.4.

Table 4.4 : Measured Gain for IF and RF filters

Filter and Operating Q	Voltage Gain	Power Gain
IF Filter, Q = 492	60.2 dB	44.8 dB
RF Filter Q = 527	-	44.5 dB

The results have been corrected for the losses in the input and output circuitry (baluns, matching and package parasitics.) For the IF filter 3 dB is added and for the RF Filter, 6 dB is added. The results match well with the circuit simulations above.

The voltage gain was measured for the IF filter using a resistive divider across the off-chip tank circuit. In the case of the RF filter, this measurement technique could not be used because of the on-chip inductors. The test circuit is shown below in Figure 4.6. The added resistance is negligible compared to the losses in the inductor and the matched impedance (with known loss) allows the output voltage at the tank to be measured directly.

Figure 4.6: Test Circuit for Voltage Gain Measurement

4.3 Dynamic Range

Q Versus 1 dB Compression Point

The dynamic range of the filter was simulated using a numerical simulation of the analysis in Section 3.3. By taking the first order model of the differential MOS transconductor with resistive degeneration, the maximum output voltage for a given

operating Q can be estimated. Figure 4.7 shows the results of this simulation using C_{ox} and K_N values from the $0.18\mu\text{m}$ CMOS process and the transistor sizes for this design.

Figure 4.7: Numerical Simulation of 1dB Compression versus Q

As expected, the 1dB compression point and therefore the dynamic range is inversely proportional to the operating Q of the filter (Note: the maximum power level is proportional to the maximum output voltage squared.) An increased resistive degeneration results in improved dynamic range with the restriction that the resistive degeneration cannot be larger than the equivalent parallel losses in the tank circuit.

Test results show a similar relationship between linearity and operating Q , which further proves the relationship developed in section 3.3. It is possible to estimate and plot the output 1dB compression voltage versus operating Q using the voltage loss calculation from the voltage and gain results in Table 4.4. This plot is found in Figure 4.8.

Figure 4.8: Measured 1 dB Compression versus Operating Q

The results above are slightly worse than the numerical simulation of Figure 4.7. This could be due to both the inaccuracies of the first order transistor model and the tank voltage measurement. The results are plotted with a $1/Q^2$ fit line. The results follow close to that line with the exception of the large jump in the center (most likely due to measurement error.)

Dynamic Range and Degeneration

The first test chip showed no improvement in linearity when resistive degeneration options were used. This is due in part to the fact that the largest resistor of 700 Ohms was not large enough to affect the overall transconductance. More seriously, it was found that the parasitic capacitance at the nodes across the resistor (the drains of the current source M_6) was too large. The parasitic capacitance caused the impedance to be less than 700 Ohms at the center frequency of the filter. The first test chip had bond pads connected to these voltage nodes in order to test the effect of external components but the bond pads created too large a capacitance. The second test chip had these bond pads

removed and included options for larger resistors as well as the variable resistor (transistor M_4). Because of space limitations, the second test chip was implemented only as an off-chip IF filter. Simulation was performed to show the potential linearity improvement using degeneration. A transient (time based) simulation was performed where the amplitude of the input signal was increased up to the point where the gain at the center frequency decreased by 1 dB. The simulation results are shown in Table 4.5. Measured results for different resistor values are shown in Table 4.6. To obtain results for the different resistive degeneration, laser fuses were blown to obtain higher overall resistance values.

Table 4.5: Simulation of Linearity for Fixed Resistive Degeneration

Resistor (Ohms)	Tank Voltage (1dB compression)
110	12 mV
1.2 k	74 mV
1.5 k	184 mV

Table 4.6: Measurement Linearity for Fixed Resistive Degeneration

Resistor (Ohms)	Output 1 dB Compression	Tank Voltage
M_4 on	-42 dBm	6.3 mV
1 k	-37.1 dBm	11 mV
1.25 k	-35 dBm	14 mV
1.5 k	-33.5 dBm	17 mV

The results show that there is an improvement in the linearity with the increase of the resistive degeneration. The improvement is much smaller than that shown from simulation. It is possible that the modeling of the integrated resistor and parasitics was

not sufficient in the simulation. The impedance of the degeneration of the test circuit may in fact be much lower than the intended resistance.

The filter was designed with a programmable linearity so that the current used in the enhancement transconductor could be minimized. To evaluate this variable linearity, the SFDR (Spurious Free Dynamic Range) was measured for different current values. This ensures that any increase in noise due to the increase in degeneration is accounted for in the overall dynamic range measurement. Table 4.7 shows results of varying the control voltage of the variable degeneration resistance with a Q of 650 for the IF filter (a bandwidth of 750 kHz is used for the dynamic range measurement.)

Table 4.7: Linearity versus Current consumption

Control Voltage (gate of M ₄)	Current in Transconductor	SFDR
2.3 V	72 μ A	30.7 dB
1.5 V	117 μ A	33.2 dB
1.4 V	181 μ A	37.2 dB

The best case 1 dB compression point measured, corresponding to a control voltage of 1.4 V as in Table 4.7 above, was -30 dBm output power, corresponding to a peak tank voltage of 25 mV. The noise level for the SFDR measurement was measured using the operating bandwidth of the filter (750 kHz in this case).

4.4 Tuning

Test Setup

Tuning for the Q-enhanced filter is performed externally to test the feasibility of automatic tuning in a fully integrated filter. The Q and frequency tune voltages are controlled using Keithly 2400 source meters. These meters provide the necessary voltage accuracy and a GPIB interface (GPIB is a standard lab bus interface) that allows

automatic control by a PC. A block diagram of the test setup is found in Figure 4.9 and a photograph of the setup is seen in Figure 4.1. The input of the filter is terminated with a 50-Ohm impedance. It was found that the input impedance was important in the filter center frequency and Q, and therefore the system design will have to take this into account when designing the attenuator or switching circuit to operate during the tuning cycle.

Figure 4.9: Block Diagram of Tuning Circuit

The output of the filter is amplified using a standard RF amplifier to provide a large enough voltage swing into a 50-Ohm load. It is then digitized by the use of an ADC. For the IF filter, a Texas Instruments TLV5580, 8-bit ADC is designed into a digital PCB (Printed Circuit Board) designed for this purpose (see Appendix A for test board schematics). The ADC has an analog input bandwidth of 750 MHz and a maximum sampling rate of 80 MSPS. This allows the filter output to be sub-sampled and processed by the PC in the test setup. For the RF filter, a Maxxim MAX108, 8-bit ADC with evaluation board was used to collect the data. The MAX108 has a 2.5 GHz input bandwidth, allowing testing of the 2.4 GHz Q-enhanced filter tuning. A GPIB interface

board was used to collect data from the ADC and transfer it over the GPIB bus to the controlling PC.

Algorithm

The tuning algorithm was written in Matlab and was run on the PC, which also operated the source meters over the GPIB bus. The algorithm for tuning the filter using this setup is outlined in Figure 4.10. Source code for this algorithm can be found in Appendix B.

Figure 4.10: Algorithm for Filter Tuning

In the test setup, 2^{10} or 1024 samples were taken for each FFT and RMS measurement. Initially the voltage V_Q is turned high so that the filter is actually in oscillation and the output of the filter is a narrow band signal. To find the center frequency of the filter, f_c ,

an FFT is performed on the sampled data. After coarse frequency tuning, the Q is reduced and the frequency is fine-tuned. To determine the Q of the filter the RMS value of the output code is calculated once the coarse frequency tuning is complete. It was found that after the voltage V_Q is reduced below the point at which the filter oscillates, it no longer has a significant effect on the frequency of the filter. This can be seen in Figure 4.11 where the spectrum analyzer output is plotted for various Q . The final output spectrum as seen by the PC is shown as an FFT in Figure 4.12. The frequency appears as the down converted frequency after sub-sampling of the filter output. In this case, the sampling frequency was 40 MHz. The filter in use was operating at 1.08 GHz plus the offset shown of 13.5 MHz to give 1.0935 GHz.

Figure 4.11: Spectrum Analyzer Plot of Q Tuning

Figure 4.12: FFT of Tuned Filter

Tuning over different bands of the filter's tuning range is accomplished by pre-calibrating the filter to a point within the tunable range of the filter. This range is one half of the sampling frequency of the ADC. Figure 4.13 shows the IF filter output spectrum seen by a spectrum analyzer. The filter input is switched off, as shown in Figure 4.9. The filter is tuned to various frequencies within the tuning range of 20 MHz. The bandwidth in each case is about 1.5 MHz or a Q of about 300. The amplitude of the noise is that seen by the ADC after the RF amplification (see Figure 4.9.) Once the filter is tuned, the RF amplification can be reduced so that the maximum dynamic range of the ADC is used for the desired signal. If the filter is pre-calibrated to different multiples of 20 MHz, the entire tuning range of the filter can be used. Figure 4.14 shows the filter tuned to different frequency bands within the overall tuning range of the filter.

Figure 4.13: IF Filter Tuned Within Sub-Sampled Spectrum

Figure 4.14: IF Filter Tuned to Different Frequency Bands

In Figure 4.14, the signal generator from the spectrum analyzer was used as an input signal for the filter to obtain the traditional, smooth filter output.

Continuous Tuning

Complete Continuous Tuning cannot be accomplished with the algorithm developed for this thesis since it relies on the fact that the noise spectrum entering the filter is flat. An incoming signal within the tuning band would result in an incorrect filter tuning. It is possible however to 'refresh' the Q and frequency tune of the filter occasionally. With the test setup described above, it was possible only to re-tune the filter at a very long interval (~ 4 seconds) because of the delays inherent in the GPIB bus and the PC processing.

4.5 *Summary of Test Chip*

The best results from above are summarized in Table 4.8 for both the RF and the IF filter test chips. In the case of the IF filter, the Q was 650 and the variable degeneration was set to 1.4 V as described in section 4.3. The RF filter had no degeneration and the Q was set to 530. Power consumed from a single 1.5 V "D cell" battery is also shown in the table. Table 4.9 compares the work in this thesis to that of recent publications involving Q-enhanced filters.

Table 4.8: Summary of RF and IF Filter Performance

Measure		IF Filter	RF Filter
Area		550 μm X 250 μm (0.138 mm ²)	1200 μm X 850 μm (1.02 mm ²)
Power Supply		1.2 – 1.8 V	
Tuning Range		> 10 %	> 10 %
Center Frequency		420 MHz – 510 MHz	2.24 GHz – 2.45 GHz
Noise Figure		2.8 dB	3.8 dB
Q Tuning		up to approximately 1500	
Operating Q		650	530
SFDR		37.2 dB ¹	33.2 dB ²
1 dB Dynamic Range		41.3 dB ¹	31.2 dB ²
Output 1 dB Compression Point		25 mV	-
Current	Input Stage	500 μA	2 mA
	Q-enhancement	181 μA	150 μA
Total Power ($V_{dd} = 1.5$ V)		1.02 mW	3.23 mW

¹A noise bandwidth of 750 kHz is used for the IF filter

²A noise bandwidth of 750 kHz is used for the RF filter, assuming it is used in conjunction with the IF filter.

Table 4.9: Comparison of This work with Recent Publications

Author, Date	Technology	Frequency	Q range	Dynamic Range
Kuhn, 1998 [17]	0.8 μm CMOS	850 MHz (2 nd order)	20 – 250	1 dB Dynamic Range of 75 dB with Q of 45
Duncan, 1997 [28]	0.8 μm BiCMOS	750 MHz (2 nd order)	10 – 490	SFDR of 25 dB with Q of 25
Pipilos, 1996 [29]	0.8 μm Bipolar	1.8 GHz (2 nd order)	3 – 350	1 dB Dynamic Range of 40 dB with Q of 35
Wu, 1997 [34]	0.8 μm CMOS	880 MHz (2 nd order)	2.2 – 44	1 dB Compression of –30 dBm with Q of 30
Li, 2001 [27]	0.25 μm BiCMOS	1.9 GHz (4 th order)	N/A	1 dB Dynamic Range of 63 dB with BW of 150 MHz
This Work [35]	0.18 μm CMOS	500 MHz	100-1000	1 dB Dynamic Range of 41 dB with Q of 650
		2.4 GHz		1 dB Dynamic Range of 31 dB with Q of 530

5 Conclusions

The Q-enhanced LC filter has been presented as a filtering alternative for modern integrated radio transceivers. It allows the implementation of on-chip, high Q filters at RF or high IF frequencies. The filters provide high selectivity and gain while operating with low power consumption.

The dynamic range restrictions of Q-enhanced filters were explored both analytically and experimentally. The linear range of the Q-enhanced filter was shown to vary inversely with the square of the operating Q. A new understanding of the dynamic range of the filter has been obtained through an analytical expression that takes into account dominant noise sources and the effect of Q-enhancement on gain compression.

Test chips were designed and implemented with both on and off-chip inductors to demonstrate the analysis of the Q-enhanced filter. The use of resistive degeneration to improve the linear range of the Q-enhanced filter was explored. The effect of degeneration showed large improvements in simulation, but only moderate improvements in the actual test chip. It was found that the effectiveness of the degeneration was very sensitive to parasitic capacitances across the resistance. A large capacitance at the current source of the enhancement circuit was found to limit the impedance and therefore the amount of degeneration in the filter.

A feasible tuning technique was demonstrated using direct digital tuning. A test setup was used to sub-sample the noise shaped by the filter and perform the necessary Q and frequency tuning. The tuning technique was able to tune the filter over a frequency range equal to half the sampling frequency.

The specific contributions made in this thesis are summarized as follows:

- A new understanding of the dynamic range of Q-enhanced filters was accomplished. A closed form expression was developed relating the dynamic range of the filter to the operating Q was developed to fully understand the effects of Q-enhancement on linear range. This expression was proven with both simulation and test results.
- The use of Q-enhanced filters with a large operating Q (500 – 1000) was explored. A dynamic range of over 40 dB is accomplished for an IF filter with a Q of 650, operating at 500 MHz.
- A Q-enhanced filter was implemented with operating frequency up to 2.4 GHz using on-chip inductors. The feasibility of using this filter as a front-end filter in radio receivers was analyzed.
- A digital tuning technique was suggested for directly tuning the Q-enhanced filter. Initial analysis and a test implementation demonstrated the feasibility of such architecture.

6 Recommendations

The work of this thesis has shown the usefulness of the Q-enhanced filter for radio transceivers. To obtain a complete on-chip filtering solution, further work, outside the scope of this thesis, must be done. Two main areas for further research are outlined below.

High Linearity Transconductors

The analysis of Section 3.3 and the results of Section 4.3 show the importance of the linearity of the enhancement transconductor in the overall dynamic range performance of the filter. Further improvements to the linearity could be possible with different circuit innovations. Many texts and papers have been written on the subject of high linearity transconductors [11]. Most of these transconductors are used for lower frequency G_m -C filters and would be limited in their high frequency capabilities because of parasitic capacitances and feedback. There are some that offer simpler alternatives that may improve the linear range without limiting the operating frequency [14]. The challenge will be to find a transconductor that can extend the linear range at high Q without sacrificing a large amount of power.

Digital Tuning Methodology

This thesis has shown that the Q-enhanced filter can be digitally tuned using sub-sampling. To show that these functions can be integrated into one system, it will be necessary to implement the tuning function in digital circuitry in an FPGA and later integrate this functionality onto the same chip as the filter. This will allow real-time tuning with the algorithm optimized for minimum interference with the desired signal.

The accuracy of using noise shaping to measure the frequency and Q of the filter is another area for further research. Spectral analysis and sampling theory can give some insight into the necessary sampling time and algorithm for accurate measurement.

Another possibility for direct digital tuning is for implementation of continuous tuning. It is conceivable that the filter Q and frequency could be adjusted in the presence of an incoming signal spectrum through signal processing in the digital domain. The exploration of this possibility is an excellent opportunity for further research.

7 References

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Appendix A: Test Circuit Diagrams

Appendix B: Matlab Code for Filter Tuning

```

% Tuning Script
% July 23, 2001

% variables

global data;
% nStepsCoarse = 2^10;
% nStepsFine = 2^14;
samplingFreq = 40e6;
tuneFreq = 18e6;           % frequency to tune to (between 0 and samplingFreq/2)
vf = -0.691;
%vf = 0.84834;
vQ = 0.18;
vflncCoarse = 2e-3;        % amount to increment each step in frequency
vflncFine = 500e-6;        % amount to increment each step in frequency
vQlncCoarse = 3e-3;        % amount to increment each step in Q
vQlncFine = 200e-6;        % amount to increment each step in Q
freqTolCoarse = 0.05e6;    % tolerance for frequency tuning
freqTolFine = 0.05e6;      % tolerance for frequency tuning
RMS_limit = 9;             % limit at which to switch the atten / rfamp
RMS_final = 40;            % final Q to meet
RMS_tol = 0.5;

% set rf amp and attenuator at minimum
attenSet(0);
rfampSet(4.5);
pause(1);
vset(SMQ, vQ);
vset(SMf, vf);             % start frequency in the center of the band (1.08 - 1.1)

[RMS_Data, f_c] = fishcount(samplingFreq);

if f_c < tuneFreq

```

```

    fincrement = 1;
else
    fincrement = 0;
end

% coarse frequency tuning

while abs(f_c-tuneFreq) > freqTolCoarse
    if f_c < tuneFreq
        if fincrement == 0
            vflncCoarse = vflncCoarse / 2;          % decrease the increment
        end
        vf = vf + vflncCoarse;
        fincrement = 1;
    else
        if fincrement == 1
            vflncCoarse = vflncCoarse / 2;          % decrease the increment
        end
        vf = vf - vflncCoarse;
        fincrement = 0;
    end

    vset(SMf,vf);
    [RMS_Data,f_c]=fishcount(samplingFreq);
    disp(sprintf('f adjusted to vf= %f, f_c = %f, Increment = %f,vf,f_c,vflncCoarse));
    %disp(sprintf('RMS= %f,f_c=%f,RMS_data,f_c));

end

Qincrement = 0;      % set previous increment to 0 meaning down

% Q tuning rfAmp @ 4.1

```

```

while abs(RMS_Data - RMS_limit) > RMS_tol

    if RMS_Data < RMS_limit
        if Qincrement == 0
            vQIncCoarse = vQIncCoarse / 2;          % decrease the increment
        end
        vQ = vQ + vQIncCoarse;
        Qincrement = 1;
    else
        if Qincrement == 1
            vQIncCoarse = vQIncCoarse / 2;          % decrease the increment
        end
        vQ = vQ - vQIncCoarse;
        Qincrement = 0;
    end

    vset(SMQ,vQ);

    [RMS_Data,f_c]=fishcount(samplingFreq);
    disp(sprintf('Q adjusted to vQ= %f, RMS_data = %f, Increment = %f,vQ,RMS_Data,vQIncCoarse));

    if f_c < tuneFreq
        fincrement = 1;
    else
        fincrement = 0;
    end

    % fine frequency tuning

    vflncFine_step = vflncFine;
    while ((abs(f_c-tuneFreq) > freqTolCoarse) & (RMS_Data > RMS_limit-RMS_tol))
        % ensure frequency tuning is done whenever we are above the limit

```

```

% or coarse Q tuning is complete (the while loop will be finished above)
if f_c < tuneFreq
    if fincrement == 0
        vflncFine_step = vflncFine_step / 2;          % decrease the increment
    end
    vf = vf + vflncFine_step;
    fincrement = 1;
else
    if fincrement == 1
        vflncFine_step = vflncFine_step / 2;          % decrease the increment
    end
    vf = vf - vflncFine_step;
    fincrement = 0;
end
vset(SMf,vf);

[RMS_Data,f_c]=fishcount(samplingFreq);
disp(sprintf('vf= %f, f_c = %f, inc = %f,vf,f_c,vflncFine_step));
end
end
disp(sprintf('finished coarse tuning, vQ = %f, frequency = %f,vQ,f_c));

% fine Q tuning rfAmp @ 4.3 no attenuation

attenSet(1); % change attenuation to minimum
rfampSet(4.3);

% 1 last fine frequency tune (with 2^14 data points)
[RMS_Data,f_c]=fishcount(samplingFreq);
disp(sprintf('FF tune: vf= %f, f_c = %f,vf,f_c));

vflncFine = 100e-6;

```



```

while (abs(f_c-tuneFreq) > freqTolFine)
% ensure frequency tuning is done whenever we are above the limit
% or coarse Q tuning is complete (the while loop will be finished above)
    if f_c<tuneFreq
        vf = vf + vfIncFine;
    else
        vf = vf - vfIncFine;
    end
    vset(SMf,vf);
    [RMS_Data,f_c]=fishcount(samplingFreq);
    disp(sprintf('FF tune: vf= %f, f_c = %f',vf,f_c));
end

```

```

[RMS_Data,f_c]=fishcount(samplingFreq);

```

```

while abs(RMS_Data-RMS_final)>RMS_tol

```

```

    if RMS_Data < RMS_final
        if Qincrement ==0
            vQIncFine = vQIncFine / 2;          % decrease the increment
        end
        vQ = vQ + vQIncFine;
        Qincrement = 1;
    else
        if Qincrement == 1
            vQIncFine = vQIncFine / 2;          % decrease the increment
        end
        vQ = vQ - vQIncFine;
        Qincrement = 0;
    end
end

```

```

vset(SMQ,vQ);

```

```

[RMS_Data,f_c]=fishcount(samplingFreq);

% filter data
%     filterOrder = 80;
%     filtDenCoef1 = fir1(filterOrder,[tuneFreq*2/samplingFreq-0.025
tuneFreq*2/samplingFreq+0.025]);
% bandpass1 definition
%     filtNumCoef = zeros(1,filterOrder);
%     filtNumCoef(1) = 1;
%     outData = filter(filtDenCoef1,filtNumCoef,outData);    % filter1 response

disp(sprintf('Q tuning, RMS level: %f, vQ: %f',RMS_Data,vQ));
end

```