A CMOS Wide Output Voltage Swing DM Modulator for Envelope Tracking Technique

By

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Abstract

Due to its low cost, fast speed but low power consumption and high integration, the CMOS technology has witnessed its own explosive development in recent years. Although the deep sub-micron CMOS technology has some limitations in power amplifier design, its advantages have always been attractive to researchers who have done their best to overcome these limitations. It has been reported that Class A, AB, C, D, E, F power amplifiers and some efficiency enhancement techniques have been successfully implemented in 0.35 μm CMOS process in the past few years.

However, research is rarely done on power amplifiers using efficiency enhancement techniques implemented in 0.18 μm and lower CMOS technology due to their breakdown voltages being too low and the expected low output power. As exploratory research, in this thesis, a wide output voltage swing delta modulated (DM) modulator for the envelope tracking technique has been designed in 0.18 μm CMOS technology. Post-layout simulation indicates that the modulator achieved a bandwidth larger than 2.0 MHz, the output voltage range from 0 V to 1.6 V, and a maximum output power close to 500 mW.

As part of the modulator, a rail-to-rail input/output wide bandwidth op-amp and an envelope detector are also designed. The simulation results supported the design methodology.

Acknowledgements

It is my great pleasure to take this opportunity to thank everyone who made this thesis possible.

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List of Abbreviations

AC	Alternating current
AM	Amplitude modulation
CDMA	Code division multiple access
CMOS	Complementary metal oxide silicon
DC	Direct current
DM	Delta modulation
EER	Envelope elimination and restoration
ET	Envelope tracking
GBW	Gain bandwidth product
IMD	Intermodulation distortion
IMD3	Third-order intermodulation
LINC	LInear amplification using nonlinear component
NMOS	N-channel metal oxide silicon
op-amp	Operational amplifier
PA	Power amplifier
PMOS	P-channel metal oxide silicon
PWM	Pulse width modulation
RF	Radio frequency
RHP	Right half plane
SEPIC	Single ended primary inductance converter
SOC	System-on-chip
THD	Total harmonic distortion
WCDMA	Wideband code division multiple access

List of Symbols


Diode


Capacitor


DC voltage source


Ground


Resistor


Inductor


Switch


Current source


PMOS transistor


VDD


NMOS transistor

CHAPTER 1 *Introduction*

Recent years have witnessed an explosive growth of portable radio frequency (RF) devices (e.g., mobile phones and personal digital assistants) and their increasing functional densities (e.g., audio, video and data). However, the battery life has always been a consideration as consumers choose these devices. Before the battery techniques achieve a tremendous improvement, how to use the battery power more efficiently continues to be an area of exploration for researchers and designers of mobile RF devices. Compared to other components of a RF system, power amplifiers (PAs) play a dominant role in energy efficiency, because PAs normally determine the power consumption of the system.

RF PAs of Class C, Class E and Class F achieve very high efficiencies (around 60% or more) in practical design. However, their linearity is poor and they are often called nonlinear PAs. The nonlinear characteristic of this type of PAs limits their applications. For some wireless communication systems (e.g., code division multiple access (CDMA), wideband CDMA (WCDMA)), the adjacent channel power ratio is a crucial specification, which requires that PAs used in these systems must be linear.

It is well known that the simple topology linear RF PAs (e.g., Class A, Class AB) have very low efficiencies, especially when the RF signal has a nonconstant envelope. The relative high efficiency can only be achieved at the high output power region (or at the peak of the envelope). However, most of the time the PA stays in idle or low output power state, which drags the average power efficiency (over the full range of output power) to a very low level, because the DC power consumption remains constant at the low output

power region (or at the valley of the envelope). Therefore, efficiency enhancement techniques with high level linearity are always of research interests.

The power efficiency enhancement techniques with high level linearity include the Doherty technique, LInear amplification using Nonlinear Component (LINC) technique, Envelope Elimination and Restoration (EER) technique and Envelope Tracking (ET) technique (also called dynamic power supply technique). Considering the system-on-chip (SOC) solutions, the configuration complexity and operation bandwidth, the envelope tracking technique is most suitable for the RF portable circuits which need high efficiency and high linearity. The basic idea of this technique is to combine a linear PA with an efficiency enhancement dynamic power supply circuit, which synchronously follows the varition of the input RF signal envelope and has little or no effect on the linearity of the linear PA.

DC-DC converters have been used as the circuit of efficiency enhancement dynamic power supply. The DC-DC converters can be categorized into three basic types, including step-down, step-up and buck-boost DC-DC converters. Based on their characteristics, these converters can provide the power supply to the linear PA with a lower or higher or form lower to higher voltage than the constant supply voltage of a battery.

When the gate length of a CMOS technology shrinks, the maximum allowable supply voltage gets lower. For example, the typical value of the supply voltage of the 90 nm CMOS technology is 1.2 V. This makes the step-down converter a better choice as the dynamic power supply circuit to a linear PA implemented in an advanced deep sub-micron CMOS technology.

In this thesis, the efficiency enhancement techniques with high level linearity and the basic types of the DC-DC converters used as the circuit of efficiency enhancement dynamic power supply are reviewed, a fast modulator, namely a delta modulated step-down DC-DC converter, is designed. The post-layout simulation results are presented.

1.1 Contributions

(i) A rail-to-rail input comparator has been proposed and this leads to a wide output voltage swing modulator to be realized.

(ii) To the best of the author's knowledge, this is the first delta modulated (DM) modulator for the dynamic power supply of a linear RF PA implemented in 0.18 μm CMOS technology.

1.2 Thesis Organization

The remainder of this thesis is organized as follows:

- Chapter 2: Overview of power efficiency enhancement techniques and DC-DC converters.
- Chapter 3: Modulator Implementation.
- Chapter 4: Simulation results.
- Chapter 5: Conclusion and future work.
- Appendices A, and B contain auxiliary information.

CHAPTER 2

Overview of Power Efficiency Enhancement Techniques and DC-DC Converters

2.1 Introduction

The battery powered nature of RF devices leads to the development of power amplifiers exhibiting maximized efficiency with an acceptable level of linearity. The intention of improving the inherent design trade-off between efficiency and linearity has drawn a great deal of interest in applying more advanced amplifier architectures. The efficiency enhancement techniques and both their advantages and disadvantages are discussed in the following section.

It has been reported in literature that three basic types of DC-DC converters are used as the circuit of efficiency enhancement dynamic power supply applied in Envelope tracking (ET) technique. For example, Ranjan used a step-down converter in [1], Hanington used a step-up converter in [2] and Staudinger used a single ended primary inductance converter (SEPIC) in [3]. All these three basic types of DC-DC converters are reviewed in section 2.3.

2.2 PA Efficiency Enhancement Techniques

In literature, a variety of efficiency enhancement techniques have been reported. In this section, the following techniques are reviewed and discussed: Doherty technique, LINC technique, EER technique and ET technique.

2.2.1 Doherty Technique

The Doherty configuration was originally proposed by Doherty in 1936 [4]. It is an efficiency enhancement technique. The block diagram of a Doherty amplifier is shown in Figure 2.1. It consists of a main (or carrier) power amplifier and an auxiliary (or peaking) amplifier. The outputs of the two power amplifiers are combined by a quarter wavelength transmission line Z_m. In order to compensate for the delay introduced by Z_m, another quarter wavelength transmission line Z_a, is inserted between the auxiliary amplifier and its input. The main amplifier is normally biased at Class B and the auxiliary amplifier is typically biased at Class C. When the input amplitude is small, only the main amplifier is active, and when the input amplitude is large, both the main and auxiliary amplifiers contribute to the output power.

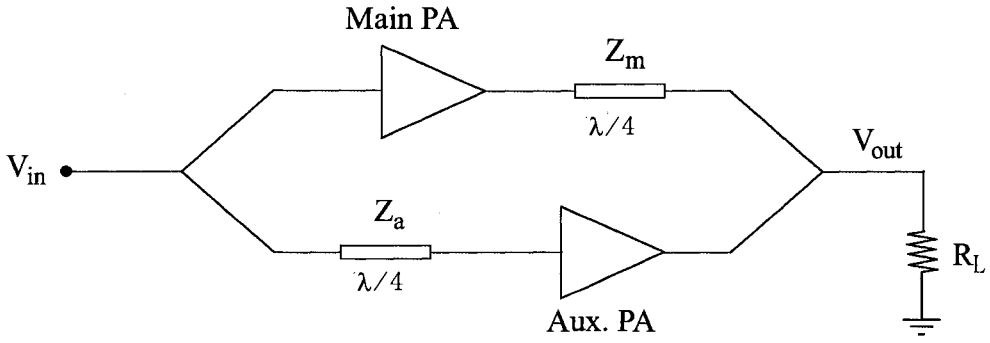


Figure 2.1 Block diagram of Doherty amplifier

The Doherty technique has three power operation modes [5], which are peak power operation, medium power operation and low power operation. In the peak power operation mode, both the main and auxiliary amplifiers are saturated. They see the same

output impedance and thus contribute the same power to the load. In the peak power mode, the efficiency is 78.5%, the same as the maximum efficiency of a Class B PA.

In the low power operation mode, the auxiliary amplifier remains to be cut off. The main amplifier operates as an ordinary class B amplifier does. Therefore, it has all the characteristics of a Class B amplifier. The instantaneous efficiency increases linearly with the output power to 78.5%.

In the medium power operation mode, the Doherty amplifier achieves a high efficiency by keeping the main amplifier at maximum device output voltage when the auxiliary amplifier is operating. The main amplifier remains saturated and acts as a voltage source. It delivers an increasing amount of power at the peak efficiency [6]. At the same time the auxiliary amplifier operates as a linear current source.

The Doherty amplifier uses the active load pull technique. This means that its operation is equivalent to the resistance or reactance of the RF load being modified by applying the current from a second phase coherent source, namely, the auxiliary amplifier [7].

The Doherty technique is an efficiency enhancer rather than a linearization technique. The intermodulation distortion (IMD) performance, when using this technique alone, is relatively poor. The linearity of the Doherty power amplifier can be improved by adopting pre-distortion or other linearization techniques. The transmission line and phase matching requirements generally restrict Doherty technique to a very narrow band of operating frequencies. The auxiliary amplifier can cause gain degradation. Furthermore, the complicated configuration of Doherty technique is challenging for portable applications.

2.2.2 LINC Technique

The LINC (also known as Chireix Outphasing Amplifier) technique was proposed by Chireix during the 1930s [8]. D.C. Cox used this technique at microwave frequencies and introduced the acronym LINC. The block diagram of LINC technique is shown in Figure 2.2. The operation of the LINC technique can be understood with the aid of the following mathematical expressions [9]. A band limited baseband input signal can be expressed as:

$$V_{in} = r(t)e^{j\phi(t)}, \qquad 0 \le r(t) \le r_{max} \tag{2-1}$$

This input signal can be separated into two constant amplitude phase modulated signals by the signal separator in Figure 2.2:

$$\left.\begin{aligned} V_1(t) &= r_{max}e^{j[\phi(t)+\theta(t)]} \\ V_2(t) &= r_{max}e^{j[\phi(t)-\theta(t)]} \\ \theta(t) &= \cos^{-1}\left(\frac{r(t)}{2r_{max}}\right) \end{aligned}\right\} \tag{2-2}$$

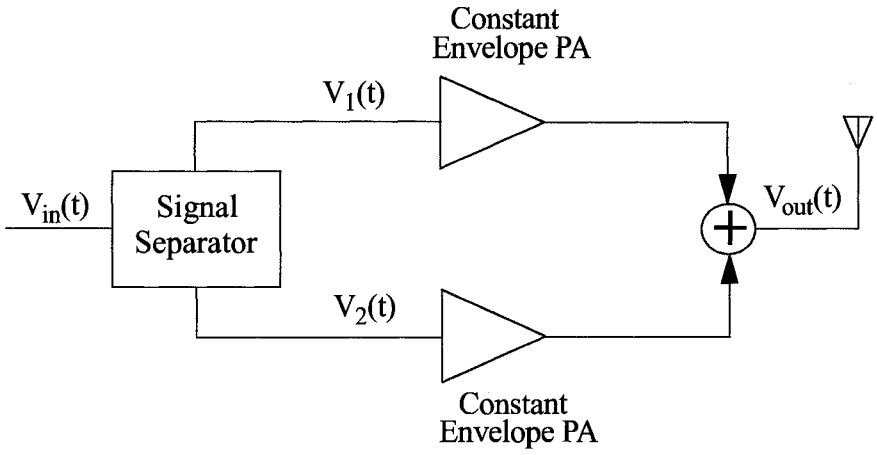


Figure 2.2 Block diagram of LINC technique

From (2-2) one can see that the two separated signals $V_1(t)$ and $V_2(t)$ have the same constant amplitude, the only difference between the two signals are their phases. Therefore, these two signals can be individually amplified by highly nonlinear but power efficient amplifiers (e.g. Class E and Class F power amplifiers). The output signals are then recombined, through a combiner, into the final output signal $V_{out}(t)$, which has the same amplitude and phase information as that of $V_{in}(t)$. Since each amplifier operates in a highly nonlinear and efficient mode, the LINC technique potentially achieves a high efficiency without compromising the linearity.

In order to assure obtaining high efficiency and high linearity, some design issues must be considered. First, the gain and phase imbalances between the two amplification paths can lead to residual distortion. Second, the interaction between the two nonlinear amplifiers through the combiner can cause the two phase modulated signals to corrupt each other's phase [10], and consequently decrease the overall linearity of the system. Therefore, more work in this field must be done before LINC can be readily integrated into portable applications.

2.2.3 Envelope Elimination and Restoration Technique

Envelope elimination and restoration technique was first proposed in 1952 by Kahn [11]. It combines a highly efficient and normally nonlinear switching-mode amplifier, e.g. Class F or Class E amplifiers, with a highly efficient and linear modulator (low frequency linear power amplifier) to realize a high efficiency and high linearity RF power amplifier. The block diagram of envelope elimination and restoration technique is shown in Figure 2.3. The envelope of the input RF signal is first eliminated by the limiter to generate a constant amplitude and phase modulated carrier signal while the amplitude information is extracted by the envelope detector. By modulating the power supply voltage of the PA, the original amplitude modulation is restored to the phase modulated signal. The primary advantage of EER technique is that there is no requirement of linearity for the RF

PA, which allows the output combiner, the RF PA, to be designed for the maximum efficiency [10].

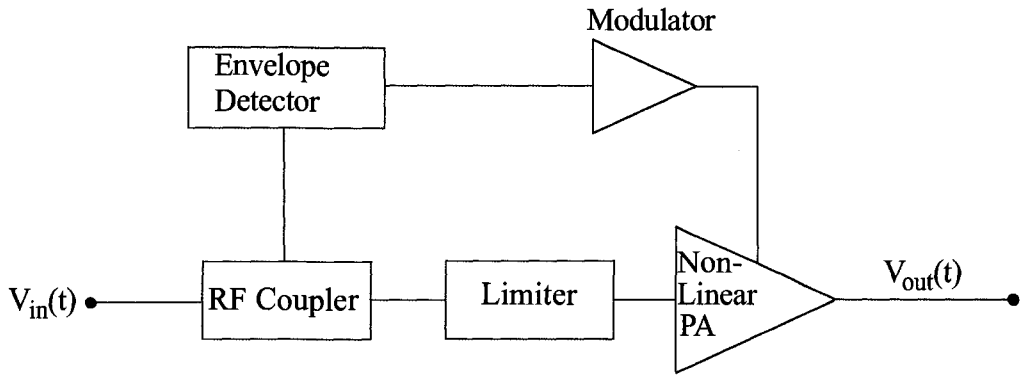


Figure 2.3 Block diagram of envelope elimination and restoration technique

Some design issues in EER technique should be considered. First, the mismatch between the delay in the phase and amplitude paths degrades the linearity. The delay in the low frequency amplitude path can be much longer than that of the RF phase path. The IMD introduced by the delay mismatch for two equal input tones has been derived by Raab [12],

$$IMD \approx 2\pi B_{RF}^2 \Delta\tau^2 \qquad (2\text{-}3)$$

where B_{RF} is the bandwidth of the RF signal and $\Delta\tau$ is the delay mismatch. For the two-tone signal, if the tone spacing is 1MHz, the third-order intermodulation (IMD3) is less than 40 dBc when the delay mismatch is less than 40 ns.

Second, the limiter can introduce substantial AM-to-PM conversion at high frequencies, this degrades the phase modulation for the output of the limiter. Third, the fidelity of the replica of the amplitude information should be high enough to assure the linearity of the EER system. These design issues make EER technique seem unattractive when being integrated on a chip.

2.2.4 Envelope tracking technique

Envelope Tracking technique is also called the dynamic power supply technique or bias adaptation [13]. Its architecture is shown in Figure 2.4, which is similar to that of the EER system. Both techniques have an envelope-detecting and a RF path. However, in ET technique there is no limiter. The RF drive of the RF power amplifier in ET technique keeps both phase and amplitude information, whereas the RF drive in EER only keeps the phase information. The combination of the envelope detector and the modulator (DC-DC converter) in Figure 2.4 provides varying supply voltage to the RF power amplifier according to the variation of the envelope. At the same time, the varying supply voltage must have sufficient headroom [6] to make sure that the RF PA operates in a linear mode.

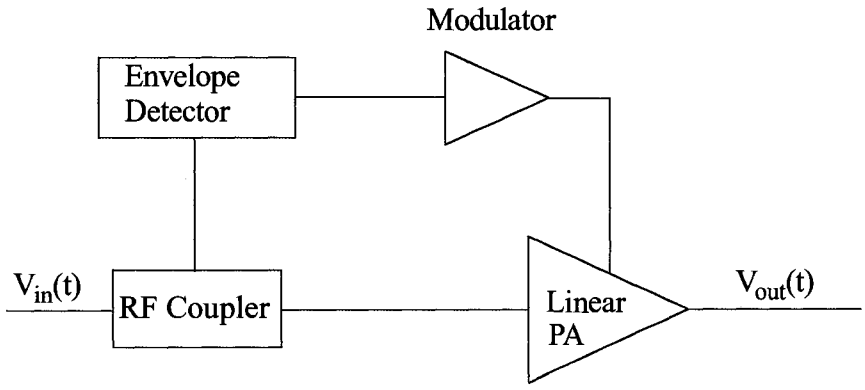


Figure 2.4 Block diagram **of envelope tracking** technique

Typically the modulator is a DC–DC converter. Based on the design requirement, three basic types of converters, step-down (or buck), step-up (or boost) and SPEIC (buck-boost) converter, can be used. A DC-DC converter can achieve a very high efficiency (normally higher than 90%).

Since the DC power consumption is reduced at low output power state, the efficiency is improved, as shown in Figure 2.5 [6]. And because the RF amplifier is operating at linear mode, the supply variations do not need to follow the envelope exactly. These

merits make the ET technique more attractive when a design requires high efficiency and high linearity.

2.2.5 Comparison of the Power Efficiency

Power efficiencies of different efficiency enhancement techniques are compared in Figure 2.5. Except for the Kahn (i.e. EER) technique, which always has the highest efficiency, and Class A, which always has the lowest efficiency, every other technique has their own region of high efficiency. For example, in the low-power region, ET performs at a higher efficiency than LINC and Doherty do, while in the high-power region, LINC has a higher efficiency than ET and Doherty.

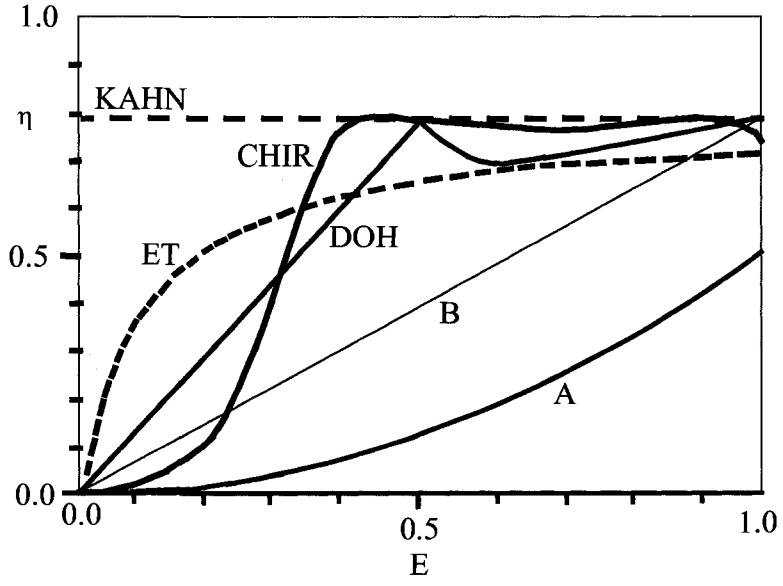


Figure 2.5 Efficiency as a function of output power [6]. A: Class A; B: Class B; ET: Envelope Tracking (i.e. Dynamic power supply); DOH: Doherty amplifier; CHIR: Chireix outphasing amplifier (i.e. LINC); KAHN: Kahn amplifier (i.e. EER)

2.3 Basic Types of DC-DC Converters

As mentioned already, the modulator in the ET architecture is essentially a DC-DC converter. A DC-DC converter converts its DC input voltage to a DC output voltage having a larger or smaller magnitude. There are more than 500 topologies of DC-DC convert-

ers [14]. In the following sections only those that can be easily used in the ET architecture are discussed. Based on the output characteristic of the DC-DC converters, they can be classified into three basic types: step-down (or buck), step-up (or boost) and SEPIC (buck-boost) converters.

2.3.1 Step-down (or Buck) Converter

A step-down converter [15] realizes the reduction of an input DC voltage. A conceptual topology is shown in Figure 2.6, which includes the input voltage supply V_{in}, switch S, diode D, inductor L and capacitor C. L and C constitute a lowpass filter and resistor R is the load of the converter. For simplicity, all the components in the converter are assumed to be ideal. The typical waveforms of the step-down converter are shown in Figure 2.8 (The detailed analysis of the typical waveform can be found in [15]).

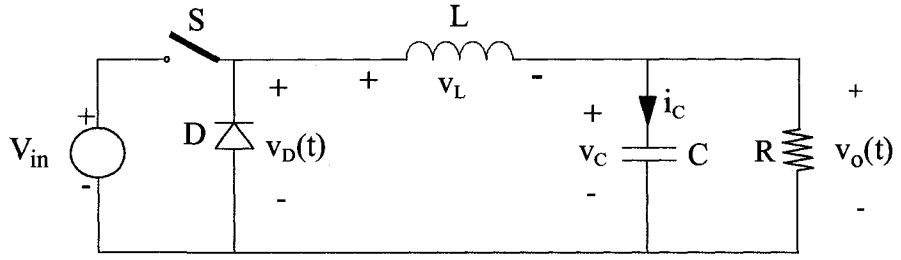


Figure 2.6 A conceptual topology of step-down converter

When S is closed, the diode D is reverse-biased, the voltage on the inductor $v_L=V_{in}-v_O$. Since v_L is nonzero, the current flowing through the inductor i_L increases linearly. The equivalent circuit is shown in Figure 2.7.

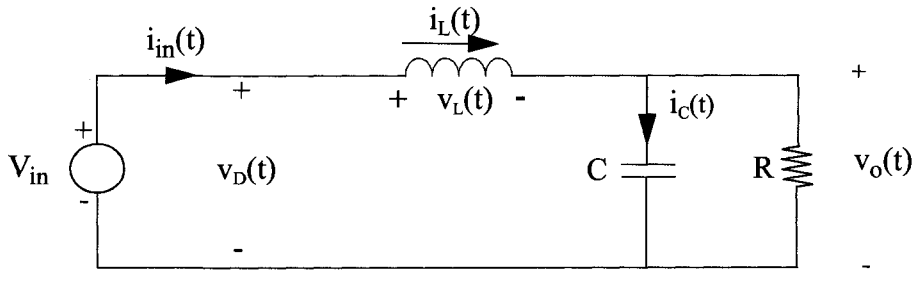


Figure 2.7 Equivalent circuit of the step-down converter with S closed

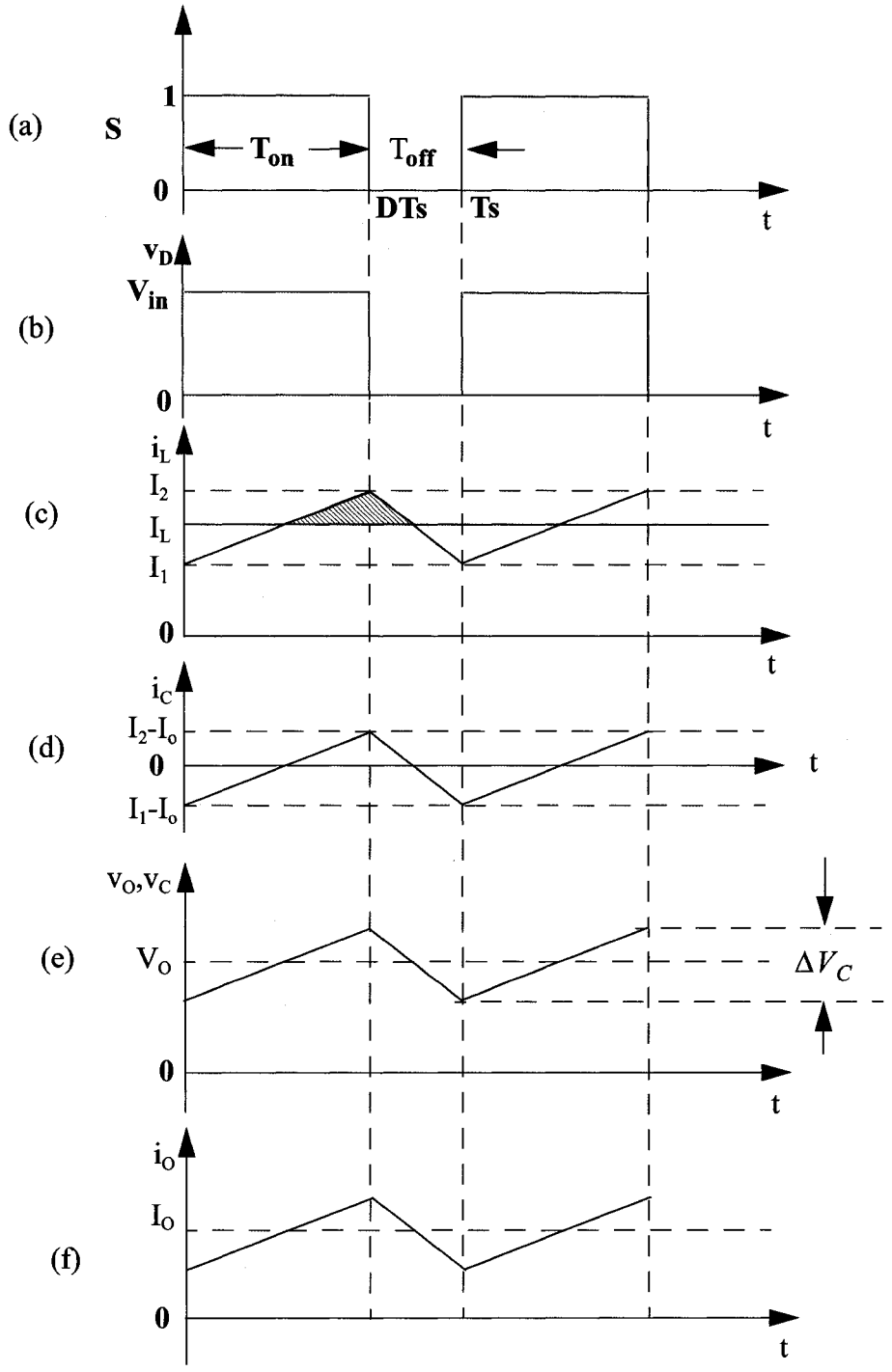


Figure 2.8 The typical waveforms of a step-down converter

When S is open, the diode D is forward-biased, the voltage on the inductor v_L=-v_O, the current flowing through the inductor i_L decreases linearly. The equivalent circuit is shown in Figure 2.9.

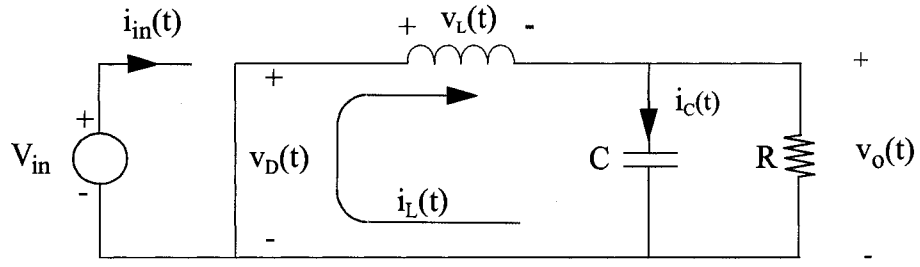


Figure 2.9 Equivalent circuit of the step-down converter with S open

During the time period T_{on}, the switch S is closed. The voltage on the inductor can be obtained from the equivalent circuit Figure 2.7,

$$v_L = L\frac{di_L}{dt} \tag{2-4}$$

The value of the capacitor C is assumed to be large enough, so the output voltage remains approximately to be a constant, the average of V_O. Therefore, the current i_L increases linearly from I_1 to I_2 (shown in Figure 2.8(c)). Equation (2-4) can be rewritten as

$$V_{in} - V_O = L\frac{I_1 - I_2}{T_{on}} = L\frac{\Delta I_L}{T_{on}} \tag{2-5}$$

Hence

$$T_{on} = \frac{(\Delta I_L)L}{V_{in} - V_O} \tag{2-6}$$

where ΔI_L is the change in current flowing through the inductor. V_O is the average of the output voltage.

During the time period T_{off}, the switch is open, the current i_L decreases linearly from I_2 to I_1 (shown in Figure 2.8(c)). The voltage on the inductor can be obtained from the equivalent circuit shown in Figure 2.9,

$$V_O = L\frac{\Delta I_L}{T_{off}}$$

Then T_{off} is given by,

$$T_{off} = \frac{(\Delta I_L)L}{V_O} \tag{2-7}$$

From (2-6) and (2-7) one can get,

$$(V_{in} - V_O)T_{on} = V_O T_{off}$$

Hence,

$$V_O = \frac{T_{on}}{T_{on} + T_{off}} V_{in} = \frac{T_{on}}{T} V_{in} = DV_{in} \tag{2-8}$$

where D is the switch duty cycle ratio. Since $0 \le D \le 1$, $0 \le V_{in} \le V_O$. At D=0, V_O=0 and at D=1, V_O=V_{in}. The voltage conversion ration M(D) is the ratio of the output to the input voltage of a DC-DC converter [15]. The voltage conversion ratio M(D) of a step-down converter is obtained from (2-8),

$$M(D) = V_O / V_{in} = D \tag{2-9}$$

The equation (2-9) is plotted in Figure 2.10.

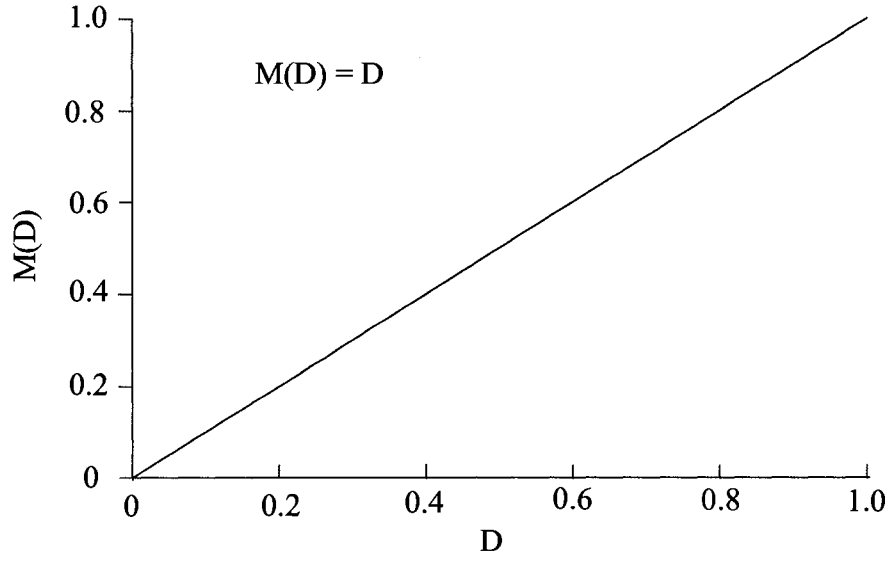


Figure 2.10 Step-down converter DC conversion ratio M(D)

Because the lowpass filter in the step-down converter is not ideal, the output voltage must consist of the desired DC component and the small undesired AC switching ripple. It is assumed that all the switching ripple in i_L flows through the capacitor C while all the DC component flows through the load resistor R. In the waveform of i_L shown in Figure 2.8(c), if $i_L<I_L$, then C will discharge through R. And if $i_L>I_L$, then C will be charged. Because in the steady state, the average of the current flow through the capacitor C should be zero in a cycle, the charge ΔQ stored in C or discharged from C during a half cycle $T_S/2$ can be calculated by the shaded area of the triangle in Figure 2.8(c),

$$\Delta Q = \frac{1}{2}\left(\frac{DT_S}{2} + \frac{T_S - DT_S}{2}\right)\frac{\Delta I_L}{2} = \frac{T_S}{8}\Delta I_L \tag{2-10}$$

The switching ripple voltage peak-to-peak (shown in Figure 2.8(e)) value is given by,

$$\Delta V_O = \Delta V_C = \frac{\Delta Q}{C} \tag{2-11}$$

Hence

$$\Delta V_O = \frac{\Delta I_L}{8 f_S C} \tag{2-12}$$

From (2-6) and (2-7), the switching cycle is

$$T_S = \frac{1}{f_S} = T_{on} + T_{off} = \frac{(\Delta I_L) L V_{in}}{V_O(V_{in} - V_O)},$$

Hence,

$$\Delta I_L = \frac{V_O(V_{in} - V_O)}{f_S L V_{in}} = \frac{V_{in} D(1-D)}{f_S L} \tag{2-13}$$

Using (2-8), (2-12) and (2-13),

$$\frac{\Delta V_O}{V_O} = \frac{1-D}{8LCf_S^2} = \frac{\pi^2}{2}(1-D)\left(\frac{f_c}{f_S}\right)^2 \tag{2-14}$$

where f_S is the switching frequency of buck converter, $f_c = \frac{1}{2\pi\sqrt{LC}}$ is the corner frequency of the lowpass filter. From (2-14) one can see that increasing f_S or decreasing f_c or doing both can decrease the amplitude of the switching ripple. This is an important observation for designing a step-down converter.

2.3.2 *Step-up (or Boost) Converter*

A step-up converter [15] can produce a DC output voltage with larger amplitude than the DC input voltage. A conceptual topology of a step-up converter is shown in figure 2.11 and its typical waveforms are shown in Figure 2.13(The detailed analysis of the typical waveform can be found in [15]).

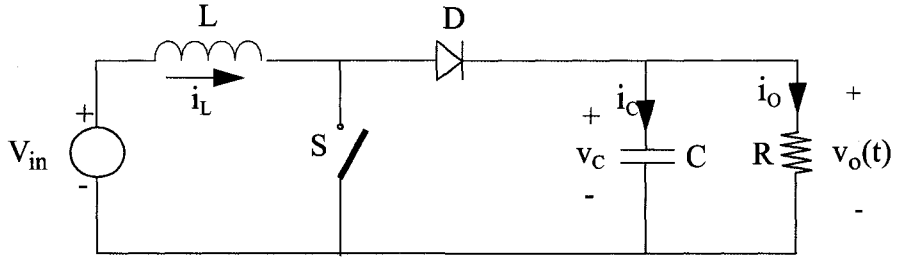


Figure 2.11 A conceptual topology of step-up converter

During the time period T_{on}, the switch S is closed. The diode D is reverse-biased. The energy coming from V_{in} is stored in the inductor L. The current i_L flowing through the inductor L increases linearly from I_1 to I_2 (shown in Figure 2.13(b)). Simultaneously capacitor C provides energy to load R. The equivalent circuit is shown in Figure 2.12. The voltage on the inductor in the equivalent circuit is

$$V_{in} = v_L = L\frac{I_2 - I_1}{T_{on}} = L\frac{\Delta I_L}{T_{on}} \tag{2-15}$$

where ΔI_L is the change of the current flowing through the inductor during the time period of T_{on}.

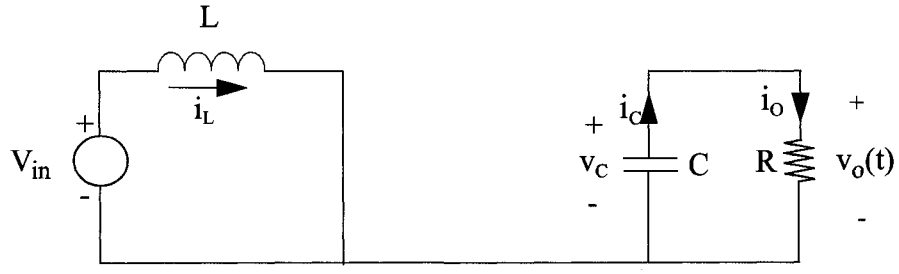


Figure 2.12 Equivalent circuit of the step-up converter with S closed

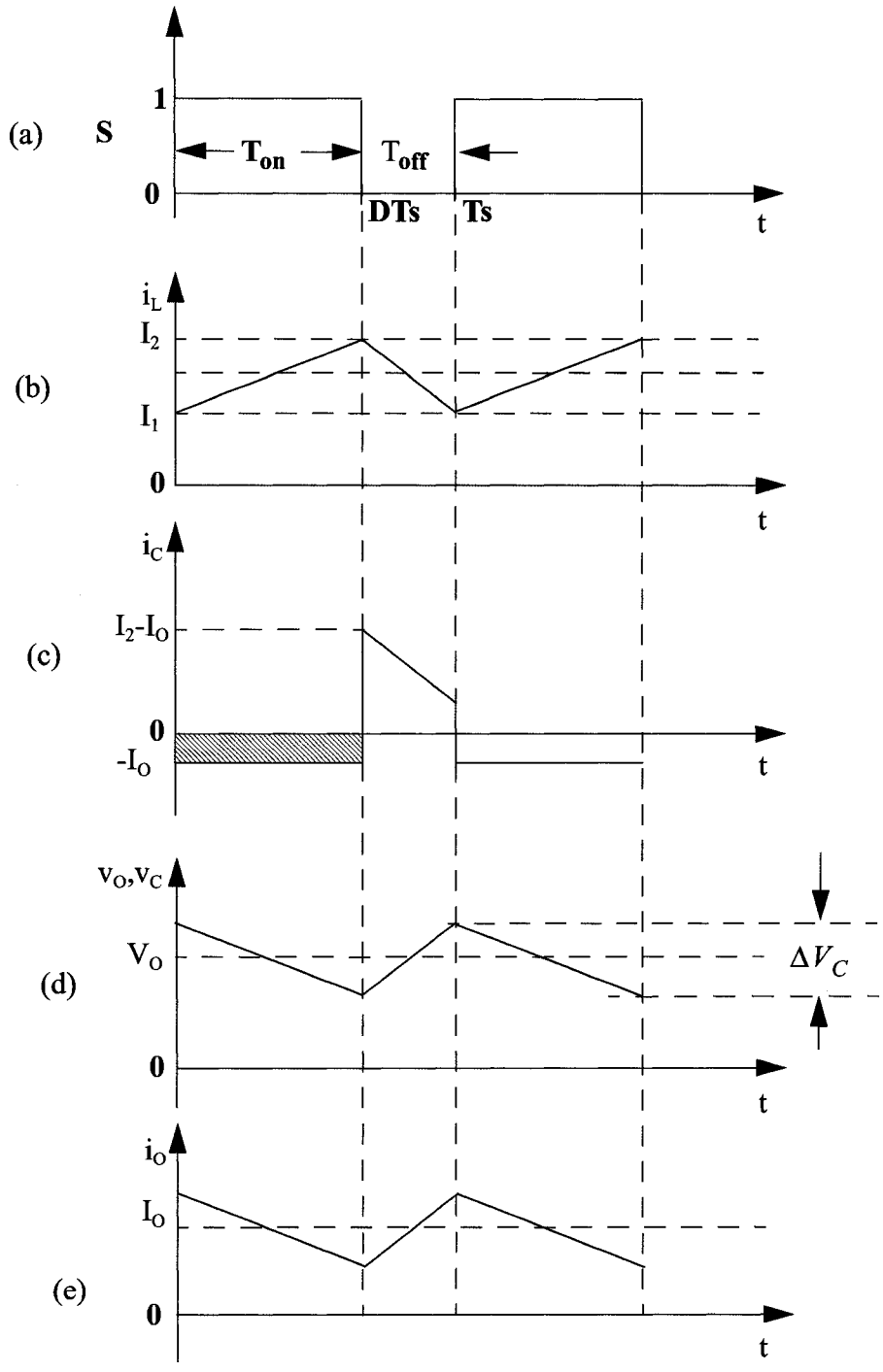


Figure 2.13 The typical waveforms of a step-up converter

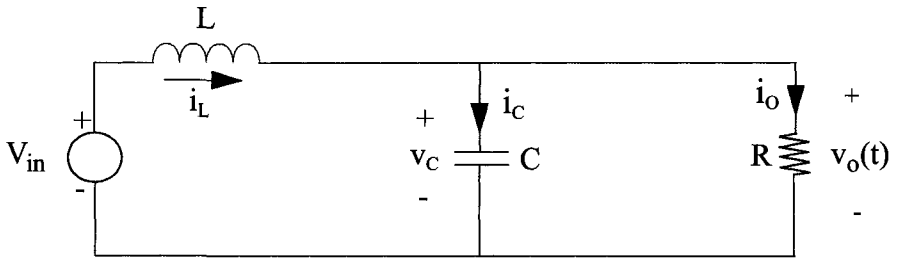


Figure 2.14 Equivalent circuit of the step-up converter with S open

During the time period T_{off}, the switch S is open. D is forward-biased. The energy stored in L charges C and provides energy to R. The current i_L decreases linearly from I_2 to I_1 (shown in Figure 2.13(b)). The equivalent circuit is shown in Figure 2.14. The voltage on the inductor can be obtained from the equivalent circuit shown in Figure 2.14,

$$V_O - V_{in} = v_L = L\frac{\Delta I_L}{T_{off}} \tag{2-16}$$

Using (2-15) and (2-16), one can easily obtain the following equation,

$$\frac{V_{in}T_{on}}{L} = \frac{V_O - V_{in}}{L}T_{off}$$

Then the average output voltage is given by,

$$V_O = \frac{T_{on} + T_{off}}{T_{off}}V_{in} = \frac{V_{in}}{1-D} \tag{2-17}$$

Then the voltage conversion ratio M(D) of a step-up converter is,

$$M(D) = \frac{1}{1-D} \tag{2-18}$$

From (2-17) one can see that at D=0, V_O=V_{in} and at D=1, V_O goes to infinity. The voltage conversion ratio is plotted in Figure 2.15.

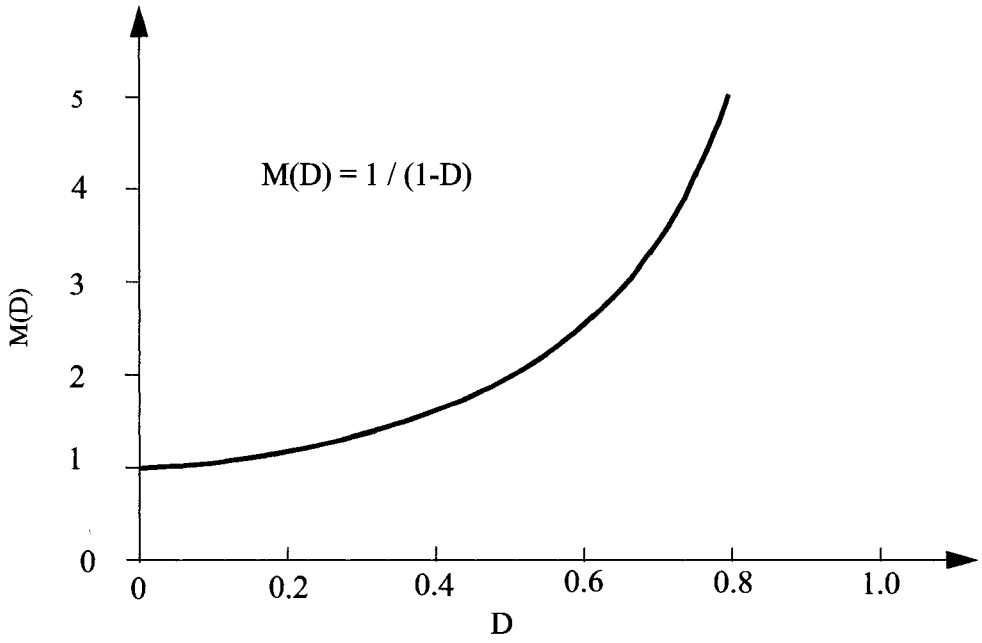


Figure 2.15 Step-up converter DC conversion ratio M(D)

2.3.3 SEPIC (Buck-Boost) Converter

A SEPIC (single-ended primary inductance converter) converter combines the properties of both the step-up and step-down converters. Based on the switch duty cycle ratio, this converter can produce the output voltage less than, greater than or equal to the input DC voltage. A conceptual topology of the SEPIC converter is shown in Figure 2.16.

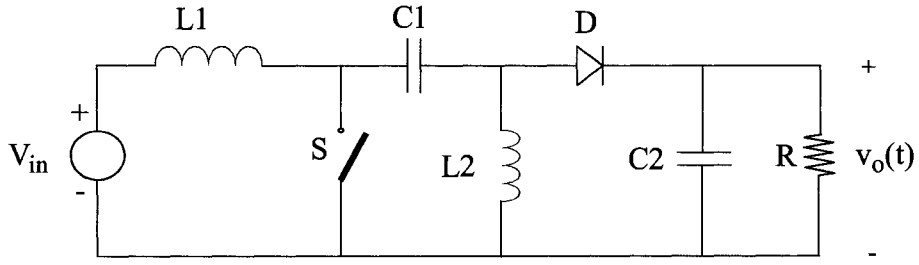


Figure 2.16 A conceptual topology of the SEPIC converter

When the switch S is closed, the equivalent circuit is shown in Figure 2.17. During this time the diode D is reverse-biased, the inductor L1 is charged from the input voltage source, L2 draws energy from C1, and C2 provides the load R current.

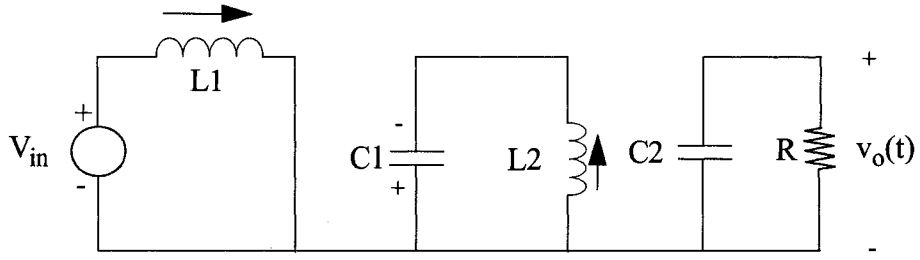


Figure 2.17 Equivalent circuit of the SEPIC converter with switch S closed

When the switch S is open, the equivalent circuit is shown in Figure 2.18. During this time period, the diode D is forward-biased, L1 charges C1 and also provides current to the load, which is connected to L2.

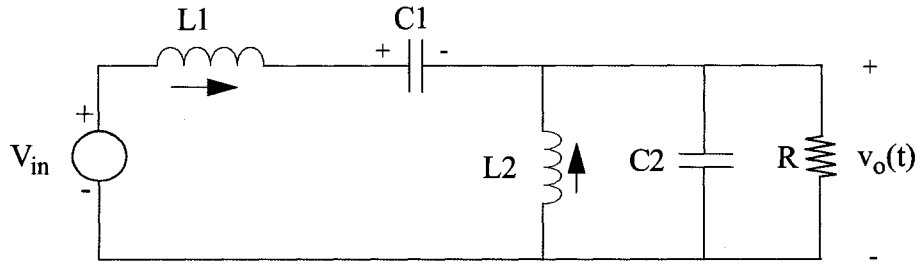


Figure 2.18 Equivalent circuit of the SEPIC converter with switch S open

The detailed analysis of SEPIC converter can be found in [16][17][18]. Here only the results are listed. The output voltage is given by

$$V_O = \frac{D}{1-D} V_{in} \tag{2-19}$$

Then the voltage conversion ratio M(D) of a step-up converter is

$$M(D) = \frac{D}{1-D} \tag{2-20}$$

From (2-19) one can see that at D=0, V_O=0 and at D=1, V_O goes to infinity. The voltage conversion ratio is plotted in Figure 2.19.

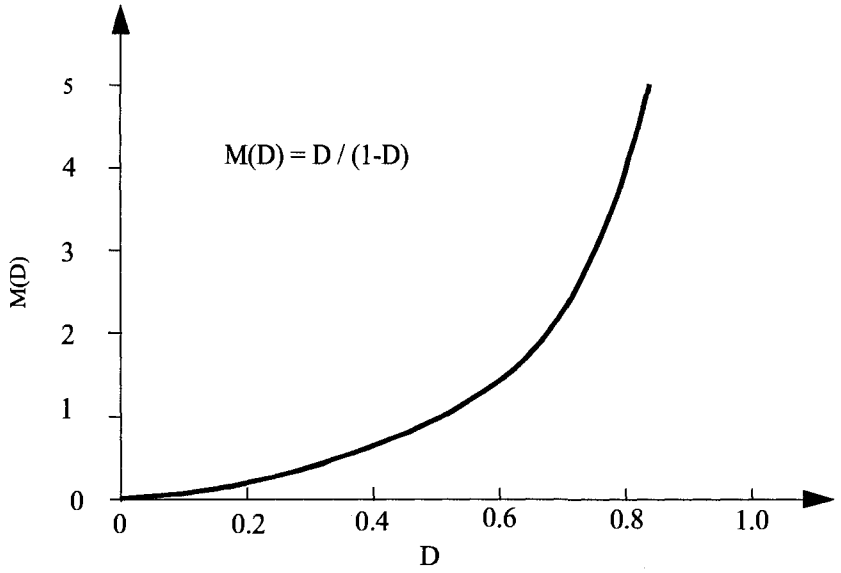


Figure 2.19 SEPIC converter dc conversion ratio M(D)

2.4 The Controller of a DC-DC Converter

A feedback controller is essential to the output of a DC-DC converter to make it less sensitive to the input disturbance, variation of the output load and variations in the converter circuit component values. The block diagram of a DC-DC converter with a feedback controller is illustrated in Figure 2.20. The following discussion focus is on two types of controller, conventional pulse width modulation (PWM) controller and delta modulation (DM) controller. The latter is discussed briefly here, and more details are discussed in Chapter 3.

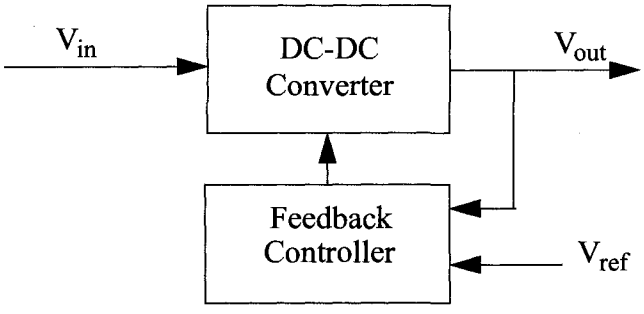


Figure 2.20 Block diagram of a DC-DC converter with feedback controller

2.4.1 Conventional Pulse Width Modulated (PWM) Controller

As shown in Figure 2.21, a conventional pulse width modulation controller posits between the output voltage V_o and the gate signal of the switch transistor M1. It is essentially a feedback loop. The operation principle is: The output voltage V_o is subtracted from the reference voltage V_{ref} to form the error signal, which is then amplified by the error amplifier to generate an amplified error signal V_{ea}. The PWM modulator consisting of the PWM comparator and the saw-tooth generator converts V_{ea} into the control signal which passes through the buffer circuit to control the switch transistor M1.

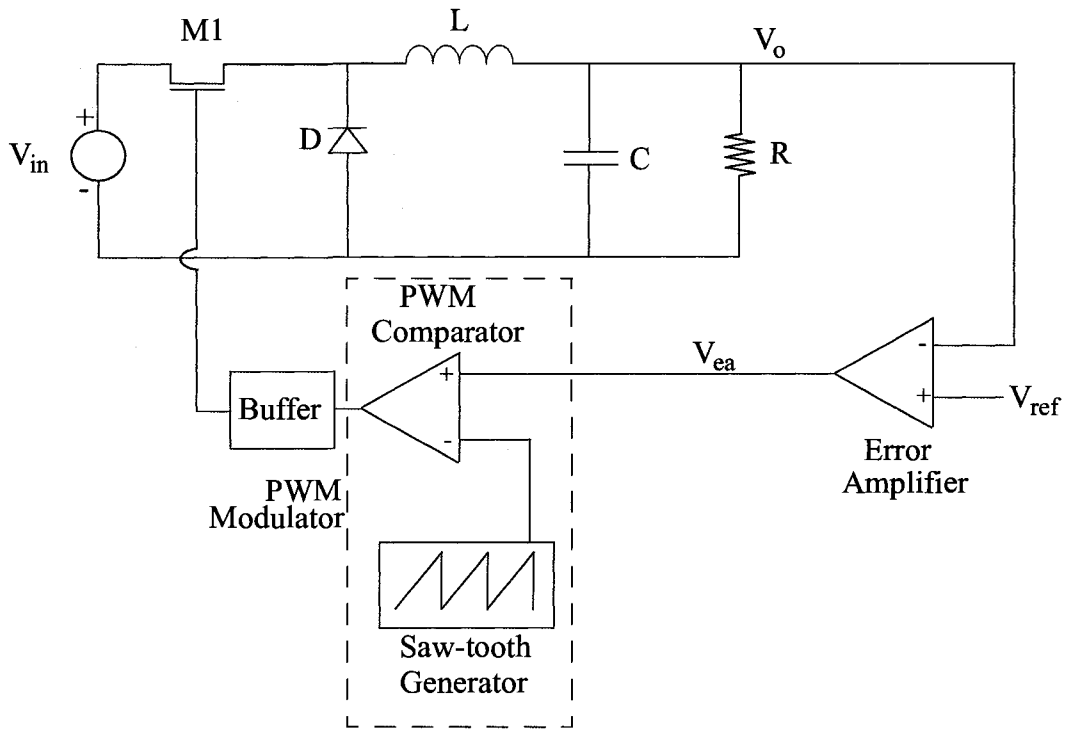


Figure 2.21 Block diagram of a DC-DC converter with feedback controller

2.4.2 Delta Modulated Controller

A delta modulated controller is another type of controlled DC-DC converter. Its topology is much simpler than that of a converter with the PWM controller feedback loop. As shown in the block diagram (Figure 2.22), the output voltage is directly fed to the comparator, and the output signal goes through the buffer to control the switch transistor M1. More details of this controller are discussed in chapter 3.

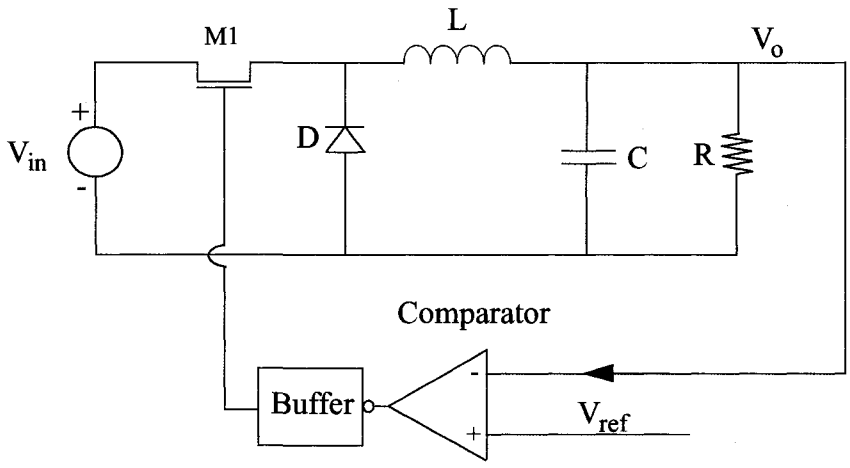


Figure 2.22 Block diagram of a delta modulated controller

2.5 Summary

From the above analysis one can see that PAs using the EER, Doherty and LINC techniques achieve higher efficiency. However, the Doherty and LINC techniques require quarter wave-length transmission lines, which make these techniques difficult to be integrated on a chip. The EER technique requires a highly accurate replica of the envelope of the input RF signal and compensation for the difference in the delay between the ampli-

tude and phase paths. The ET technique demonstrates a relatively high efficiency and high linearity, the accuracy of the replication of the envelope is not very strict, and it does not need the transmission line, so it is relatively easy to realize this technique on chips.

When designing a DC-DC converter (or modulator) for the ET power amplifier, according to the specific requirement, a step-down, step-up or SEPIC converter can be used. However, in this thesis, the goal is to design a modulator which can provide a dynamic power supply to a linear PA implemented by an advanced CMOS technology (the channel length is equal to or shorter than 0.18 μm). Therefore, the 0.18 μm CMOS technology and the step-down converter are chosen for the modulator implementation.

The next chapter describes the implementation of a wide output voltage swing delta modulator for the ET technique.

CHAPTER 3 *Modulator Implementation*

The architecture of the DM modulator is briefly described in Section 2.4.2. Figure 2.22 shows the core of the DM modulator. As a completely functional block, it also needs an envelope detector and an envelope amplification subblock. The complete block diagram of the DM modulator is shown in Figure 3.1. In this chapter, the operation of the modulator is analyzed and the hardware implementations of each subblock are described. Some design issues occurring at both the architectural and gate levels are discussed.

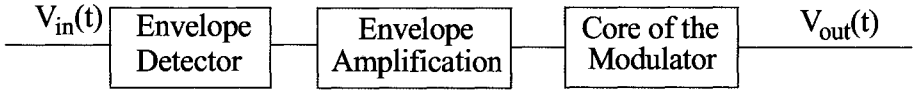


Figure 3.1 Block diagram of the complete DM modulator

3.1 The Core of the DM Modulator

3.1.1 Operation principle of the DM modulator

The principle block diagram of the modulator is shown in Figure 3.2. The operation of the modulator can be diveded into two procedures: (1) $V_o < V_{ref}$; (2) $V_o > V_{ref}$. During procedure 1, $V_o < V_{ref}$, hence V_{o1} is high and V_{o2} is low, therefore M1 is on and M2 is off. As a result, capacitor C will be charged by VDD and will V_o increase. As V_o increases to the level higher than V_{ref}, $V_o > V_{ref}$, the operation enters procedure 2. During this procedure, V_{o1} becomes low, V_{o2} becomes high, and M1 is off, M2 is on. Capacitor C will dis-

charge through M2, as a result V_0 will decrease. When V_0 decreases to the level lower than V_{ref}, the operation goes into procedure 1. The operation of procedure 1 and 2 happens alternatively, this operation is called self-oscillation. The oscillating frequency is dependent on the propagation delay between V_{ref} and V_0 and charge/discharge time of capacitor C.

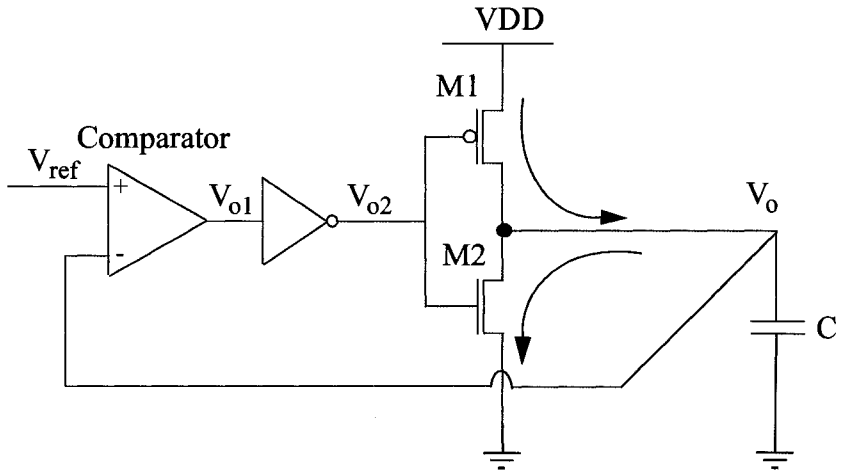


Figure 3.2 Principle block diagram of the modulator

3.1.2 Design of the modulator

A conceptual topology of DM modulator is shown in Figure 2.22. In order to implement it in a CMOS technology, the power stage must be redesigned. The diode D needs to be replaced because an ideal diode cannot be realized in a CMOS technology. Since the diode acts as a switch, it can be replaced by an NMOS transistor. And the switch MOSFET M1 can be replaced by a PMOS transistor. The two equivalent switches of NMOS and PMOS are complementary, so their gate drive signals are the same. After the replacement, a basic step-down converter without a controller implemented by CMOS process is shown in Figure 3.3.

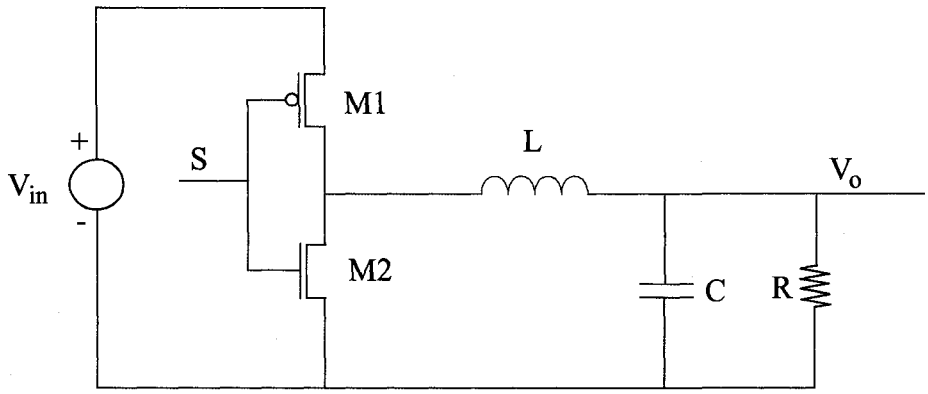


Figure 3.3 A basic CMOS step-down DC-DC converter

The replacement of the diode by an NMOS transistor brings the advantage of increasing power efficiency. This is because the replacement decreases the voltage drop (a typical value is 0.7 V) on a diode to the drain-source voltage of a transistor, which can be lower than 0.1 V.

In Figure 3.3, the two transistors M1 and M2 constitute an inverter. The transistors of this type of inverter inevitably conduct simultaneously during a period of time due to some kinds of nonidealities (such as the difference in the threshold voltage). This will cause the power efficiency to decrease especially when the switch frequency increases. To overcome this drawback, a non-overlapping circuit [19] is used, as shown in Figure 3.4, which assures that these two power transistors M1 and M2 can never conduct simultaneously. The outputs of the non-overlapping circuit are shown in Figure 3.5. The amount of the separation Δt is set by the delay of the NAND gate and the two inverters in series with the NAND gate output.

With the non-overlapping circuit, the modulator is transformed to the one shown in Figure 3.6, where the input voltage source V_{in} is replaced by VDD.

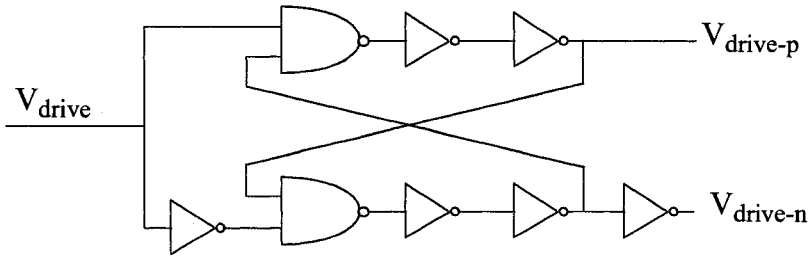


Figure 3.4 Block diagram of a non-overlapping circuit

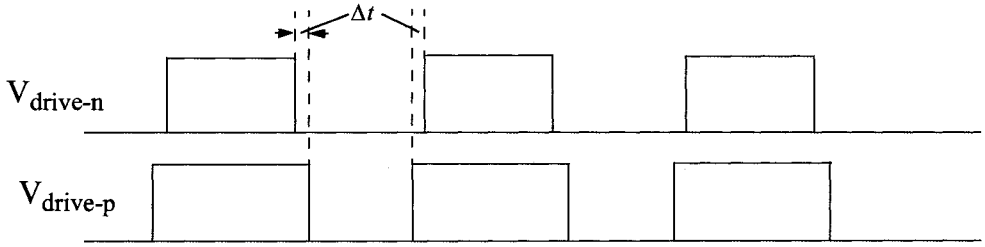


Figure 3.5 The outputs of the non-overlapping circuit

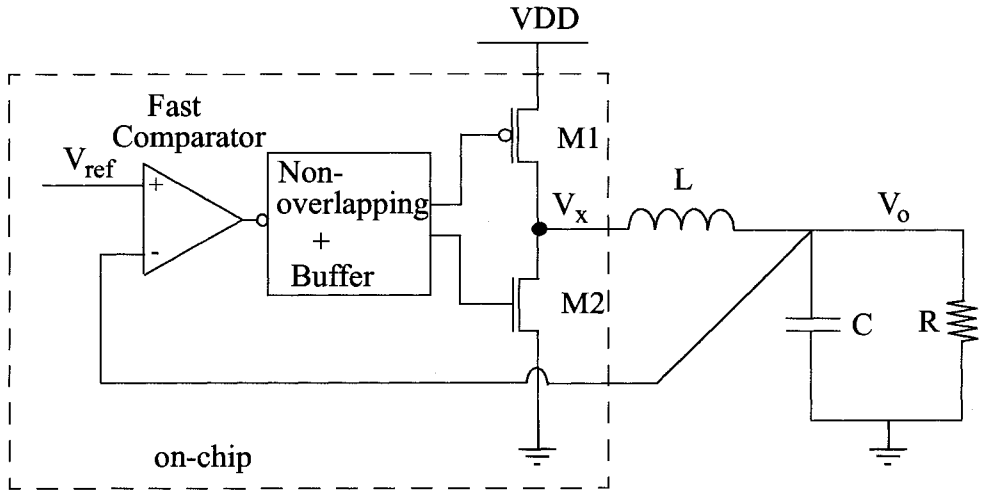


Figure 3.6 Block diagram of the modulator

3.1.3 Analysis of the Modulator

Considering the block diagram of the modulator in Figure 3.6, the input-to-output transfer function of the system is that $H_{LP}(s)$, the transfer function of the LC filter, multiplies $H_C(s)$, the transfer function of the circuit combination of the comparator, non-overlapping and buffer circuits. The magnitude of $H_C(s)$ can be modeled as a very large constant number while the phase of $H_C(s)$ is a function of the overall modulator delay and the switching frequency. When open-loop, the system transfer function can be presented by its magnitude and phase respectively. The magnitude of the system is

$$\|H(s)\| = \|H_{LP}(s)\| \cdot \|H_C(s)\| = \left\| \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \right\| \cdot A \tag{3-1}$$

where $\|H_C(s)\| = A$, $s = j\omega$, $\omega_0 = 1/\sqrt{LC}$

$$\|H_{LP}(s)\| = \left\| \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \right\| \tag{3-2}$$

Q is the quality factor of the second order L, C and R system and

$$Q = R\sqrt{\frac{C}{L}} = \frac{1}{2\zeta} \tag{3-3}$$

where ζ is the damping factor of the L, C and R low pass filter.

The duty cycle is assumed to be 50%, the phase of the system is given by,

$$\angle H(s) = \angle H_C(s) + \angle H_{LP}(s) = T_d \cdot f_s \cdot 2\pi + \angle H_{LP}(s) \tag{3-4}$$

where T_d is the overall modulator delay including the delay in the comparator, the non-overlapping and the buffer circuit. $\angle H_{LP}(s)$ is

$$\angle H_{LP}(s) = \angle H_{LP}(j\omega) = \text{atan}\left(\frac{\frac{1}{Q}\frac{\omega}{\omega_0}}{1 - \left(\frac{\omega}{\omega_0}\right)^2} \right) = \text{atan}\left(\frac{\frac{1}{Q}\left(\frac{f_s}{f_0}\right)}{1 - \left(\frac{f_s}{f_0}\right)^2} \right) \tag{3-5}$$

where $\omega = 2\pi \cdot f_s$, f_s is the switching frequency. $f_0 = \frac{1}{2\pi\omega_0} = \frac{1}{2\pi\sqrt{LC}}$.

Since the system is self-oscillating, the following condition is satisfied,

$$\angle H(s) = \pi = T_d \cdot f_s \cdot 2\pi + \text{atan}\left(\frac{\frac{1}{Q}\left(\frac{f_s}{f_0}\right)}{1-\left(\frac{f_s}{f_0}\right)^2}\right) \tag{3-6}$$

3.1.4 Output Residue Ripple

The waveform of switching supply V_x (in Figure 3.6) shown in Figure 3.7 has the switching frequency f_s. The primary component of the switching ripple in the output is the fundamental of the waveform. Using Fourier analysis, the coefficients of the fundamental are given by

$$a_1 = 2\int_{-\frac{1}{2}}^{-\frac{1}{2}+D} V_{DD}\cos(2\pi t)dt = -\frac{V_{DD}}{\pi}\sin(2\pi D - \pi) \tag{3-7}$$

$$b_1 = 2\int_{-\frac{1}{2}}^{-\frac{1}{2}+D} V_{DD}\sin(2\pi t)dt = -\frac{V_{DD}}{\pi}(\cos(2\pi D - \pi) + 1) \tag{3-8}$$

where D is the duty cycle ratio, then the magnitude of the fundamental is,

$$c_1 = \sqrt{a_1^2 + b_1^2} \tag{3-9}$$

the phase of the fundamental is,

$$\varphi_1 = -\text{atan}\left(\frac{b_1}{a_1}\right) \tag{3-10}$$

The magnitude of the fundamental vs. D is shown in Figure 3.8 and the phase of the fundamental vs. D is shown in Figure 3.9. According to Figure 3.8, when the duty cycle ratio is greater or less than 50%, the magnitude of the switching supply waveform fundamental will decrease. The phase is a linear function of the duty cycle D. When D is smaller than 50%, it leads to a phase advance and when D is larger than 50%, it leads to a phase lag.

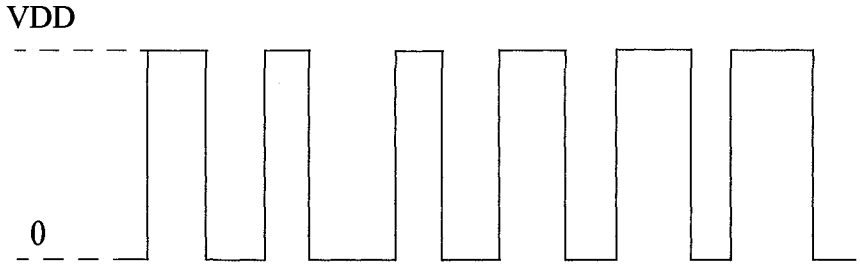


Figure 3.7 The waveform of switching supply V_x

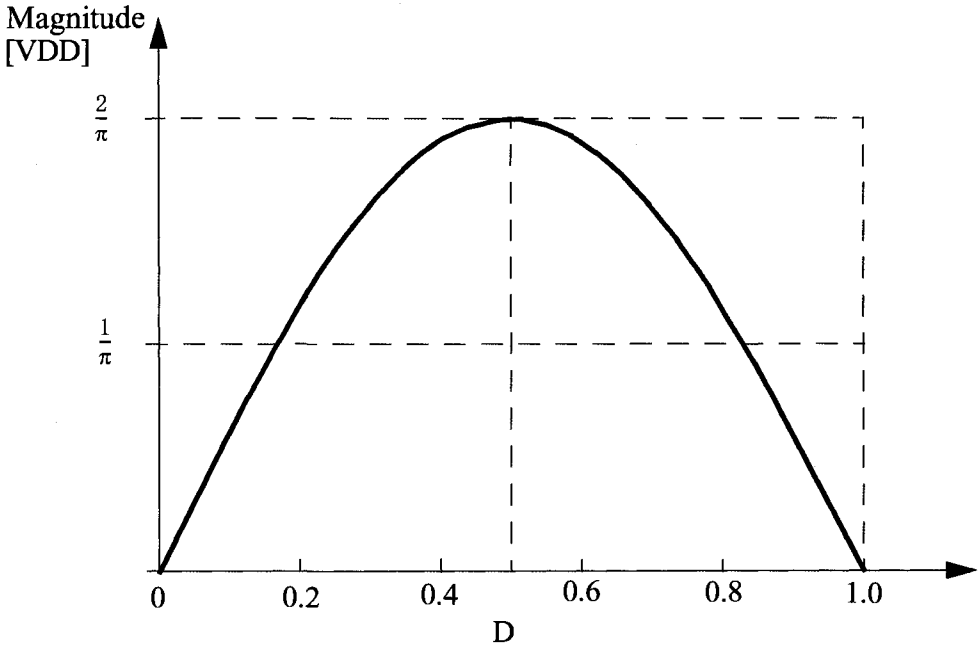


Figure 3.8 The magnitude of V_x fundamental vs. D

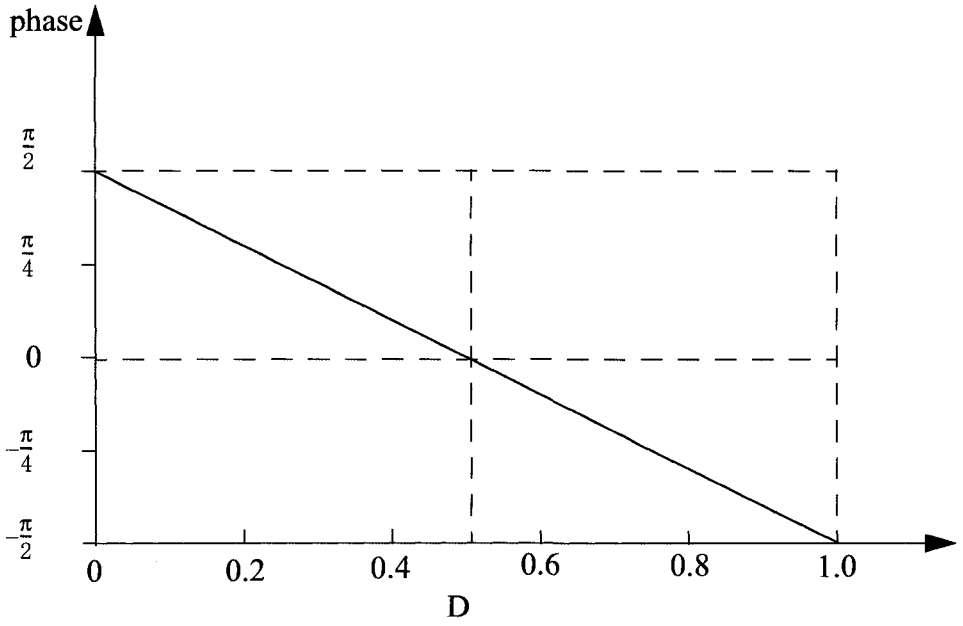


Figure 3.9 The phase of V_x fundamental vs. D

In order to obtain a flat frequency response of the low-pass filter, the damping factor is chosen to be $\sqrt{2}/2$. The residue ripple in the output is determined by the fundamental of the waveform V_x and the characteristic of the LC output low-pass filter which attenuates the switching supply waveform fundamental. When the duty cycle D is 50%, using (3-2), (3-8), (3-9) and (3-10), the switching ripple in the output is given by

$$v_{rip} = c_1\big|_{D=0.5} \times \left\| \frac{1}{1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \right\|_{\substack{Q=\sqrt{2}/2 \\ D=0.5}}$$

$$= \frac{2V_{DD}}{\pi}\frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_0}\right)^4}} \cong \frac{2V_{DD}}{\pi}\left(\frac{f_0}{f_s}\right)^2 \qquad (3\text{-}11)$$

According to (3-11), if the switching frequency f_s increases, the amplitude of the switching ripple will decrease. To increase f_s, one way is to decrease the overall modulator delay T_d, which needs a fast comparator and an optimally designed multistage buffer. Due to the high output power, the size of the transistors in the output stage is much larger

than that of a conventional logic circuit. Therefore the parasitic capacitance C_p is large. In order to achieve the optimal delay in the multistage buffer, the following equation [20] is used,

$$T_{buf} = e \ln \frac{C_p}{C_i} t_{p0} \tag{3-12}$$

where T_{buf} is the optimal delay in the multistage buffer, C_i is the input capacitance of a unity inverter and t_{p0} is the delay of the unity inverter with C_i.

The DM modulator has an advantage of keeping the residue switching ripple in the output close to a constant. Figure 3.9 suggests that the phase of the fundamental will change if the duty cycle is not 50%. Consequently, the output low-pass filter phase, the second term in (3-6), must be adjusted to compensate this change so that the oscillation condition can be maintained. This causes the oscillation condition of (3-6) to be invalid when the duty cycle is different from 50%. Figure 3.8 shows that the amplitude of the fundamental will decrease when D is higher or lower than 50%, however, the switching frequency will decrease due to the change of the oscillation condition, leading to less attenuation in the amplitude when the fundamental passes through the low-pass filter.

3.2 Wideband Rail-to-rail Input/Output Op-amp

In this design both envelope detector and envelope amplification blocks need an operational amplifier (op-amp). For the time issue, only one topology of the op-amp is designed, which can satisfy the requirements of both blocks mentioned above by changing some device parameters.

The op-amp used in the envelope detector should have a rail-to-rail input/output range and a relatively high open-loop gain at about 3 MHz, which assures a wide input range of the envelope detector and a wide enough bandwidth of the envelope to be detected. The op-amp used in the envelope amplification should have a rail-to-rail output range, a high gain and a wide bandwidth to ensure that the envelope amplification sub-

block can provide a wide input range to the fast comparator and enough gain to amplify the output signal of the envelope detector. Because the goal of the bandwidth of the modulator is to be as wide as possible, the design specification of the op-amp is: a rail-to-rail input/output, 200MHz wideband and open-loop gain larger than 90dB for the envelope amplification and larger than 50 dB at 3MHz for the envelope detector.

3.2.1 Rail-to-rail Input Stage

The input stage for most of the op-amps is a differential amplifier. Figure 3.10 gives a simple example. It is known that the maximum input common mode range for an NMOS differential pair is $VDD-V_{Dsat,Mn}-V_{GS,M12}$. A similar result can be obtained for a PMOS differential pair. This is a significant limitation, especially if the op-amp is used for a general purpose, say a unity-gain buffer.

In order to overcome the input range limitation of a single differential pair input stage, there has been much research with the focus on op-amps with linear operation regions that extend from rail-to-rail for low voltage applications. In these op-amps, an NMOS differential pair and a PMOS differential pair are connected in parallel, as shown in Figure 3.11. This technique is called complementary differential input stage. It allows the input stage to operate rail-to-rail. For this input stage, there are three operation regions. When the common mode voltage, V_{CM} ($V_{CM}= (V_{in+} + V_{in-})/2$), is near the negative power supply (or GND for single power supply), only the PMOS input pair is operational. When V_{CM} near the positive power supply VDD, only the NMOS input pair is operational. Under the third condition, when V_{CM} is around mid-rail, both NMOS and PMOS differential pairs operate. As a result, at least one of the two differential pairs will operate for any V_{CM} between both power supply rails.

Although the complementary differential input stage provides the rail-to-rail input range, as a single-stage op-amp, it has two major drawbacks. The first one is that the voltage gain is limited with a typical value of 50 [21]. The second one is that the output volt-

age swing is limited to the range, $V_{CM} - V_{th} \leq V_{out} \leq VDD - V_{Dsat4}$ (derived from Figure 3.10). In order to achieve a high gain, the cascode scheme could be the first choice. The cascode scheme has two main forms, one is the telescopic cascode, the other is the folded cascode. In order to increase the swing range of the output voltage and drive ability, a Class AB output buffer is used. All these circuits are discussed in the following sections.

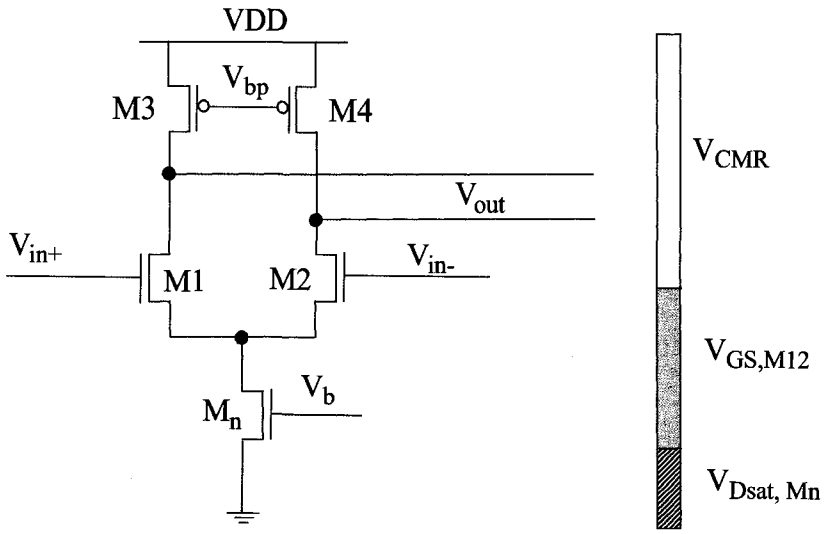


Figure 3.10 A simple differential input stage

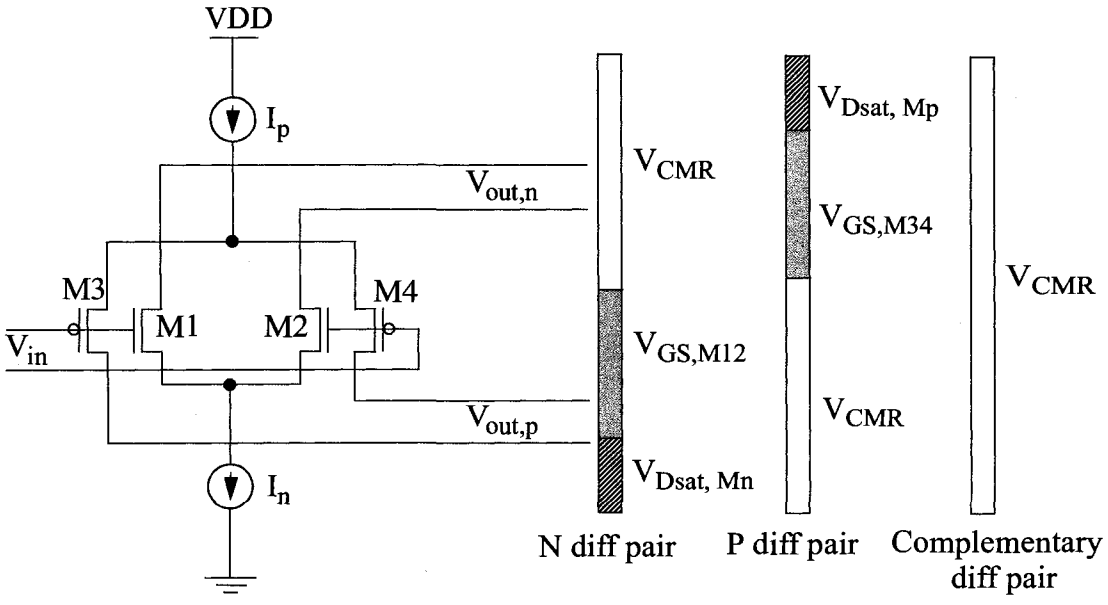


Figure 3.11 Rail-to-rail complementary differential input stage

3.2.2 Telescopic Cascode Op-amp

The telescopic cascode op-amp [22] is shown in Figure 3.12. In Figure 3.12 (a) and (b), M1, M3 and M2, M4 form two cascode amplifiers, while M5, M7 and M6, M8 form a cascode current source acting as an active load. Then the output impedance is given by,

$$r_o = g_{m4}(r_{o4}r_{o2}) \,\|\, g_{m6}(r_{o6}r_{o8}) \tag{3-13}$$

Normally $g_{m4}r_{o4}$ and $g_{m6}r_{o6}$ are much larger than 1, so the output impedance of a telescopic cascode op-amp r_o is much larger than $r_{o2}\|r_{o4}$ which is the output impedance of the simple differential input stage shown in Figure 3.10. As a result, the gain of telescopic op-amp increases substantially.

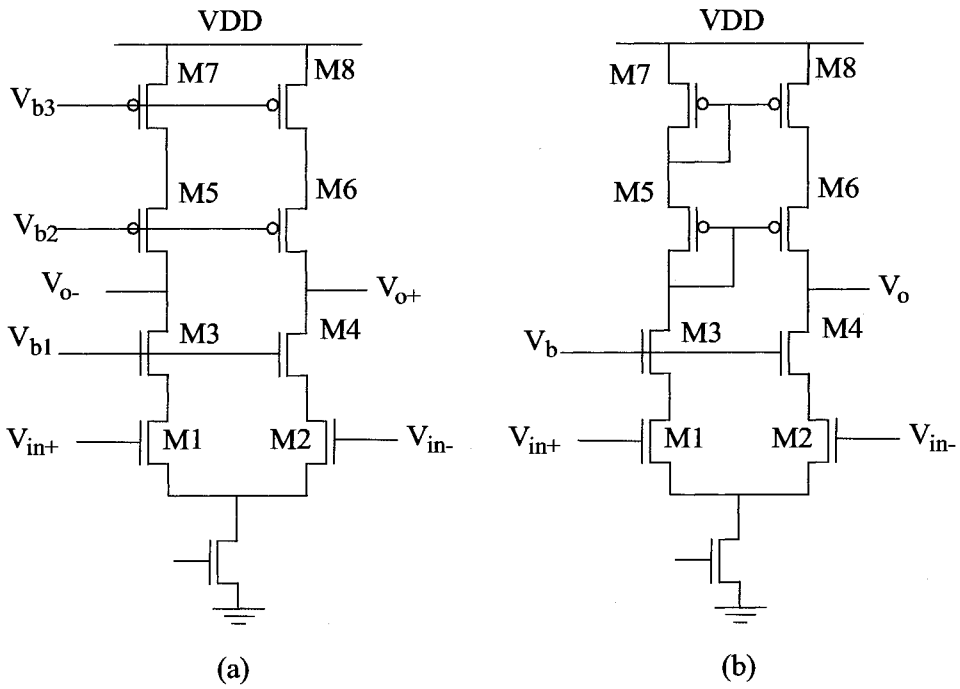


Figure 3.12 Telescopic op-amp (a) with differential output (b) with single-ended output

For a telescopic cascode op-amp, both the gain bandwidth product (GBW) and the lowest non-dominant pole are determined by NMOS devices, resulting in both wide band-

width and good phase margin. The power consumption is small because it has only one current source leg.

The most prominent drawback of this architecture is the limited voltage swing both at the output and the input of the op-amp. From the high side the output swing is limited to $2V_{Dsat}$ below VDD and from the low side a minimum of $3V_{Dsat}$ above GND (or VSS for two voltage supplies). With this maximum possible output swing, the input common mode range is zero [22]. In practice a telescopic cascode is only used in the case of a high supply voltage. When the supply voltage gets low, the swing is too small for most applications.

3.2.3 Folded Cascode Op-amp

The folded cascode op-amp [23] shown in Figure 3.13 is a widely used op-amp architecture. It provides a larger output swing and input CM range than the telescopic op-amp with the same DC gain. The output swing, $VDD\text{-}4V_{Dsat}$, is not affected by the input CM range, which is $VDD\text{-}V_{th}\text{-}2V_{Dsat}$ (obtained by using $V_{GS}=V_{th}+V_{Dsat}$).

The input pair can be both the NMOS and PMOS transistors. The NMOS input architecture shown in Figure 3.13 offers high unity gain frequency ($g_{m1}/2\pi C_L$) [19] due to the NMOS input transistors. The lower nondominant pole (g_{m7}/C_1) associated with the node n1 is determined by the low PMOS transconductance and the large stray capacitances of the PMOS current sources and the cascode devices. Utilizing a PMOS input pair causes lower GBW, but the non-dominant pole is higher, due to the NMOS cascode devices.

Feedforward capacitors can be used to bypass the cascode transistors at high frequencies to improve the phase margin [24][25]. In principle, the technique produces a zero, which is used to cancel the pole associated with the cascode node. It is, however, not

possible to place this zero exactly on top of the pole. Thus, there is a sufficiently closely spaced pole-zero pair which is known to introduce a slowly settling component in the step response [26]. Consequently, feedforward techniques should be used with caution in op-amps.

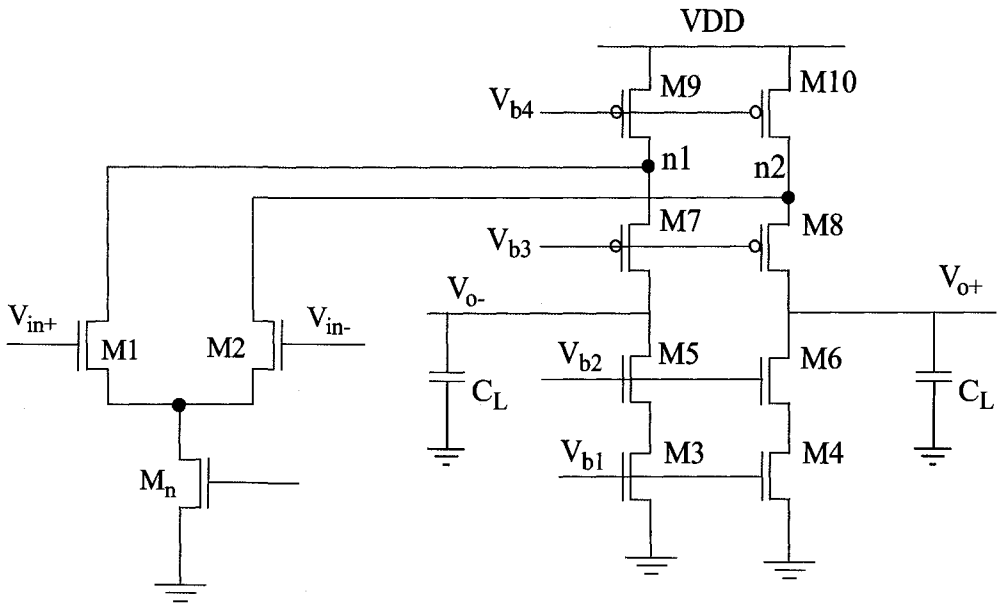


Figure 3.13 Folded cascode op-amp

It is possible to employ the complementary differential pair input stage, which increases the slew rate (with the same total current consumption) [27], but at the same time the input capacitance increases and the nondominant pole becomes lower.

3.2.4 Two-stage Op-amp

From the above analysis, one can see that the rail-to-rail input range and high open-loop gain can be realized by a folded cascode op-am with a complementary differential input pair, but a folded cascode op-amp does not provide rail-to-rail output, so to meet this requirement, a rail-to-rail output stage is needed, which means a two-stage op-amp should be used. In the followings, the two-stage op-amp design issues are discussed.

3.2.4.1 Positioning the Second (Non-dominant) Pole

Although a high gain can be acheived by cascading two gain stages, each gain stage will add a low frequency pole. In this case, sufficient phase margin becomes a challenging design constraint.

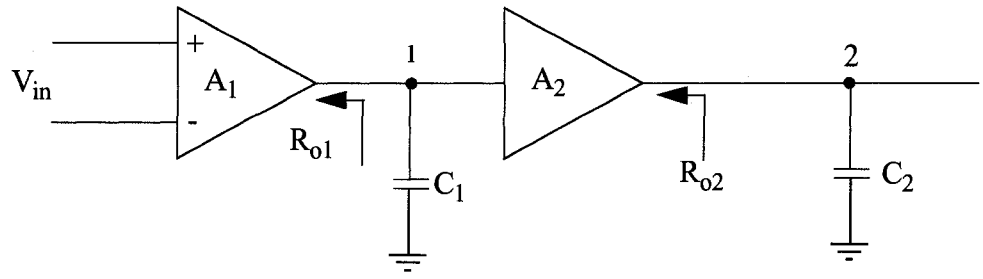


Figure 3.14 Block diagram of a two-stage op-amp

The basic block diagram of a two-stage op-amp is shown in Figure 3.14. The transfer function of the two-stage op-amp is given by

$$A(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{A_1}{1 + sR_{o1}C_1} \cdot \frac{A_2}{1 + sR_{o2}C_2} \tag{3-14}$$

where R_{o1} and R_{o2} are the output impedance of the first and second stage respectively, C_1 and C_2 are the total capacitance at node 1 and 2 respectively, A_1 and A_2 are the DC gain of each stage. Equation (3-14) has two poles, $s_1 = -1/(R_{o1}C_1)$ and $s_2 = -1/(R_{o2}C_2)$. If both stages have high gains, namely high output impedance, both s_1 and s_2 are close to $j\omega$ axis in s plane, then both s_1 and s_2 are dominant poles. Therefore the bandwidth of the two-stage op-amp is limited. If the first stage has a high gain and the second stage has a moderate gain (this is a typical case for a two-stage op-amp), this means R_{o2} has a moderate value. Then s_1 is the dominant pole, the role of s_2 depends on the load capacitance. However, the load capacitance can be very large, so s_2 still is a dominant pole. If a two-

stage op-amp has two dominant poles, the phase margin becomes much smaller, which means the op-amp is instable. In order to overcome this drawback, the miller compensation technique is applied.

The Miller compensation technique is shown in Figure 3.15, where C_M is the Miller capacitor. The main idea of Miller compensation is shown in Figure 3.16. With Miller compensation, the dominant pole s_1 will move close to the origin and the output pole s_2 will move away from the origin. As a result, the bandwidth of the system increases dramatically at the expense of adding only a small capacitor C_M.

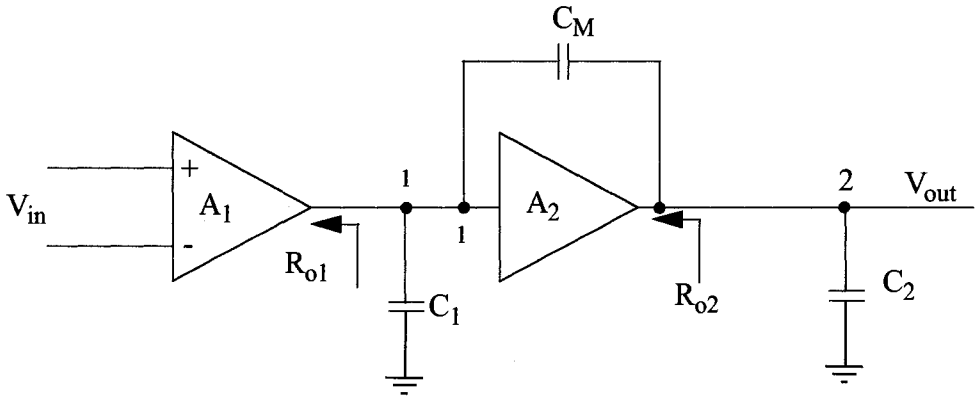


Figure 3.15 Block diagram of a two-stage operational amplifier with Miller compensation

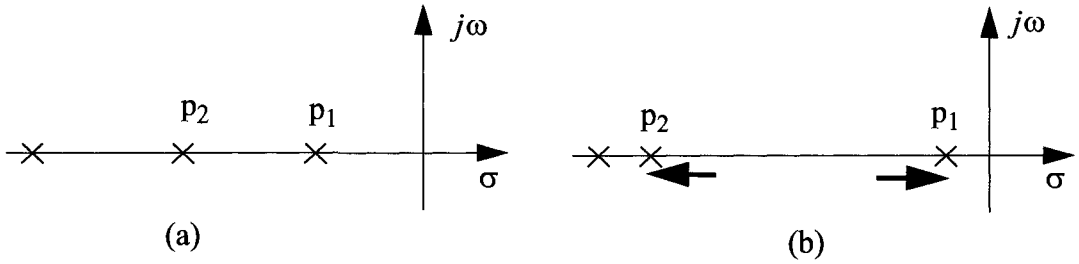


Figure 3.16 Pole splitting of Miller compensation (a) before compensation (b) after compensation

According to the Miller effect, the equivalent capacitance at node 1 is $C_1 + (1 + A_2(s))C_M$, so the dominant pole moves towards the origin to $1/(R_{o1}(C_1 + (1 + A_2(s))C_M))$. And the open loop gain of the two-stage op-amp with a Miller capacitor is given by

$$A(s) = A_1(s)A_2(s) \cong \frac{A_1}{1 + sR_{o1}(C_1 + (1 + A_2(s))C_M)} \cdot A_2(s) \tag{3-15}$$

If $A_2(s) \gg 1$ and $sR_{o1}A_2(s)C_M > 1$, then (3-15) can be simplified as

$$A(s) \cong \frac{A_1}{sR_{o1}A_2(s)C_M} \cdot A_2(s) = \frac{A_1}{sR_{o1}C_M} \tag{3-16}$$

From (3-16) one can see that the pole at the second stage output does not appear in the overall system. Hence the pole at the second stage output does not cause a pole in the overall system.

Additionally, if $A_2(s)>1$ and the second stage unity gain frequency is well above the crossover of the system, then the gain of the second stage will not affect the crossover of the system. For example, an increase in A_2 will cause an increase in both the DC gain of the amplifier and the effective value of Miller capacitor, as a result, the crossover frequency will not be affected.

If $A_2(s)<1$ equation (3-10) reduces to

$$A(s) = A_1(s)A_2(s) \cong \frac{A_1}{sR_{o1}(C_1 + C_M)} \cdot A_2(s) \tag{3-17}$$

and thus both the poles of the first stage and the second stage are present in the overall transfer function. $A_2(s)=1$ corresponds to the position of the second pole. Therefore a design strategy of making the unity gain frequency of the second stage to be equal to the allowed position of the second pole can be adopted.

The equivalent capacitance at node 1 also explains that the best condition of Miller compensation is that the second stage provides a medium gain. If the gain of the second

stage is too large, then the equivalent capacitance $C_1 + (1 + A_2(s))C_M$ becomes very large, this will slew the first stage. If the gain is too small the Miller effect could be ignored.

Although the Miller capacitor increases the system bandwidth, it also introduces a right plane zero which worsens the phase margin. So to cautiously position the zero is very important in the design of a Miller two-stage op-amp.

3.2.4.2 Feed Forward Zero

With any capacitor which connects the output with the input of an amplification stage, there is an alternative path for the signal from input to output of the stage. This means that there is potentially a zero in the system transfer function. As an example [28], a common source amplifier with a Miller capacitor is shown in Figure 3.17, where R_S is the output impedance of the previous stage, C_M includes the capacitance of C_{GD}, C_{DB} equals to all the capacitance at output node, and C_{GS} includes all the capacitance at node 1. According to Figure 3.17(b), the transfer function of the circuit is given by,

$$\frac{V_o(s)}{V_{in}(s)} = \frac{(sC_M - g_{m1})R}{1 + \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right)s + \frac{s^2}{\omega_{p1}\omega_{p2}}}$$

where $\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}} = R_S(1 + g_m R)C_M + R_S C_{GS} + R(C_M + C_{DB})$,

$$\frac{1}{\omega_{p1}\omega_{p2}} = RR_S(C_{GS}C_M + C_M C_{DB} + C_{DB}C_{GS}).$$

Obviously, the common source stage is an inverting stage, so the feedforward path through C_M introduces a zero in the right half plane (RHP). This contributes a factor $(1 - s/\omega_z)$ to the numerator of the transfer function of the system, which means that the phase margin decreases by $\mathtt{atan}(\omega/\omega_z)$. When the Miller gain stage is made up of a sin-

gle stage, the position of the zero can be approximated as $\omega_z = g_m/C_M$, where g_m is the transconductance of the miller stage. In this example it is g_{m1}.

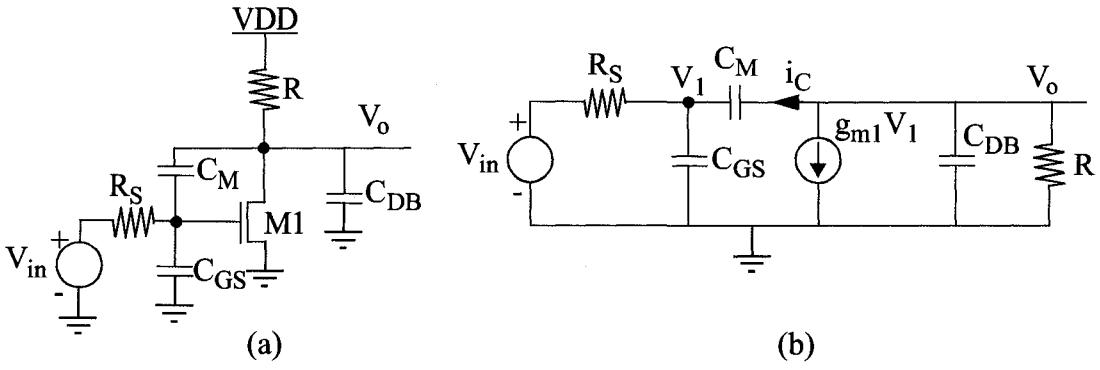


Figure 3.17 Common source amplifier (a) schematic (b) small signal model

The reason of causing the RHP zero can be explained by the currents flowing through C_M and the gain stage g_m related to V_1 in Figure 3.17(b) [29]. The current flowing through C_M, $i_C = sC_M(V_o(s)-V_1(s))$, has a feedforward component $sC_MV_1(s)$ and a feedback component $sC_MV_o(s)$. The current flowing through the gain stage is $g_{m1}V_1$. The total current related V_1 at the output node is given by

$$i_{V_1} = (g_{m1} - sC_M)V_1(s) \tag{3-18}$$

Thus, a zero is in the transfer function where i_{V_1} is zero, at $\omega_z = g_{m1}/C_M$.

For a two-stage op-amp, the zero and the poles typically have the relation as $|\omega_{p1}| < |\omega_z| < |\omega_{p2}|$ [28], which means that the zero typically can cause serious degeneration of the phase margin. To overcome the effect of the RHP zero, three techniques have been proposed based on controlling the feedforward current.

The first one is to put a source follower in series with Miller capacitor [29], thus the feedforward current is blocked and the zero is eliminated. The main disadvantages are that the source follower needs extra devices and bias current and a nonzero dc voltage exists between the input and the output of the source follower, which affects the output

voltage swing. The second technique is to use a common gate transistor to block the feed-forward current from flowing through the compensation capacitor [29]. The disadvantages remain to be the demand of extra devices, bias current and potential mismatch problem.

The third way is to insert a resistor in series with the compensation capacitor. This way neither directly blocks the feedforward current nor eliminates the zero. The resistor modifies the feedforward current and moves the zero far away form the second poles. As a result, the effect of the RHP zero is eliminated. The position of the zero is given by

$$\omega_z = \frac{1}{(1/g_m - R_c)C_M} \tag{3-19}$$

where R_c is the compensation in series resistor. Equation (3-19) implies that when $1/g_m = R_c$, the zero will be moved to infinity.

3.2.5 Rail-to-rail Output Class-AB Buffer

In this op-amp design, the output stage should satisfy the following three requirements. The first one is to have a rail-to-rail output voltage swing. The second one is to be able to drive a relatively large load capacitance and/or a small resistance with an acceptably low level distortion. The third one is that it should have a high power efficiency, which means low quiescent current.

The rail-to-rail output voltage swing can be realized by a push-pull stage which consists of two complementary common source transistors [21]. High efficiency means the high ratio of the maximum current that can be delivered to the load to the quiescent current of the output stage. A Class-B amplifier can exactly satisfy this requirement. Because the active device in the amplifier is biased at threshold voltage, there is almost no quiescent current flowing through the active device. However, the drawback of a Class-B amplifier used as a rail-to-rail output stage is the large crossover distortion [29]. A Class-A amplifier can provide the highest linearity, namely the lowest distortion, but at the expense of efficiency. Because in Class-A operation, the quiescent current is equal to or

larger than the maximum output current. As a trade-off between the output signal distortion and quiescent current, a Class-AB amplifier can provide relatively low distortion and relatively high efficiency. These features make Class-AB to be widely used as an output stage in op-amp design.

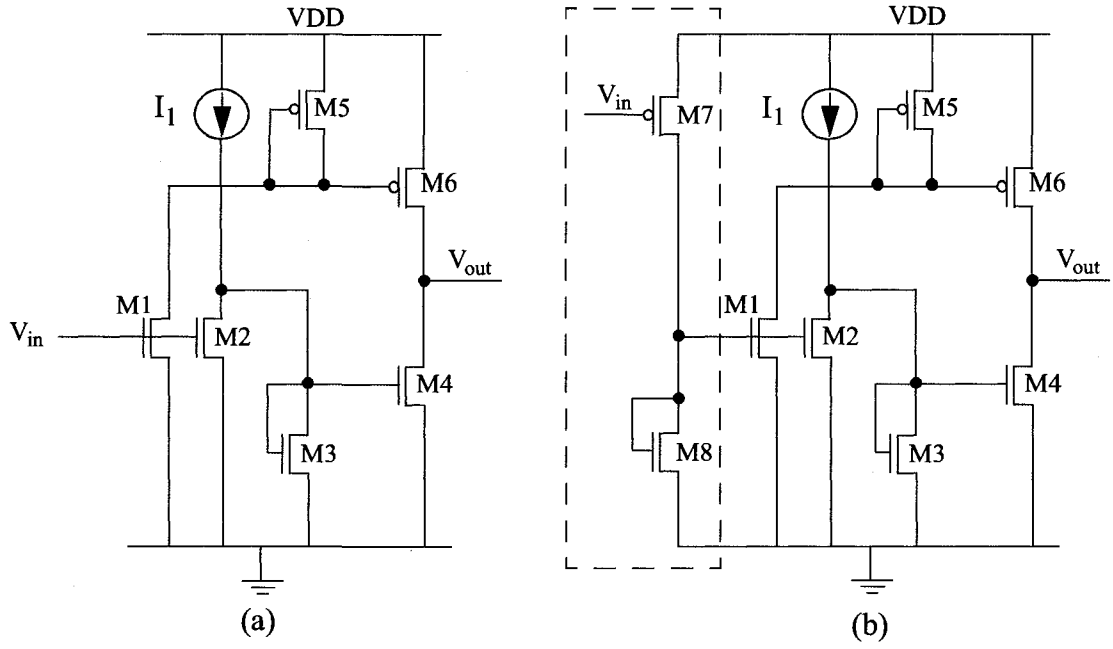


Figure 3.18 Class AB output stage (a) without inverting stage (b) with inverting stage

Figure 3.18(a) shows a Class-AB output stage [30]. The operation principle is: Transistors M1 and M2 have the same size with the same gate connection, hence they have the same current, $I_{D1} = I_{D2}$. When the gate voltage of M1 increases, I_{D1} increases, which will cause an increase in the output PMOS current, I_{D6}, which will cause the output voltage to rise. Additionally, the same increase in input voltage will cause current I_{D2} to increase. As I_1 is fixed, the current in M3 will decrease, as $I_1 = I_{D2} + I_{D3}$, and hence the output NMOS current I_{D4} will decrease. This will also cause the output to rise. In a reverse

way, when the input goes down, the output goes down. The output can source or sink current much greater than the value of quiescent current, resulting in better power performance for the same slew rate than a Class-A amplifier. (A Class-A amplifier can only provide current greater than the quiescent current in one direction.) This is important as a large capacitor is driven. However, this circuit does have a slew limit in the negative direction. The maximum current that the transistor M4 can sink equals to $I_{D3}(W_4/W_3)$, where W_4 and W_3 are the width of transistors M4 and M3 respectively. The slew limit in the negative direction can be overcomed by increasing the width of M4.

As discussed already, due to the limited output swing of the first cascode stage, a high gain can be achieved by the first stage, making the overall gain specifications relatively easy to be achieved with only two stages. The Miller capacitor that will be used requires an inverting stage across it. However, from the above analysis of the Class-AB output stage in Figure 3.18(a), one can see that this stage is non-inverting, this means an additional stage needs to be added to invert the signal. This stage will require a wide bandwidth, since it is part of the Miller stage, which needs to have a unity gain frequency well above the crossover of the overall amplifier. This stage should also have a low gain, because its gain will contribute to A_2, which may already have enough gain to meet the moderate gain condition for a Miller stage. For this reason, a common source PMOS input with a diode connected NMOS load was chosen. As shown in Figure 3.18(b) (in the dash box), the PMOS transistor is M7 and the NMOS transistor is M8.

3.2.6 Summary of the Op-amp

From section 3.2.1 to 3.2.5, the single-stage and two-stage op-amps are discussed. Considering the input and output voltage swing range, a two-stage op-amp is used in this design. For the input stage, in order to obtain the rail-to-rail input voltage range, the application of the complementary differential input stage is necessary. As discussed in the last section, the overall gain specifications can be relatively easily achieved with a two-stage

op-amp. This is because a single cascode stage, whether a telescopic or folded one, can achieve a fairly high gain. Although this decreases the output voltage swing, the output voltage swing range is not a requirement for the first stage of a two-stage op-amp. Because this circuit is implemented by 0.18 μm CMOS technology which has a typical supply voltage of 1.8 V. A folded cascode stage is used in this design. This assures that the circuit still can work normally even when the supply voltage decreases to a certain low level. The rail-to-rail output voltage swing can be obtained by the second stage, the Class-AB output stage with an inverting stage. The second stage also contributes a moderate gain to the overall specification. To achieve the bandwidth specification, the Miller compensation technique is used. A Miller capacitor in series with a resistor is connected from the input to the output of the second stage. The serial resistor is used to position RHP the zero introduced by the feedforward path of Miller capacitor, and thus it can eliminate the effect of the RHP zero. The schematic of the two-stage op-amp with Miller compensation is shown in Figure 3.19.

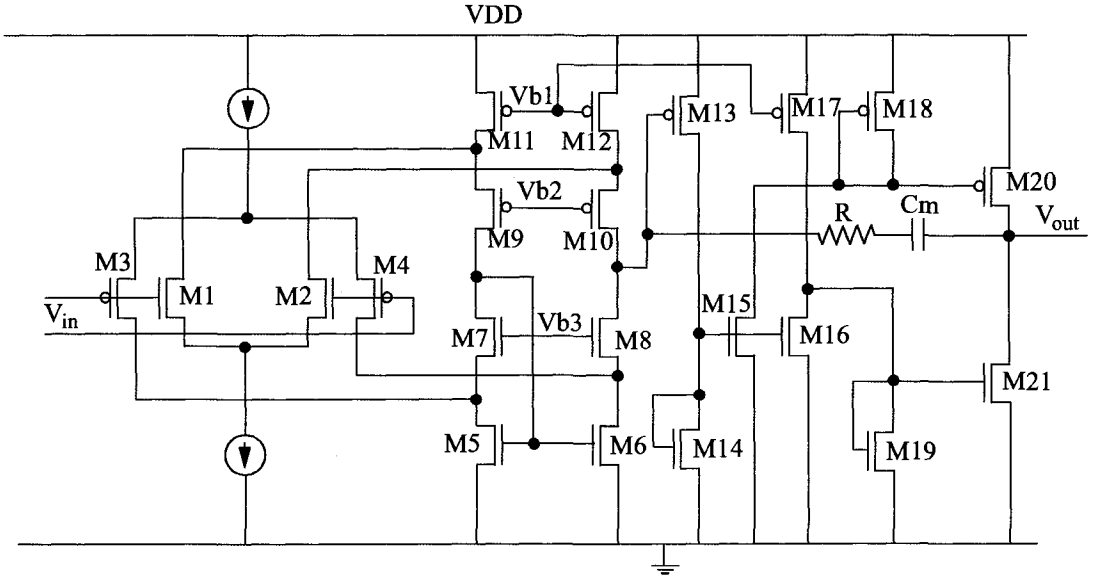


Figure 3.19 Schematic of a two-stage op-amp with Miller compensation

As mentioned above, the op-amps in the envelope amplification and the envelope detector circuits will use the same topology. This can be realized by changing the position of the dominant pole. In order to keep the overall bandwidth unaffected, the simplest way is to change the output impedance of the first stage, which means to change the sizes of transistors M7, M8, M9 and M10.

3.3 Fast Comparator

Comparators are necessary components in the control loop of a DC-DC converter. Usually comparators are categorized into open-loop and regenerative comparators [31]. Essentially an open-loop comparator can be viewed as an op-amp operating in the open-loop configuration. The main difference between an open-loop comparator and an op-amp is that a comparator does not need frequency compensation for stable operation over frequency, whereas an op-amp normally needs.

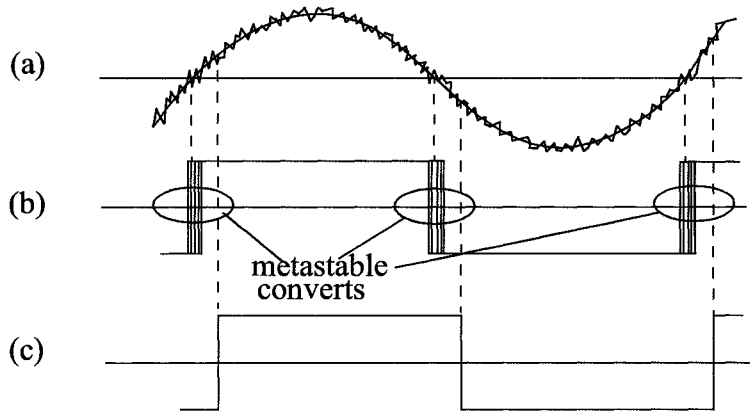


Figure 3.20 Metastable state of a comparator in a noisy environment (a) noisy input (b) metastable output without hysteresis (c) stable output with hysteresis

A regenerative comparator is normally used with a slowly varying signal, or in a noisy environment, which will result in a metastable state of the output. Figure 3.20 shows

the metastable or unknown state caused by the noisy input. A regenerative comparator employs positive feedback to modify the comparator threshold reference voltage. The amount of deviation from the unmodified reference is called hysteresis voltage, which is used to eliminate the metastable state effect that is caused by the noise of the input signal.

3.3.1 Propagation Delay Time

As discussed already, in this design, a fast comparator is very important, since it can increase the switching frequency of the modulator, which directly leads to a smaller output switching ripple and a wider modulator bandwidth. Here "fast" means the response time of the comparator is small. The definition of the response time or propagation delay is the delay between the time when the differential input passes the comparator threshold voltage and the time when the output exceeds the input logic level of the subsequent stage [21].

When a comparator is modeled as an open-loop op-amp with a finite gain and a single (dominant) pole, the propagation delay is given by Allen [31],

$$t_p = \tau_c \ln\left(\frac{2k}{2k-1}\right) \tag{3-20}$$

where $k = V_{in}/V_{in,min}$, $V_{in,min}$ is the minimum change of voltage to the comparator. It equals to the resolution of the comparator, $\tau_c = 1/\omega_c$, where ω_c is the -3dB frequency of the single pole approximation to the comparator frequency response. The plot of t_p/τ_c vs. k is shown in Figure 3.21. In a specific circuit, τ_c is constant, so according to Figure 3.21, the propagation delay t_p decreases when k increases. This means that when $V_{in,min}$ is constant, increasing the amplitude of V_{in} will decrease t_p. When V_{in} is constant, decreasing $V_{in,min}$ will decrease t_p.

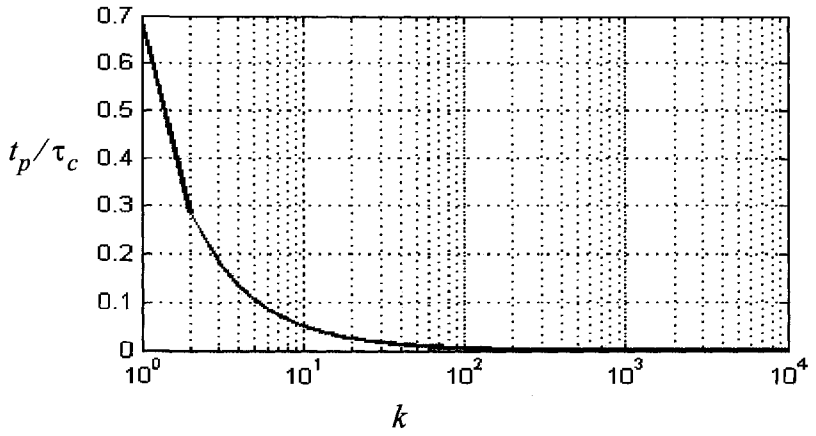


Figure 3.21 t_p/τ_c Vs. k

In the comparator design [31], the combination of the open-loop and the regenerative comparators results in a comparator with a very low propagation time delay. Baker [19] reaches the similar conclusion that the propagation delay of a single high gain stage is generally larger than that of several cascaded low-gain stages. This can be roughly explained by the time constant at the output pole of the comparator, which is τ_{c1} in (3-21). A single high gain stage comparator normally uses cascode topology (for example, Figure 3.12), so using (3-13) the time constant is given by

$$\tau_{c1} = R_o C_o = (g_{m4}(r_{o4}r_{o2}) \parallel g_{m6}(r_{o6}r_{o8}))C_o \approx \frac{1}{2} g_m r_o^2 C_o \qquad (3\text{-}21)$$

where R_o is the resistance at the output node, C_o is the capacitance at the output node, r_o is the approximation of the drain source resistance of each transistor.

In the case of n cascaded low-gain stages, each stage can use the topology shown in Figure 3.10. In this case the time constant can roughly be given by

$$\tau_{c2} = n(R_o C_o) = n(r_{o2} \parallel r_{o4})C_o \approx \frac{1}{2} n r_o C_o \qquad (3\text{-}22)$$

When equation (3-21) is divided by (3-22), the result is $\tau_{c1}/\tau_{c2} = (g_m r_o)/n$, where the typical value of n in (3-22) may not be larger than 10 while $g_m r_o$ can be the order of several tens or higher, so normally $\tau_{c1} > \tau_{c2}$. Although this analysis is not very

strict, the result is a correct estimation and can provide guidance for the comparator design.

3.3.2 Three-cascaded-stage Comparator

Based on the above analysis of propagation time delay in a comparator, in this design a three-cascaded-stage topology is used. The basic block diagram is shown in Figure 3.22. The first stage is a preamplification one. In essence, it is a simple op-amp and is used to increase the minimum input signal, namely the comparator sensitivity. Another function of the preamplification stage is to isolate the input of the comparator from kick-back noise coming from the decision-making stage which has a positive feedback. The second stage is the decision-making stage, which, as its name indicates, makes a decision on whether the input voltage is larger or smaller than the reference voltage. A positive feedback assures this stage to achieve a high gain. The last stage is the postamplification stage which amplifies the decision signal from the second stage and converts the output to a digital signal.

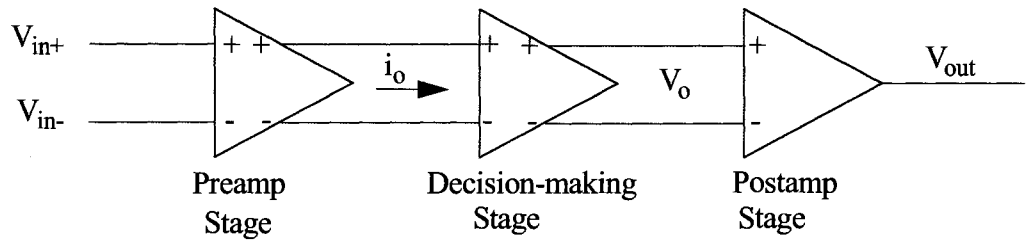


Figure 3.22 Block diagram of a high performance comparator

As described by Allen in [31], the preamplifier has a time domain response with a negative argument of the exponential while the positive feedback stage (the latch) has a time domain response with a positive argument of the exponential (shown in Figure 3.23). The preamplification stage amplifies the input signal to a certain voltage level V_X by taking the propagation delay of t_1. The decision-making stage (the latch) then amplifies V_X to the digital form output by taking t_2. This configuration combines the advantageous aspect

of each stage to achieve a smaller propagation delay $t_1 + t_2$. Obviously, if the comparator consists only of several stages of preamplifier or latches, the propagation delay will be longer than $t_1 + t_2$.

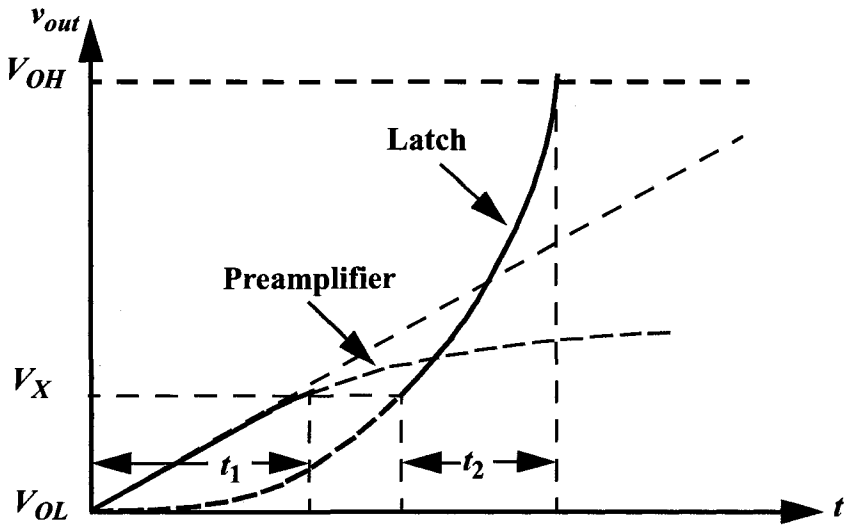


Figure 3.23 Preamplifier and latch step response [31]

3.3.2.1 Preamplification Stage

Because this stage is essentially a simple op-amp, a simple differential pair with diode connected transistors load is used. The schematic is shown in Figure 3. 24. The size of transistor M1 and M2 is very important, because it directly affects the transconductance and the input capacitance. These two factors have opposite effects on the propagation delay. For example, the increase of the width of these two transistors results in the increase of the transconductance, consequently the sensitivity of the comparator will increase and the propagation delay will decrease. However, the increase of the width of these two transistors will increase the input capacitance, therefore the propagation delay will increase.

The gain of this stage can be modified by the transistors of M5 and M6 as well, because M5 and M6 will sink current in proportion to the width of M3 and M4 respectively.

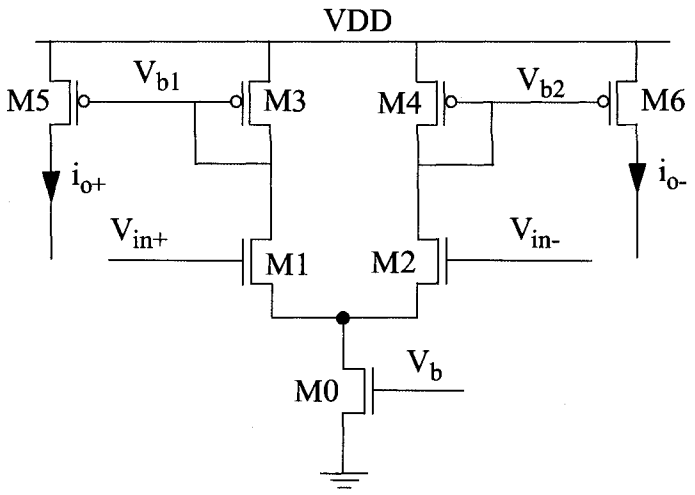


Figure 3.24 Preamplification stage

3.3.2.2 Decision-making Stage

This stage realizes the comparison function by determining whether the input voltage is higher or lower than the reference voltage and outputs digital form signal. Therefore the gain should be large to assure the digital form output. In order to assure the circuit to be robust enough to work in a certain noisy environment or overcome the noise on the input signal, the circuit should have some hysteresis. The schematic of this stage is a dynamic latch shown in Figure 3.25, which was first presented in [32]. The cross-coupled transistors M7 and M8 provide positive feedback to increase the gain of this stage. Transistors M9 and M10 are used to make sure that this stage has a gain boost but to avoid entering latch-up. The gain of the first two stages is given by,

$$A = \frac{g_{m12} \cdot a}{g_{m910}} \cdot \frac{1}{1 - g_{m78}/g_{m910}} \tag{3-23}$$

where $a = \frac{I_{D56}}{I_{D34}} = \frac{(W/L)_{56}}{(W/L)_{34}} = \frac{W_{56}}{W_{34}}$, the lengths of transistors M3 to M6 are the same. For the decision-making stage, when g_{m78}/g_{m910} is larger than 1, the overall feedback is positive and hysteresis occurs.

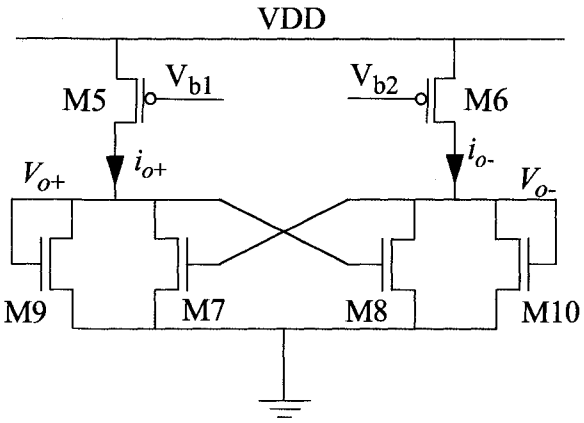


Figure 3.25 Decision-making stage

The hysteresis is analyzed as following. In Figure 3.25, M7 and M8 have the same size, and M9 and M10 have the same size. At the beginning, the current i_{o+} is assumed to be much larger than i_{o-}, therefore M8 and M9 are on while M7 and M10 are off. With i_{o+} increasing and i_{o-} decreasing, V_{o+} decreases and V_{o-} increases. When V_{o-} increases to the threshold voltage of M7, M7 turns on and begins to sink current from i_{o+}. This makes the current flowing M9 decrease, and then V_{o+} decreases, causing M8 to turn off. Obviously the switching occurs at this point, and i_{o-} and i_{o+} meet the following equations respectively,

$$i_{o-} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_8 (v_{o+} - V_{thn})^2 \tag{3-24}$$

$$i_{o+} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_9 (v_{o+} - V_{thn})^2 \tag{3-25}$$

Using (3-24) and (3-25), i_{o-} can be expressed as,

$$i_{o-} = \frac{(W/L)_8}{(W/L)_9} \cdot i_{o+} \tag{3-26}$$

Similarly, when i_{o+} increases and i_{o-} decreases, at the switching point, the following equation can be obtained,

$$i_{o+} = \frac{(W/L)_7}{(W/L)_{10}} \cdot i_{o-} \tag{3-27}$$

Considering the first and second stage together, the following equation is obtained,

$$i_{o+} = \left(\frac{g_{m12}}{2}(V_{in+} - V_{in-}) + \frac{I_{D0}}{2}\right) \cdot a = a \cdot I_{D0} - i_{o-} \tag{3-28}$$

Using (3-26), (3-27) and (3-28), the hysteresis V_H can be obtained,

$$V_H = V_{in+} - V_{in-} = \frac{I_{D0}}{g_{m12} \cdot a} \cdot \frac{\alpha - 1}{\alpha + 1} \qquad \text{for } \alpha > 1 \tag{3-29}$$

where $\alpha = \frac{(W/L)_8}{(W/L)_9} = \frac{(W/L)_7}{(W/L)_{10}}$.

3.3.2.3 Output Stage

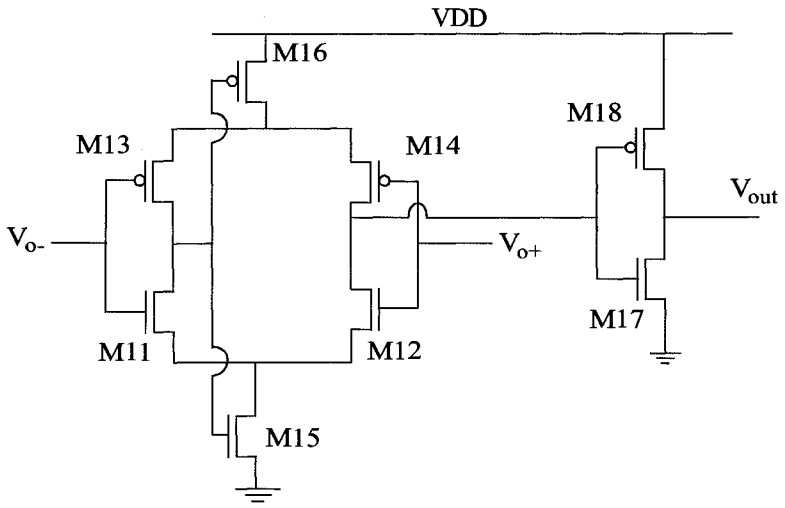


Figure 3.26 Output stage

The output stage is used for converting the output voltage coming from the decision-making circuit to a rail-to-rail digital wave. A self-biased differential amplifier [19] has been used (shown in Figure 3.26). This circuit is able to source and sink much larger currents than the quiescent bias current and it also has low sensitivity to biasing variations. In order to further increase the gain, an inverter is added on the output of the amplifier. This inverter can also isolate load capacitance from the amplifier.

3.3.2.4 Complete Hysteresis Comparator

The final short propagation delay three-stage comparator with hysteresis is shown in Figure 3.27. Since the common-mode level of the second stage does not match that of the output stage, a level shifter, a diode connected transistor, is used to solve this issue.

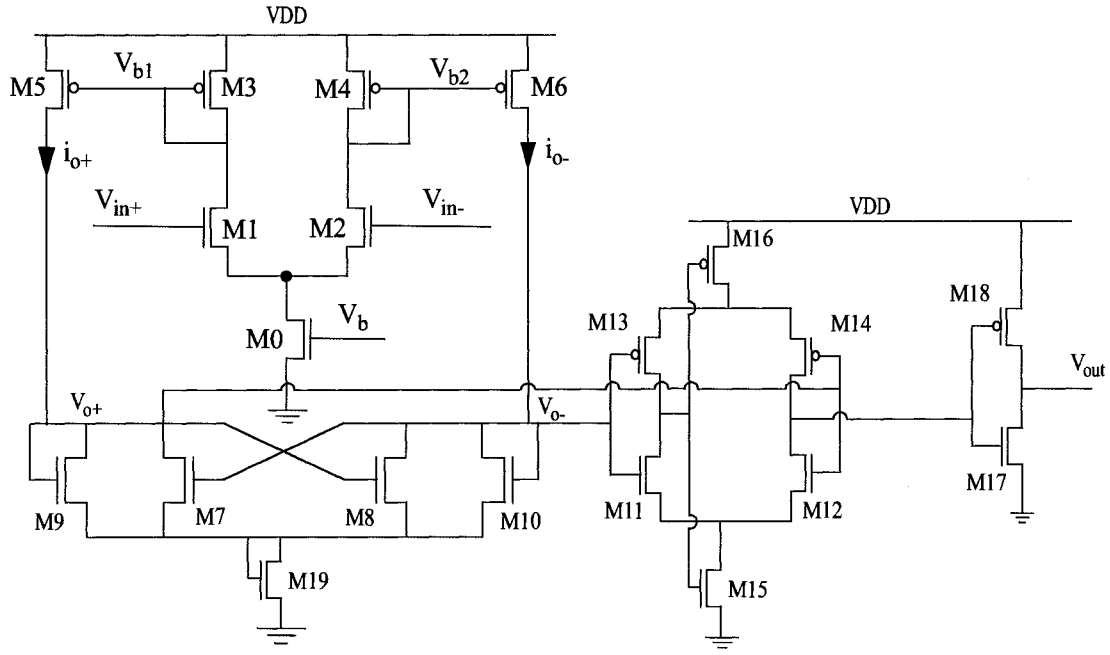


Figure 3.27 Hysterestis comparator with NMOS input stage

3.3.3 Rail-to-rail Input Comparator

As discussed already, the output V_o of the modulator is a replica of the reference signal V_{ref} shown in Figure 3.6, so the modulator output swing is determined by the input range of the comparator. To realize a rail-to-rail output swing, the input range must be rail-to-rail.

The comparator discussed in section 3.3.2 has only one NMOS differential pair as the input stage, from the discussion in section 3.2.1, one can see that its input common mode range is limited. To increase the input range to rail-to-rail, the input stage must be a combination of both NMOS and PMOS input stages. The proposed comparator is shown in Figure 3.28.

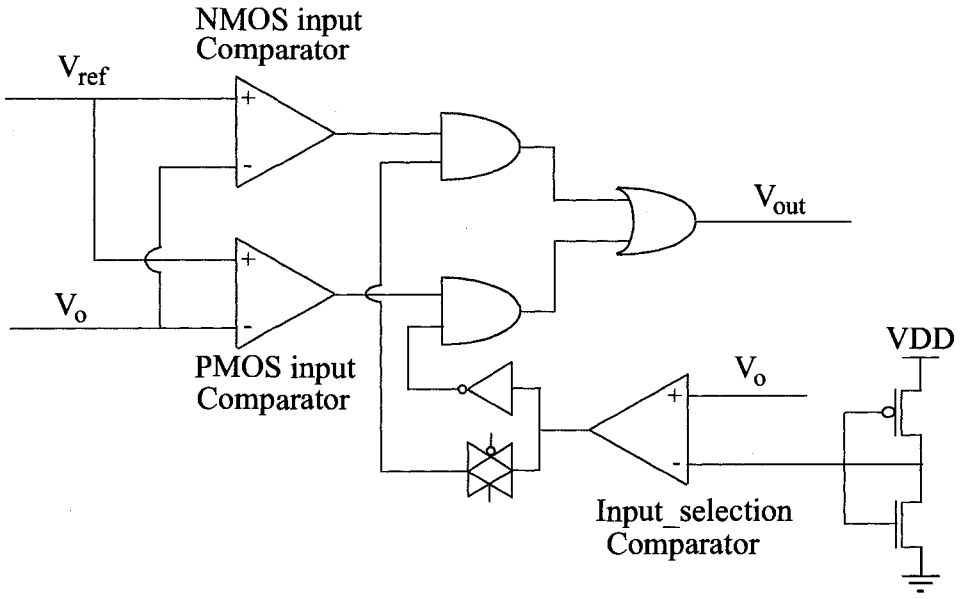


Figure 3.28 Rail-to-rail input comparator

In the rail-to-rail comparator, the NMOS input comparator uses the architecture discussed in section 3.3.2. The PMOS comparator uses the same architecture as the NMOS counterpart does, but the transistor types (n-channel or p-channel) in the input and decision-making stages are changed to be suitable for PMOS input stage and its schematic is shown in Appendix A. As discussed in section 3.2.1, when the common mode voltage

V_{CM} is near the negative power supply (or GND for single power supply), only the PMOS comparator is operational. When V_{CM} is near the positive power supply VDD, only the NMOS comparator is operational. And with V_{CM} around mid-rail, both NMOS and PMOS comparators operate. The comparators' outputs are fed to two AND gates respectively. The AND gates operate as switches to assure that each time only one comparator output is delivered to the output stage of the modulator. As a result, the modulator output avoids the error introduced by the mismatch of the two comparators' outputs. The control signals of the two AND gates are produced by the input_selection comparator which compares the modulator output voltage V_o (the replica of the rail-to-rail comparator input signal) with a reference voltage produced by a voltage divider. The reference voltage is in the range that both the PMOS and NMOS comparators operate.

3.3.4 Summary of the Comparator

In section 3.3, the propagation delay in a comparator is discussed, and a short propagation delay three-stage comparator with hysteresis is analyzed and designed. Based on the above discussion, a rail-to-rail input comparator is proposed. This is an important component to assure a wide output voltage swing modulator to be realized. The schematics of the logic circuits used in Figure 3.28 are shown in Appendix A.

3.4 Envelope Detector

Traditionally the envelope detector, shown in Figure 3.29, consists of a diode and a parallel RC low-pass filter. When the input V_{in} has a positive potential compared to the output V_{out}, the diode D will conduct. And the capacitor C will charge up approximately to the peak value of V_{in}. When V_{in} is less than V_{out} across the capacitor, the diode conduction will be cut off and the capacitor will start to discharge through the resistor R with the voltage falling off exponentially [33].

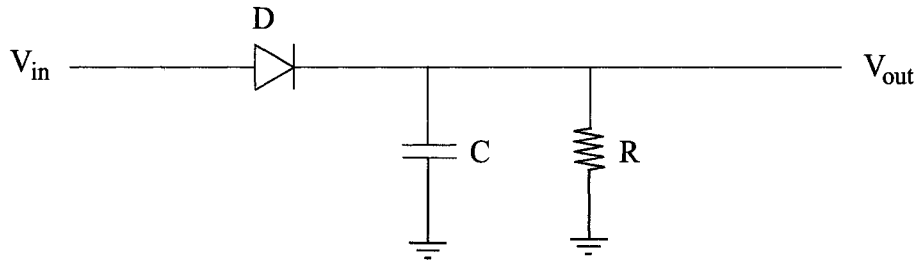


Figure 3.29 A conceptual envelope detector

Here it is assumed that an amplitude modulation (AM) signal has the form [34]

$$V_{in} = A_0(1 + m\cos\omega_s t)\sin\omega_c t \tag{3-30}$$

where A_0 is the amplitude, ω_s is the modulating signal angle frequency, ω_c is the carrier angle frequency and m is the modulation index.

If the signal is fed to a half-wave rectifier, the output may have the form as

$$V_{out} = \eta A_0(1 + m\cos\omega_s t)\frac{(\cos\omega_c t + |\cos\omega_c t|)}{2} \tag{3-31}$$

Because the Fourier series expansion of $\frac{(\cos\omega_c t + |\cos\omega_c t|)}{2}$ is

$$\frac{(\cos\omega_c t + |\cos\omega_c t|)}{2} = \frac{1}{\pi}\left(1 + \frac{\pi}{2}\cos(\omega_c t) - 2\sum_{k=1}^{\infty}\frac{\cos(2k\omega_c t)}{4k^2 - 1}\right) \tag{3-32}$$

Hence

$$V_{out} = \frac{\eta A_0}{\pi}(1 + m\cos\omega_s t)\left(1 + \frac{\pi}{2}\cos(\omega_c t) - 2\sum_{k=1}^{\infty}\frac{\cos(2k\omega_c t)}{4k^2 - 1}\right)$$

$$= \frac{\eta A_0}{\pi}\left\{(1 + m\cos\omega_s t) + \frac{\pi}{2}\left(\cos\omega_c t + \frac{m}{2}(\cos(\omega_c + \omega_s)t + \cos(\omega_c - \omega_s)t)\right)\right.$$

$$-2\sum_{k=1}^{\infty}\left\{\frac{\cos(2k\omega_c t)}{4k^2-1}-\frac{m}{2}\frac{(\cos(2k\omega_c+\omega_s)t+\cos(2k\omega_c-\omega_s)t)}{4k^2-1}\right\} \qquad (3\text{-}33)$$

From (3-33) one can see that the output signal includes many frequency components: the modulating ω_s, the carrier ω_c, the sidebands with frequency $\omega_c+\omega_s$, $\omega_c-\omega_s$, the even harmonics of carrier $2k\omega_c$ and the sidebands with frequency $2k\omega_c+\omega_s$, $2k\omega_c-\omega_s$. In general, the modulating frequency ω_s is much lower than the carrier ω_c, so a simple *RC* network can be used to filter out the higher frequency components.

In a CMOS technology, an ideal diode can not be realized. In this design, the gate-source PN junction of an NMOS transistor is used as a diode. The whole circuit of the envelope detector used in this design is shown in Figure 3.30 [12]. Transistor M1, capacitor C1 and current source M3 constitute the diode envelope detector. To cancel the first order DC voltage and distortion introduced by M1, a pseudoreplica circuit is used. The pseudoreplica circuit consists of M2 and current source M4.

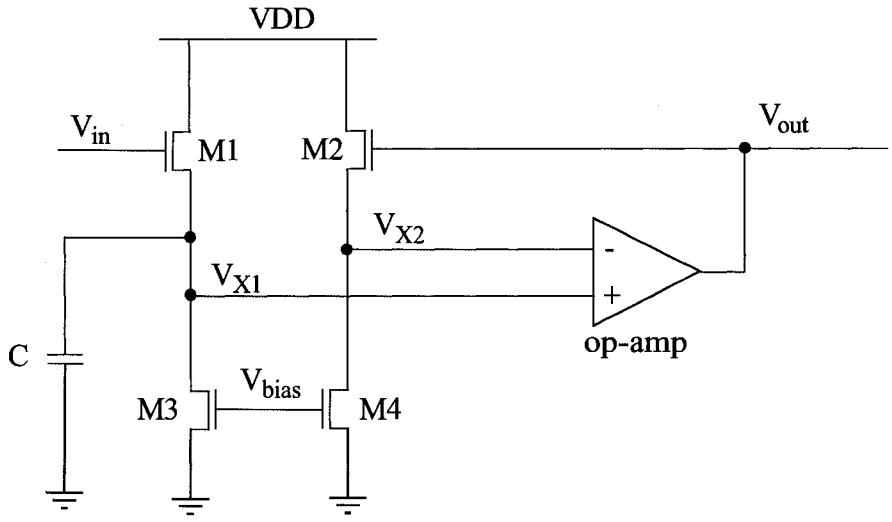


Figure 3.30 CMOS envelope detector

The equivalent small signal circuit of the envelope detector circuit without pseudoreplica circuit is shown in Figure 3.30. From Figure 3.30(b), one can find that $V_1 = V_{in} - V_{X1}$, $g_{m1}V_1 - g_{mb1}V_{X1} = V_{X1}/(r_{o1} \| r_{o3} \| (1/(sC)))$, thus,

$$V_{X1} = \frac{\frac{1}{g_{mb1}} \| r_{o1} \| r_{o3} \| \frac{1}{sC}}{\frac{1}{g_{mb1}} \| r_{o1} \| r_{o3} \| \frac{1}{sC} + \frac{1}{g_{m1}}} V_{in} \tag{3-34}$$

From (3-34) one can see that at high frequency, i.e. at frequency ω_c, the value of $\frac{1}{sC}$ is very small, $\frac{1}{sC} \ll \frac{1}{g_{mb1}} \| r_{o1} \| r_{o3}$, thus (3-34) can be simplified as $V_{X1} = \frac{1/(sC)}{1/(sC) + 1/g_{m1}} V_{in}$. Since $\frac{1}{sC} \ll \frac{1}{g_m}$, so for high frequency components, V_{X1}/V_{in} is close to 0. Whereas at low frequency, i.e. at frequency ω_s,the value of $\frac{1}{sC}$ is very large, $\frac{1}{sC} \gg \frac{1}{g_{mb1}} \| r_{o1} \| r_{o3}$, then (3-34) can be simplified as

$$V_{X1} = \frac{\frac{1}{g_{mb1}} \| r_{o1} \| r_{o3}}{\frac{1}{g_{mb1}} \| r_{o1} \| r_{o3} + \frac{1}{g_{m1}}} V_{in} \tag{3-35}$$

so for low frequency component, V_{X1}/V_{in} is close to a constant value $V_{X1}/V_{in} = \frac{1/g_{mb1} \| r_{o1} \| r_{o3}}{1/g_{mb1} \| r_{o1} \| r_{o3} + 1/g_{m1}}$, which is only dependent on the circuit parameters. This explains why this circuit can be used as a envelope detector.

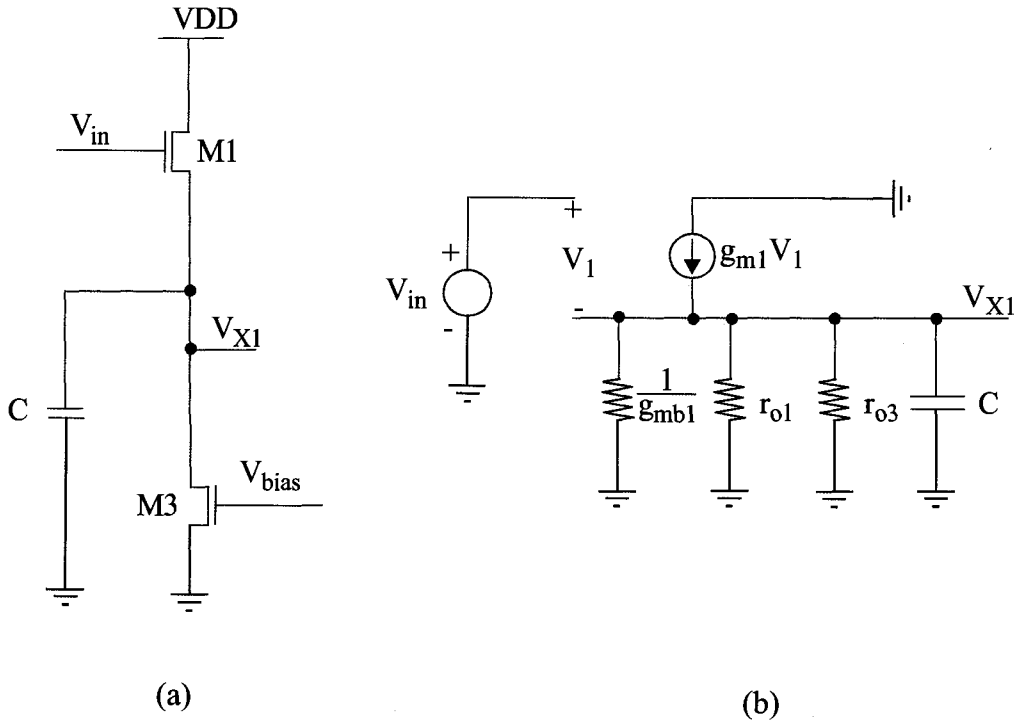


Figure 3.31 (a) Envelope detector without psuedoreplica circuit (b) small signal equivalent circuit

The circuit in Figure 3.30 is analyzed as following. Similar to (3-34), one can get the expression of V_{X2} as

$$V_{X2} = \frac{\frac{1}{g_{mb2}} \| r_{o2} \| r_{o4}}{\frac{1}{g_{mb2}} \| r_{o2} \| r_{o4} + \frac{1}{g_{m2}}} V_{out} \tag{3-36}$$

From Figure 3.30 one can get

$$(V_{X1} - V_{X2})A = V_{out} \tag{3-37}$$

where A is the open-loop gain of the op-amp. Substituting (3-35) and (3-36) for (3-37), one can obtain,

$$V_{out} = \frac{BAV_{in}}{1+BA} = V_{in}\left(1-\frac{1}{1+BA}\right) \tag{3-38}$$

where $B = \dfrac{1/g_{mb1} \| r_{o1} \| r_{o3}}{1/g_{mb1} \| r_{o1} \| r_{o3} + 1/g_{m1}} = \dfrac{1/g_{mb2} \| r_{o2} \| r_{o4}}{1/g_{mb2} \| r_{o2} \| r_{o4} + 1/g_{m2}}$.

Here it is assumed that transistor M1 and M2, M3 and M4 have the same dimension respectively. From (3-38), it can be seen that as the open-loop gain of op-amp $A \to \infty$, then $V_{out} \to V_{in}$.

From the above analysis one can understand that a high gain op-amp is important in this envelope detector design. And a key point of this envelope detector is that the pseudoreplica circuit operates at the modulating frequency, not at the carrier frequency.

3.5 Summary

In this chapter the operation and hardware implementations of the DM modulator have been presented, which include the core of the modulator, a wideband rail-to-rail input/output operational amplifier, a fast rail-to-rail comparator with hysteresis and the envelope detector. The simulation results of this modulator will be presented in the next chapter.

CHAPTER 4

Simulation Results

4.1 Introduction

The modulator layout is implemented by Cadence Virtuso which is shown in the Appendix. In order to evaluate the modulator performance, the post-layout simulation results of each subblock and the complete modulator are obtained.

4.2 Simulation Results of Envelope Detector

The envelope detector occupies 0.01 mm^2 active die area, dissipates 1.5 mW static power, and has a sensitivity of -10 dBm. The waveforms of transient response are shown in Figure 4.1. The input is a two-tone signal: one tone is 2 GHz and the other is 2.001GHz, 2.002GHz or 2.005GHz respectively (shown in Figure 4.1(a)). Each signal has the same amplitude of 90 mV. The outputs of the envelope are shown in Figure 4.1(b), (c) and (d).

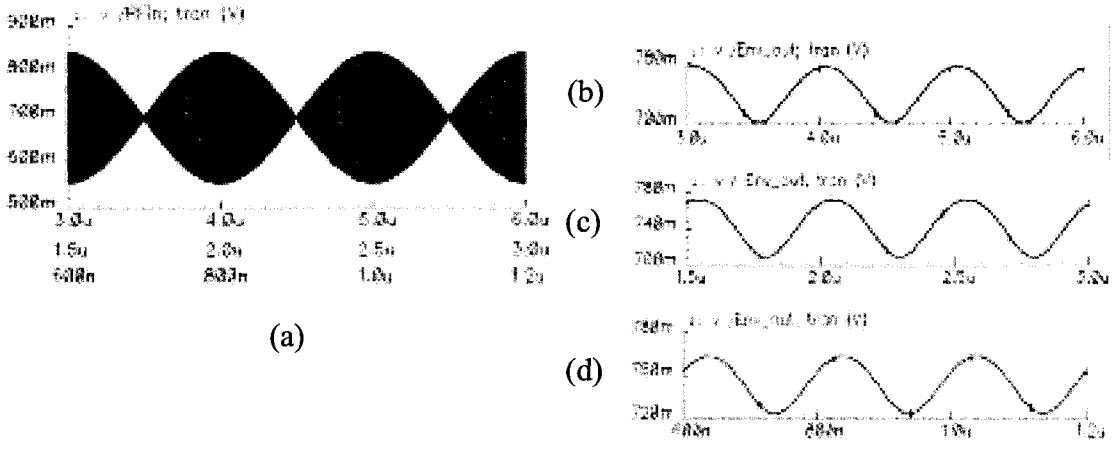


Figure 4.1 Two-tone input signal transient simulation (a) input signal with tone spacing of 1MHz, 2MHz and 5MHz (b) 1MHz tone spacing output (c) 2MHz tone spacing output (d) 5MHz tone spacing output

In Figure 4.1(d), it can be seen that the envelope detector is capable of extracting a 5 MHz envelope from a 2 GHz RF input signal. The quantitive distortion of the extracted envelope can be obtained by the total harmonic distortion (THD) which is defined as,

$$THD = \frac{\sum HarmonicPowers}{FoundamentalFrequencyPower} = \frac{P_2 + P_3 + \ldots + P_n}{P_1}$$

Although the extracted 5 MHz envelope has a certain level distortion, the dynamic power supply technique does not need a high fidelity of the envelope replica. So this envelope detector can meet the requirement of the dynamic power supply technique.

The performance of the envelope detector is summarized in Table 4.1.

TABLE 4.1: Envelope Detector performance summary

Specification	Value	Unit
Bandwidth	5.0	MHz
Sensitivity	-10	dBm
Power dissipation	1.5	mW
Die area	0.04	mm^2

4.3 Simulation Results of Op-amps

As discussed in section 3.2, this modulator uses two op-amps with the same topology. In the block of envelope amplification, the op-amp should have a wide bandwidth and rail-to-rail output. In the block of envelope detector, the op-amp should have a rail-to-rail input range and a relatively high open-loop gain at a frequency greater than the modulator bandwidth. To obtain the simulation results, the load of all the test benches in this section is a capacitor of 2 pF. The simulation results are shown in the following sections.

4.3.1 Op-amp for Envelope Amplification

A transient simulation of the amplifier in unity gain configuration with the rail-to-rail swing at the input is shown in Figure 4.2. The op-amp is not slewing and exhibits reasonable linear behavior. The excellent transient performance of this amplifier can be

attributed to the output class AB stage. Figure 4.2 shows the transient response with a rail-to-rail input signal at 4 MHz and the output swing is -0.885 ~ 0.885 V.

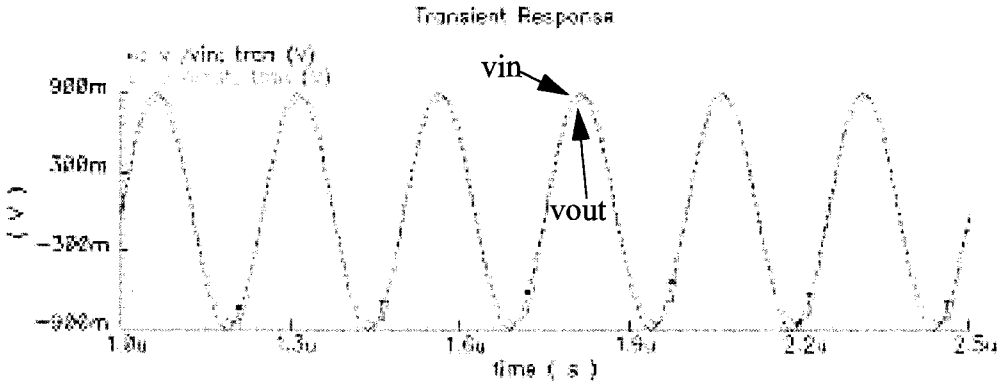


Figure 4.2 Transient response of unity gain feedback configuration with 4MHz rail-to-rail input

The frequency response of the op-amp is shown is Figure 4.3. It can be seen that the op-amp achieves a open loop gain of 91.6dB and a phase margin of 68°. The unity gain frequency of the op-amp is 197.78 MHz.

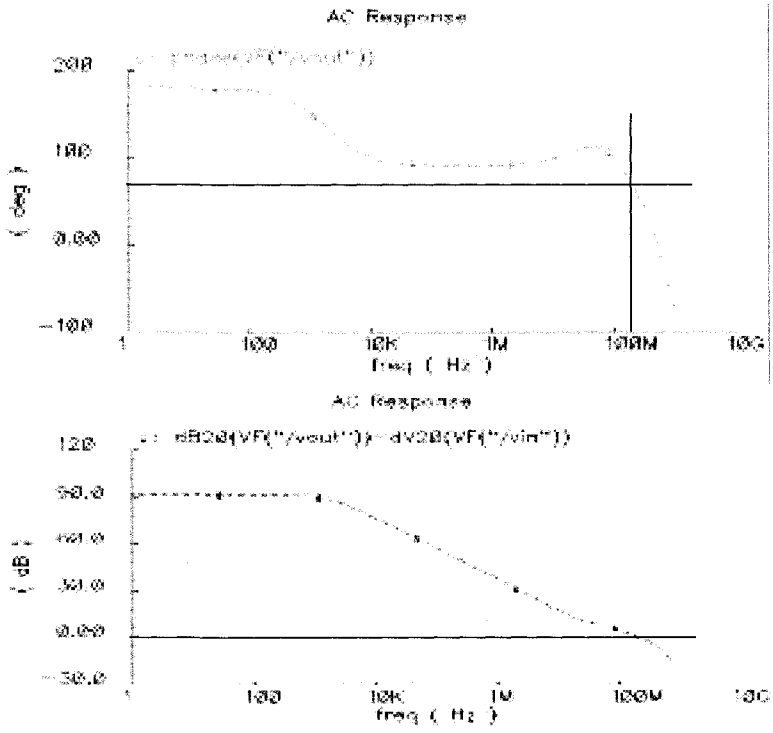


Figure 4.3 Frequency response of the op-amp for the envelope amplification

A DC simulation result of the amplifier in unity gain configuration with the swing at the input rail-to-rail is shown in Figure 4.4, which shows the DC characteristic common-mode input range of this op-amp. The common-mode input range is from 0 to 1.8 V which is rail-to-rail.

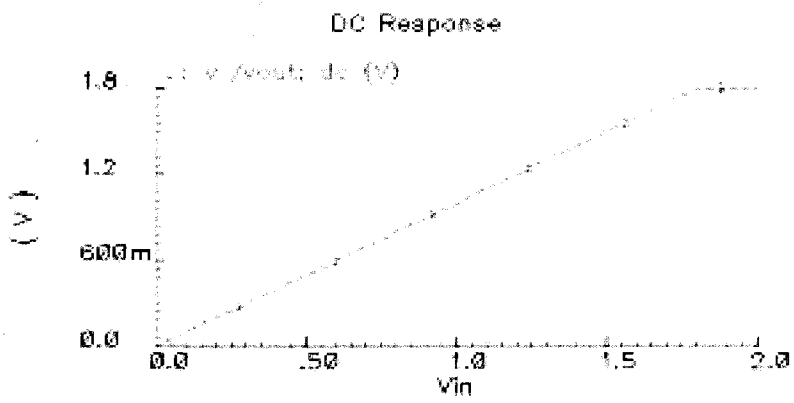


Figure 4.4 DC characteristic common-mode input range of the op-amp for the envelope amplification

A step response of unity gain feedback configuration with 100 mV step input is shown in Figure 4.5, which shows that the settling-time is 36.88 ns.

Table 4.2 summarizes the op-amp performances.

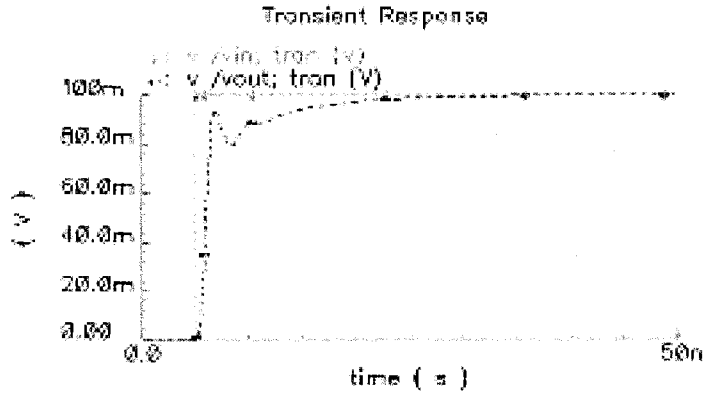


Figure 4.5 Step response of unity gain feedback configuration with 100 mV step input

TABLE 4.2: Op-amp in envelope amplification block performance summary

Specifications	Value	Unit
Supply voltage	-0.9~0.9	V
Load capacitance	2.0	pF
Open loop voltage gain	91.62	dB
Unity gain bandwidth	197.78	MHz
Phase margin	68.17	degree
Common mode rejection ratio	101.5	dB
Power supply rejection ratio+	95.59	dB
Power supply rejection ratio-	66.96	dB
Slew rate	44.55	V/μs
Settling time	36.88	ns
Input offset voltage	4.62	mV
Common mode input range	-0.9~0.9	V
Output swing (@ 4MHz)	-0.85~0.84	mV
Power dissipation	1.4	mW
Active die area	50*100	μm * μm

4.3.2 Op-amp for Envelope Detector

Figure 4.6 shows the DC characteristic common-mode input range of this op-amp in unity gain configuration with the swing of rail-to-rail at the input. The common-mode input range is from 0 to 1.8 V which is rail-to-rail.

The frequency response of the op-amp is shown is Figure 4.7. It can be seen that the op-amp has an open loop gain of 47.4dB, and a phase margin of 86° at 3 MHz.

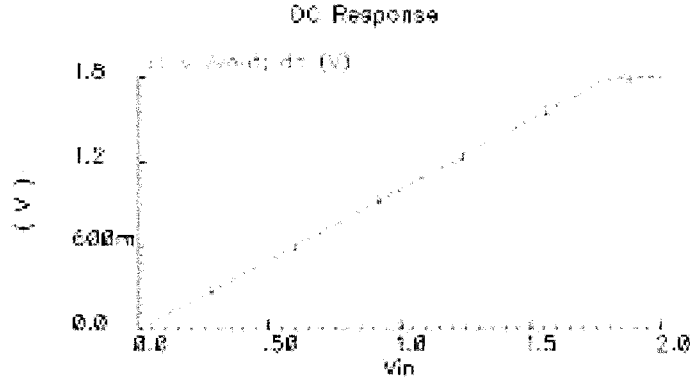


Figure 4.6 DC characteristic common-mode input range of the op-amp for the envelope detector

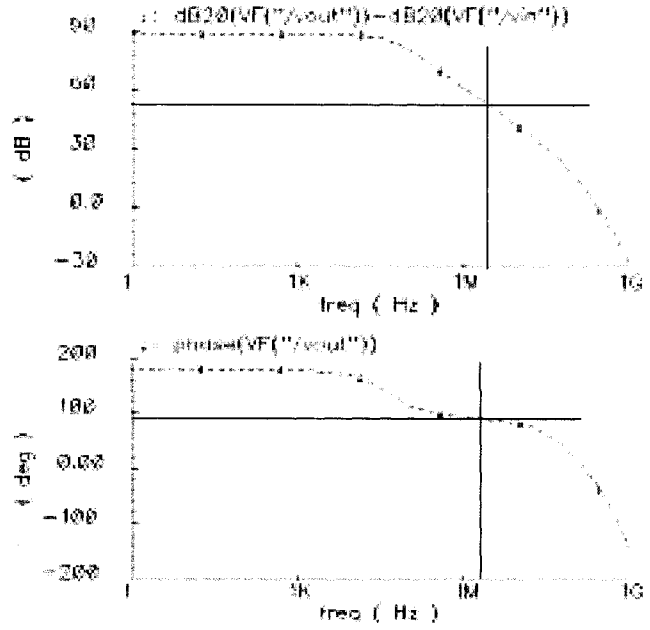


Figure 4.7 Frequency response of the op-amp for the envelope detector

The performance of the op-amp in envelope detector block is summarized in Table 4.3.

TABLE 4.3: Op-amp in envelope detector block performance summary

Specifications	Value	Unit
Supply voltage	-0.9~0.9	V
Load capacitance	2.0	pF
Open loop voltage gain (@ 3MHz)	51.2	dB
Common mode input range	0.9~0.9	V
Output swing (@ 4MHz)	-0.85~0.84	mV
Power dissipation	1.5	mW
Active die area	50*100	μm * μm

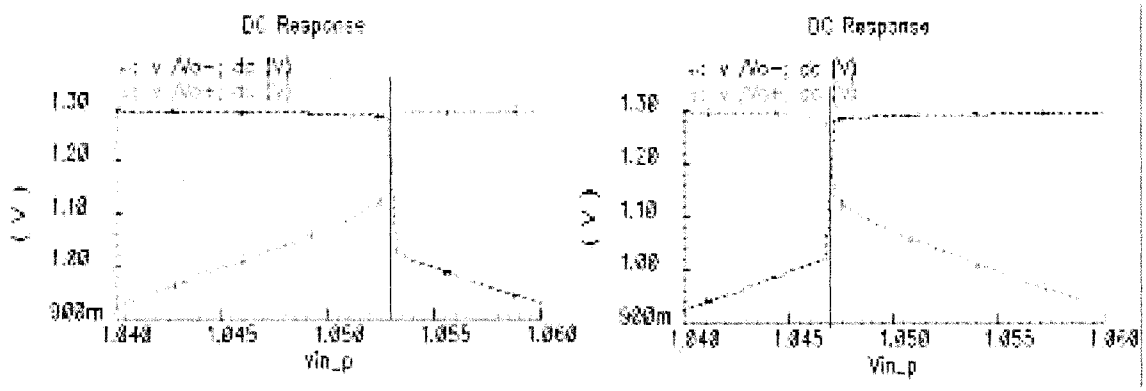
4.4 Simulation Results of the Rail-to-rail Comparator

In order to compress the noise, a hysteresis comparator is used in this design. Figure 4.8(a) shows a sweep of V_{in+} from 1.04 V to 1.06 V, with V_{in-} held at 1.05V. From Figure 4.8(a) one can see that the decision circuit switches states when V_{in+} is 3 mV above

V_{in-} (i.e., V_{in-}=1.053). The case of V_{in+} being swept from 1.06 V to 1.04 V is shown in Figure 4.8(b). Switching occurs in this situation when V_{in+} =1.047 V. So the hysteresis in this comparator is 3 mV.

In this comparator, the main noise is the kickback noise, however, as discussed in section 3.2.2, the kickback noise is isolated by the preamplification stage, so the coupled kickback noise at the input terminals of the comparator can not be larger than 3 mV.

The comparator has a propagation delay of 4.2 ns, a dc gain of 80.3 dB, and the power dissipation is 0.9 mW. The anti-overlapping and buffer circuit has the total delay of 2.6 ns. The overall propagation delay from comparator input to the input of the LC low-pass filter is in the order of 7 ns. The performance of the comparator is summarized in Table 4.4.



(a) (b)

Figure 4.8 DC response of getting comparator hysteresis (a) positive hysteresis (b) negative hysteresis

TABLE 4.4: Comparator performance summary

Specifications	Value	Unit
Supply voltage	1.8	V
DC gain	80.3	dB
Hysteresis voltage	3	mV
Input range	0~1.8	V
Propagation delay	4.2	ns
Power dissipation	0.9	mW
Active die area	100* 50	μm * μm

4.5 Simulation Results of the Modulator

In this section the simulations have been performed with a load resistor of 5 Ω, lowpass filter inductor of 850 nH and capacitor of 150 pF. Figure 4.9 shows the transient response with 1.5 MHz sinusoidal input to the comparator.

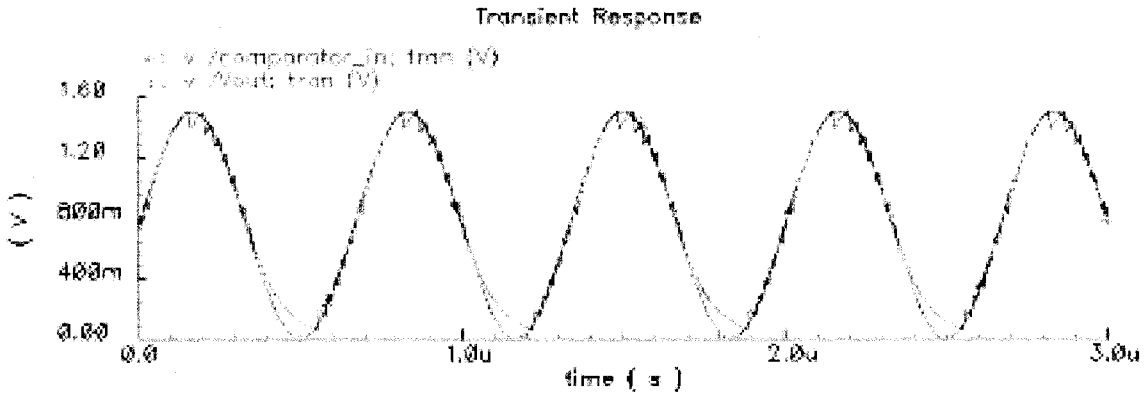


Figure 4.9 Waveforms of transient response with 1.5 MHz sinusoidal input to comparator

Figure 4.10 shows the modulator transient response to the pulse with different input levels from 0.01 V to 1.6 V. The simulation results of output power, input power, total power loss, efficiency, output residue ripple and switching frequency are summarized in Table 4.5. From Table 4.5 one can see that in the output voltage range from 0 V to 1.6 V, the amplitudes of the output residue ripple are approximately 50 mV_{pp}. In this simulation, the reference voltage of the input_selection comparator is set at 0.75V.

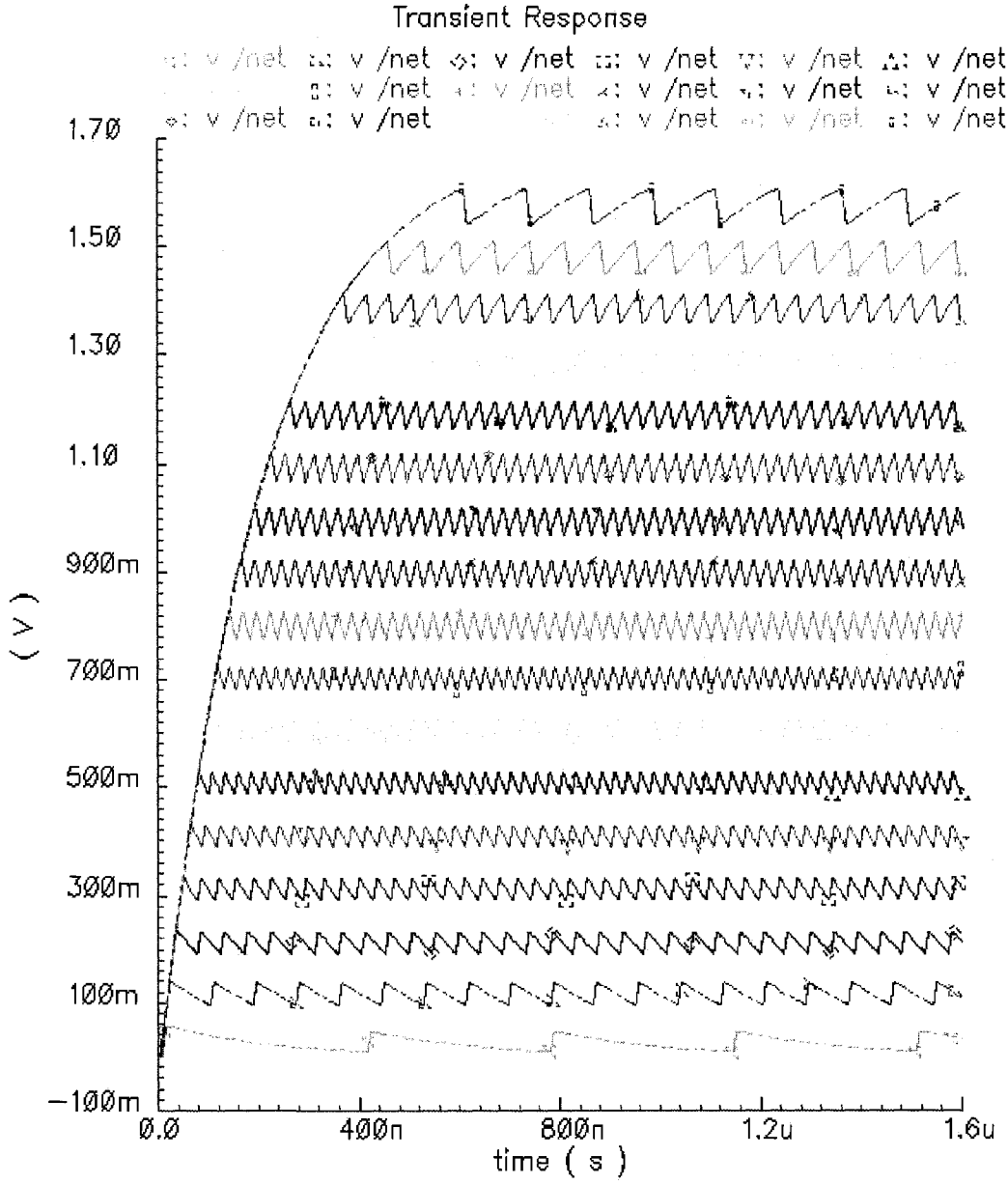


Figure 4.10 Transient response to the pulse with different input levels from

TABLE 4.5: Modulator (excluding envelope detector and amplification) performance summary

Vout (V) Goal/ Simulated	P_{out} (mW)	P_{in} (mW)	Efficiency	Total Loss (mW)	Output Residue Ripple (mV_{pp})	Switching Frequency (MHz)
1.6 / 1.57	497.3	531.9	93.5%	34.6	67	4.3
1.5 / 1.48	438.3	469.4	93.4%	31.1	61	14.3
1.4 / 1.38	383.5	417.6	91.9%	34.1	48	23.3
1.3 / 1.29	331.5	368.2	90.0%	36.7	46	25.6
1.2 / 1.19	283.3	318.3	89.0%	35.0	46	29.4
1.1 / 1.09	238.8	272.5	87.6%	33.7	49	32.2
1.0 / 0.99	198.3	231.4	85.7%	33.1	49	37.0
0.9 / 0.90	161.3	192.7	83.7%	31.4	48	37.0
0.8 / 0.80	128.3	159.1	80.6%	30.8	46	37.0
0.7 / 0.70	98.6	132.3	74.6%	33.7	40	45.4
0.6 / 0.60	73.1	103.6	70.6%	30.5	39	41.6
0.5 / 0.50	51.4	78.5	65.5%	27.5	39	38.5
0.4 / 0.41	33.5	57.6	58.1%	24.1	38	33.3
0.3 / 0.31	19.4	40.6	47.9%	21.2	36	28.6
0.2 / 0.21	9.14	24.7	37.0%	15.6	38	20.0
0.1 / 0.12	2.72	13.0	20.9%	10.3	38	11.8

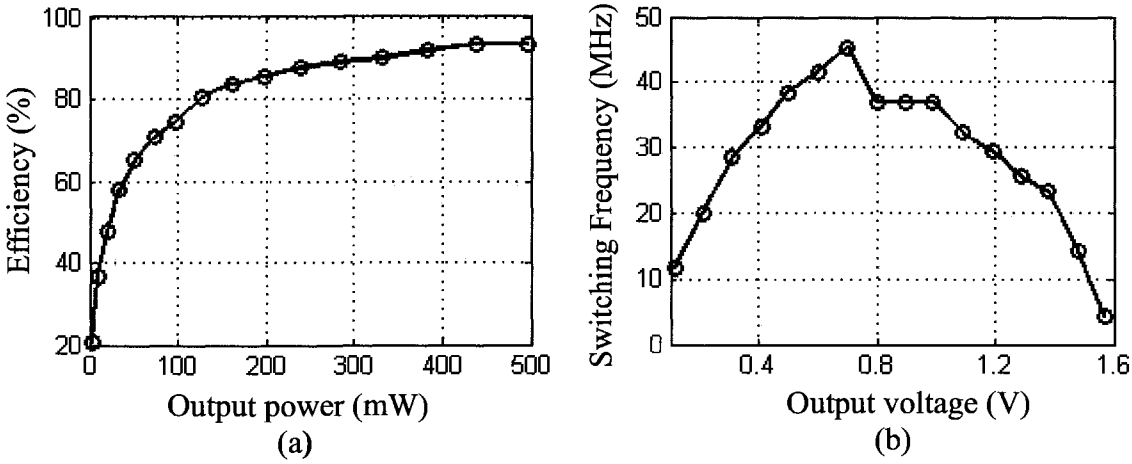


Figure 4.11 (a) Efficiency vs. output voltage (b) Switching frequency vs. output voltage

Figure 4.11 shows the modulator efficiency vs. output voltage and the switching frequency vs. output voltage. Figure 4.11(a) shows that the efficiency of the modulator (excluding envelope detector and amplification) is higher than 75% when the output power is higher than 100mW . Figure 4.11(b) shows that the typical switching frequencies are larger than 20 MHz.

Figure 4.12 shows the transient response of the modulator with a two-tone input signal with a tone spacing of 1.5 MHz. The amplitude of each tone signal is 90 mV_{pp}.

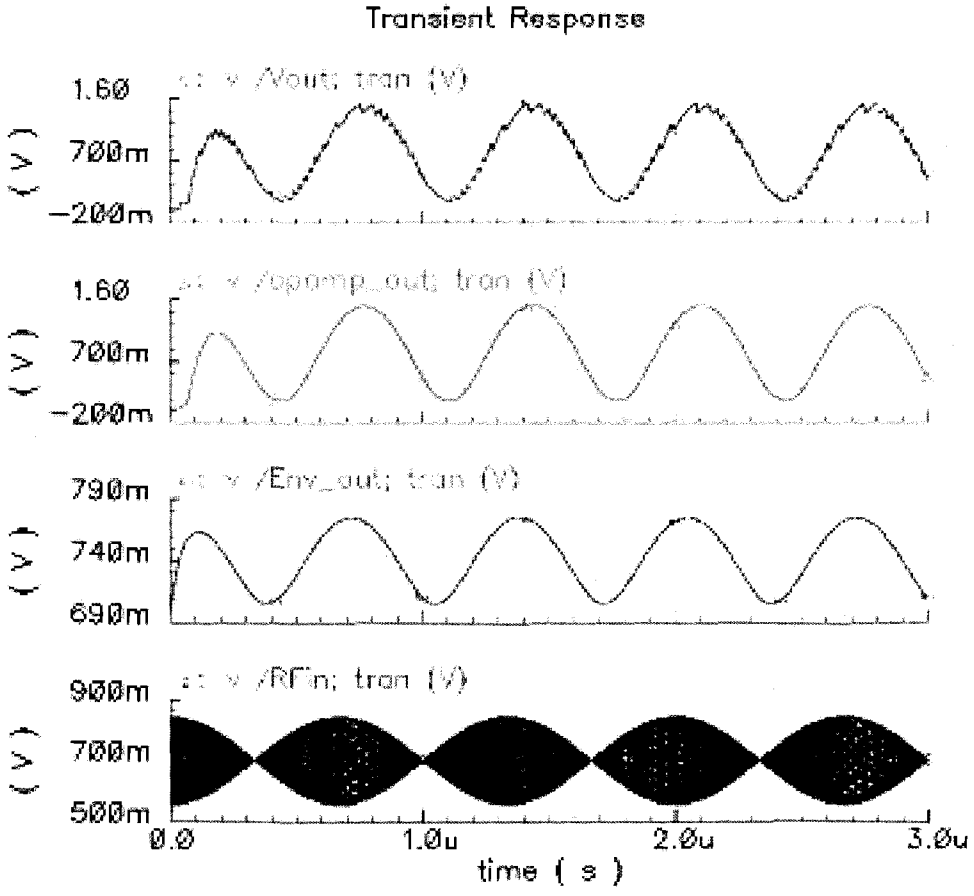


Figure 4.12 Efficiency (a) vs. Input reference voltage (b) vs. Output power

The overall performance of the modulator is summarized in Table 4.6 and the performance comparison of recently reported modulators is shown in Table 4.7.

TABLE 4.6: Modulator (including envelope detector and amplification) performance summary

Parameter	Value	Unit
L (off-chip)	850	nH
C (off-chip)	150	pF
Load resistor	5	Ω
Die area	1.5 * 2	mm^2
Effective output voltage range	0 ~ 1.6	V
Typical output residue ripple	~ 50	mV_{pp}
Typical switching frequency	> 20	MHz

TABLE 4.7: Performance comparison of recently reported modulators

Reference	[13]	[35]	This work
Technology	0.35 μm CMOS technology	IBM's SiGe BiCMOS 6HP process	0.18 μm CMOS technology
Bandwidth	2 MHz	5.2 MHz	2 MHz
Modulation mode	DM	PWM	DM
Output voltage range	1.25 ~ 3.3 V	1.3 ~ 3.3 V	0 ~ 1.6 V
Switching frequency	16 MHz	88.7 MHz	> 20 MHz
Output residue ripple	~180 mV_{pp}	< 0.5%	~50 mV_{pp}
Die area	1.15*2.1 mm^2	700 * 215 μm^2 (without pads)	1.5 * 2 mm^2

4.6 Summary

In this chapter, various simulations have been conducted on the designed modulator. The simulation results support the design methodology. The modulator has achieved a bandwidth larger than 2.0 MHz, the maximum output power is close to 500 mW, the output voltage range from 0 V to 1.6 V. The envelope detector and rail-to-rail op-amps have met the requirements of the DM modulator.

CHAPTER 5 *Conclusion and Future Work*

5.1 Conclusion

In this thesis, a wide output voltage swing DM modulator for the envelope tracking technique has been designed. A rail-to-rail input comparator with hysteresis has been proposed. To the best of the author's knowledge, this is the first DM modulator for the envelope tracking technique implemented in 0.18 μm CMOS process. The bandwidth is larger than 2.0 MHz, the output voltage range is from 0 V to 1.6 V, and the maximum output power is close to 500 mW. All these specifications show that this modulator can be a choice for the power amplifier design using the dynamic power supply technique where the linear RF power is implemented in 0.18 μm CMOS technology or even more advanced one.

5.2 Future Work

Improvement of this modulator can be made in the area of its efficiency at low output power level. From Figure 4.11(a), one can see that as the output power is smaller than 100 mW, the efficiency decreases dramatically with the decreasing output power. This can be improved by a technique called W-switching [36]. The idea behind this technique is that when the output power decreases, the ouptput stage power transistors can be made smaller, consequently the gate charge or discharge losesses will be decreased. The conduction loss inevitably increases, but the overall losses can still be decreased and therefore the overall efficiency increases.

The amplitude of the envelope detector output decreases with the increase of the envelope bandwidth. The wider the envelope bandwidth is, the more distortion will be introduced by this envelope detector. The distortion damages the modulator efficiency, so for a wider bandwidth (for example, 5 MHz) modulator, this envelope detector should be replaced.

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Appendix A: Schematics used in Figure 3.27

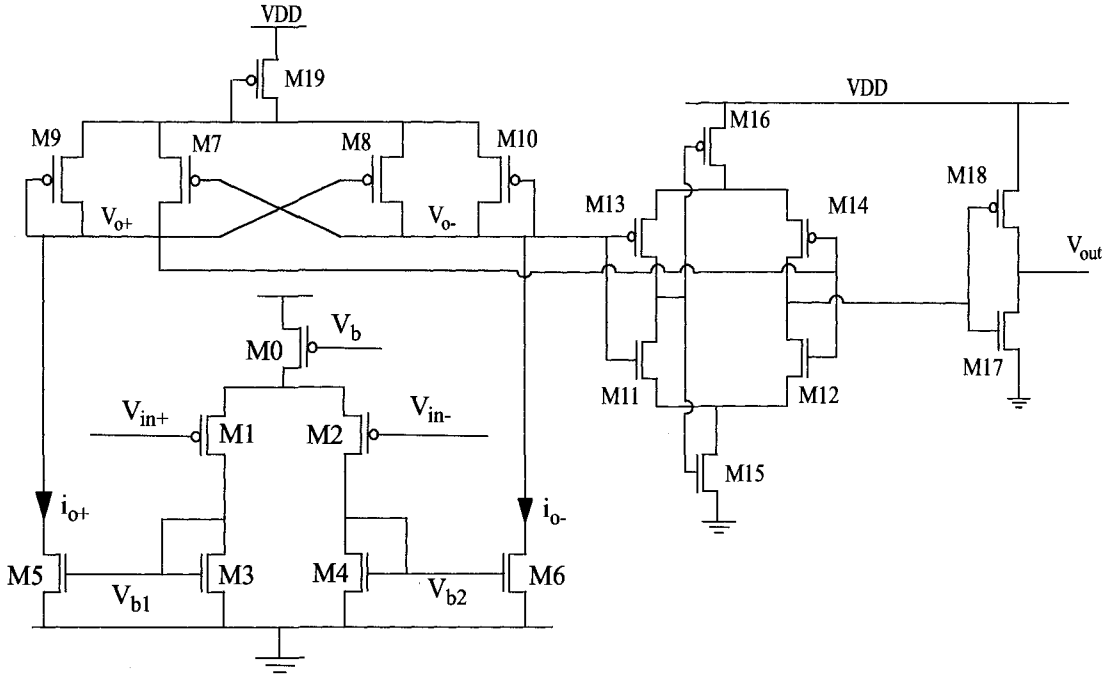

Figure A-1 Hysterestis comparator with PMOS input stage

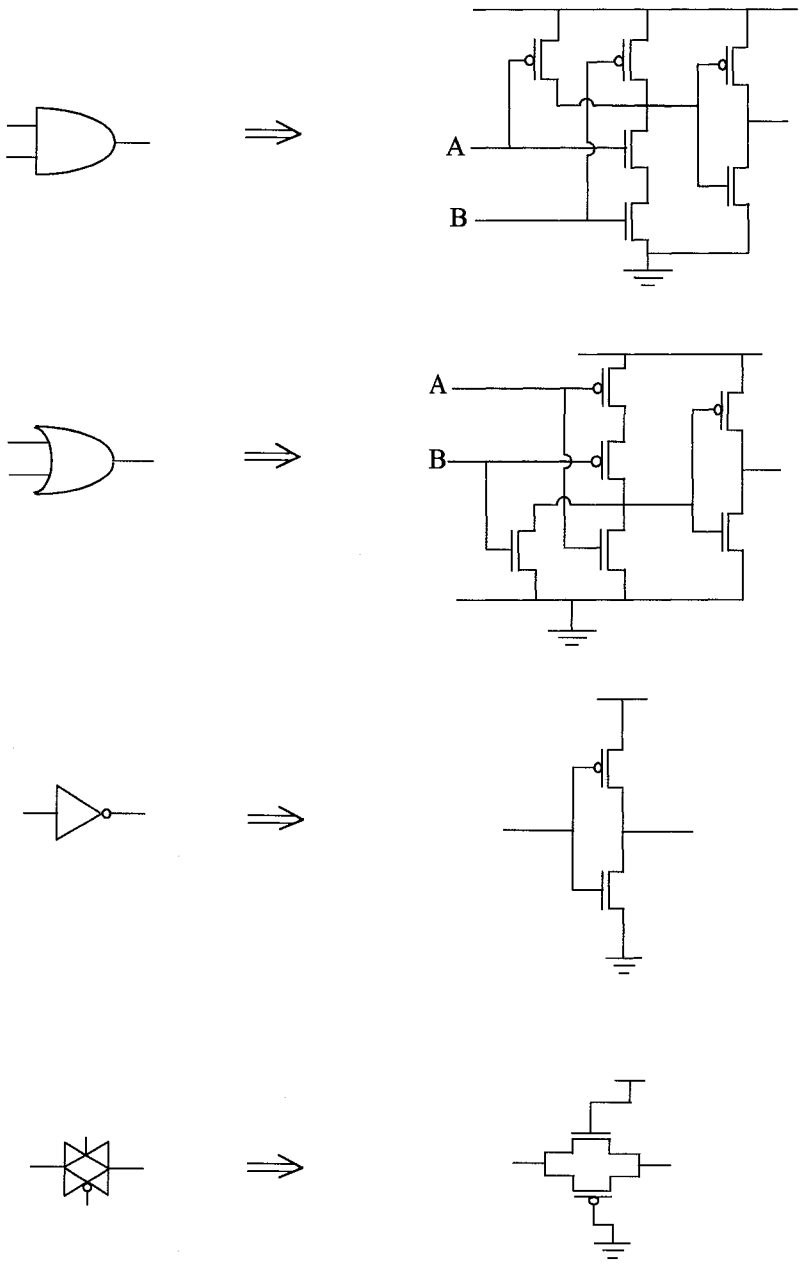

Figure A-2 Schematics of logic gate circuit used in Figure 3.27

Appendix B: Layout of the Modulator