MODELING OF THE DUAL-GATE GaAs MESFET

by

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in partial fulfillment of the requirements
for the degree of
Doctor of Philosophy

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ABSTRACT

Dual-Gate GaAs metal semiconductor Field Effect Transistors (DGFETs) are devices that find many microwave circuit applications such as mixers, phase shifters, and variable gain amplifiers. Accurate small-signal and large-signal models of the DGFET are needed for use in computer-aided design tools so that the circuit performance can be optimized before costly manufacturing steps are applied. Modeling the DGFET is the objective of this thesis.

The author introduces an analytical small-signal model of the device that is based on representing the common-source DGFET as a cascode connection of two single-gate FETs (SGFET) with the source of one SGFET grounded. The small-signal model parameters are extracted over a wide range of bias points over the frequency range 0.5-26 GHz. To develop a large-signal model, the model parameters of each SGFET part are then represented by functions of the drain-source voltage and the gate-source voltage applied on that SGFET part. To properly apply these control voltages, this model requires knowledge of the voltage at the inaccessible node artificially introduced between the two SGFET parts. A graphical technique or a numerical technique can be used to determine this node voltage at every bias point, but such methods are impractical. To overcome this difficulty, a second small-signal model of the DGFET is introduced. This new model deals with the DGFET as a four-port device (with the source grounded) rather than a cascode connection of two SGFETs. The four-port small-signal model accurately predicts the S-parameters of many common-source DGFETs of varying size over the full range of bias voltages and frequency range 0.5-26 GHz.

The author also introduces a large-signal four-port model of the DGFET based solely on voltage-dependent charge sources and voltage-dependent current sources. Empirical formulas are developed to describe the bias dependence of these sources, as determined from DC current-voltage measurements, and the bias-dependence of the small-signal model RF parameters. A new expression for the DGFET drain current is introduced. The new large-signal model accurately simulates the DC drain current, and the DC gate currents under extreme bias conditions (forward gate bias and gates breakdown). The model incorporates scaling rules and some thermal modeling. The new DGFET large-signal model is implemented in a standard RF circuit design tool (HPADS) where it accurately simulates the small-signal S-parameters, the DC I-V characteristics and large-signal measurements. The absolute error between the measured and the calculated S-parameters did not exceed 10% for magnitude or ± 12 degrees for phase over the three-dimensional extraction bias range and the frequency range 0.5-26.5 GHz.

As part of the modeling effort, a new and accurate technique to extract the extrinsic resistances of the DGFET is introduced.

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CHAPTER 1

INTRODUCTION

1.1 Thesis Motivation

Dual-gate GaAs MESFETs (DGFETs) are attractive devices for many microwave circuit applications such as frequency converters [1], mixers [2], modulators [3], pulse regenerators [4], phase shifters [5], and variable gain amplifiers [6], due primarily to the presence of the extra input terminal. To minimize the number of design cycles from initial design to working chip, the performance of final circuit design must be simulated accurately before fabrication. Accurate small-signal and large-signal models of the DGFET are essential for these simulations.

The DGFET exhibits complex behavior, which is difficult to model. To the best of the author's knowledge, no complete and efficient large-signal model of the device has been reported in the published literature. For circuit design, the usual approach is to represent a DGFET by a cascode connection of two identical single-gate MESFETs (SGFETs) [7]. This representation does not model the DGFET accurately. This lack of an accurate large-signal model prevents the use of the device on a wide scale or at least makes circuit design difficult.

Most large-signal device models are built from knowledge of the small-signal device model's dependence on different bias conditions. An accurate complete small-signal model of the DGFET also does not exist. This is one of the main reasons that a large-signal model of the DGFET has not yet been developed. Once the analytical small-

signal model exists, it can be extracted at different bias points and an empirical large-signal model can be developed.

The purpose of this thesis is divided into the following main parts:

1. The development of an analytical, small-signal model of the DGFET that can be extracted easily and accurately from standard S-parameter measurements.
2. The development of a large-signal model of the DGFET based on the new small-signal model.
3. Implementation of both new models within a standard microwave computer-aided design tool and verification of the models with small-signal S-parameter measurements, DC current-voltage characteristics, and available large-signal measurements.

1.2 Types of Device Models for Circuit Simulation

1.2.1 Physical Models

Physical device models are based on the actual physics of operation of the device. The model is based on solution of a set of basic semiconductor device equations subject to appropriate boundary conditions determined by the transistor geometry and doping profile and the applied boundary conditions. These equations include Poisson's equation, the current continuity equation and Schrodinger's equation.

Physical-based models are difficult to work with since they require detailed information about semiconductor process parameters, which may not be readily available. These models often do not accurately track measured data due to idealization of device behavior.

1.2.2 Empirical Models

The most common models for high-frequency circuit simulations are empirical models. The device is represented by an equivalent circuit topology whose layout and components mimic device performance. To represent the non-linearity of the model, the components are characterized by equations that are formulated either empirically or from the device physics. Those equations are parameterized functions of the controlling voltages. The accuracy of an empirical model depends on the following:

- i) The accuracy of the measured data.
- ii) The ability of the equations to predict the bias dependence of the circuit elements.

One major disadvantage of an empirical model is the inability to predict the changes in the device performance arising from variation in the device geometry and/or fabrication process. To overcome this problem, the empirical models can be adapted for varying gate widths by scaling the elements of the equivalent circuit topology.

1.2.3 Table-Based Models

Table-based empirical models have been developed as an alternative approach to nonlinear analytical models [8,9]. A circuit topology is used to represent the device like the empirical model. However, no analytical equations are used to describe the bias dependency of the circuit topology elements. The simulations of this type of model use the measured data at each bias point to calculate the elements of the device's equivalent circuit. For bias points where there is no data, the simulator interpolates between the data points. The accuracy of this type of modeling is high. However, an accurate and extensive experimental device characterization is required to achieve this high accuracy.

Coupled data acquisition and large storage requirements are two major drawbacks to this type of modeling.

1.3 Previous Small-Signal and Large-Signal Models of the Dual-Gate GaAs MESFET

The DGFET was originally fabricated by Turner et al. [10] in 1971. Since then, the DGFET has been involved in different applications. In the following, the published work done for modeling DGFETs will be reviewed.

1.3.1 Previous DGFET Small-Signal Models

In 1975, Liechti [3] suggested that the DGFET be modeled as a cascode connection of two SGFETs, FET^I and FET^{II} having gates $gate_1$ and $gate_2$ respectively. The operation and characterization of the DGFET can therefore be realized by combining the characteristics of the two SGFETs operated under the same drain current. This hypothesis is validated from physical studies using two-dimensional or quasi-two dimensional software [11]. These simulations show that the average longitudinal electric field remains very small inside the area between the two gates for an inter-gate distance of about $2\mu m$. Consequently, the average variations between the two gates are very small.

Initial modeling techniques utilizing approximate analytical expressions to determine the element values in the equivalent circuit model were reported [12,13]. Asai et al. [12] and Furutsuka et al. [13] introduced two small-signal, physical based, equivalent circuit models. Those models were limited to the case when $gate_2$ is RF grounded and reverse biased. The element values and the valid frequency range were not reported. To extend the work of Asai et al. [12] and Furutsuka et al. [13] for the case

when gate_2 is forward biased, Chao et al. [14] introduced a model that describes the behavior of the drain current based on Pucel's model [15].

The elements of the above models [12-14] can only be evaluated if the exact knowledge of mobility, doping density, and profile as well as the effective thickness of the active layer, is provided. These data result from tedious (often destructive) material characterization measurements and are normally not available to the circuit designer.

In 1981, two DGFET equivalent circuit models were reported [16-17]. The two models are determined from measured two-port S-parameters assuming the two SGFET parts to be equal. This assumption led to limited accuracy and frequency range validity of these models.

A more accurate small-signal model of DGFET has been proposed by Tsironis et al. [18,19]. A bi-directional DC transfer characteristics [20] was used to determine the bias conditions of each FET part of the DGFET. The extraction of the extrinsic elements was reported. Unfortunately, the procedures for extracting the model elements are very lengthy. They utilize DC and microwave measurements to characterize each FET part separately under its actual bias conditions. At a given device bias point, two sets of two-port S-parameters need to be measured at two different auxiliary bias conditions, as well as the three-port S-parameters of the device over a broad frequency range. In addition, four levels of computer optimization are required to define the model elements. The same procedures were carried out by Deng and Chu [21] but with only one level of optimization.

Scott and Minasian [22] introduced a model that is based on a simplified form of a small-signal model of a SGFET introduced by Minasian [23]. To extract the model,

beside the need for additional measurements, many assumptions were introduced that were not accurate enough and limited the use of the model at high frequencies.

Schöön [24] has described an empirical bias-dependent small-signal model of the DGFET. The model consists of two nonlinear, intrinsic SGFET models connected in cascode and embedded in a network of passive components that model different parasitics. However only gate-source capacitance C_{gs} , gate-drain capacitance C_{gd} , and the drain current generator were considered to vary with bias. The determination of the model parameters is accomplished by complicated optimization procedures.

It is clear from the above review that no complete analytical small-signal model for the DGFET has been published.

1.3.2 Previous DGFET Large-Signal Models

A few attempts to develop a large-signal model of the DGFET have been reported in the literature. Madjar [25] presented a physical-based large-signal model of DGFET by extending a physical-based large-signal model of a SGFET [26]. Besides the need for physical details to extract the model, which are not easily determined, the results published for both I-V characteristics and S-parameters did not show good agreement with the measurements [25]. Allam et al. [27] presented a non-linear model for a dual-gate hetero-structure FET. In this model, the bias-dependent elements taken into account were the current generators and the capacitances C_{gs} and C_{gd} of each SGFET part, while gate-source capacitance charging resistance R_i , delay time τ , transconductance g_m , drain-source capacitance C_{ds} and channel conductance g_d were considered to be bias-independent. To extract the model, Allam et al. [27] needed extra measurements of

single-gate HFETs fabricated on the same wafer containing the dual-gate HFETs. Besides being incomplete, the model parameters are difficult to extract.

Some numerical models of DGFET were reported [28], but these models are computationally inefficient.

As discussed in this section, a complete and efficient model of the DGFET does not exist in the open literature.

1.4 Original Contributions and the Organization of the Thesis

In this work, the author reports six original contributions, as follows:

1. The development of a new technique to determine the DGFET extrinsic resistances based on DC measurements [29].
2. The development of an analytical small-signal model of the DGFET [30] that deals with the device as a cascode connection of two SGFETs.
3. The development of a consistent small-signal model of the DGFET that is based on considering the DGFET as a four-port device [31].
4. The development of an empirical model of the DGFET drain current that is able to model both the DC and the RF drain current [32].
5. The DGFET gate currents under extreme bias conditions (forward gate bias and gates breakdown) were modeled [33].
6. The development of a large-signal model of the DGFET [33] based on the consistent small-signal model.

This thesis is organized into 7 chapters. In Chapter 2, the measurement methods used to characterize the DGFET are presented and discussed. In Chapter 3, the techniques used to extract the extrinsic parameters of the DGFET are discussed. The cascode DGFET small-signal model is reported and verified in Chapter 4. The development and verification of the consistent DGFET small-signal model are discussed in Chapter 5. In Chapter 6, the DGFET large-signal model is developed. Finally, the results, conclusions and suggestions for future work are presented in Chapter 7.

CHAPTER 2

CHARACTERIZATION OF THE DUAL-GATE GaAs MESFET

2.1 Introduction

The process of developing a model for a certain device has many steps. The first step is to study the physical structure of that device and its modes of operation. The second step is to perform a series of DC and RF measurements that characterize the device. Based on the physical structure and the characterizing measurements of the device, small-signal and large-signal analytical models that mimic the device are then developed. The last step is to verify the developed model using the characterizing measurements.

In this Chapter, the basic structure and modes of operation of the DGFET are briefly discussed. The methodology of the DC and RF measurements used to characterize the DGFET is also presented.

2.2 Basic Dual-Gate MESFET Operation

The physical structure of the DGFET is presented in Figure 2.1. As shown, the structure is similar to a single-gate FET except for the existence of a second gate electrode between the source and the drain. The device is built on a 100 μm thick semi-insulating substrate of GaAs. An n-type epitaxial active layer is grown on the substrate, and on top of it an n^+ layer. The source and drain electrodes form ohmic contacts to the GaAs n^+ material, while the two gate electrodes form Schottky-barrier junctions. I_{g1} , I_{g2} ,

l_{sg1} , l_{g1g2} and l_{g2d} are gate₁ length, gate₂ length, distance between the source and gate₁, inter-gate distance and the distance between gate₂ and the drain, respectively. Liechti *et al.* [3] showed that electrically, the DGFET is a cascode connection of two single-gate FET parts, FET^I and FET^{II} as shown in Figure 2.2.

Figure 2.1. Cross-section view of a dual-gate GaAs MESFET.

When a positive voltage is applied between the drain and the source (V_{ds}), it will be partitioned into two parts, V_{d1} (the effective drain voltage of FET^I) and V_{d2} (the effective drain voltage of FET^{II}) or

$$V_{ds} = V_{d1} + V_{d2} \quad (2.1)$$

The bias applied at the second gate (V_{g2s}) controls V_{d1} according to the relationship

$$V_{g2s} = V_{g2x} + V_{d1} \quad (2.2)$$

where x is the inaccessible node introduced between FET^I and FET^{II}.

Since the drain current carried by FET^I equals the current carried by FET^{II} , V_{d1} adjusts to establish the proper V_{g2x} value that allows FET^{II} to carry the DC current from FET^I .

Figure 2.2. The DGFET is composed of two SGFET parts.

The drain current of the DGFET will be modulated according to the voltage drop between each gate and its associating channel. No drain current will flow if the one of the depletion regions beneath one gate is totally depleted. Current saturation in the DGFET occurs when either of the two channels associated with the two gates individually saturates.

The DGFET has four characteristic operational modes depending on the internal bias conditions of the individual FET parts. These modes are [12]:

1. Both FET^I and FET^{II} in the saturation region.
2. FET^I in the resistance region while FET^{II} in the saturation region.
3. FET^{II} in the resistance region while FET^I in the saturation region.
4. Both FET^I and FET^{II} in the resistance region.

The advantages of the DGFET in comparison with the SGFET are [12]:

1. The increased functional capabilities such as gain control and signal mixing due to the presence of two independent control gates.
2. The reduced feedback or resulting improvement in power gain and stability.
3. When used as a mixer, one gate can be used as the LO port while the other is used as the RF port, thereby increasing the RF-LO isolation.

2.3 Design and Fabrication of Dual-Gate GaAs MESFETs

To model the DGFET, ten devices were layed out using Cadence software, and fabricated using the SAGDFET (Self-Aligned-Gate-Depletion mode-Field-Effect-Transistor) process [34] at Nortel Networks, Ottawa, Canada.

The basic FET parameters for this process are 1 μm gate length, current gain cutoff frequency $f_T = 18$ GHz, saturation drain current 118 mA/mm gate width, and pinch-off voltage -1.1 V.

The experimental devices are summarized in Table 2.1 where it is clear that except for devices 8, 9, and 10, all the devices are geometrically symmetric. The source terminals of all these devices are grounded using via holes.

Table 2.1 Description of the designed dual-gate GaAs MESFETs.

Device		# of gate	$W_g(\mu\text{m})$	$l_{g1}(\mu\text{m})$	$l_{g2}(\mu\text{m})$	$l_{sg1}(\mu\text{m})$	$l_{g1g2}(\mu\text{m})$	$l_{g2d}(\mu\text{m})$
1	1x50 μm	1	50	1	1	1.5	2	1.5
2	2x50 μm	2	100	1	1	1.5	2	1.5
3	2x100 μm	2	200	1	1	1.5	2	1.5
4	4x50 μm	4	200	1	1	1.5	2	1.5
5	6x50 μm	6	300	1	1	1.5	2	1.5
6	4x100 μm	4	400	1	1	1.5	2	1.5
7	6x100 μm	6	600	1	1	1.5	2	1.5
8	6x50 μm	6	300	1	1	3	2	1.5
9	6x50 μm	6	300	1	1	4.5	2	1.5
10	6x50 μm	6	300	1	1	6	2	1.5

where W_g is the total gate width.

The layout of a 6x100 μm DGFET is shown in Figure 2.3 as a sample of the transistor design. To be able to perform DC and RF measurements, the intrinsic DGFET terminals are connected with 50 Ω transmission lines to ground-signal-ground pads with 150 μm pitches. All the devices are fabricated on a GaAs substrate of 100 μm thickness. The abbreviations G_1 , G_2 , and D on Figure 2.3 refer to gate₁, gate₂, and the drain electrodes respectively. The source terminal will be referred to as “S” in the upcoming Figures.

Figure 2.3. The layout of the 6x100 μm DGFET described in Table 2.1

2.4 Measurements for Device Characterization

The target of this work is to develop both small-signal and large-signal models of the DGFET. As such, measurement of the DGFET DC and high frequency characteristics plays an important role. The measurements have two purposes. Firstly, the measured data are used to extract the parameters of the small-signal and large-signal models. Secondly, the measured data are used to evaluate the accuracy of the models.

2.4.1 DC I-V Characterization of the DGFET

DC I-V measurements are the most fundamental of all device characterization measurements. Figure 2.4 illustrates a schematic of a common source DGFET. The DC quantities that are measured, namely, the drain current I_d , gate₁ current I_{g1} and gate₂ current I_{g2} are also shown in Figure 2.4. From charge conservation, the source current, I_s , is equal to $-(I_{g1}+I_{g2}+I_d)$.

Figure 2.4. The DC quantities measured during DC I-V characterization.

The voltage difference between gate₁ and the source is referred to as the port voltage V_{g1s} . The voltage difference between gate₂ and the source is referred to as the port voltage V_{g2s} . The voltage difference between the drain and the source is referred to as the port voltage V_{ds} .

Before extensive measurements are made, two simple tests are used to make sure that the device under test (DUT) works normally. In both tests the drain current is measured at a fixed V_{ds} value (usually the value at which the pinch-off voltage is to be

measured) when the voltage of one gate is swept from some negative value (beyond the expected pinch-off voltage) to some positive value (few tenths of a volt), while the other gate is biased with zero current with the source grounded. For a normal device, the measured drain current should be almost zero when the gate voltage is more negative than the pinch-off voltage. The drain current should increase as the gate voltage becomes less negative, then saturates for positive values of the gate voltage. The measured drain current of a $6 \times 100 \mu\text{m}$ DGFET is shown in Figure 2.5 as V_{g1s} is swept from -2 V to 0.6 V with steps of 5 mV . Similar dependency is obtained by measuring I_d as a function of swept V_{g2s} while gate₁ is open circuited and the source is grounded.

The above two measurements are also used to determine the pinch-off voltage of each gate electrode. In this case the square root of the drain current is plotted (on the y-axis) versus the voltage of one gate (on the x-axis) and the linear part of the curve is extrapolated to intersect with the x-axis. The voltage at the intersection point is the pinch-off voltage of that gate electrode. Figure 2.6 shows a plot of the square root of the measured drain current versus V_{g1s} of a $6 \times 100 \mu\text{m}$ DGFET and shows how to calculate gate₁ pinch-off voltage (V_{p1}). From Figure 2.6, V_{p1} equals -1.1 V . A similar value is obtained for gate₂ pinch-off voltage (V_{p2}).

Figure 2.5. The measured drain current of a 6x100 μm DGFET at $V_{ds}=3\text{V}$ as V_{g1s} is swept from -2V to 0.6V with 5 mV steps.

Figure 2.6. The square root of the measured drain current of a 6x100 μm DGFET at $V_{ds}=3\text{V}$ as V_{g1s} is swept from -2V to 0.6V with 5 mV steps.

Once the DGFET is found to work properly, a sequence of DC and RF measurements are made. There are five types of I-V measurements to be made on a DGFET. These measurements are gate₁-diode measurements, gate₂-diode measurements, drain-current measurements, extrinsic resistances extraction measurements, and gate₁-source breakdown measurements.

In gate₁-diode measurement, the gate₁-source junction is forced into forward-bias configuration by applying a swept positive voltage at gate₁ when both gate₂ and the drain are open-circuited and the source is grounded. The current flowing into gate₁, I_{g1} , is measured as V_{g1s} is swept. The data from this measurement is used to extract gate₁-diode parameters V_{bi1} (built-in voltage), I_{s1} (junction saturation current), and n_1 (gate₁-diode ideality factor).

The gate₂-diode measurement is similar to the gate₁-diode measurements. Both gate₁ and the drain are open-circuited while the source is grounded. The current flowing into gate₂, I_{g2} , is measured as V_{g2s} is swept.

The forward gate₁ current of a 6x100 μm DGFET is shown in Figure 2.7. The gate current is very low at small forward bias voltages while the curve bends at the high end where the parasitic gate and drain resistances are having an effect. The bend at the high end of the curve defines where the parasitics start to dominate, and sets the bounds for model extraction. A similar curve is obtained for gate₂ electrode. In this work, the maximum positive values of V_{g1s} and V_{g2s} are found to be 0.6 V.

Figure 2.7. The measured gate₁ forward current as V_{g1s} varies from 0.2V to 0.75V with 5 mV steps.

The most common DC I-V characterization of the DGFET is the measurement of the device drain current I_d with respect to the drain voltage, at several values of V_{g1s} and V_{g2s} . The drain voltage is swept from 0 V to the upper limit of its normal operating range. Both V_{g1s} and V_{g2s} are swept from the pinch-off voltage to a maximum positive value defined from the gate-diode measurements. In this work, V_{ds} is swept from 0 V to 6 V with 0.1 V steps, while both V_{g1s} and V_{g2s} are swept from -1.2 V to 0.6 V with 0.2 V steps. Figure 2.8 shows the measured drain current of a 6x100 μm DGFET as a function of V_{ds} for different values of V_{g1s} when V_{g2s} is kept at 0 V.

Figure 2.8. The measured drain current for 6x100 μm DGFET as V_{ds} changes from 0V to 6V with 0.1V steps, V_{g1s} varies from -1V to 0.6V with 0.2V steps, and $V_{g2s}=0\text{V}$.

The extrinsic resistances are extracted using six different DC measurement setups.

These measurements are to be discussed in details in Chapter 3.

In the gate₁-source breakdown measurement, both the drain and gate₂ terminals are open-circuited while the source terminal is grounded and the current flowing out of gate₂, I_{g1} , is measured as the gate₁-source voltage is increased from 0 V in the negative direction. Figure 2.9 shows the measured gate₁ current of a 6x100 μm DGFET when V_{g1s} is swept from 0 V to -14 V when both gate₂ and drain terminals are open circuited.

In the gate₂-drain breakdown measurement, both the source and gate₁ terminals should be open-circuited while the drain terminal is grounded and the current flowing out of gate₂, I_{g2} , is measured as the gate₂-drain voltage is increased from 0 V in the negative

direction. Since the source terminals of all the DGFETs used in this work are grounded, the source can not be open-circuited. To overcome this problem, the author used the fact that the DGFETs under investigation are symmetric. In this case, it is assumed that measuring I_{g2} as the gate₂-drain voltage increases from 0 V in the negative direction when both gate₁ and the source are open-circuited is equivalent to measuring I_{g1} as gate₁-source voltage increases from 0 V in the negative direction when both gate₂ and the drain are open-circuited.

It was found that gate₁-drain breakdown measurement is unnecessary since the gate₂ diode will breakdown first and permanently damaging the DUT. Similarly, it is unnecessary to measure gate₂-source breakdown since the gate₁ diode will breakdown first and the DUT will be permanently damaged.

Figure 2.9. The measured current flowing out of gate₁ of 6x100 μ m DGFET as V_{g1s} is swept from 0V to -14V with -0.1V steps, when both gate₂ and the drain are open-circuited.

A schematic of the setup used for both the DC and the S-parameters measurements is shown in Figure 2.10. The two internal bias networks of the vector network analyzer (VNA) and an external bias network are used to supply bias to DUT. The equipment used in the setup are Anritsu 37369A vector network analyzer, an Hewlett Packard 4142B source and monitor unit (SMU), an Hewlett Packard 11612A bias network, a Temptronic temperature controller, and a Cascade probe station with 150 μm pico probes.

Figure 2.10. Schematic of the automated DC I-V and S-parameters measurement setup.

2.4.2 Correction of the DC Measurements

In the DC measurements just described, the voltages V_{g1s} , V_{g2s} , and V_{ds} are measured at the SMU. However, due to the resistance of the DC bias cables, the bias networks resistances, the resistance between the probe tips and the wafer, and the resistance of the length of transmission line connecting the probe pads to the device, the voltages at the device terminals are not equal to those measured by the SMU. To determine the voltages at the DUT terminals, the resistances of the three paths starting at

the SMU and ending at the DUT terminals must be measured. For this purpose, the author introduces a very simple, yet accurate, technique. This technique is summarized as follows:

1. The three on-wafer probes are set to contact the three RF short calibration structures. These structures are grounded using VIA holes.
2. Equal currents are swept from the three channels of the SMU into the three paths connecting the SMU to the device terminals and the voltages at the SMU are measured simultaneously.
3. The three path resistances are determined from the slopes of the measured I-V characteristics.

Figure 2.11 illustrates the measured I-V characteristics using the above technique. It is clear that the resistance of the path that contains an external bias network (port 3) is smaller than the resistances of the other two paths that contain the internal bias networks of the VNA since a shorter length of DC bias cable is used. From Figure 2.11 the values of R_{path1} , R_{path2} , and R_{path3} are 2.4Ω , 2.25Ω , and 0.73Ω , respectively.

Once the path resistances R_{path1} , R_{path2} , and R_{path3} are determined, the DUT terminal voltages are calculated using the following simple relationships derived using Figure 2.12.

$$V_{g1s} = V_{g1s, \text{SMU}} - I_{g1} R_{\text{path1}} \quad (2.3)$$

$$V_{g2s} = V_{g2s, \text{SMU}} - I_{g2} R_{\text{path2}} \quad (2.4)$$

$$V_{ds} = V_{ds, \text{SMU}} - I_d R_{\text{path3}} \quad (2.5)$$

where $V_{g1s, \text{SMU}}$, $V_{g2s, \text{SMU}}$ and $V_{ds, \text{SMU}}$ are the voltage values at the SMU terminals.

Figure 2.11. The measured voltages at the SMU when sweeping equal currents (1 mA to 20 mA with steps of 0.25 mA) into the three paths connecting the SMU to the DUT terminals.

Figure 2.12. Definition of control voltages in the DGFET model. $V_{g1s,SMU}$, $V_{g2s,SMU}$, and $V_{ds,SMU}$ are voltages defined at the source and monitor unit (SMU) while V_{g1s} , V_{g2s} , and V_{ds} are voltages defined at the device terminals.

2.4.3 Three-Port S-parameter Measurements

The three-port S-parameters are defined by:

$$b_1 = S_{11}a_1 + S_{12}a_2 + S_{13}a_3 \quad (2.6)$$

$$b_2 = S_{21}a_1 + S_{22}a_2 + S_{23}a_3 \quad (2.7)$$

$$b_3 = S_{31}a_1 + S_{32}a_2 + S_{33}a_3 \quad (2.8)$$

where a_i and b_i are, respectively, the incident and the reflected power waves at port i .

These are defined by:

$$a_i = \frac{V_i + Z_{oi}I_i}{2\sqrt{\text{Re}(Z_{oi})}} \quad \text{and} \quad b_i = \frac{V_i - Z_{oi}^*I_i}{2\sqrt{\text{Re}(Z_{oi})}} \quad (2.9)$$

where V_i denotes the voltage at port i , I_i denotes the current running into port i , $*$ denotes complex conjugate, and Z_{oi} denotes a reference impedance of port i .

A two-port vector network analyzer can be used to make three-port S-parameter measurements by terminating the third port with a known impedance (usually 50 ohm load). Applying this extra termination to the free port (referred to as the “third” port) reduces the DUT to a two-port, and a set of two-port S-parameters can be measured.

Three sets of two-port measurements are needed to get all 3-port S-parameter data. These are obtained in sequence, by moving the termination to port₃ and measuring port₁ to port₂, moving the termination to port₂ and measuring port₁ to port₃, and finally, by moving the termination to port₁ and measuring port₂ to port₃. In this work ports 1, 2 and 3 will refer to gate₁, gate₂ and drain ports, respectively.

2.4.4 Calibration of the Vector Network Analyzer

The SOLT calibration technique is used to calibrate the VNA for on-wafer S-parameter measurements. It utilizes four calibration standards: SHORT, OPEN, LOAD

and THRU, and provides a non-iterative solution. Calibration structures were designed and fabricated on the same wafer containing the DGFETs. The reference planes set by these calibration structures were intended to be at the device terminals. However, it was found that the reference planes set by these calibration structures were not precise. This was evident when extracting a negative value for the extrinsic inductance of gate₁. An explanation for this result is that the reference plane set for gate₁ terminal was beyond the position it should be, which added more length of transmission line that increased the phase of the measured S_{11} so that the small inductance of gate₁ looked negative. To overcome this problem, a Pico-probe CS-5 calibration wafer [35] is used to calibrate the VNA and to set the measurements reference planes at the probes tips. The reference planes are then shifted to the DUT terminals using the well-known techniques described in many references [36]. The reference planes set by this calibration wafer were very precise and repeatable which resulted in very accurate measurements.

2.4.5 Error Correction of the Measured S-parameters

The main sources of error introduced to the measured 3-port S-parameters when measured using a two-port vector network analyzer are:

1. The non-ideal termination of the free (third) port. This results from two causes: (i) the $50\ \Omega$ termination at the third port is not constant over the whole measurement frequency range; (ii) the $50\ \Omega$ termination is not directly connected to the device terminal, but through a length of transmission line, a probe, and a bias network. These two effects increase the magnitude of the reflection coefficient seen by the device terminal from its zero ideal value. An example of the magnitude of such reflection coefficient is shown in Figure 2.13.

2. Since the three-port S-parameters of the DUT are to be determined from three sets of two-port S-parameters measurements, probe placement accuracy is very essential for accurate measurements [37].

Figure 2.13. The measured magnitude of the reflection coefficient seen by the DUT when terminated by $50\ \Omega$ at the free (third) port.

2.4.5.1. Error correction for non-ideal third port termination

Since the third port termination is not ideal, an error is introduced in the measured S-parameters. Generally, the relation between measured and correct S-parameters is given by:

$$S_{ij}^m = S_{ij} + \frac{S_{ik}S_{ki}\Gamma_k}{1 - S_{kk}\Gamma_k} \quad (2.10)$$

where k is the port to be terminated, i and j are the ports connected to the network analyzer ($i, j \neq k$), Γ_k is the reflection coefficient of the termination, S_{ij}^m is the measured

2-port S-parameter, and S_{ij} is the correct S-parameter. The reflection coefficient Γ_k at port k is given by:

$$\Gamma_k = \frac{a_k}{b_k} = \frac{Z_k - Z_{ok}}{Z_k + Z_{ok}^*} \quad (2.11)$$

where Z_{ok} is the reference impedance of port k, and Z_k is the reference seen looking into the termination impedance of port k.

It is obvious from (2.11) that for correct determination of the three-port S-parameters through two-port measurements, Γ_k must be zero. This can be obtained by either using an ideal termination $Z_k = Z_{ok}$ which is typically impossible, or by redefining the reference impedance of the terminated port so that $Z_k = Z_{ok}$ which is known as the renormalization method.

Many renormalization techniques have been introduced in the literature to correct for the non-ideal termination of the third port [38,39]. In this work the closed form technique introduced by [39] is used. The algorithm is as follows:

- (i) Measure three sets of two-port S-parameters as described in Section 2.3.3.
- (ii) Measure the three reflection coefficients corresponding to the three-port terminations.
- (iii) Convert each of the 2-port S-parameters to R-parameters (called Gamma-R parameters in [39]) as follows:

$$R = (\Gamma^* + S)(I - \Gamma S)^{-1} \quad (2.12)$$

where Γ is a diagonal matrix containing the reflection coefficients of the corresponding terminations and I is a 2x2 identity matrix.

(iv) Fill the 3x3 Gamma-R matrix with the Gamma-R parameters generated from the individual sets of 2-port S-parameters in step (iii).

(v) Convert the 3x3 Gamma-R matrix back to S-parameters as follows:

$$S = (I + R\Gamma)^{-1} (R - \Gamma^*) \quad (2.13)$$

To verify the validity of this technique, the following procedures are followed:

- (i) A set of 3-port S-parameters is generated using the nonlinear simulator HPADS [40] and the DGFET model published in [21]. This set represents the correct S-parameters.
- (ii) Three sets of 2-port S-parameters are generated using the above FET model and “third” port terminations shown in Figure 2.14. These sets represent the measured S-parameters.
- (iii) Three sets of reflection coefficients of the “third” port terminations are generated.

The algorithm described in [39] is coded using LABVIEW software [41] and is used to generate the corrected 3-port S-parameters.

Figure 2.14. HPADS schematic of the non-ideal third port termination loads.

The technique showed very good efficiency that results in a dramatic reduction of the error introduced to the S-parameters. For example the maximum absolute error of the measured magnitude of S_{33} is reduced from 14% to 1.1%

2.4.5.2. Accuracy of probes positions

Great care was taken by the author to make sure that the probe positions are almost the same for the three sets of two-port S-parameters measurements.

To demonstrate this accuracy, the magnitude and phase of the reflection coefficient of gate₂ (S_{22}) of a 6x100 μm DGFET measured from two different setups over the frequency range of 0.5 GHz to 26.5 GHz (Setup₁: gate₁ is at port₁ of the VNA and gate₂ is at port₂ of the VNA, setup2: gate₂ is at port₁ of the VNA and the drain is at port₂ of the VNA) when both gates are biased with 10 mA current and $V_{ds}=0\text{V}$ are shown in Figures 2.15 and 2.16 respectively (this measurement is used to extract the extrinsic inductance of the DUT). It is clear from these Figures that the measured S_{22} is almost the same from the two different setups. The maximum relative errors in magnitude and phase of S_{22} at this bias point are 1.6% and ± 2 degrees, respectively.

Figure 2.15. Comparison between the measured magnitudes of the reflection coefficient at gate₂ terminal (S_{22}) from two different setups of a 6x100 μm DGFET over the frequency range of 0.5-26.5 GHz when both gates are biased with 10 mA current while $V_{ds}=0\text{V}$.

Figure 2.16. Comparison between the measured phase of the reflection coefficient at gate₂ terminal (S_{22}) from two different setups of a $6 \times 100 \mu\text{m}$ DGFET over the frequency range of 0.5-26.5 GHz when both gates are biased with 10 mA current while $V_{ds}=0\text{V}$.

2.4.6 Large-Signal Measurements

Load pull measurements are useful for investigating the nonlinear performance of active microwave devices. In this work these measurements are used to partially test the validity of the large-signal model of the DGFET. The fundamental (at 10 GHz) and the second harmonic (at 20 GHz) output powers of a $6 \times 100 \mu\text{m}$ DGFET are measured when terminating the drain with a conjugate matched load at different bias points. These measurements have been done for the author at Nortel Networks, Ottawa, Canada. Figure 2.17 shows a sample of these measurements when the DUT is biased at $V_{g1s} = 0 \text{ V}$, $V_{g2s} = 0 \text{ V}$, and $V_{ds} = 6 \text{ V}$.

Figure 2.17. The measured output power of the first two harmonics (fundamental measured at 10 GHz) of a 6x100 μm DGFET as the input power at gate₁ terminal is swept from -6 dBm to 8 dBm when the DUT is biased at $V_{g1s}=0\text{V}$, $V_{g2s}=0\text{V}$, and $V_{ds}=6\text{V}$.

CHAPTER 3

EXTRACTION OF THE DUAL-GATE GaAs MESFET EXTRINSIC PARAMETERS

3.1 Introduction

The DGFET is partitioned into an intrinsic DGFET, which includes all elements that depend on bias and signal level, and the remainder of the device, which includes all extrinsic elements that are assumed to be bias independent.

The extrinsic parameters (also called parasitic parameters) include extrinsic inductances, capacitances and resistances. The extrinsic parameters of the DGFET are shown in Figure 3.1. The inductors L_{g1} , L_{g2} , L_d , and L_s represent the extrinsic inductances of gate₁, gate₂, the drain, and the source terminals, respectively. The capacitors C_{pg1} , C_{pg2} and C_{pd} represent the pad capacitances of gate₁, gate₂ and drain respectively; C_{g1d} and C_{g2d} are the coupling capacitances between each gate and the drain; C_{g12} is the inter-gate coupling capacitance. The resistors R_{g1} , R_{g2} , R_d , and R_s represent the extrinsic resistances of gate₁, gate₂, the drain, and the source terminals, respectively.

In this work, the extrinsic capacitances and inductances are extracted from S-parameter measurements when the DGFET is operating in the cold regime, i.e. when the applied voltage between the drain and source is zero ($V_{ds}=0$). The extrinsic resistances are extracted using six DC measurement setups.

Figure 3.1. The equivalent circuit model of the Dual-Gate GaAs MESFET

3.2 Extraction of the Parasitic Resistances

3.2.1 Introduction

The extrinsic resistances of the DGFET are key parameters that affect the gain and the noise figure of the transistor. While several techniques for extracting the parasitic resistances of the SGFET have been reported [42-46], much less has been published to extract the extrinsic resistances of the DGFET [47,48,18,21]. The reported techniques make use of either DC or S-parameter measurements from which some relations between the unknown resistances are derived.

Extending the technique introduced by Dambrine *et al.* [45] to calculate the extrinsic resistances for a SGFET using S-parameter measurements, only five independent equations can be derived for the DGFET. Assuming common source connection, these equations are: (port 1 is gate₁, port 2 is gate₂ and port 3 is the drain)

$$\text{Re}[Z_{11}] = R_{g1} + \frac{n_1 V_T}{I_{g1}} + \frac{R_{c1}}{3} + R_s \quad (3.1)$$

$$\text{Re}[Z_{22}] = R_{g2} + \frac{n_2 V_T}{I_{g2}} + \frac{R_{c2}}{3} + R_{12} + R_{c1} + R_s \quad (3.2)$$

$$\text{Re}[Z_{33}] = R_d + R_{c2} + R_{12} + R_{c1} + R_s \quad (3.3)$$

$$\text{Re}[Z_{12}] = \text{Re}[Z_{13}] = \text{Re}[Z_{21}] = \text{Re}[Z_{31}] = \frac{R_{c1}}{2} + R_s \quad (3.4)$$

$$\text{Re}[Z_{23}] = \text{Re}[Z_{32}] = \frac{R_{c2}}{2} + R_{12} + R_{c1} + R_s \quad (3.5)$$

where R_{c1} and R_{c2} are the resistances of channel₁ and channel₂, respectively; R_{12} is the inter-gate resistance; n_1 and n_2 are the ideality factors of gate₁ and gate₂ Schottky barriers, respectively; V_T is the thermal voltage; I_{g1} and I_{g2} are the forward currents for gate₁ and gate₂, respectively.

Since there are seven unknown resistances to be extracted, two additional equations are required. Langrez *et al.* [47,48] assumed that the channel resistances are equal (which is not valid for non-symmetric devices) to reduce the number of unknowns. Even with this assumption, an additional equation is still required. Langrez *et al.* [47,48] did not show how they extracted the six unknown resistances by using only five independent equations.

Tsironis and Meierer [18] introduced DC measurements to extract the extrinsic resistances of the DGFET. When extracting R_s , R_d and R_{12} , the channel resistances were ignored. This assumption introduced large errors to the calculated extrinsic resistances since the channel resistances can be in the order of (or even larger than) R_s , R_d or R_{12} .

To extract the extrinsic resistances of the DGFET, Deng *et al.* [21] used the end-resistance method [49] to derive five independent equations and proposed to use other techniques to derive two additional independent equations. Using different techniques makes the extraction procedure complex. Furthermore, two of the five equations derived from the end-resistance technique are based on measurements performed when the source is floating. These measurements cannot be obtained for on-wafer devices that have sources grounded. Another drawback of the reported technique in [21] is that the forward bias and the non-forward bias values of the channel resistance are assumed to be equal.

In this work the author introduces simple, yet accurate, DC measurements that generate nine independent equations to be used to determine the seven parasitic resistances of the DGFET. Each channel resistance is allowed to have two different values with and without forward bias applied to its controlling gate, resulting in nine unknowns. All the measurements are performed when the source is grounded which make this technique suitable for modeling on-wafer DGFETs whose sources are grounded.

3.2.2 Extraction Procedure

The basic model of a DGFET is a cascode connection of two single-gate MESFETs, FET_1 and FET_2 [3]. The DC equivalent circuit of the cold DGFET when both gates are forward biased is shown in Figure 3.2. [21].

Using six different DC measurements, nine independent relations between the nine unknown resistance values are generated by using the end-resistance technique [49] as follows:

Figure 3.2. The DC equivalent circuit of cold DGFET with both gates forward biased [21].

In the first measurement setup, a current I_{g1} is forced to sweep through gate₁, while at the same time both gate₂ and the drain are left open and the source is grounded. The voltage at gate₁ and the drain are measured simultaneously and given by:

$$\frac{\Delta V_{g1}}{\Delta I_{g1}} = R_{g1} + \frac{n_1 V_T}{I_{g1}} + \frac{R_{c1}^f}{3} + R_s \quad (3.6)$$

$$\frac{V_d}{I_{g1}} = \frac{R_{c1}^f}{2} + R_s \quad (3.7)$$

where R_{c1}^f is channel₁ resistance when gate₁ is forward biased. Equation (3.6) shows a straight line for $\Delta V_{g1}/\Delta I_{g1}$ vs. $1/I_{g1}$ characteristics with $n_1 V_T$ as the slope and $R_{g1} + R_{c1}^f/3 + R_s$ as the intercept point.

The second measurement setup is similar to the first setup where a current I_{g2} is forced to sweep through gate₂, while at the same time both gate₁ and the drain are left

open and the source is grounded. The voltages at gate₂ and the drain are measured simultaneously. It can be shown that:

$$\frac{\Delta V_{g2}}{\Delta I_{g2}} = R_{g2} + \frac{n_2 V_T}{I_{g2}} + \frac{R_{c2}^f}{3} + R_{l2} + R_{c1} + R_s \quad (3.8)$$

$$\frac{V_d}{I_{g2}} = \frac{R_{c2}^f}{2} + R_{l2} + R_{c1} + R_s \quad (3.9)$$

where R_{c2}^f is channel₂ resistance when gate₂ is forward biased. Equation (3.8) shows a straight line for $\Delta V_{g2}/\Delta I_{g2}$ vs. $1/I_{g2}$ characteristics with $n_2 V_T$ as the slope and $R_{g2} + R_{c2}^f/3 + R_{l2} + R_{c1} + R_s$ as the intercept point.

In the third measurement setup, a current I_{g1} is forced to sweep through gate₁, while a second current source sinks a current equals to gate₁ current, I_{g1} , out of the drain. At the same time gate₂ is left open and the source is grounded. In this case, no current will flow to the source. The voltages at the drain is measured and given by:

$$\frac{|V_d|}{I_{g1}} = \frac{R_{c1}^f}{2} + R_{l2} + R_{c2} + R_d \quad (3.10)$$

In the fourth measurement setup, a current I_{g2} is forced to sweep through gate₂, while a second current source sinks a current equals to gate₂ current, I_{g2} , out of the drain. At the same time gate₁ is left open and the source is grounded. No current will flow to the source. The voltages at both gate₂ and the drain are measured simultaneously. It can be shown that:

$$\frac{\Delta(V_{g2} - V_d)}{\Delta I_{g2}} = R_{g2} + \frac{n_2 V_T}{I_{g2}} + \frac{R_{c2}^f}{3} + R_d \quad (3.11)$$

$$\frac{|V_d|}{I_{g2}} = \frac{R_{c2}^f}{2} + R_d \quad (3.12)$$

Equation (3.11) shows a straight line for $\Delta(V_{g2} - V_d)/\Delta I_{g2} - (1/I_{g2})$ characteristics with $n_2 V_T$ as the slope and $R_{g2} + R_{c2}^f/3 + R_d$ as the intercept point.

In the fifth measurement setup, a current I_{g1} is forced to sweep through gate₁, while a second current source sinks half of this current out of the drain. At the same time gate₂ is left open and the source is grounded. The voltage at the drain is measured. In this case, the source current equals half of gate₁ current. Because FET₁ is driven symmetrically, no current will flow through R_{c1} and the drain voltage is given by:

$$\frac{2|V_d|}{I_{g1}} = R_{l2} + R_{c2} + R_d - R_s \quad (3.13)$$

The sixth measurement setup is similar to the fifth setup. In this setup, a current I_{g2} is forced to sweep through gate₂, while a second current source sinks half of this current out of the drain. At the same time gate₁ is left open and the source is grounded. The drain voltage is measured. Again, the source current I_s equals half of gate₂ current. Because FET₂ is driven symmetrically, no current will flow through R_{c2} . The drain voltage can be written as:

$$\frac{2V_d}{I_{g1}} = R_{l2} + R_{c1} + R_s - R_d \quad (3.14)$$

Equations (3.6)-(3.14) are used to extract all the nine unknown resistance values.

3.2.3 Experimental Results

The above technique is applied to characterize the ten DGFETs described in Table 2.1. The extracted extrinsic resistances of these transistors are shown in Table 3.1.

Table 3.1. The extracted extrinsic resistances of different DGFETs.

	Device	$R_s(\Omega)$	$R_{c1}(\Omega)$	$R_{l2}(\Omega)$	$R_{c2}(\Omega)$	$R_d(\Omega)$	$R_{g1}(\Omega)$	$R_{g2}(\Omega)$
1	1x50 μm	16.3	16.2	33	16.1	16.2	21.8	25
2	2x50 μm	8.2	8	16	8	8.1	11.35	12.3
3	2x100 μm	4.2	4.1	8.2	4.1	4.1	11.25	12.2
4	4x50 μm	4.2	4.23	8.5	4.28	4.16	5.4	5.87
5	6x50 μm	2.87	2.8	5.6	2.82	2.8	3.57	3.9
6	4x100 μm	2.37	2.1	4.3	2.17	2.34	5.6	5.88
7	6x100 μm	1.44	1.4	2.82	1.4	1.43	3.6	3.95
8	6x50 μm	3.55	2.9	5.7	2.8	2.81	3.6	3.93
9	6x50 μm	4.2	2.9	5.54	2.8	2.78	3.56	3.94
10	6x50 μm	4.85	3	5.65	2.78	2.78	3.56	3.9

It can be seen that the scaling rules versus gate width are generally verified. The gate resistances scale to the number of gate fingers. This is similar to the results published in [48]. It is also clear that the source resistance, which includes bulk resistance of the region from the source to gate₁, increases with the distance L_{g1s} , as shown by the 6x50 μm devices (5), (8), (9), and (10).

It was found that if $R_c = R_c^f$ is assumed, the extracted source and drain resistances are under estimated. Since the channel resistance is smaller under forward bias condition, (3.7) and (3.12) show that the calculated source and drain resistances will be smaller than their real values. For example, if $R_c = R_c^f$ is assumed, the extracted resistances of device (5) are $R_s=1.7 \Omega$, $R_{c1}=3 \Omega$, $R_{l2}=5.67 \Omega$, $R_{c2}=2.97 \Omega$, $R_d=1.64 \Omega$, $R_{g1}=3.96 \Omega$ and $R_{g2}=4.1 \Omega$. In comparison with the values for of device (5) in Table 3.1, the source and drain resistance values are affected more than the other parasitic resistances.

It is useful to compare the extrinsic resistance values extracted by the above technique to those extracted from S-parameters measurements. Equations (3.1)-(3.5) are solved for a $6 \times 100 \mu\text{m}$ DGFET (which is a symmetric device) by assuming that $R_s=R_d$ and $R_{c1}=R_{c2}$. Since the Z-parameters in (3.1)-(3.5) are measured when both gates of the DGFET are forward biased with high currents [45, 47], R_{c1} and R_{c2} in these equations should be replaced by R_{c1}^f and R_{c2}^f , respectively. The real parts of the Z-parameters of a $6 \times 100 \mu\text{m}$ DGFET over the frequency range 0.5 GHz-7.26 GHz when the device is biased at $I_{g1}=I_{g2}= 10 \text{ mA}$ and $V_{ds}=0\text{V}$ are shown in Figure 3.3. The extracted extrinsic resistances are: $R_s=R_d=1.41 \Omega$, $R_{c1}^f = R_{c2}^f=0.31 \Omega$, $R_{l2}=2.83 \Omega$, $R_{g1}=3.63 \Omega$, and $R_{g2}=3.89 \Omega$. These values are very close to the results shown in Table 3.1 for the $6 \times 100 \mu\text{m}$ DGFET, which confirms the above technique.

Figure 3.3. The real part of the measured Z-parameters of a $6 \times 100 \mu\text{m}$ DGFET over the frequency range 0.5GHz-7.26 GHz when the device is biased at $I_{g1}=I_{g2}= 10 \text{ mA}$ and $V_{ds}=0\text{V}$.

3.3 Extraction of the Parasitic Capacitances

When the DGFET is operating in the cold regime ($V_{ds} = 0$ V) and the two gates are largely reverse biased ($V_{g1s} < V_{p1}$ and $V_{g2s} < V_{p2}$), with the three terminals (gate₁, gate₂ and drain) opened, then the intrinsic part of the device is equivalent to a pure passive network including only the edge capacitance C_b related to each gate. The equivalent scheme of the DGFET under these conditions is shown in Figure 3.4 [47, 48]. The contribution of the series elements (inductances and resistances) is found to be only in the third-order terms versus frequency in the Y-parameters, thus will be neglected at low frequency range [47].

Figure 3.4. Equivalent scheme of DGFET in the cold regime under largely reverse bias.

The imaginary part of the DGFET three-port Y-parameters under these bias conditions can be written as follows:

$$\text{Im}[Y_{11}] = \omega(C_{pg1} + 3C_b/2 + C_{g1d} + C_{g12}) \quad (3.15)$$

$$\text{Im}[Y_{12}] = \text{Im}[Y_{21}] = -\omega(C_b/2 + C_{g12}) \quad (3.16)$$

$$\text{Im}[Y_{13}] = \text{Im}[Y_{31}] = -\omega C_{g1d} \quad (3.17)$$

$$\text{Im}[Y_{22}] = \omega(C_{pg2} + 3C_b/2 + C_{g2d} + C_{g12}) \quad (3.18)$$

$$\text{Im}[Y_{23}] = \text{Im}[Y_{32}] = -\omega(C_b + C_{g2d}) \quad (3.19)$$

$$\text{Im}[Y_{33}] = \omega(C_{pd} + C_b + C_{g1d} + C_{g2d}) \quad (3.20)$$

As suggested by (3.15)-(3.20), the plot of the imaginary part of the Y-parameters versus frequency ($\omega = 2\pi f$) should be straight line. This is confirmed from Figure 3.5 that shows plots of the imaginary part of the Y-parameters (determined from the measured S-parameters through well known transformations) of a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -4 \text{ V}$, $V_{g2s} = -4 \text{ V}$, and $V_{ds} = 0 \text{ V}$.

To solve for the seven unknown extrinsic capacitances, one more equation is needed. Alternatively, if one extrinsic capacitance is to be neglected, (3.15)-(3.20) can be solved as an under-determined system of equations. Obviously, all the three-port Y-parameters are used in (3.15)-(3.20) so there cannot be another equation. On the other hand, the above six equations represent enough constraints to estimate the seven unknown capacitances with good accuracy. Labview [41] was used to optimize the constrained system of equations (3.15)-(3.20) to determine the unknown seven extrinsic capacitances for the first seven DGFETs described in Table 2.1. It was concluded that C_{g12} is always very small and can be neglected. For example, the value of C_{g12} for the

biggest DGFET (6x100 μm) is found to be 3.23 fF. This is the same conclusion reached by Langrez *et al.* [47, 48].

Figure 3.5. The imaginary part of the Y-parameters of a 6x100 μm DGFET biased at $V_{g1s}=-4$ V, $V_{g2s}=-4$ V, and $V_{ds}=0$ V.

Neglecting C_{g12} from equations (3.15), (3.16), and (3.17), the DGFET extrinsic capacitances are given by:

$$C_{g1d} = \frac{-\text{Im}[Y_{13}]}{\omega} \quad (3.21)$$

$$C_b = \frac{-2\text{Im}[Y_{12}]}{\omega} \quad (3.22)$$

$$C_{g2d} = \frac{-\text{Im}[Y_{23}]}{\omega} - C_b \quad (3.23)$$

$$C_{pg1} = \frac{\text{Im}[Y_{11}]}{\omega} - \frac{3}{2}C_b - C_{g1d} \quad (3.24)$$

$$C_{pg2} = \frac{\text{Im}(Y_{22})}{\omega} - \frac{3}{2}C_b - C_{g2d} \quad (3.25)$$

$$C_{pd} = \frac{\text{Im}[Y_{33}]}{\omega} - C_b - C_{g1d} - C_{g2d} \quad (3.26)$$

The extracted extrinsic capacitances for devices (1)-(7) described in Table 2.1 using (3.21)-(3.26) are shown in Table 3.2.

Table 3.2. The extracted extrinsic capacitances of different DGFETs.

Device		C_{pg1} (fF)	C_{pg2} (fF)	C_{pd} (fF)	C_{g1d} (fF)	C_{g2d} (fF)
1	1x50 μm	1.17	1.13	3.13	3.4	4.98
2	2x50 μm	3.87	3.87	6.9	5.3	7.54
3	2x100 μm	9.67	9.46	15.5	9.28	12.38
4	4x50 μm	10.1	9.9	14.9	10.1	12.8
5	6x50 μm	15.09	14.89	24	12.67	16.92
6	4x100 μm	20.85	20.38	32.2	16.6	21.79
7	6x100 μm	31.8	31.48	47.51	23.66	29.59

The following conclusions can be made from the results in Table 3.2:

1. The extrinsic capacitances C_{pg1} and C_{pg2} of both gates are approximately equal.
2. C_{g2d} is always larger than C_{g1d} since gate₂ is closer to the drain than gate₁.
3. The extrinsic capacitances of devices (3) and (4) are equal since they have the same total gate width (200 μm).
4. To establish scaling rules, the capacitances are plotted versus the total gate width in Figure 3.6. It can be seen that the extracted extrinsic capacitances scale with the total DGFET gate width.

Figure 3.6. The variation of the extrinsic capacitances with the total gate width.

3.4 Extraction of the Parasitic Inductances

Under the cold regime ($V_{ds}=0$), with both gates largely forward biased ($I_{g1}=I_{g2}$), FET_1 and FET_2 can be modeled as resistive networks. Under these bias conditions, the imaginary part of the DGFET three-port Z-parameters can be written as follows [47, 48, 21]:

$$\text{Im}[Z_{11}] = \omega (L_{g1} + L_s) \quad (3.27)$$

$$\text{Im}[Z_{22}] = \omega (L_{g2} + L_s) \quad (3.28)$$

$$\text{Im}[Z_{33}] = \omega (L_d + L_s) \quad (3.29)$$

$$\text{Im}[Z_{12}] = \omega L_s \quad (3.30)$$

Equations (3.27)-(3.30) show straight lines for $\text{Im}[Z_{11}]-\omega$, $\text{Im}[Z_{22}]-\omega$, $\text{Im}[Z_{33}]-\omega$, and $\text{Im}[Z_{12}]-\omega$ characteristics, respectively. This is verified from Figure 3.7 that shows plots of the imaginary part of the Z-parameters (determined from the measured S-parameters through well known transformations) of a $6 \times 100 \mu\text{m}$ DGFET biased at $I_{g1} = I_{g2} = 10 \text{ mA}$, and $V_{ds} = 0 \text{ V}$.

Figure 3.7. The imaginary part of the Z-parameters of a $6 \times 100 \mu\text{m}$ DGFET biased at $I_{g1}=I_{g2}= 10 \text{ mA}$ and $V_{ds}=0 \text{ V}$.

From (3.27)-(3.30), the DGFET extrinsic inductances are given by:

$$L_{g1} = \frac{\text{Im}[Z_{11}] - \text{Im}[Z_{12}]}{\omega} \quad (3.31)$$

$$L_{g2} = \frac{\text{Im}[Z_{22}] - \text{Im}[(Z_{12})]}{\omega} \quad (3.32)$$

$$L_d = \frac{\text{Im}[Z_{33}] - \text{Im}[(Z_{12})]}{\omega} \quad (3.33)$$

$$L_s = \frac{\text{Im}[Z_{12}]}{\omega} \quad (3.34)$$

The extracted extrinsic inductances of a 6x100 μm DGFET using (3.31)-(3.34) are shown in Figure 3.6. The two gates of the device are biased with a 10 mA current while $V_{ds} = 0$ V.

Figure 3.8. The extrinsic inductances of a 6x100 μm DGFET biased at $I_{g1}=I_{g2}= 10$ mA and $V_{ds}=0$ V.

The average values of the extracted extrinsic inductances for devices (1)-(7) described in Table 2.1 using (3.31)-(3.34) are shown in Table 3.3.

Table 3.3. The extracted extrinsic inductances of different DGFETs.

Device		L_{g1} (pH)	L_{g2} (pH)	L_d (pH)	L_s (pH)
1	1x50 μm	130	148	99.4	22.4
2	2x50 μm	110	172	120	47
3	2x100 μm	94.6	179	141	30.2
4	4x50 μm	105	167	113	56
5	6x50 μm	102	157	108	63.8
6	4x100 μm	88.3	166	125	39
7	6x100 μm	83.7	176	145	44.6

The extrinsic inductance values are dependent on the DGFET layout [47, 48]. This can be observed from the results shown in Table 3.3. The following conclusions can be made from the results in Table 3.3:

1. The L_s values increase when the total gate width decreases for a given number of gate fingers. This is explained by the fact that the width of the line between the via hole and the source pad decreases when the total gate width decreases, and so a more inductive behavior appears.
2. For a given gate finger width, L_s values increase as the number of fingers increase because of air bridges.
3. L_s and L_d values are always greater for multifinger-gate devices as compared to the single one (device (1)).
4. For all the devices, L_{g2} values are always greater than L_{g1} values. This is due to the presence of a narrow metal line (5 μm wide) connecting gate₂ fingers to

the $50\ \Omega$ transmission line leading to gate₂ pad, as shown in Figure 3.9 for a $6 \times 100\ \mu\text{m}$ DGFET.

Figure 3.9. The layout of the $6 \times 100\ \mu\text{m}$ DGFET.

3.5 De-Embedding the Intrinsic DGFET

Once all the extrinsic elements have been extracted, the intrinsic DGFET can be de-embedded. First, the measured S-parameters are converted to Z-parameters (Z_m). The intrinsic Z-parameters (Z_i) of the intrinsic DGFET are then given by

$$Z_i = \left[\left((Z_m - Z_{ind})^{-1} - Y_{cap} \right)^{-1} - R_{res} \right] \quad (3.35)$$

where

$$Z_{\text{ind}} = j\omega \begin{bmatrix} L_{g1} + L_s & L_s & L_s \\ L_s & L_{g2} + L_s & L_s \\ L_s & L_s & L_d + L_s \end{bmatrix} \quad (3.36)$$

$$Y_{\text{cap}} = j\omega \begin{bmatrix} C_{pg1} + C_{g1d} & 0 & C_{g1d} \\ 0 & C_{pg2} + C_{g2d} & C_{g2d} \\ C_{g1d} & C_{g2d} & C_{pd} + C_{g1d} + C_{g2d} \end{bmatrix} \quad (3.37)$$

$$R_{\text{res}} = \begin{bmatrix} R_{g1} + R_s & R_s & R_s \\ R_s & R_{g2} + R_s & R_s \\ R_s & R_s & R_d + R_s \end{bmatrix} \quad (3.38)$$

All the intrinsic elements are then determined from the intrinsic Z-parameters according to the small-signal models described in Chapters 4 and 5.

CHAPTER 4

CASCODE SMALL-SIGNAL MODEL OF THE DUAL-GATE GaAs MESFET

4.1 Introduction

The basic model of a DGFET is a cascode connection of two single-gate FET parts, FET^I and FET^{II} [3]. The typical intrinsic small-signal model of a DGFET is shown in Figure 4.1.

Figure 4.1. The small-signal equivalent circuit of the intrinsic DGFET.

In Figure 4.1, G_1 , G_2 , D , and S represent gate₁, gate₂, the drain and the source terminals, respectively. C_{gs} , C_{gd} and C_{ds} are, respectively, the gate-source capacitance, the

gate-drain capacitance and the drain-source capacitance. g_m , g_{ds} and τ are the transconductance, output conductance and transconductance delay, respectively. R_i and R_{12} are the internal charging resistor for C_{gs} and the inter-gate resistance respectively.

Scott and Minasian [22] derived relationships between the three-port Z-parameters of the DGFET (Z) and the individual two-port Z-parameters of the two single-gate FETs (Z^I and Z^{II}). Except for Z_{22}^I , the two-port Z-parameters of FET^I are given explicitly from the three-port Z-parameters of the DGFET. To separate Z_{22}^I , Scott and Minasian [22] assumed that $Z_{22}^I \approx Z_{23}$, up to moderate frequencies. Extracting the elements of FET^I from its two-port Z-matrix, Scott and Minasian [22] found that the elements of FET^{II} can be evaluated analytically from the three-port Y-parameters of DGFET provided that the transconductance of FET^{II} (g_{m2}) is available. Measuring g_{m2} by using the model presented by Minasian [50], Scott and Minasian [22] derived expressions for extracting the elements of FET^{II} under the assumptions that:

$$1 + j\omega C_{gs_1} R_{i_1} \approx 1, \text{ and } 1 + j\omega C_{gs_2} R_{i_2} \approx 1$$

In this Chapter, an analytical expression of Z_{22}^I that can be evaluated from the measured three-port Z-parameters of the DGFET is derived. Once Z_{22}^I is evaluated, the Z-matrix of each individual FET part is separated and the intrinsic elements of each FET can be evaluated analytically from the analytical model developed for single-gate MESFET.

4.2 Derivation of Z_{22}^I Expression

For simplicity, Figure 4.2 will be used where the current sources and the admittances of each branch of the small-signal model pictured in Figure 4.1 are shown, and given by the following equations:

$$Y_1 = \frac{\omega^2 R_{i_1} C_{gs_1}^2}{E_1} + j \frac{\omega C_{gs_1}}{E_1} \quad (4.1)$$

$$Y_2 = j\omega C_{gd_1} \quad (4.2)$$

$$Y_3 = g_{d_1} + j\omega C_{ds_1} \quad (4.3)$$

$$Y_4 = \frac{1}{R_{l_2}} \quad (4.4)$$

$$Y_5 = g_{d_2} + j\omega C_{ds_2} \quad (4.5)$$

$$Y_6 = j\omega C_{gd_2} \quad (4.6)$$

$$Y_7 = \frac{\omega^2 R_{i_2} C_{gs_2}^2}{E_2} + j \frac{\omega C_{gs_2}}{E_2} \quad (4.7)$$

$$G_1 = G_{1r} + jG_{1i} \quad (4.8)$$

$$G_2 = G_{2r} + jG_{2i} \quad (4.9)$$

where

$$E_1 = 1 + \omega^2 R_{i_1}^2 C_{gs_1}^2 \quad (4.10)$$

$$E_2 = 1 + \omega^2 R_{i_2}^2 C_{gs_2}^2 \quad (4.11)$$

$$G_{1r} = \frac{g_{m_1}}{E_1} \left(\cos(\omega \tau_1) - \omega R_{i_1} C_{gs_1} \sin(\omega \tau_1) \right) \quad (4.12)$$

$$G_{1i} = \frac{-g_{m1}}{E_1} (\omega R_{i1} C_{gs1} \cos(\omega \tau_1) + \sin(\omega \tau_1)) \quad (4.13)$$

$$G_{2r} = \frac{g_{m2}}{E_2} (\cos(\omega \tau_2) - \omega R_{i2} C_{gs2} \sin(\omega \tau_2)) \quad (4.14)$$

$$G_{2i} = \frac{-g_{m2}}{E_2} (\omega R_{i2} C_{gs2} \cos(\omega \tau_2) + \sin(\omega \tau_2)) \quad (4.15)$$

Figure 4.2. The simplified equivalent circuit of the DGFET used for analysis.

When the inter-gate resistance R_{12} is taken into consideration, the three-port Z-parameters derived by Scott and Minasian [22] are modified as follows:

$$Z_{11} = Z_{11}^I$$

$$Z_{12} = Z_{12}^I$$

$$Z_{21} = Z_{21}^I$$

$$Z_{13} = Z_{12}^I$$

$$Z_{22} = Z_{22}^I + Z_{11}^{II} + R_{12}$$

$$Z_{23} = Z_{22}^I + Z_{12}^{II} + R_{12}$$

$$Z_{31} = Z_{21}^I$$

$$\begin{aligned}
Z_{32} &= Z_{22}^I + Z_{21}^{II} + R_{12} \\
Z_{33} &= Z_{22}^I + Z_{22}^{II} + R_{12}
\end{aligned} \tag{4.16}$$

The two-port Y and Z-matrices of FET^I are given by:

$$Y^I = \begin{bmatrix} Y_1 + Y_2 & -Y_2 \\ G_1 - Y_2 & Y_2 + Y_3 \end{bmatrix} \tag{4.17}$$

$$Z^I = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22}^I \end{bmatrix} \tag{4.18}$$

Since $Y = Z^{-1}$, the following relationship results:

$$Y_2 = \frac{Z_{12}}{\det(Z^I)} \tag{4.19}$$

where

$$\det(Z^I) = Z_{11}Z_{22}^I - Z_{12}Z_{21} \tag{4.20}$$

Similarly the two-port Y and Z-matrices of FET^{II} are:

$$Y^{II} = \begin{bmatrix} Y_6 + Y_7 & -Y_6 \\ G_2 - Y_6 & Y_5 + Y_6 \end{bmatrix} \tag{4.21}$$

$$Z^{II} = \begin{bmatrix} Z_{22} - R_{12} - Z_{22}^I & Z_{23} - R_{12} - Z_{22}^I \\ Z_{32} - R_{12} - Z_{22}^I & Z_{33} - R_{12} - Z_{22}^I \end{bmatrix} \tag{4.22}$$

It can be shown that:

$$Y_6 = \frac{Z_{23} - R_{12} - Z_{22}^I}{\det(Z^{II})} \tag{4.23}$$

where

$$\det(Z^{II}) = \alpha_1 - \alpha_2 Z_{22}^I \tag{4.24}$$

$$\alpha_1 = (Z_{22} - R_{12})(Z_{33} - R_{12}) - (Z_{23} - R_{12})(Z_{32} - R_{12}) \tag{4.25}$$

$$\alpha_2 = Z_{22} + Z_{33} - Z_{23} - Z_{32} \quad (4.26)$$

It is clear from (4.2) and (4.6) that the real parts of both Y_2 and Y_6 are zeros. Solving

$\text{Re}(Y_2) = 0$ gives:

$$k_1 \text{Re}(Z_{22}^I) - k_2 \text{Im}(Z_{22}^I) = k_3 \quad (4.27)$$

where

$$k_1 = \text{Re}(Z_{11}) \text{Re}(Z_{12}) + \text{Im}(Z_{11}) \text{Im}(Z_{12}) \quad (4.28)$$

$$k_2 = \text{Im}(Z_{11}) \text{Re}(Z_{12}) - \text{Re}(Z_{11}) \text{Im}(Z_{12}) \quad (4.29)$$

$$k_3 = \text{Re}(Z_{12}) \text{Re}(Z_{12} Z_{21}) + \text{Im}(Z_{12}) \text{Im}(Z_{12} Z_{21}) \quad (4.30)$$

Solving $\text{Re}(Y_6) = 0$ gives:

$$\beta_1 (\text{Re}^2(Z_{22}^I) + \text{Im}^2(Z_{22}^I)) - \beta_2 \text{Re}(Z_{22}^I) + \beta_3 \text{Im}(Z_{22}^I) + \beta_4 = 0 \quad (4.31)$$

where

$$\beta_1 = \text{Re}(\alpha_2) \quad (4.32)$$

$$\beta_2 = \text{Re}(\alpha_2) \text{Re}(Z_{23} - R_{12}) + \text{Re}(\alpha_1) + \text{Im}(\alpha_2) \text{Im}(Z_{23}) \quad (4.33)$$

$$\beta_3 = \text{Im}(\alpha_2) \text{Re}(Z_{23} - R_{12}) - \text{Re}(\alpha_2) \text{Im}(Z_{23}) - \text{Im}(\alpha_1) \quad (4.34)$$

$$\beta_4 = \text{Re}(\alpha_1) \text{Re}(Z_{23} - R_{12}) + \text{Im}(\alpha_1) \text{Im}(Z_{23}) \quad (4.35)$$

Solving (4.27) and (4.31) results in:

$$\text{Re}[Z_{22}^I] = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \quad (4.36)$$

$$\text{Im}[Z_{22}^I] = \frac{k_1 \text{Re}(Z_{22}^I) - k_3}{k_2} \quad (4.37)$$

where

$$A = \beta_1 \left(1 + \left(\frac{k_1}{k_2} \right)^2 \right) \quad (4.38)$$

$$B = \beta_3 \left(\frac{k_1}{k_2} \right) - \beta_2 - 2\beta_1 \frac{k_1 k_3}{k_2^2} \quad (4.39)$$

$$C = \beta_1 \left(\frac{k_3}{k_2} \right)^2 - \beta_3 \left(\frac{k_3}{k_2} \right) + \beta_4 \quad (4.40)$$

Once Z_{22}^I is evaluated using (4.36)-(4.40), the two-port Z-matrix of each individual FET part is separated using (4.16). Converting the Z-matrix into a Y-matrix, the intrinsic elements of each FET part are evaluated using the well-established analytical model of a single-gate FET [51] given by:

$$C_{gd} = -\frac{\text{Im}[Y_{12}]}{\omega} \quad (4.41)$$

$$C_{ds} = \frac{\text{Im}[Y_{22}] + \text{Im}[Y_{12}]}{\omega} \quad (4.42)$$

$$C_{gs} = \left(\frac{\text{Im}[Y_{11}] + \text{Im}[Y_{12}]}{\omega} \right) \left(1 + \frac{(\text{Re}[Y_{11}])^2}{(\text{Im}[Y_{11}] + \text{Im}[Y_{12}])^2} \right) \quad (4.43)$$

$$R_i = \frac{\text{Re}[Y_{11}]}{(\text{Im}[Y_{11}] + \text{Im}[Y_{12}])^2 + (\text{Re}[Y_{11}])^2} \quad (4.44)$$

$$g_m = \sqrt{((\text{Re}[Y_{21}])^2 + (\text{Im}[Y_{21}] - \text{Im}[Y_{12}])^2) (1 + \omega^2 C_{gs}^2 R_i^2)} \quad (4.45)$$

$$\tau = \frac{1}{\omega} \arcsin \left(\frac{\text{Im}[Y_{12}] - \text{Im}[Y_{21}] - \omega C_{gs} R_i \text{Re}[Y_{21}]}{g_m} \right) \quad (4.46)$$

$$g_{ds} = \text{Re}[Y_{22}] \quad (4.47)$$

4.3 Verification of the Cascode Small-Signal Model

The above model is used to extract the intrinsic elements of different DGFETs over a wide range of bias conditions. The calculated S-parameters using this model were in very good agreement with the measured data over a wide frequency range of 0.5 GHz-26.5 GHz. Figure 4.3 shows a comparison between the calculated and the measured S-parameters of a 6x100 μm DGFET biased at V_{g1s} of -0.2 V, V_{g2s} of -0.2 V, and V_{ds} of 3 V. It is clear that the model accurately follows the measured data. Good agreement was also achieved for different devices at many other bias points.

Although the above model succeeded to model the small-signal behavior of the DGFET, complications appeared when attempting to use this model to develop a large-signal model of the DGFET.

To develop a large-signal model of the DGFET, the small-signal model parameters are extracted over a wide range of bias points in the I-V plane. The parameters of FET^{I} and FET^{II} are then represented by functions of the drain-source voltage and the gate-source voltage applied on that FET part. In applying this technique to develop a large-signal model of the DGFET using the above small-signal model, two complications arise. **Firstly**, the voltage at the inaccessible node introduced between the two FET parts is difficult to determine [20,27]. Knowledge of this node voltage is necessary to determine the intrinsic controlling voltages of each FET part. Tsironis and Meierer [20] developed a graphical technique based on DC measurements to construct a nomogram at each bias point to determine the controlling voltages of FET^{I} and FET^{II} . Knowing that the DGFET large-signal model in this work is to be extracted over 1815 bias points (11 bias point for V_{g1s} , 11 bias point for V_{g2s} , and 15 bias point for V_{ds}),

developing a graphical nomogram at each bias point is completely unpractical. Allam *et al.* [27] used a numerical technique to solve for the voltage at the inaccessible node introduced between FET^I and FET^{II} . Using numerical techniques will largely increase the simulation time when using the developed large-signal model. **Secondly**, since each of the nonlinear capacitors in the small-signal model is to be represented by a bivariate charge source in the large-signal model, the consistency between the small-signal and the large-signal models requires that each nonlinear capacitor in the small-signal model must be in parallel with a transcapacitor [52]. The small-signal model described above does not include such transcapacitors, which makes it inconsistent with its counterpart large-signal model.

To overcome these problems, a consistent small-signal model of the DGFET is developed. The new model does not deal with the DGFET as a cascode connection of two single-gate FET parts, but as a four-port device. The new small-signal model is derived from a general large-signal model of the DGFET, which makes it consistent with the large-signal model. The model parameters are extracted directly from the measured S-parameters. The new model is described in details in Chapter five.

Figure 4.3. Measured (x) and calculated (solid) three-port S-parameters of a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2 \text{ V}$, $V_{g2s} = -0.2 \text{ V}$, and $V_{ds} = 3 \text{ V}$ over the frequency range 0.5-26.5 GHz.

CHAPTER 5

CONSISTENT SMALL-SIGNAL MODEL OF THE DUAL-GATE GaAs MESFET

5.1 Introduction

The DGFET large-signal model in this work is to be generated from the use of small-signal S-parameter data measured at various bias points in the I-V plane. From the S-parameter data, small-signal linear models at each bias point are obtained using a direct extraction procedure. The variations of each element in the small-signal model with respect to its controlling voltages are then implemented in a large-signal model. However, one of the major problems associated with this procedure is the discrepancy that occurs when attempting to regenerate the original small-signal model at each bias from the large-signal model.

To address this discrepancy, recall that the definition of capacitance is given by:

$$C = \frac{dQ}{dV} \quad (5.1)$$

where Q is the charge on the capacitor terminals and V is the voltage difference between the two terminals. Knowing that the capacitors in the cascode small-signal model described in Chapter 4, are function of two voltages, (5.1) can be written as:

$$C(V_L, V_R) = \frac{\partial Q(V_L, V_R)}{\partial V_L} \quad (5.2)$$

where V_L and V_R are defined as the voltage across the capacitor's terminals (local voltage) and the voltage across a remote set of terminals (remote voltage), respectively.

By integrating (5.2), it can be seen how each bias dependent capacitor $C(V_L, V_R)$ in the small-signal model (Figure 5.1) is used to generate a corresponding charge source $Q(V_L, V_R)$ for the large-signal model (Figure 5.2). The result is:

$$Q(V_L, V_R) = \int_0^{V_L} C(\zeta, V_R) d\zeta + Q_0(V_R) \quad (5.3)$$

The current flowing through the small-signal capacitor (Figure 5.1) is given by:

$$i_C = C(V_L, V_R) \frac{dV_L}{dt} = \frac{\partial Q(V_L, V_R)}{\partial V_L} \frac{dV_L}{dt} \quad (5.4)$$

However the current flowing through the charge source (Figure 5.2) in the large-signal model is given by:

$$i_Q = \frac{dQ(V_L, V_R)}{dt} = \frac{\partial Q(V_L, V_R)}{\partial V_L} \frac{dV_L}{dt} + \frac{\partial Q(V_L, V_R)}{\partial V_R} \frac{dV_R}{dt} \quad (5.5)$$

This results in the small-signal model shown in Figure 5.3 where a new element called a transcapacitor is unavoidably introduced [52]. The transcapacitance is described by:

$$C_T(V_L, V_R) = \frac{\partial Q(V_L, V_R)}{\partial V_R} \quad (5.6)$$

This transcapacitor causes the discrepancy between the capacitor in Figure 5.1 of the original small-signal model and the linearization of the corresponding charge source shown in Figure 5.3.

To overcome this problem, the small-signal model should include a transcapacitor in parallel with each capacitor whose capacitance value is a function of two voltages. If the capacitance of a capacitor is a function of three controlling voltages (for example V_{gs} , V_{gs} , and V_{ds}), it should be in parallel with two transcapacitors in the small-signal model, to avoid any inconsistency with the generated large-signal model to take place.

Figure 5.1. Small-signal model capacitor at each bias point.

Figure 5.2. Large-signal model charge source.

Figure 5.3. Linearization of the charge source.

In this Chapter a new consistent small-signal model of the DGFET is introduced. The new model is an extension of the work done by Root *et al.* [53] and Corbella *et al.* [54] for the single-gate FET. The consistency between the small-signal model and the large-signal model is guaranteed by deriving the small-signal model from the basic large-signal model of the DGFET [52-55].

5.2 The Consistent Small-Signal Model

Figure 5.4 shows a general large-signal DGFET model. V_1 , V_2 , V_3 , and V_4 are gate₁, gate₂, drain, and source voltages, respectively. The total current flowing into gate₁, gate₂, drain, and source are I_1 , I_2 , I_3 , and I_4 , respectively. Q_{g1} , Q_{g2} , Q_d , and Q_s are gate₁, gate₂, drain, and source charges, respectively. The sum of these charges is the total charge stored in the device.

The total current flowing into each terminal is composed of conduction current and displacement current. The total current at each terminal is given by:

$$I_1(t) = I_{g1}(V_1(t), V_2(t), V_3(t), V_4(t)) + \frac{d}{dt} Q_{g1}(V_1(t), V_2(t), V_3(t), V_4(t)) \quad (5.7)$$

$$I_2(t) = I_{g2}(V_1(t), V_2(t), V_3(t), V_4(t)) + \frac{d}{dt} Q_{g2}(V_1(t), V_2(t), V_3(t), V_4(t)) \quad (5.8)$$

$$I_3(t) = I_d(V_1(t), V_2(t), V_3(t), V_4(t)) + \frac{d}{dt} Q_d(V_1(t), V_2(t), V_3(t), V_4(t)) \quad (5.9)$$

$$I_4(t) = -(I_1(t) + I_2(t) + I_3(t)) \quad (5.10)$$

Figure 5.4. A schematic of the basic large-signal model of the dual-gate FET.

Under small-signal excitation, the total voltage at each terminal, $V_i(t)$, consists of a small-signal voltage $v_i(t)$ superimposed on the DC node voltage V_{i0} , with $i=1,2,3$, and 4. Let $V_0=(V_{10}, V_{20}, V_{30}, V_{40})$ denote the quiescent bias condition. To derive the small-signal terminal currents, (5.7)-(5.10) are expanded in a Taylor series about the quiescent point V_0 and only the linear terms are retained. Starting with I_{g1} in (5.7), the Taylor series expansion including the linear terms is given by:

$$I_{g1} \approx I_{g1}(V_0) + \left. \frac{\partial I_{g1}}{\partial V_1} \right|_{V_0} \cdot v_1 + \left. \frac{\partial I_{g1}}{\partial V_2} \right|_{V_0} \cdot v_2 + \left. \frac{\partial I_{g1}}{\partial V_3} \right|_{V_0} \cdot v_3 + \left. \frac{\partial I_{g1}}{\partial V_4} \right|_{V_0} \cdot v_4 \quad (5.11)$$

Subtracting the DC term $I_{g1}(V_0)$ from (5.11), the small-signal conduction current i_{g1} is:

$$i_{g1} = \left. \frac{\partial I_{g1}}{\partial V_1} \right|_{V_0} \cdot v_1 + \left. \frac{\partial I_{g1}}{\partial V_2} \right|_{V_0} \cdot v_2 + \left. \frac{\partial I_{g1}}{\partial V_3} \right|_{V_0} \cdot v_3 + \left. \frac{\partial I_{g1}}{\partial V_4} \right|_{V_0} \cdot v_4 \quad (5.12)$$

Equation (5.12) can be written as:

$$i_{g1} = g_{11} \cdot v_1 + g_{12} \cdot v_2 + g_{13} \cdot v_3 + g_{14} \cdot v_4 \quad (5.13)$$

where $g_{1i} = \left. \frac{\partial I_{g1}}{\partial V_i} \right|_{V_0}$ with $i=1,2,3$, and 4.

Similarly, the small-signal conduction currents i_{g2} and i_d are given by:

$$i_{g2} = g_{21} \cdot v_1 + g_{22} \cdot v_2 + g_{23} \cdot v_3 + g_{24} \cdot v_4 \quad (5.14)$$

$$i_d = g_{31} \cdot v_1 + g_{32} \cdot v_2 + g_{33} \cdot v_3 + g_{34} \cdot v_4 \quad (5.15)$$

where $g_{2i} = \left. \frac{\partial I_{g2}}{\partial V_i} \right|_{V_0}$ and $g_{3i} = \left. \frac{\partial I_d}{\partial V_i} \right|_{V_0}$ with $i=1,2,3$, and 4.

In a similar way, the small-signal charge components q_{g1} , q_{g2} and q_d are given by:

$$q_{g1} = \left. \frac{\partial Q_{g1}}{\partial V_1} \right|_{V_0} \cdot v_1 + \left. \frac{\partial Q_{g1}}{\partial V_2} \right|_{V_0} \cdot v_2 + \left. \frac{\partial Q_{g1}}{\partial V_3} \right|_{V_0} \cdot v_3 + \left. \frac{\partial Q_{g1}}{\partial V_4} \right|_{V_0} \cdot v_4 \quad (5.16)$$

$$q_{g2} = \left. \frac{\partial Q_{g2}}{\partial V_1} \right|_{V_0} \cdot v_1 + \left. \frac{\partial Q_{g2}}{\partial V_2} \right|_{V_0} \cdot v_2 + \left. \frac{\partial Q_{g2}}{\partial V_3} \right|_{V_0} \cdot v_3 + \left. \frac{\partial Q_{g2}}{\partial V_4} \right|_{V_0} \cdot v_4 \quad (5.17)$$

$$q_d = \left. \frac{\partial Q_d}{\partial V_1} \right|_{V_0} \cdot v_1 + \left. \frac{\partial Q_d}{\partial V_2} \right|_{V_0} \cdot v_2 + \left. \frac{\partial Q_d}{\partial V_3} \right|_{V_0} \cdot v_3 + \left. \frac{\partial Q_d}{\partial V_4} \right|_{V_0} \cdot v_4 \quad (5.18)$$

Differentiating (5.16)-(5.18) with respect to time results in the small-signal displacement currents of gate₁, gate₂, and the drain, respectively:

$$i_{dg1} = \frac{dq_{g1}}{dt} = C_{11} \frac{dv_1}{dt} + C_{12} \frac{dv_2}{dt} + C_{13} \frac{dv_3}{dt} + C_{14} \frac{dv_4}{dt} \quad (5.19)$$

$$i_{dg2} = \frac{dq_{g2}}{dt} = C_{21} \frac{dv_1}{dt} + C_{22} \frac{dv_2}{dt} + C_{23} \frac{dv_3}{dt} + C_{24} \frac{dv_4}{dt} \quad (5.20)$$

$$i_{dd} = \frac{dq_d}{dt} = C_{31} \frac{dv_1}{dt} + C_{32} \frac{dv_2}{dt} + C_{33} \frac{dv_3}{dt} + C_{34} \frac{dv_4}{dt} \quad (5.21)$$

where:

$$C_{1i} = \left. \frac{\partial Q_{g1}}{\partial V_i} \right|_{V_0}, C_{2i} = \left. \frac{\partial Q_{g2}}{\partial V_i} \right|_{V_0}, \text{ and } C_{3i} = \left. \frac{\partial Q_d}{\partial V_i} \right|_{V_0} \text{ with } i=1,2,3, \text{ and } 4.$$

The total small-signal current flowing into terminals 1,2,3, and 4 are:

$$i_1 = i_{g1} + i_{dg1} \quad (5.22)$$

$$i_2 = i_{g2} + i_{dg2} \quad (5.23)$$

$$i_3 = i_d + i_{dd} \quad (5.24)$$

$$i_4 = -(i_1 + i_2 + i_3) \quad (5.25)$$

Assuming that v_1, v_2, v_3 , and v_4 are sinusoidal, (5.22)-(5.25) can be transformed to frequency domain using Laplace transformation. The frequency domain terminal currents are given by:

$$\tilde{i}_1 = g_{11} \tilde{v}_1 + g_{12} \tilde{v}_2 + g_{13} \tilde{v}_3 + g_{14} \tilde{v}_4 + j\omega C_{11} \tilde{v}_1 + j\omega C_{12} \tilde{v}_2 + j\omega C_{13} \tilde{v}_3 + j\omega C_{14} \tilde{v}_4 \quad (5.26)$$

$$\tilde{i}_2 = g_{21} \tilde{v}_1 + g_{22} \tilde{v}_2 + g_{23} \tilde{v}_3 + g_{24} \tilde{v}_4 + j\omega C_{21} \tilde{v}_1 + j\omega C_{22} \tilde{v}_2 + j\omega C_{23} \tilde{v}_3 + j\omega C_{24} \tilde{v}_4 \quad (5.27)$$

$$\tilde{i}_3 = g_{31} \tilde{v}_1 + g_{32} \tilde{v}_2 + g_{33} \tilde{v}_3 + g_{34} \tilde{v}_4 + j\omega C_{31} \tilde{v}_1 + j\omega C_{32} \tilde{v}_2 + j\omega C_{33} \tilde{v}_3 + j\omega C_{34} \tilde{v}_4 \quad (5.28)$$

$$\tilde{i}_4 = -(\tilde{i}_1 + \tilde{i}_2 + \tilde{i}_3) \quad (5.29)$$

where $\tilde{i}_i$ and $\tilde{v}_i$, with $i=1,2,3$, and 4 are phasor quantities.

Equations (5.26)-(5.29) can be written in the form:

$$\begin{bmatrix} \tilde{i}_1 \\ \tilde{i}_2 \\ \tilde{i}_3 \\ \tilde{i}_4 \end{bmatrix} = [Y'] \begin{bmatrix} \tilde{v}_1 \\ \tilde{v}_2 \\ \tilde{v}_3 \\ \tilde{v}_4 \end{bmatrix} \quad (5.30)$$

where $[Y']$ is the four-port admittance matrix. Most likely, the DGFET is used in a common source configuration. In this case, (5.30) is rewritten as:

$$\begin{bmatrix} \tilde{i}_1 \\ \tilde{i}_2 \\ \tilde{i}_3 \end{bmatrix} = [Y] \begin{bmatrix} \tilde{v}_1 - \tilde{v}_4 \\ \tilde{v}_2 - \tilde{v}_4 \\ \tilde{v}_3 - \tilde{v}_4 \end{bmatrix} \quad (5.31)$$

where the common-source three-port Y-matrix $[Y]$ is given by:

$$[Y] = \begin{bmatrix} g_{11} + j\omega C_{11} & g_{12} + j\omega C_{12} & g_{13} + j\omega C_{13} \\ g_{21} + j\omega C_{21} & g_{22} + j\omega C_{22} & g_{23} + j\omega C_{23} \\ g_{31} + j\omega C_{31} & g_{32} + j\omega C_{32} & g_{33} + j\omega C_{33} \end{bmatrix} \quad (5.32)$$

Equation (5.32) can be written in the form:

$$[Y] = G_{\text{matrix}} + j\omega C_{\text{matrix}} \quad (5.33)$$

where

$$G_{\text{matrix}} = \begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{21} & g_{22} & g_{23} \\ g_{31} & g_{32} & g_{33} \end{bmatrix} \quad (5.34)$$

$$C_{\text{matrix}} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \quad (5.35)$$

Equation (5.32) represents the intrinsic Y-matrix of the new DGFET model. C_{11} , C_{22} , and C_{33} are capacitors, while C_{12} , C_{13} , C_{21} , C_{23} , C_{31} , and C_{32} are transcapacitors. In the large-signal model, each capacitor is to be represented by a charge source that is a function of the intrinsic controlling voltages on the DGFET, namely, gate₁-source voltage (V_{g1s}), gate₂-source voltage (V_{g2s}), and drain-source voltage (V_{ds}). Each capacitor in the small-signal model is in parallel with two transcapacitors, which satisfy the consistency requirements with the large-signal model.

At normal bias conditions, gate conduction currents are negligible, so that the values of g_{1i} and g_{2i} , with $i=1,2$ and 3 , are almost zeros. The parameters g_{31} and g_{32} are the DGFET transconductances g_{m1} and g_{m2} , respectively. The parameter g_{33} is the DGFET output conductance g_{ds} .

5.3 Model Verification

To verify the validity of the above model, the S-parameters of devices (1)-(7) described in Table 2.1, are measured at different bias points in the frequency range of 0.5 to 26.5 GHz. Seven bias points are chosen carefully, over the three-dimensional bias plane (V_{g1s} , V_{g2s} , V_{ds}), to demonstrate the ability of the model to accurately mimic the small-signal behavior of a 6x100 μm DGFET. These points (A) through (G) are shown by circles on the measured I-V characteristics of the 6x100 μm DGFET in Figures 5.5-5.8. The description of these bias points is summarized in Table 5.1.

Table 5.1. Bias points selected to verify the consistent small-signal model.

Bias Point	V_{g1s} (V)	V_{g2s} (V)	V_{ds} (V)	Description
A	0	0	0	At the origin
B	-1.4	0	3	Constant V_{ds} and V_{g2s} while changing V_{g1s} starting below pinch-off voltage (-1.4V) up to forward gate ₁ bias (0.6V).
C	-0.2	0	3	
D	0.6	0	3	
E	-0.2	-0.4	0.5	At the knee of a general point in the I-V plane
F	-1.2	-1.2	6	Both gates are slightly below pinch-off voltage
G	0.6	0.6	1	Both gates are forward biased

Figure 5.5. The measured drain current of a 6x100 μm DGFET as V_{ds} is swept from 0V to 6V with 0.1V steps when V_{g1s} changes from -1.4V to 0.6V at $V_{g2s}=0\text{V}$.

Figure 5.6. The measured drain current of a $6 \times 100 \mu\text{m}$ DGFET as V_{ds} is swept from 0V to 6V with 0.1V steps when V_{g1s} changes from -1 V to 0.6 V at $V_{g2s} = -0.4 \text{ V}$.

Figure 5.7. The measured drain current of a $6 \times 100 \mu\text{m}$ DGFET as V_{ds} is swept from 0V to 6V with 0.1V steps when V_{g1s} changes from -1.2 V to 0.6 V at $V_{g2s} = -1.2 \text{ V}$.

Figure 5.8. The measured drain current of a 6x100 μm DGFET as V_{ds} is swept from 0V to 6V with 0.1V steps when V_{g1s} changes from -1V to 0.6V at $V_{g2s}=0.6\text{V}$.

Using the above model, the S-parameters at the bias points (A)-(G) are calculated and compared to the measured data as shown in Figures 5.9-5.15. Very good agreement is obtained which confirms the validity of the above model. Similar agreement is obtained all over the I-V bias plane. The absolute error between the measured and the calculated S-parameters did not exceed 7% for magnitude or ± 8 degrees for phase over the three-dimensional extraction bias range and the frequency range 0.5-26.5 GHz, except at bias points close to or at the DGFET pinch-off voltage, where the maximum error in magnitude increased to 10%.

Figure 5.9. Measured (x) and calculated (solid) three-port S-parameters of 6x100 μm DGFET biased at $V_{g1s}=0\text{V}$, $V_{g2s}=0\text{V}$, and $V_{ds}=0\text{V}$ (bias point A) in the frequency range 0.5-26.5 GHz.

Figure 5.10. Measured (x) and calculated (solid) three-port S-parameters of 6x100 μm DGFET biased at $V_{g1s}=-1.4\text{V}$, $V_{g2s}=0\text{V}$, and $V_{ds}=3\text{V}$ (bias point B) in the frequency range 0.5-26.5 GHz.

Figure 5.11. Measured (x) and calculated (solid) three-port S-parameters of 6x100 μm DGFET biased at $V_{g1s}=-0.2\text{V}$, $V_{g2s}=0\text{V}$, and $V_{ds}=3\text{V}$ (bias point C) in the frequency range 0.5-26.5 GHz.

Figure 5.12. Measured (x) and calculated (solid) three-port S-parameters of 6x100 μm DGFET biased at $V_{g1s}=0.6\text{V}$, $V_{g2s}=0\text{V}$, and $V_{ds}=3\text{V}$ (bias point D) in the frequency range 0.5-26.5 GHz.

Figure 5.13. Measured (x) and calculated (solid) three-port S-parameters of 6x100 μm DGFET biased at $V_{g1s}=-0.4\text{V}$, $V_{g2s}=-0.2\text{V}$, and $V_{ds}=0.5\text{V}$ (bias point E) in the frequency range 0.5-26.5 GHz.

Figure 5.14. Measured (x) and calculated (solid) three-port S-parameters of 6x100 μm DGFET biased at $V_{g1s}=-1.2\text{V}$, $V_{g2s}=-1.2\text{V}$, and $V_{ds}=6\text{V}$ (bias point F) in the frequency range 0.5-26.5 GHz.

Figure 5.15. Measured (x) and calculated (solid) three-port S-parameters of a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s}=0.6\text{V}$, $V_{g2s}=0.6\text{V}$, and $V_{ds}=1\text{V}$ (bias point G) in the frequency range 0.5-26.5 GHz.

The variation of the extracted model parameters with frequency for a $6 \times 100 \mu\text{m}$ DGFET biased at point (E) in the frequency range 0.5-26.5 GHz is shown in Figures 5.16-5.18. The figures show that the extracted parameters are almost independent of frequency. This means that the small-signal model can be used over the measured frequency range 0.5-26.5 GHz.

Figure 5.16. The variation of the extracted capacitances with frequency for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.4\text{V}$, $V_{g2s} = -0.2\text{V}$, and $V_{ds} = 0.5\text{V}$ in the frequency range 0.5-26.5 GHz.

Figure 5.17. The variation of the extracted output conductance with frequency for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.4\text{V}$, $V_{g2s} = -0.2\text{V}$, and $V_{ds} = 0.5\text{V}$ in the frequency range 0.5-26.5 GHz.

Figure 5.18. The variation of the extracted transconductances with frequency for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.4\text{V}$, $V_{g2s} = -0.2\text{V}$, and $V_{ds} = 0.5\text{V}$ in the frequency range 0.5-26.5 GHz.

5.4 Comparison Between the Cascode and the Consistent Small-Signal Models

The cascode small-signal model and the consistent small-signal model are compared at bias point A in Figure 5.19. While both models are able to accurately represent the small-signal behavior of the DGFET, there are several differences between the two models. These differences are:

- (i) The consistent small-signal model is directly extracted from the intrinsic Y-parameters of the DGFET, which, in turn can be obtained from the measured S-parameters after de-embedding of the extrinsic parameters. This makes the extraction procedure of this model easier than that of the cascode small signal model where the model parameters are extracted using several mathematical formulas.
- (ii) Unlike the cascode small-signal model, the consistent small-signal model is able to model the DGFET when the gates are forward biased for substantial gate current.
- (iii) Under normal bias conditions, gate conduction currents are negligible, and the values of g_{1i} and g_{2i} , with $i=1,2$ and 3 , are almost zeros. This makes the number of parameters of the consistent small-signal model to be twelve versus fourteen parameters in the cascode small-signal model.
- (iv) Four parameters are not included in the consistent small-signal model but are part of the cascode-based small-signal model: the resistances R_{i1} and R_{i2} and the transit time delays τ_1 and τ_2 . At high frequencies, the resistances R_{i1} and R_{i2} are used to obtain good fitting of the

magnitudes of S_{11} and S_{22} respectively. To include the effect of R_{i1} and R_{i2} into the consistent small-signal model, Golio's approach [56] is adapted, where a resistor in series with the gate resistance can compensate for the absence of R_i . On the other hand, while there is no explicit transit time delays in the consistent small-signal model, the comparison between the intrinsic Y-matrix of the consistent small-signal model and that of the cascode-based small-signal model shows that transit time effects are implicitly included in the new model. The effects of the transit time must be included to simulate S_{31} and S_{32} accurately at high frequencies.

- (v) To develop a large-signal model using the cascode small-signal model, it is necessary know the value of voltage at the inaccessible node introduced between the two FET parts. This has been avoided by using the consistent small-signal model, which simplifies the procedure of developing a large-signal model of the DGFET.

Figure 5.19. Measured (x), calculated using cascode-based small-signal model (blue), and calculated using consistent small-signal model (red) three-port S-parameters of a 6x100 μm DGFET biased at $V_{g1s}=0\text{V}$, $V_{g2s}=0\text{V}$, and $V_{ds}=0\text{ V}$ (bias point A) in the frequency range 0.5-26.5 GHz.

CHAPTER 6

LARGE-SIGNAL MODEL OF THE DUAL-GATE GaAs MESFET

6.1 Introduction

The concept of a large-signal FET model is to simulate the transistor's nonlinear terminal currents as a function of the terminal voltages. If this is done accurately, other device characteristics such as bias-dependent S-parameters, harmonic power, and power added efficiency can also be simulated.

The intrinsic large-signal model is composed of nonlinear charge sources and nonlinear current sources that together simulate the terminal currents of the device. The charge sources simulate the displacement current, dQ/dt , while the current sources simulate the conduction current. Besides simulating the terminal currents of the device under nonlinear conditions, the charge and current sources must also model the bias dependence of the small-signal model parameters under linear conditions.

In this chapter the large-signal model of the DGFET is developed. It will be shown how the bias dependent small-signal model parameters and the measured DC I-V data are used to generate the charge and current sources of the large-signal model.

Along with the development of the large-signal model, the problem of frequency dispersion of g_{m1} , g_{m2} and g_{ds} parameters is also discussed in the next section.

6.2 Modeling the Frequency Dispersion of the Output Conductance and the Transconductances of the DGFET

6.2.1 Introduction

Frequency dispersion is a phenomenon that affects the transconductance and the output conductance of field effect transistors. Based on the published work, the frequency dispersion of the transconductance and the output conductance of the SGFET is discussed in this section. The author extended the techniques used to model the frequency dispersion of the SGFET to model this effect in the DGFET.

6.2.2 Frequency Dispersion

Frequency dispersion is the variation of the transconductance and the output conductance of microwave MESFETs over frequency. Due to frequency dispersion, the transconductance and the output conductance have higher values at low frequency (DC) than at high frequency (RF) [57]. Typically above 10 kHz both the transconductance and the output conductance have reached their high frequency values. In the following, the low frequency values of the transconductance and the output conductance will be referred to as g_m^{DC} and g_{ds}^{DC} , respectively. The high frequency values the transconductance and the output conductance will be referred to as g_m^{RF} and g_{ds}^{RF} , respectively. In nonlinear modeling, g_m^{DC} and g_{ds}^{DC} are calculated from the DC drain current. On the other hand, g_m^{RF} and g_{ds}^{RF} are extracted from the measured S-parameters.

The cause of frequency dispersion in the transconductance and the output conductance is attributed to surface states and deep-level traps [57]. Deep level traps and surface states, hereafter referred to as traps, are centers where electrons and/or holes are

captured or emitted. In the case of the transconductance and the output conductance, the dispersion appears to be caused by the interaction of electrons with the traps. The probability of electron capture or emission is a function of the trap's position within the bandgap in relation to the Fermi level, which in turn is dependent upon the potentials within the device. Because the traps cannot fill or empty instantaneously, the traps are frozen out or do not affect the electrical characteristics of the device when the frequency of the stimulus signal is greater than the trap time constant.

A large-signal model must account for frequency dispersion since the model must be able to accurately simulate both DC and RF characteristics of the device. In the DGFET model g_{m1}^{RF} affects the magnitude of S_{31} , g_{m2}^{RF} affects the magnitude of S_{32} , while g_{ds}^{RF} affects the magnitude of S_{33} . Hence, to accurately simulate the device S-parameters, the large-signal model must accurately represent g_{m1}^{RF} , g_{m2}^{RF} , and g_{ds}^{RF} of the device.

Early SGFET models, like the Curtice [58] and Statz [59] models, only modeled the DC drain current, I_d^{DC} . In simulating the S-parameters, these models calculated g_m^{DC} and g_{ds}^{DC} which are used to approximate g_m^{RF} and g_{ds}^{RF} . Hence these early large-signal models may not accurately predict the S-parameters of the device.

Penalosa and Aitchison [60] accounted for the dispersion of the output conductance by adding a series RC circuit to the FET model in parallel with g_{ds}^{DC} . While this technique works very well to model g_{ds}^{RF} at a single bias point, there is no accommodation for bias dependence in the frequency dispersion of the output conductance. Also the frequency dispersion of the transconductance is not addressed.

To account for the dispersion of both the transconductance and the output conductance, Golio et al. [57] added a transconductance to the RC circuit of Penalosa and Aitchison [60]. Similar to the Penalosa and Aitchison [60] approach, this method does not account for the bias dependence in the frequency dispersion of the transconductance and the output conductance.

A method for modeling the bias dependent frequency dispersion of the transconductance and the output conductance is to model the high frequency component of the drain current, I_d^{RF} . In general, I_d^{RF} represents the drain current at operating frequencies above the trap time constant. There are two methods by which I_d^{RF} can be determined: either by using pulsed I-V measurements [61], or from path integration of g_m^{RF} and g_{ds}^{RF} [52].

In pulsed I-V measurements, a DC quiescent bias fixes the trap occupancy level in the device. The gate and the drain voltages are then pulsed away from the quiescent voltage to the desired pulsed voltage value. During this pulse, the drain current is measured. Because the duration of the pulse is very small (on the order of 1 μ s), deep level traps and surface states cannot respond and so are frozen at the level set by the DC quiescent bias. Hence the drain current measured using pulsed I-V is free from the trap effects.

The problem with measuring I_d^{RF} using pulsed I-V is that the measured current appears to be quiescent bias dependent [55]. Winson [55] showed that as the gate quiescent bias, V_{gs} , is decreased, the current in the device decreased. Winson [55] also showed that as the drain quiescent bias is increased, the knee of the curves become gentler and the slopes of the curves in the saturation region increased. This implies that

the values of g_m^{RF} and g_{ds}^{RF} calculated from the pulsed I-V data would be dependent on the quiescent bias. Moreover, because of this apparent quiescent bias dependence, it is unlikely that g_m^{RF} and g_{ds}^{RF} determined from pulsed I-V data and g_m^{RF} and g_{ds}^{RF} extracted from S-parameters data will be equal, respectively.

Which method is chosen to determine I_d^{RF} depends on the emphasis of the large-signal model and the available measurement equipment. In this work, the emphasis is on modeling the DGFET S-parameters over bias; that is the large-signal model must represent g_{m1}^{RF} , g_{m2}^{RF} , and g_{ds}^{RF} extracted from the S-parameters. Therefore, I_d^{RF} is determined from path integration. In addition, the author did not have access to the equipment needed to perform pulsed I-V measurements.

To model both I_d^{DC} and I_d^{RF} , the method suggested by Root, Fan and Meyer [53] for the SGFET is expanded to be used to model the drain current of the DGFET. The total DGFET drain current is then given by:

$$I_d(V_{g1s}, V_{g2s}, V_{ds}) = h(f)I_d^{DC}(V_{g1s}, V_{g2s}, V_{ds}) + [1 - h(f)]I_d^{RF}(V_{g1s}, V_{g2s}, V_{ds}) \quad (6.1)$$

The first term of (6.1) models the DC drain current while the second term models the RF drain current. The function $h(f)$ is used to make a smooth transition from the DC current function to the RF current function. However, since the interest is in modeling the DGFET characteristics at DC or at RF ($f > 45$ MHz), $h(f)$ need not be smooth and is approximated here as a step function:

$$h(f) = \begin{cases} 1 & f = 0 \\ 0 & f > 0 \end{cases} \quad (6.2)$$

6.3 Development of the DGFET Large-Signal Model

In this section, the large-signal model is developed. Recall from Section 5.2 that the terminal current flowing into gate₁, gate₂, the drain, and the source are respectively given by:

$$I_1(t) = I_{g1}(V_1(t), V_2(t), V_3(t), V_4(t)) + \frac{d}{dt} Q_{g1}(V_1(t), V_2(t), V_3(t), V_4(t)) \quad (6.3)$$

$$I_2(t) = I_{g2}(V_1(t), V_2(t), V_3(t), V_4(t)) + \frac{d}{dt} Q_{g2}(V_1(t), V_2(t), V_3(t), V_4(t)) \quad (6.4)$$

$$I_3(t) = I_d(V_1(t), V_2(t), V_3(t), V_4(t)) + \frac{d}{dt} Q_d(V_1(t), V_2(t), V_3(t), V_4(t)) \quad (6.5)$$

$$I_4(t) = I_s(V_1(t), V_2(t), V_3(t), V_4(t)) + \frac{d}{dt} Q_s(V_1(t), V_2(t), V_3(t), V_4(t)) \quad (6.6)$$

Then from Kirchoff's current law, the sum of all terminal currents is zero. Hence, the sum of the conduction currents is zero, or

$$I_{g1}(t) + I_{g2}(t) + I_d(t) + I_s(t) = 0 \quad (6.7)$$

Following from the sum of the displacement currents being equal to zero, the sum of the terminal charges is also zero, or

$$Q_{g1} + Q_{g2} + Q_d + Q_s = 0 \quad (6.8)$$

From (6.7) and (6.8), it is clear that once three of the four terms are known, the fourth term can be calculated from the other three. In this work I_s and Q_s are chosen to be the dependent variables, or

$$I_s(t) = -(I_{g1}(t) + I_{g2}(t) + I_d(t)) \quad (6.9)$$

and

$$Q_s(t) = -(Q_{g1}(t) + Q_{g2}(t) + Q_d(t)) \quad (6.10)$$

The network of nonlinear current and charge sources shown in Figure 6.1, representing the basic DGFET large-signal model, can be used to represent (6.9) and (6.10). In (6.9), the source current equals the negative sum of gate₁, gate₂, and the drain conduction currents, and this relationship can be represented symbolically by three current sources, I_{g1} connected from gate₁ to the source, I_{g2} connected from gate₂ to the source, and I_{DC} connected from the drain to the source. Here I_{DC} represents the DC drain current. I_{g1} and I_{g2} represent respectively gate₁ and gate₂ conduction currents when the DGFET operates in the forward gate bias or in the gate₁-source or in the gate₂-drain breakdown regions. Three charge sources Q_{g1} , Q_{g2} , and Q_d connected as shown in Figure 6.1 are used to represent (6.10). It has been shown in Section 5.2 that the large-signal model shown in Figure 6.1 is consistent with the small-signal model developed in Chapter 5.

The basic model shown in Figure 6.1 represents a first order approximation of the DGFET characteristics. To increase the accuracy in modeling the bias dependence of the DGFET capacitance matrix (C_{matrix}), the author extends the technique introduced by Winson [55] for the SGFET to be used for the DGFET. As such, the author divides Q_{g1} into Q_{11} , Q_{12} , and Q_{13} , divides Q_{g2} into Q_{21} , Q_{22} , and Q_{23} , and divides Q_d into Q_{31} , Q_{32} , and Q_{33} . The nine charge sources will each model the nine elements of C_{matrix} independently. Additionally, the author added three additional current sources I_{gm1} , I_{gm2} ,

and I_{gds} to account for the bias dependent frequency dispersion of g_{m1}^{RF} , g_{m2}^{RF} , and g_{ds}^{RF} .

Together, I_{gm1} , I_{gm2} , and I_{gds} model I_d^{RF} .

Figure 6.2 shows a schematic of the complete DGFET large-signal model developed in this work. The charge sources Q_{11} , Q_{12} , Q_{13} , Q_{21} , Q_{22} , Q_{23} , Q_{31} , Q_{32} , and Q_{33} and the current sources I_{gm1} , I_{gm2} , I_{gds} , and I_{DC} are functions of V_{g1s} , V_{g2s} , and V_{ds} . The current sources I_{g1f} models the forward current of gate₁ while the current sources I_{g2fs} and I_{g2fd} model gate₂ forward current flowing to the source and to the drain, respectively. The current sources I_{g1bd} and I_{g2bd} represent the breakdown currents of source-gate₁ and drain-gate₂ respectively.

Figure 6.1. Topology of the basic DGFET large-signal model.

Figure 6.2. Schematic of the complete DGFET large-signal model

6.4 Modeling the Nonlinear Sources

The large-signal model shown in Figure 6.2 is composed of nonlinear charge and current sources. Modeling a nonlinear source is a two-steps process. The first step involves characterizing the nonlinear source as a function of the controlling voltages V_{g1s} , V_{g2s} , and V_{ds} .

Characterizing the sources may involve measuring a particular DGFET characteristic. For example, the current source I_{DC} in Figure 6.2 models the DC drain current as a function of V_{g1s} , V_{g2s} , and V_{ds} . Hence, measuring the DC drain current as a function of V_{g1s} , V_{g2s} , and V_{ds} characterizes I_{DC} . On the other hand, the nonlinear sources may be modeled using calculation from other data. For example, the charge modeled by the charge source cannot be measured directly and has to be calculated from capacitance and transcapacitance data extracted from bias-dependent S-parameters measurements.

Once the sources have been characterized, the final step in modeling is to approximate the source characterization data with an analytic equation. In general, approximating the source characterization data with an analytic equation involves determining the equation coefficients that produce the best fit to the data. Nonlinear curve fitting is used to determine the coefficients of the model equations.

6.4.1 Modeling the Charge Sources

In his extensive study in modeling the SGFET, Winson [55] showed that using two charge sources Q_{gs} and Q_{ds} to respectively model the capacitance pairs $[C_{11}, C_{12}]$ and $[C_{21}, C_{22}]$ is not accurate enough. To overcome this problem, Winson [55] suggested that

each capacitance or transcapacitance should be modeled individually using a charge source. In this work, the author extends the work of Winson [55] to model the DGFET.

The DGFET capacitances and transcapacitances C_{11} , C_{12} , C_{13} , C_{21} , C_{22} , C_{23} , C_{31} , C_{32} , and C_{33} are respectively modeled using nine charge sources Q_{11} , Q_{12} , Q_{13} , Q_{21} , Q_{22} , Q_{23} , Q_{31} , Q_{32} , and Q_{33} . These charge sources are connected as shown in Figure 6.2. The capacitances and transcapacitances are then given by:

$$C_{11} = \frac{\partial Q_{11}}{\partial V_{g1s}} \quad (6.11)$$

$$C_{12} = \frac{\partial Q_{12}}{\partial V_{g2s}} \quad (6.12)$$

$$C_{13} = \frac{\partial Q_{13}}{\partial V_{ds}} \quad (6.13)$$

$$C_{21} = \frac{\partial Q_{21}}{\partial V_{g1s}} \quad (6.14)$$

$$C_{22} = \frac{\partial Q_{22}}{\partial V_{g2s}} \quad (6.15)$$

$$C_{23} = \frac{\partial Q_{23}}{\partial V_{ds}} \quad (6.16)$$

$$C_{31} = \frac{\partial Q_{31}}{\partial V_{g1s}} \quad (6.17)$$

$$C_{32} = \frac{\partial Q_{32}}{\partial V_{g2s}} \quad (6.18)$$

$$C_{33} = \frac{\partial Q_{33}}{\partial V_{ds}} \quad (6.19)$$

Recall from Section 5.2 that a charge source that is controlled by more than one voltage produces additional capacitances and transcapacitances when linearized. Thus

linearizing the charge sources above would produce not only C_{matrix} but also eighteen additional elements:

$$C_{111} = \frac{\partial Q_{11}}{\partial V_{g2s}} \quad (6.20)$$

$$C_{112} = \frac{\partial Q_{11}}{\partial V_{ds}} \quad (6.21)$$

$$C_{121} = \frac{\partial Q_{12}}{\partial V_{g1s}} \quad (6.22)$$

$$C_{122} = \frac{\partial Q_{12}}{\partial V_{ds}} \quad (6.23)$$

$$C_{131} = \frac{\partial Q_{13}}{\partial V_{g1s}} \quad (6.24)$$

$$C_{132} = \frac{\partial Q_{13}}{\partial V_{g2s}} \quad (6.25)$$

$$C_{211} = \frac{\partial Q_{21}}{\partial V_{g2s}} \quad (6.26)$$

$$C_{212} = \frac{\partial Q_{21}}{\partial V_{ds}} \quad (6.27)$$

$$C_{221} = \frac{\partial Q_{22}}{\partial V_{g1s}} \quad (6.28)$$

$$C_{222} = \frac{\partial Q_{22}}{\partial V_{ds}} \quad (6.29)$$

$$C_{231} = \frac{\partial Q_{23}}{\partial V_{g1s}} \quad (6.30)$$

$$C_{232} = \frac{\partial Q_{23}}{\partial V_{g2s}} \quad (6.31)$$

$$C_{311} = \frac{\partial Q_{31}}{\partial V_{g2s}} \quad (6.32)$$

$$C_{312} = \frac{\partial Q_{31}}{\partial V_{ds}} \quad (6.33)$$

$$C_{321} = \frac{\partial Q_{32}}{\partial V_{g1s}} \quad (6.34)$$

$$C_{322} = \frac{\partial Q_{32}}{\partial V_{ds}} \quad (6.35)$$

$$C_{331} = \frac{\partial Q_{33}}{\partial V_{g1s}} \quad (6.36)$$

$$C_{332} = \frac{\partial Q_{33}}{\partial V_{g2s}} \quad (6.37)$$

where C_{111} , C_{112} , C_{122} , C_{132} , C_{212} , C_{221} , C_{222} , C_{231} , C_{311} , C_{321} , C_{331} , and C_{332} are transcapacitances, and C_{121} , C_{131} , C_{211} , C_{232} , C_{312} , and C_{322} are capacitances. The generation of these eighteen additional elements will cause inconsistency between the small-signal and the large-signal models. To overcome this problem the “transcapacitance-nulling technique” developed by Calvo [62] for the SGFET, is extended to be used for the DGFET.

The transcapacitance-nulling technique [62] is best described using Q_{11} as example. Q_{11} as implied by (6.13) can be derived by integrating C_{11} with respect to V_{g1s} . Hence, the general equation for Q_{11} can be written as:

$$Q_{11}(V_{g1s}, V_{g2s}, V_{ds}) = f_1(V_{g1s}, V_{g2s}, V_{ds}) + k_1(V_{g2s}, V_{ds}) \quad (6.38)$$

where $f_1(V_{g1s}, V_{g2s}, V_{ds})$ represents the integral of C_{11} with respect to V_{g1s} and $k_1(V_{g2s}, V_{ds})$ is the integration constant.

In (6.38), the integration constant is a free parameter that can be used to negate the unwanted C_{111} and C_{112} terms. The integration constant that will negate the C_{111} term can be derived by setting $\partial Q_{11}/\partial V_{g2s}$ equal to zero, or

$$\left. \frac{\partial Q_{11}(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{g2s}} \right|_{V_{g1s}=V_{g1s0}} = \left. \frac{\partial f_1(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{g2s}} \right|_{V_{g1s}=V_{g1s0}} + \frac{\partial k_1(V_{g2s}, V_{ds})}{\partial V_{g2s}} = 0 \quad (6.39)$$

where V_{g1s0} is the gate₁-source quiescent voltage. Integrating (6.39) with respect to V_{g2s} , the integration constant is found to be:

$$k_1(V_{g2s}, V_{ds}) = -f_1(V_{g1s0}, V_{g2s}, V_{ds}) \quad (6.40)$$

On the other hand the integration constant that will negate the C_{112} term can be derived by setting $\partial Q_{11}/\partial V_{ds}$ equal to zero, or

$$\left. \frac{\partial Q_{11}(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{ds}} \right|_{V_{g1s}=V_{g1s0}} = \left. \frac{\partial f_1(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{ds}} \right|_{V_{g1s}=V_{g1s0}} + \frac{\partial k_1(V_{g2s}, V_{ds})}{\partial V_{ds}} = 0 \quad (6.41)$$

Integrating (6.41) with respect to V_{ds} will give in the same result for $k_1(V_{g2s}, V_{ds})$ given by (6.40). Substituting with (6.40) into (6.38) results in:

$$Q_{11}(V_{g1s}, V_{g2s}, V_{ds}) = f_1(V_{g1s}, V_{g2s}, V_{ds}) - f_1(V_{g1s0}, V_{g2s}, V_{ds}) \quad (6.42)$$

From (6.42) it can be seen that

$$\frac{\partial Q_{11}(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{g1s}} = \frac{\partial f_1(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{g1s}} = C_{11} \quad (6.43)$$

and

$$\left. \frac{\partial Q_{11}(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{g2s}} \right|_{V_{g1s}=V_{g1s0}} = \left. \frac{\partial f_1(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{g2s}} \right|_{V_{g1s}=V_{g1s0}} - \frac{\partial f_1(V_{g1s0}, V_{g2s}, V_{ds})}{\partial V_{g2s}} = 0$$

(6.44)

$$\left. \frac{\partial Q_{11}(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{ds}} \right|_{V_{g1s}=V_{g1s0}} = \left. \frac{\partial f_1(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{ds}} \right|_{V_{g1s}=V_{g1s0}} - \frac{\partial f_1(V_{g1s0}, V_{g2s}, V_{ds})}{\partial V_{ds}} = 0$$

(6.45)

In the limit, (6.43), (6.44), and (6.45) show that as the amplitudes of V_{g1s} , V_{g2s} , and V_{ds} approach zero, Q_{11} linearizes to correctly produce the capacitance C_{11} and transcapacitance terms that are zero at the quiescent bias point V_{g1s0} . In practice, under small-signal conditions, the AC signal is a very small perturbation about the quiescent bias point $(V_{g1s0}, V_{g2s0}, V_{ds0})$. Hence, (6.43) is a good approximation of C_{11} and both (6.44) and (6.45) are practically zero.

The derivation of Q_{12} , Q_{13} , Q_{21} , Q_{22} , Q_{23} , Q_{31} , Q_{32} , and Q_{33} follow the same manner as the derivation of Q_{11} . Thus the general functional forms for these charge sources are:

$$Q_{12}(V_{g1s}, V_{g2s}, V_{ds}) = f_2(V_{g1s}, V_{g2s}, V_{ds}) - f_2(V_{g1s}, V_{g2s0}, V_{ds}) \quad (6.46)$$

$$Q_{13}(V_{g1s}, V_{g2s}, V_{ds}) = f_3(V_{g1s}, V_{g2s}, V_{ds}) - f_3(V_{g1s}, V_{g2s}, V_{ds0}) \quad (6.47)$$

$$Q_{21}(V_{g1s}, V_{g2s}, V_{ds}) = f_4(V_{g1s}, V_{g2s}, V_{ds}) - f_4(V_{g1s0}, V_{g2s}, V_{ds}) \quad (6.48)$$

$$Q_{22}(V_{g1s}, V_{g2s}, V_{ds}) = f_5(V_{g1s}, V_{g2s}, V_{ds}) - f_5(V_{g1s}, V_{g2s0}, V_{ds}) \quad (6.49)$$

$$Q_{23}(V_{g1s}, V_{g2s}, V_{ds}) = f_6(V_{g1s}, V_{g2s}, V_{ds}) - f_6(V_{g1s}, V_{g2s}, V_{ds0}) \quad (6.50)$$

$$Q_{31}(V_{g1s}, V_{g2s}, V_{ds}) = f_7(V_{g1s}, V_{g2s}, V_{ds}) - f_7(V_{g1s0}, V_{g2s}, V_{ds}) \quad (6.51)$$

$$Q_{32}(V_{g1s}, V_{g2s}, V_{ds}) = f_8(V_{g1s}, V_{g2s}, V_{ds}) - f_8(V_{g1s}, V_{g2s0}, V_{ds}) \quad (6.52)$$

$$Q_{33}(V_{g1s}, V_{g2s}, V_{ds}) = f_9(V_{g1s}, V_{g2s}, V_{ds}) - f_9(V_{g1s}, V_{g2s}, V_{ds0}) \quad (6.53)$$

Note that in (6.46)-(6.53) the nullification occurs at the quiescent bias point $(V_{g1s0}, V_{g2s0}, V_{ds0})$.

Now that the general equations for the charge sources have been derived, the final step is to specify the equations that best fit the extracted C_{matrix} data. After exhaustive attempts to find equations that best fit the three-dimensional C_{matrix} data, the author concluded that three-dimensional power series are the best choice. The equations introduced by the author to fit the extracted data of the C_{matrix} components, C_{11} , C_{12} , C_{13} , C_{21} , C_{22} , C_{23} , C_{31} , C_{32} , and C_{33} are given by:

$$C_{11}(V_{g1s}, V_{g2s}, V_{ds}) = \sum_{l=0}^M \sum_{m=0}^{M-l} \sum_{n=0}^{M-l-m} a_{l,m,n} V_{ds}^l V_{g1s}^m V_{g2s}^n \quad (6.54)$$

$$C_{12}(V_{g1s}, V_{g2s}, V_{ds}) = \sum_{l=0}^M \sum_{m=0}^{M-l} \sum_{n=0}^{M-l-m} b_{l,m,n} V_{ds}^l V_{g1s}^m V_{g2s}^n \quad (6.55)$$

$$C_{13}(V_{g1s}, V_{g2s}, V_{ds}) = \sum_{l=0}^M \sum_{m=0}^{M-l} \sum_{n=0}^{M-l-m} c_{l,m,n} V_{ds}^l V_{g1s}^m V_{g2s}^n \quad (6.56)$$

$$C_{21}(V_{g1s}, V_{g2s}, V_{ds}) = \sum_{l=0}^M \sum_{m=0}^{M-l} \sum_{n=0}^{M-l-m} d_{l,m,n} V_{ds}^l V_{g1s}^m V_{g2s}^n \quad (6.57)$$

$$C_{22}(V_{g1s}, V_{g2s}, V_{ds}) = \sum_{l=0}^M \sum_{m=0}^{M-l} \sum_{n=0}^{M-l-m} e_{l,m,n} V_{ds}^l V_{g1s}^m V_{g2s}^n \quad (6.58)$$

$$C_{23}(V_{g1s}, V_{g2s}, V_{ds}) = \sum_{l=0}^M \sum_{m=0}^{M-l} \sum_{n=0}^{M-l-m} f_{l,m,n} V_{ds}^l V_{g1s}^m V_{g2s}^n \quad (6.59)$$

$$C_{31}(V_{g1s}, V_{g2s}, V_{ds}) = \sum_{l=0}^M \sum_{m=0}^{M-l} \sum_{n=0}^{M-l-m} g_{l,m,n} V_{ds}^l V_{g1s}^m V_{g2s}^n \quad (6.60)$$

$$C_{32}(V_{g1s}, V_{g2s}, V_{ds}) = \sum_{l=0}^M \sum_{m=0}^{M-l} \sum_{n=0}^{M-l-m} h_{l,m,n} V_{ds}^l V_{g1s}^m V_{g2s}^n \quad (6.61)$$

$$C_{33}(V_{g1s}, V_{g2s}, V_{ds}) = \sum_{l=0}^M \sum_{m=0}^{M-l} \sum_{n=0}^{M-l-m} i_{l,m,n} V_{ds}^l V_{g1s}^m V_{g2s}^n \quad (6.62)$$

where M denotes the maximum order, i.e. the highest allowable sum of powers $l+m+n \leq M$ (In this work $M=6$). $a_{l,m,n}$ to $i_{l,m,n}$ denote the power series coefficients which constitute the model parameters.

To demonstrate the accuracy by which the above expressions are able to fit the extracted C_{matrix} data, Figures 6.3, 6.4, and 6.5 show a comparison between the data and the models for C_{11} , C_{22} , and C_{33} for a $6 \times 100 \mu\text{m}$ DGFET.

Figure 6.3. Result of curve fitting to C_{11} data of a $6 \times 100 \mu\text{m}$ DGFET using (6.54), at $V_{g2s} = 0.6\text{V}$ as V_{ds} changes from 0V to 6V and V_{g1s} varies from -1.4V to 0.6V with steps of 0.2V .

Figure 6.4. Result of curve fitting to C_{22} data of a $6 \times 100 \mu\text{m}$ DGFET using (6.58), at $V_{g2s}=0.6\text{V}$ as V_{ds} changes from 0V to 6V and V_{g1s} varies from -1.4V to 0.6V with steps of 0.2V .

Figure 6.5. Result of curve fitting to C_{33} data of a $6 \times 100 \mu\text{m}$ DGFET using (6.62), at $V_{g2s}=0.6\text{V}$ as V_{ds} changes from 0V to 6V and V_{g1s} varies from -1.4V to 0.6V with steps of 0.2V .

6.4.2 Modeling the DGFET Drain Current

As shown in Figure 6.2, the DC drain current is modeled by using a current generator I_d^{DC} . This suggests that one expression is to be used to fit the measured drain current of the DGFET in the three-dimensional bias space (gate₁-source voltage, gate₂-source voltage and drain-source voltage).

While several DC models for the drain current of the SGFET have been reported [58,59,63], much less has been published to model the drain current of the DGFET [50,25,64]. Except for Jenner's [64] model, all the published models dealt with the DGFET as a cascode connection of two SGFETs, FET₁ and FET₂, where each FET part has a current generator that represents the drain current flowing in this particular part.

Minasian [50] used a simple analytical DC model of a SGFET to derive analytical expressions of the drain current of the DGFET in the different modes of operation, but these analytical expressions did not fit the measured data well.

Madjar [25] solved a set of nonlinear equations describing the internal voltages across FET₁ and FET₂ to calculate the drain current of the DGFET. A comparison between the calculated and the measured DC curves in [25] showed a large disagreement. This makes the model unsuitable for accurate modeling of the DGFET.

On the other hand, Jenner [64] represented the drain current by a current generator and used a three-dimensional power series expression to model the drain current of the DGFET. To obtain good accuracy, a large number of model parameters are needed. This number can be as large as 165. Moreover, none of the above models took into consideration the frequency dispersion of the output conductance and the transconductances.

In this work the author introduces a new empirical model of the DGFET drain current using a nonlinear expression of the current generator I_d^{DC} as a function of the three applied intrinsic voltages, gate₁-source voltage (V_{g1s}), gate₂-source voltage (V_{g2s}) and drain-source voltage (V_{ds}). This model has 49 parameters, which is much less than the 165 parameters of Jenner's model [64]. On the other hand, the developed model not only succeeded to model the DC drain current but also successfully modeled g_{m1}^{RF} , g_{m2}^{RF} , and g_{ds}^{RF} as well. The bias dependent frequency dispersion is taken into consideration in this model by modeling the I_d^{RF} using three parallel current sources I_{gm1} , I_{gm2} , and I_{gds} shown in Figure 6.2, to model g_{m1}^{RF} , g_{m2}^{RF} , and g_{ds}^{RF} .

6.4.2.1 The DC drain current generator

The following empirical model is developed by the author to accurately model the DGFET DC drain current

$$I_d^{DC}(V_{g1s}, V_{ds}, V_{g2s}) = f_1(V_{g1s}, V_{ds}) f_2(V_{g2s}, V_{ds}) f_3(V_{g1s}, V_{g2s}, V_{ds}) \quad (6.63)$$

where $f_1(V_{g1s}, V_{ds})$, $f_2(V_{g2s}, V_{ds})$, and $f_3(V_{g1s}, V_{g2s}, V_{ds})$ are given by:

$$\begin{aligned} f_1(V_{g1s}, V_{ds}) = & \{(a_0 + a_1 V_{ds}) + (a_2 + a_3 V_{ds}) V_{g1s} + (a_4 + a_5 V_{ds}) V_{g1s}^2 + (a_6 + a_7 V_{ds}) V_{g1s}^3 \\ & + (a_8 + a_9 V_{ds}) V_{g1s}^4 + (a_{10} + a_{11} V_{ds}) V_{g1s}^5 + (a_{12} + a_{13} V_{ds}) V_{g1s}^6\} \{a_{14} + a_{15} V_{ds} + a_{16} V_{ds}^2 + a_{17} V_{ds}^3\} \end{aligned} \quad (6.64)$$

$$\begin{aligned} f_2(V_{g2s}, V_{ds}) = & \{(b_0 + b_1 V_{ds}) + (b_2 + b_3 V_{ds}) V_{g2s} + (b_4 + b_5 V_{ds}) V_{g2s}^2 + (b_6 + b_7 V_{ds}) V_{g2s}^3 \\ & + (b_8 + b_9 V_{ds}) V_{g2s}^4 + (b_{10} + b_{11} V_{ds}) V_{g2s}^5 + (b_{12} + b_{13} V_{ds}) V_{g2s}^6\} \{b_{14} + b_{15} V_{ds} + b_{16} V_{ds}^2 + b_{17} V_{ds}^3\} \end{aligned} \quad (6.65)$$

$$\begin{aligned} f_3(V_{g1s}, V_{g2s}, V_{ds}) = & \tanh(c_0 V_{ds}) + c_1 (c_2 + c_3 V_{g1s} + c_4 V_{g1s}^2 + c_5 V_{g1s}^3 + c_6 V_{g1s}^4) \\ & + c_7 (c_8 + c_9 V_{g2s} + c_{10} V_{g2s}^2 + c_{11} V_{g2s}^3 + c_{12} V_{g2s}^4) \end{aligned} \quad (6.66)$$

The a_i , b_i , and c_i coefficients are the model fitting parameters that can be simultaneously extracted by the least-squares method.

Figure 6.6 shows a comparison between the measured and the calculated DC drain current for a $6 \times 100 \mu\text{m}$ DGFET. Very good agreement between the measured and the calculated data is shown. Very good agreement is also obtained at other bias conditions.

Figure 6.6. The calculated (solid) versus measured (symbols) I/V characteristics of a $6 \times 100 \mu\text{m}$ DGFET using the new model (6.65), at $V_{g2s}=0.6\text{V}$ as V_{ds} changes from 0V to 6V and V_{g1s} varies from -1V to 0.6V with steps of 0.2V .

6.4.2.2 The RF drain current generator

To model the bias-dependent frequency dispersion of the transconductance and the output conductance of the SGFET, Winson [55] investigated the use of $I_d^{\text{RF}}(V_{gs}, V_{ds})$ to model both $g_m^{\text{RF}}(V_{gs}, V_{ds})$ and $g_d^{\text{RF}}(V_{gs}, V_{ds})$ where $I_d^{\text{RF}}(V_{gs}, V_{ds})$ is calculated from path integration of $g_m^{\text{RF}}(V_{gs}, V_{ds})$ and $g_d^{\text{RF}}(V_{gs}, V_{ds})$. Winson [55] concluded that

$I_d^{RF}(V_{gs}, V_{ds})$ can not simultaneously model both $g_m^{RF}(V_{gs}, V_{ds})$ and $g_d^{RF}(V_{gs}, V_{ds})$ with good accuracy. To increase the accuracy of modeling $I_d^{RF}(V_{gs}, V_{ds})$, Winson [55] added two current sources to the SGFET large-signal model. Each of these sources individually models the transconductance and the output conductance, and together these parallel two sources model $I_d^{RF}(V_{gs}, V_{ds})$. In this work, the author extends Winson's technique to model the RF drain current of the DGFET. Hence, three parallel current sources I_{gm1} , I_{gm2} , and I_{gds} are added to the DGFET large-signal model to model $I_d^{RF}(V_{gs1}, V_{gs2}, V_{ds})$, as shown in Figure 6.2. The current source I_{gm1} is used to model the transconductance g_{m1}^{RF} , the current source I_{gm2} is used to model the transconductance g_{m2}^{RF} , and the current source I_{gds} is used to model the output conductance g_{ds}^{RF} .

However, using three independent current sources (I_{gm1} , I_{gm2} , and I_{gds}) to model $I_d^{RF}(V_{gs1}, V_{gs2}, V_{ds})$ will encounter consistency problems. The linearization of each of these current sources will generate other conductances and transconductances. In the case of I_{gm1} , linearization produces two transconductances g_{m1}^{RF} and $g_{m11} = \partial I_{gm1} / \partial V_{gs2}$, and a conductance $g_{m12} = \partial I_{gm1} / \partial V_{ds}$. Similarly the linearization of I_{gm2} produces two transconductances g_{m2}^{RF} and $g_{m21} = \partial I_{gm2} / \partial V_{gs1}$, and a conductance $g_{m22} = \partial I_{gm2} / \partial V_{ds}$. On the other hand the linearization of I_{gds} produces a conductance g_{ds}^{RF} and two transconductances $g_{ds1} = \partial I_{gds} / \partial V_{gs1}$ and $g_{ds2} = \partial I_{gds} / \partial V_{gs2}$. Here g_{m11} , g_{m12} , g_{m21} , g_{m22} , g_{ds1} , and g_{ds2} are undesired components since they will cause inconsistencies between the small-signal and the large-signal models. The “transcapacitance-nulling technique” [62] is used to eliminate these undesired

components in a way similar to that explained in Section 6.4.2. The general equations used to model I_{gm1} , I_{gm2} , and I_{gds} are

$$I_{gm1}(V_{g1s}, V_{g2s}, V_{ds}) = A_1(V_{g1s}, V_{g2s}, V_{ds}) - A_1(V_{g1s0}, V_{g2s}, V_{ds}) \quad (6.67)$$

$$I_{gm2}(V_{g1s}, V_{g2s}, V_{ds}) = A_2(V_{g1s}, V_{g2s}, V_{ds}) - A_2(V_{g1s}, V_{g2s0}, V_{ds}) \quad (6.68)$$

$$I_{gds}(V_{g1s}, V_{g2s}, V_{ds}) = A_3(V_{g1s}, V_{g2s}, V_{ds}) - A_3(V_{g1s}, V_{g2s}, V_{ds0}) \quad (6.69)$$

From (6.67) it is easy to see that:

$$\frac{\partial I_{gm1}(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{g1s}} = \frac{\partial A_1(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{g1s}} = g_{m1}^{RF} \quad (6.70)$$

and

$$\left. \frac{\partial I_{gm1}(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{g2s}} \right|_{V_{g1s}=V_{g1s0}} = \left. \frac{\partial A_1(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{g2s}} \right|_{V_{g1s}=V_{g1s0}} - \left. \frac{\partial A_1(V_{g1s0}, V_{g2s}, V_{ds})}{\partial V_{g2s}} \right|_{V_{g1s}=V_{g1s0}} = 0 \quad (6.71)$$

$$\left. \frac{\partial I_{gm1}(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{ds}} \right|_{V_{g1s}=V_{g1s0}} = \left. \frac{\partial A_1(V_{g1s}, V_{g2s}, V_{ds})}{\partial V_{ds}} \right|_{V_{g1s}=V_{g1s0}} - \left. \frac{\partial A_1(V_{g1s0}, V_{g2s}, V_{ds})}{\partial V_{ds}} \right|_{V_{g1s}=V_{g1s0}} = 0 \quad (6.72)$$

In the same manner, it can be shown that when linearized, (6.68) and (6.69) produce g_{m2}^{RF} and g_{ds}^{RF} , respectively.

Equations (6.67)-(6.69) represent general models of the RF current sources I_{gm1} , I_{gm2} , and I_{gds} . To derive the specific equations for A_1 , A_2 , and A_3 , a simple procedure is followed. Taking A_1 as an example, the following procedure is followed:

- (i) Differentiate the DC drain current expression shown in (6.63) with respect to V_{g1s} to determine g_{m1}^{DC} .
- (ii) Use the g_{m1}^{DC} expression derived in (i) to fit the g_{m1}^{RF} data extracted from the measured S-parameters using the consistent small-signal model described in

Chapter 5, and extract the model parameters a_i , b_i , and c_i that best fit g_{m1}^{RF} . Let

the new parameters be a_{igm1} , b_{igm1} , and c_{igm1} .

- (iii) The A_1 expression in this case will be the same expression in (6.63) but with the a_{igm1} , b_{igm1} , and c_{igm1} parameters.

The same procedure is followed to derive A_2 and A_3 .

The above expressions successfully model the RF drain current. This is clear from Figures 6.7, 6.8 and 6.9, where very good agreement between the modeled data and the extracted data of the RF transconductances and the output conductance of a $6 \times 100 \mu\text{m}$ DGFET, biased at $V_{g2s} = 0.6 \text{ V}$ as V_{ds} changes from 0 V to 6 V and V_{g1s} varies from -1.2 V to 0 V with steps of 0.2 V, is shown. Very good agreement is also obtained at other bias points.

Figure 6.7. Comparison of simulated (solid) and extracted (symbols) g_{m1}^{RF} of a $6 \times 100 \mu\text{m}$ DGFET at $V_{g2s} = 0.6 \text{ V}$ as V_{ds} changes from 0V to 6V and V_{g1s} varies from -1.2 V to 0V with steps of 0.2V.

Figure 6.8. Comparison of simulated (solid) and extracted (symbols) g_{m2}^{RF} of a 6x100 μm DGFET at $V_{g1s}=0.6$ V as V_{ds} changes from 0V to 6V and V_{g2s} varies from -1.2 V to 0V with steps of 0.2V.

Figure 6.9. Comparison of simulated (solid) and extracted (symbols) g_{ds}^{RF} (c) of a 6x100 μm DGFET at $V_{g2s}=0.6$ V as V_{ds} changes from 0V to 6V and V_{g1s} varies from -1.2 V to 0V with steps of 0.2V.

6.4.3 Modeling the DGFET Extreme Bias Conditions

As described in Chapter 2, the DGFET is composed of two Schottky junctions from gate₁ to channel₁ and from gate₂ to channel₂. Under normal bias conditions, each junction is reverse biased, and the current at each gate terminal is negligible. Therefore it can be assumed that all the current at the drain terminal flows to the source terminal ($I_s = I_d$). However in large-signal applications, the DGFET might be driven into extreme biasing conditions where substantial current will be present at the gate terminals and the assumption $I_s = I_d$ is no longer valid.

There are two types of extreme biasing conditions. The first is when the voltage between one gate and its channel underneath is positive enough that the Schottky junction is forward biased and conducts. The second case is when the voltage between the gate and its channel is largely negative causing the Schottky junction to break down. In either case, DC current flows into (for forward bias) or out of (for breakdown) the gate terminal.

6.4.3.1 Breakdown current sources

Since the DGFET is almost always operated with the source terminal grounded and a positive voltage at the drain terminal, a large negative voltage applied at gate₂ will cause the Schottky diode to be more reverse biased near the drain end of channel₂ than near the source end. This will cause the gate₂ Schottky diode to break down in the drain side of channel₂, causing a surge of current to flow from the drain to gate₂. Therefore, this breakdown current is incorporated in the model as a current source, I_{g2bd} , between gate₂ and the drain terminals.

On the other hand, applying a large negative voltage at gate₁ will cause the Schottky diode to be more reverse biased near the source end of the channel₁ than near the drain end. This will cause gate₁ Schottky diode to break down in the source side of channel₁, causing a surge of current to flow from the source to gate₁. Therefore, this breakdown current is incorporated in the model as a current source, I_{g1bd} , between gate₁ and the source terminals.

This model is confirmed experimentally using a 6x100 μm DGFET as follows:

- (i) A voltage source is connected between gate₁ and the source where V_{g1s} is increased from 0 V in the negative direction when the drain is open-circuited and gate₂ is grounded. I_{g1bd} and I_{g2bd} are simultaneously measured. The measured I_{g1bd} shows the expected behavior of an Schottky diode under large negative bias as shown in Figure 6.10 while I_{g2bd} has a negligible value.
- (ii) A voltage source is connected between gate₂ and the source where V_{g2s} is increased from 0 V in the negative direction when the drain is open-circuited and gate₁ is grounded. I_{g1bd} and I_{g2bd} are simultaneously measured. Even when gate₂ diode is the one under large negative bias, the measured I_{g2bd} is found to be negligible while I_{g1bd} shows similar behavior to that shown Figure 6.10.

This confirms that gate₁ diode will break down when a large negative voltage is applied between either gate₁ or gate₂ and the source. As such, there is no need to model gate₂-source breakdown, and modeling gate₁-source breakdown is enough, since the breakdown of one gate will lead to the damage of the DGFET. By symmetry, applying a

large negative voltage between either gate₁ or gate₂ and the drain will cause gate₂ diode to break down and there is no need to model gate₁-drain breakdown.

To model the DGFET breakdown, the author follows Golio [56] who used an inverted form of the diode formula to model the SGFET breakdown current. The two current sources I_{g1bd} and I_{g2db} shown in Figure 6.2 are modeled using the following equations.

$$I_{g1bd} = -I_{o1} \left(e^{\frac{-qV_{g1s}}{kT}} - 1 \right) \quad (6.73)$$

$$I_{g2bd} = -I_{o2} \left(e^{\frac{-qV_{g2d}}{kT}} - 1 \right) \quad (6.74)$$

Figure 6.10. The measured gate₁ current of a 6x100 μm DGFET when V_{g1s} is swept from 0V to -14V when both gate₂ and the drain are floating.

6.4.3.2 Forward bias current sources

To extend the use of the model when one gate or both gates are forward biased, the forward currents of gate₁ (I_{g1f}) and gate₂ (I_{g2f}) of the DGFET devices under study are measured over the three-dimensional bias plane (V_{g1s} , V_{g2s} , V_{ds}).

When V_{g1s} is positive enough to make gate₁ Schottky diode conduct, I_{g1f} is found to be not only dependent on V_{g1s} but also on V_{g2s} and V_{ds} . The dependence of I_{g1f} on V_{g1s} for a 6x100 μm DGFET is shown in Figure 6.11. It is clear from Figure 6.11 that the dependence of I_{g1f} on V_{g1s} can be described by:

$$I_{g1f}(V_{g1s}) = I_{o1} \left(e^{\frac{qV_{g1s}}{n_1 kT}} - 1 \right) \quad (6.75)$$

Figure 6.11. The measured gate₁ forward current of a 6x100 μm DGFET when V_{g1s} is swept from 0.2V to 0.75V when both gate₂ and the drain are floating.

On the other hand, the dependence of I_{g1f} on both V_{g2s} and V_{ds} at a fixed value of V_{g1s} of a $6 \times 100 \mu\text{m}$ DGFET is shown in Figure 6.12. It is clear from Figure 6.12 that neglecting the dependence of I_{g1f} on both V_{g2s} and V_{ds} when modeling I_{g1f} will introduce a large error.

Figure 6.12. The measured I_{g1f} of $6 \times 100 \mu\text{m}$ DGFET externally biased at V_{g1s} of 0.6V while V_{ds} is swept from 0V to 6V when V_{g2s} changes from -1.4V to 0.6V with 0.2V steps.

To model the current source I_{g1f} , shown in Figure 6.2, as a function of V_{g1s} , V_{g2s} , and V_{ds} , the author introduces the following equation:

$$\begin{aligned}
 I_{g1f}(V_{g1s}, V_{g2s}, V_{ds}) = & [I_{g1f}(V_{g1s}) - \{(a_1 + a_2 V_{ds}) + (a_3 + a_4 V_{ds}) V_{g2s} + (a_5 + a_6 V_{ds}) V_{g2s}^2 \\
 & + (a_7 + a_8 V_{ds}) V_{g2s}^3 + (a_9 + a_{10} V_{ds}) V_{g2s}^4 + (a_{11} + a_{12} V_{ds}) V_{g2s}^5 \\
 & + (a_{13} + a_{14} V_{ds}) V_{g2s}^6\} (1 + a_{15} V_{ds}) \tanh(a_{16} V_{ds} + a_{17} V_{ds} V_{g2s} + a_{18} V_{ds}^2)] e^{k_1(V_{g1s} - V_{g1s})}
 \end{aligned}
 \quad (6.76)$$

$I_{glf}(V_{gls})$ is given by (6.75) where the parameters I_{o1} and n_1 are extracted by fitting (6.75) to the measured $gate_1$ forward current when V_{gls} is swept from 0 V in the positive direction to some upper limit (0.75 V in this work) when both $gate_2$ and the drain are floating. At a given value of $gate_1$ -source voltage (V_{gls}), the a_i parameters of (6.76) are extracted by fitting (6.76) to the measured $gate_1$ forward current $I_{glf}(V_{g2s}, V_{ds})$.

Figure 6.13 shows a comparison between the measured data shown in Figure 6.12 and the calculated data using (6.76). Good agreement is achieved.

From the measured I_{glf} data, it is found that the portion of I_{glf} that flows to the drain is negligible and almost all the current flows to the source. Hence the current source I_{glf} shown in Figure 6.2 is connected in the model between $gate_1$ terminal and the source terminal.

Figure 6.13. The calculated (solid) versus measured ($\bullet$) I_{gl} of a $6 \times 100 \mu m$ DGFET using the new model (6.76), biased at V_{gls} of 0.6V while V_{ds} is swept from 0V to 6V when V_{g2s} changes from $-1.4V$ to $0.6V$ with $0.2V$ steps.

To model gate₂ forward current, the measured I_{g2f} over three-dimensional bias plane (V_{g1s} , V_{g2s} , V_{ds}) is analyzed. The following remarks are noticed:

- (i) I_{g2f} is almost independent on V_{g1s} . This is clear from Figure 6.14.
- (ii) I_{g2f} exists only when the drain is grounded ($V_{ds} = 0$ V). This is shown in Figure 6.15 for a 6x100 μm DGFET. This can be explained by the fact that V_{ds} is distributed between the two FET parts comprising the DGFET. The inaccessible node between the two FET parts has a positive potential to be subtracted from the external V_{g2s} , which makes the internal voltage drop on gate₂ diode less positive and hence is not enough to drive the diode to conduct and generate forward current.
- (iii) By symmetry, the dependence of I_{g2f} on V_{g2d} for grounded drain is exactly the same as the dependence of I_{g1f} on V_{g1s} for grounded source and hence can be described by the equation:

$$I_{g2f}(V_{g2d}) = I_{o2} \left(e^{\frac{qV_{g2d}}{n_2 kT}} - 1 \right) \quad (6.77)$$

- (iv) When gate₂ diode conducts, it is found that almost all I_{g2f} flows to the drain when V_{g1s} is more negative than the pinch off voltage. When V_{g1s} is less negative than the pinch off voltage, gate₁ depletion region is not totally depleted and allows some current to flow to the source, as shown in Figure 6.14.

Let I_{g2fs} and I_{g2fd} denote the components of I_{g2f} flowing to the source and to the drain respectively. The two components are incorporated in the DGFET large-signal model using two current sources I_{g2fs} and I_{g2fd} shown in Figure 6.2. The following procedure is followed to model I_{g2fs} and I_{g2fd} :

- (i) Knowing V_{g2d} , I_{g2f} is determined using (6.77).
- (ii) Let $\alpha(V_{g1s})$ denotes the ratio I_{g2fs}/I_{g2f} . $\alpha(V_{g1s})$ is modeled using a 7th order polynomial and $I_{g2fs}(V_{g1s})$ is calculated from the relation:

$$I_{g2fs}(V_{g1s}) = \alpha(V_{g1s}) I_{g2f} \quad (6.78)$$

- (iii) I_{g2fd} is calculated from the relation:

$$I_{g2fd} = I_{g2f} - I_{g2fs} \quad (6.79)$$

Figure 6.14. The measured I_{g2f} , I_d , and I_s of a 6x100 μm DGFET when gate₂ is externally biased by 0.6V and the drain is grounded.

Figure 6.15. The measured I_{g2f} of a $6 \times 100 \mu m$ DGFET externally biased at V_{g1s} of $-1.4V$ while V_{ds} is swept from $0V$ to $6V$ when $V_{g2s}=0.6V$.

6.5 Model Continuity

To ensure that the developed DGFET large-signal model will not encounter convergency problems when implemented into a CAD tool, the functions used to approximate the model charge and current sources must be continuous at the borders of the extraction range (the bias range within which the small-signal model parameters were extracted, or the bias range within which the measurements were done) and outside the extraction range as well. In this work, the author assumes that outside the extraction range, these functions vary linearly with respect to its controlling voltages.

6.5.1 Continuity of the C_{matrix} Functions

The extraction range has an upper limit and a lower limit. Let the bias point $(V_{g1s0}, V_{g2s0}, V_{ds0})$ be the upper limit (In this work $V_{g1s0} = 0.6V$, $V_{g2s0} = 0.6V$ and $V_{ds0} = 6V$), any capacitance or a transcapacitance C_{ij} , with i and j takes the values 1, 2, and 3, at

a bias point $(V_{g1s} \geq V_{g1s0}, V_{g2s} \geq V_{g2s0}, V_{ds} \geq V_{ds0})$ is required to vary linearly with bias.

Since there are three controlling voltages, eight cases arise and C_{ij} is given by:

$$C_{ij}(V_{g1s} \leq V_{g1s0}, V_{g2s} \leq V_{g2s0}, V_{ds} \leq V_{ds0}) = F(V_{g1s}, V_{g2s}, V_{ds}) \quad (6.80)$$

$$C_{ij}(V_{g1s} > V_{g1s0}, V_{g2s} < V_{g2s0}, V_{ds} < V_{ds0}) = F(V_{g1s0}, V_{g2s}, V_{ds}) + \left. \frac{\partial F}{\partial V_{g1s}} \right|_{V_{g1s0}} (V_{g1s} - V_{g1s0}) \quad (6.81)$$

$$C_{ij}(V_{g1s} < V_{g1s0}, V_{g2s} > V_{g2s0}, V_{ds} < V_{ds0}) = F(V_{g1s}, V_{g2s0}, V_{ds}) + \left. \frac{\partial F}{\partial V_{g2s}} \right|_{V_{g2s0}} (V_{g2s} - V_{g2s0}) \quad (6.82)$$

$$C_{ij}(V_{g1s} < V_{g1s0}, V_{g2s} < V_{g2s0}, V_{ds} > V_{ds0}) = F(V_{g1s}, V_{g2s}, V_{ds0}) + \left. \frac{\partial F}{\partial V_{ds}} \right|_{V_{ds0}} (V_{ds} - V_{ds0}) \quad (6.83)$$

$$C_{ij}(V_{g1s} > V_{g1s0}, V_{g2s} > V_{g2s0}, V_{ds} < V_{ds0}) = F(V_{g1s0}, V_{g2s0}, V_{ds}) + \left. \frac{\partial F}{\partial V_{g1s}} \right|_{V_{g1s0}} (V_{g1s} - V_{g1s0}) \\ + \left. \frac{\partial F}{\partial V_{g2s}} \right|_{V_{g2s0}} (V_{g2s} - V_{g2s0}) \quad (6.84)$$

$$C_{ij}(V_{g1s} > V_{g1s0}, V_{g2s} < V_{g2s0}, V_{ds} > V_{ds0}) = F(V_{g1s0}, V_{g2s}, V_{ds0}) + \left. \frac{\partial F}{\partial V_{g1s}} \right|_{V_{g1s0}} (V_{g1s} - V_{g1s0}) \\ + \left. \frac{\partial F}{\partial V_{ds}} \right|_{V_{ds0}} (V_{ds} - V_{ds0}) \quad (6.85)$$

$$C_{ij}(V_{g1s} < V_{g1s0}, V_{g2s} > V_{g2s0}, V_{ds} > V_{ds0}) = F(V_{g1s}, V_{g2s0}, V_{ds0}) + \left. \frac{\partial F}{\partial V_{g2s}} \right|_{V_{g2s0}} (V_{g2s} - V_{g2s0}) + \left. \frac{\partial F}{\partial V_{ds}} \right|_{V_{ds0}} (V_{ds} - V_{ds0}) \quad (6.86)$$

$$C_{ij}(V_{g1s} \geq V_{g1s0}, V_{g2s} \geq V_{g2s0}, V_{ds} \geq V_{ds0}) = F(V_{g1s0}, V_{g2s0}, V_{ds0}) + \left. \frac{\partial F}{\partial V_{g1s}} \right|_{V_{g1s0}} (V_{g1s} - V_{g1s0}) + \left. \frac{\partial F}{\partial V_{g2s}} \right|_{V_{g2s0}} (V_{g2s} - V_{g2s0}) + \left. \frac{\partial F}{\partial V_{ds}} \right|_{V_{ds0}} (V_{ds} - V_{ds0}) \quad (6.87)$$

where F generally represent the functions shown in equations (6.54)-(6.62).

At bias points below the lower extraction limit (In this work $V_{g1s0} = -1.4$ V, $V_{g2s0} = -1.4$ V and $V_{ds0} = 0$ V) the above equations are used after appropriate changes in the larger than (>) and lower than (<) signs.

6.5.2 Continuity of the Drain Current Source Functions

At bias points equal to or greater than the upper limit of the extraction range, (6.80)-(6.87) are used. If V_{ds} becomes negative the drain and the source terminals switch positions and the drain current is calculated using the relationship:

$$I_d(V_{g1s}, V_{g2s}, -V_{ds}) = -I_d(V_{g1s}, V_{g2s}, V_{ds}) \quad (6.88)$$

6.6 Scaling Rules of the DGFET Intrinsic Parameters

To make the developed model usable for different DGFET topologies, seven devices were characterized. These devices are 1x50 μm , 2x50 μm , 4x50 μm , 2x100 μm , 6x50 μm , 4x100 μm , and 6x100 μm . The consistent small-signal model parameters of the 6x100 DGFET were extracted at 1815 bias points and a large-signal model was

developed for this device. For the other devices, consistent small-signal model parameters were extracted at several bias points distributed over the three-dimensional bias plane, and the scaling rules for all the model parameters were extracted.

The variation of the model parameters C_{11} , C_{12} , C_{22} , C_{33} , g_{m1} , g_{m2} , and g_{ds} with the total gate width at three different bias points A ($V_{g1s} = -0.2$ V, $V_{g2s} = 0$ V and $V_{ds} = 3$ V), B ($V_{g1s} = -0.2$ V, $V_{g2s} = -0.4$ V and $V_{ds} = 1$ V), and C ($V_{g1s} = 0.6$ V, $V_{g2s} = 0.6$ V and $V_{ds} = 3$ V) is shown in Figures 6.16-6.22. All the capacitances (C_{11} , C_{22} , C_{33}) and transcapacitances (C_{12} , C_{13} , C_{21} , C_{23} , C_{31} , C_{32}) are proportional to the total gate width. The transconductances (g_{m1} and g_{m2}) and the output conductance (g_{ds}) are also proportional to the total gate width.

Figure 6.16. The variation of C_{11} with the total gate width at three bias points: A ($V_{g1s} = -0.2$ V, $V_{g2s} = 0$ V and $V_{ds} = 3$ V), B ($V_{g1s} = -0.2$ V, $V_{g2s} = -0.4$ V and $V_{ds} = 1$ V), and C ($V_{g1s} = 0.6$ V, $V_{g2s} = 0.6$ V and $V_{ds} = 3$ V).

Figure 6.17. The variation of C_{12} with the total gate width at three bias points: A ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=0\text{V}$ and $V_{ds}=3\text{V}$), B ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=-0.4\text{V}$ and $V_{ds}=1\text{V}$), and C ($V_{g1s}=0.6\text{V}$, $V_{g2s}=0.6\text{V}$ and $V_{ds}=3\text{V}$).

Figure 6.18. The variation of C_{22} with the total gate width at three bias points: A ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=0\text{V}$ and $V_{ds}=3\text{V}$), B ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=-0.4\text{V}$ and $V_{ds}=1\text{V}$), and C ($V_{g1s}=0.6\text{V}$, $V_{g2s}=0.6\text{V}$ and $V_{ds}=3\text{V}$).

Figure 6.19. The variation of C_{33} with the total gate width at three bias points: A ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=0\text{V}$ and $V_{ds}=3\text{V}$), B ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=-0.4\text{V}$ and $V_{ds}=1\text{V}$), and C ($V_{g1s}=0.6\text{V}$, $V_{g2s}=0.6\text{V}$ and $V_{ds}=3\text{V}$).

Figure 6.20. The variation of g_{m1} with the total gate width at three bias points: A ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=0\text{V}$ and $V_{ds}=3\text{V}$), B ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=-0.4\text{V}$ and $V_{ds}=1\text{V}$), and C ($V_{g1s}=0.6\text{V}$, $V_{g2s}=0.6\text{V}$ and $V_{ds}=3\text{V}$).

Figure 6.21. The variation of g_{m2} with the total gate width at three bias points: A ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=0\text{V}$ and $V_{ds}=3\text{V}$), B ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=-0.4\text{V}$ and $V_{ds}=1\text{V}$), and C ($V_{g1s}=0.6\text{V}$, $V_{g2s}=0.6\text{V}$ and $V_{ds}=3\text{V}$).

Figure 6.22. The variation of g_{ds} with the total gate width at three bias points: A ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=0\text{V}$ and $V_{ds}=3\text{V}$), B ($V_{g1s}=-0.2\text{V}$, $V_{g2s}=-0.4\text{V}$ and $V_{ds}=1\text{V}$), and C ($V_{g1s}=0.6\text{V}$, $V_{g2s}=0.6\text{V}$ and $V_{ds}=3\text{V}$).

6.7 Temperature Dependence of the DGFET Electrical Characteristics

6.7.1 DGFET Thermal Environment

Before studying the dependence of the DGFET model parameters on temperature, a discussion of the thermal environment of the DGFET is presented. Figure 6.23 shows a simplified schematic of a DGFET on a GaAs chip mounted to a heat sink. The temperature at the backside of the chip is referred to as the backside temperature and is denoted by T_{bs} . It is assumed that the backside of the chip is in intimate contact with the heat sink; hence, T_{bs} equals the temperature of the heat sink.

Figure 6.23. Schematic of a GaAs chip attached to a heat sink.

The internal temperature of the DGFET is referred to as the channel-temperature or T_{ch} . In general, under DC bias, T_{ch} is greater than T_{bs} by an amount ΔT due to an effect called self-heating.

In any device on the chip, heat generated due to DC power dissipation is transferred throughout the chip via the process of conduction. At the sides and top

surfaces of the chip, heat is transferred to the surrounding air mass via the process of convection. The amount of heat transfer via convection is proportional to the surface area involved. Assuming that the area involved in convection is the gates metallurgical area (very small area), the amount of heat transferred to the environment is negligible. At the chip backside, the heat is transferred to the heat sink through the process of conduction.

For the measurements employed in this work, the chip is placed on top of a hot plate called thermal chuck, as shown in Figure 6.24. Measurements of the DGFET characteristics are then made at different chuck temperatures. Since the chuck is in intimate contact with the chip's backside, the DGFET characteristics can be viewed as a function of T_{bs} .

Figure 6.24. Schematic of thermal chuck and GaAs chip during device measurements made over T_{bs} .

Ultimately, the DGFET characteristics are functions of T_{ch} . T_{ch} is equal to $T_{bs} + \Delta T$ where ΔT is the change in temperature due to self-heating which is a function of the DC power dissipation associated with the DGFET DC bias conditions. As the measurements

are taken under different DC bias conditions, the amount of self-heating changes and T_{ch} would change accordingly, thereby affecting the measured characteristics.

While there are several mechanisms that can generate heat in a semiconductor device [65], Joule heating is found to be the predominant cause of self-heating in GaAs MESFETs [66]. The heat generated due to Joule heating is equal to the total DC power dissipated by the device and is given by

$$P_d = I_{g1s} V_{g1s} + I_{g2s} V_{g2s} + I_d V_{ds} \quad (6.89)$$

T_{ch} can then be calculated from the relationship:

$$T_{ch} = T_{bs} + \theta P_d \quad (6.90)$$

Where θ is the thermal resistance of the device and is given from the foundry.

Although the DGFET characteristics are functions of T_{ch} , in measuring the DGFET characteristics over temperature, only the T_{bs} component of T_{ch} is known. Hence in the study below, the electrical characteristics are plotted versus T_{bs} .

6.7.2 Effects of Temperature in DGFETs

There are several measurable DGFET characteristics that are affected by temperature. DC I-V, S-parameters, and extrinsic parameters are some of the characteristics examined below.

To examine the temperature dependence of the DGFET characteristics, the DC I-V and the S-parameters of the devices under test are measured at five values of T_{bs} . These values are 15 °C, 25 °C, 45 °C, 65 °C, and 85 °C respectively.

6.7.2.1 Temperature effects in the measured drain current

Figure 6.25 shows the measured drain current of a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g2s} = 0.6 \text{ V}$ when V_{g1s} changes from -1 V to 0.6 V with 0.2 V steps and V_{ds} changes from 0 V to 6 V with 0.1 V steps for three values of T_{bs} .

Figure 6.25. The variation of I_d with T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g2s} = 0.6 \text{ V}$ when V_{g1s} changes from -1 V to 0.6 V with 0.2 V steps and V_{ds} changes from 0 V to 6 V with 0.1 V steps for three values of T_{bs} .

There are two main temperature effects on the measured drain current. First, the downward shift in the top curves as T_{bs} increases. Second, the negative slopes taken by the top curves in the saturation region. Both of these temperature effects are due to the temperature dependence of the saturated electron velocity that decreases with increasing

temperature [67]. Since the drain current is proportional to the electron velocity, the drain current also decreases with increasing temperature [68].

Although these temperature effects are the result of a temperature dependent saturated velocity, the effects have different causes. The negative slope in the top curves is due to self-heating. As the drain current and V_{ds} voltage increases, more DC power is dissipated and more heat is generated. This increases T_{ch} away from T_{bs} causing the drain current to decrease due to the decrease in the saturated electron velocity.

The downward shift in the top curves is due to an increase in T_{ch} through an increase in T_{bs} , as shown in Figure 6.25. Again this is the result of a temperature dependent saturated electron velocity. This amount of shift is nonlinear. The shift in the curves for $V_{gls} = 0.6$ V is larger than that at $V_{gls} = 0$ V.

The type of shift in the measured drain current curves varies for different devices. Some FETs display not only a downward shift in the I-V curves but also an upward shift. Figure 6.3 shows that the curves at the top have a downward shift, and the curves at the bottom have an upward shift. The upward shift can be explained by a decrease (a more negative V_{gls} required to turn off the device) in the threshold voltage as temperature increases [68]. It is interesting to note that the downward shift approximately cancels the upward shift at $V_{gls} = -0.2$ V.

The temperature effect in the measured drain current is to be incorporated into the DGFET large-signal model by extracting the DC drain current model, (6.63), at different values of T_{bs} and allow the coefficients of (6.64), (6.65) and (6.66) to be function of temperature.

6.7.2.2 Temperature effect in the measured S-parameters

The measured S-parameters are measurable quantities that are temperature dependent. Figures 6.26-6.34 show the magnitudes and the phases of the measured S-parameters of a $6 \times 100 \mu\text{m}$ DGFET as a function of T_{bs} when the device is biased at $V_{\text{gls}} = -0.2 \text{ V}$, $V_{\text{g2s}} = 0 \text{ V}$, and $V_{\text{ds}} = 3 \text{ V}$.

The following is noticed when Figures 6.26-6.34 are analyzed:

- (i) $\text{Mag}[S_{11}]$, $\text{Mag}[S_{13}]$, $\text{Mag}[S_{21}]$, and $\text{Mag}[S_{22}]$ slightly decrease as T_{bs} increases.
- (ii) $\text{Mag}[S_{31}]$ and $\text{Mag}[S_{32}]$ show a clear decreasing trend versus temperature.
- (iii) $\text{Mag}[S_{33}]$ shows a clear increasing trend versus temperature.
- (iv) $\text{Mag}[S_{12}]$ and $\text{Mag}[S_{23}]$ show independence on temperature.
- (v) Temperature appears to affect the transition frequency (where the phase changes from -180 to 180 degrees) of $\text{Phase}[S_{11}]$ and $\text{Phase}[S_{21}]$ but otherwise does not affect the phase much, except for $\text{Phase}[S_{12}]$ and $\text{Phase}[S_{13}]$ that show a clear decreasing trend versus temperature at high frequencies.

It is clear from these figures that the amount of change over temperature is generally very small. This is the same conclusion found by Winson [55] for SGFET. Except for $\text{Mag}[S_{31}]$, $\text{Mag}[S_{32}]$ and $\text{Mag}[S_{33}]$, it is hard to distinguish a clear trend by which the magnitudes and the phases change with temperature.

(a)

(b)

Figure 6.26. Magnitude (a) and phase (b) of S_{11} as a function of T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

(a)

(b)

Figure 6.27. Magnitude (a) and phase (b) of S_{12} as a function of T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

(a)

(b)

Figure 6.28. Magnitude (a) and phase (b) of S_{13} as a function of T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

(a)

(b)

Figure 6.29. Magnitude (a) and phase (b) of S_{21} as a function of T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

(a)

(b)

Figure 6.30. Magnitude (a) and phase (b) of S_{22} as a function of T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

(a)

(b)

Figure 6.31. Magnitude (a) and phase (b) of S_{23} as a function of T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

(a)

(b)

Figure 6.32. Magnitude (a) and phase (b) of S_{31} as a function of T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

(a)

(b)

Figure 6.33. Magnitude (a) and phase (b) of S_{32} as a function of T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

(a)

(b)

Figure 6.34. Magnitude (a) and phase (b) of S_{33} as a function of T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

6.7.2.3 Temperature effects in the extracted small-signal model parameters

Since the measured S-parameters are found to slightly change with temperature, the small-signal model parameters extracted from the S-parameters will also vary with temperature. Figures 6.35-6.41 show the variation of the extracted small-signal model parameters with T_{bs} for a 6x100 μm DGFET biased at $V_{g1s} = -0.2$ V, $V_{g2s} = 0$ V, and $V_{ds} = 3$ V. The following can be noticed from these Figures:

- (i) As seen in Figure 6.35, C_{11} is almost independent on temperature. As T_{bs} changes from 15 °C to 85 °C, C_{11} changes by an amount of approximately 6 fF.
- (ii) C_{12} , C_{13} , C_{23} , C_{31} , and C_{32} also show independence on temperature as recognized from Figure 6.36.
- (iii) C_{21} shows a decreasing trend versus temperature (Figure 6.37) while C_{22} and C_{33} show an increasing trend versus temperature (Figure 6.38).
- (iv) g_{m1} , g_{m2} , and g_{ds} show a clear decreasing trend versus temperature as shown in Figures 6.39-6.41.

Anholt and Swirhun [66] showed that for GaAs SGFET, the small-signal model parameters vary linearly with temperature over the temperature range of – 70 °C to 110 °C. In this work, the author follows Anholt and Swirhun [66] and consider that all the DGFET small-signal model parameters vary linearly with temperature. In this case the variation of any small-signal model parameter, P , with temperature can be described by:

$$P(T) = P(T_0) [1 + \alpha(T-T_0)] \quad (6.91)$$

Where T_0 is the reference temperature (25 °C in this work) and α is the temperature coefficient of the parameter.

Figure 6.35. The variation of C_{11} with T_{bs} for a 6x100 μm DGFET biased at $V_{g1s}=-0.2\text{V}$, $V_{g2s}=0\text{V}$, and $V_{ds}=3\text{V}$.

Figure 6.36. The variation of C_{12} , C_{13} , C_{23} , C_{31} , and C_{32} with T_{bs} for a 6x100 μm DGFET biased at $V_{g1s}=-0.2\text{V}$, $V_{g2s}=0\text{V}$, and $V_{ds}=3\text{V}$.

Figure 6.37. The variation of C_{21} with T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

Figure 6.38. The variation of C_{22} and C_{33} with T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

Figure 6.39. The variation of g_{m1} with T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

Figure 6.40. The variation of g_{m2} with T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

Figure 6.41. The variation of g_{ds} with T_{bs} for a $6 \times 100 \mu\text{m}$ DGFET biased at $V_{g1s} = -0.2\text{V}$, $V_{g2s} = 0\text{V}$, and $V_{ds} = 3\text{V}$.

6.7.2.4 Temperature effects in the extracted extrinsic parameters

The extrinsic parameters of the devices under test are extracted at five values of T_{bs} . These temperatures are 15°C , 25°C , 45°C , 65°C , and 85°C , respectively. The variation of the extracted extrinsic parameters of a $6 \times 100 \mu\text{m}$ DGFET with T_{bs} are shown in Figures 6.42-6.43. The extrinsic resistances and capacitances show an increasing trend versus temperature while the extrinsic inductances show a decreasing trend versus temperature.

The temperature dependence of each extrinsic parameter is to be incorporated into the large-signal model using (6.91).

Figure 6.42. The variation of the extrinsic resistances of a $6 \times 100 \mu\text{m}$ DGFET with T_{bs} .

Figure 6.43. The variation of the extrinsic inductances of a $6 \times 100 \mu\text{m}$ DGFET with T_{bs} .

Figure 6.44. The variation of the extrinsic capacitances of a 6x100 μm DGFET with T_{bs} .

CHAPTER 7

RESULTS, CONCLUSIONS, AND RECOMMENDATIONS

7.1 Implementation of the Large-Signal Model in HPADS

In Chapter 6, the development of the DGFET large-signal model was described. The topology shown in Figure 6.2 was incorporated in the nonlinear simulator HPADS [40] as a user defined model using the template called Symbolic Defined Device (SDD). In SDD, the model is characterized by describing the charge and current in each branch of the circuit as functions of the nodal voltages. Once this process is completed, the new model can be accessed from a circuit file and simulated just like any other component.

7.2 Simulations, Verification, and Discussions

The following series of simulations were used to test the validity of the DGFET large-signal model.

7.2.1 DC I-V Characteristics

Figures 7.1-7.3 compare the measured DC-IV characteristics to the simulated characteristics of a $6 \times 100 \mu\text{m}$ DGFET. Figure 7.1 shows a comparison of the measured to the simulated $I_d(V_{g1s}, V_{ds})$ at $V_{g2s} = -0.6 \text{ V}$. Very good agreement is shown, however little disagreement is realized at low values of V_{ds} when $V_{g1s} = -0.8 \text{ V}$. Figures 7.2 and 7.3 show a comparison of the measured to the simulated $I_d(V_{g1s}, V_{ds})$ when gate₂ is grounded (Figure 7.2) or biased at 0.6 V (Figure 7.3). Very good agreement is shown which confirms that the model does a very good job of describing the data.

The maximum absolute error between the measured and calculated DC I-V characteristics of a $6 \times 100 \mu\text{m}$ DGFET at different values of V_{g2s} is shown in figure 7.4. As shown in figure 7.4, the maximum absolute error did not exceed 6% over the three-dimensional extraction bias range, except at bias points close to or at the DGFET pinch-off voltage (-1.1 V), where the maximum error increased to 12.4%.

Figure 7.1. Comparison of simulated (solid) and measured (symbols) DC-IV characteristics (at the extrinsic terminals) of a $6 \times 100 \mu\text{m}$ DGFET at $V_{g2s} = -0.6 \text{ V}$ as V_{ds} changes from 0 V to 6 V and V_{g1s} varies from -1 V to 0.6 V with steps of 0.2 V .

Figure 7.2. Comparison of simulated (solid) and measured (symbols) DC-IV characteristics (at the extrinsic terminals) of a 6x100 μm DGFET at $V_{g2s}=0\text{V}$ as V_{ds} changes from 0V to 6V and V_{g1s} varies from -1V to 0.6V with steps of 0.2V .

Figure 7.3. Comparison of simulated (solid) and measured (symbols) DC-IV characteristics (at the extrinsic terminals) of a 6x100 μm DGFET at $V_{g2s}=0.6\text{V}$ as V_{ds} changes from 0V to 6V and V_{g1s} varies from -1V to 0.6V with steps of 0.2V .

Figure 7.4. The maximum absolute error between the measured DC I-V characteristics and the simulated characteristics of a 6x100 μm DGFET at different values of V_{g2s} .

7.2.2 S-parameters Prediction

Figures 7.5-7.8 show a comparison between the measured S-parameters and the S-parameters generated by simulating the large-signal model of a 6x100 μm DGFET. Each of these Figures performs this comparison at a different bias point. These Figures show that the large-signal model can accurately predict small-signal performance of the device. This confirms that the large-signal model is consistent with the small-signal model. It is also clear that the functions used to model the bias dependence of the small-signal model parameters are accurate. It is also clear from Figure 7.7 that gate₁ diode is on and the large-signal model successfully simulated this situation.

Figure 7.5. Comparison of simulated (solid) and measured (x) three-port S-parameters of 6x100 μm DGFET biased at $V_{g1s}=0$ V, $V_{g2s}=0$ V, and $V_{ds}=0$ V in the frequency range 0.5-26.5 GHz.

Figure 7.6. Comparison of simulated (solid) and measured (x) three-port S-parameters of 6x100 μm DGFET biased at $V_{g1s}=-0.2$ V, $V_{g2s}=0$ V, and $V_{ds}=3$ V in the frequency range 0.5-26.5 GHz.

Figure 7.7. Comparison of simulated (solid) and measured (x) three-port S-parameters of 6x100 μm DGFET biased at $V_{g1s}=0.6$ V, $V_{g2s}=0$ V, and $V_{ds}=3$ V in the frequency range 0.5-26.5 GHz.

Figure 7.8. Comparison of simulated (solid) and measured (x) three-port S-parameters of 6x100 μm DGFET biased at $V_{g1s}=-0.6$ V, $V_{g2s}=-0.2$ V, and $V_{ds}=4$ V in the frequency range 0.5-26.5 GHz.

While the absolute error between the measured and the calculated S-parameters using the consistent small-signal model did not exceed 7% for magnitude or ± 8 degrees for phase over the three-dimensional extraction bias range and the frequency range 0.5-26.5 GHz, the maximum absolute error between the measured and the calculated S-parameters using the large-signal model is found to be 10% for magnitude and ± 12 degrees for phase over the three-dimensional extraction bias range and the frequency range 0.5-26.5 GHz. This increase in the absolute error is due to the error introduced by the fitting functions used to represent the bias dependence of the consistent small-signal model parameters.

7.2.3 Prediction of Nonlinear Behavior

As a test of the model's ability to simulate the device characteristics under nonlinear conditions, simulations of harmonic power are compared to measured data. In this measurement, the frequency of the input power or the fundamental is 10 GHz and the output power is measured at the fundamental and the second harmonic of 20 GHz. The available system of measurement was not able to measure any higher harmonics.

Figures 7.9-7.12 show the comparison of the simulated and measured harmonic power of a $6 \times 100 \mu\text{m}$ DGFET biased at four different bias points. The figures show that the fit between the simulated and the measured power at 10 GHz is within 0.6 dBm. However, at 20 GHz frequency the predicted power is within 2.5 dBm higher than the measured power. Currently, the author cannot give a reason for the larger discrepancy between modeled and measured data at 20 GHz. However it is suspected that the fit to the measured power at 20 GHz is affected by how well the first and the second derivative of

the RF drain current ($I_{gm1}+I_{gm2}+I_{gds}$) fit the first and the second derivatives of the high-frequency drain current of the device. This investigation is left for future work.

Fig. 7.9. Comparison of simulated and measured harmonic power of a 6x100 μm DGFET biased at $V_{g1s}=-0.4$ V, $V_{g2s}=0$ V, and $V_{ds}=3$ V.

Fig. 7.10. Comparison of simulated and measured harmonic power of a 6x100 μm DGFET biased at $V_{g1s}=0$ V, $V_{g2s}=0$ V, and $V_{ds}=6$ V.

Fig. 7.11. Comparison of simulated and measured harmonic power of a 6x100 μm DGFET biased at $V_{g1s}=-0.4$ V, $V_{g2s}=0$ V, and $V_{ds}=6$ V.

Fig. 7.12. Comparison of simulated and measured harmonic power of a 6x100 μm DGFET biased at $V_{g1s}=-0.4$ V, $V_{g2s}=-0.4$ V, and $V_{ds}=6$ V.

7.3 Conclusions

The results presented in the previous section show that an accurate large-signal model of the DGFET has been developed. During its development the following has been accomplished:

1. A new and accurate technique to extract the extrinsic resistances of the DGFET [29] was introduced. The new technique is based on a series of DC measurements. This technique is simple to implement and accurate as well.
2. A new analytical small-signal model of the DGFET was developed [30]. The model is based on representing the DGFET as a cascode connection of two SGFET parts. The two-port Z-parameters of each SGFET part are separated analytically from the 3-port Z-parameters without any simplifications or assumptions. The model is extracted directly from the measured three-port S-parameters.
3. A four-port small-signal model of the DGFET was developed [31]. This model does not deal with the DGFET as a cascode connection of two SGFET parts, but as a four-port device. This model avoids the complexity by which the voltage at the inaccessible node introduced between the two SGFET parts (when representing the DGFET as a cascode connection of two SGFET parts) is calculated. The model is simple yet very accurate and is extracted directly from the measured S-parameters. Extracting this model over a wide range of bias conditions resulted in the development of the DGFET large-signal model.

4. A new DC model of the DGFET was introduced [32]. The new model succeeded to accurately simulate the DC drain current and the RF drain current.
5. The gate currents of DGFET under extreme bias conditions (forward gate bias and gates breakdown) were modeled [33].
6. A large-signal model of the DGFET was developed [33] and implemented in a standard RF circuit tool, where it accurately simulated the small-signal S-parameters, the DC I-V characteristics and large-signal measurements.

7.4 Recommendations for Future Work

In the above study, the modeling was restricted to dual-gate GaAs MESFETs. Within the family of field effect transistors, there are other types of devices that are used in microwave circuits. One such device is the HEMT or High Electron Mobility Transistor. Future studies can include modeling the HEMT characteristics using the developed small-signal and large-signal models.

In this work, the author was limited in the types of measurements (DC I-V, S-parameters, and harmonic power) that could be made. Hence there was a restriction on the type of comparisons that were made between the model and the measured data. In the future, pulsed I-V and load pull measurements could be made, allowing for a more thorough test of the DGFET model.

As was discussed in section 7.2.3, little is known about how the nonlinear characteristics of the model affect the prediction of harmonic power (especially the 2nd and higher harmonics). Future research can study the effects of different I-V equations on

the prediction of harmonic power. In particular, an examination could be made on how the fit of each I-V equation to the 1st, 2nd, and 3rd derivatives of the measured DC I-V or RF I-V data affect the accuracy of the simulated harmonic power. In addition, the effect of nonlinear capacitances on harmonic power simulation can also be studied.

In this thesis an attempt was made to study the temperature dependence of the model parameters. However since this issue was not the main focus of this work, it is recommended that a full-scale investigation of the temperature dependence of the DGFET linear and nonlinear characteristics be made.

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