

Integration of Electronics and Planar Waveguide Photonics in the Silicon-on-Insulator Platform

By

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ABSTRACT

The overall goal of this research project is to develop new techniques for the monolithic integration of electronic and optical waveguide devices in the SOI platform. We have focused on designing and demonstrating monolithic integrated waveguide photodetectors and transimpedance amplifiers since these components will be vital to most systems. In the absence of a commercial foundry SOI technology offering conventional CMOS electronic devices integrated with photonic components, we have taken two different approaches towards the integration of amplifiers and photodetectors. First, we implemented lateral bipolar junction transistors (*LBJT*s) and Junction Field Effect Transistors (*JFET*s) in a widely used commercial foundry SOI photonics technology lacking MOS devices but offering a variety of *n*- and *p*-type ion implants intended to provide waveguide modulators and photodetectors. Based on knowledge of device doping and geometry, simple compact *LBJT* and *JFET* device models for circuit simulation were developed. These models were then used to design basic transimpedance amplifiers integrated with optical waveguides, which were fabricated along with a suite of test devices. Experimental test results for the completed structures are reported and used to refine the compact device models. The second approach has been to show how low-loss optical waveguides can be integrated in a simple fully-depleted SOI CMOS technology used for in-house student project fabrication in the Carleton University Microfabrication Facility. In particular experimental and theoretical results are given for loss and photoresponse for Schottky diode photodetectors integrated with these waveguides. A CMOS transimpedance amplifier is also demonstrated in this technology.

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LIST OF ABBREVIATIONS

USB	Universal Serial Bus.....	2
CPU	Central Processing Unit.....	2
LIDAR	Light Detection and Ranging.....	2
CMOS	Complementary Metal Oxide Semiconductor.....	2
SOI	Silicon on Insulator.....	3
LOCOS	Local Oxidation o Silicon.....	4
SiEPIC	Silicon Electronic Photonic Integrated Circuit.....	5
LBJT	Lateral Bipolar Junction Transistor.....	5
JFET	Junction Field Effect Transistor.....	5
TIA	Transimdepance Amplifier.....	6
DIBL	Drain Induced Barrier Lowering.....	9
PDK	Process Design Kit.....	10
MZI	Mach Zehnder Interferometer.....	13
MRR	Microring Resonator.....	13
POC	Point of Care.....	13
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.....	21
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor.....	23

NMOS	N-type Metal Oxide Semiconductor.....	37
SEM	Scanning Electron Microscope.....	42
SPICE	Simulation Program with Integrated Circuit Emphasis.....	48
TCAD	Technology Computer Aided Design.....	62
SRH	Shockley Read Hall.....	72
DNA	Deoxyribonucleic Acid.....	83
TE	Transverse Electric.....	87
TM	Transverse Magnetic.....	87
FMM	Film Mode Matching.....	87
MGW	Mixed Geometry Waveguide.....	88

Chapter 1: Introduction

1.1 Motivation

Monolithic silicon photonics integration provides advantages of high speed of operation, high quality of sensing, low parasitic capacitance of interconnects, and better portability of devices. It has grown quickly from a niche research field to an industrial technology with applications in telecommunication, data transmission, optical biosensors (lab-on-chip) in biomedical applications, and remote sensing in environmental monitoring and defense security systems [1]. One of the attractions of silicon photonics is the potential to integrate conventional electronics with photonic components on the same chip.

The hybrid integration is a popular method in which discrete devices on separate functional chips are connected using electronic or optical interconnects. Most optical receivers rely on hybrid integration which interconnects multiple ICs from different technologies through bonding. The disadvantage of hybrid integration is lack of compactness and enhanced parasitic effects in terms of interconnects and bonding pads, so that there are negative effects on system noise and reliability. Photonic devices provide the inherent advantages of high capacity in transmission, wavelength selective detection, and refractive index sensing. However, they do not provide input-output isolation and electronic signals readout during operation. In monolithic integration all photonic and electronic components are fabricated on the same chip, reducing parasitic effects, and potentially providing high reliability and efficiency. Commercialization efforts towards this integration have focused on application in

high speed transmission and high performance computing. These might include board-to-board, short reach connections on the scale of USB and perhaps CPU core-to-core communications [2]. Beyond data communications and transmission, there are many applications being explored including optical gyroscopes [3, 4], gas sensors [5], novel light sources [6, 7], LIDAR systems [8] and many more. For sensors applications, there is a huge advantage for having integration of optical components and electronic readout circuitry on the same substrate, providing compactness, low noise, high reliability and easy provision of redundancy in critical paths [9].

Monolithic electronic/photonic integration is also being driven by the relentless increase in the complexity of conventional CMOS electronics as described by Moore's law [10]. As the result, the technology is reaching limitations of electrical interconnection and power consumption. In particular, it is required to handle several hundreds of gigabits per second in high-performance computing systems and data communication systems. Channel reflection, crosstalk and bandwidth are primary limitations of high-speed electrical data transfer in these systems. Optical data transfer is sought because it is not affected by reflection and crosstalk from joule heating and power dissipation [11].

Monolithic photonics/electronics integration was first reported in the mid 1980s [12], driven initially by the telecommunication industry. The vision of a 'superchip' combining electronics and photonics emerged in the early 1990s [13]. However, optical - electronic integration suffers from electrical, thermal and optical cross-talk issues that need to be overcome to make real progress. These are the subject of intense research and development efforts worldwide. Luxtera was the pioneer in

developing CMOS-photonics integration based on a 130 nm technology at Freescale, and brought the first silicon photonics product to the market [14]. IBM developed a silicon photonic transmitter for next-generation short-reach optical interconnects. This is the first fully monolithically integrated silicon photonic four-level pulse-amplitude modulation (PAM) transmitter operating at 56 Gb/s with error-free transmission [15]. Intel has announced the development of 100GHz silicon photonics transceivers to be used for 5G and IoT applications, not just in data centers [16]. Unfortunately, there were no public foundries offering monolithic integration of full CMOS microelectronics and photonic components at the time of work described in the thesis commenced. That changed recently with the offering of public access to the Global Foundries process [17] . In 2012, with the promise to provide foundry access to CMOS/photonics technology, the Optoelectronic Systems in Silicon (OpSIS) program was established by Professor Hochberg's research group at the University of Washington and the University of Delaware, but it was ended after a few years operation [18]. Singapore's Institute for Microelectronics (IME) is now the main international foundry providing multi-project wafer (MPW) silicon photonics fabrication. CMC Microsystems offers access to this foundry for Canadian universities [19]. This provided an opportunity that we could fabricate electronic-photonics monolithic design by using the standard process flow supported by IME's silicon photonic MPW runs.

1.2 Thesis Objectives

Based on the introduction and motivation discussed above, we are going to design and fabricate electronic circuitry and monolithic integrated waveguide optical components including photodetectors on a SOI platform that could be used in lower speed applications such as sensing and biomedical industries. With bandwidth, gain and noise optimization, these optoelectronic building blocks could be used for any optical receiver system. These are critical elements and necessary in many applications including fiber telecommunications and data communication networks. We will use two novel approaches to realize this monolithic integration of optical and electronic circuits, since as yet, there are no commercial foundries available for full CMOS-photonics integration even though some companies have such technologies for their own internal use.

We began by designing and fabricating Schottky diode photodetectors integrated with waveguides formed by the Local Oxidation of Silicon (LOCOS) process using Carleton's own Microelectronics Fabrication Facility. LOCOS and Schottky diode fabrication are two proven processes that could easily be implemented in almost any silicon foundry. This part of the research builds on earlier M.A.Sc thesis research [20, 21], in which LOCOS was used to fabricate waveguide Schottky diode photodetectors with relatively coarse dimensions. Here we extend this work by presenting a theoretical modeling and literature review of the optical loss associated with Schottky waveguide photodetectors. The LOCOS waveguide process is highly compatible with integration with CMOS electronics, offering a novel and very simple approach to CMOS – photonics integration. We present a process flow showing how the LOCOS

– defined waveguides and Schottky waveguide photodetectors could readily be integrated with an existing fully – depleted SOI CMOS technology used for in-house student project fabrication at Carleton. To further illustrate how this integration could proceed we designed, fabricated and successfully tested a CMOS transimpedance amplifier in this technology.

While developing the Carleton LOCOS technology, we had an opportunity to participate in the CMC- sponsored workshop on S ilicon Electronic Photonic Integrated Circuits (SiEPIC), in 2015. This workshop made use of the IME integrated photonics fabrication process mentioned above. The IME technology supports design and fabrication of waveguides, modulators, detectors and other optoelectronics components. It provides six implants for optical modulators but was never intended to provide full electronics capability. We noted that JFET and lateral BJT transistors could be realized by using the available implantation steps. Using these improvised electronic devices, we have designed transimpedance amplifiers integrated with photodiodes, we then integrated the electronic circuits with photonic devices including input/output grating couplers, SOI strip waveguide, and a Ge photo-detector. All the photonics and electronics devices were laid out and fabricated on the same SOI substrate. This is an example of comprehensive monolithic electronics and photonics integration in a foundry SOI technology. This is also the major contribution of this thesis. We decided to focus our effort on this approach since an existing foundry technology is much more likely to be adopted by other researchers than an experimental technology developed in a university fabrication facility would be.

1.3 Thesis Organization

This thesis is divided into seven chapters. Chapter 2 gives background reviews on silicon photonics including Silicon-on-Insulator (SOI) waveguide integration and monolithic photonics CMOS integration. Chapter 3 presents theories of Lateral Bipolar Junction Transistors (*LBJTs*), Junction Field Effect Transistors (*JFETs*), and transimpedance amplifiers (TIA) design. Chapter 4 explores an alternative approach to photonics and electronics integration using the SiEPIC process. The implementation of *LBJTs*, *JFETs* and photodiode amplifiers in this technology is discussed in detail. The integration of these electronic and photonics devices on a SOI substrate is then presented. The detailed fabrication process flow will be given and discussed in this chapter. Chapter 5 provides device characterization and circuit functionality results on *LBJTs*, *JFETs* and photodiode amplifiers fabricated in SiEPIC 2015. Chapter 6 focuses on the electronic and optic integration using CMOS electronics and Schottky waveguide photodetectors fabricated in Carleton's Microelectronics Fabrication Facility. A process flow for demonstrating full integration by LOCOS is given. A comparison of the optical and electronics performance between Pt/nSi, Pd/nSi and Ni/nSi Schottky diodes is provided. Optical loss in these devices is studied by Fimmwave simulation. Chapter 7 draws conclusion on the current work with proposes feasible improvement in the future.

Chapter 2: General Background and Literature Review

This chapter provides background on the silicon photonic integration especially on silicon photonics-CMOS and waveguide optics in the Silicon-on-Insulator (SOI) platform. The literature review of each element will be given on both aspects of academic and industrial developments.

2.1 SOI Platform

In the last two decades, SOI has become a widely available substrate extensively used for electronic and photonic integrated circuits. It not only helps the reduction of parasitic capacitance and eliminates latch up, enabling high-speed operation in electronic circuits, but also provides unique optical properties because of the large refractive index difference between silicon and SiO_2 layers. The first silicon waveguide was created using doping to produce a refractive index contrast in the mid - 1980s [22, 23]. In the late 1980s, Separation by IMplanted Oxygen (SIMOX) and Bond and Etch-back SOI (BESOI) substrates were developed for waveguides, but losses in these early devices were large [24 - 27]. The loss was improved during 1990s, Kurdi *et al.* demonstrated a loss less than 1 dB/cm for a 0.2 μm silicon planar waveguide with a 0.5 μm buried oxide layer [28]. Schmidtchen *et al.* reported a loss of 0.4 dB/cm for a silicon waveguide [29]. Rickman *et al.* confirmed that the propagation loss was not going to be a serious issue in the development of the SOI technology [30]. The earliest SOI planar waveguides were rib waveguides with multi-micron width [31]. More recently, sub-micron dimension “wire” waveguides and ring structures have become popular for both sensing and data communication applications [32-34]. The SOI waveguide is therefore an excellent candidate for optical and electronic integration, because it provides both electrical and

optical isolation to eliminate leakage and crosstalk [35]. It is now considered as one of the most attractive routes towards large-scale deployment of photonic integrated circuits. It is a superior platform for silicon photonics such as waveguides and modulators by providing a high path confinement and a low optical leakage [36].

2.2 Silicon Photonics and CMOS Integration

Silicon photonics is in principle compatible with CMOS processes which should enable photonic and electronic devices to be integrated on the same substrate, although progress in this field has so far been surprisingly slow. Integration of photonics with CMOS circuitry offers new functionality and high performance by enabling of electronic - photonics convergence on a single SOI substrate. Photonic - electronic integration can significantly improve system reliability, reduce cost and increase the multifunction performance.

2.2.1 Technology Development

In 1990s, Soref proposed the earliest architecture of silicon photonics integration [37,38], but little progress was made during 1993-2003 despite the promising applications. The concept of electronics and photonics monolithic integration introduces trade-off changes of CMOS process flow to enable photonics devices feasible. Ideally, inclusion of high performance optoelectronic circuits should minimally disrupt CMOS device performance. While most passive devices such as waveguides, splitters, and multiplexers can be achieved with etching processes alone, active devices modulators and detectors do require additional steps to realize. The SiO₂ thickness and the top silicon thickness are two significant parameters for photonics and electronics performance. The thickness of SiO₂ layer and top silicon are decreasing as CMOS technologies nodes are in the 100-nm

range. Unfortunately, photonics do not benefit in terms of performance of the smaller technology node, the top silicon thickness must be in the range of 200 to 300 nm in order to provide optimal confinement, and the SiO₂ layer must be thick enough ($\sim 1 \mu\text{m}$) to ensure no significant leakage into the substrate and minimize propagation loss. Thicker SiO₂ layer degrades the performance of deeply-scaled transistors via drain-induced barrier lowering (DIBL) [39, 40]. Although there is complexity and cost associated with monolithic front-end integration, the potential benefits in terms of performance, fabrication yield and cost still make it worthwhile to invest efforts on continuing along the path of integrating photonics and CMOS electronics.

2.2.2 Progress Review

Recently, industry and governments are now spurring this field forward at an accelerated rate. For CMOS photonic monolithic integration, Intel has presented a two-channel photonic/electronic IC used in 100G data center interconnect for data communications [41]. IBM demonstrated photonics/electronics integration in a 90 nm CMOS SOI technology node. The transistor gate length was further scaled down to increase the bandwidth in order to stabilize optical receiver performance at 25 Gbps [42]. Luxtera is the pioneer in developing CMOS-photonics integration based on a 130 nm technology at Freescale and brought the first silicon photonics product to the market [43]. Recently, they collaborated with ST Microelectronics to deliver low cost 28Gbits/s silicon photonics platform using 300mm SOI wafer [44]. This required tremendous effort on process development to add germanium photodetector and waveguide formation while having no adverse effects on the existing CMOS transistors. In addition to the industrial contribution, university research has consistently played a key role in silicon photonics. A

research group at MIT has reported the first monolithic optical transceiver in a sub-100 – nm standard SOI process [45]. A monolithic optical transceiver operating at higher speed was also reported jointly by UC San Diego and Oracle in the same year [46]. The chip is implemented in a 0.13 μ m SOI CMOS technology and achieves an operating speed of 25 Gb/s for the entire transceiver. A proposal of “zero-change” silicon photonic SOI platform was reported by using an unmodified commercial 45 nm CMOS SOI process [47].

In order to achieve widespread use of silicon photonic integration technology, an essential element is a multi-project wafers (MPWs) service provided by fabrication foundries. Making production processes available to the research and industrial community is the key part of the fabless ecosystem in microelectronics. MOSIS has made these processes accessible over the past decades [48]. The first silicon photonics multi-project wafer foundry services were offered by IMEC and CEA-Leti via ePIXfab beginning in 2006 [49, 50]. The silicon photonics cells and design tools, included an advanced Process Design Kit (PDK) provided by Optoelectronic Systems Integration in Silicon (OpSIS) [51]. The OpSIS was established by Professor Michael Hochberg at the University of Delaware who is known as a founder of Luxtera. It originally aimed to develop the fundamental tools and methodologies that required to successfully design complex electronic-photonic integrated devices in silicon. During the time, OpSIS fulfilled its scientific mission of providing tools represent the state of the art in photonic design automation and PDK. Unfortunately, it was not able to transition these innovations into the commercial sphere by a fabrication foundry. However, OpSIS has developed advanced photonic Process Design Kits (PDKs) at both the Institute of Microelectronics

(IME), a member of Agency of Science, Technology and Research (A*STAR) in Singapore and BAE Systems. The BAE Systems interaction came to an end shortly after the delivery to them of working photonics process due to the shutdown of their captive fabrication facility serving the Department of Defence (DOD).

Despite the lack of public foundries offering commercial service of CMOS photonic monolithic integration, much progress has been made by industry companies and university research groups using their own resources. The core project of this thesis was fabricated by *IME* with the support of Silicon Electronic Photonic Integrated Circuits (SiEPIC) program offered by CMC Microsystems.

2.3 Waveguide Photodiodes

The waveguide-integrated photodiode is an effective approach to optical - electronic signal conversion in photonic integrated circuits. It provides high bandwidth and low dark current because it can enable fully optical absorption along the waveguide and minimize carrier transit time in a smaller active device area [52]. There is extensive research in waveguide photodiodes, lasers, and modulators integration for fiber-optic telecommunications. Indeed, all the devices necessary to build a complete photonics transceiver were already available in the SOI platform in 2000s, except for the laser light source which is still challenging. In the case of waveguide photodiodes, Si itself cannot be used efficiently for optical fiber communication due to its inherently large bandgap. A number of techniques have therefore been developed to build photodiodes which including germanium epitaxy, plasmonic absorption and implant damage photodiode [53-57]. Germanium-based photodiodes is the most compatible method with CMOS process although there is challenge of lattice mismatch on Ge epitaxy, it has strong absorption at

communication wavelength (1.3-1.55 um) and high carrier mobility [58-60]. The recent research reports Ge photodiode have achieved up high bandwidth of 40-60 GHz [61, 62].

Alternatively, one of technique for obtaining a sub-bandgap photodetector is to use a metal-semiconductor Schottky barrier diode [63-68]. their simple structure allows for easy fabrication and integration. The built-in energy barrier of the metal-semiconductor Schottky diode is less than that of a *pn* junction, so that photons with energy less than the bandgap may be capable of exciting electrons over the barrier and giving rise to a photocurrent. An attractive method of forming such a device involves the deposition of a metal layer over a waveguide fabricated by the Local Oxidation of Silicon (LOCOS) technique [69, 70], where selective oxidation is used to define a rib waveguide surrounded by thermally-grown oxide. LOCOS has great potential to produce the ultralow loss SOI waveguides due to the inherent smoothness of the oxidized waveguide sidewall. The smooth LOCOS surface is also ideal for minimizing diode leakage. With an appropriate choice of metal and hence barrier height good sub-bandgap photoresponse can be obtained with relatively low dark current leakage. The optical absorption by the Schottky metallic layer is the main contributor to the photocurrent generation, but also causes optical loss and attenuation in the metal-clad optical waveguide. The experimental and simulation results demonstrated that palladium (Pd) and nickel (Ni) barrier layers are suitable for the 1310 - 1550 nm wavelength range detection [71].

2.4 Biosensing

Although silicon photonics research has been driven by telecom and data communication applications, another important application is integrated SOI waveguide label-free silicon photonics biosensors for clinical diagnostics. These offer significant advantages by providing a portable, easy-to-use and highly sensitive biosensor lab-on-a-chip platform for real-time diagnosis [72, 73]. Highly sensitive, fast and economic techniques of analysis are desired for point-of-care (POC) diagnostic applications to improve access to cost-effective healthcare technologies. It enables the development of miniaturized compact sensing devices due to the high refractive index contrast between silicon and silicon dioxide. For example, Mach-Zehnder interferometers (MZIs), microring resonators (MRRs), microdisk resonators, Bragg grating resonators and one-dimensional (1D) or two-dimensional (2D) photonic crystals (PhCs) have been developed over the past decades for biosensing diagnostic applications [74-77]. The label-free SOI based biosensor allows simultaneous multiplexed detection on a single chip, and high production volumes with CMOS-compatible low-cost process make it a promising optical device. In recent years, integration is popular in multiple functions including on-chip fluidic handling and optical analysis, as well as data processing [78]. For a lab-on-a-chip system, an on-chip photodetector is required to convert the light signal for further processing. A Ge-based photodetector shows high responsivity of 0.74 A/W and low dark currents of less than 4 nA [79], its performance was analyzed in an on-chip biosensor [80]. For conventional evanescent field biosensing techniques, the real-time sensor's surface is analyzed by monitoring the wavelength shift in the transmission spectrum or detecting the transmission intensity change caused by shifts at a fixed wavelength [81, 82]. Startup

companies in San Diego and Belgium developed silicon-photonic based biosensors for a number of medical diagnostic test and needle-free glucose sensors [83-85]. However, due to the challenge of the monolithic integration on Si substrate, a complete chip-scale integration of the portable biosensing platform for POC diagnosis requires further development. Compared to very commercially-mature label-free biosensing technique such as SPR, the Si-based sensing approach still needs improvement in sensitivity for label-free detection of small molecule analytes to fulfill the market demand.

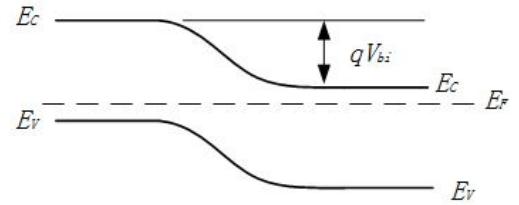
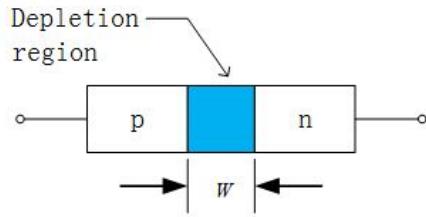
Chapter 3: Theoretical Background

Chapter 3 reviews semiconductor physics and devices including the *p-n* junction, Bipolar Junction Transistors (*BJTs*), Junction Field Effect Transistors (*JFETs*), waveguide photodiodes and trans-impedance amplifiers (*TIAs*). This provides fundamental background on designing *LBJTs*, *JFETs*, *TIAs*, and waveguide photodetectors integration in Chapter 4.

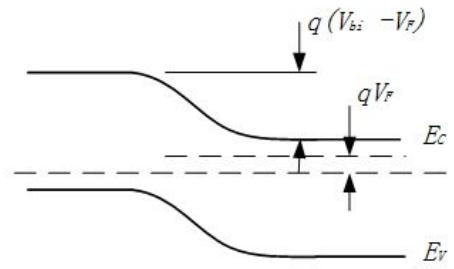
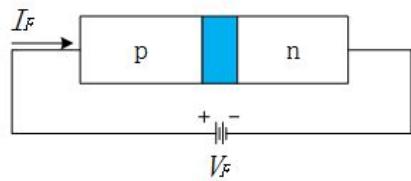
3.1 *p-n* Junction

3.1.1 Depletion region

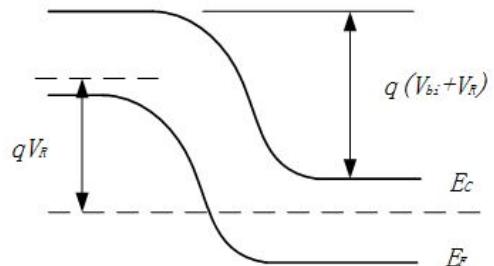
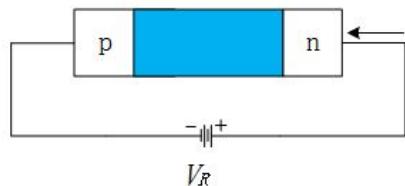
A *p-n* junction is the basic building block for the bipolar transistor and the JFET. Static characteristics, depletion capacitance, carrier generation - recombination and junction breakdown were discussed in this section. A diagram of *p-n* junction is illustrated in Fig. 3.1 [86]. The corresponding potential energy difference from the *p*-side to the *n*-side is qV_{bi} . If a positive voltage V_F is applied to the *p*-side, the total electrostatic potential across the junction and depletion layer width were decreased. By contrast, the total electrostatic potential across the junction and the depletion width increases if positive voltage V_R is applied to the *n*-side with respect to the *p*-side.



(a)



(b)



(c)

Figure 3.1 Schematic representations of depletion layer width and energy band diagrams of a *p-n* junction under various biasing conditions. (a) Thermal-equilibrium condition. (b) Forward-bias condition. (c) Reverse-bias condition. The doping concentration is N_a for *p*-side, N_d for *n*-side. ϵ_s is the semiconductor permittivity [86].

The built-in potential [87] is the total electrostatic potential difference between the *p*-side and the *n*-side neutral regions at thermal equilibrium. It is defined by

$$\phi_{bi} = \frac{kT}{q} \ln \frac{N_d N_a}{n_i^2} \quad 3.1.1$$

We can calculate the depletion layer width by following equation:

$$W_{dep} = \sqrt{\frac{2\epsilon_s \phi_{bi}}{q} \left(\frac{1}{N_a} + \frac{1}{N_d} \right)} \quad 3.1.2$$

If $N_a \gg N_d$, as in a P+N junction,

$$W_{dep} \approx \sqrt{\frac{2\epsilon_s \phi_{bi}}{q N_d}} \quad 3.1.3$$

If $N_d \gg N_a$, as in an N+P junction,

$$W_{dep} \approx \sqrt{\frac{2\epsilon_s \phi_{bi}}{q N_a}} \quad 3.1.4$$

The PN junction may be modeled as a parallel-plate capacitor with depletion capacitance

$$C_{dep} = A \frac{\epsilon_s}{W_{dep}} \quad 3.1.5$$

Where C_{dep} is the depletion-layer capacitance and A is the area. The capacitance is an unwelcome capacitive load to devices and circuits. It can be lowered by reducing the junction area and increased by reducing the doping concentrations and applying a reverse bias.

3.1.2 Current-Voltage characteristics of *pn* junction

In an ideal junction, no current is generated within the depletion region; all currents come from the neutral regions. The minority carrier densities are shown in the middle of Fig.

3.2 [86], and the electron and hole currents are shown at the bottom of Fig. 3.2. It illustrates the injected minority carriers recombine with the majority carriers as the minority carriers move away from the boundaries. The hole diffusion current will decay exponentially in the *n*-region with diffusion length L_p , and the electron diffusion current will decay exponentially in the *p*-region with diffusion length L_n . The total current is constant throughout the device:

$$J = J_p(x_n) + J_n(-x_p) = J_s \left(e^{qV/kT} - 1 \right) \quad 3.1.6$$

$$J_s \equiv \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{po}}{L_n} \quad 3.1.7$$

Where J_s is the saturation current density, n_{po} and p_{no} are the equilibrium electron densities in the *p*-sides and hole densities in the *n*-sides, respectively.

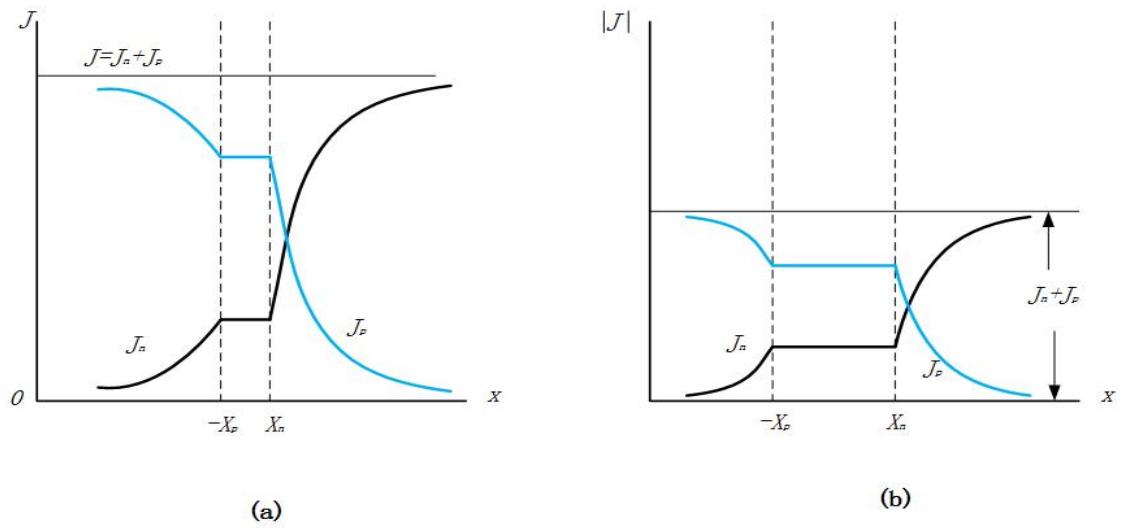
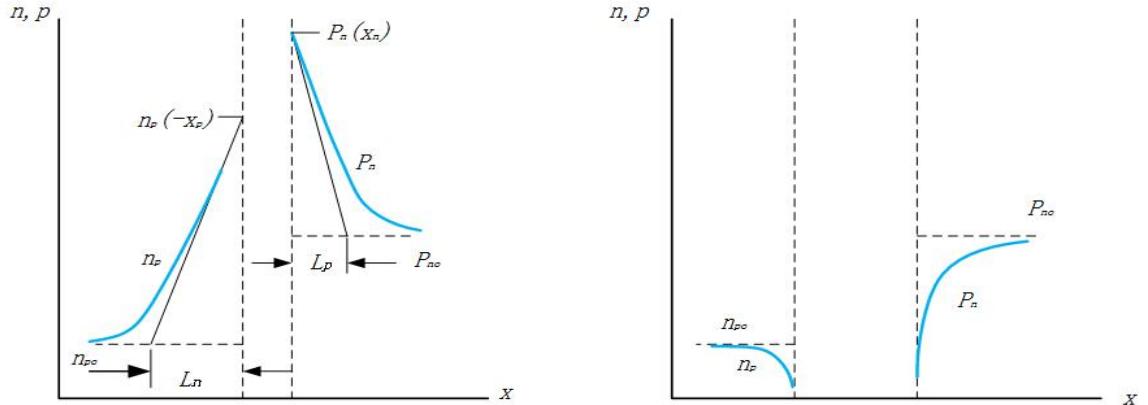


Figure 3.2 Injected minority carrier distribution and electron and hole currents. (a) Forward bias. (b) Reverse bias. The figure illustrates idealized currents. In practical devices, the currents are not constant across the space charge layer [86]

3.1.3 Generation-recombination current

For silicon and gallium arsenide p-n junction, the ideal equation can give only qualitative agreement because of the generation or recombination of carriers in the depletion region. Whenever the thermal-equilibrium condition is disturbed in *pn* junction, generation-recombination processes exist to restore the system to equilibrium. Under reverse bias, carrier concentrations in the depletion region fall far below their equilibrium concentrations. The dominant generation-recombination processes are electron and hole emissions through generation-recombination centers with energies in the forbidden gap. The capture processes are not important because their rates are proportional to the concentration of free carriers. Under forward bias, the concentrations of both electrons and holes exceed their equilibrium values. The carriers will attempt to return to their equilibrium values by recombination. Therefore, the dominant generation-recombination processes in the depletion region are the capture processes. In the case of injection of excess carriers, the mechanism that restores equilibrium is recombination of the injected minority carriers with the majority carriers. Recombination phenomena can be classified as direct and indirect processes. Direct recombination usually dominates in direct-bandgap semiconductors such as gallium arsenide, whereas indirect recombination via bandgap recombination centers dominates in indirect-bandgap semiconductors such as silicon. Fig.3.3 [86] shows a diagram of surface recombination. Surface recombination happens when the abrupt discontinuity of the lattice structure at the surface, a large number of localized energy states or generation-recombination centers may be introduced at the surface region. These energy states, called surface states, may greatly enhance the recombination rate at the surface region.

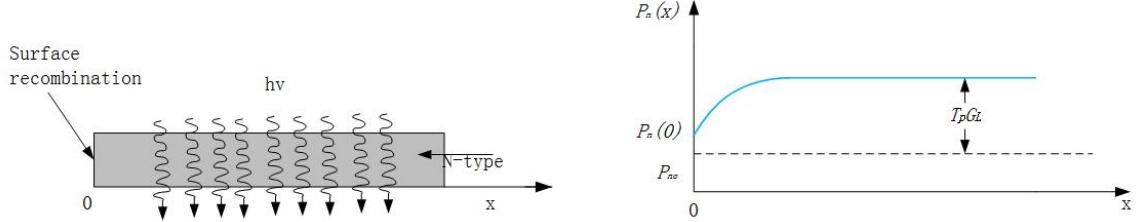


Figure 3.3 Surface recombination at $x=0$. The minority carrier distribution near the surface is affected by the surface recombination velocity [86].

Fig. 3.3 shows the effect of surface recombination in a semiconductor sample under illumination. The surface recombination leads to a lower carrier concentration at the surface. This gradient of hole concentration yields a diffusion current density that is equal to the surface recombination current.

3.1.4 Junction breakdown

Junction breakdown occurs when the peak electric field in the *pn* junction reaches a critical value as shown in Fig.3.4 [86]. When forward bias is applied to the junction, the current increases rapidly as the voltage increases. However, when a reverse bias is applied, a sudden current flow until a critical voltage is reached, this sudden increase in current is referred to as the junction breakdown. Two important breakdown mechanisms are the tunnelling effect and avalanche multiplication. Avalanche breakdown limits the collector voltage of a bipolar transistor and the drain voltage of a MOSFET.

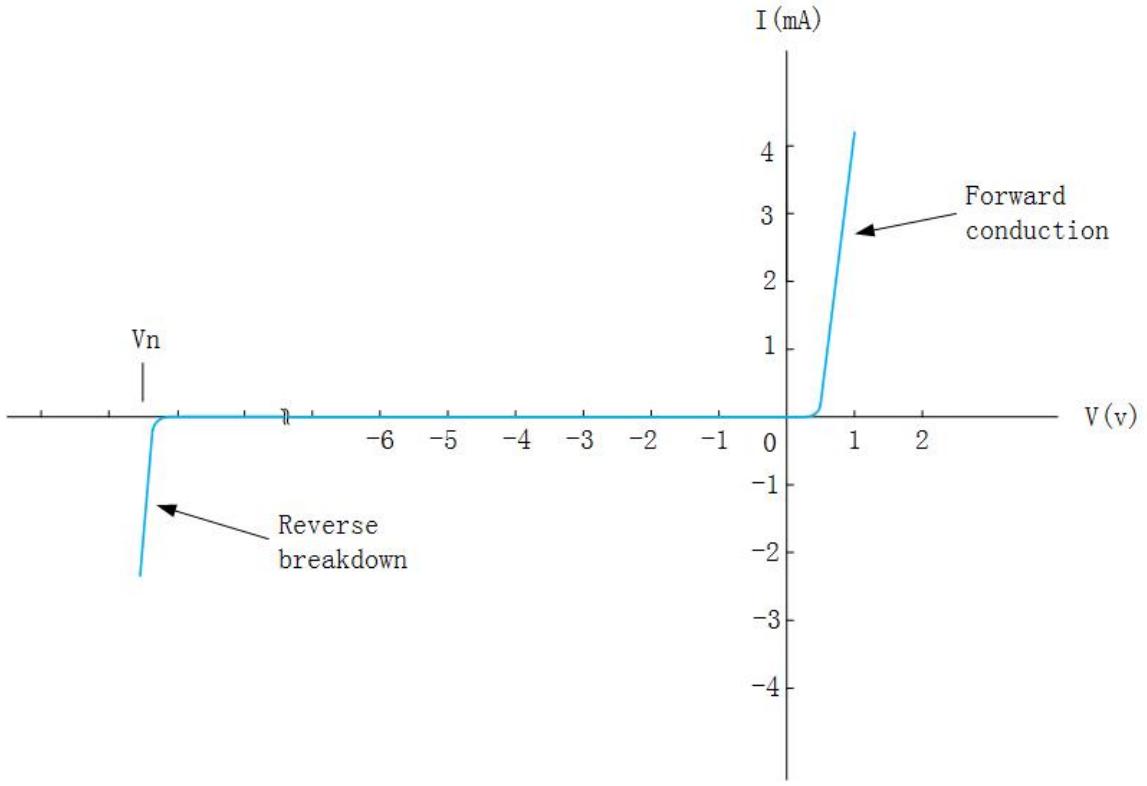


Figure 3.4 Reverse breakdown IV characteristics in *pn* junction [86]

The peak electric field is found at $x=0$, and is given by

$$\mathcal{E}_p = \mathcal{E}(0) = \left[\frac{2qN}{\epsilon_s} (\phi_{bi} + |V_r|) \right]^{1/2} \quad 3.1.8$$

When the electric field reaches some critical value, breakdown occurs and can be calculated by

$$V_B = \frac{\epsilon_s \mathcal{E}_{crit}^2}{2qN} - \phi_{bi} \quad 3.1.9$$

Where N is the lightly-doped side density of one-sided junction.

3.2 Bipolar Junction Transistors (BJTs)

The Bipolar Junction Transistor (*BJT*) was invented by Bardeen, Brattain and Shockley at the Bell Telephone Laboratories in 1948 [88]. Bipolar transistors are used extensively as discrete devices or in integrated circuits, it is still desirable in BiCMOS technology applications today because of its advantage in high speed, low noise, and high output power. In bipolar transistors, the current flows in the bulk of the semiconductor materials as opposed to the surface layer of a field-effect transistor. The most common structures are vertical devices but a low-performance lateral structure is also used in some applications. Fig. 3.5 illustrates a npn *BJT* made of a heavily doped *n*-type emitter, a *p*-type medium doped base, and an *n*-type lightly doped collector [89]. A *npn* transistor exhibits higher trans-conductance and operation speed than a *pnp* transistor of comparable structure because electron mobility is larger than the hole mobility.

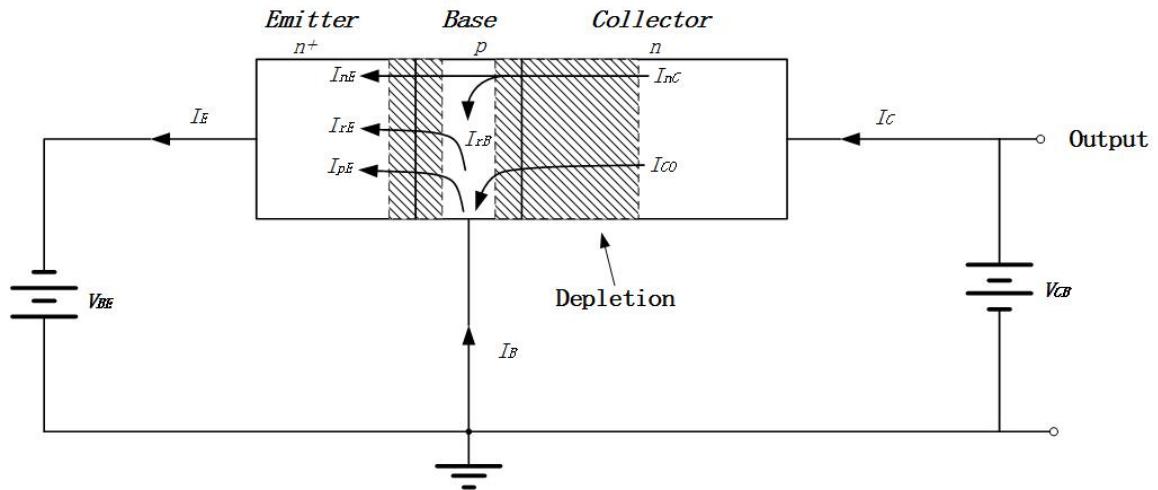


Figure 3.5 An n-p-n transistor biased in the normal operating conditions [89]

The collector current I_C is the output current of BJT in a forward bias and can be calculated from 3.2.1 [89]:

$$I_C = \frac{A_E q D_B n_i^2}{N_B W_B} \left(e^{|V_{BE}|/V_T} - 1 \right) \cong I_S \left(e^{|V_{BE}|/V_T} - 1 \right) \quad 3.2.1$$

Where A_E is the area (in cm^2) of emitter, D_B is the minority carrier (electron) diffusion constant in the base, N_B is the base doping concentration, W_B is the width of base neutral region, and V_{BE} is the forward bias cross the base and the emitter.

I_S is the reverse saturation current of base-emitter pn junction expressed in 3.2.2 [89].

$$I_S = A_E q n_i^2 \left[\frac{D_B}{N_B W_B} + \frac{D_E}{N_E W_E} \right] \cong \frac{A_E q D_B n_i^2}{N_B W_B} \quad 3.2.2$$

The base current is usually primarily comprised of carrier flow from base into emitter and can be calculated by equation 3.2.3 [88]

$$I_B = A_E q \frac{D_E n_{iE}^2}{W_E N_E} (e^{qV_{BE}/kT} - 1) \quad 3.2.3$$

where D_E is the minority carrier diffusion constant within neutral emitter region, N_E is the dopant concentration in base, and W_E is the width of the neutral emitter region. In a real transistor, there is a generation current in the depletion region of the reverse-biased base-collector junction. This current is added to the leakage current. A forward-biased base-emitter junction has a recombination current in its depletion region which is added to the base current. This recombination current has a profound effect on the current gain because it is the dominant current component at low-current levels. The common-emitter

current gain is β_F which ignoring depletion region recombination can be calculated by

3.2.4 [89]

$$\beta_F \equiv \frac{I_C}{I_B} = \frac{D_B W_E N_E n_{iB}^2}{D_E W_B N_B n_{iE}^2} \quad 3.2.4$$

According to the equation above, the most efficient way to obtain high gain is to use larger N_E and smaller N_B , however, a small N_B introduces too large a base resistance which degrades the *BJTs* performance at high frequency, typically N_B is around 10^{18} cm^{-3} . Reducing W_B can also obtain high gain, but it is not possible in a lateral *BJT*.

Fig. 3.6 shows typical base and collector characteristics as function of base-emitter voltage V_{BE} . Four regimes are observed: (1) the low-current non-ideal regime, recombination is more pronounced and base current varies as $\exp(qV_{BE}/2kT)$; (2) the ideal regime; (3) the moderate-injection regime with significant voltage drop on the base resistance R_B ; (4) the high –injection regime. The base resistance is given by 3.2.5 [89]

$$R_B = \frac{R_{\square} S}{12X} \quad 3.2.5$$

Where R_{\square} is the base sheet resistance, S is the emitter strip width, X is the size of emitter perpendicular to S .

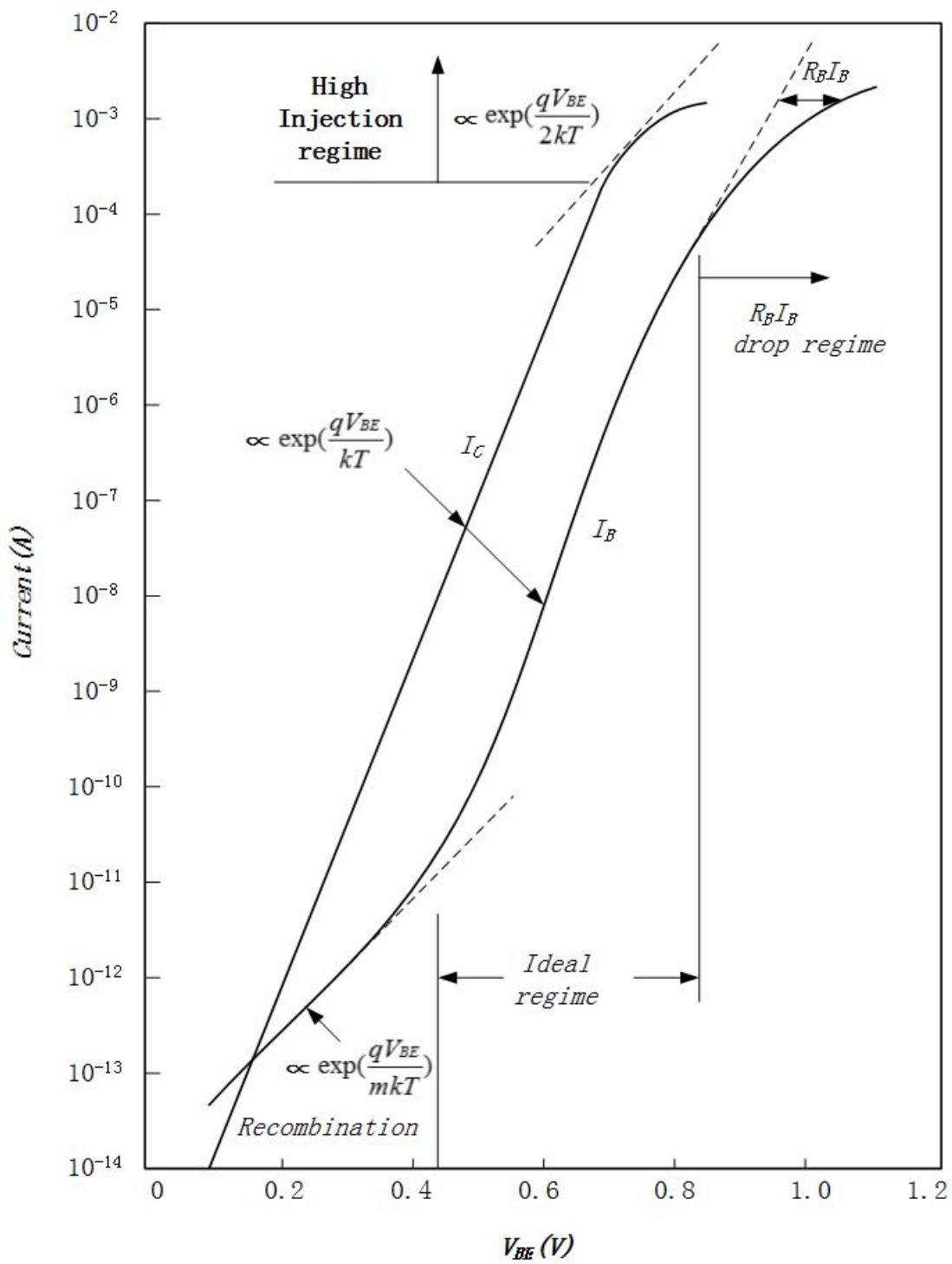


Figure 3.6 Collector and base current as a function of base-emitter voltage [89]

Fig.3.7 shows the output current of a typical *n-p-n* transistor in common-emitter configuration. I_{CEO} is the saturation current with the collector current with open base current. The current I_C increases with V_{CE} increases, the neutral base width W decreases when V_{CE} increases. The voltage V_A is the Early voltage where the extrapolated output curves meets on x-axis. For a transistor with base width much larger than the depletion region in the base, the V_A is given by 3.2.6

$$V_A = \frac{qN_B W_B^2}{\epsilon_s} \quad 3.2.6$$

Where W_B is the base width, N_B is the base doping concentration, ϵ_s is silicon permittivity.

As V_{CE} increases the collector current starts to increase rapidly, V_{BCEO} is the breakdown voltage. In conclusion, the high doping in the emitter is good for injection efficiency. The high base doping and base width are useful for a high Early voltage. The collector has the lowest doping for high breakdown voltage [89].

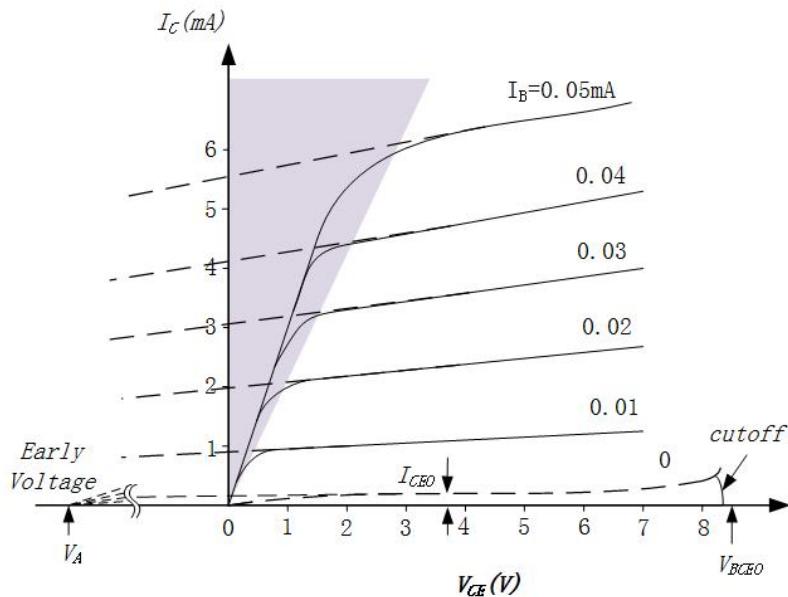


Figure 3.7 Output characteristics of an *n-p-n* transistor in common-emitter configuration

Considering high-speed applications, transconductance g_m is one of main figures-of-merit for high speed circuits. Taking into account the base width modulation effect, there is a finite output conductance g_{EC} and input conductance g_{EB} , g_m is defined in 3.2.7 [89]

$$g_m \equiv \frac{dI_C}{dV_{BE}} = \left(\frac{q}{kT}\right) I_C \quad 3.2.7$$

A high transconductance g_m benefits large current drive which makes *BJTs* is attractive for high-speed applications. The transconductance g_m and input conductance g_{EB} are dependent on the common-base current gain. At low frequencies, the current gain is a constant, independent of the operation frequency. However, the current gain will decrease after a critical frequency f_T is reached. g_m is proportional to the cut-off frequency f_T which is given in 3.2.8 [89].

$$f_T = \frac{g_m}{2\pi C'_{in}} \quad 3.2.8$$

Where C' is the total capacitance including parasitic capacitance, diffusion capacitance and depletion capacitance in a *BJT* structure. The cutoff frequency can also be expressed as $(2\pi\tau_T)^{-1}$, where τ_T is the total time of the carrier transit from the emitter to the collector. The most important is the effective minority-carrier velocity in the base. To improve the frequency response, the transit time of minority carriers across the base must be short. The key device parameter of a bipolar transistor is the base width, which must be very small compared with the minority-carrier diffusion length to improve the current gain and to increase the cut-off frequency.

3.3 Junction Field-Effect Transistors (JFETs)

The Junction Field-Effect Transistor (JFET) was proposed by Shockley in 1952. The JFET has the advantage of avoiding interface traps and reliability issues arising from hot-electron injection and trapping related to the oxide-semiconductor interface in MOSFETs. This is because only majority carriers transport through the channel in the bulk and free of surface or interface scattering in the JFET operation. It is useful for low-noise amplification and high-efficiency power generation applications [89].

The JFET is basically a voltage-controlled resistor and available in two types: *n*-channel and *p*-channel. Fig. 3.8 [89] shows a schematic structure of the *n*-channel JFET. The basic dimension is: the channel length L , channel depth a , depletion-layer width W_D , net channel opening b , and channel width Z (into the page). It consists of a conductive channel provided with two ohmic contacts, one acting as the source and the other as the drain. Two *p*-type regions electrically connected together on its side to form the gate. The gate forms a *p-n* rectifying junction and controls the net opening of the channel by varying the depletion width. It uses reverse bias on this junction to control the channel width and hence the current flow from drain to source.

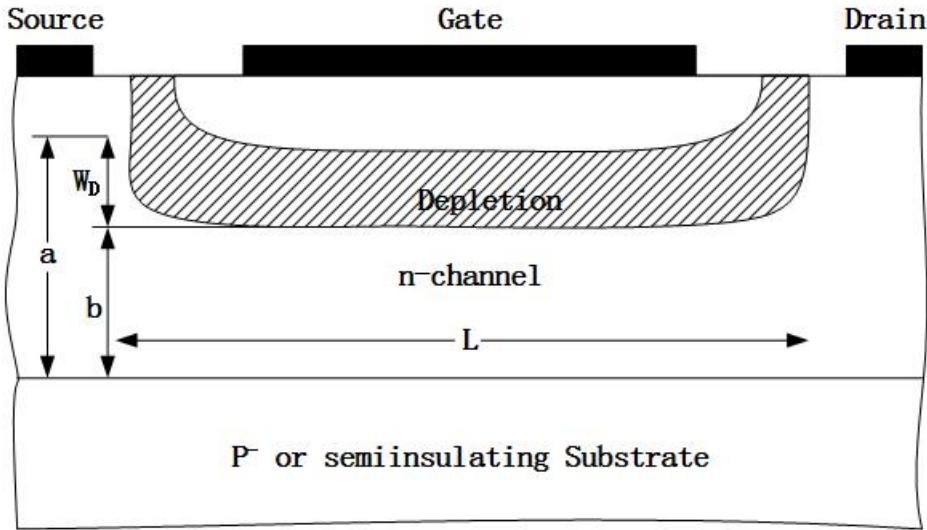


Figure 3.8 Schematic structure of *n*-channel JFET [89]

The basic current-voltage characteristics of a *JFET* is shown in Fig. 3.9. When $V_G=V_D=0$, the device is in equilibrium and there is no current conduction. If the drain is biased at small positive value while the gate voltage V_G is equal to zero, the current of electrons flowing from source to drain is due to drift mechanism. When negative gate voltage is applied to the cross-sectional area of the channel through which electrons flow shrinks, the resistance of the channel increases and the drain current decreases. If the two depletion regions meet no current can flow between source and drain, the gate voltage for which the depletion zones meet is called the “threshold voltage” V_{th}

$$V_{TH} = \Phi_0 - \frac{q N_d a^2}{2 \epsilon_{si}} \quad 3.3.1$$

For a given V_G above the threshold voltage, the channel current increases with the drain voltage. Eventually the current will saturate to a value I_{Dsat} for sufficiently large V_D .

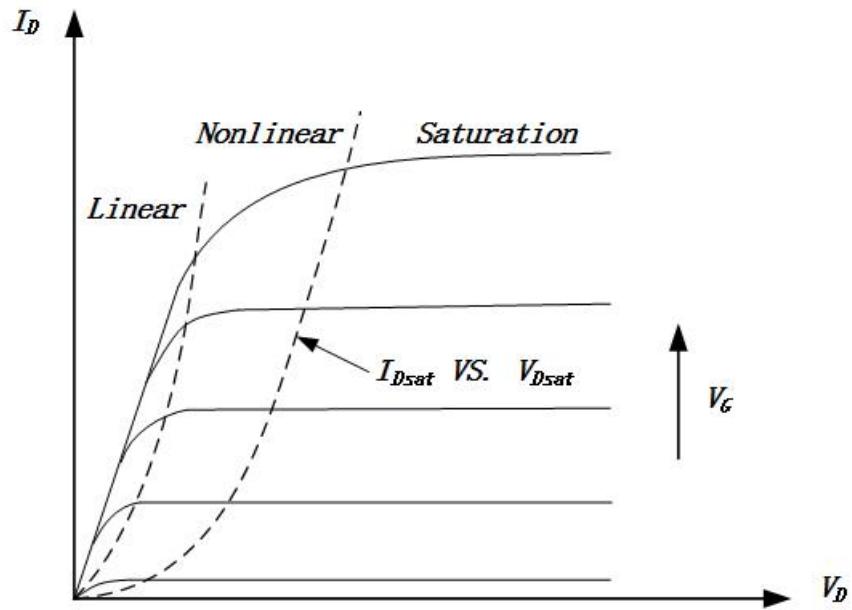


Figure3.9 General I-V characteristics of the JFET [89]

Furthermore, when the drain voltage is increased to given value called “saturation drain voltage”, and denoted $V_{D\text{sat}}$, the two depletion regions will touch one another near the drain. This phenomenon is known as the channel “pinch-off” in Fig.3.10 [89].

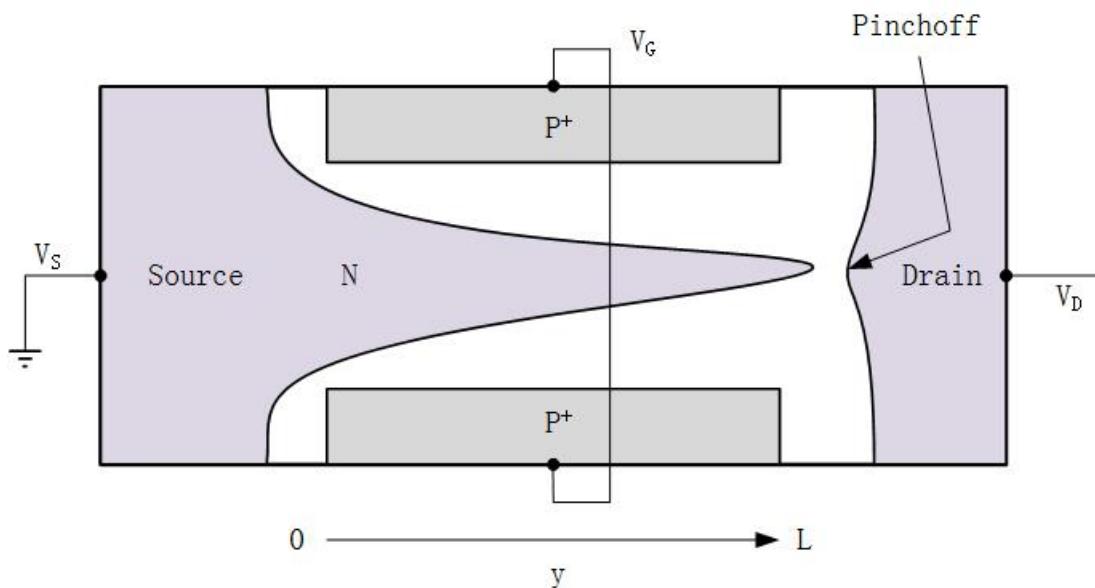


Figure 3.10 Cross-section view of the JFET channel pinch-off

The value of pinch-off voltage can be expressed as:

$$V_p = \Phi_0 - \frac{qN_D a^2}{2\epsilon_{si}} \quad 3.3.2$$

As the drain voltage increases beyond V_p , breakdown occurs where the current rises sharply with the drain bias in JFET. The fundamental mechanism for breakdown is impact ionization. Considering the gate-drain structure as a reverse-biased diode, the drain breakdown voltage V_{DB} is linearly dependent on the relative voltage of the drain to the gate in 3.3.3.

$$V_{DB} = V_B - V_G \quad 3.3.3$$

Where V_B the breakdown voltage of the gate diode and is a function of channel doping level. The breakdown voltage can be improved by extending the region between the gate and the drain. Furthermore, field distribution should be made as uniform as possible to maximize its function. The transconductance g_m and cutoff frequency are important parameters in JFET analysis. The transconductance gm is defined as 3.3.4 [90]

$$g_m = ZC_{GS}v_s \quad 3.3.4$$

where Z is the channel width, C_{GS} is the gate-source capacitance, v_s is the velocity saturation. This equation shown that g_m is constant and totally independent of gate bias as well as channel length. In real applications, it is often preferable to have good linearity such as constant g_m meaning I_{Dsat} changes linearly with V_G .

The cutoff frequency f_T is used to evaluate high-speed capability in amplified circuit applications. It is defined as the frequency of unity gain is expressed in 3.3.5 [86].

$$f_T = \frac{g_m}{2\pi C'_G} = \frac{v}{2\pi L} \quad 3.3.5$$

Where C_G' is the sum of gate-source capacitance and gate-drain capacitance, L is the channel length and v is the carrier drift velocity. The f_T is related to the transit time for a carrier to travel from source to drain. The drift velocity v is equal to the saturation velocity v_s for short channels. The speed limitations of *JFETs* are dependent on device geometry and material properties. It can be improved by reducing gate length L as decreasing L will decrease the total gate capacitance C_G' and increase the transconductance g_m (before velocity saturation) based on the equation 3.3.5.

3.4 Integrated Photodetectors

The Photodetector is essential to convert optical energy to electrical signals in opto-electronics integration. Monolithic integration of the photodetector and readout circuitry has benefits of reducing capacitance and improving reliability in a more compact system. It is better to implement integration in a standard BiCMOS or CMOS circuit technology [91]. For example, the Schottky diode formed between gate metal and the semiconductor can be used in a MESFET technology [92], the base-collector may be used as photodiodes in a bipolar technology [93], and the n-well to p-substrate or the p+ to n-well junction maybe serve as photodiodes in wavelength around 1550 nm detections [94].

3.4.1 Germanium waveguide photodetector

Si is transparent through the wavelength 1250-1650 nm, so bulk Si *pn* junctions are not useful for photodetection in the 1300-1500 nm wavelength range commonly used for silicon photonics. The Ge photodetector is an ideal candidate for infrared optical

detection since it shows strong absorption around wavelength 1550 nm. It has been significantly developed despite the large lattice mismatch (4.2%) between Si and Ge.

Two kinds of Ge photodetectors have been demonstrated including surface illuminated photodetectors and SOI waveguide photodetectors. For waveguide Ge photodetectors, the absorption path is in the longitudinal direction along the waveguide which enables full absorption of the input optical power. On the other hand, carrier collection is implemented in a transverse direction which minimizes carrier transit time, so high responsivity and high bandwidth can be simultaneously obtained in a Ge waveguide photodetector [95]. The structure of a vertical Ge waveguide p-i-n photodetector is illustrated in Fig. 3.11 [96].

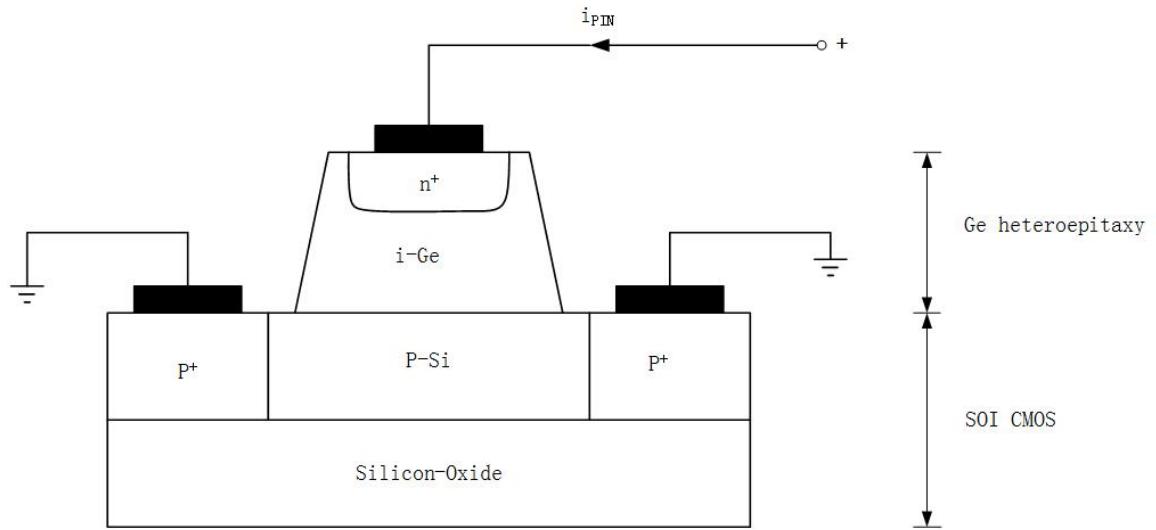


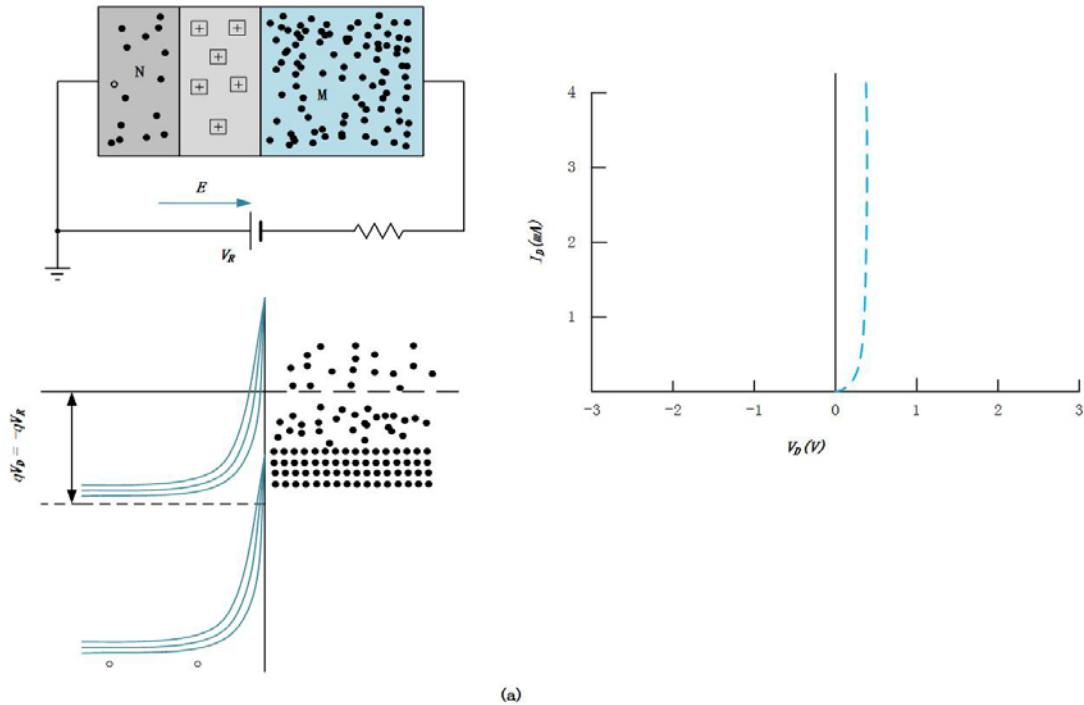
Figure 3.11 MOS compatible Ge p-i-n photodetector

As illustrated in the Fig.3.10, the intrinsic Ge absorption layer is located on top of the silicon waveguide to form a vertical p-i-n structure. Depositing Ge directly on silicon may lead to the formation of tensile strain due to the thermal mismatch between the Si

and Ge layers [97]. Tensile strain has the effect of extending energy edge for strong absorption from 1550 nm to 1620 nm, which covers both C-band (1530-1560 nm) and L-band (1560-1620 nm) used in long-haul fiber-optic communications [98].

3.4.2 Metal-Semiconductor (Schottky) photodetector

The Schottky photodetector has the advantage of simplicity and planarity. It can be integrated with waveguides without adding fabrication complexity [99-101]. Schottky diodes have current-voltage characteristics dominated by majority carriers without stored-charge effect of minority carriers, which makes Schottky diodes suitable for fast switching application [102]. Fig. 3.12 illustrates reverse-biased and forward-biased characteristics of Schottky diode.



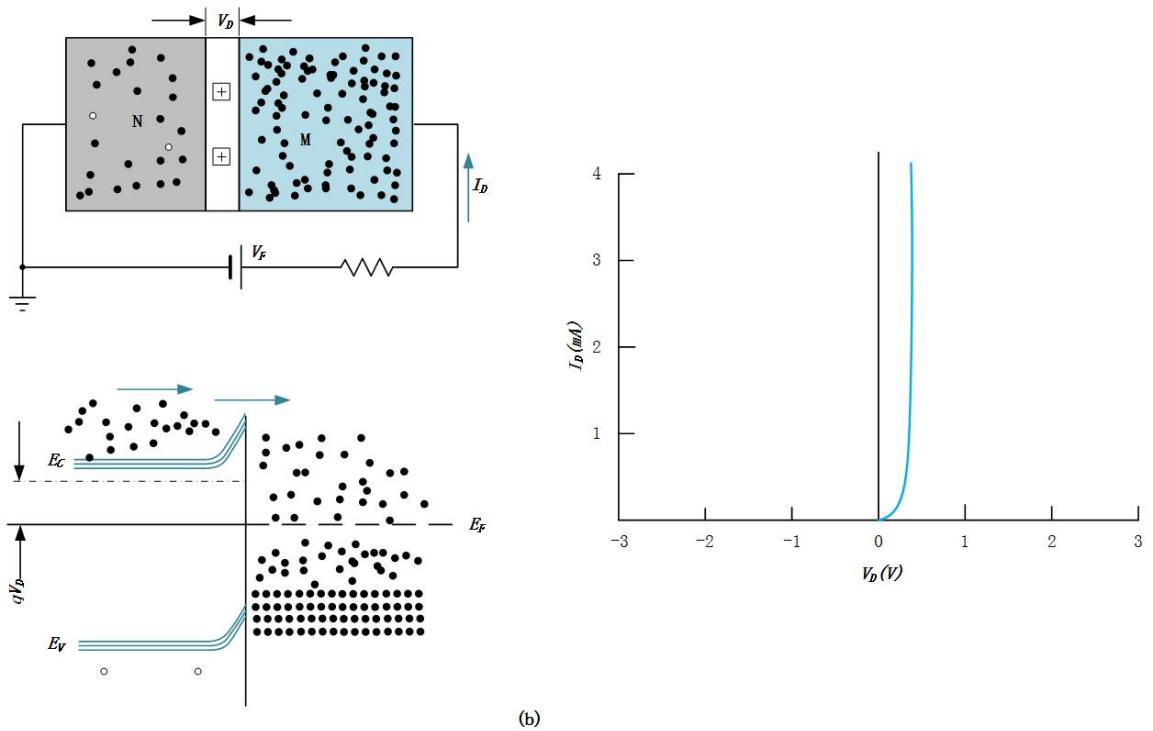


Figure 3.12 Schottky diode at reverse-bias(a) and forward-bias (b) [102]

At a reverse bias, negative voltage applied increases the energy barrier height in the depletion layer of semiconductor prevents the electrons moving from the semiconductor through the contact. Schottky diode current I_S is generated due to thermal emission of electrons over the barrier $q\phi_B$ expressed in 3.4.1 [102]

$$I_S = A_J A^* T^2 e^{-q\phi_B/kT} \quad 3.4.1$$

Where A_J is the diode area, T is absolute temperature, $q\phi_B$ is the barrier height, and A^* is the effective Richardson constant. At a forward bias, the positive voltage applied reduces the energy barrier height in the depletion layer. This enables a number of electrons

overcome the barrier from semiconductor into metal. The current of Schottky diode can be expressed in 3.4.2

$$I_D = I_S e^{V_D/nV_t} \quad 3.4.2$$

3.5 Transimpedance Amplifiers

The Transimpedance amplifier (TIA) is used to convert photodetector current to an output voltage which proportional to the input current. Here we review examples circuit constructed by CMOS, BICMOS and JFET technologies [103]. Fig. 3.13 shows circuit schematic of an NMOS transimpedance preamplifier. It consists of a common-source amplifier M₁, a depletion load M₂ and a feedback transistor M₃ in the first stage. The second stage consists M₄ and M₅ further amplifies the signal and is used as a buffer to drive the depletion source follower M₇ at the output. The circuit demonstrates good performance by implementing NMOS transistors in reference [104].

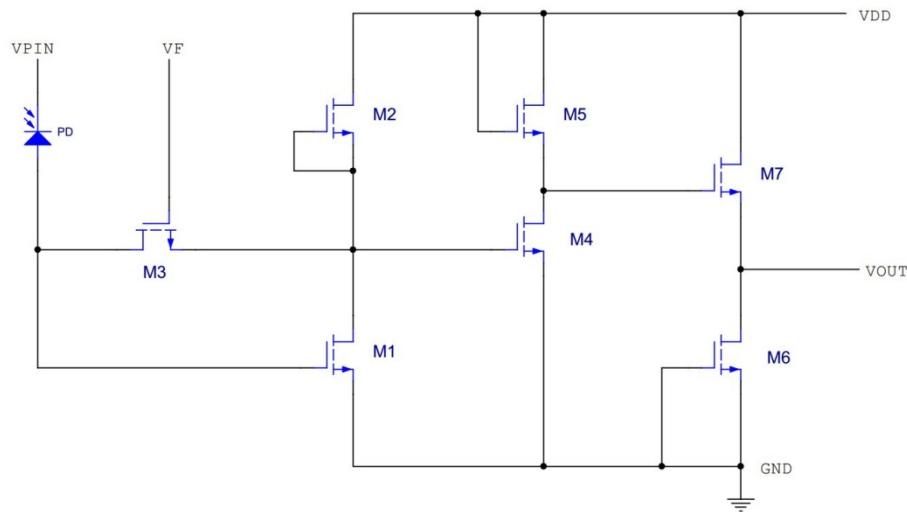


Figure 3.13 A NMOS transimpedance amplifier [104]

A BJTs transimpedance amplifier consists of a photodiode, a common emitter gain stage, two emitter follower buffers, and a resistive feedback loop in Fig. 3.14. The transistors Q₁, Q₄ and Q₅ are used as level shifting diodes. Q₁ and Q₅ reduce V_{CE} of Q₂ and Q₆, respectively. The two voltage supplies V_{DD} and V_{CC} are used to optimize the operating point of the amplifier. The feedback resistor R_F determines the bandwidth, gain, and noise characteristics of the amplifier. The value is usually chosen based on a trade-off between these three parameters.

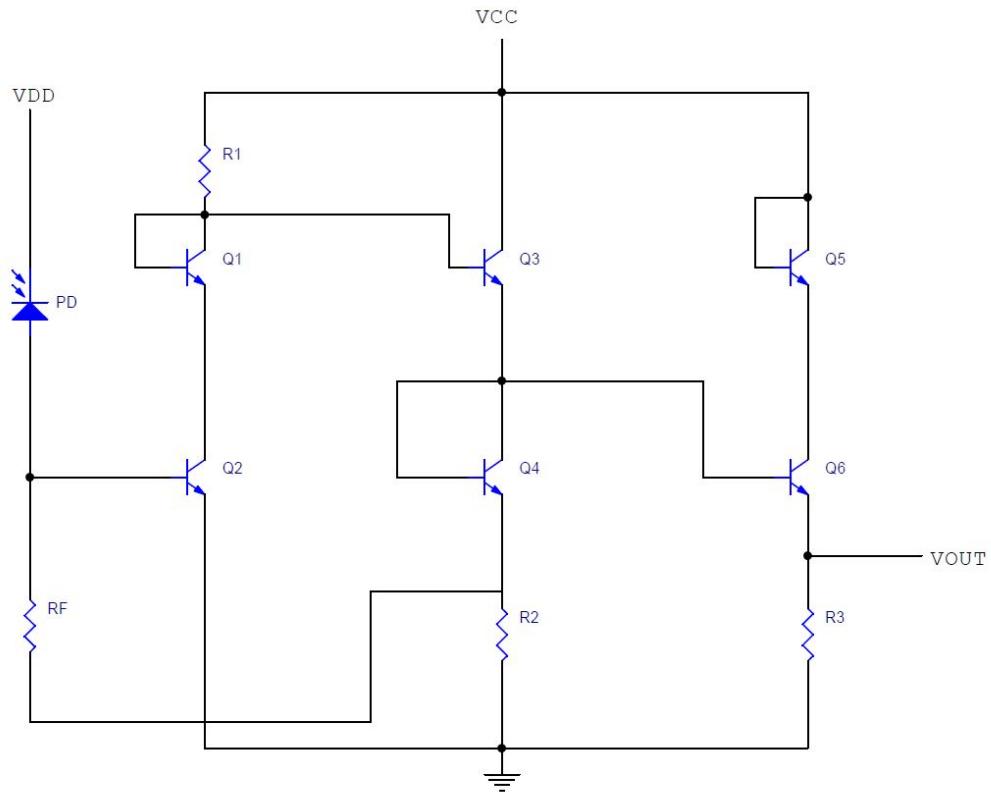


Figure3.14 Circuit diagram of a bipolar transimpedance amplifier [105]

A circuit schematic of the JFET-based transimpedance amplifier is shown in Fig. 3.15 [106]. Q₁ is a common-source JFET amplifier with source degeneration, the circuit

provides a feed back loop consisting of a feedback resistor R1 and a DC blocking capacitor C1.

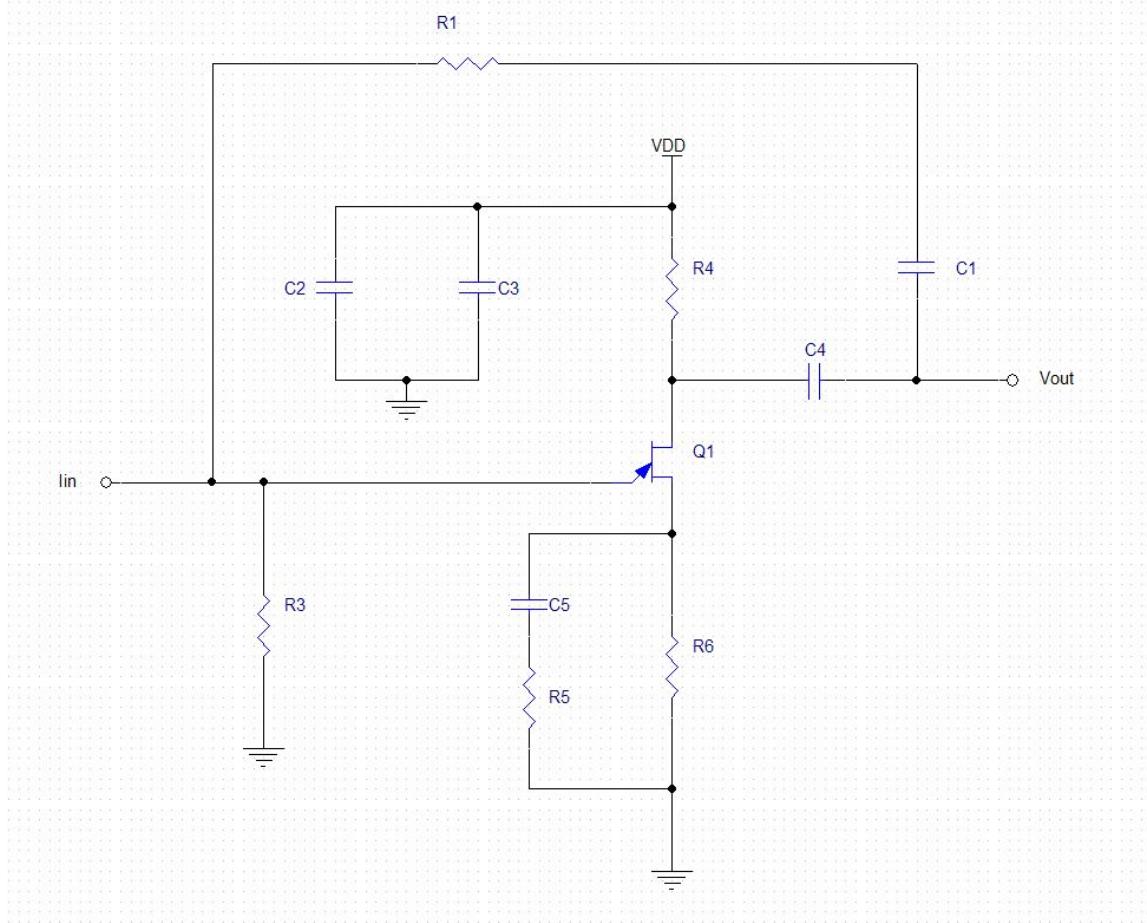


Figure 3.15 JFET-based common-source transimpedance amplifier [106]

Comparing with the three TIA examples constructed by *MOSFETs*, *BJTs* and *JFETs*, *JFETs* offer the best noise performance with high transconductance and low gate-cutoff voltages. It is the best choice for discrete low-noise design, particularly when low noise is required in low frequency applications [107].

Chapter 4: Monolithic Integration of Silicon Photonics and Electronic Circuitry in a Foundry Technology

This chapter focuses on demonstrating the monolithic integration of conventional electronics with SOI photonics using the commercial silicon photonics foundry technology offered by A*STAR’s Institute of Microelectronics (IME) in Singapore. Access to this technology was supported by CMC Microsystems (CMC) and arranged through CMC’s Silicon Electronic Photonic Integration Circuit (SiEPIC) workshop in 2015. Using a foundry platform provides advantages on resource efficiency, cell accessibility and design transferability [108]. The IME process is intended for integration of passive photonic devices (waveguide, grating couplers, multiplexer etc.) and active photonic devices (modulators, Ge photodiodes, resonators etc.) onto a monolithic chip. Various *n*-type and *p*-type ion implants for *pn* junction formation used in optical modulators and epitaxial Ge photodetectors are available [109]. Although the process was not intended to create transistors, it occurred to us that these implants could be used to create lateral bipolar junction transistors (*LBJTs*) and junction field effect transistors (*JFETs*). Although the silicon MOSFET is the workhorse device of modern electronic design, the IME process does not support the fabrication of MOS devices due to lack of polysilicon deposition and a high-quality gate oxide formation. Therefore, we chose to demonstrate the integrated electronic components using *LBJTs* and *JFETs*. We also focussed on SOI-based photonic sensing application, because the speed requirements of sensors are usually much more relaxed than those needed in telecommunications.

4.1 The SiEPIC Fabrication Process

The IME technology uses Silicon-on-Insulator (SOI) substrate which are commonly used in silicon photonics and in the electronics industry. The typical 200 m m (8") wafer

consists of a 700 μm silicon substrate, 2 μm buried oxide and 220 nm top crystalline silicon layer as shown in Fig. 4.1. The top silicon layer is the active region for waveguide and devices formation. The buried oxide layer provides isolation for electronic and photonics devices.



Figure 4.1 Cross – section view of starting SOI wafer

The basic passive device is a strip waveguide which is usually used for carrying and routing light for modulators and photodetectors. Optical loss is a main concern of waveguide transmission. In a 500 nm \times 220 nm strip waveguide fabricated by the IME process, absorption loss due to contact metal layer above is around 1.8±dB/cm [110], the sidewall scattering loss is typically 2-3 dB/cm [111-113]. The bending losses of the strip waveguide is 0.1 dB per 90° for a bending radius of 1 μm and 0.01 dB per 90° for a bending radius of 5 μm [114]. The propagation loss and material loss for passive structure can be negligible as they are very small in the waveguide. Therefore, the strip waveguide is suitable for opto-electronic integration with quite small optical losses.

Beside the strip waveguide, a sub-bandgap photodetector is a critical component for monolithic integration. The epitaxy-grown Ge detector has been demonstrated in the IME

process flow as illustrated in Fig. 4.2 which is the cross-section view of a vertical Ge photodetector [115]. The thickness of intrinsic Ge region is controlled by Ge epitaxy and n+ doping conditions. The dark current can be reduced by inserting a low-thermal-budget anneal step after Ge epitaxial growth, the responsivity and speed in the low-voltage regime are also improved [116].

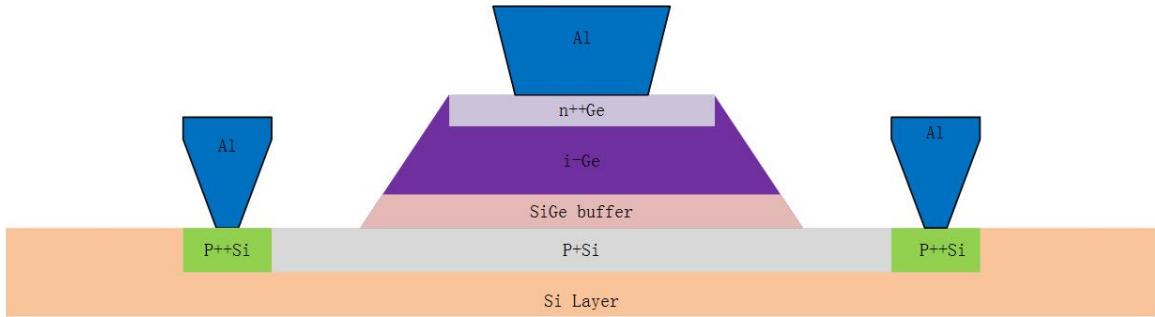


Figure 4.2 Cross section view of a PIN Ge photodetector

In addition, grating coupler is included for coupling light between fibre and sub-micrometer SOI waveguide. We use a confocal grating to couple light at the input and output of a strip waveguide in the IME process as shown in Fig. 4.3 [117, 118]. The grating lines are ellipses with a common focal point, which coincides with the optical focal point of the coupler. There are several parameters that decide the performance of a grating coupler: period, fill factor, incident angle, incident position, etch depth, thickness of SiO₂ substrate, thickness of the SiO₂ cladding, and number of grating periods. Etch depth and SiO₂ thickness are determined by the IME fabrication process. A shallow etch of 60 to 70 nm is optimal for grating couplers [119].

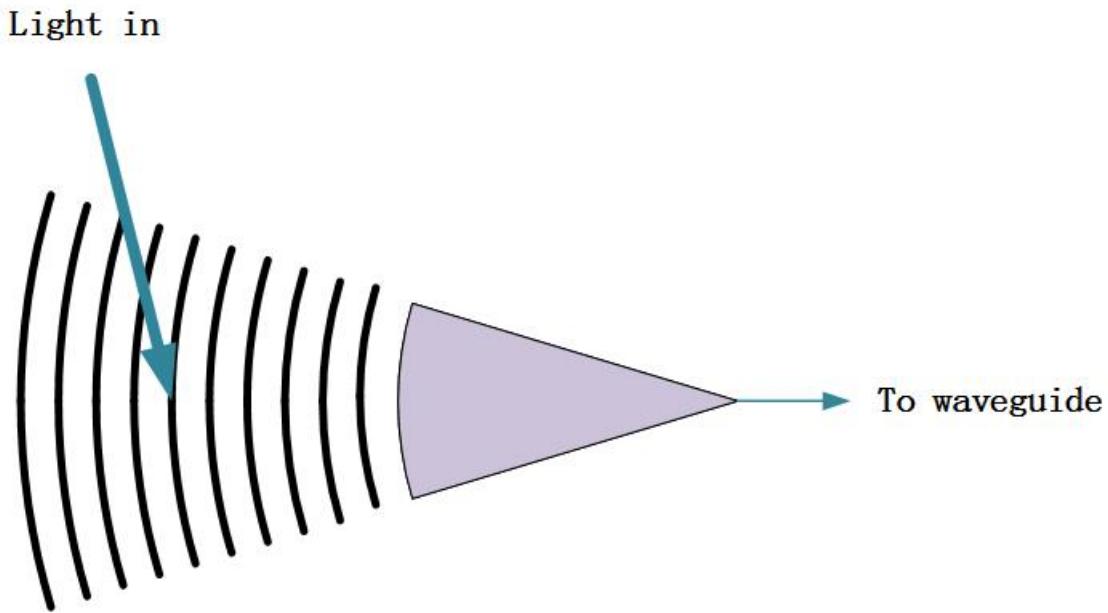


Figure 4.3 Mask layout of a fabricated grating coupler

The main steps in the process are listed below. A cross-section through the integrated structure is shown in Fig. 4.4 [109].

1. 3 steps of etching form optical waveguides by repeated photo-resist coating, exposure and dry etching
2. 6+ steps of ion implantation for optical modulators and Ge photodiode formation
3. 2 + metal depositions provide interconnection
4. Grating coupler and deep trench definition to enable facet fiber coupling

The process starts with a sequence of selective etching, hard mask deposition, waveguide formation, ion implants for modulators and photodetectors, Ge epitaxy, Ge top implant, and ends with metal connections and bond pads.

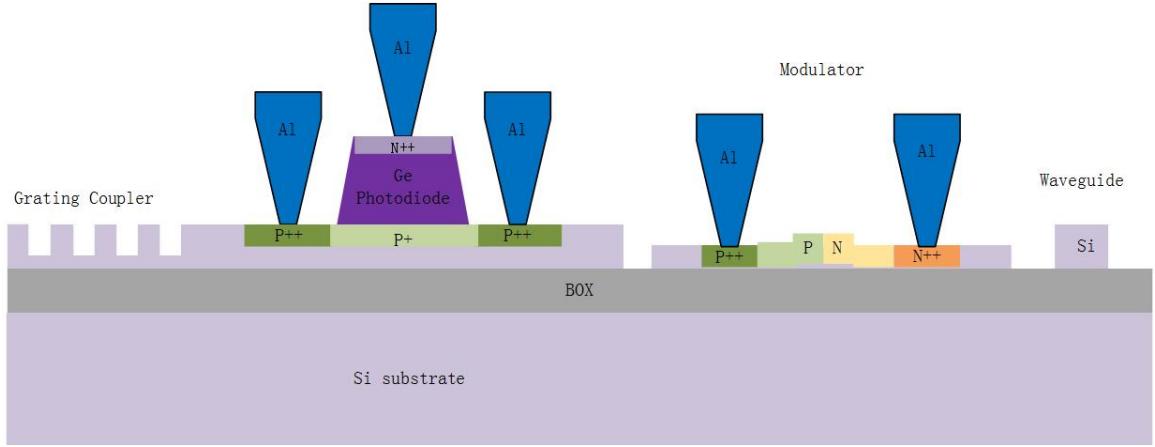


Figure 4.4 The cross - section view of the IME fabrication

4.2 Lateral *npn* BJTs Design

In order to be compatible with the IME fabrication process, *npn* BJTs implant and anneal condition were all given in the IME technology descriptions. All implant parameters were chosen based on practical *npn* BJT operation: an *n*- type heavily doped emitter, a *p*-type light doped base and an *n*- type medium doped collector. The lateral *npn* BJT structure used here is shown in cross-section in Fig. 4.5 (a), top view in Fig. 4.5 (b) and mask layout in Fig. 4.5 (c). A *npn* structure is used since electrons in silicon have a significantly longer minority carrier lifetime and diffusion length than do holes. A central *n*⁺⁺ emitter stripe is used to inject electrons that diffuse across the base to two *n*⁺ collector stripes at the outer edges of the Si area defining the device. Allowing for depletion region extension into the *p*-type region, the neutral base width was estimated as 6 μm at zero bias. Contact to the base was made through a *p*⁺⁺ region at one edge of the device.

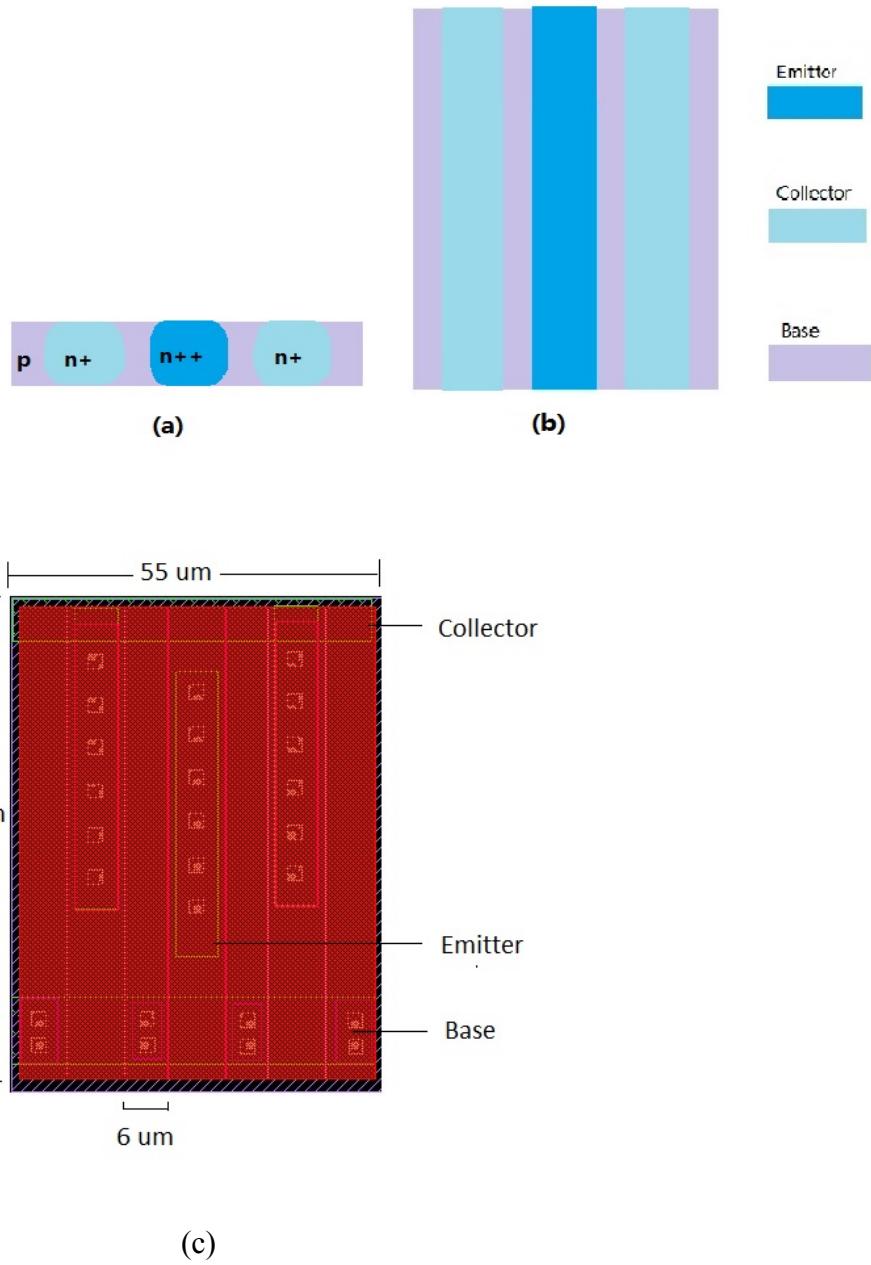


Figure 4.5 The cross-section view (a), top view (b) and the layout of LBJT structure (c)

The doping concentration in each region was estimated by Suprem4 simulation. The Suprem4 was developed by Prof. Dutton's group at Standford University, it was the first consistent approach to simulate the physical behaviour of dopants in two-dimensional cut through a wafer during semiconductor processing [120]. The input file is attached in

Appendix I. All implant doses, energies and anneal conditions were provided in PDK by the IME 's technology. The doping concentration is plotted in Fig. 4.6, Fig.4.7 and Fig.4.8 for base, collector and emitter region, respectively. An uniform distribution of n -type, p -type and $n++$ - type regions were obtained in the active silicon layer (220 nm). It is seen here that the emitter has the highest doping compared to the base, and the collect has the lowest doping level in a typical BJT design.

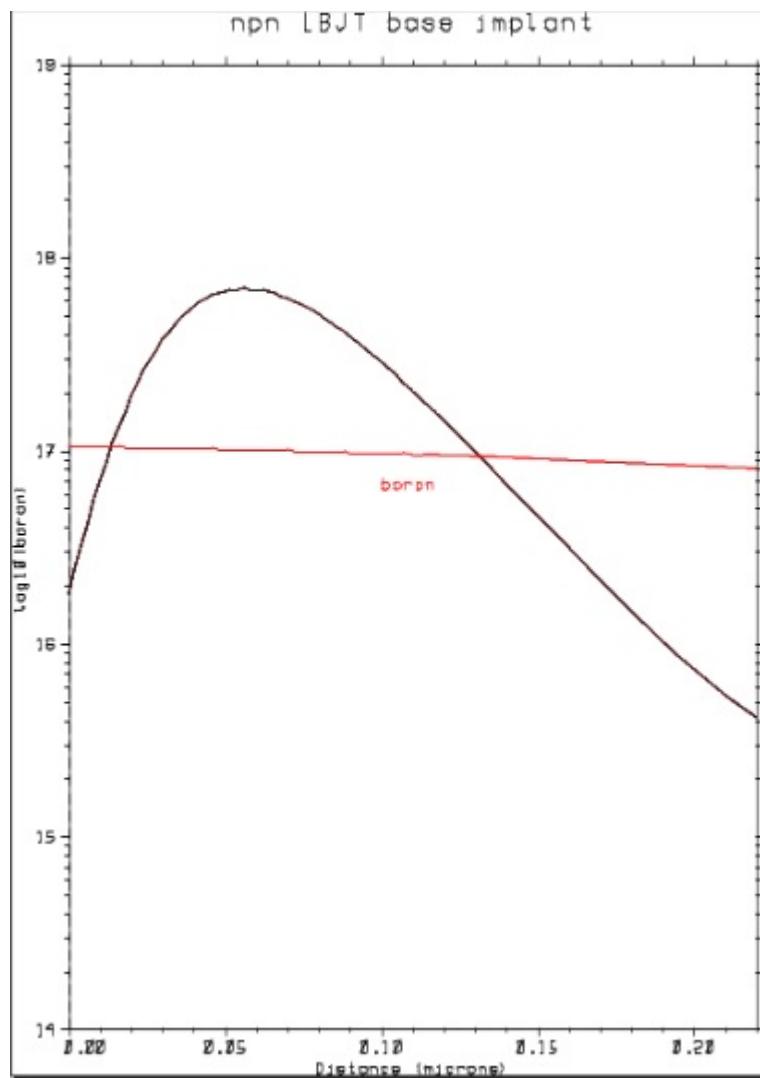


Figure 4.6 npn transistor base implantation

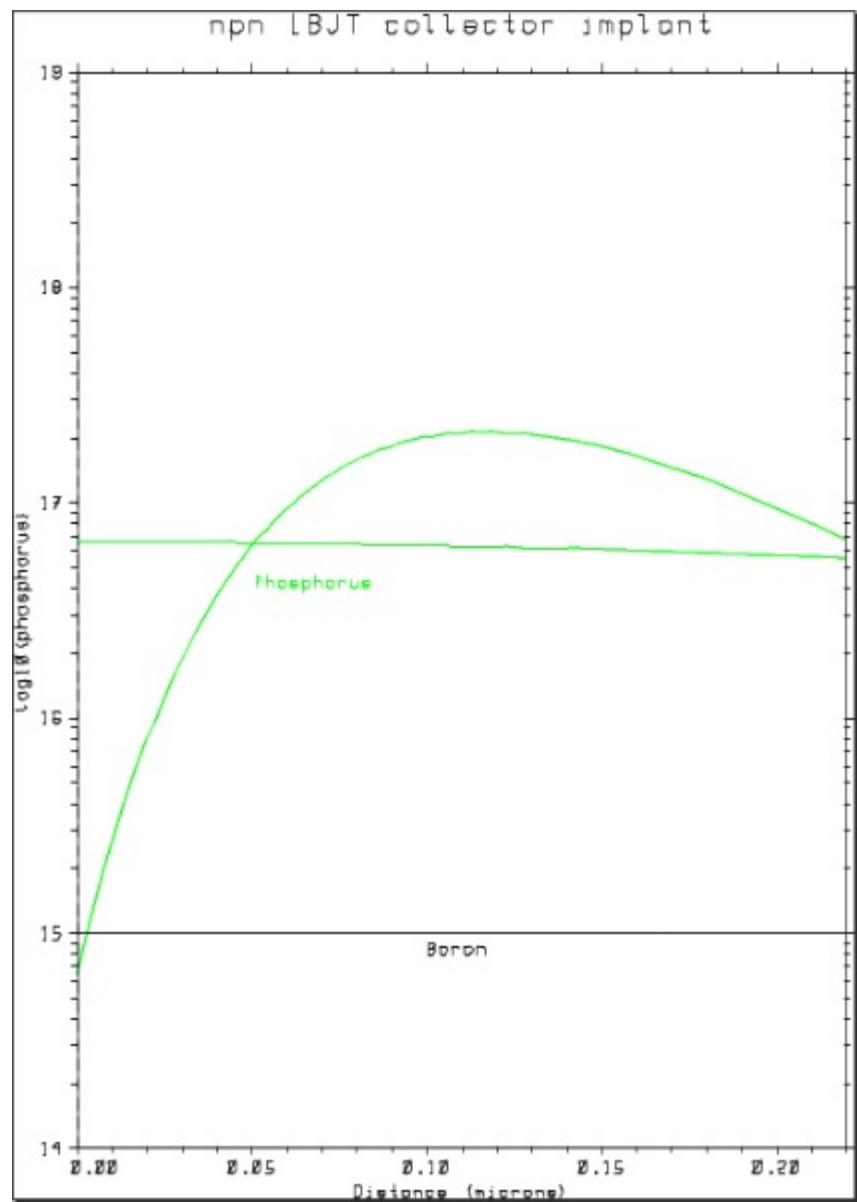


Figure 4.7 *npn* transistor collector implantation

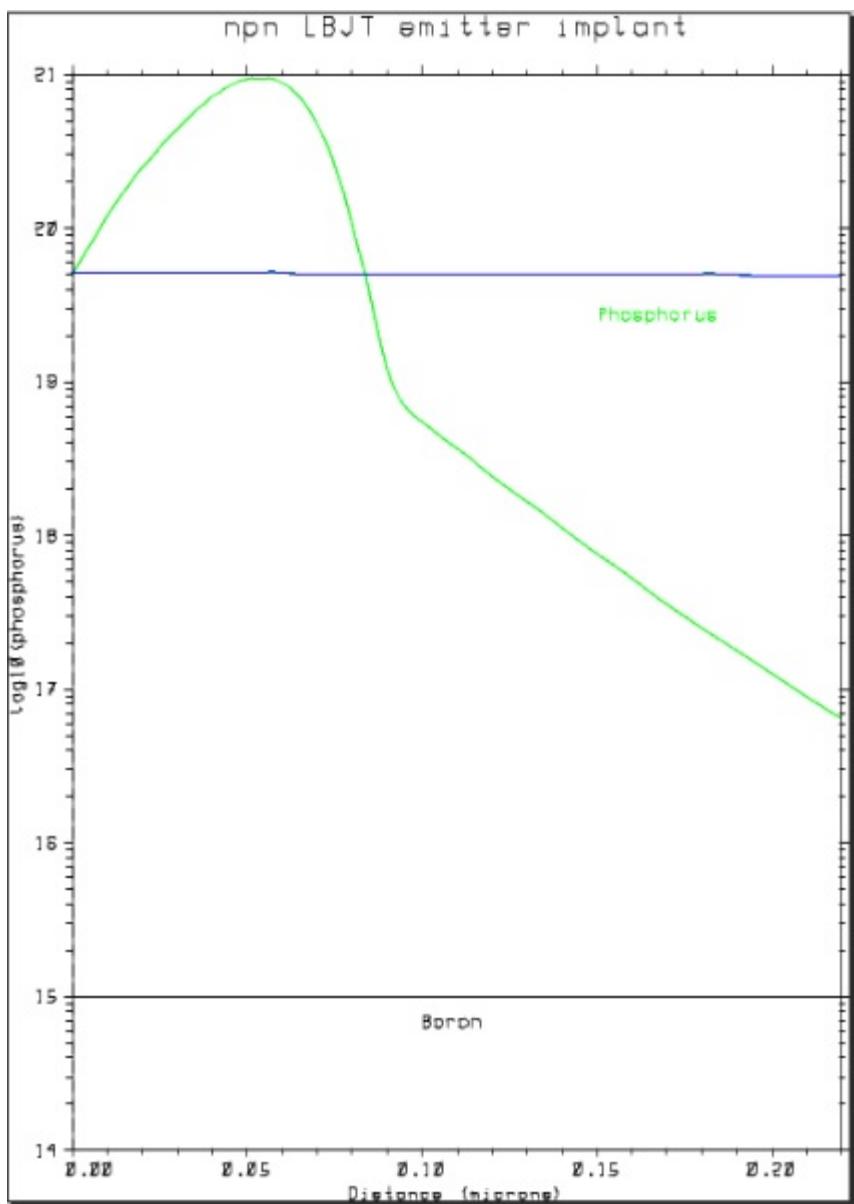


Figure 4.8 *npn* transistor emitter implantation

From the device structure established by these simulations Ebers-Moll model SPICE parameters in Table 4.1 were calculated based on equations given in the sections 3.1 and 3.2 of Chapter 3 [89]. The Ebers-Moll model is the classic mathematical model for the bipolar junction transistors, it provides the voltage-current equation for both forward and reverse static voltages applied across the transistor junction. A Gummel plot of calculated base and collector current versus V_{BE} is shown in Fig.4.9. As theoretical demonstration in

Fig. 3.6, The surface recombination-generation, series resistance and high level injection affect the Gummel plot. The “turn over” at the bottom of the I_B curve is due to recombination in the depletion region. The collector current does not include this additional current since the recombination does not affect the flow of electrons through the base. From the *BJT* characteristics in Fig. 4.10, the Early voltage V_A can be extrapolated at a point on x-axis where output curves meet. According to the equation 3.2.6, the base doping concentration and the base width are main factors dominated the Early voltage.

TABLE 4.1
LBJT HSPICE MODEL PARAMETERS

Parameters	Name (Units)	Values
Saturation current	I_S (A)	2.8e-18
Forward Beta	β_F	41
Reverse Beta	β_R	6.9
Base-emitter built in potential	V_{JE} (V)	0.98
Base-collector built in potential	V_{JC} (V)	0.81
Base-collector zero-bias depletion capacitance	C_{JC} (fF)	10
Base-emitter zero-bias depletion capacitance	C_{JE} (fF)	10.6
Base resistance	R_B (k Ω)	1.8
Early voltage	V_A (V)	139

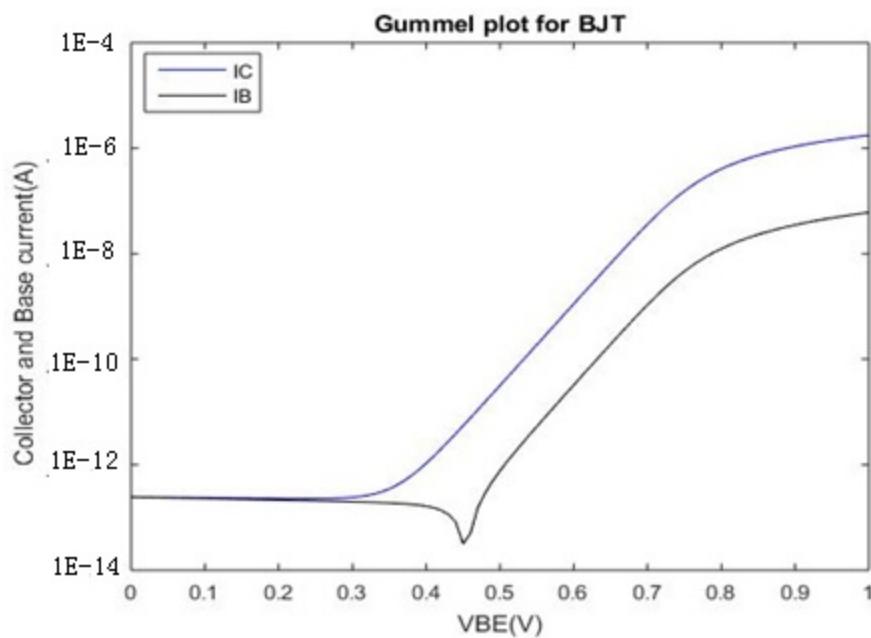


Figure 4.9 Hspice simulated Gummel plot

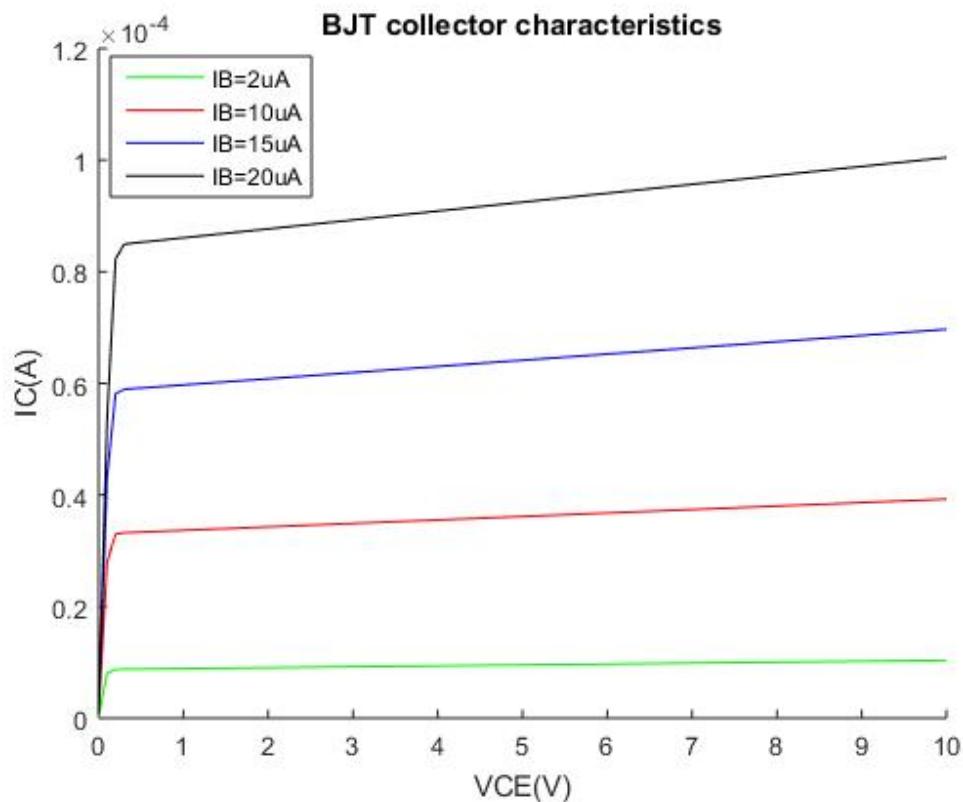
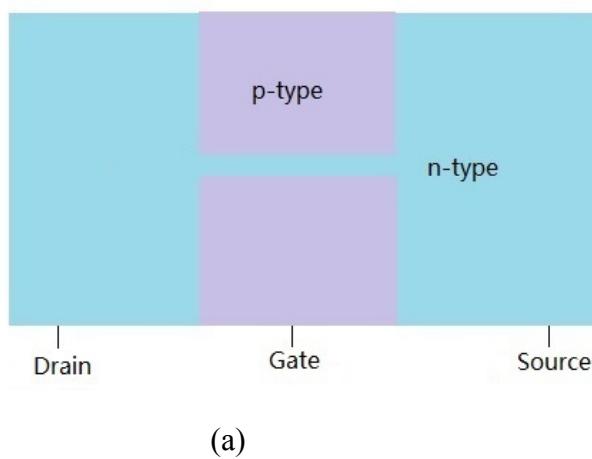


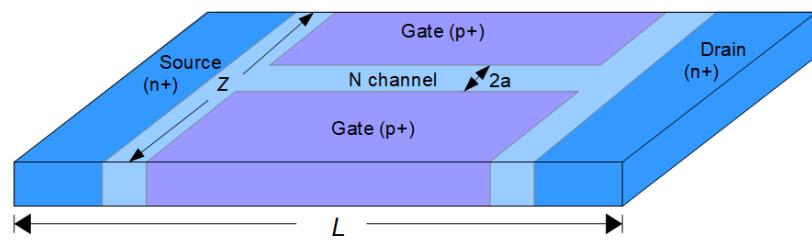
Figure 4.10 Simulated BJT collector characteristics

4.3 N - channel JFET design

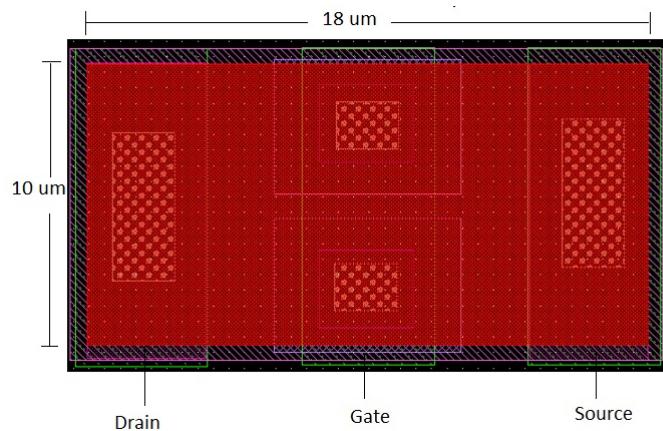
Fig. 4.11 shown top view (a), perspective view (b) and mask layout (c) of a JFET. An *n*-channel device is used since the electron mobility in silicon is roughly three times that of holes. Two ohmic contacts are connected at the ends of the channel, with one acting as the source and the other as the drain. When a positive voltage is applied to the drain with respect to the source, electrons flow from the source to the drain. Two electrically connected *p*⁺ regions on both sides of the channel form the gate. The concentration of channel and gate regions were estimated by Suprem4 simulations. The Suprem4 simulation input file is attached in Appendix II. All implant parameters were determined by the *IME* technology. An uniform doping distribution of the channel and gate is shown in Fig. 4.12 and Fig.4.13, respectively. Here the device width Z is 10 μm and length L is 18 μm . The gate channel width $2a$ is 0.8 μm and depth d is 0.22 μm . A reverse bias applied to the gate-channel *pn* junction widens the junction depletion region, modulating the width of the undepleted channel and hence controlling the current flow between the source and drain.



(a)



(b)



(c)

Figure 4.11 Top view (a), perspective view (b) and layout of JFET structure (c)

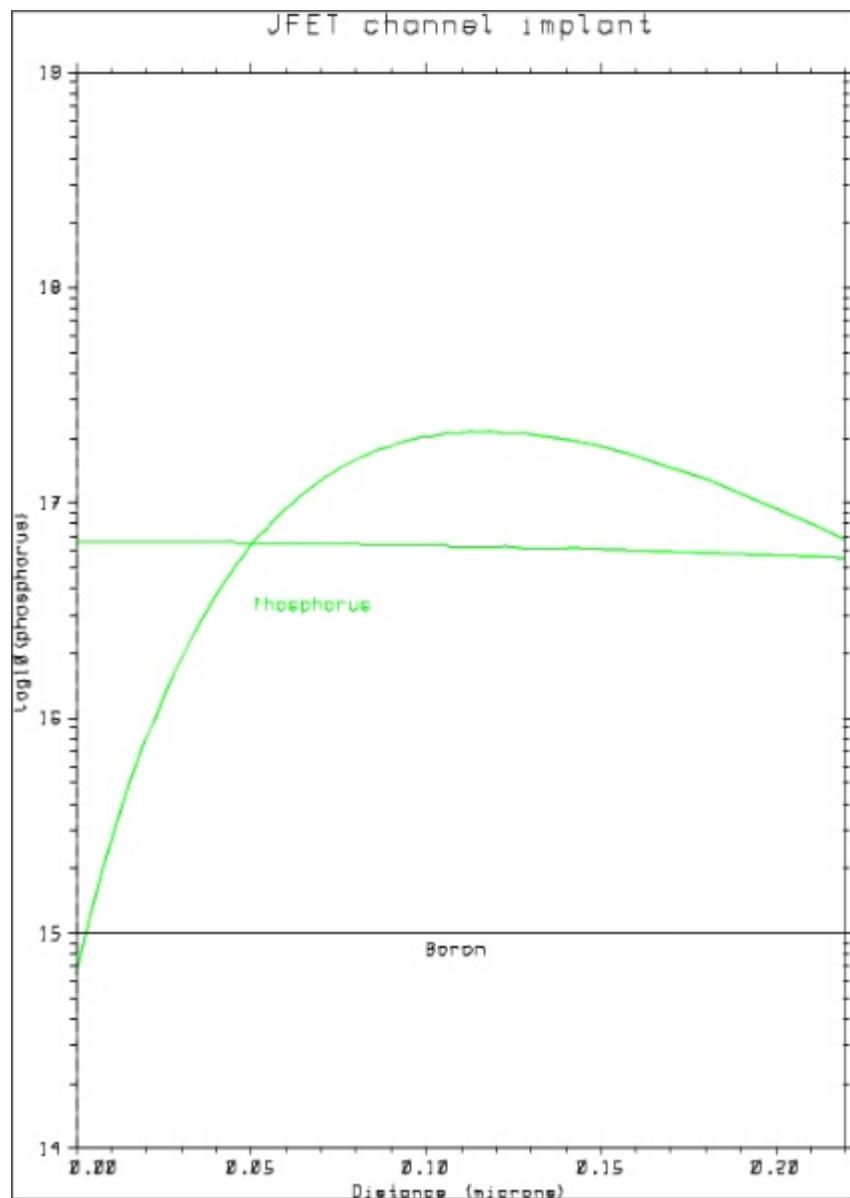


Figure 12 JFET channel implantation

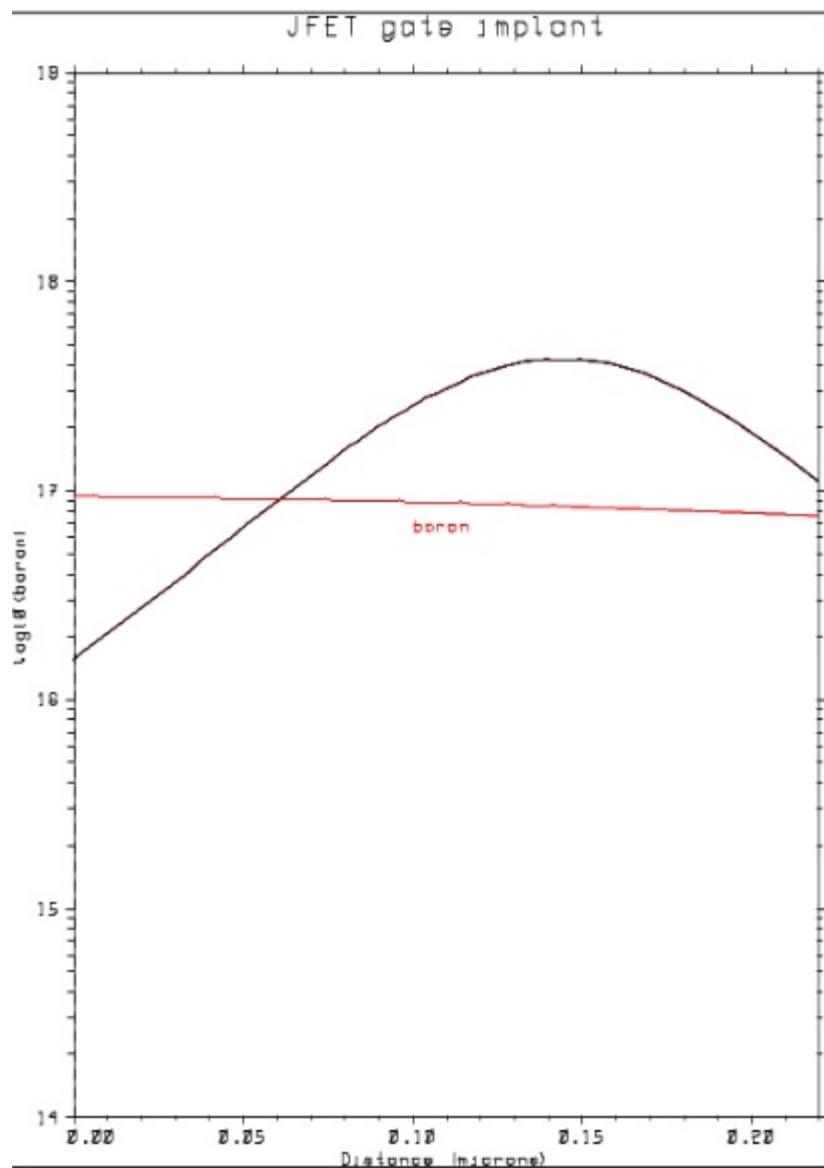


Figure 4.13 JFET gate implantation

SPICE model parameters were listed in Table 4.2 and calculated using the theoretical analysis in the sections 3.1 and 3.3 of Chapter 3. The most significant parameters include the pinch-off voltage V_p and cut-off frequency f_T . The V_p is the gate-channel voltage at which the depletion region extends completely across the channel and current flow between the source and drain is cut off. The cutoff frequency f_T refers to the maximum operating frequency, above which the JFET can no longer amplify an input signal. Here

V_p and f_T were computed using equation 4.3.1 and 4.3.2 [121].

$$V_p = \Phi_0 - \frac{qN_D a^2}{2\epsilon_{si}} \quad 4.3.1$$

$$f_T = \frac{g_m}{2\pi C} \leq \frac{g_m}{(\frac{2\pi\epsilon_{si}ZL}{2a})} = \frac{2\mu_n q N_D a^2}{\pi\epsilon_{si} L^2} \quad 4.3.2$$

Φ_0 is built-in potential voltage, N_D is doping concentration in the n -type channel, ϵ_{si} is silicon permittivity, q is the electron charge, and g_m is transconductance. According to equation 4.3.2, an n -channel JFET is preferred for obtaining good frequency response due to the high mobility of electrons compared to holes. Frequency response is also improved by using a short channel length.

TABLE 4.2
JFET HSPICE MODEL PARAMETERS

Description	Parameters (Units)	Design Value
Transconductance	g_m (A/V)	1.0×10^{-5}
Channel conductance	g_D (A/V)	1.2×10^{-5}
Pinch-off voltage	V_p (V)	-7.8
Cut-off frequency	f_T (GHz)	4.8
Gate junction saturation current	I_s (A)	3.4×10^{-5}
Gate-drain zero-bias capacitance	C_{gd} (fF)	0.3
Source (drain) resistance	R_s (Ω)	30

The pinch-off voltage is typically in the range of -1 V - -5 V for n -type JFETs [122]. Here equation 4.3.1 predicts a value of -7.8 V at the n-type doping level specified by the IME process. The channel width was set at the minimum value of 0.8 μm allowed by the IME layout design rules. The simulated JFET drain current is demonstrated in Fig. 4.14, all current curves are saturated when V_{DS} exceeds 10 V. As gate bias V_{GS} increases, the channel conductance decreases until it becomes zero at the pinch-off voltage, around -7 V.

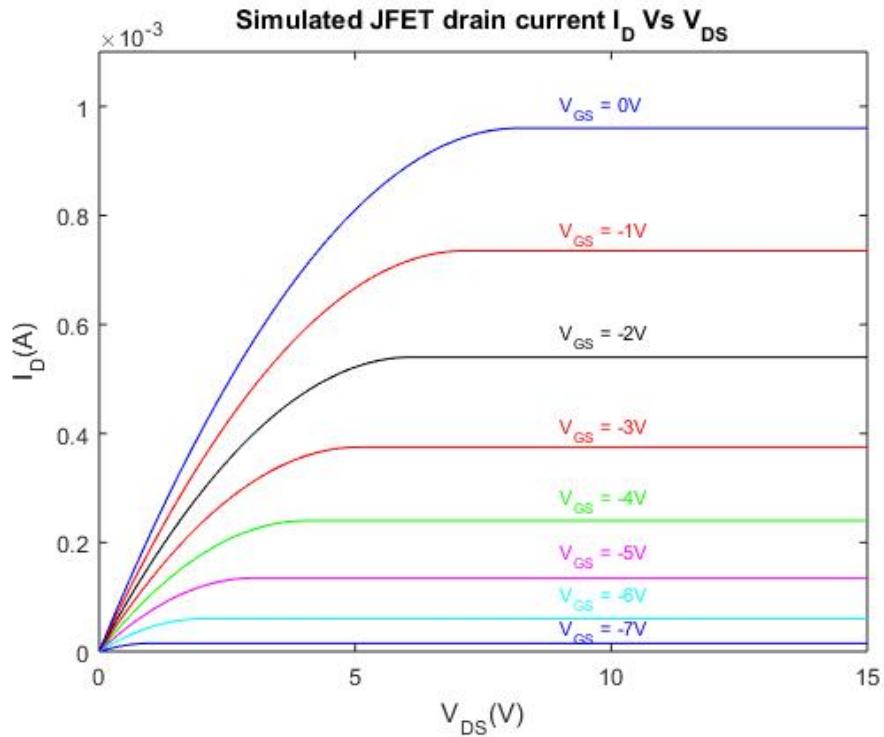


Figure 4.14 Simulated JFET drain characteristics

4.4 Transimpedance amplifier design

Once Spice compact model parameters were estimated for the available transistors, a basic transimpedance amplifier was designed for low - frequency analog applications. An example of a transimpedance amplifier based on BJTs is shown in Fig.4.15 [124]. We use a common-emitter input stage (Q1) and an emitter follower (Q2) to create a low - impedance output and feedback source in the circuit. All the resistors were realized by *n*-type or *p*-type implant in silicon. Photodiode *D1* is modeled by a current source in parallel with a regular diode in SPICE simulation. Results is shown in Fig. 4.16. The input current was given according to the responsivity of $500\mu\text{A}/\text{mW}$ reported by waveguide Ge photodiode in the *IME* process [123].

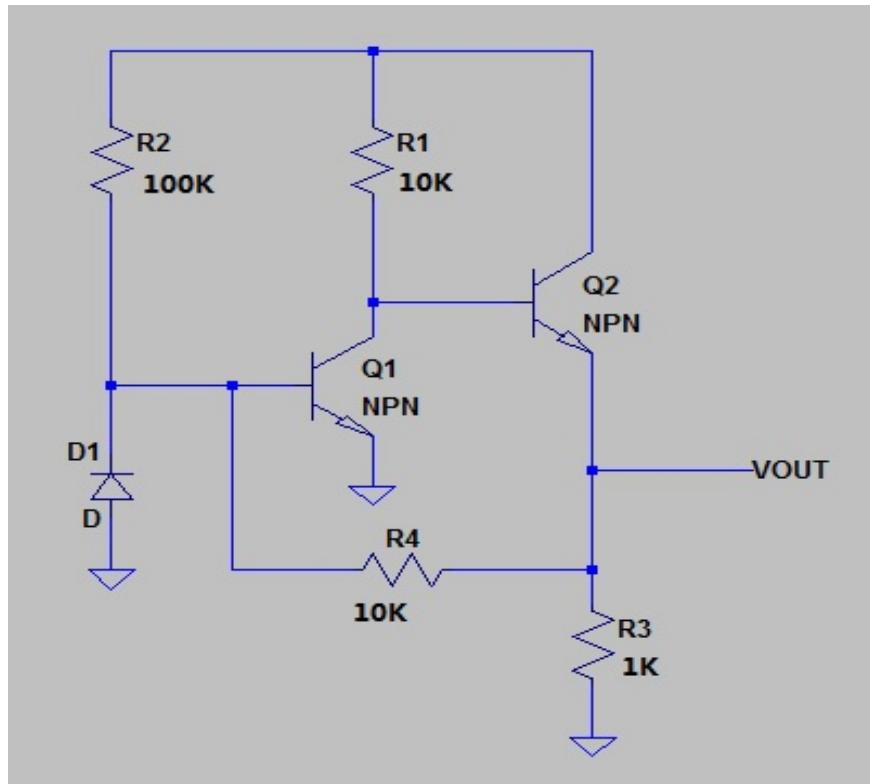


Figure 4.15 The schematic of *n*p*n* BJT transimpedance amplifier

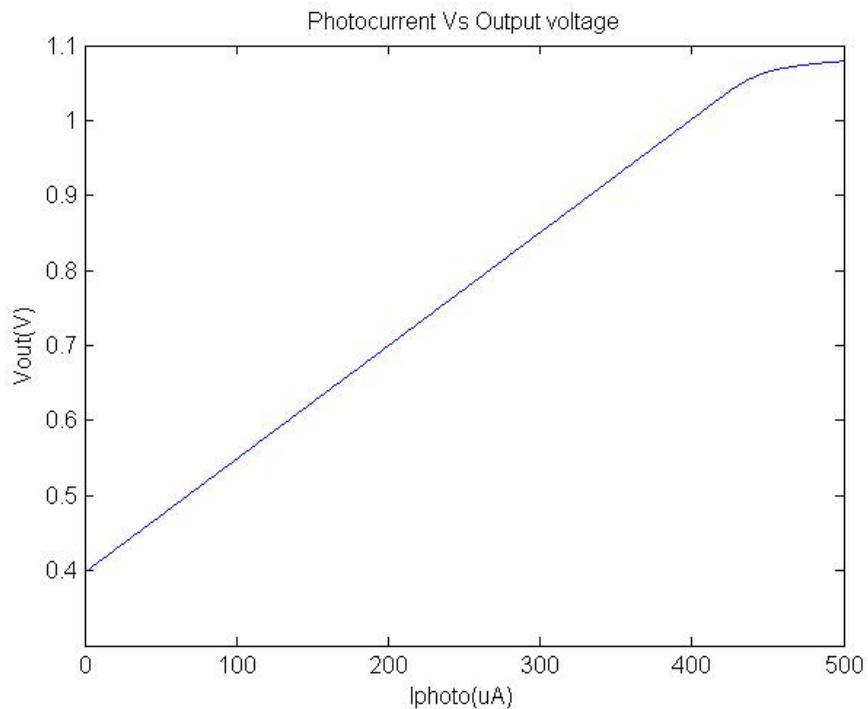


Figure 4.16 Hspice simulation of input photocurrent Vs output voltage

Another example of single JFET common source preamplifier is included in the Fig.4.17 [89]. The resistor R_1 is $10\text{ k}\Omega$, the resistor R_2 is $10\text{ k}\Omega$ and the bias resistor R_3 is $80\text{ k}\Omega$. When V_{DD} supply is 10V, input current bias I_{photo} represents Ge photocurrent in the range of 0-100 μA , a linear output voltage 6.4-10 V was obtained by SPICE simulation in Fig. 4.18.

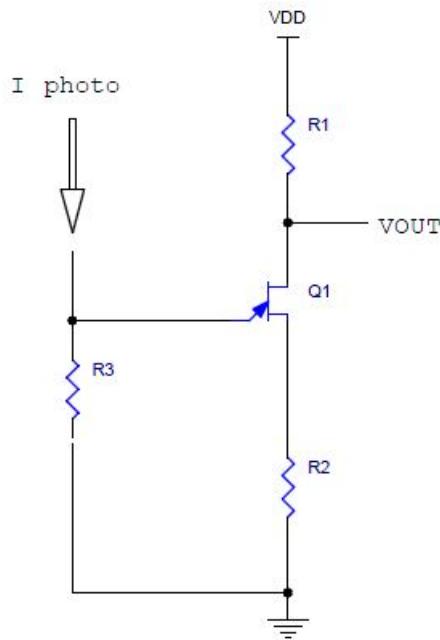


Figure 4.17 JFET common source preamplifiers

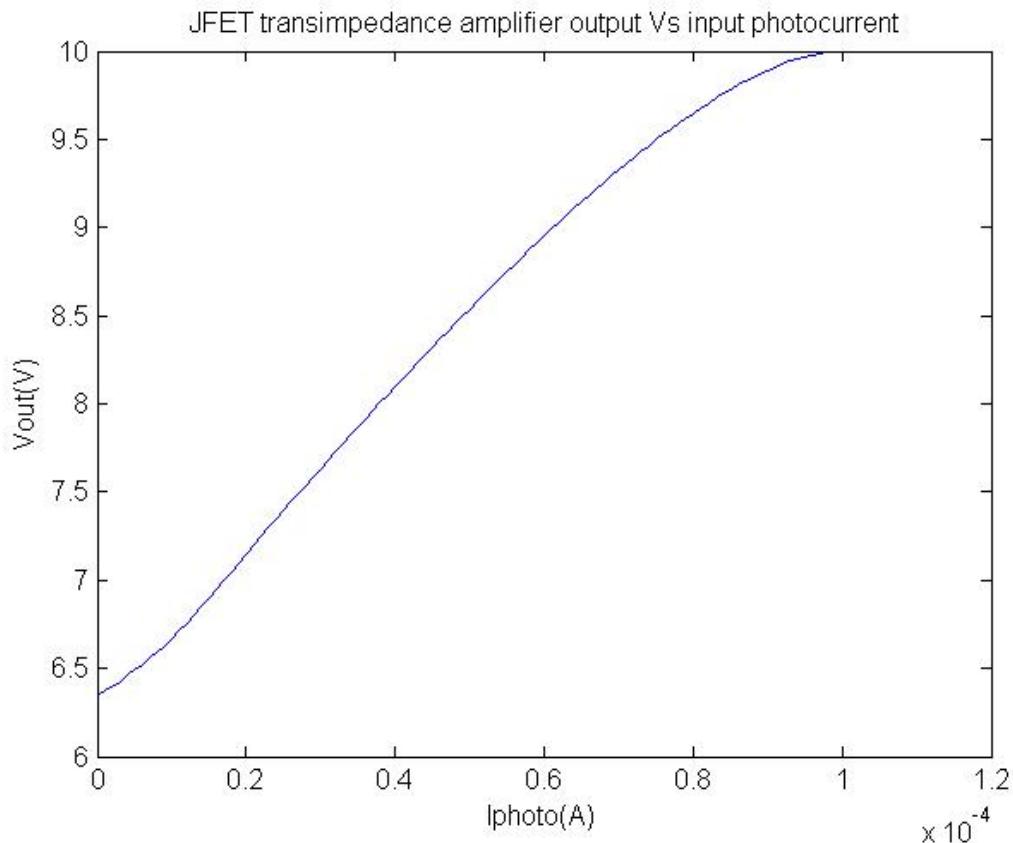


Figure 4.18 Single JFET common-source amplifier simulation results

4.5 Phonics and microelectronic devices integration

In order to demonstrate a full integration of optical components and electronic circuits, we included grating couplers, a strip waveguide, Ge photodiodes, and transimpedance amplifiers in the prototype SOI chip. All optical components are selected from the design library offered by the foundry service. We custom designed the transimpedance amplifiers by using *LBJTs* and *JFETs*. Fig.4.19 shows a block diagram of the integration, using the standard processing parameters supported by A*STAR IME's silicon photonic multi-project wafer service. A waveguide is used to carry and transmit light on the integrated platform. A $500\text{ nm} \times 220\text{ nm}$ strip waveguide was used to connect each optical component. The TE 1550-nm surface grating coupler and Ge PIN photodiode

were selected in the support library for input/output light coupling and detection. A transimpedance amplifier (TIA) is connected at the back end of the Ge photodetector. As we mentioned previously, the IME silicon photonics general-purpose fabrication process does not support the fabrication of MOS devices due to a lack of polysilicon deposition. A MOSFET would also need a high-quality gate oxide. Therefore, we chose to demonstrate the integrated electronic components using *BJTs* and JFETs.

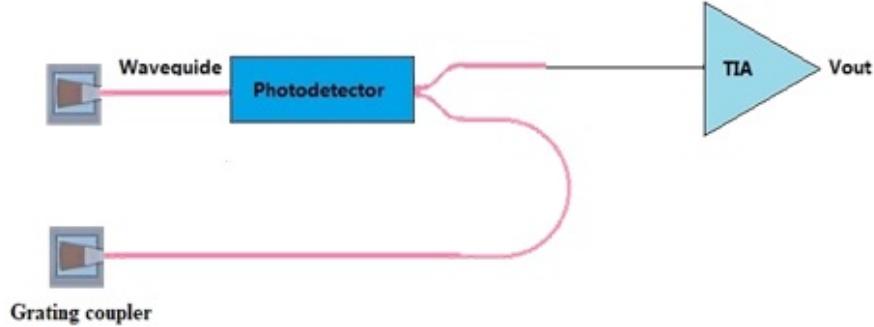


Figure 4.19 Block diagram of a complementary metal oxide semiconductor (CMOS) photonic circuit.

Project layout was completed using the Mentor Graphics Pyxis layout tool which provides SiEPIC project libraries of silicon photonic devices and a flexible editing environment. All layouts were checked for compatibility with the *IME* technology design rules before submission. A complete 6 mm by 1.5 mm test chip was submitted for fabrication at *IME* through *CMC Microsystems*. In order to measure the electrical characteristics of each device and verify original design, various test structures of *LBJTs*, *JFETs* and amplifiers were included in the chip. The fabricated prototype image in Fig.4.20 and Fig.4.21 show test structures, grating couplers, Ge photodiodes and transimpedance amplifier fabricated by the *IME* process. Devices characteristics and performance evaluation will be reported in the following Chapter.

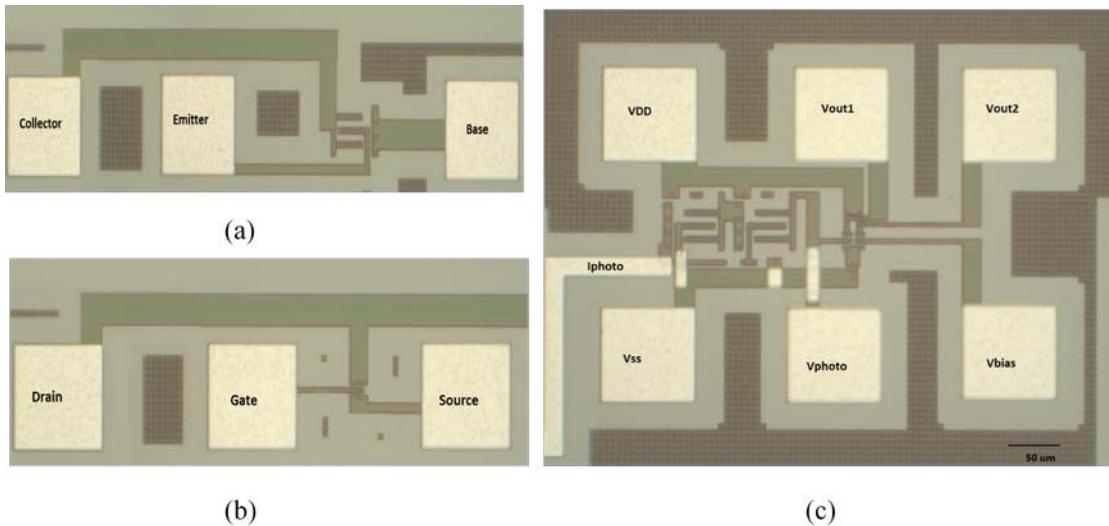


Figure 4.20 A microscope view of fabricated LBJT (a), JFET (b) and BJT/JFET amplifiers (c)

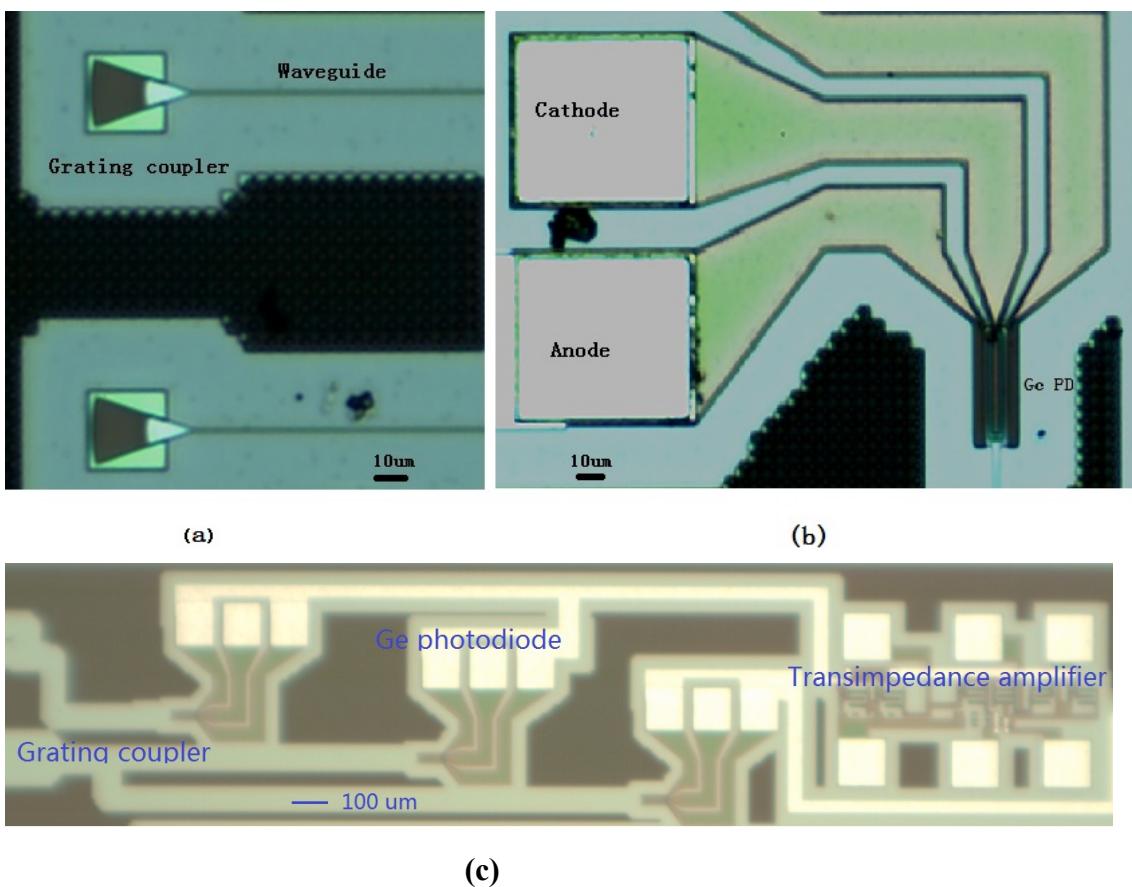


Figure 4.21 A microscope view of grating coupler (a), Ge photodiode (b) and optical and electrical devices integration (c)

Chapter 5: Device Characterization and Results Analysis

This chapter describes experimental characterization of *LBJT*, *JFET* and Ge photodiodes fabricated in the IME technology. Testing results were analyzed by comparison to TCAD simulation and, in the case of the JFET, a revised compact model for circuit simulation was generated.

5.1 Characterization of *LBJT*

In order to evaluate device performance, various test structures were included for characterization on the chip fabricated. Fig.5.1 shows a photograph of a test *LBJT* made in this project. All terminal contact pads are square shape with $100\text{ }\mu\text{m}$ length which ensures good contacts during testing. Current-voltage characteristics of *LBJTs* were measured by using a Wentworth wafer probe station and Hewlett-Packard 4155 Semiconductor Parameter Analyzer. The prober station was enclosed in a light-shielding box during measurements.

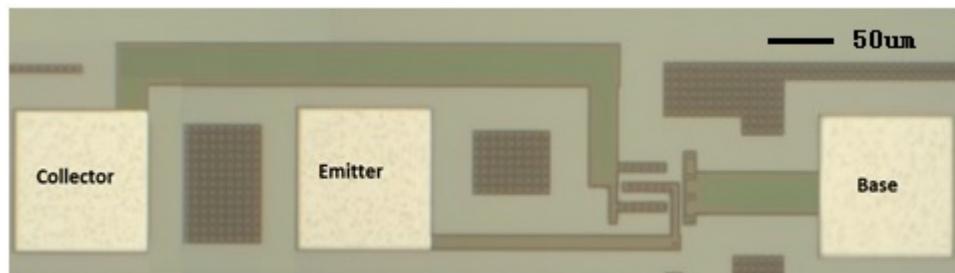


Figure 5.1 Test structure of *LBJT* Fabricated by IME

5.1.1 The Gummel plot

The Gummel plot is typically used to evaluate quality of the emitter-base junction and minority carrier transport across the base. Fig.5.2 shows the *LBJT* Gummel plot. I_C is collector current including electron injection current from emitter to base and generation

current in the collector-base depletion region; I_B is base current which results from hole injection from base to emitter, recombination in the neutral base, and recombination current in the emitter-base depletion region. The collector current is less than the base current which is completely unexpected. Lateral *BJTs* are routinely implemented in CMOS technologies and, although current gains are usually not very high, they are typically greater than ten [89].

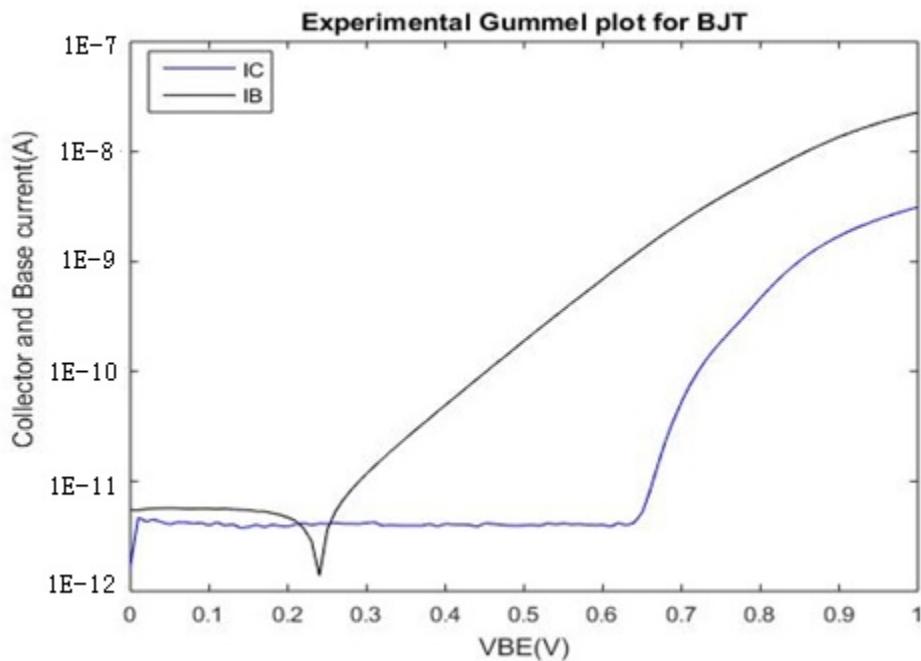


Figure 5.2 Experimental Gummel plot for *LBJT* fabricated in the IME process

5.1.2 *LBJT* result analysis

The Gummel plot in Fig. 5.2 reveals that the most of minority carrier recombine before reaching the collector. A possible explanation for this unexpected result is that the IME process does not passivate the silicon film surface to the degree expected in a normal CMOS process. The in-completed passivating may cause interruption to the periodicity of

crystal lattice, which leads to recombination of electrons and holes in the surface. In the simplest possible model, the recombination rate Us (carriers/second/cm²) at a surface is proportional to the excess minority carrier density n_p (carriers/cm³). The surface recombination rate can be defined by 5.1.1 [89].

$$Us = S(n_p - n_{p0}) \quad 5.1.1$$

Where n_p is the electron concentration in the base and given approximately by equation 5.1.2

$$n_p = (n_i^2 / N_B) \exp(qV_{BE}/kT) \quad 5.1.2$$

N_B is the doping concentration in the base. S is the proportionality constant which has units of cm/s, and hence is called a recombination velocity. In practice, the surface recombination velocity is a simply way to specify the strength of the recombination rate, is given approximately by equation 5.1.3

$$S = I_B / (q n_p A) \quad 5.1.3$$

Where A is the base area [125]. Using the value of I_B measured at $V_{BE}=0.6V$ the calculated surface recombination velocity is about 8,000 cm/s. This is a higher value than would be expected at a properly passivated oxidized silicon surface [126]. A high minority carrier recombination velocity along the base surface could explain why so few electrons reach the collector. Later in this chapter a numerical simulation of the *LBJT* will be presented and used for more accurate confirmation of this explanation for the very low observed current gain.

5.2 Characterization of JFET

Fig.5.3 shows a photograph of a test JFET fabricated by the IME. Drain characteristics and transfer characteristics were obtained on this structure by once again using a Wentworth wafer probe station and Hewlett-Packard 4155 S emiconductor Parameter Analyzer.

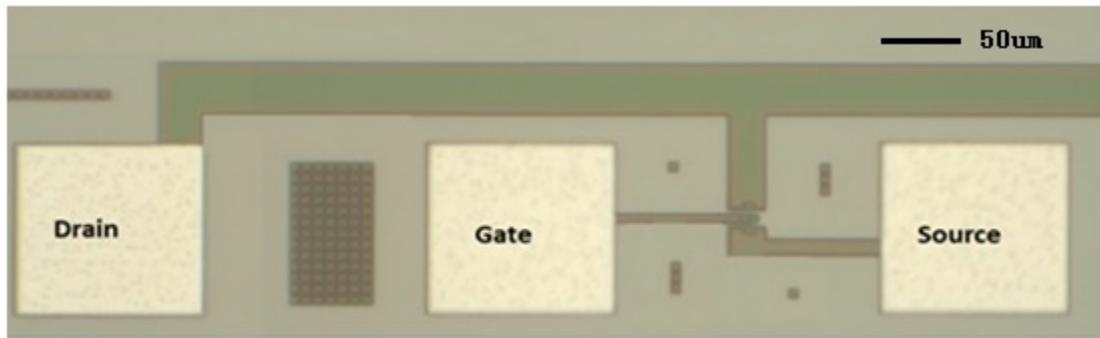


Figure 5.3 Test schematic of JFET Fabricated by the IME

5.2.1 Drain characteristics

The fabricated JFET drain characteristic is shown in Fig. 5.4. Textbook JFET behavior is observed, with I_D nearly constant in the saturation region. The breakdown voltage is observed when the current increases abruptly on each curve. However, the pinch-off voltage is much larger than the design value, at $V_{GS} = -20$ V. This could be due to the variation of the doping concentration in the fabrication process or inaccurate doping profiles estimated by Suprem simulations. The cutoff frequency is 1 GHz as calculated by equation 5.2.1

$$f_T = g_m / (2 \pi C) = g_m / (2\pi \epsilon_s ZL / 2a) \quad 5.2.1$$

Where the transconductance g_m is 1.2×10^{-5} A/V as measured from the slope of Fig. 5.4. Z is the channel depth, L is the channel length and a is the channel width. The JFET noise voltage e_n is essentially the Johnson noise of the channel resistance, can be calculated by equation 5.2.2 [107]

$$e_n = \sqrt{4kT \left(\frac{2}{3g_m} \right)} \quad 5.2.2$$

where the inverse transconductance takes the place of resistance in the Johnson-noise formula. The noise voltage is $0.3 \text{ nV}/\sqrt{\text{Hz}}$ for the JFET fabricated in the IME process.

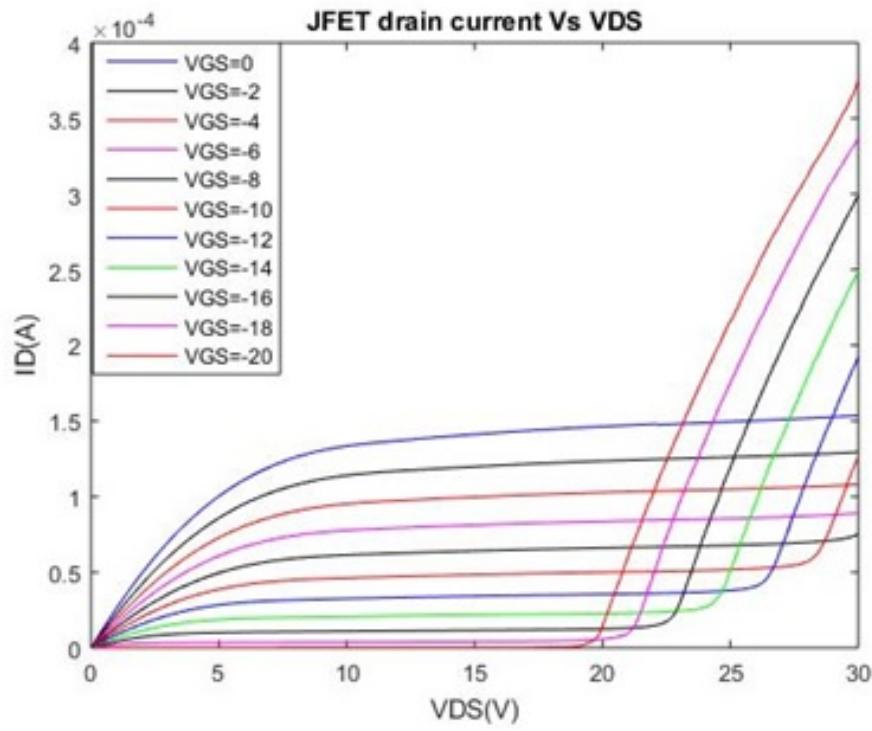


Figure 5.4 Drain characteristics of JFET fabricated in the IME process

5.2.2 Transfer characteristics

The transfer characteristic of the JFET at $V_D = 10V$ was plotted in Fig.5.5. The intersection points on the x-axis and y-axis indicate the pinch-off voltage is - 20 V and the saturation drain current I_{DSS} is 0.14 mA at $V_{GS}=0$ V, respectively. The actual channel doping level is estimated to be $N_D = 1.6 \times 10^{17} \text{ cm}^{-3}$, based on the measured V_p using Equation 5.2.3

$$V_p = \Phi_0 - \frac{qN_D a^2}{2\epsilon_{si}} \quad 5.2.3$$

which is a little higher than our estimated doping level of $7 \times 10^{16} \text{ cm}^{-3}$. This doping variation is acceptable for proving the accuracy of doping profile obtained in Chapter 3.

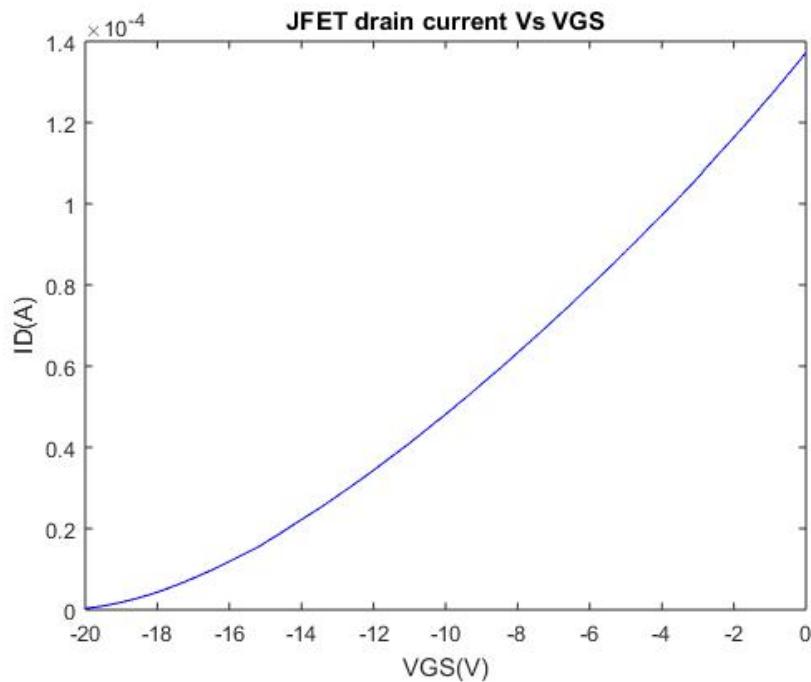


Figure 5.5 Transfer characteristic of JFET fabricated in the IME process ($V_D=10V$)

5.2.3 Revised model parameters

Since there is discrepancy between testing and simulation, the original design parameters need to be improved in order to support circuit design and simulation. Revised *SPICE* model parameters listed in Table 5.1 were extracted from Fig. 5.4 and Fig 5.5. The cutoff frequency is calculated to be 1 GHz according to Equation 5.3, with transconductance g_m being 1.2×10^{-5} A/V. The frequency response limitation is dependent on the dimensions and physical constants of the transistors [127]. To obtain a higher frequency response, we can either decrease the channel length L to reduce the capacitance and increase g_m , or enhance the channel doping level. In this work, we do not have an option to vary the implant dosage parameters since these are pre-defined by the fabrication technology. We also have the design limitation of the layout rules with a fixed minimum feature size.

TABLE 5.1 Revised JFET HSPICE model parameters

Description	Parameters (Units)	Design Value	Revised Value
Transconductance	g_m (A/V)	1.5×10^{-5}	1.2×10^{-5}
Channel conductance	g_D (A/V)	1.2×10^{-5}	2×10^{-5}
Pinch-off voltage	V_p (V)	-7.8	-20
Cut-off frequency	f_T (GHz)	4.8	1
Gate junction saturation current	I_s (A)	3.4×10^{-5}	1.4×10^{-4}
Gate-drain zero-bias capacitance	C_{gd} (fF)	0.3	5.1
Source (drain) resistance	R_s (Ω)	30	400

The fabricated *JFET* behaves well including expected drain characteristics and transfer characteristics, with 1 GHz cut-off frequency. With the revised *SPICE* model parameters in Table 5.1, the preamplifier circuit in Fig.4.17 could be used for monolithic integration with the photonic components provided by the IME technology.

5.3 Characterization of Ge photodiode

5.3.1 Experimental setup

The set-up used for Ge photodiode testing is illustrated in Figure 5.6. Incident light of 1550 nm wavelength is provided by a Phoenix benchtop tunable laser. The laser is driven by a circuit designed for low noise and linear swept performance. The Luna's Phoenix 1400 software includes an intuitive graphical interface to control the laser and collect the data. On the probe station, a customized fiber array is aligned to input and output surface grating couplers as shown in Fig. 5.7. The data obtained was plotted and analyzed by using Luna's Phoenix 1400.

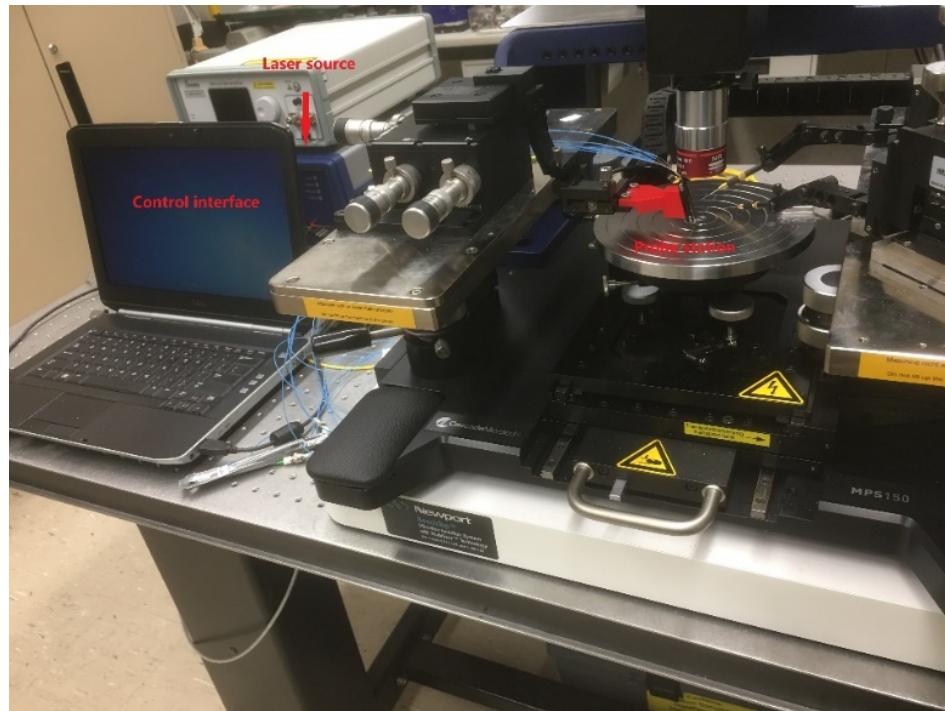


Figure 5.6 Optical and electrical measurement setup

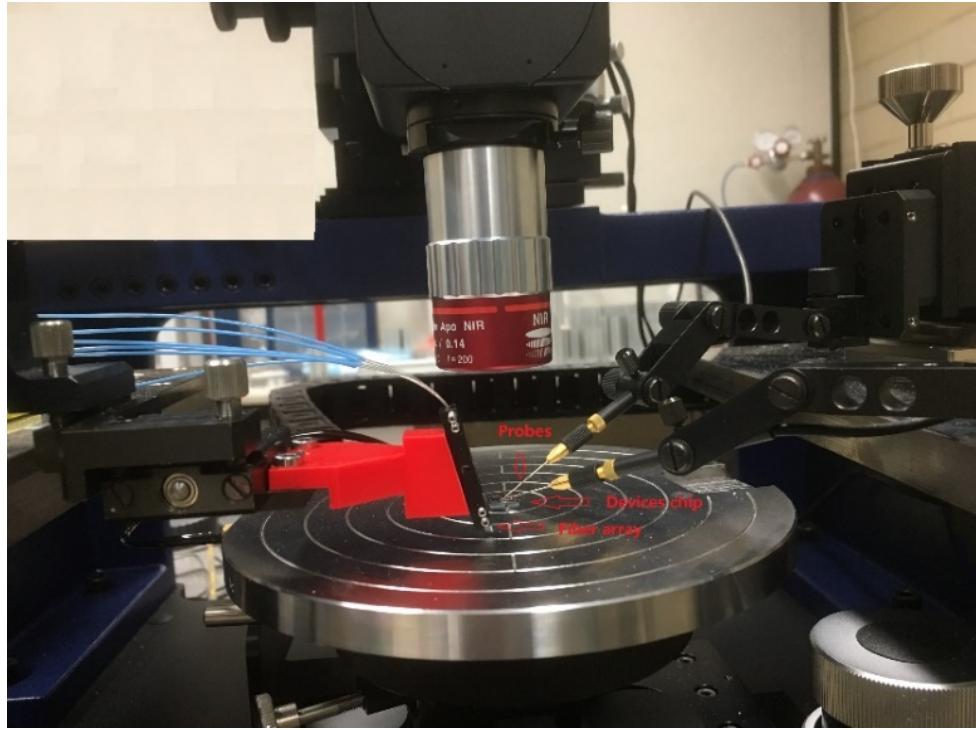


Figure 5.7 A setup for Ge photodiode measurement

5.3.2 I-V curve of Ge photodiode

As mentioned earlier, we extracted a Ge photodiode from design kits library for integration. Fig. 5.8 shows an example of test structure. Beside the Phoenix benchtop tunable laser and Luna's Phoenix 1400 software, a HP 4145 semiconductor parameter analyzer is used to capture the characteristics of Ge photodiode. Firstly, two probes are connected to HP 4145 semiconductor parameter analyzer and also need to make a good contact to the anode/cathode of the Ge diode. Secondly, a fiber array is aligned to the input and output grating couplers in order to estimate the incident light power transmitted to the Ge photodiode.

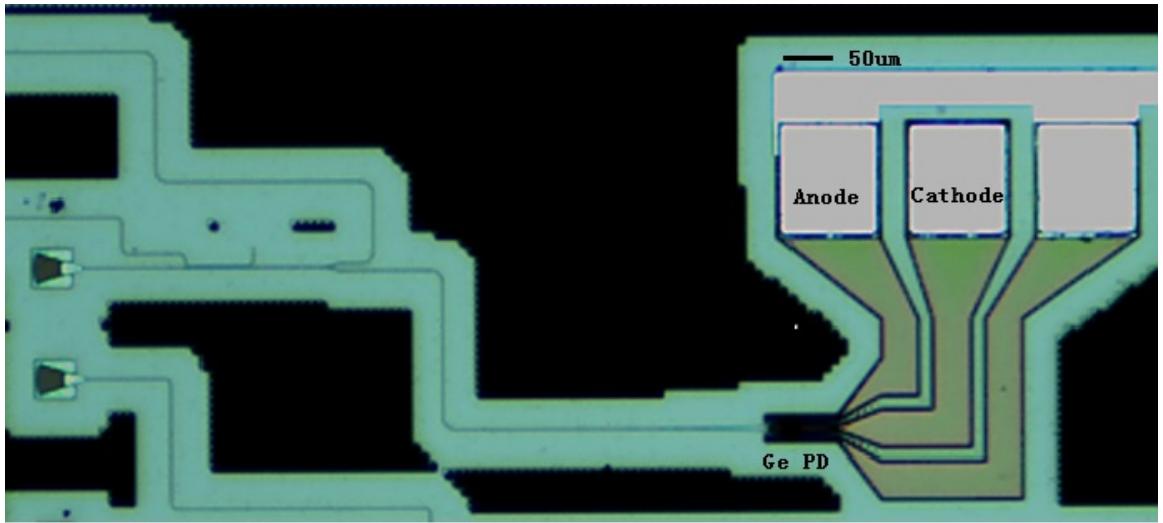


Figure 5.8 Test schematic of Ge photodiode fabricated by IME process

Fig. 5.9 shows rectifying characteristics of the Ge photodiode in both illuminated and dark conditions. It demonstrates photo and dark current ratio in 1 order of magnitude for 1550 nm wavelength incident light power of $\sim 100 \mu\text{W}$. The photo current and dark current is $0.7\mu\text{A}$ and 70nA , separately. The shot noise due to the dark current can be calculated by equation 5.3.1 [108]

$$In = \sqrt{2qI_{dark}BW} \quad 5.3.1$$

where I_{dark} is the dark current, BW is bandwidth. The short noise is only 0.15nA when bandwidth is 10 GHz .

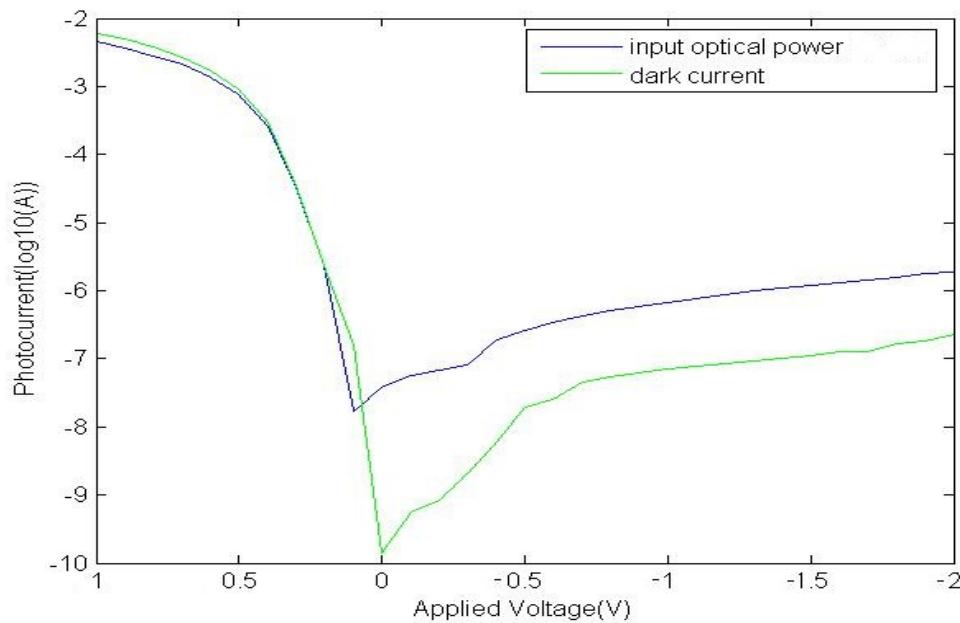


Figure 5.9 Measured current-voltage characteristics of the Ge photodiode under 1550 nm optical power ($100 \mu\text{W}$) and dark condition

5.4 Medici simulation

In TaurusTM Medici simulation, the three fundamental partial differential equations governing semiconductor device operation (Poisson's equation, the Continuity equations and the Boltzmann transport theory) are solved in two dimensions. There are three basic models for carrier recombination: Shockley-Read-Hall (SRH), Auger and direct recombination related to band –to-band or optical recombination. SRH recombination is a trap assisted process which dominants trap level in the middle of the bandgap. It is expressed by following formula in equation 5.4.1

$$R_{SRH} = \frac{pn - n_i^2}{\tau_n(n_i + p) + \tau_p(n_i + n)} \quad 5.4.1$$

The electron and hole lifetime τ_n and τ_p depend on the material and on the fabrication process. Auger recombination is a band-to band process which is the reverse of avalanche generation. It can be modeled by equation 5.4.2

$$R_{Aug} = (C_n n + C_p p) (n p - n_i^2) \quad 5.4.2$$

Where C_n and C_p are the Auger coefficients. At high doping concentrations, Auger recombination is the dominant recombination mechanism. In each device simulation, electrical characteristics are predicted by using corresponding physical models and numerical methods.

5.4.1 LBJT simulations

In *LBJT* simulation, the device structure is defined by dimensions and doping concentration which are derived from device layout and fabrication conditions. The schematic cross section view of *LBJT* in Fig.5.10 was generated by Medici. The top layer is 220 nm active silicon layer with n-type emitter and collector, and p-type base in lateral structure. 2 μ m buried oxide layer and 700 μ m silicon substrate were also included in the simulation profile. The doping concentration is exactly same with proposed value in the *IME* fabrication: $5 \times 10^{19}/\text{cm}^3$ for n-type emitter, 1×10^{17} for p-type base region and 7×10^{16} for n-type collector region. With these parameters, a simulation is performed on the structure defined by MESH, REGION, ELECTRONDE and PROFILE in the Medici statements (See APPENDIX III).

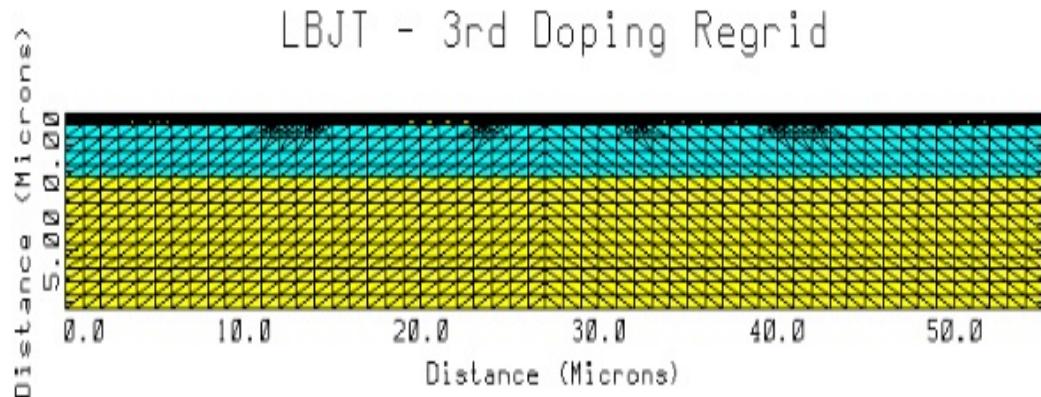


Figure 5.10 LBJT cross-section view with 3rd doping regrid

The physical models considered including SRH, auger recombination, surface recombination mechanisms, and neutral impurity models. The emitter-base space charge region is the largest contributor to SRH recombination. Auger recombination is important at high injection levels typical for BJTs. Surface recombination model also has a significant impact on the device if there is incomplete oxide passivation on the chip surface. In order to obtain an accurate simulation result, the surface recombination velocity, carrier mobility and lifetime are considered in the simulation. With these fundamental semiconductor equations and models discussed above, any specific Medici command can be selected by the Medici statement. Fig.5.11 is the simulated Gurnmel plot.

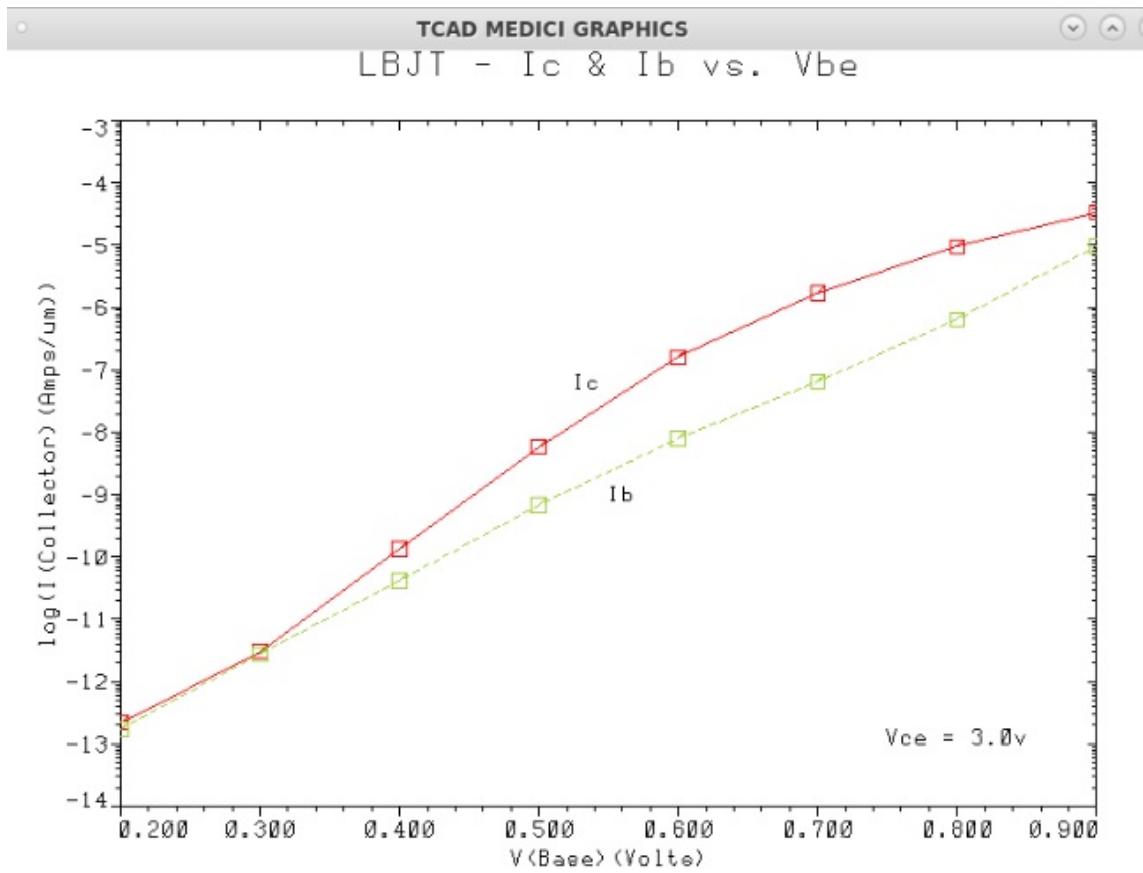


Figure 5.11 Simulated Gummel plot by Medici

Fig.5.12 shows the effect of increasing the surface recombination velocity to 1×10^9 cm/s.

Fig. 5.13 illustrates the DC current gain versus surface recombination velocity, confirming the dependence of current gain on the surface recombination velocity. In LBJT, high velocity surface recombination may be caused by incomplete oxide passivation. It increases the carrier diffusion to the surface which results in the degradation of the current gain by increasing the SRH recombination rate and base recombination current. As the result, higher surface recombination velocity decreases the number of carriers that would be reach at the collector region and lowers the current gain.

LBJT - I_C & I_B vs. V_{BE}

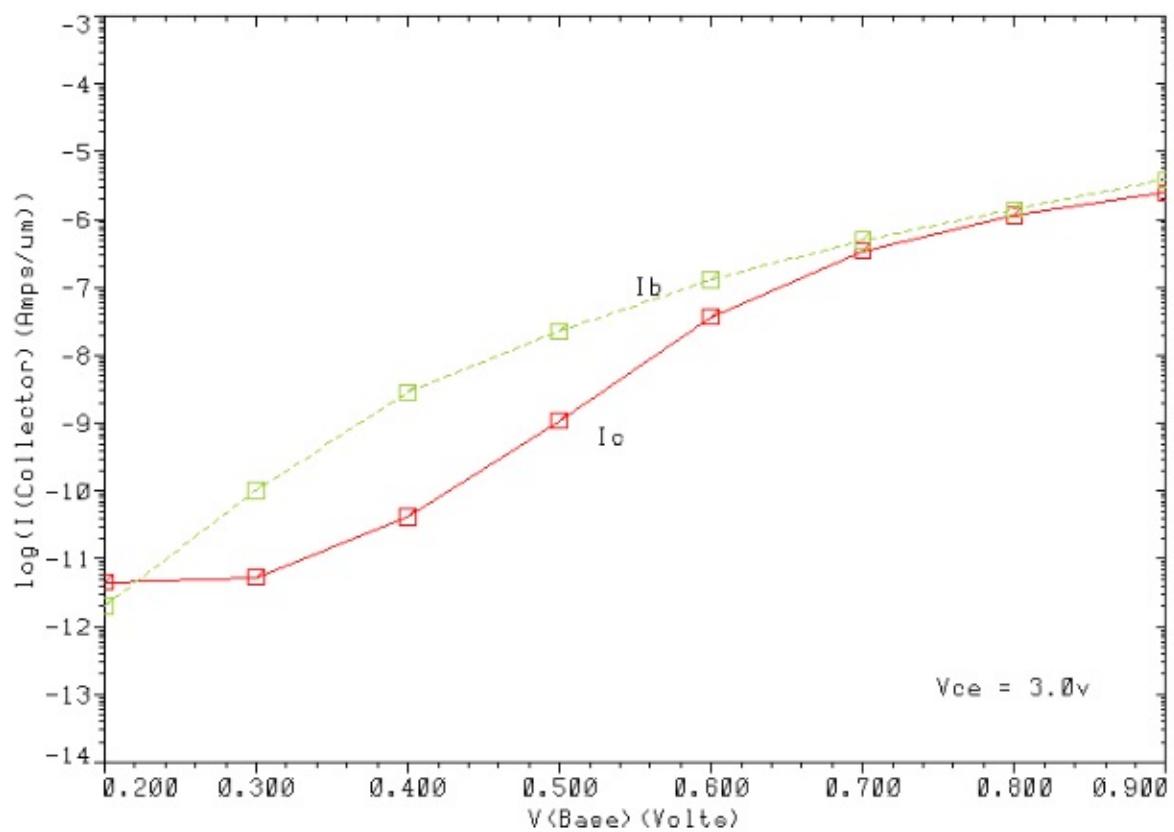


Figure 5.12 Gummel plot with surface recombination

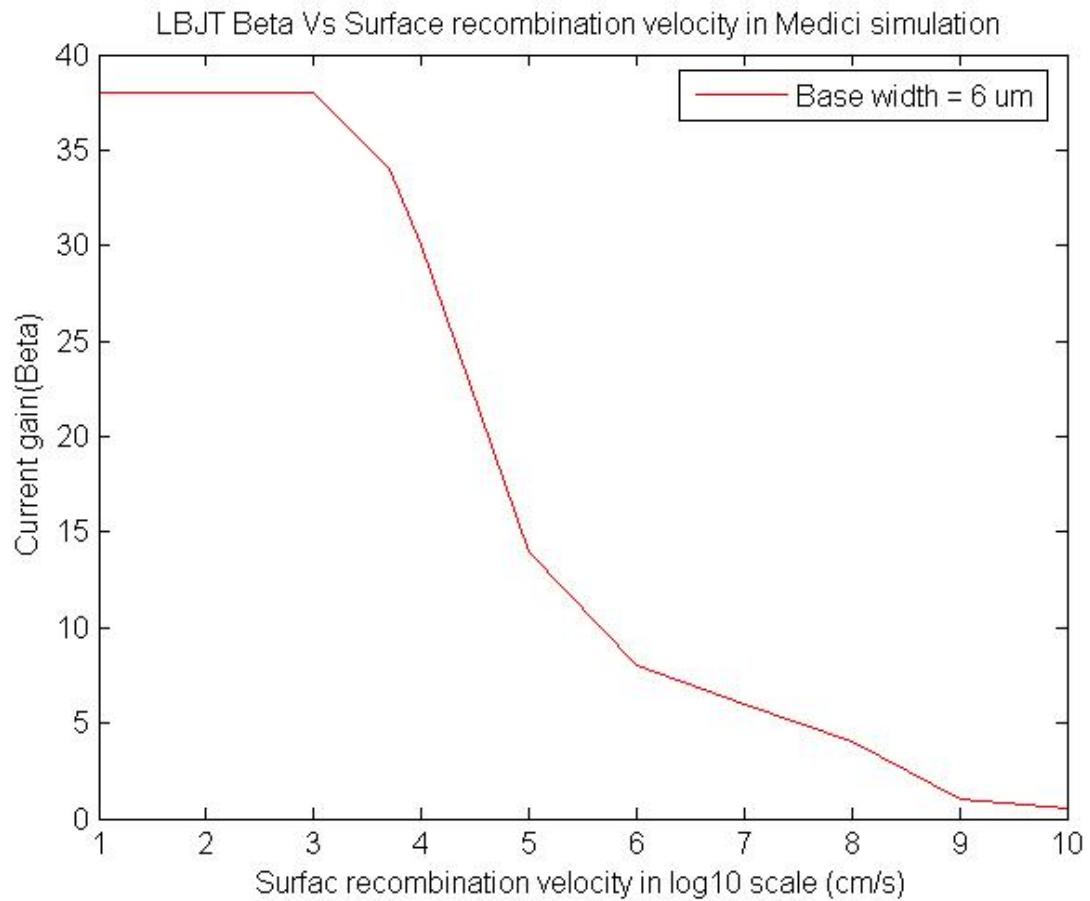


Figure 5.13 The current gain Vs surface recombination velocity in Medici simulation

5.4.2 JFET simulations

The JFET structure simulated in MEDICI is also defined by dimensions and doping concentration which are originally from its layout and fabrication conditions. The top view of the JFET in Fig.5.14 was generated by Medici. It consists of n+-type source/drain contact, n-type channel, and p-type double gate regions. The doping concentration is $1 \times 10^{17}/\text{cm}^3$ boron for gate region and $7 \times 10^{16} / \text{cm}^3$ phosphorus for channel region, respectively. The physical models are considered here including SRH recombination, band-gap narrowing, lifetime and mobility models. The simulation statement is attached in APPENDIX IV.

JFET- Doping Regrid

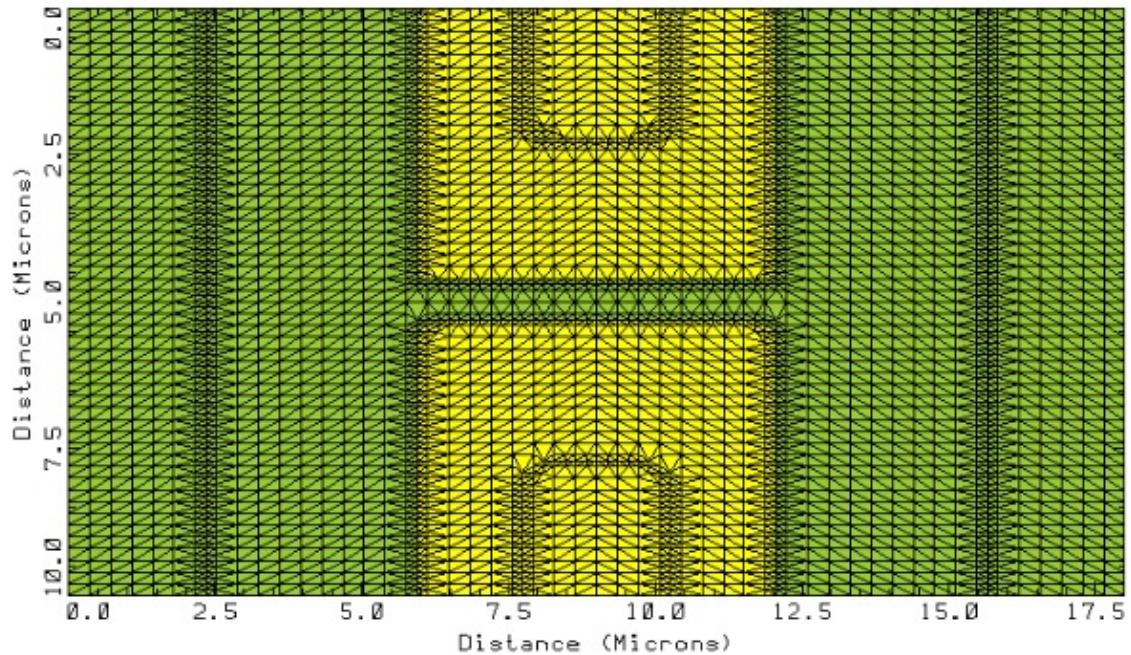


Figure 5.14 Top view of JFET generated by Medici

Since the channel width is a crucial parameter in the JFET design, the simulation have been done by changing channel width in Fig.5.15. It is confirmed that the pinch-off voltage is affected by the channel width variations. Fig.5.16 demonstrates JFET drain characteristics of Medici simulation, revised Hspice simulation and IME fabrication. This provides evidence that the revised model matches Medici simulation and measurement results very well.

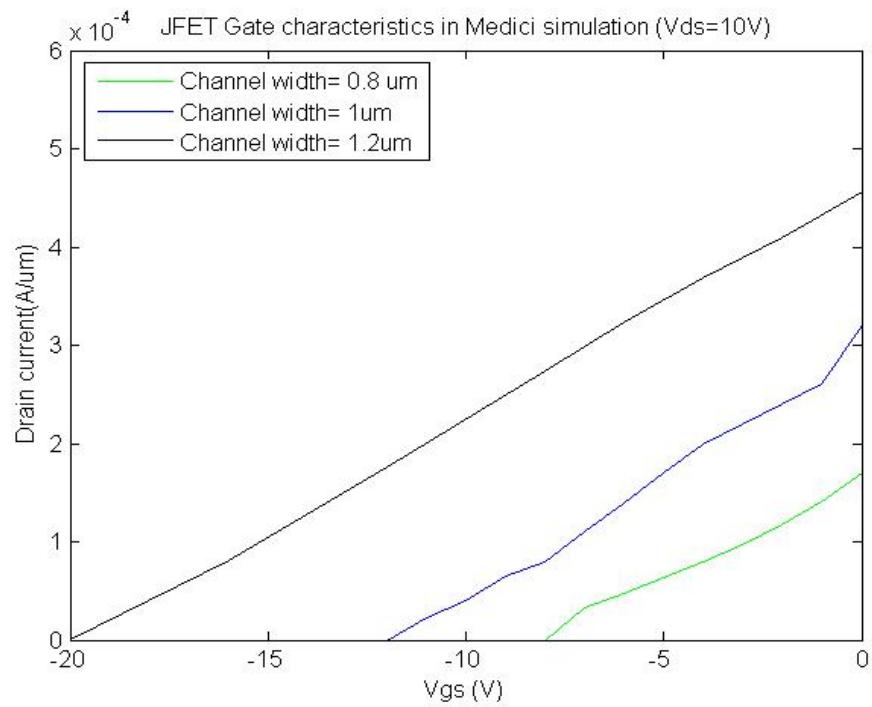


Figure 5.15 JFET gate characteristics in Medici simulation

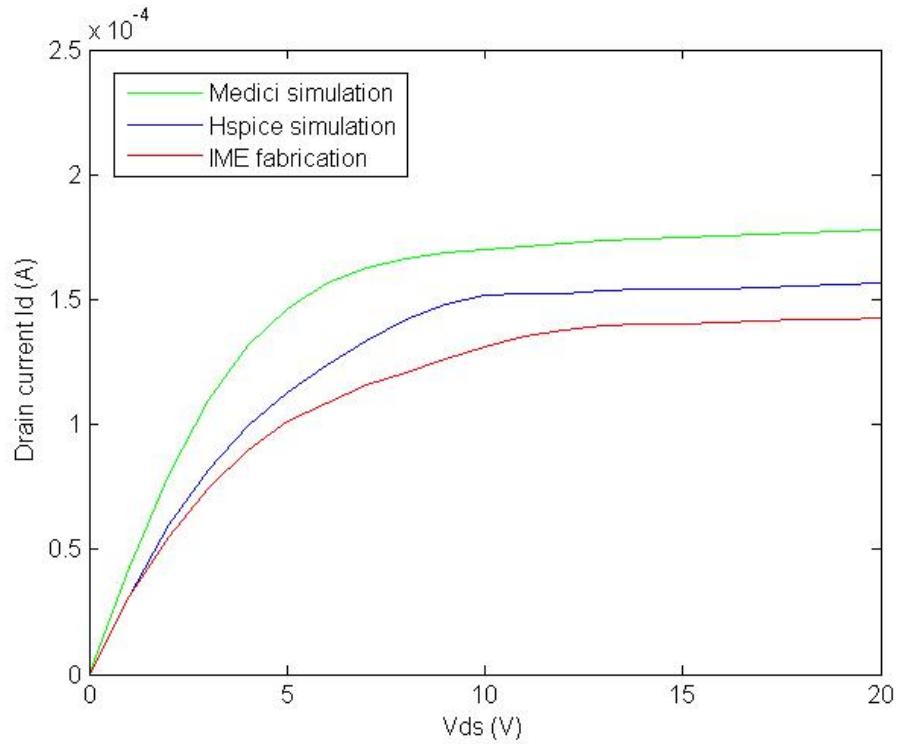


Figure 5.16 Experimental and simulated drain characteristics of JFET ($V_{gs}=0V$)

In conclusion, accurate device models of the *LBJT* and JFET are created in order to predict the gain and current characteristics. The unexpected Gummel plot in Fig. 5.2 is verified by Medici simulation when surface recombination is high. An incomplete oxide passivation could cause high surface recombination velocity in lateral BJTs. For JFET measurement results in Fig. 5.4 and Fig.5.5, a variation in channel width during fabrication easily increases pinch-off voltage which demonstrated by simulation in Fig.5.15. Comparing with revised SPICE simulation and Medici simulation results, the drain characteristic of JFET fabricated by IME shows consistence in Fig. 5.16. This confirmed that JFET could be used for further integration in the following paragraph.

5.5 An application in silicon photonic wire biosensor

The common source JFET transimpedance amplifier in Fig.4.17 can be resigned with the revised SPICE model parameters listed in Table 5.1. The resistor R_1 , R_2 and R_3 is $25\text{ k}\Omega$, $25\text{ k}\Omega$ and $200\text{ k}\Omega$, respectively. The supply voltage V_{DD} is 20 V. Fig.5.17 shows linear output voltage with photocurrent input of $0\text{-}100\text{ }\mu\text{A}$.

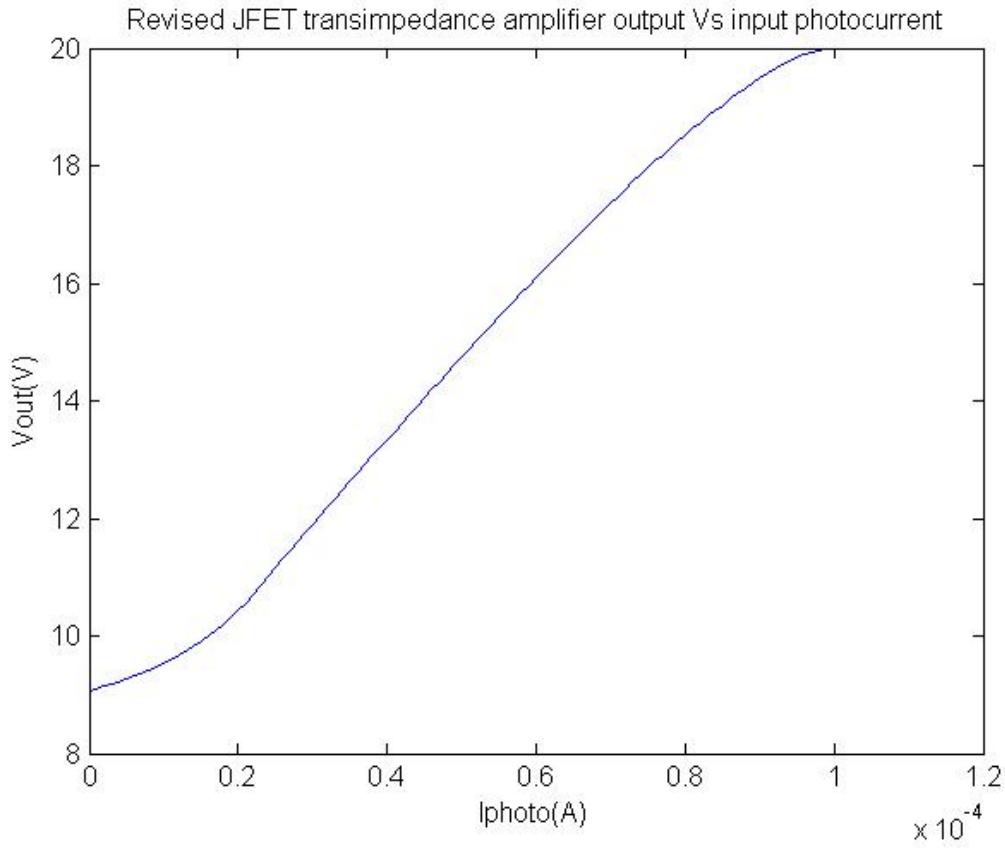


Figure 5.17 JFET transimpedance amplifier simulated by revised SPICE parameters

One useful application is integrated readout circuit for silicon photonic wire biosensor reported by NRC research group [128, 129]. The sensor fabricated within $0.26 \mu\text{m} \times 0.45 \mu\text{m}$ wire waveguide on the SOI platform with $0.26 \mu\text{m}$ silicon layer and a $2 \mu\text{m}$ buried oxide. Since there is similar dimension of the strip waveguide and SOI platform in the IME process, the NRC biosensor, Ge photodiode and JFET transimpedance amplifier can be monolithic implanted on a single SOI chip illustrated in Fig. 5.18. The NRC biosensor is an interferometer which consists of two identical spiral or folded structure used for verifying DNA sequence. The incoming light enters interferometer through a tapered waveguide, then splits equally into the two arms of the interferometer. One arm of the

interferometer is coated with a monolayer of a chosen DNA strand split down the middle, exposed to a solution that maybe contain the “complementary” split DNA strand, the type of DNA will bind to the chosen stand. The effective refractive index of the waveguide will be changes slightly if the DNA was matched. The light power level at the output of the interferometer will be changed as well. The light power was detected by Ge photodetector, then sent to transimpedance amplifier to buffer the signal for further processing.

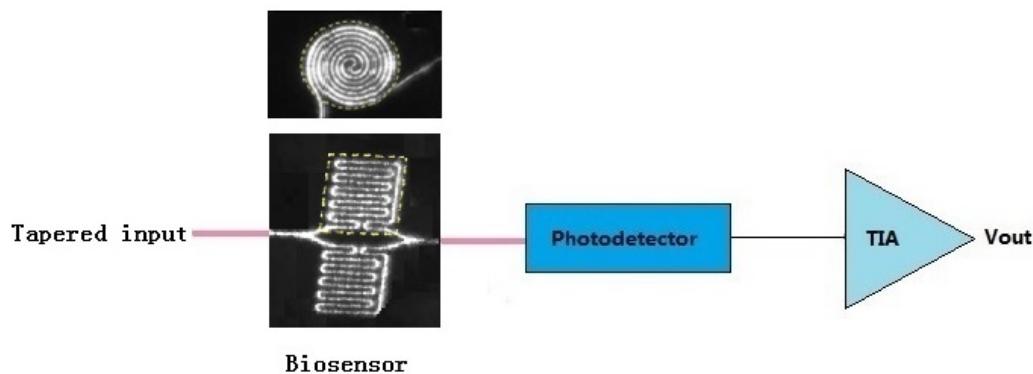


Figure 5. 18 An integration of Ge photodiode, transimpedance amplifier and biosensor

Chapter 6: CMOS and Schottky waveguide photodetector Integration

This chapter presents an extension work from my M. A. Sc thesis which centered on the first demonstration of Schottky photodiode detectors for sub-bandgap light integrated with waveguides defined by the Local Oxidation of Silicon (LOCOS) technique [130, 131]. It was confirmed that the LOCOS waveguide structure is ideally suited for this integration, providing low diode reverse leakage due to the absence of sharp topography where the metal overlaps the waveguide. Diodes were fabricated using Pt, Pd and Ni barriers deposited by thermal evaporation. Diodes electrical characteristics and photoresponse in the 1310 – 1550 nm wavelength range were measured. The devices studied had ridge waveguides with rib widths of approximately 5 μm , which was typical of early SOI integrated optics but coarse compared to modern “photonic wire” waveguides with submicron widths. This work reported measurement results of Pt/Pd diode and optical loss simulation in waveguide Schottky diode photodetectors as a function of metal thickness and wavelength. It will be shown that the waveguide Schottky diodes can be easily integrated with Carleton’s fully-depleted SOI CMOS electronics technology. To demonstrate the potential of this integration, a CMOS transimpedance amplifier is designed, fabricated and tested in this technology. All the devices reported here and in the earlier M. A. Sc research were fabricated at Carleton.

6.1 Comparison of Pd, Pt and Ni Schottky diodes

This section reports Schottky diode photodetector integration with waveguides fabricated by a self-aligned LOCOS process which offers a nearly planar integration platform and smooth edge isolation, giving low dark current and leakage effects. In particular, we

report on and compare the characteristics of LOCOS waveguide integrated palladium (Pd), Nickel (Ni) and Platinum (Pt) Schottky photodetectors fabricated in my M.A.Sc research work.

The waveguide structure examined is shown in cross-section in Fig. 6.1. The buried oxide thickness is 0.4 μm and initial silicon film thickness 3.4 μm . The Si film was doped by implantation to give an active phosphorus concentration of approximately 10^{16}cm^{-3} . Following a conventional LOCOS process flow [132], a 20 nm stress-relief pad oxide was grown on the Si film and overlaid with a 50 nm Si_3N_4 film. The Si_3N_4 film was then patterned by plasma etching to define 5 mm long, 5 μm wide waveguides, and the samples oxidized to give a rib height of 0.5 μm . The Si_3N_4 and pad oxide layers were then removed but the thick oxide formed on either side of the rib was left in place to provide cladding and electrical isolation. The thin Schottky barrier layers were deposited by e-beam evaporation and patterned by lift-off lithography. A Schottky metal thickness of just 10 nm was used because a thin metallic layer (10—20 nm) can be used to enhance the internal photoemission through multiple hot carrier reflections off the internal metal-semiconductor interface [133]. Metal silicide is a thin film formed by solid-state reaction between the metal and silicon and annealed at a temperature range of 300 - 600°C, which provides a rectification junction with a built-in electric field on the metal/Si contact. In addition, a 200 nm thick Al layer was deposited adjacent to the optically active rib to form an ohmic contact to the Si film. At the end of processing the samples were cleaved to form facets for optical coupling.

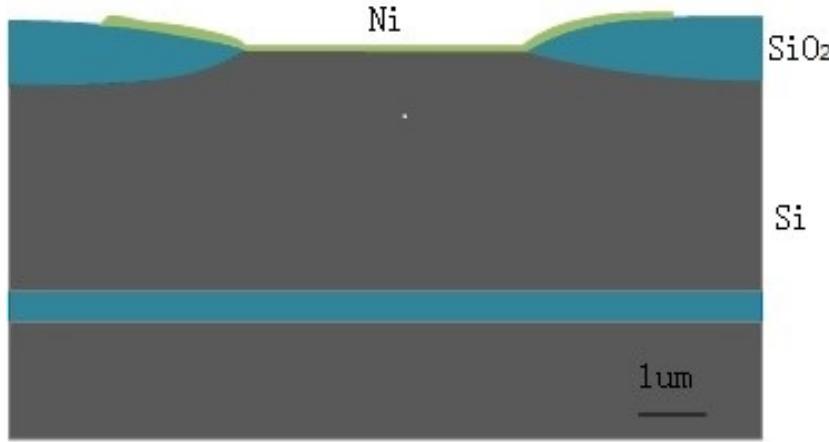


Figure6.1 Cross - section of Ni Schottky diode on LOCOS waveguide

Table 6.1 summarizes the results of electrical and optical testing using a tapered fiber end-fire coupled to the waveguide. Schottky barrier heights were estimated by fitting a tangent to the current – voltage plot and then calculated to be 0.73 eV, 0.79 eV and 0.85 eV for the Ni/nSi, Pd/nSi, and Pt/nSi interface, respectively [131]. Dark current is the reverse leakage current density at 1 V reverse bias. Optical responsivity was measured at wavelengths of 1310 nm and 1550 nm.

TABLE 6.1 Comparison of Schottky diodes

	Barrier heights (eV)	Dark current (A/cm ²)	Responsivities (mA/W) (TM1310nm)	Responsivities (mA/W) (TM1550nm)
Ni/nSi	0.73	1×10^{-6}	4.7	1.8
Pd/nSi	0.79	2×10^{-8}	0.33	0.15
Pt/nSi	0.85	1×10^{-8}	0.12	0.03

The Ni/nSi diode had the best optical performance: the responsivity is 10 times stronger than that of the Pd/nSi and Pt/nSi Schottky diode. Regardless of contribution from the lowest barrier heights of Ni/nSi, a good adhesion between Ni and silicon also provides a lower resistivity of contact. However, the low barrier height of these devices gives high dark current. The high barrier height of the PtSi/nSi diode gives low dark current but optical response is poor, particularly at 1550 nm. The Pd/nSi devices gave a better trade-off between the dark current and photoresponse.

The Ni/nSi photodetector was evaluated under a transverse electric (TE) polarization as well as TM polarization. The optical response with TE polarization is approximately 60% of the value obtained from the TM polarization, because the TM and TE mode have different field distribution inside and outside of the waveguiding core. The TM mode has more evanescent field extending into the top layer of the waveguide ridge [134], exciting more surface plasmons at the metal/nSi interface. Therefore, the Schottky metal film above the ridge absorbs more light power and generates a larger photo current with the TM polarization. This interpretation was verified by FIMMWAVE simulation [135] in the following section 6.2.

6.2 Optical loss simulation

In a waveguide Schottky diode photocurrent is generated through the interaction of the guided EM wave with the overlying Schottky metal. It is therefore very important to determine the optical attenuation as the wave propagates. Here the optical loss due to the metallic layer absorption and transmission was estimated theoretically using the FIMMWAVE (Version 6.0.1) Film Mode Matching (FMM) solver. This is a semi-analytical, fully vectorial waveguide solver based on the film mode matching method

[136]. The FMM solver is generally suited for waveguides which have large parts of uniform refractive index. It can accurately model lossy, metallic, leaky, or radiating structures. Since the loss in a 1 mm LOCOS SOI waveguide without a metallic overlayer is known to be quite low [137], the primary contributor to loss estimated in the simulations here must be the presence of the metal layer. The refractive indices of metals are complex, where the imaginary part describes the optical absorption. The optical properties of Ni and Pd are given in Table 6.2 [138].

TABLE 6.2 Optical properties of Ni and Pd at 1310 nm and 1550 nm wavelength

	Ni		Pd	
	1310 nm	1550 nm	1310 nm	1550 nm
<i>n</i>	3.21	3.44	2.85	3.16
<i>k</i>	6.02	6.74	7.20	8.21
α (μm^{-1})	57.72	54.61	69.00	66.53
P/P_0 (%)	56	58	50	51

Here n and k are the real and imaginary parts of the refractive index, and α is the absorption coefficient. The relation between α and k is $\alpha=4\pi k / \lambda$. Power loss can be calculated based on Bouguer's law $P = P_0 e^{-\alpha x}$ where P is the total penetration power, P_0 is the original input power and x is the thickness of absorbing metal layer perpendicular to light propagation [139]. The waveguide structure was specified in the mixed-geometry waveguide (MGW) interface in which the slanted ridge sidewalls typically formed by the LOCOS process can be properly approximated. In initial simulation the waveguide rib was set to 5 μm in width and 0.5 μm in height, topped with a Schottky metal layer with thickness of 10 – 100 nm. According to the simulations, this rib structure supports only

the fundamental transverse electric (TE) and transverse magnetic (TM) modes. The electric field profiles of the fundamental TE mode is shown in Fig.6.2. Most of the electric field is confined within the silicon SOI waveguide core. Here we use the approximate measured dimensions of the fabricated LOCOS SOI waveguides as the reference for the cross-sections of the waveguide in all simulations. As illustrated in Fig. 6.2, the LOCOS waveguides have slanted sidewalls as a result of the local oxidation process. Most of the electric field is confined within the silicon SOI waveguide core. Here we approximate the waveguide dimensions using the average measured dimensions of the in-house fabricated LOCOS SOI waveguides for all simulations.

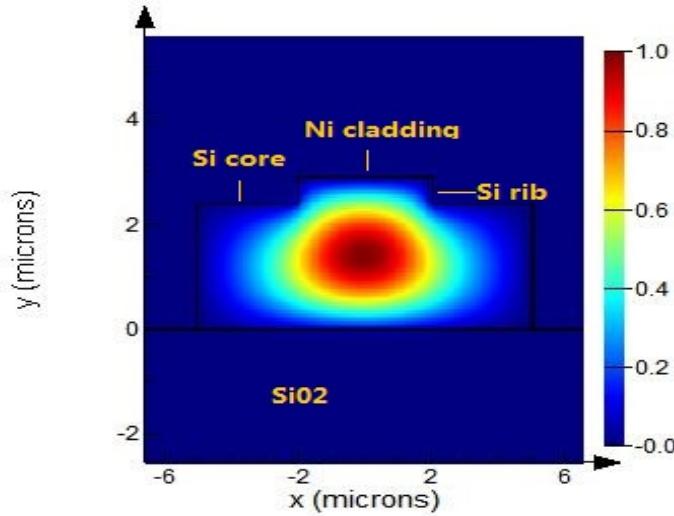
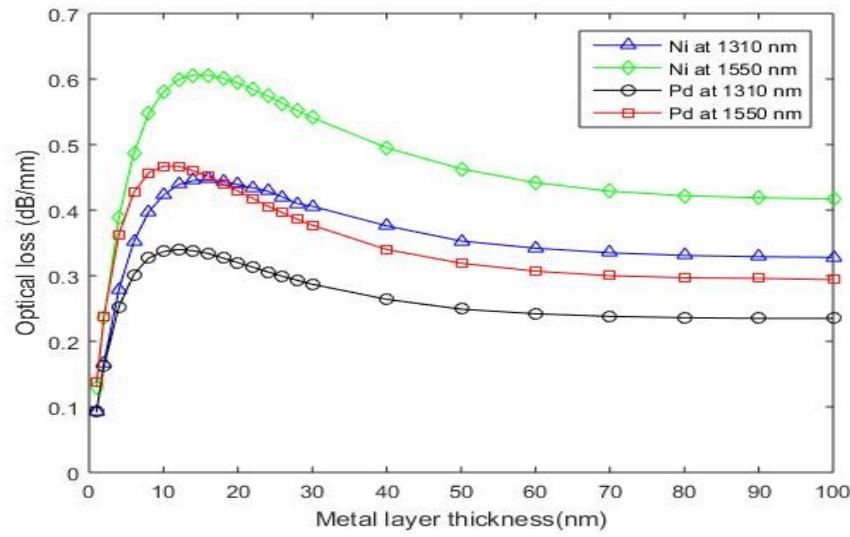


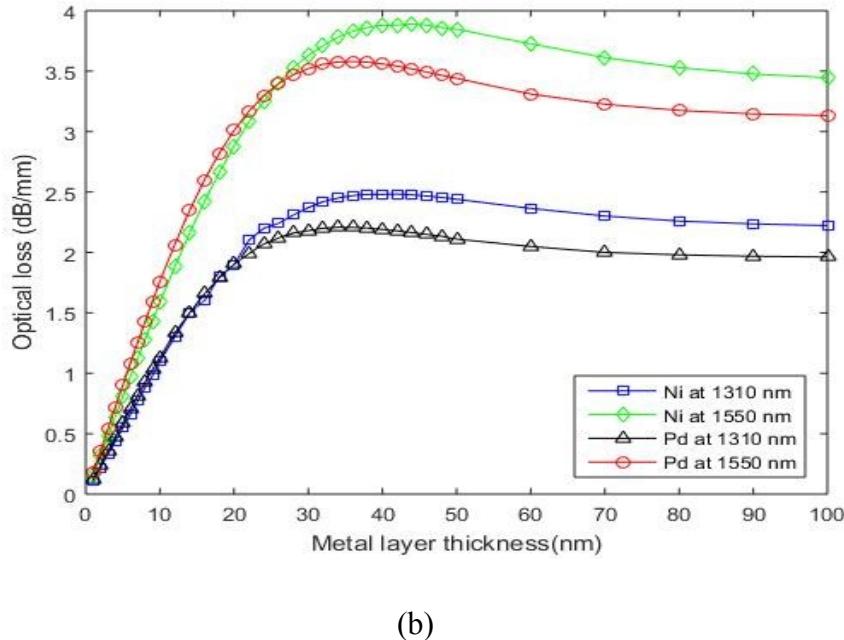
Figure 6.2 *Ex* profile of the fundamental TE mode in a rib LOCOS SOI waveguide. The target rib width w_r is 5 μm and rib height h_r is 0.5 μm , the top of the rib is a 30 nm Ni metal layer.

The optical loss of the SOI waveguide as a function of the Schottky metal thickness is shown in Fig.6.3 (a) and (b), respectively. According to the plot in Fig.6.3 (a), the loss for the TE polarized mode in waveguides with either Ni or Pd layer is below 1 dB/mm at 1550 nm and 1310 nm. At a critical thickness of the metal cladding, the optical loss and

attenuation both reach a maximum value. For the Pd films, the maximum attenuation occurs around the thickness of 10 nm, while the maximum attenuation occurs at 15 nm for Ni films. For the TM polarized mode shown in Fig.6.3 (b), the optical loss in waveguides with Ni and Pd layers is much larger than that in the TE mode, with a critical thickness of metals being around 35 nm. As the thickness of metal film increases, the optical loss reaches a plateau value for thicknesses greater than about 50 nm for both TE and TM polarizations. Any thicker metal layer no longer contributes to the optical loss, confirming that light absorption occurs mainly in the vicinity of the interface between the metal layer and the silicon waveguide.



(a)



(b)

Figure 6.3 Simulated optical loss of the SOI waveguide ($w_r=5 \mu\text{m}$, $h_r=0.5 \mu\text{m}$, $H=3.4 \mu\text{m}$) under a TE mode (a) and a TM mode (b) as a function of the Schottky metal thickness for various free-space wavelengths. Two metals are used on top of the rib waveguide: Pd and Ni.

Fig. 6.4 plots the wavelength dependence of the optical loss for Ni- and Pd-clad SOI waveguides. It is shown that the optical loss increases as wavelength increases. This is mainly caused by the increases of the extinction coefficient [139]. According to Table 6.2, both Ni and Pd have wavelength-dependent refractive indices. At 1550 nm, the refractive indices of both metals are larger than that at 1310 nm. The waveguide optical loss therefore is expected to be higher when wavelength increases. Moreover, the attenuation coefficient of the TM mode is one order of magnitude higher than that of the TE mode [140]. The loss variation can be explained by the characteristics of the mode profiles of TE and TM. The TE mode propagates with the electric field mainly parallel to the metal-dielectric interface of the rib waveguide; while the TM mode electric field is

perpendicular to the interface of the rib waveguide, causing more light absorption and scattering at the metal/silicon interface.

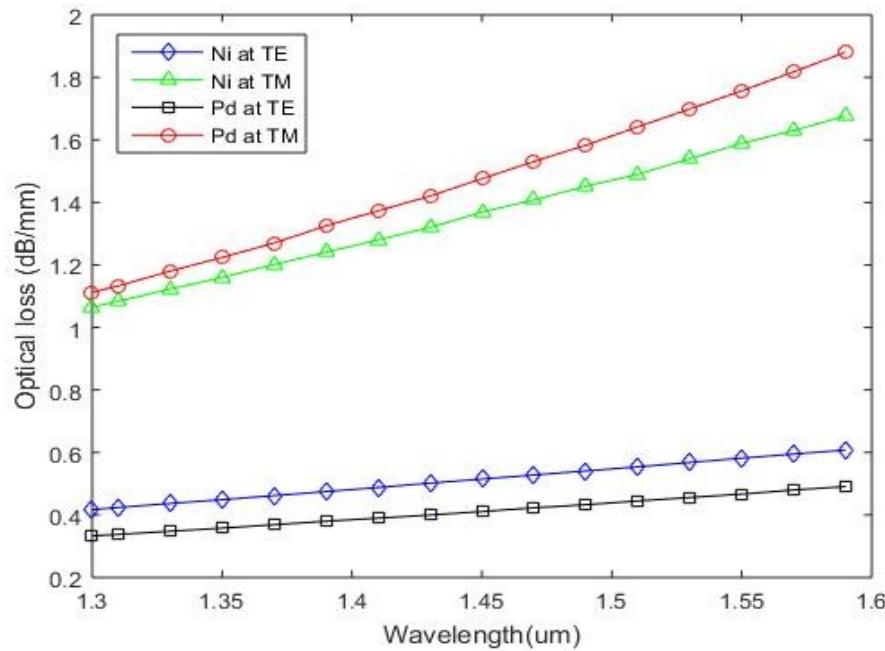


Figure 6.4 Simulated optical loss of the SOI waveguide ($w_r=5\text{ }\mu\text{m}$, $h_r=0.5\text{ }\mu\text{m}$, $H=3.4\text{ }\mu\text{m}$) versus free space wavelength for TE and TM polarization, with a 10 nm metal cladding layer (Ni or Pd).

Losses are significantly higher for the TM mode than for the TE mode, as expected. Simulated loss increases roughly linearly with increasing metal thickness until a plateau is reached at a thickness of about 10 nm (TE) or 20 nm (TM). The plateau loss is approximately 1 dB /mm for TE and 2 dB /mm for TM. Loss increases slightly with increasing wavelength in the range between 1310 and 1550 nm.

In summary, three type of Schottky diodes - Ni/nSi, Pd/nSi, and Pt/nSi - were integrated with LOCOS-defined waveguides and characterized optically and electrically in addition to my M.A.Sc work. The Pd/nSi diode is the most promising candidate for further investigation due to its relatively low dark current combined with good optical

characteristics. This work has shown that, with an appropriate choice of barrier metal, Schottky photodiodes integrated with LOCOS-defined waveguides can provide simple yet effective sub-bandgap photodetectors for SOI photonics.

6.3 CMOS transimpedance amplifier design

In order to demonstrate in-house fabricated CMOS circuits can be used for photonic systems, we have designed and fabricated a CMOS transimpedance amplifier in the Carleton MicroFab using a technology completely compatible with LOCOS waveguide formation. The amplifier was fabricated along with a set of student projects for undergraduate course ELEC 4609. This CMOS technology was developed primarily to provide rapid fabrication for the undergraduate course projects including differential amplifiers, source follower buffers, current mirrors and logic gates. The MOSFET SPICE model parameters were determined and refined by measuring test device experimental characteristics over several process runs. The fabrication is started with a SOITEC wafer in 100 mm diameter, 280 nm top silicon and 400 nm silicon dioxide. The main process includes oxidation, ion implantation, diffusion, thin film deposition, photolithography and etching. The CMOS fabrication detail will be given in the process flow at the end of this chapter.

The schematic diagram for the transimpedance amplifier is shown in Fig.6.5 [141]. The transimpedance front-end circuit consists of M_1 and M_3 followed by a decision stage which consists of M_2 and M_4 . Feedback circuitry consists of a saturated NMOS M_5 and diode connected PMOS M_4 . The photodiode is modeled by a junction capacitor, a photocurrent and a regular diode. Hspice was used to establish CMOS large signal model and to evaluate the performance of the circuit. We were aiming to realize functionality

and integration rather than higher speed and lower noise because integration concept is the main goal of this design.

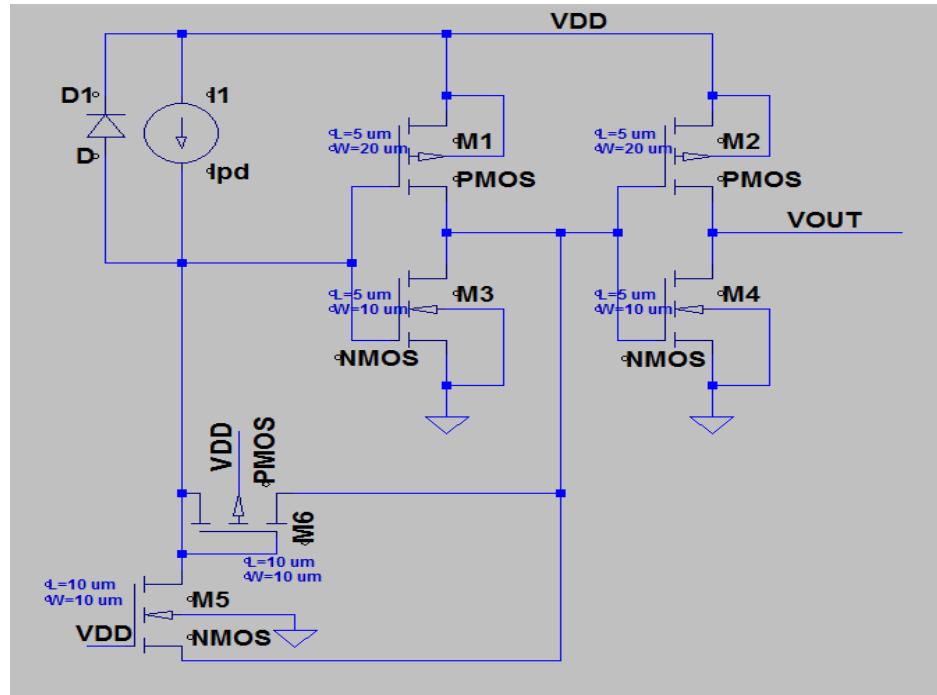


Figure6. 5 The schematic of CMOS transimpedance amplifier

The CMOS amplifier simulation is shown in Fig. 6.6. The x-axis is input photocurrent in μA , and y-axis is output voltage in Volts. The output voltage is 2.3 V as input photocurrent is around 10 μA . The project layout was done by L-edit 7.0 illustrated in Fig.6.7. The red layer represents polysilicon, the green layer is device wells, and the blue layer indicates metal connections and contact pads. Beside the MOSFET pattern, there is a substrate diode on the middle left which can be used to provide internal photocurrent for the circuitry. Fig.6.8 is experimental result of the amplifier fabricated. The injected photocurrent range is 0 – 15 μA which approximates results from waveguide Schottky diode testing but this assumes a reasonable optical input power. It demonstrated that there

is small discrepancy between simulated results in Fig. 6.6 and measured results in Fig. 6.8.

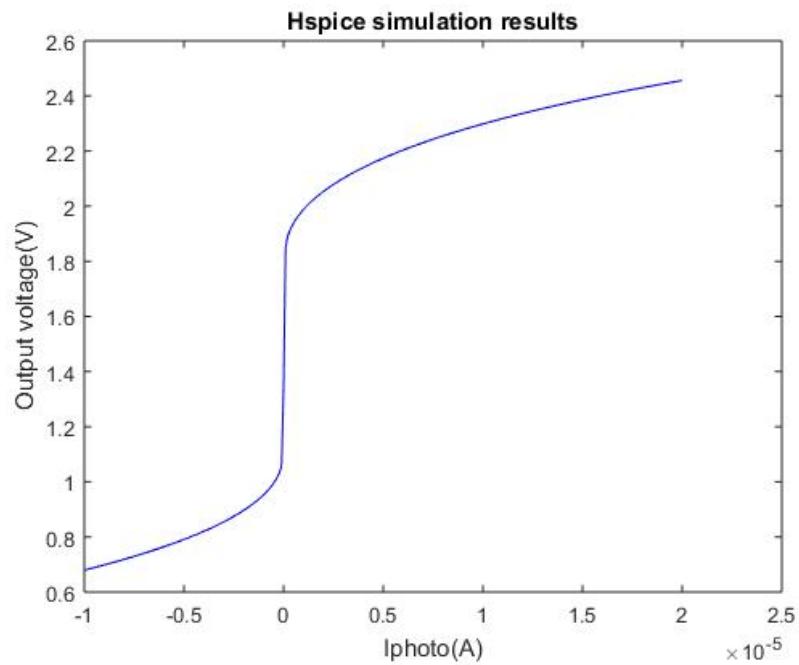


Figure 6.6 Output voltage versus input photo current

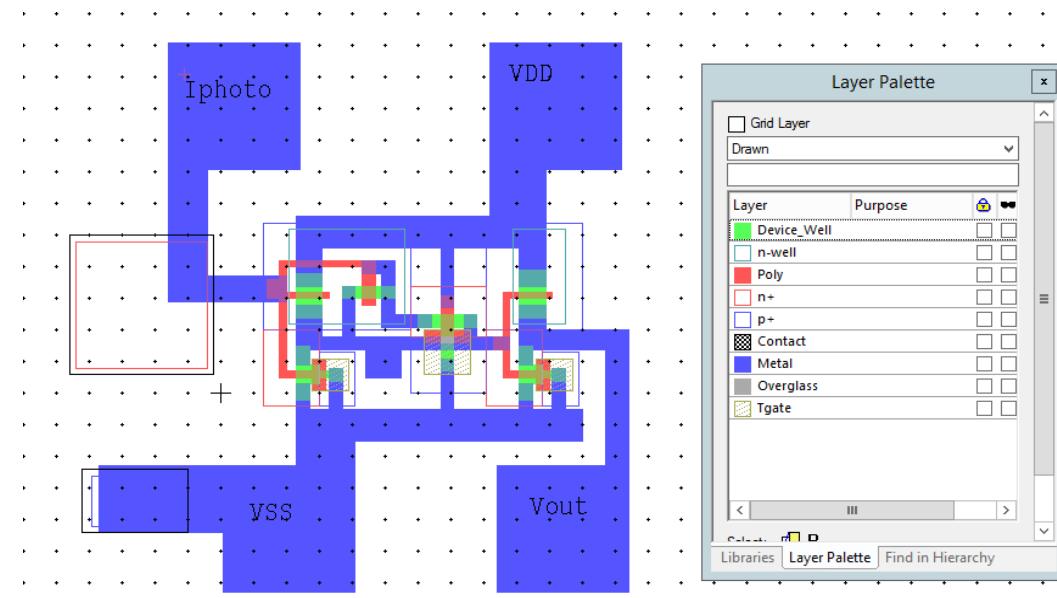


Figure 6.7 Layout of CMOS transimpedance amplifier

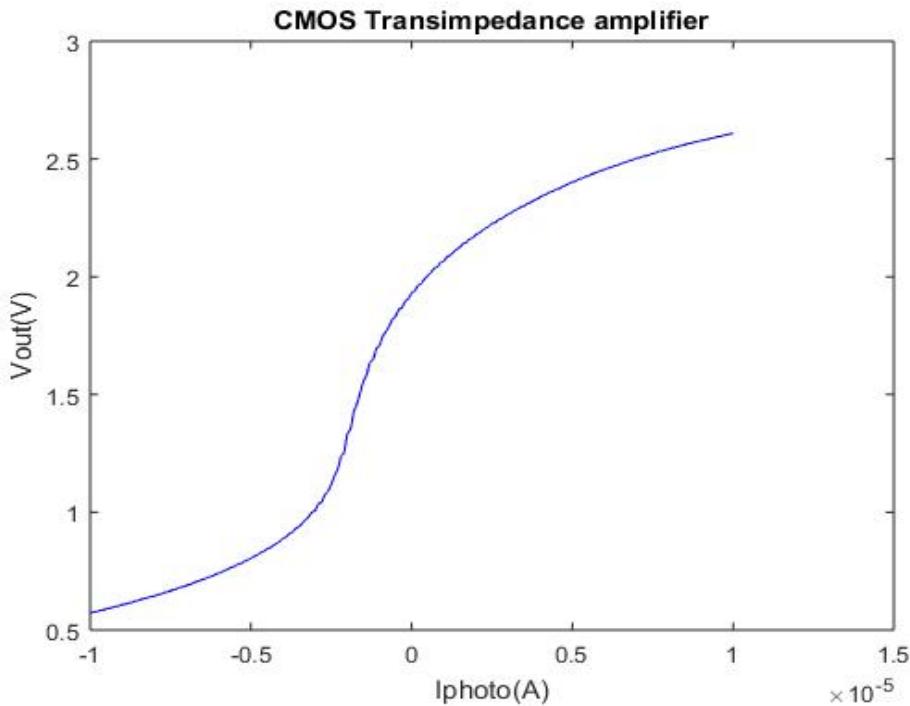


Figure 6.8 CMOS transimpedance amplifier fabricated in Carleton Fab

6.4 Conclusion

This chapter explored an alternative approach to demonstrate electronic and optical integration. All devices have been fabricated by in-house facilities at Carleton Micro Fab. CMOS circuit has been built on a fully depleted SOI microelectronics technology developed for fourth year undergraduate student project fabrication. We designed and successfully tested a CMOS transimpedance amplifier in this technology. We listed a process flow which can be used for monolithically integrate CMOS transimpedance amplifier and Schottky barrier waveguide photodiodes by Local Oxidation of Silicon Technique (LOCOS) in Appendix V. As part of this work we also evaluated the optical loss performance of Ni/nSi and Pd/nSi Schottky metal overlayers experimentally and

theoretically. Although the LOCOS technique for waveguide formation has received relatively little commercial attention, it provides an extremely simple and effective approach to integrate electronic and photonic components in SOI platform.

Chapter 7: Conclusions

7.1 Conclusions

The overall goal of this research project is to develop new techniques for the monolithic integration of electronic and optical waveguide devices in the SOI platform. We have focused on designing and demonstrating monolithic integrated waveguide photodetectors and transimpedance amplifiers since these components will be vital to most systems. We have also concentrated on devices suitable for sensor integration, in part because many important applications of SOI-based photonic sensing are under development, but also because the speed requirements of sensors are usually much more relaxed than those needed in telecommunications. However with plausible reductions in feature size using more advanced lithography than was available for this project the techniques and devices developed here could be extended to telecommunications or even intra-chip data transfer.

In the absence of a commercial foundry SOI technology offering conventional CMOS electronic devices integrated with photonic components, we have taken two different approaches towards the integration of amplifiers and photodetectors. In chapter 4, we have investigated the realization of lateral BJTs and JFETs in a co mmercial SOI photonics technology, the Singapore Institute of Microelectronics (IME) process. This technology includes low and high dose *n*- and *p*-type ion implants intended to provide doping for *pn* junction optical waveguide modulators and for photodiode optical detectors, but does not provide MOS devices. Using published implant parameters and Si film thicknesses, doping levels in the film were estimated and used to design BJTs and JFETs in accordance with the technology's layout rules. Simple SPICE models for the devices

were developed and used to support basic BJT transimpedance amplifier design. A complete layout including a variety of BJTs and JFETs test structures, waveguides, Ge photodiodes, and transimpedance amplifiers was submitted for fabrication via CMC in June 2016. Finished chips were returned in January 2017, and extensive testing has been carried out as described in chapter 5. Unfortunately the testing revealed that although the lateral BJTs demonstrate good base-emitter and base-collector diode characteristics, the common emitter current gain is less than unity. This extremely low current gain might be due to incomplete passivation resulting in high surface recombination velocity on the large base surface area. Working n-channel JFETs were obtained, although the pinch-off voltage was much higher than expected. In order to investigate these discrepancies between the initial design and the measurement. Medici simulation was used to generate structures based on the realistic device layout and fabrication conditions. All measured results were verified by physics modeling in Medici simulations. The low current gain in *LBJT* is certainly due to high surface recombination velocity with an incomplete oxide passivation on the device surface area. A small variation in JFET channel width could cause much difference in pinch-off voltage. Therefore, Medici simulation provided an agreement with SPICE model in the initial design, and a concept understanding of the investigated device in measurements.

In chapter 6, the second approach has been to develop our own technology in the Carleton University Microfabrication facility. This approach has been built on a fully depleted SOI microelectronics technology developed for fourth year undergraduate student project fabrication. We designed and successfully tested a CMOS transimpedance amplifier in this technology. As part of this work we evaluated the optical loss

performance of Ni/nSi and Pd/nSi Schottky metal overlayers experimentally and theoretically. Although the LOCOS technique for waveguide formation has received relatively little commercial attention, we show that it provides an extremely simple and effective approach to integrate electronic and photonic components in SOI. The devices and structures described in Chapter 6 could easily be integrated in almost any CMOS fabrication facility.

7.2 Contributions

We developed two novel approaches to realize monolithic integration of optical and electronic circuits. To our best knowledge, there are no commercial foundries available for full CMOS-photonics integration even though some industry companies have such technologies for their internal use.

We were extending my M.A.Sc research work - Schottky diode photodetectors integrated with waveguides formed by the Local Oxidation of Silicon (LOCOS) process using Carleton Microelectronics Fabrication Facility. We began by presenting a theoretical and experimental study of the optical loss associated with Schottky waveguide photodetectors. Then we have fabricated and evaluated a C MOS transimpedance amplifier using a technology completely compatible with LOCOS waveguide formation in the Carleton MicroFab. In order to realize optical and electronics integration with an existing fully – depleted SOI CMOS technology, we developed a plausible process flow for the waveguide Schottky diode and CMOS transimpedance amplifier monolithic integration by using in-house fabrication at Carleton.

While working on the Carleton LOCOS technology, we had an opportunity to participate in the CMC- sponsored workshop on Silicon Electronic Photonic Integrated Circuits

(SiEPIC), in 2015. We decided to focus our effort on this approach since an existing foundry technology is much more likely to be adopted by other researchers than an experimental technology developed in an in-house fabrication facility would be. We noted that the process could not support MOSFET fabrication due to lack of Polysilicon deposition, but JFET and lateral BJT transistors could be realized by using the implantation conditions for photonic components. With these electronic transistors, we then integrated transimpedance amplifiers with photonic devices including input/output grating couplers, SOI strip waveguide, and a Ge photo-detector. All the photonics and electronics devices were laid out and fabricated on the same SOI substrate. This is an example of comprehensive monolithic electronics and photonics integration in a foundry SOI technology. This is also the major contribution of this thesis. Regarding of the significance of this research work, we have published two journal and three conference papers as listed below:

1. S. Li, N. G. Tarr, P. Berini, and W. N. Ye," Optical and electrical performance of Schottky diodes on low loss SOI waveguides," *OSA Continuum*, vol.2, no.1, Jan. 2019
2. S. Li, N. G. Tarr and W. N. Ye," JFET integration using a foundry SOI photonics platform," *Appl. Sci.*, vol.9, no.19, 2019
 - This paper was selected as the Issue Cover for Issue 19, 2019 of Applied Science.
3. S. Li, N. G. Tarr, W. N. Ye, and P. Berini," Pd Schottky barrier photodetector integrated with LOCOS -defined SOI waveguides," *IEEE 12th International Conference Group IV Photonics*, August 2015

4. S. Li, N. G. Tarr, and W. N. Ye," Monolithic integration of SOI waveguide photodetectors and transimpedance amplifiers," *SPIE Proc.*, vol.10537, 2018
5. S. Li, N. G. Tarr and W. N. Ye," Monolithic integration of opto-electronics by silicon photonics foundry service," *SPIE Proc.*, vol.10922, 2019

7.3 Future work

We have focused on designing and demonstrating monolithic integration of opto-electronics by IME – a commercial foundry offering conventional CMOS electronic devices integrated with photonic components on SOI platform. We implemented *LBJT* and *JFET* using variety of *n*- and *p*-type ion implants intended to support waveguide modulators and photodetectors fabrication. Experimental results could be used to refine the compact device models and apply to further integration with biosensors. A second SiEPIC run with revised transistors and transimpedance amplifiers design can be fabricated in the IME technology. Moreover, we have designed a process flow for integration of low-loss optical waveguides and fully-depleted SOI CMOS technology by using an in-house fabrication in the Carleton University Microfabrication Facility. With the availability of resource and investment at Carleton Fab, an optical and electronics fully integration can be explored for “wire” dimensional waveguide and CMOS transimpedance amplifier on SOI platform.

Bibliography of References:

- [1] X. Fan, I. M. White, S. I. Shopova, H. Zhu et al, “Sensitive optical biosensors for unlabeled targets: A review,” *Analytica Chimica Acta*, vol. 620, no. 1-2, pp. 8-26, Jul 2008.
- [2] A. Shacham, K. Bergman, and L. P. Carloni. “Photonic networks on-chip for future generations of chip multiprocessors,” *IEEE Transactions on Computers*, vol. 57, no. 9, pp. 1246–1260, Sept. 2008.
- [3] A. A. Trusov, I. P. Prikhodko, S. A. Zotov, A. R. Schofield, and A. M. Shkel. “Ultra-High Q Silicon Gyroscopes with Interchangeable Rate and Whole Angle Modes of Operation,” *Proc. IEEE Sensors*, pp. 864–867, Nov. 2010
- [4] M. Guilln-Torres, E. Cretu, N.A.F. Jaeger, and L. Chrostowski. “Ring Resonator Optical Gyroscopes – Parameter Optimization and Robustness Analysis,” *Journal of Lightwave Technology*, vol. 30, no. 12, pp. 1802–1817, 2012.
- [5] K. Busch, S. Lolkes, R. B. Wehrspohn, H. Foll, *Photonic Crystals: Advances in Design, Fabrication, and Characterization*, pp. 238-246, Wiley-VCH Verlag GmbH& Co. KGaA, May 2006.
- [6] R. Camacho-Aguilera, Y. Cai, N. Patel, J. Bessette, M. Romagnoli, L. Kimerling, and J. Michel. “An electrically pumped germanium laser,” *Opt Express*, vol. 20, no. 10, pp. 11316–11320, May 2012.
- [7] H. Y. Liu, T. Wang, Q. Jiang, R. Hogg, F. Tutu, F. Pozzi, and A. Seeds. “Long-wavelength InAs/GaAs quantum-dot laser diode monolithically grown on Ge substrate,” *Nature Photonics*, pp. 416–419, Feb. 2011.

- [8] J. K. Doylend, M. J. R. Heck, J. T. Bovington, J. D. Peters, L. A. Coldren, and J. E. Bowers. “Two-dimensional free-space beam steering with an optical phased array on silicon-on-insulator,” Opt Express, vol. 19, no. 22, pp. 21595–21604, Oct. 2011.
- [9] Pallab Bhattacharya, *Semiconductor Optoelectronic Devices*, 2nd edition, Prentice Hall, 1997.
- [10] Moore, G. E., Cramming more components onto integrated circuits, Proc. IEEE, 86 (1), pp. 82–85, 1998.
- [11] G-S Jeong, W. Bae adnd D-K Jeong, “Review of CMOS integrated circuit technologies for High-speed Photo-detection”, Sensors, 17(9), 2017
- [12] Soref R and Lorenzo J 1985 Single-crystal silicon: a new material for 1.3 and 1.6 μm integrated-optical components Electron. Lett. 21 953–4
- [13] R. A. Soref, Silicon-based optoelectronics, Proc. IEEE, 81, pp. 1687–1706, 1993.
- [14] C. Gunn, “CMOS photonics technology overview,” IEEE Compound Semiconductor Integrated Circuit Symposium, 139-140 (2006).
- [15] C. Xiong, D. M. Gill, J. E. Proesel, J. S. Orcutt, W. Haensch, and W. M. J. Green, “Monolithic 56 Gb/s silicon photonic pulse-amplitude modulation transmitter,” Optica, vol.3, no.10, pp. 1060-1065, 2016
- [16] <https://www.sdxcentral.com/articles/news/intel-says-silicon-photonics-transceivers-will-be-a-5g-fronthaul-savior/2018/09/>
- [17] <https://www.globalfoundries.com/>
- [18] Xiaodoing Xu, “Optoelectronic device integration in silicon,” University of Washington, Final report, 2015
- [19] Agency for Science, Technology and Research (A*STAR) Institute of Microelectronics (IME) Silicon Photonics. http://www.ime.astar.edu.sg/page/silicon_photonics

- [20] S. Li, N. G. Tarr, N. Ye, "Pd Schottky Barrier Photodetector Integrated With LOCOS-Defined SOI Waveguides," IEEE 12th International Conference Group IV Photonics, Aug. 2015.
- [21] S. Li, N. G. Tarr and P. Berini, "Schottky Photodetector Integration on LOCOS-Defined SOI Waveguides," Proc. SPIE, vol. 7750, Photonics North 2010.
- [22] R. A. Soref and J. P. Lorenzo, "All-silicon active and passive guided-wave component for $\lambda=1.3$ and $1.6 \mu\text{m}$," IEEE Journal of Quantum Electronics, vol. 22, no. 6, pp. 873-879, Jun 1986.
- [23] R. A. Soref and J. P. Lorenzo, "Single-crystal silicon: a new material for 1.3 and $1.6 \mu\text{m}$ integrated-optical components," Electronics Lett., vol. 21, no. 21, pp. 953-954, Oct 1985.
- [24] E. Cortesi, F. Namavar and R. A. Soref, "Novel silicon-on-Insulator structure for silicon waveguides," IEEE SOS/SOI Technology Conference, Stateline, NV, USA, Oct 1989.
- [25] B. N. Kurdi and D. G. Hall, "Optical waveguide in oxygen-implanted buried-oxide silicon-on-insulator structures," Opt. Lett., vol. 13, no. 2, pp. 175-177, 1988.
- [26] Reed, G.T., L. Jinhua, C.K. Tang, L. Chenglu, P.L.F. Hemment, and A.G. Rickman, Silicon on insulator optical waveguides formed by direct wafer bonding. Mat. Sci. Eng. B: Solid, 1992. B15 (2): p. 156-159
- [27] Evans, A.F., D.G. Hall, and W.P. Maszara, Propagation loss measurements in silicon-on-insulator optical waveguides formed by the bond-and-etchback process. Appl. Phys. Lett., 1991. 59(14): p. 1667-9
- [28] Kurdi, B.N. and D.G. Hall, Optical waveguides in oxygen-implanted buried-oxide silicon-on-insulator structures. Opt. Lett., 1988. 13(2): p. 175-7
- [29] Schmidtchen, J., A. Splett, B. Schuppert, and K. Petermann. Low loss integrated-optical rib-waveguides in SOI. in 1991 IEEE International SOI Conference, Oct 1-3 1991. 1992. Vail Valley, CO, USA: Publ by IEEE, Piscataway, NJ, USA. 75

- [30] G.T. Reed, W. R. Headley, C. E. Jason Png, "Silicon photonics: the early years," Proc.SPIE 5730, Optoelectronic Integration on Silicon II, 2005
- [31] Reed, Graham T, *Silicon Photonics: the state of art*, Chichester: Wiley, 2008
- [32] A. Densmore, D-X. Xu, P. Waldron, "A silicon-on-insulator photonic wire based evanescent field sensor," IEEE Photonics Technology Letters, vol. 18, no. 23, pp. 2520-2522, Dec 2006
- [33] A. Densmore, M. Vachon, D-X. Xu, S Janz et al, "Silicon photonic ware biosensor array for multiplexed real-time and label-free molecular detection," Opt Lett., vol. 34, no. 23, pp. 3598-3600, Dec. 2009.
- [34] V. M. N. Passaro, F. Dell'Olio, B. Casamassima and F. D. Leonardis, "Guided-Wave Optical Biosensors," Sensors, vol.7, no. 4, pp. 508-536, Apr. 2007.
- [35] N. S. Droz, A. Gondarenko and M. Lipson, "Oxidized Silicon-On-Insulator (OxSOI) from bulk silicon: a new photonic platform," Opt. Express, vol.18, no. 6, pp. 5785-5790, Mar 2010.
- [36] S. Sridaran and S. A. Bhave, "Nanophotonic devices on thin buried oxide Silicon-On-Insulator substrates," Opt. Express, vol. 18, no. 4, pp. 3850-3857, Feb 2010.
- [37] R. A. Soref, J. Schmidtchen, and K. Petermann, "Large single mode rib waveguides in GeSi-Si and Si-on-SiO₂," IEEE J. Quant. Electron., VOL. 27, NO. 8, pp. 1971–1974, Aug. 1991.
- [38] R. A. Soref and J. P. Lorenzo, "Single-crystal silicon – a new material for 1.3 and 1.6 μm integrated-optical components," Electron. Lett, vol. 21, no. 21, pp. 953–954, 1985.
- [39] T. Ernst, C. Tinella, C. Raynoud, and S. Cristoloveanu, "Fringing fields in sub-0.1 μm fully depleted SOI MOSFETs: optimization of the device architecture," Solid-State Electron. 46(3), 373–378 (2002).

- [40] T. Ernst, and S. Cristoloveanu, “Buried oxide fringing capacitance: a new physical model and its implication on SOI device scaling and architecture,” in Proceedings of IEEE International SOI Conference (Institute of Electrical and Electronics Engineers, New York, 1999), pp. 38–39.
- [41] J. Gao, H. –C. Wu, G. Liu, E. Lau, L. Yuan, C. Krause, and H. Cheng, “ 2×25 G low power optical IC for Thunderbolt optical cable technology,” IEEE Optical Interconnects Conference, 18-19 (2016).
- [42] S. Assefa, S. Shank, W. Green, et al., “A 90 nm CMOS integrated nano-photonics technology for 25 Gbps WDM optical communications applications,” IEDM IEEE International, 809-811 (2012).
- [43] C. Gunn, “CMOS photonics technology overview,” IEEE Compound Semiconductor Integrated Circuit Symposium, 139-140 (2006).
- [44] F. Boefu, S. Cremer, E. Temporiti, M. Fere, et al., “Recent progress in silicon photonics R&D and manufacturing on 300mm wafer platform”, IEEE Optical society of America, 2015.
- [45] Georgas, M.; Orcutt, J.; Ram, R.J.; Stojanovic, V. A monolithically-integrated optical receiver in standard 45-nm SOI. IEEE J. Solid-State Circuits 2012, 47, 1693–1702.
- [46] Buckwalter, J.F.; Zheng, X.; Li, G.; Raj, K.; Krishnamoorthy, A.V. A monolithic 25-Gb/s transceiver with photonic ring modulators and Ge detectors in a 130-nm CMOS SOI process. IEEE J. Solid-State Circuits 2012, 47, 1309–1322.
- [47] V. Stojanovic, R.J. Ram, M. Popovic, S. Lin, S. Moazeni, M. Wade, C. Sun, L. Alloatti, A. Atabaki, F. Pavanello, N. Mehta, and P. Bhargava, “Monolithic silicon-photonic platforms in state-of-the-art CMOS SOI processes,” Optics express, 28 (10), 2018.
- [48] C. Tomovich, “MOSIS -- A gateway to silicon,” IEEE Circuits and Devices Magazine, pp. 22–23, 1988.

[49] Khanna, Y. Drissi, P. Dumon, et al. “ePIXfab: the silicon photonics platform,” Proc. SPIE, Integrated photonics: materials, devices, and applications II, vol. 8767, May 2013.

[50] PIXfab - The silicon photonics platform - MPW Technologies,
http://www.epixfab.eu/index.php?option=com_content&view=article&id=50&Itemid=60.

[51] Op SIS Foundry. url: <http://www.opsisfoundry.org> (cit. on pp. 14, 32).

[52] *Handbook of silicon photonics*

[53] Vivien, L.; Polzer, A.; Marris-Morini, D.; Osmond, J.; Hartmann, J.M.; Crozat, P.; Cassan, E.; Kopp, C.; Zimmermann, H.; Fédeli, J.M. Zero-bias 40 Gbit/s germanium waveguide photodetector on silicon. *Opt. Express* 2012, 20, 1096–1101.

[54] Assefa, S.; Xia, F.; Vlasov, Y.A. Reinventing germanium avalanche photodetector for nanophotonic on-chip optical interconnects. *Nature* 2010, 464, 80–84.

[55] J. J. Ackert, A. S. Karar, D. J. Paez, P. E. Jessop, J. C. Cartledge, and A. P. Knights, “10 Gbps silicon waveguide-integrated infrared avalanche photodiode”, *Opt. Express* 21.17(2013), pp.19530-19537

[56] R. R. Grote, K. Padmaraju, B. Souhan, J. B. Driscoll, K. Bergman, and RM Osgood, “10 Gb/s Error-free operation of all-silicon ion-implanted waveguide photodiodes at 1.55”, *Photonics technology Lett. IEEE* 2.1(2013), pp.67-70

[57] JK Doylend, PE Jessop, and A. P. Knights, “Silicon photonic resonator enhanced defect-mediated photodiode for sub-bandgap detection”, *Optics express* 18.14 (2010) pp.14671-14678

[58] G. Dehlinger, S. J. Koester, J. D. Schaub, J. O. Chu, Q. C. Ouyang, and A. Grill, “ High-speed germanium-on-SOI lateral PIN photodiodes,” *IEEE Photon. Technol. Lett.*, vol. 16, no. 11, pp. 2547-2549,2004

- [59] D. Ahn, C.-Y. Hong, J. Liu, W. Giziewiez, M. Beals, L. C. Kimerling, J. Michel, J. Chen, and F. X. Kartner, "high performance waveguide integrated Ge photodetector," *Opt.Exp.*, vol 15, pp.3916-3921,2007
- [60] G. Masini, L. Colace, and G. Assanto, "2.5 Gbit/s polycrystalline germanium-on-silicon photodetector operating from 1.3-1.55 um," *Appl. Phys. Lett.*, vol. 82, pp.2524-2526,2003
- [61] A. Novack, M. Gould, Y. Yang, Z. Xuan, M. Streshinsky, Y. Liu, G. Capellini, A. Eu-Jin Lim, G. Lo, Tom B.-J., and M.Hochberg, " Germanium photodetector with 60 GHz bandwidth using inductive gain peaking", *Opt. Express* 21.23(2013), pp. 28387{28393.
- [62] T. Y. Liow, K.-W. Ang, Q. Fang, J.-F. Song, Y.-Z. Xiong, M.-B. Yu, G.-Q. Lo, and D.-L. Kwong, "Silicon modulators and germanium photodetectors on SOI: monolithic integration, compatibility, and performance optimization". *Selected Top- topics in Quantum Electronics*, IEEE Journal of 16.1 (2010), pp. 307
- [63] I. Goykhman, U.Sassi, B. Desiatov, N. Mazurski, S. Milana, D. de Fazio, A. Eiden, J. Khurgin, J. Shappir, U. Levy and A. C. Ferrari, "On-chip integrated, silicon-Graphene plasmonic Schottky photodetector with high responsivity and avalanche photogain," *Nano Lett.* **16**(5), 3005–3013 (2015).
- [64] S. Li, N.G. Tarr and P. Berini, "Schottky Photodetector Integration on LOCOS-Defined SOI Waveguides," *Proc. of SPIE* **7750**, 77501M (2010).
- [65] S. Li, Winnie N. Ye, N. G. Tarr and P. Berini," Pd Schottky barrier photodetector integrated with LCOS-defined SOI waveguides." 7305975, 2015 IEEE 12th International Conf. on Group IV photonics (GFP), 2015
- [66] M. Casalino, G. Coppola, R. M. De La Rue, and D. F. Logan, "State-of-the-art all-silicon sub-bandgap photodetectors at telecom and Datacom wavelengths," *Laser & Photonics Rev.***10**(6), 895–921 (2016).

- [67] I. Goykhman, B. Desiatov, J. Khurgin, J. Shappir and U. Levy, “Waveguide based compact silicon Schottky photodetector with enhanced responsivity in the telecom spectral band,” Opt. Express **20**(27), 28594–28602 (2012).
- [68] Dimitrijev, Sima, *Principles of Semiconductor Devices* (2nd Edition) Oxford University Press 2012
- [69] L. K. Rowe, M. Elsey, E. Post, N. G. Tarr and A. P. Knights, “A CMOS-compatible rib waveguide with local oxidation of silicon isolation,” Proc. SPIE **6477**, 64770L (2007).
- [70] F. Y. Gardes, G. T. Reed, A. P. Knights, G. Mashanovich, P. E. Jessop, L. Rowe, S. McFaul, D. Bruce, N. G. Tarr, “Sub – micron optical waveguides for silicon photonics formed via the local oxidation of silicon (LOCOS),” proc. SPIE **6898**, 68980R (2008).
- [71] S. Li, N. G. Tarr, P. Berini and W. N. Ye, “Optical and electrical performance of Schottky diodes on low loss SOI waveguides,” OSA Continuum, 2 (1), pp.74-82, 2019
- [72] J. Hu, X. Sun, A. Agarwal, and L. Kimerling. “Design guidelines for optical resonator biochemical sensors,” Journal of the Optics Society of America B, vol. 26, no. 5, pp. 1032–1041, 2009.
- [73] M. Iqbal, M. A. Gleeson, B. Spaugh et al., “Label-free biosensor arrays based on silicon ring resonators and high-speed optical scanning instrumentation,” IEEE Journal of Selected Topics in Quantum Electronics, vol. 16, no. 3, pp. 654–661, Mar. 2010.
- [74] Densmore, A.; Xu, D.X.; Janz, S.; Waldron, P.; Mischki, T.; Lopinski, G.; Delâge, A.; Lapointe, J.; Cheben, P.; Lamontagne, B.; et al. Spiral-path high-sensitivity silicon photonic wire molecular sensor with temperature-independent response. Opt. Lett. 2008, 33, 596–598.
- [75] De Vos, K.; Bartolozzi, I.; Schacht, E.; Bienstman, P.; Baets, R. Silicon-on-Insulator microring resonator for sensitive and label-free biosensing. Opt. Express 2007, 15, 7610–7615.

- [76] Grist, S.M.; Schmidt, S.A.; Flueckiger, J.; Donzella, V.; Shi, W.; Fard, S.T.; Kirk, J.T.; Ratner, D.M.; Cheung, K.C.; Chrostowski, L. Silicon photonic micro-disk resonators for label-free biosensing. *Opt. Express* 2013, 21, 7994–8006.
- [77] Jugessur, A.; Dou, J.; Aitchison, J.; DeLaRue, R.; Gnan, M. A photonic nano-Bragg grating device integrated with microfluidic channels for bio-sensing applications. *Microelectron. Eng.* 2009, 86, 1488–1490.
- [78] Xu, D.X.; Schmid, J.H.; Reed, G.T.; Mashanovich, G.Z.; Thomson, D.J.; Nedeljkovic, M.; Chen, X.; Van Thourhout, D.; Keyvaninia, S.; Selvaraja, S.K. Silicon photonic integration platform—Have we found the sweet spot? *IEEE J. Sel. Top. Quantum Electron.* 2014, 20, 189–205.
- [79] Chen, H.; Verheyen, P.; De Heyn, P.; Lepage, G.; De Coster, J.; Balakrishnan, S.; Absil, P.; Yao, W.; Shen, L.; Roelkens, G.; Van Campenhout, J. -1 V bias 67 GHz bandwidth Si-contacted germanium waveguide p-i-n photodetector for optical links at 56 Gbps and beyond. *Opt. Express* 2016, 24, 4622.
- [80] Laplatine, L.; Al'Mrayat, O.; Luan, E.; Fang, C.; Rezaiezadeh, S.; Ratner, D.; Cheung, K.; Dattner, Y.; Chrostowski, L. System-level integration of active silicon photonic biosensors. *Microfluidics BioMEMS Med. Microsyst. XV* 2017, 10061, 100610I.
- [81] Wang, J.; Yao, Z.; Lei, T.; Poon, A.W. Silicon coupled-resonator optical-waveguide-based biosensors using light-scattering pattern recognition with pixelized mode-field-intensity distributions. *Sci. Rep.* 2014, 4, 7528.
- [82] Chao, C.Y.; Guo, L.J. Biochemical sensors based on polymer microrings with sharp asymmetrical resonance. *Appl. Phys. Lett.* 2003, 83, 1527–1529.
- [83] Genalyte 2017 Silicon photonics biosensor technology www.genalyte.com/about-us/ourtechnology/

- [84] Chen C 2017 Silicon valley cash is still chasing blood despite theranos bust (Bloomberg)
www.bloomberg.com/news/articles/2017-01-06/silicon-valley-cash-is-still-chasing-blood-despite-theranos-bust
- [85] 2016 Belgian startup lands EUR 7M for optical glucose monitoring chip SPIE/Optics.org
<http://optics.org/news/7/12/30>
- [86] S.M.Sze, M.K.Lee, *Semiconductor Devices: Physics and Technology*, 3rd Edition, John Wiley & Sons, Inc
- [87] C. Hu, *Modern Semiconductor devices for integrated circuit*, Pearson, 2010
- [88] Dimitrijev, Sima, *Principles of Semiconductor Devices* (2nd Edition) Oxford University Press 2012 ref: BJT1 and JFET1
- [89] S. M. Sze, and Kwok K. Ng, *Physics of semiconductor devices*, John Wiley & Sons, Incorporated, 2006
- [90] Jean-Pierre, Colinge, C. A. Colinge, *Physics of semiconductor devices*, Kluwer Academic Publishers, Boston, 2002
- [91] E. Sackinger, *Analysis and design of transimpedance amplifiers for optical receivers*, Wiley, 2017
- [92] J. Choi, B. J. Sheu, and O.T.-C. Chen, A monolithic GaAs receiver for optical interconnect systems, *IEEE J. Solid-State Circuit*, SC-29(3), pp 328-331, 1994
- [93] K. D. Pedrotti, R. L. Pierson Jr., N. H. Sheng, R. B. Nubling, C. W. Farley, and M. F. Chang, High-bandwidth OEIC receivers using heterojunction bipolar transistors: design and demonstration, *J. Lightwave Technol.*, LT-11(10), PP 1601-1614, 1992
- [94] S. Radovanovic, A.-J. Annema, and B. Nauta, A 3-Gb/s optical detector in standard CMOS for 850-nm optical communication, *IEEE J. Solid-State Circuits*, SC-40(8), pp 1706-1717, 2005

- [95] L. Vivien, L. Pavesi, *Handbook of Silicon Photonics*, 1st edition, CRC press, 2013
- [96] T.-Y. Liow, K.-W. Ang, Q. Fang, J.-F. Song, Y.-Z. Xiong, M.-B. Yu, G.-Q. Lo, and D.-L. Kwong. Silicon modulators and germanium photodetectors on SOI: monolithic integration, compatibility, and performance optimization. *IEEE J. Sel. Top. Quantum Electron.*, **16**(1):307–315, 2010.
- [97] D.D. Cannon, J. Liu, Y. Ishikawa, K. Wada, “Tensile strained epitaxial Ge films on Si(100) substrates with potential application in L-band telecommunications,” *Apiled Phy Lett.*, 84(6) pp 906-908,2004
- [98] O.I. Dosunmu, D.D. Cannon, M.K. Emsley, and L.C. Kimerling, “High speed resonant-cavity enhanced Ge photodetectors on reflecting Si substrates for 1550 nm operation,” *Conf. Lasers and Electro-Optics Society*, 2004
- [99] I. Goykhman. B. Desiatov, J. Khurgin, J. Shappir and U. Levy, “Locally-oxidized silicon surface-plasmon Schottky detector for telecom regime,” *Nano Lett.* **11**(6), 2219-2224 (2011).
- [100] S. Zhu, H. S. Chu, G. Q. Lo, P. Bai and D. L. Kwong, “Waveguide-integrated near-infrared detector with self-assembled metal silicide nanoparticles embedded in a silicon p-n junction,” *Appl. Phys. Lett.* 100, 061109 (2012).
- [101] S. Li, N. G. Tarr, W. N. Ye, “Pd Schottky Barrier Photodetector Integrated With LOCOS-Defined SOI Waveguides,” *IEEE Group IV Photonics conference* (IEEE, 2015), pp. 112-113.
- [102] Dimitrijev, Sima, *Principles of semiconductor devices*, 2nd edition, Oxford University Press, 2012
- [103] H. K. Zimmermann, *Integrated Silicon Optoelectronics*, Springer Berlin Heidelberg, 2010
- [104] J. Qi, C.L. Schow, L.D. Garrett, J.C. Campbell,” A silicon NMOS monolithically integrated optical receiver”, *IEEE Photonics Techno Lett.* 9 (5), pp.663-665

- [105] J.S. Rieh, D. Klotzkin, O. Qasaimeh, L.H. Lu, K. Yang, L.P.B. Katehi, P. Bhattacharya, E.T. Croke, IEEE Photonics Technol. Lett. 10(3), 415 (1998)
- [106] T.-Y. Lin, R. J. Green and P.B. O'Connor, "A low noise single-transistor transimpedance preamplifier for Fourier-transform mass spectrometry using a T feedback network," Rev. Sci. Instrum. 83, 094102 (2012)
- [107] P. Horowitz, W. Hill, The art of electronics, Cambridge University Press, Third edition, 2015
- [108] L. Chrostowski, M. Hochberg, *Silicon Photonics design*, pp. 31, 2014
- [109] IME Silicon Photonics Process flow
- [110] T. -Y. Liow, K.-W. Ang, Q. Fang, J.-F. Song, Y.-Z. Xiong, M.-B. Yu, G.-Q. Lo and D.-L. Kwong, "Silicon modulators and Germanium photodetectors on SOI: Monolithic integration, compatibility, and performance optimization," IEEE Journal of Selected Topics in Quantum Electronics, vol.16, no.1, pp. 307-315, Feb.2010.
- [111] KP Yap, J. Lapointe, B. Lamontagne, A. Delge, A. Bogdanov, S. Janz, and B. Syretta. "SOI waveguide fabrication process development using star coupler scattering loss measurements". Proc. Device and Process Technologies for Microelectronics, MEMS, Photonics, and Nanotechnology IV, SPIE (2008)
- [112] Christopher G Poulton, Christian Koos, Masafumi Fujii, Andreas Pfrang, Thomas Schimmel, Jrg Leuthold, and Wolfgang Freude. "Radiation modes and roughness loss in high index-contrast waveguides". Selected Topics in Quantum Electronics, IEEE Journal of 12.6 (2006), pp. 1306–1321
- [113] Frdric Grillot, Laurent Vivien, Suzanne Laval, and Eric Cassan. "Propagation loss in single-mode ultrasmall square silicon-on-insulator optical waveguides". Journal of lightwave technology 24.2 (2006), p. 891

- [114] Wim Bogaerts, Pieter Dumon, et al. "Compact Wavelength-Selective Functions in Silicon-on-Insulator Photonic Wires". IEEE Journal of Selected Topics in Quantum Electronics 12, Issue 6 (2006)
- [115] Tsung-Yang Liow, Kah-Wee Ang, Qing Fang, Jun-Feng Song, YongZhong Xiong, Ming-Bin Yu, Guo-Qiang Lo, and Dim-Lee Kwong. "Silicon modulators and germanium photodetectors on SOI: monolithic integration, compatibility, and performance optimization". Selected Topics in Quantum Electronics, IEEE Journal of 16.1 (2010), pp. 307–315
- [116] T.-Y. Liow, E.-J Lim, N. Duan, M. Yu and G.-Q, Lo, "Waveguide Germanium photodetector with high bandwidth and high L-band responsivity," OFC Technical digest 2013 OSA
- [117] F. Van Laere, T. Claes, J. Schrauwen, S. Scheerlinck, W. Bogaerts, D. Taillaert, L. O'Faolain, D. Van Thourhout, and R. Baets. "Compact focusing grating couplers for silicon-on-insulator integrated circuits". Photonics Technology Letters, IEEE 19.23 (2007), pp. 1919–1921
- [118] R. Waldhusl, B. Schnabel, P. Dannberg, E.B. Kley, A. Bruer, and W. Karthe. "Efficient coupling into polymer waveguides by gratings". Applied optics 36.36 (1997), pp. 9383–9390
- [119] Tom Baehr-Jones, Ran Ding, Ali Ayazi, Thierry Pinguet, Matt Streshinsky, Nick Harris, Jing Li, Li He, Mike Gould, Yi Zhang, Andy Eu-Jin Lim, Tsung-Yang Liow, Selin Hwee-Gee Teo, Guo-Qiang Lo, and Michael Hochberg. "A 25 Gb/s Silicon Photonics Platform". arXiv:1203.0767v1 (2012)
- [120] R. Dutton, ``TCAD Tools at Stanford University: SUPREM4," <http://www-tcad.stanford.edu/tcad/programs/suprem4.html>.
- [121] Dimitrijev Sima, *Principles of semiconductor devices*, 2nd edition, Oxford University Press, 2012

- [122] Jean-Pierre, Colinge, Cynthia A. Colinge, *Physics of semiconductor devices*, Kluwer Academic Publishers, 2002.
- [123] K.-W. Ang, G.-Q. Lo, D.-L. Kwong, *Semiconductor Technologise*, 2010
- [124] Paul, H., Winfield, H., [The Art of Electronics], Cambridge University Press, New York, 2015
- [125] E. Bendada, K. Rais, P. Mialhe and J.P. Charles, "Surface recombination via interface defects in field effect transistors," Active and Passive Elec. Comp. Vol.21, pp. 61-71, 1998
- [126] Simon M. Sze, Ming-Kwei Lee, *Semiconductor Devices: Physics and Technology*, 3rd Edition, John Wiley & Sons, 2012
- [127] Kanaan Kano, *Semiconductor devices*, Prentice Hall Inc., New Jersey, 1998.
- [128] A. Densmore, D.-X.Xu, S. Janz, P. Waldron, T. Mischki, G. Lopinski, A. Delage, J. Lapointe, P.Cheben, B.Lamontagne, and J. H. Schmid, "Spiral-path high-sensitivity silicon photonic wire molecular sensor with temperature-independent response," Optics lett., vol.33(6),2008
- [129] A. Densmore, M. Vachon, D.-X. Xu, S. Janz, R. Ma, Y.-H. Li, G. Lopinski, A. Delage, J. Lapointe, C. C. Luebbert, Q. Y. Liu, P. Cheben, and J. H. Schmid, "Silicon photonic wire biosensor array for multiplexed real-time and label-free molecular detection," Optics Lett., vol.34 (23),2009
- [130] S. Li, N. G. Tarr, N. Ye, "Pd Schottky Barrier Photodetector Integrated With LOCOS-Defined SOI Waveguides," IEEE 12th International Conference Group IV Photonics, Aug. 2015.
- [131] S. Li, N. G. Tarr and P. Berini, "Schottky Photodetector Integration on LOCOS-Defined SOI Waveguides," Proc. SPIE, vol. 7750, Photonics North 2010.

- [132] L. K. Rowe, M. Elsey, E. Post, N. G. Tarr and A. P. Knights, “A CMOS-compatible rib waveguide with local oxidation of silicon isolation,” Proc. SPIE **6477**, Silicon Photonics II, 64770L (2007).
- [133] C. Scales and P. Berini, “Thin-film Schottky Barrier Photodetector Models,” IEEE J. Quantum Electronics, **46** (5), 633-643 (2010).
- [134] S. T. Fard, S. M. Grist, V. Donzella, S. A. Schmidt, J. Flueckiger, X. Wang, W. Shi, A. Millspaugh, M. Webb, D. M. Ratner, K. C. Cheung, L. Chrostowski, “Label-free silicon photonic biosensors for use in clinical diagnostics,” Proc. SPIE **8629**, 862909 (2013).
- [135] A. S. Sudbo, “Film mode matching: a versatile numerical method for vector mode field calculations in dielectric waveguides,” Pure Appl. Opt. **2** (3), 211-233 (1993).
- [136] A. S. Sudbo, “Film mode matching: a versatile numerical method for vector mode field calculations in dielectric waveguides,” Pure Appl. Opt., vol. 2, no. 3, pp. 211-233, 1993.
- [137] F. Y. Gardes, G. T. Reed, A. P. Knights, et al., “Sub – micron optical waveguides for silicon photonics formed via the local oxidation of silicon (LOCOS),” proc. SPIE, vol. 6898, Feb. 2008.
- [138] A. D. Rakić, A. B. Djurišić, J. M. Elazar, and M. L. Majewski. “Optical properties of metallic films for vertical-cavity optoelectronic devices,” Appl. Opt., vol. 37, no. 22, pp. 5271-5283, Aug. 1998.
- [139] E. D. Palik, G. Ghosh, “*Handbook of optical constants of solids*,” Elsevier, 1998.
- [140] P. Karasinski, “Modal attenuation in metal-clad graded-index slab optical waveguides,” Optics Communications, vol. 280, no. 2, pp. 351-358, Dec. 2007.
- [141] A. M. Moloney, A. P. Morrison, J. C. Jackson, et al., “Monolithically integrated avalanche photodiode and transimpedance amplifier in hybrid bulk/SOI CMOS process,” Electronics Lett., vol. 39, no. 4, Feb. 2003.

APPENDIX I

```
$ npn Base Boron implantation

$ Full non-equilibrium point defect model
$(includes transient enhanced diffusion)
method pd.full

$ Graphics written as postscript file
option device="c/postscript" plot.out="basenpn.ps"

$set the grid spacing
mesh dy.surf=0.002

$ Set the well background doping
initialize boron=1e15

implant boron dose=5e12 energy=16

$ Plot the as-implanted phosphorus distribution
select z=log10(boron) title="npn LBJT base implant"
plot.1d top=19 bottom=14 right=0.22 color=2
select z=log10(boron)
plot.1d ^ax ^cl color=1

$pad oxide
deposit oxide thick=0.05

$drive-in
diffusion temp=1030 time=300

$ remove oxide
Etch oxide

$ Plot the phosphorus distribution
select z=log10(boron)
plot.1d ^ax ^cl color=2

$ Label the plot
Label x=0.5 y=14.9 Label=Boron color=1
Label x=0.2 y=16.6 Label=boron color=2

select z=doping
print.1d layers

stop
```

```

end

$ collector Phosphorus implantation

$ Full non-equilibrium point defect model
$(includes transient enhanced diffusion)
method pd.full

$ Graphics written as postscript file
option device="c/postscript" plot.out="collectornpn.ps"

$set the grid spacing
mesh dy.surf=0.002

$ Set the well background doping
initialize boron=1e15

implant phosphorus dose=3e12 energy=110

$ Plot the as-implanted phosphorus distribution
select z=log10(phosphorus) title="npn LBJT collector implant"
plot.1d top=19 bottom=14 right=0.22 color=3
select z=log10(boron)
plot.1d ^ax ^cl color=1

$pad oxide
deposit oxide thick=0.05

$drive-in
diffusion temp=1030 time=300

$ remove oxide
Etch oxide

$ Plot the phosphorus distribution
select z=log10(phosphorus)
plot.1d ^ax ^cl color=3

$ Label the plot
Label x=0.5 y=14.9 Label=Boron color=1
Label x=0.05 y=16.6 Label=Phosphorus color=3

select z=doping
print.1d layers

```

```

stop
end

$ emitter Phosphorus implantation

$ Full non-equilibrium point defect model
$(includes transient enhanced diffusion)
method pd.full

$ Graphics written as postscript file
option device="c/postscript" plot.out="emitternpn.ps"

$set the grid spacing
mesh dy.surf=0.002

$ Set the well background doping
initialize boron=1e15

implant phosphorus dose=4e15 energy=30

$ Plot the as-implanted phosphorus distribution
select z=log10(phosphorus) title="npn LBJT emitter implant"
plot.1d top=21 bottom=14 right=0.22 color=3
select z=log10(boron)
plot.1d ^ax ^cl color=1

$pad oxide
deposit oxide thick=0.05

$drive-in
diffusion temp=1030 time=300

$ remove oxide
Etch oxide

$ Plot the phosphorus distribution
select z=log10(phosphorus)
plot.1d ^ax ^cl color=3

$ Check that all the phosphorus is electrically active
select z=log10(active(phosphorus))
plot.1d ^ax ^cl color=4

```

```
$ Label the plot  
Label x=0.5 y=14.8 Label=Boron color=1  
Label x=0.2 y=19.4 Label=Phosphorus color=3
```

```
select z=doping  
print.1d layers
```

```
stop
```

```
end
```

APPENDIX II

```
$ JFET channel implantation

$ Full non-equilibrium point defect model
$(includes transient enhanced diffusion)
method pd.full

$ Graphics written as postscript file
option device="c/postscript" plot.out="jfetn.ps"

$set the grid spacing
mesh dy.surf=0.002

$ Set the well background doping
initialize boron=1e15

implant phosphorus dose=3e12 energy=110

$ Plot the as-implanted phosphorus distribution
select z=log10(phosphorus) title="JFET channel implant"
plot.1d top=19 bottom=14 right=0.22 color=3
select z=log10(boron)
plot.1d ^ax ^cl color=1

$pad oxide
deposit oxide thick=0.05

$drive-in
diffusion temp=1030 time=300

$ remove oxide
Etch oxide

$ Plot the phosphorus distribution
select z=log10(phosphorus)
plot.1d ^ax ^cl color=3

$ Label the plot
Label x=0.5 y=14.9 Label=Boron color=1
Label x=0.05 y=16.5 Label=Phosphorus color=3

select z=doping
```

```

print.1d layers
stop
end

$ JFET Gate Boron implantation

$ Full non-equilibrium point defect model
$(includes transient enhanced diffusion)
method pd.full

$ Graphics written as postscript file
option device="c/postscript" plot.out="jfetp.ps"

$set the grid spacing
mesh dy.surf=0.002

$ Set the well background doping
initialize boron=1e15

implant boron dose=5e12 energy=40

$ Plot the as-implanted phosphorus distribution
select z=log10(boron) title="JFET gate implant"
plot.1d top=19 bottom=14 right=0.22 color=2
select z=log10(boron)
plot.1d ^ax ^cl color=1

$pad oxide
deposit oxide thick=0.05

$drive-in
diffusion temp=1030 time=300

$ remove oxide
Etch oxide

$ Plot the phosphorus distribution
select z=log10(boron)
plot.1d ^ax ^cl color=2

$ Label the plot
Label x=0.5 y=14.9 Label=Boron color=1
Label x=0.1 y=16.8 Label=boron color=2

select z=doping

```

print.1d layers

stop

end

APPENDIX III

ITLE Avant! MEDICI Example 2 - Lateral NPN Transistor Simulation
COMMENT Grid Generation and Initial Biasing

COMMENT Specify a rectangular mesh
MESH
X.MESH WIDTH=55 H1=1.0
Y.MESH Y.MIN=-0.2 Y.MAX=0.0 N.SPACES=2
Y.MESH DEPTH=0.22 H1=0.04
Y.MESH DEPTH=700.0 H1=14

COMMENT Region definition
REGION NAME=Silicon SILICON
REGION NAME=Oxide OXIDE Y.MIN=-0.2 Y.MAX=0
REGION NAME=Oxide OXIDE Y.MIN=0.22 Y.MAX=2.22

COMMENT Electrodes

ELECTR MAJORITY NAME=Base X.MIN=20 X.MAX=22 Y.MAX=0
ELECTR MAJORITY NAME=Base X.MIN=34 X.MAX=36 Y.MAX=0

ELECTR MAJORITY NAME=Base X.MIN=4 X.MAX=6 Y.MAX=0
ELECTR MAJORITY NAME=Base X.MIN=50 X.MAX=52 Y.MAX=0

ELECTR NAME=Emitter X.MIN=26 X.MAX=28 Y.MAX=0
ELECTR NAME=Collector X.MIN=12 X.MAX=14 Y.MAX=0
ELECTR NAME=Collector X.MIN=40 X.MAX=42 Y.MAX=0
COMMENT ELECTR NAME=Substrate BOTTOM

COMMENT Specify impurity profiles

PROFILE P-TYPE N.PEAK=1E15 UNIFORM OUT.FILE=LBJT21DS

COMMENT Base and contact regions
PROFILE P-TYPE N.PEAK=1e17 Y.MIN=0.0 Y.MAX=0.22 Y.CHAR=0.01
+ X.MIN=18 WIDTH=6 XY.RAT=0.75

PROFILE P-TYPE N.PEAK=1e21 Y.MIN=0.0 Y.CHAR=0.02
+ X.MIN=20 WIDTH=2 XY.RAT=0.75

PROFILE P-TYPE N.PEAK=1e17 Y.MIN=0.0 Y.MAX=0.22 Y.CHAR=0.01
+ X.MIN=32 WIDTH=6 XY.RAT=0.75

```

PROFILE P-TYPE N.PEAK=1e21 Y.MIN=0.0 Y.CHAR=0.02
+
X.MIN=34 WIDTH=2 XY.RAT=0.75

PROFILE P-TYPE N.PEAK=1e17 Y.MIN=0.0 Y.MAX=0.1 Y.CHAR=0.01
+
X.MIN=0 WIDTH=10 XY.RAT=0.75

PROFILE P-TYPE N.PEAK=1e21 Y.MIN=0.0 Y.CHAR=0.02
+
X.MIN=4 WIDTH=2 XY.RAT=0.75

PROFILE P-TYPE N.PEAK=1e17 Y.MIN=0.0 Y.MAX=0.1 Y.CHAR=0.01
+
X.MIN=46 WIDTH=9 XY.RAT=0.75

PROFILE P-TYPE N.PEAK=1e21 Y.MIN=0.0 Y.CHAR=0.02
+
X.MIN=50 WIDTH=2 XY.RAT=0.75

COMMENT Emitter region
PROFILE N-TYPE N.PEAK=5e19 Y.MIN=0.0 Y.MAX=0.22 Y.CHAR=0.01
+
X.MIN=24 WIDTH=8 XY.RAT=0.75

COMMENT Collector and contact regions
PROFILE N-TYPE N.PEAK=7e16 Y.MIN=0.0 Y.MAX=0.22 Y.CHAR=0.01
+
X.MIN=10 WIDTH=8 XY.RAT=0.75

PROFILE N-TYPE N.PEAK=1e21 Y.MIN=0.0 Y.CHAR=0.01
+
X.MIN=12 WIDTH=2 XY.RAT=0.75

PROFILE N-TYPE N.PEAK=7e16 Y.MIN=0.0 Y.MAX=0.22 Y.CHAR=0.01
+
X.MIN=38 WIDTH=8 XY.RAT=0.75

PROFILE N-TYPE N.PEAK=1e21 Y.MIN=0.0 Y.CHAR=0.01
+
X.MIN=40 WIDTH=2 XY.RAT=0.75

PLOT.2D GRID TITLE="LBJT - Initial Grid" SCALE FILL

COMMENT Regrid on doping
REGRID DOPING LOG IGNORE=OXIDE
RATIO=2 SMOOTH=2 IN.FILE=LBJT21DS
PLOT.2D GRID TITLE="LBJT - 1st Doping Regrid" SCALE FILL
LABEL LABEL="Collector" X=8 Y=0.5
LABEL LABEL="Base" X=18 Y=0.5
LABEL LABEL="Emitter" X=25 Y=0.5 C.SI=0.2
LABEL LABEL="Base" X=35 Y=0.5
LABEL LABEL="Collector" X=40 Y=0.5

REGRID DOPING LOG IGNORE=OXIDE
RATIO=2 SMOOTH=2 IN.FILE=LBJT21DS

```

```
PLOT.2D GRID TITLE="LBJT - 2nd Doping Regrid" SCALE FILL  
COMMENT Extra regrid in emitter-base junction region only.  
  
REGRID DOPING LOG IGNORE=OXIDE RATIO=2 SMOOTH=2  
IN.FILE=LBJT21DS  
+ Y.MIN=0.0 Y.MAX=0.22 X.MAX=55 OUT.FILE=LBJT21MS  
PLOT.2D GRID TITLE="LBJT - 3rd Doping Regrid" SCALE FILL
```

```
COMMENT Modify properties of emitter region  
MOBILITY SILICON CONC=5E19 HOLE=2.3 FIRST LAST  
MATERIAL SILICON TAUN0=5E-7
```

```
INTERFACE REGION=(Silicon,Oxide) S.N=1E2 S.P=1E2
```

```
COMMENT Define models  
MODELS CONMOB CONSRH AUGER BGN FLDMOB PRPMOB
```

```
COMMENT Solve for Vce=3 volts  
SYMB CARRIERS=0  
METHOD ICCG DAMPED  
SOLVE V(Collector)=3.0
```

```
COMMENT Switch to Newton and two carriers - save solution  
SYMB NEWTON CARRIERS=2  
SOLVE OUT.FILE=LBJT21S
```

Lbjt21f.inp

```
TITLE Avant! MEDICI Example 2 - NPN Transistor Simulation  
COMMENT Forward Bias Points
```

```
COMMENT Read in simulation mesh  
MESH IN.FILE=LBJT21MS
```

```
COMMENT Load previous solution: Vce=3.0 Vbe=0.0  
LOAD IN.FILE=LBJT21S
```

```
COMMENT Use Newton's method with 2 carriers  
SYMB NEWTON CARRIERS=2
```

```
COMMENT Setup log file for I-V and AC data  
LOG OUT.FILE=LBJT21FI
```

```

COMMENT Forward bias the base-emitter junction and
$      calculate the admittance matrix at 1.0 MHz

SOLVE V(Base)=0.2 ELEC=Base VSTEP=0.1 NSTEP=4
+      AC.ANAL FREQ=1E6 TERM=Base
SOLVE V(Base)=0.7 ELEC=Base VSTEP=0.1 NSTEP=2
+      AC.ANAL FREQ=1E6 TERM=Base OUT.FILE=LBJT21S7

```

- lbjt21fp.inp

```

TITLE Avant! MEDICI Example 21FP - Lateral NPN Transistor Simulation
COMMENT Post-Processing of LBJT21F Results

```

```

COMMENT Plot Ic and Ib vs. Vbe
PLOT.1D IN.FILE=LBJT21FI Y.AXIS=I(Collector) X.AXIS=V(Base)
+      LINE=1 COLOR=2 TITLE="LBJT - Ic & Ib vs. Vbe"
+      Y.LOG POINTS BOT=1E-14 TOP=1E-3
PLOT.1D IN.FILE=LBJT21FI Y.AXIS=I(Base) X.AXIS=V(Base)
+      Y.LOG POINTS LINE=2 COLOR=3 UNCHANGE
LABEL  LABEL="Ic" X=.525 Y=5E-8
LABEL  LABEL="Ib" X=.550 Y=8E-10
LABEL  LABEL="Vce = 3.0v" X=.75 Y=1E-13

```

```

COMMENT Plot the current gain (Beta) vs. collector current
EXTRACT NAME=Beta EXPRESS=@I(Collector)/@I(Base)
PLOT.1D IN.FILE=LBJT21FI X.AXIS=I(Collector) Y.AXIS=Beta
+      TITLE="LBJT - Beta vs. Collector Current"
+      BOTTOM=0.0 TOP=50 LEFT=1E-14 RIGHT=1E-3
+      X.LOG POINTS COLOR=2
LABEL  LABEL="Vce = 3.0v" X=5E-14 Y=23

```

```

COMMENT Plot the cutoff frequency Ft=Gcb/(2*pi*Cbb)
EXTRACT NAME=Ft UNITS=Hz
+      EXPRESS="@G(Collector,Base)/(6.28*@C(Base,Base))"
PLOT.1D IN.FILE=LBJT21FI X.AXIS=I(Collector) Y.AXIS=Ft
+      TITLE="LBJT - Ft vs. Collector Current"
+      BOTTOM=1 TOP=1E10 LEFT=1E-14 RIGHT=1E-3
+      X.LOG Y.LOG POINTS COLOR=2
LABEL  LABEL="Vce = 3.0v" X=5E-14 Y=1E9

```

```

COMMENT Read in the simulation mesh and solution for Vbe=0.9v
MESH   IN.FILE=LBJT21MS

```

```

LOAD IN.FILE=LBJT21S9

COMMENT Vector plot of total current for Vbe=0.9v
PLOT.2D BOUND JUNC SCALE FILL
+ TITLE="LBJT - Total Current Vectors"
VECTOR J.TOTAL COLOR=2
LABEL LABEL="Vbe = 0.9v" X=0.4 Y=3
LABEL LABEL="Vce = 3.0v"

COMMENT Potential contour plot for Vbe=0.9v
PLOT.2D BOUND JUNC DEPL SCALE FILL
+ TITLE="LBJT - Potential Contours"
CONTOUR POTEN MIN=-1 MAX=4 DEL=.25 COLOR=6
LABEL LABEL="Collector" X=10 Y=0.5
LABEL LABEL="Base" X=20 Y=0.5
LABEL LABEL="Emitter" X=28 Y=0.5
LABEL LABEL="Base" X=36 Y=0.5
LABEL LABEL="Collector" X=42 Y=0.5
LABEL LABEL="Vbe=0.9V" X=0.5 Y=3
LABEL LABEL="Vbe=3.0V"

COMMENT Plot doping and carrier concentrations for Vbe=0.7v
LOAD IN.FILE=LBJT21S7

PLOT.1D DOPING Y.LOG SYMBOL=1 COLOR=2 LINE=1
+ BOT=1E10 TOP=1E20
+ X.STA=0 X.END=55 Y.STA=0 Y.END=0
+ TITLE="LBJT - Carrier & Impurity Conc."

PLOT.1D ELECTR Y.LOG SYMBOL=2 COLOR=3 LINE=2 UNCHANGE
+ X.STA=0 X.END=55 Y.STA=0 Y.END=0

PLOT.1D HOLES Y.LOG SYMBOL=3 COLOR=4 LINE=3 UNCHANGE
+ X.STA=0 X.END=55 Y.STA=0 Y.END=0

LABEL LABEL="Vbe = 0.7v" X=1.55 Y=5E19
LABEL LABEL="Vce = 3.0v"
LABEL LABEL="Doping" SYMBOL=1 COLOR=2
LABEL LABEL="Electrons" SYMBOL=2 COLOR=3
LABEL LABEL="Holes" SYMBOL=3 COLOR=4

```

APPENDIX IV

TITLE Avant! MEDICI Example 1 - N-Channel JFET

COMMENT Specify a rectangular mesh

```
MESH SMOOTH=1
X.MESH WIDTH=18 H1=0.36
COMMENT Y.MESH Y.MIN=-0.2 Y.MAX=0.0 N.SPACES=2
COMMENT Y.MESH DEPTH=0.22 H1=0.04
COMMENT Y.MESH DEPTH=7.0 H1=0.14
Y.MESH DEPTH=10.0 H1=0.2
```

COMMENT Region definition

```
REGION NAME=Silicon SILICON
COMMENT REGION NAME=Oxide OXIDE Y.MIN=-0.2 Y.MAX=0.0
COMMENT REGION NAME=Oxide OXIDE Y.MIN=0.22 Y.MAX=2.22
```

COMMENT Electrode definition

```
ELECTR NAME=Gate X.MIN=8.0 X.MAX=10.0 TOP
ELECTR NAME=Gate X.MIN=8.0 X.MAX=10.0 BOTTOM
ELECTR NAME=Drain X.MIN=0.0 X.MAX=2.0 TOP
ELECTR NAME=Source X.MIN=16.0 X.MAX=18.0 TOP
```

COMMENT Specify impurity profiles

PROFILE P-TYPE N.PEAK=1E15 UNIFORM OUT.FILE=JFET1DS

COMMENT gate regions

```
PROFILE P-TYPE N.PEAK=1e17 Y.MIN=0.0 Y.MAX=4.6 Y.CHAR=0.1
+ X.MIN=6.0 WIDTH=6.0 XY.RAT=0.75
```

```
PROFILE P-TYPE N.PEAK=1e21 Y.MIN=0.0 Y.MAX=0.1 Y.CHAR=0.1
+ X.MIN=8.0 WIDTH=2.0 XY.RAT=0.75
```

```
PROFILE P-TYPE N.PEAK=1e17 Y.MIN=5.4 Y.MAX=10.0 Y.CHAR=0.1
+ X.MIN=6.0 WIDTH=6.0 XY.RAT=0.75
```

```
PROFILE P-TYPE N.PEAK=1e21 Y.MIN=9.9 Y.MAX=10 Y.CHAR=0.1
+ X.MIN=8.0 WIDTH=2.0 XY.RAT=0.75
```

COMMENT Drain and source region

```
PROFILE N-TYPE N.PEAK=7e16 Y.MIN=4.6 Y.MAX=5.4 Y.CHAR=0.1
+           X.MIN=6.0 WIDTH=6.0 XY.RAT=0.75
```

```
PROFILE N-TYPE N.PEAK=7e16 Y.MIN=0.0 Y.MAX=10.0 Y.CHAR=0.1
+           X.MIN=0.0 WIDTH=6.0 XY.RAT=0.75
```

```
PROFILE N-TYPE N.PEAK=1e21 Y.MIN=0.0 Y.MAX=0.1 Y.CHAR=0.1
+           X.MIN=0.0 WIDTH=2.0 XY.RAT=0.75
```

```
PROFILE N-TYPE N.PEAK=7e16 Y.MIN=0.0 Y.MAX=10.0 Y.CHAR=0.1
+           X.MIN=12.0 WIDTH=6.0 XY.RAT=0.75
```

```
PROFILE N-TYPE N.PEAK=1e21 Y.MIN=0.0 Y.MAX=0.1 Y.CHAR=0.1
+           X.MIN=16.0 WIDTH=2.0 XY.RAT=0.75
```

COMMENT INTERFAC QF=1E10

PLOT.2D GRID TITLE="JFET - Initial Grid" FILL SCALE

COMMENT Regrid on doping

```
REGRID DOPING LOG RATIO=2 SMOOTH=1
+           IN.FILE=JFET1DS
```

PLOT.2D GRID TITLE="JFET- Doping Regrid" FILL SCALE

COMMENT Specify contact parameters

COMMENT CONTACT NAME=Gate N.POLY

COMMENT Specify physical models to use

MODELS CONMOB FLDMOB SRFMOB2

COMMENT MODELS CONMOB CONSRH AUGER BGN FLDMOB PRPMOB

COMMENT Symbolic factorization, solve, regrid on potential

SYMB CARRIERS=0

METHOD ICCG DAMPED

SOLVE

```

REGRID POTEN RATIO=.2 MAX=1.0 Y.MAX=10.0 SMOOTH=1
+     IN.FILE=JFET1DS
+     OUT.FILE=JFET1MS
PLOT.2D GRID TITLE="JFET- Potential Regrid" FILL SCALE

COMMENT Solve using the refined grid, save solution for later use
SYMB   CARRIERS=0
SOLVE  OUT.FILE=JFET1S

COMMENT Impurity profile plots
PLOT.1D DOPING X.START=16.0 X.END=16.0 Y.START=0 Y.END=10.0
+     Y.LOG POINTS BOT=1E15 TOP=1E21 COLOR=2
+     TITLE="JFET - Source Impurity Profile"
PLOT.1D DOPING X.START=10.0 X.END=10.0 Y.START=0 Y.END=10.0
+     Y.LOG POINTS BOT=1E15 TOP=1E17 COLOR=2
+     TITLE="JFET - Gate Impurity Profile"
PLOT.2D BOUND TITLE="JFET - Impurity Contours" FILL SCALE
CONTOUR DOPING LOG MIN=16 MAX=20 DEL=.5 COLOR=2
CONTOUR DOPING LOG MIN=-16 MAX=-15 DEL=.5 COLOR=1 LINE=2

```

jfet1d.inp

```

TITLE Avant! MEDICI Example 1D - N-Channel JFET
COMMENT Calculate Drain Characteristics

```

```

COMMENT Read in simulation mesh
MESH   IN.FILE=JFET1MS

```

```

COMMENT Read in initial solution
LOAD   IN.FILE=JFET1S

```

```

COMMENT Use Newton's method and solve for electrons
SYMB   NEWTON CARRIERS=1 ELECTRON

```

```

COMMENT Setup log file for IV data
LOG    OUT.FILE=JFET1DI

```

```

SOLVE  V(Gate)=0 LOCAL
COMMENT Ramp the drain and gate
COMMENT SOLVE  V(Gate)=0.0 ELEC=Gate VSTEP=-1 NSTEP=5
SOLVE  V(Drain)=0.0 ELEC=Drain VSTEP=1.0 NSTEP=20

```

```
COMMENT Plot Ids vs. Vds
PLOT.1D Y.AXIS=I(Drain) X.AXIS=V(Drain) POINTS COLOR=2
+      TITLE="JFET - Drain Characteristics"
LABEL   LABEL="Vgs = V(Gate) v" X=10 Y=4E-4

COMMENT Potential contour plot using most recent solution
COMMENT PLOT.2D BOUND JUNC DEPL FILL SCALE
+      TITLE="JFET - Potential Contours"
COMMENT CONTOUR POTENTIA MIN=-1 MAX=10 DEL=.25 COLOR=6
COMMENT LABEL   LABEL="Vgs = -7 v" X=0.2 Y=1.6
COMMENT LABEL   LABEL="Vds = 20.0v"
```

APPENDIX V

CMOS transimpedance amplifier integrated with SOI waveguide Schottky photodetector process flow:

STARTING MATERIAL: SOITEC SOI 220 nm top Si, *p*-type doping $1\text{e}^{15}\text{ cm}^{-3}$, 3 μm buried oxide

1. SCREEN OXIDATION

Oxidation tube temperature 1000°C thickness 10 nm

2. BLANKET PHOSPHORUS IMPLANT

Approximately doping level $1\text{e}16\text{cm}^{-3}$ in Si film for Schottky diodes

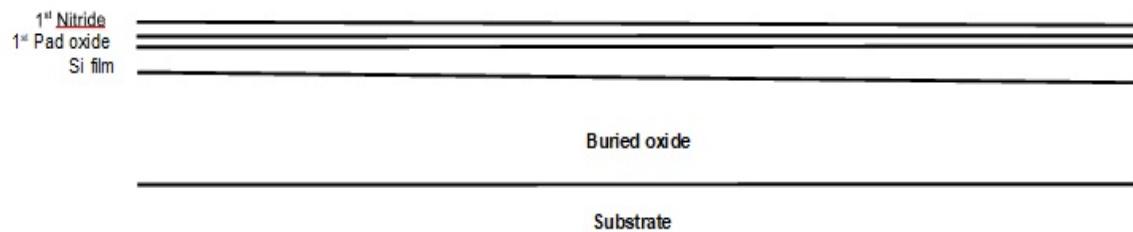
Implant 31P+ $4\text{e}11\text{cm}^{-2}$ 60keV

3. FIRST PAD OXIDATION and FIRST NITRIDE DEPOSITION

a) HF etch to hydrophobia (remove screen oxide)

b) 50 nm thermal pad oxide

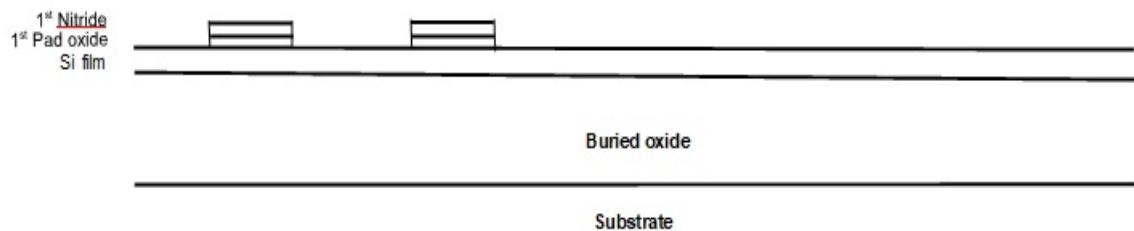
c) 80 nm nitride LPCVD



4. PATTERN RIB WAVEGUIDE

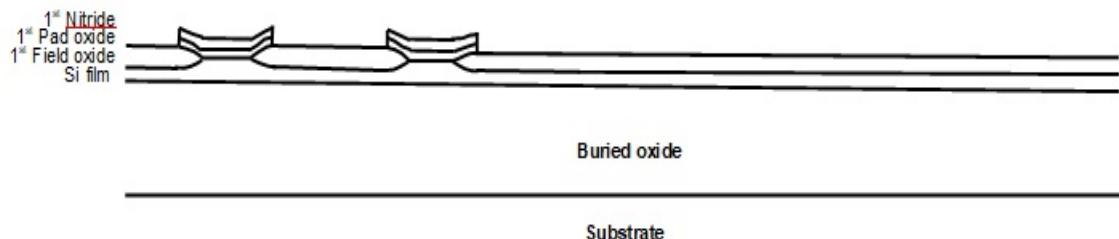
PE1

- a) Plasma etch nitride
- b) Remove pad oxide



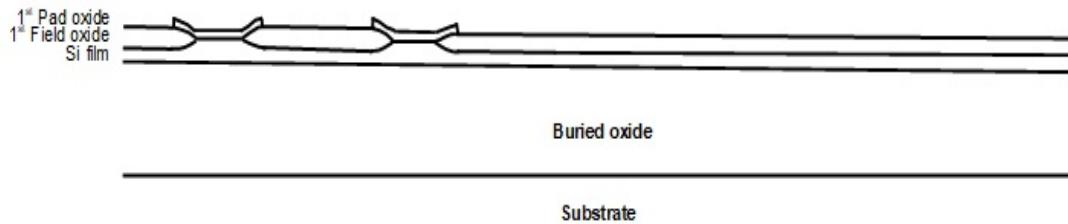
5. FIRST FIELD OXIDATION

Oxidation tube temperature 1000°C, grow 250 nm oxide, leave 100 nm Si film in the field



6. REMOVE NITRIDE

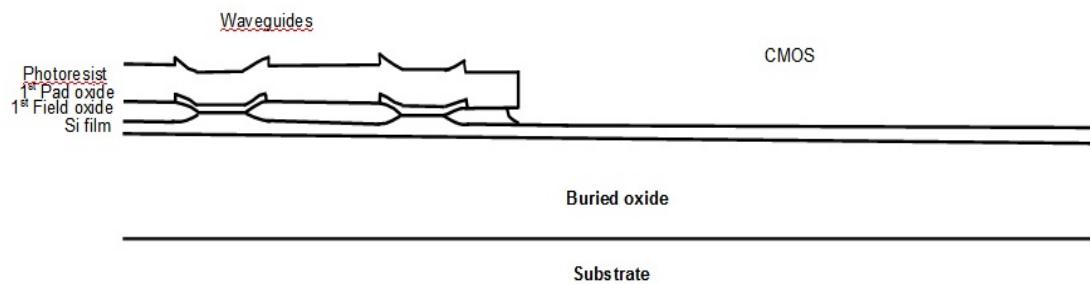
Leave pad oxide to provide some additional protection for waveguide ribs



7. REMOVE FIELD OXIDE in CMOS AREAS

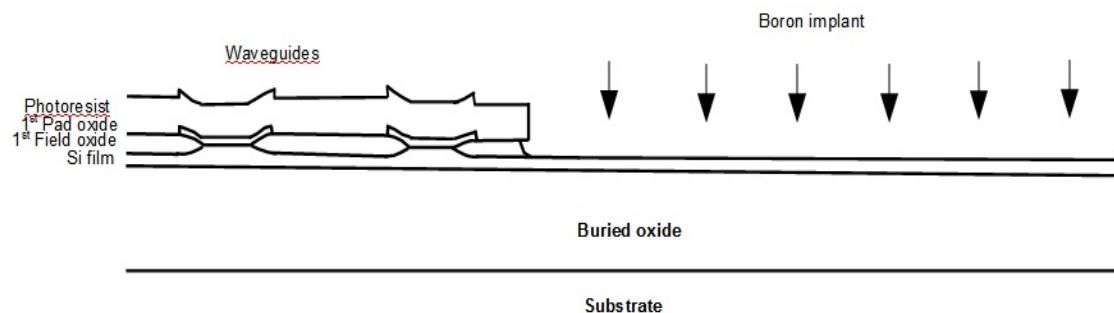
PE2

Etch in 10% buffered HF until field oxide removed in CMOS area



8. P-TYPE IMPLANT

Boron doping to $4 \times 10^{16} \text{ cm}^{-3}$ in CMOS regions (implant $11\text{B}+$ $1.4 \times 10^{12} \text{ cm}^{-2}$ 18keV), strip PR after implant



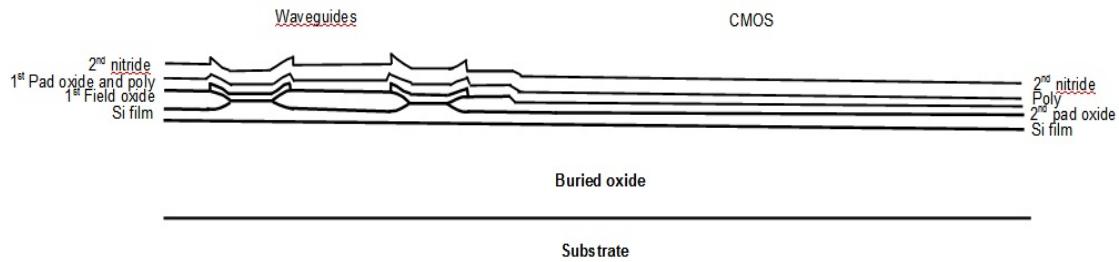
9. SECOND PAD OXIDE, DEPOSIT POLY BUFFER, DEPOSIT SECOND NITRIDE

Form buffered LOCOS (PBL) stack

20nm thermal pad oxide, tube temperature 1000°C

Deposit 25nm polysilicon

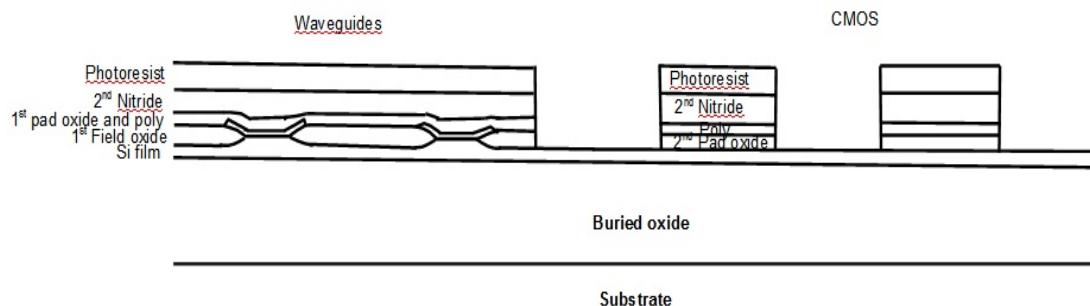
Deposit 150nm Si₃N₄



10. PATTERN DEVICE WELL PE3

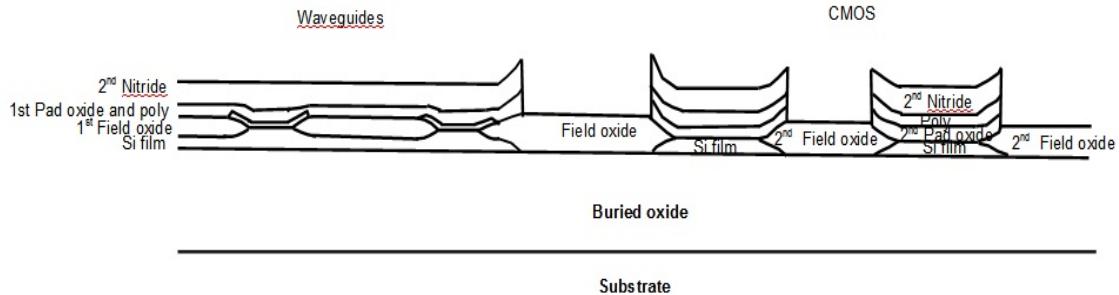
CF₄/O₂ plasma etch Si₃N₄ and Si

Buffered HF etch pad oxide

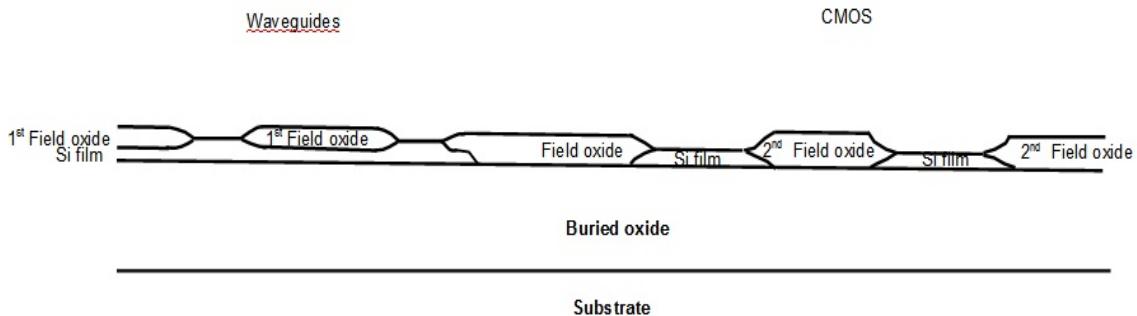


11. GROW 220 nm SECOND FIELD OXIDE

Completely consume 100 nm Si film in CMOS areas



12. STRIP PBL STACK



13. GROW 25nm GATE OXIDE

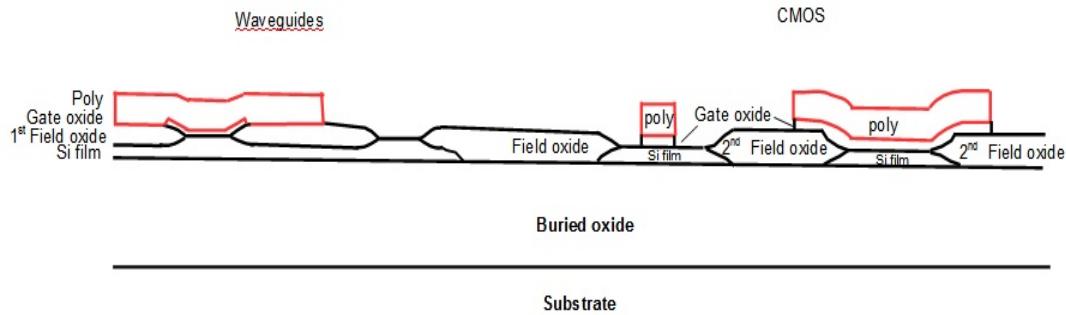
950°C dry O₂

14. DEPOSIT 350nm GATE POLYSILICON by LPCVD

15. PATTERN nMOS POLY GATES PE4

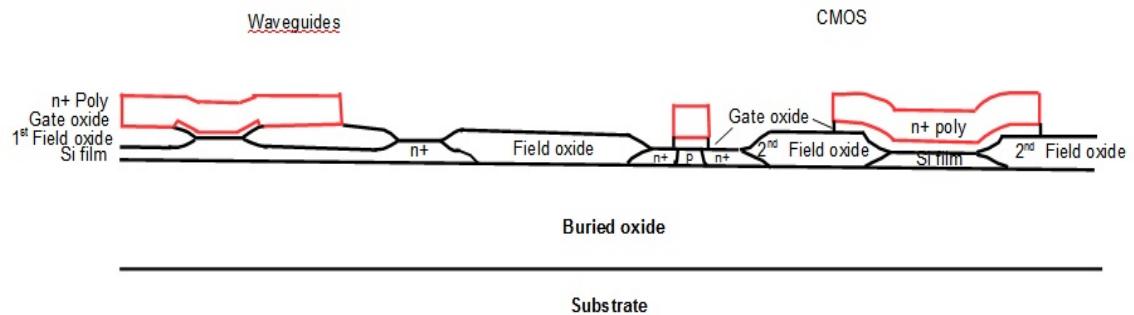
CF₄/O₂ plasma etch poly

Buffered HF etch gate oxide (keep pMOS regions covered)



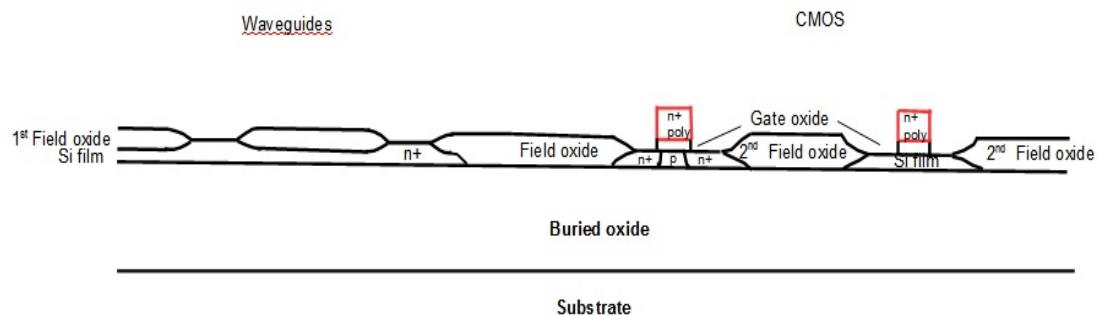
16. DOPE n+ REGIONS

Diffuse phosphorus 950°C 5min N2 + O2 + POCl3



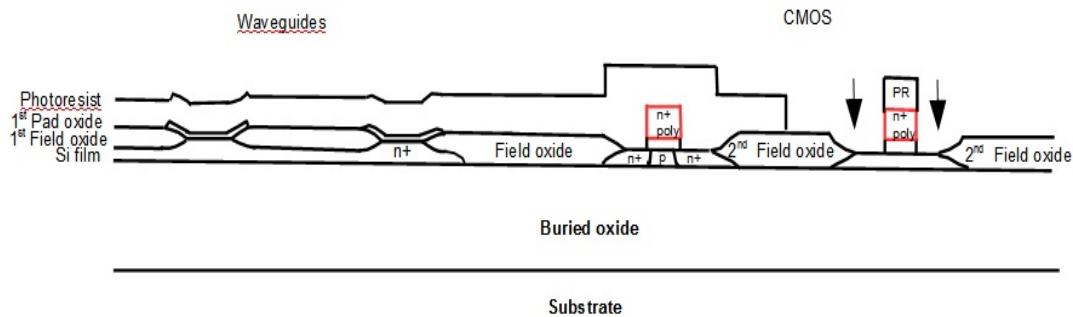
17. PATTERN pMOS POLY GATES PE5

Remove poly from waveguide region



18. DOPE p+ REGIONS PE6

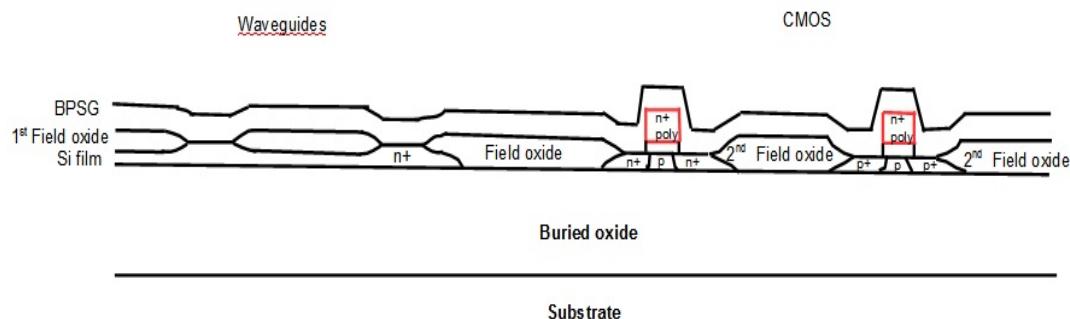
Implant 11B+ 11B+ 3X1015cm⁻² 15keV



19. DEPOSIT BPSG DIELECTRIC

100nm undoped oxide 500nm BPSG deposited by LPCVD

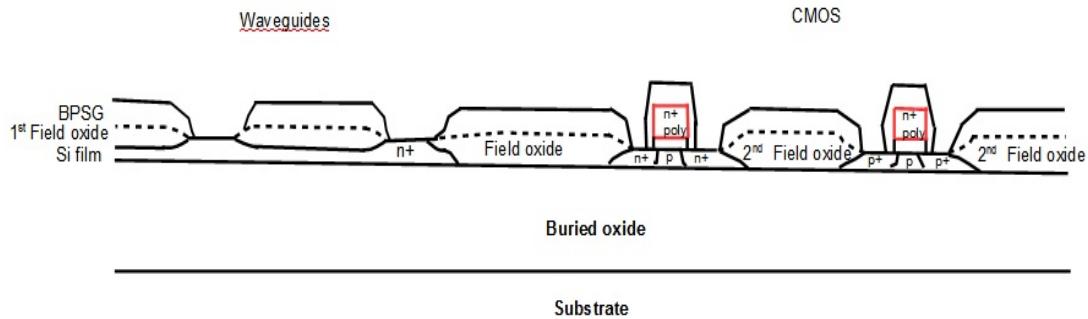
Flow BPSG 900°C 10 min (anneals p+ implant)



20. OPEN CONTACT WINDOWS

PE7

CHF₃ plasma etch BPSG



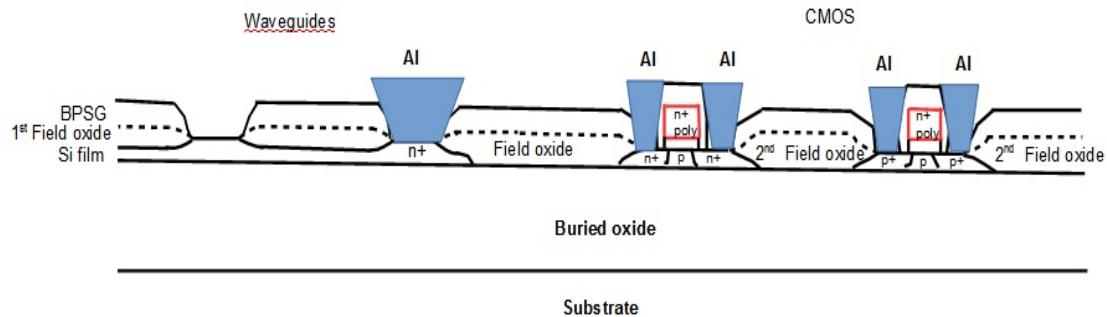
21. OHMIC METAL LIFT-OFF MASK PE 8

22. OHMIC METAL DEPOSITION

E-beam aluminum

Target thickness: 1.0 μm actual thickness:

23. OHMIC METAL LIFT-OFF



24. OHMIC METAL ANNEAL

Tube temperature: 400°C 10 min H₂

25. SCHOTTKY METAL LIFT-OFF MASK PE 9

26. SCHOTTKY METAL DEPOSITION

E-beam evaporation Ni or Pd

Target thickness: 20 nm

27. SCHOTTKY METAL LIFT-OFF

