INFORMATION TO USERS

This manuscript has been reproduced from the microfilm master. UMI films the text directly from the original or copy submitted. Thus, some thesis and dissertation copies are in typewriter face, while others may be from any type of computer printer.

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleedthrough, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send UMI a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, charts) are reproduced by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps. Each original is also photographed in one exposure and is included in reduced form at the back of the book.

Photographs included in the original manuscript have been reproduced xerographically in this copy. Higher quality 6" x 9" black and white photographic prints are available for any photographs or illustrations appearing in this copy for an additional charge. Contact UMI directly to order.

UMI

A Bell & Howell Information Company
300 North Zeeb Road, Ann Arbor MI 48106-1346 USA
313/761-4700 800/521-0600

NOTE TO USERS

The original manuscript received by UMI contains broken or light print. All efforts were made to acquire the highest quality manuscript from the author or school. Page(s) were microfilmed as received.

This reproduction is the best copy available

UMI

High-Efficiency Class E Amplifier Employing Silicon Carbide MESFETs

by

Reginald E. Grayston

A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of
Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada

© Reginald E. Grayston, 1998

National Library
of Canada

Acquisitions and
Bibliographic Services

395 Wellington Street
Ottawa ON K1A 0N4
Canada

Bibliothèque nationale
du Canada

Acquisitions et
services bibliographiques

395, rue Wellington
Ottawa ON K1A 0N4
Canada

Your file Votre référence

Our file Notre référence

The author has granted a non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of this thesis in microform, paper or electronic formats.

The author retains ownership of the copyright in this thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without the author's permission.

L'auteur a accordé une licence non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de cette thèse sous la forme de microfiche/film, de reproduction sur papier ou sur format électronique.

L'auteur conserve la propriété du droit d'auteur qui protège cette thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

0-612-32397-8

The undersigned recommend to the Faculty of Graduate Studies and
Research acceptance of this thesis

“High-Efficiency Class E Amplifier Employing Silicon Carbide MESFETs”

submitted by Reginald E. Grayston (BEng.)
in partial fulfillment of the requirements for
the degree of Master of Engineering

Thesis Supervisor
Dr. Miles Copeland

Chairman, Department of Electronics
Dr. Jim Wight

Carleton University

May 8, 1998

Abstract

This thesis reports on work that has been accomplished in the design, simulation and characterization of a high-efficiency power amplifier. The design is based on a combination of Class F and Class E power amplifier topologies utilizing silicon carbide MESFETs as the active devices. The hybrid amplifier design promises to provide approximately 1.1W of output power at 835MHz. The design procedure includes a derivation of the design equations for Class E amplifiers and provides a set of normalized design curves to assist designers in quickly obtaining amplifier parameters for an initial design. Issues relating to the impact of parasitics on high-efficiency amplifiers operating at high frequencies are addressed. In addition, comments on the suitability of silicon carbide for use in high-efficiency amplifiers are provided.

Acknowledgments

As is common with acknowledgments for such a project, there are too many to thank and too little space in which to do it.

First and foremost, I would like to express my appreciation and gratitude to my supervisor Dr. Miles Copeland. Without your patient mentoring and guidance this project would not have been nearly as rewarding. You taught me the value of intuition in circuit design and I only hope that someday I can make it look as easy as you do. Thanks Miles!

I also owe a debt of gratitude to Nortel and in particular to the Technology Access and Applications Group headed by Robert Hadaway. In addition to providing funding for this research, fabrication services, and test facilities, the group provided me with the opportunity to work with some of the most talented engineers and scientists. My thanks go out to all of you in 5C60, but especially to Peter Schvan, Tom MacElwee, Sorin Voinigescu and Mike Maliepaard. Working with all of you made this a worthwhile endeavour. In addition, the support of the Advanced Packaging Group and in particular the assistance of Brian Gunsekera were vital to the timely completion of this project.

Thanks also must go out to the members of the radio group in Carleton's Electronics department. Without the support of people like; Leonard Daupinee, Jose Macedo, and Walt Bax this project would have been much more difficult and much less enjoyable. Thanks to all of you for making this a memorable experience.

And finally, thanks to my wife Andrea and my son Alexander. The journey we agreed to take some seven years ago has now finally come to an end. Without your unquestionable love and support the journey would have been without meaning. It is to you both that I dedicate this work.

Per Ardua Ad Astra

Table of Contents

<i>Abstract</i>	<i>iii</i>
<i>Acknowledgments</i>	<i>iv</i>
<i>List of Tables</i>	<i>viii</i>
<i>List of Figures</i>	<i>ix</i>
<i>List of Symbols & Abbreviations</i>	<i>xi</i>
CHAPTER 1 <i>Introduction</i>	<i>12</i>
1.1 Motivation	12
1.2 Thesis Goals & Objectives	15
1.3 Thesis Organization	17
CHAPTER 2 <i>Power Amplifier Fundamentals</i>	<i>19</i>
2.1 Introduction	19
2.2 Class A Power Amplification	20
2.3 Class B Power Amplification	26
2.3.1 Crossover Distortion and Class AB Operation	29
2.4 Class C Amplification	32
2.5 Class F Amplification	37
2.6 Class D Amplification	42
2.7 Class E Amplification	44
2.8 Why Choose Class E Amplification?	48
CHAPTER 3 <i>Technology and Active Device Selection</i>	<i>49</i>
3.1 Technology Issues in Power Amplifier Design	49
3.2 Metallization Properties	50
3.2.1 On-Chip Filtering Issues	50
3.3 Device Breakdown Voltages	51
3.4 Current Handling Capability	52
3.5 Properties of Silicon Carbide (SiC)	53
3.6 Structure of the SiC MESFET	56
3.7 Current Status of Silicon Carbide Technology	57
3.8 Research Project Limitations Resulting from SiC	58

CHAPTER 4	<i>Design Methodology for a Class E Switching Power Amplifier</i>	60
	4.1 Introduction.	60
	4.2 Derivation of the Ideal Class E Design Equations	62
	4.3 Normalization of the Design Equations.	70
	4.4 Issues Affecting the Validity of the Ideal Class E Analysis	86
	4.5 Design Example: Ideal Class E Amplifier	87
	4.5.1 Impact of Load Quality Factor (QL) on Amplifier Performance	89
	4.5.2 Impact of Drive Waveform Transition Times on Amplifier Performance	91
 CHAPTER 5	 <i>Design Methodology for the Class F Driver Amplifier</i> . .	 93
	5.1 Introduction.	93
	5.2 Design of a Square Wave Generating Class F Amplifier	97
	5.3 Difficulties Driving Non-Linear Capacitances With the Class F Amplifier	103
 CHAPTER 6	 <i>Design, Simulation and Measurement of the Class E & F Amplifier Stages</i>	 105
	6.1 Introduction.	105
	6.2 Active Device and Substrate Properties	105
	6.2.1 Silicon Carbide MESFET Characteristics	106
	6.2.2 TMM3 Board / Substrate Properties	107
	6.3 Class E Amplifier Design	110
	6.3.3 Amplifier Specifications	110
	6.3.4 Supply Voltage Determination	111
	6.3.5 Active Device Sizing	111
	6.3.6 Component Value Determination	112
	6.4 Simulation of the Class E Design	114
	6.5 Class F Stage Design	116
	6.5.7 Characteristics of the Drive Waveform for the SiC Based Class E Design	117
	6.6 Design of the Class F Stage	118
	6.7 Parasitic Calculations	122
	6.8 Board Level Design Issues	126
	6.9 Measured Amplifier Performance.	129

CHAPTER 7	<i>Recommendations & Conclusions</i>	134
	7.1 Summary	134
	7.2 Conclusions	135
	7.3 Recommendations for Future Work	138
	<i>References</i>	139
Appendix A	Normalized Class E Design Curves	143

List of Tables

TABLE 1-1	Common Wireless Communication Standards	13
TABLE 1-2	Spectral Efficiency of Various Modulation Schemes [Mundr93]	14
TABLE 2-1	Amplifier Class Characteristics	48
TABLE 3-1	Material Properties Comparison : SiC to Common Semiconductors [Neude85] [MacEl97]	53
TABLE 3-2	Modelled Power Densities for Various Technologies [Wietz95]	57
TABLE 4-1	Design Values for $k=1.412$	88
TABLE 4-2	Impact of Loaded Q on Ideal Class E Amplifier	89
TABLE 5-1	Harmonic Generation in a Square Law Device	98
TABLE 6-1	TMM3 Substrate Material Properties [Best97]	107
TABLE 6-2	Class E Design Values @ $k=1.412$	110
TABLE 6-3	Component Values for Class E Amplifier	112
TABLE 6-4	Class E Amplifier Performance	116
TABLE 6-5	Class E/F Amplifier Performance	121
TABLE 6-6	Class E/F Amplifier Performance with Parasitics	125
TABLE 6-7	DC Bias Measurements	129
TABLE 6-8	Amplifier #2 RF Data	130
TABLE 6-9	Amplifier #3 RF Data	131

List of Figures

FIGURE 1-1	Power Amplifier Topology Suitable for All Modulation Schemes	15
FIGURE 2-1	Class A Power Amplifier	21
FIGURE 2-2	Typical I-V Characteristics Illustrating Class A Load Line	23
FIGURE 2-3	f_T Plot for a Typical Device	24
FIGURE 2-4	Class A Operation: Bias Point and Time Domain Waveforms	25
FIGURE 2-5	Class B Amplifier Topology	26
FIGURE 2-6	Class B Amplifier Waveforms	27
FIGURE 2-7	Crossover Distortion in Class B Amplifiers (not to scale)	30
FIGURE 2-8	Bias Operating Points: Class A, B, AB and C	31
FIGURE 2-9	Class C Amplifier Topology	32
FIGURE 2-10	Class C Amplifier Waveforms	33
FIGURE 2-11	Efficiency as a Function of Conduction Angle (2ϕ)	35
FIGURE 2-12	Class F Amplifier Schematic	37
FIGURE 2-13	Class F Amplifier Waveforms (Fundamental and 3RD Harmonic Only)	38
FIGURE 2-14	Harmonic Components for Maximally Flat Drain Voltage Waveform	39
FIGURE 2-15	Transmission Line Tuned Class F Amplifier	40
FIGURE 2-16	Typical Waveforms : Transmission Line Tuned Class F Amplifier	42
FIGURE 2-17	Class D Amplifier: Voltage-Switching Version	43
FIGURE 2-18	Class E Amplifier Topology	44
FIGURE 2-19	Typical Class E Waveforms	45
FIGURE 2-20	Class E Amplifier Equivalent Circuit	46
FIGURE 3-1	Physical Structure of a Silicon Carbide MESFET	56
FIGURE 4-1	Basic Class E Amplifier (RFC in DC Supply Line)	61
FIGURE 4-2	Class E Amplifier Equivalent Circuit ($LDC < LRFC$)	62
FIGURE 4-3	Ideal Class E Amplifier Waveforms Showing Input Drive	63
FIGURE 4-4	Φ as a Function of Resonance Ratio (k)	71
FIGURE 4-5	$B \cdot RL$ as a Function of Resonance Ratio (k)	72
FIGURE 4-6	P_o as a Function of Resonance Ratio (k)	73
FIGURE 4-7	XDC/RL as a Function of Resonance Ratio (k)	74
FIGURE 4-8	Peak V_o as a Function of Resonance Ratio (k)	75
FIGURE 4-9	$IL\theta_1$ as a Function of Resonance Ratio (k)	76
FIGURE 4-10	IDC as a Function of Resonance Ratio (k)	77
FIGURE 4-11	$V_{SF}(k)$ as a Function of θ for $k=[0.5, 1.1, 1.4, 1.7]$	78
FIGURE 4-12	$ILF(k)$ as a Function of θ for $k=[0.5, 1.1, 1.4, 1.7]$	80
FIGURE 4-13	$IOF(k)$ as a Function of θ for $k=[0.5, 1.1, 1.4, 1.7]$	82
FIGURE 4-14	$ISF(k)$ as a Function of θ for $k=[0.5, 1.1, 1.4, 1.7]$	83

List of Figures

FIGURE 4-15	ICF(k) as a Function of theta for $k=[0.5, 1.1, 1.4, 1.7]$	84
FIGURE 4-16	XF(k) as a Function of Resonance Ratio (k)	85
FIGURE 4-17	Impact of Loaded Q on the Class E Amplifier	90
FIGURE 4-18	Impact of Drive Waveform Transition Times on the Class E Amplifier	91
FIGURE 5-1	Class F Amplifier: Standard Topology	93
FIGURE 5-2	Class F Amplifier Typical Waveforms	94
FIGURE 5-3	Class F Amplifier Topology for Square Wave Generation	95
FIGURE 5-4	Generation of a Square Wave Through Diode Clipping	96
FIGURE 5-5	Square Wave Class F Driving a Resistive Load	99
FIGURE 5-6	Simulated Square Wave Class F Waveforms	101
FIGURE 5-7	Load Impedance Seen by the Class F Amplifier	102
FIGURE 6-1	IV Characteristics for a 1X250 SiC MESFET	106
FIGURE 6-2	Attachment of SiC Transistor Die to TMM3 Substrate	108
FIGURE 6-3	Initial Class E Design Without Parasitics	114
FIGURE 6-4	Class E Amplifier Without Parasitics	115
FIGURE 6-5	Amplifier Incorporating Class F Driver	119
FIGURE 6-6	Simulated Results for the Amplifier with Class F Incorporated ..	120
FIGURE 6-7	Completed Class F/ Class E Amplifier Incorporating Parasitics ..	124
FIGURE 6-8	Simulated Amplifier Performance @ 824, 835 and 849MHz	126
FIGURE 6-9	High-Efficiency Amplifier Layout Versions 1 and 2	127
FIGURE 6-10	Amplifier Test Measurement Setup	129
FIGURE 6-11	Amplifier #2 Output Power	131
FIGURE 6-12	Amplifier # 3 Output Power	132

List of Symbols & Abbreviations

BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
DC	Direct Current
DECT	Digital European Cordless Telephone
DQPSK	Doppler shifted Quadrature Phase Shift Keying
DSP	Digital Signal Processing
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
GSM	Groupe Special Mobile
HEPA	High Efficiency Power Amplifier
IMD	Intermodulation Distortion
JDC	Japanese Digital Cellular
JPHP	Japanese Personal Handi-Phone
MESFET	Metal Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTBF	Mean Time Between Failures
NADC	North American Digital Cellular
PA	Power Amplifier
PAE	Power Added Efficiency
PLL	Phase Locked Loop
PCN	Personal Communication Network
PCS	Personal Communications System
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RFC	Radio Frequency Choke
SNR	Signal to Noise Ratio
TF	Transfer Function
WLAN	Wideband Local Area Network
UGBW	Unity-Gain Bandwidth
VCO	Voltage Controlled Oscillator

1.1 Motivation

The past few years have seen a phenomenal growth in the quantity and quality of personal communications devices entering the marketplace. The consumers of these new devices are extremely demanding. Common consumer demands are “dual mode phones” (digital cellular units capable of operating on the older analog system as a backup), smaller, lighter handsets, and increased “talk time”. All of these “specifications” must be met with essentially no increase in unit cost (from the consumers point of view) - an extremely difficult design task. From the service provider perspective, the cellular system must efficiently utilize the available spectral bandwidth and minimize power requirements to reduce cost. In both handheld and base-station applications one module is responsible for a large portion of the power consumption - the power amplifier. In general, the higher the output power of the transmitter, the higher the power amplifier consumption as a percentage of the total.

The efficiency of the power amplifier has a direct impact on the cost of the wireless communication system. Increasing the efficiency of the power amplifier in a handheld transmitter results in reduced DC power drain on the batteries, reduced handset weight resulting from reduced heat sinking requirements, and increased reliability due to reduced junction operating temperatures.

In a base-station application, increased efficiency results in benefits similar to those accrued to handsets using efficient power amplifiers. In addition, the reduction in input power (considering the large output powers required) significantly reduces the cost of amplification. As a result, efficient power amplification is highly desirable regardless of the final application. In this regard the quest for higher efficiency power amplifiers continues.

As with most engineering designs, efficient power amplification cannot be achieved without cost. The designer, in his quest for efficiency, must trade off linearity (another desirable quality of a power amplifier). The difficulty in trading linearity for efficiency manifests itself in the limited applicability of highly efficient amplification to a few (spectrally inefficient) modulation schemes. The data in Table 1-1 illustrates the bandwidth, modulation scheme and amplification requirements for some common wireless standards.

TABLE 1-1 Common Wireless Communication Standards

Standard	Frequency Band GHz	Modulation	Envelope	Amplification
NADC	0.824-0.849	$\pi/4$ -DQPSK	Variable	Linear
GSM	0.890-0.915	GMSK	Constant	Nonlinear
DECT	1.88-1.898	GFSK	Constant	Nonlinear
JPHP	1.895-1.918	$\pi/4$ -DQPSK	Variable	Linear
WLAN	2.4	QPSK	Constant	Nonlinear

Modulation schemes having variable signal envelopes (e.g. $\pi/4$ -DQPSK) must be amplified using linear methods, as the application of the time varying envelope to a nonlinear amplifier results in generation of extraneous sidebands due to AM to PM conversion in the varactor capacitances of the active devices. These sidebands deprive the information signal of some of its power and result in adjacent channel interference [Sklar88]. Of the modulation schemes in Table 1-1, those exhibiting constant envelopes (GMSK, GFSK) can be amplified using efficient, nonlinear power amplifiers. It should

be noted; however, that all the modulation schemes in Table 1-1 exhibit some amplitude variation as filtering of a modulated carrier (band limiting) results in some envelope ripple.

While the variable envelope modulation schemes require linear (more costly) amplification, they have higher spectral efficiency than the continuous phase modulation methods (GMSK). Spectral efficiency is defined as the number of bits transmitted per Hertz of bandwidth per second. With the electromagnetic spectrum becoming more congested, the use of spectrally efficiency modulation and coding schemes is a necessity. Table 1-2 provides data on the spectral efficiency of common wireless modulation schemes.

TABLE 1-2 Spectral Efficiency of Various Modulation Schemes [Mundr93]

System	Modulation	Channel BW kHz	Data Rate kbps	Spectral Efficiency b/Hz/s
JDC	$\pi/4$ -DQPSK	25	42	1.68
NADC	$\pi/4$ -DQPSK	30	48.6	1.62
GSM	GMSK	200	270.8	1.35
DECT	GMSK	1728	1572	0.67

The ideal power amplifier topology would be one which is capable of efficiently amplifying both constant envelope signals and those signals having variable envelopes. Sowlati [Sowla96] has proposed using a phase linearizing loop to accomplish this goal. A more general method for implementing an amplifier capable of efficient operation with all types of modulation is through inclusion of the amplifier (HEPA in Figure 1-1) in a phase locked loop (PLL) consisting of a low pass loop filter, a voltage controlled oscillator (VCO) and a dual modulus divider. The main reason for including the PA in the phase locked loop is to allow the loop feedback to compensate for any AM to PM conversion created as a result of using a non-linear (efficient) amplification scheme. For loop operation with non-constant envelope modulation schemes such as $\pi/4$ -DQPSK, the digital signal processing block (DSP) separates the amplitude and phase modulated

components of the information signal. The non-linear Class E amplifier amplifies the phase/frequency modulation efficiently and then the amplitude variations are applied through modulation of the power supply of the Class E stage. The linear relationship between V_o and V_{DD} prevents conversion of AM to PM within the amplifier.

FIGURE 1-1 Power Amplifier Topology Suitable for All Modulation Schemes

For use in a constant amplitude (continuous phase modulation, GMSK) modulation scheme, the amplitude information would be essentially constant and $A(t)$ in the figure would be constant. In reality, due to band limiting and filtering of the modulated carrier, some ripple would be present in the amplitude information and $A(t)$ would provide this ripple modulation of the supply voltage.

1.2 Thesis Goals & Objectives

As previously mentioned the ideal power amplifier topology would be one suitable for efficient amplification of signals modulated with either constant or variable envelopes. While the implementation of such a power amplifier incorporated within a PLL is beyond

the scope of this research project, the implementation of such an amplifier topology is viewed as a future goal.

The purpose of this thesis work is to evaluate, design and fabricate a high-efficiency power amplifier operating in the 824-849 MHz band of frequencies. As it is not the intention of this research to design and build the entire PLL linearization loop, the isolated amplifier's purpose is twofold. First, to provide experience in the design of high efficiency power amplifiers. In this regard, the design process for high-efficiency amplifier design is detailed. Secondly, the design of the amplifier is based on high-voltage, high-power silicon carbide Metal Semiconductor Field Effect Devices (MESFETs) in order to evaluate the potential of this interesting technology for use in high-efficiency power amplifiers.

As silicon carbide (SiC) is a high-power technology which is relatively immature (compared with Silicon or GaAs) certain limitations with respect to the design result. The first is that due to the supply voltages required, amplifiers designed in the SiC technology would not be suitable for handset use. Due to its high-power capability SiC is more suitably employed in the base-station arena.

In addition, the devices used in this research are provided by a third-party vendor for experimental (measurement and modeling) activities. As such a fully integrated version of the amplifier is not possible. In this regard, a hybrid design approach is used in this thesis utilizing individual transistor die and surface mount components. This results in a much lower output power than a typical base-station application would require. The amplifier however provides a test vehicle to refine the high-efficiency design methods and to evaluate the technology for use in high-efficiency amplifiers. The design approach used also is aimed at making the amplifier suitable for applications involving envelope modulation, such as NADC signals, when its power supply is modulated.

To summarize the main goals of this research are to:

1. refine the design procedure for Class E high-efficiency power amplifiers,
2. design a high-efficiency Class E / Class F power amplifier operating in the 824-849 MHz band capable of providing 1-3 Watts of output power into a 50 Ω load without resorting to power combining techniques,
3. evaluate the suitability of these amplifier classes for use in the RF regime, and
4. evaluate the suitability of silicon carbide MESFET devices for use in Class E and Class F amplifier topologies for use in wireless (base-station) applications.

1.3 Thesis Organization

Chapter 2 describes the background material which forms the foundation for this research work. A brief description of the operating principles and performance of the variety of power amplifier classes will be provided. Examination of the applicability of each amplifier topology for use in the various communication standards will also be provided. From this information one is able to select a suitable power amplifier topology/class for a given modulation scheme.

As the fabrication technology and active devices themselves are fundamental determinants of amplifier performance, Chapter 3 examines these issues in power amplifier design.

The design methodology for a highly efficient Class E switching power amplifier is presented in Chapter 4. The design difficulties are examined and solutions are proposed to ensure the efficiency of the amplifier is maintained at a high level.

Chapter 5 examines the design issues resulting from attempting to operate Class E amplifiers at RF frequencies. In this regard, the design methodology for a Class F 'harmonic tuned' amplifier is examined.

Chapter 6 details the design of the high efficiency power amplifier. The design and optimization of the Class E output stage is examined first. The Class F driver amplifier is then detailed and examined. Details of the hybrid implementation of the highly efficient power amplification are examined including surface mount component selection and board level design issues. Measured performance of the amplifier is provided and compared with simulation.

Finally, conclusions arising from this work and recommendations for additional research into high efficiency power amplification is provided in Chapter 7.

2.1 Introduction

The power amplifier is the final stage of amplification in the transmission path for all wireless communication systems. Its task is to amplify the modulated carrier signal to allow signal propagation over “long” distances. “Long” in this context is relative and is determined by the communication system standards being considered. Cordless telephony standards for example require much shorter propagation ranges (and thus lower output powers) than do cellular systems.

The power amplifier (PA) must perform its function without introducing significant distortion into the transmitted signal. Being the final stage in the transmitter path, the power amplifier is subjected to large input signal levels and as a result of (inherent) device nonlinearities is capable of generating large amounts of distortion. This distortion manifests itself in the form of harmonics or intermodulation distortion (IMD). Intermodulation occurs when multiple signals are applied to a nonlinear element and mixing products are generated. Different power amplifier topologies vary in the amount of distortion that is produced. In addition, different modulation schemes can tolerate different amounts of distortion. Therefore the choice of amplifier topology must be made based on the type of modulation used in the system under consideration.

Power amplifiers are classified according to their mode of operation. Amplifier operating modes are determined from active device bias conditions and the output network topology. The bias conditions determine whether the active device is operated as a current source or as a switch, and also determine the period over which the active device conducts current (commonly referred to as the conduction angle) [Smith86]. Power amplifier designs are commonly referred to by their class names which are alphabetical designations (A, B, AB, C etc.). Each power amplifier class has a unique set of characteristics defining the class. The sections which follow examine the basic characteristics of the main classes of power amplifiers to provide a broad overview of the principles of power amplification and to highlight the unique characteristics of each class.

2.2 Class A Power Amplification

The Class A power amplifier is by far the simplest to understand. Fundamentally its operation differs very little from the small-signal amplifiers that all engineers are familiar with. The amplifier if biased correctly produces a linearly scaled replica of the input signal. A sine wave input to a Class A amplifier will produce at its output a sine wave exhibiting the same frequency but with a maximum amplitude determined by the amplifier gain. The linearity of Class A amplifiers is highly desirable in amplification of signals

carrying information in the modulated amplitude (AM) of the carrier such as Single Side Band (SSB) signals.

FIGURE 2-1 Class A Power Amplifier

In the Class A amplifier (refer to Figure 2-1) the active device is operated as a current source and is biased to ensure that it remains in the high output impedance region of its I-V characteristics. This region of the I-V characteristic curve is referred to as the saturation region for FETs and the active region for BJTs (see Figure 2-2). The DC drain bias is provided through a Radio Frequency Choke (RFC) which provides significant impedance to harmonic currents and acts as a constant current source. The blocking capacitor CB removes the DC component from the load current. The tank circuit on the output is tuned to the fundamental operating frequency and provides a low impedance path for harmonic currents (generated by the device nonlinearities), providing for an (essentially) sinusoidal output current in R_L . This tank circuit is optional in Class A amplifiers; however, it is normally included to reduce the harmonic content in the load current to acceptable levels. As a result, the drain current of the Class A amplifier can therefore be represented as:

$$i_D(\theta) = I_D + I_{dp} \sin(\theta) \quad (2-1)$$

Where I_D is the quiescent drain current (DC), I_{dp} is the peak value of the AC drain current and $\theta = \omega t = 2\pi f t$ represents angular time. As the blocking capacitor removes the DC component and the parallel tank removes (ideally) all harmonics, the load current is:

$$i_L(\theta) = I_{dp} \cdot \sin(\theta) \quad (2-2)$$

The efficiency of the Class A amplifier can be determined by obtaining the ratio of RF output power to DC input power. For the Class A amplifier presented in Figure 2-1, the DC input power (neglecting the small DC resistance of the RFC) is:

$$P_{DC} = V_{DD} \cdot I_D \quad (2-3)$$

Similarly, the RF output power can be determined by:

$$P_{out} = \frac{(I_{dp})^2 \cdot R_L}{2} = \frac{(V_{dp})^2}{2R_L} \quad (2-4)$$

Now in order to ensure the active device remains a high impedance current source, the peak output voltage V_{dp} and peak output current I_{dp} must be less than V_{DD} and I_D respectively. Thus the output power and drain efficiency (η) are:

$$P_{out} \leq \frac{(I_D)^2 \cdot R_L}{2} = \frac{(V_{DD})^2}{2R_L} \quad (2-5)$$

$$\eta \leq \frac{P_{out}}{P_{DC}} \leq \frac{\left(\frac{(V_{DD})^2}{2R_L}\right)}{V_{DD} \cdot I_D} = \frac{V_{DD}}{2R_L \cdot I_D} = 0.5 \quad (2-6)$$

While the drain efficiency of the Class A amplifier is only 50%, this amplifier topology is used in applications where linearity is of prime importance.

From (2-4) we can see that the maximum output power is obtained for a given load resistance when V_{dp} and I_{dp} are maximized considering the device capabilities (breakdown voltage: V_{BR} and maximum current: I_{MAX}). The optimal loading of the

amplifier can be determined through load line analysis [Vende90]. Using the RF measured I-V characteristics the designer plots a load line from the maximum RF device current I_{MAX} to the breakdown voltage V_{BR} . The slope of this load line provides the optimum load resistance (slope = $-1/R_{opt}$). This analysis neglects the impact of device parasitics and the output conductance. Parasitics would have to be compensated for through matching using reactive (lossless) elements and the value of R_{opt} is adjusted to compensate for the device output conductance.

Figure 2-2 illustrates a typical load line for class A operation. In order to ensure linear operation, the voltage swing at the drain must remain between the limits of V_{BR} and V_{MIN} , while the current swing at the drain must remain between ~ 0 and I_{MAX} .

FIGURE 2-2 Typical I-V Characteristics Illustrating Class A Load Line

To obtain the correct bias point for Class A operation the designer looks to the transit frequency (f_T) data for the device in question (see Figure 2-3). The selection of the DC bias current is based on the required bandwidth of the amplifier and the speed of the

device (f_T). Given the bandwidth required and the DC gain of the amplifier, the designer can determine the DC bias current to operate the device at the optimum f_T . The maximum bandwidth for the amplifier will occur when it is biased close to its peak f_T current. Depending on bandwidth requirements biasing near peak f_T results in wasted DC power.

FIGURE 2-3 f_T Plot for a Typical Device

Using the load line (which yields optimum load resistance) and the DC bias current the designer then determines the supply voltage required. It is important to note that in many designs the supply voltage is specified and as a result a load resistance which is not the optimum for the amplifier results. The efficiency under such conditions will also be lower than optimum. Figure 2-4 illustrates the Class A bias point, I-V characteristics and time domain drain voltage and current for a typical device. The progression from input signal

waveform to output signal waveforms follows a clockwise flow from the bottom left through the upper center as indicated by the arrows.

FIGURE 2-4 Class A Operation: Bias Point and Time Domain Waveforms

From Figure 2-4 it is apparent that the amplifier provides a linear representation of the input signal current over the complete RF cycle (conduction angle of 360°). This is true as long as the input signal (V_{GS}) is of small enough amplitude to ensure that V_{DS} remains between V_{MIN} and V_{BR} . If this is not the case, the amplified waveform contains high frequency components and distortion. Also apparent from the figure is the most significant limitation of Class A amplification - the zero-input-signal power dissipation. Under zero-signal conditions the Class A amplifier will dissipate $V_{DD} \cdot I_D$ watts. To overcome the limitations of Class A, a more efficient but less linear amplifier is used.

2.3 Class B Power Amplification

From the main limitation of the Class A amplifier - large zero-signal power dissipation - one can identify the main design principle of the Class B amplifier. If the quiescent power dissipation can be reduced, the efficiency of the amplifier can be increased significantly.

This is achieved in the Class B amplifier by utilizing a push-pull arrangement of two active devices driven through a transformer. The two devices are driven in such a manner that only one device is conducting current at a time. Using this arrangement both devices are biased at cutoff and dissipate zero quiescent power. The circuit topology of the Class B amplifier is illustrated in Figure 2-5.

FIGURE 2-5 Class B Amplifier Topology

The input transformer T_1 ensures that the gate inputs of the two FET devices are driven 180° out of phase. The DC source V_{GG} is present in the schematic for generality. In the event that depletion-mode devices are to be employed, V_{GG} would be set to the device pinch off voltage (< 0) to ensure the devices were cutoff when no RF input was applied. For enhancement devices the center tap of the secondary side of T_1 would be grounded ($V_{GG} = 0V$). For Class AB operation, discussed later, a small positive bias is applied through V_{GG} . The drain bias is applied through the center tap of the primary of T_2 .

As the RF input signal swings from zero to a positive value, the upper transistor conducts and amplifies the (positive going half) of the input signal. As the input signal falls to zero and below, the upper transistor becomes cutoff and the lower transistor conducts and amplifies the negative going half of the input signal. Each active device conducts current for half of the input RF cycle (conduction angle 180°), and during its conduction angle operates as a current source. Typical waveforms for the Class B amplifier are illustrated in Figure 2-6. The drain currents i_{d1} and i_{d2} flow in pulses, and when a device is conducting current the drain-source voltage is at its lowest level. This fact is responsible for the increased efficiency of the Class B amplifier.

FIGURE 2-6 Class B Amplifier Waveforms

As the drain current waveforms (i_{d1} and i_{d2}) are half sinusoids having a peak values of I_{dp} , the output current (i_o) is determined to be:

$$i_o(\theta) = I_{dp} \cdot \left(\frac{m}{n}\right) \sin(\theta) \quad (2-7)$$

The tuned output filter consisting of L_f and C_f ensures the output current is sinusoidal in the event harmonic current components are generated by device nonlinearity. The output voltage is simply:

$$v_o(\theta) = i_o(\theta)R_L = I_{dp}\left(\frac{m}{n}\right)\sin(\theta) \cdot R_L \quad (2-8)$$

The resulting drain voltage (across one half of the primary of T_2) becomes:

$$v_D(\theta) = V_{DD} + v_o(\theta) \cdot \left(\frac{m}{n}\right) = V_{DD} + I_{dp}R_L\left(\frac{m}{n}\right)^2 \sin\theta \quad (2-9)$$

where the peak value of the AC component of $v_D(\theta)$ is

$$V_{dp} = I_{dp} \cdot \left(\frac{m}{n}\right)^2 R_L = I_{dp} \cdot R \quad (2-10)$$

Where R is the load resistance transformed to the active half of T_2 's primary. To determine the efficiency of the push-pull Class B amplifier, we must obtain an expression for the DC input current. As current only flows in one half of the primary windings of T_2 each RF cycle, the total center tap current $i_{CT}(\theta)$ is simply the sum of the two drain currents or $I_{dp} |\sin(\theta)|$. The DC component of $i_{CT}(\theta)$ is:

$$I_{DC} = \frac{1}{2\pi} \cdot \int_0^{2\pi} I_{dp} |\sin(\theta)| d\theta = \frac{2I_{dp}}{\pi} \quad (2-11)$$

The DC input power is simply $V_{DD} * I_{DC}$ while the RF output power is computed from

$$P_o = \frac{v_o^2}{2R_L} = \frac{V_{dp}^2}{2R} \quad (2-12)$$

Finally, (as $V_{dp} \leq V_{DD}$) the maximum drain efficiency of the Class B amplifier is

$$\eta = \frac{P_o}{V_{DD} \cdot I_{DC}} = \frac{\left(\frac{V_{dp}^2}{2R}\right)}{\left(\frac{2V_{DD} \cdot I_{dp}}{\pi}\right)} = \frac{\pi \cdot V_{dp}^2}{4V_{DD} \cdot I_{dp} \cdot R} = \frac{\pi \cdot V_{dp}}{4V_{DD}} \leq \frac{\pi}{4} \approx 0.785 \quad (2-13)$$

This improvement in drain efficiency (of ~ 50%) provided by using Class B instead of Class A amplification is not without cost. As a result of biasing the active devices at cutoff, nonlinear distortion is introduced into the output and amplifier linearity is reduced.

2.3.1 Crossover Distortion and Class AB Operation

As mentioned previously, the parallel tuned circuit in Figure 2-5 is provided to ensure the output current is sinusoidal in the event that harmonic current components are generated by the active device nonlinearities. One significant source of nonlinearity is the fact that FETs exhibit a non-constant transconductance for small values of V_{GS} [Kraus80]. For larger values of V_{GS} the transconductance is essentially constant. When no RF input signal is applied to T_1 's primary, both FETs are cut off and no current flows in the load. As the RF input signal starts to rise above zero, the output current increases nonlinearly until the input signal level increases to the point where the transconductance becomes constant (point 'vn' in Figure 2-7). As a result, the output current is distorted for low input signal levels. A similar situation occurs when the RF signal falls below zero. Until the magnitude of the RF input signal exceeds the voltage at which the transconductance

becomes constant, the output current is distorted. This form of distortion is known as crossover distortion as it occurs when the RF input signal crosses over zero.

FIGURE 2-7 Crossover Distortion in Class B Amplifiers (not to scale)

Crossover distortion results in harmonic currents flowing in the output circuit. The parallel tuned filter is provided to ensure that harmonic currents reaching the load are reduced to an acceptable level.

The advantages of Class B operation can be achieved without the reduced linearity caused by crossover distortion by operating the active devices with a small quiescent bias current. Under these conditions (referred to as class AB operation) the DC source V_{GG} in Figure 2-5 is provided to supply the necessary bias voltage. Recall that for Class B operation this source is replaced by a short circuit to ground. If V_{GG} is set such that it is slightly greater than 'vn' (Figure 2-7), then distortion will be minimized and linearity will be improved.

While the quiescent bias current reduces the efficiency of the amplifier somewhat, the linearity achieved is worth the cost. The ideal efficiency of the Class AB amplifier is between that obtained for Class A and B amplifiers (50% - 75%). Class AB amplifiers are

commonly used in applications requiring linearity (such as SSB modulation schemes). The bias points for Class A, B, AB and C (described in the next section) are illustrated in Figure 2-8 for comparison. The bias points (solid dots in the figure) clearly show that for supply voltage V_{DD} the quiescent bias current increases from zero for Class B to the highest value for Class A.

FIGURE 2-8 Bias Operating Points: Class A, B, AB and C

The main limitation of the Class B amplifier is the requirement for transformers having large bandwidths (in excess of 2 octaves). The bandwidth requirements are due to the high harmonic content in the drain voltage and current waveforms.

For applications not requiring linear amplification (such as FM modulation schemes), higher efficiencies can be achieved through the use of a Class C power amplifier.

2.4 Class C Amplification

Higher efficiencies can be obtained through the use of Class C amplifiers. These amplifiers produce an output which is nonlinearly related to the input signal resulting in higher efficiency. The standard Class C amplifier consists of a single active device which is driven to act as a current source. Figure 2-9 illustrates the standard Class C amplifier which looks identical to the Class A amplifier topology in Figure 2-1. It is important to note however, that the parallel tuned circuit, while optional for the Class A amplifier, cannot be omitted from the Class C topology. The requirement for the filter stems from the necessity to filter harmonic components generated in the load current (resulting from the nonlinear amplification) to an acceptable level.

FIGURE 2-9 Class C Amplifier Topology

The major difference between Class A and Class C operation is in the biasing of the device. While both amplifiers operate the active device as a current source, the Class C amplifier biases the device below the point at which the device is cutoff. Recall that Class A biased the device midway between the limits of the minimum voltage to maintain current source operation (V_{MIN}) and the breakdown voltage for the device (V_{BR}).

Biasing the Class C amplifier below cutoff results in the drain current which flows in pulses, the duration of which is less than half of the RF cycle dependant on the amount of

negative gate bias applied. To clarify this point, the time domain waveforms for Class C operation are illustrated below.

FIGURE 2-10 Class C Amplifier Waveforms

From Figure 2-10 one can see that the drain current for the amplifier can be modeled as a sinusoid with a negative offset. During the period when the input signal is less than zero the device is cutoff and the drain current is negligible. Drain current flows during the period over which the input signal exceeds zero. From the waveforms it is apparent that the conduction angle for the Class C amplifier is less than 180° . This drain current waveform is rich in harmonics and necessitates the use of a narrowband tuned filter to ensure that harmonic currents in the load are reduced to acceptable levels (-60dB is a typical requirement).

To determine the efficiency of the Class C amplifier topology we must determine the DC input current. As the drain current can be modeled as a biased sinusoid one obtains :

$$i_D(\theta) = \begin{cases} I_{DP}\cos(\theta) + I_{DQ} & : I_{DP}\cos(\theta) + I_{DQ} \geq 0 \\ 0 & : I_{DP}\cos(\theta) + I_{DQ} < 0 \end{cases} \quad (2-14)$$

where I_{DQ} is analogous to the quiescent current in Class A and Class AB amplifiers (however here I_{DQ} is negative), and I_{DP} is the peak value of the AC drain current as the result of RF drive.

The conduction angle of the device can be related to the values of I_{DQ} and I_{DP} as follows [Kraus80]:

$$\phi = \begin{cases} \arccos\left(\frac{-I_{DQ}}{I_{DP}}\right) & : |I_{DQ}| < I_{DP} \\ \pi & : I_{DQ} - I_{DP} > 0 \\ 0 & : I_{DP} + I_{DQ} < 0 \end{cases} \quad (2-15)$$

where 2ϕ is the conduction angle. From (2-15) it is apparent that when I_{DQ} is greater than zero and larger than I_{DP} the device conducts current for a complete RF cycle (360° or 2π radians). For I_{DQ} less than zero but having a magnitude greater than I_{DP} the device is cut off and no current will flow. For Class C operation (from (2-15))

$$I_{DQ} = -I_{DP} \cos(\phi) \quad (2-16)$$

The DC current is obtained by averaging the drain current over one RF cycle. Substitution of (2-16) into (2-14) and averaging yields:

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} i_D(\theta) d\theta = \frac{1}{\pi} \int_0^\phi (I_{DP}\cos(\theta) + I_{DQ}) d\theta = \frac{I_{DP}}{\pi} (\sin\phi - \phi \cos\phi) \quad (2-17)$$

The DC power consumed by the device is simply $V_{DD}I_{DC}$. As the tuned filter prevents harmonic currents in the load, the magnitude of load current is equal to the magnitude of the fundamental component of the drain current. Through Fourier analysis the fundamental component of the drain current can be shown to be [Plett97]:

$$I_{D1} = \frac{I_{DP}}{2\pi}(2\phi - \sin 2\phi) = I_O \quad (2-18)$$

The output power of the Class C amplifier is simply the product of the rms output voltage and current. As with the Class A and B amplifiers, the Class C amplifier achieves maximum efficiency when the output voltage swing is maximized. In this respect the peak output voltage will be a maximum of V_{DD} resulting in an output voltage swing of 0V to approximately $2V_{DD}$. From this, the maximum output power is:

$$P_{out} = \frac{V_{OP}}{\sqrt{2}} \cdot \frac{I_{OP}}{\sqrt{2}} \leq \frac{V_{DD} \cdot I_{OP}}{2} = \frac{V_{DD} \cdot I_{DP}(2\phi - \sin 2\phi)}{4\pi} \quad (2-19)$$

From which the maximum drain efficiency is determined to be:

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{\left(\frac{V_{DD} \cdot I_{DP}(2\phi - \sin 2\phi)}{2\pi} \right)}{\left(V_{DD} \cdot \frac{I_{DP}}{\pi}(\sin \phi - \phi \cos \phi) \right)} = \frac{2\phi - \sin 2\phi}{4(\sin \phi - \phi \cos \phi)} \quad (2-20)$$

Figure 2-11 illustrates the maximum efficiency achievable as a function of conduction angle.

FIGURE 2-11 Efficiency as a Function of Conduction Angle (2ϕ)

From the figure it is apparent that as the conduction angle is decreased the efficiency of the amplifier increases. Also apparent are the efficiencies for Class A operation (50% @ 360 °) and Class B operation (78.5% @ 180 °). Not apparent from the figure; however, is the fact that as the conduction angle decreases and efficiency increases, the output power provided decreases, for a fixed V_{DD} . The decline in output power can be identified from (2-19) . As the conduction angle (2ϕ) decreases to zero the output power declines to zero as well. Hence for typical Class C operation, the amplifier is designed to provide efficiencies on the order of 80% to achieve a suitable balance between efficiency and output power.

The analysis provided above assumes that the output current waveform is the tip of a sinusoid. This implies that the transconductance of the device is constant. While this provides tractable equations leading to closed form expressions, it is not as accurate as numerical analysis. In numerical analysis the transconductance of the device is assumed to be a linear or exponential function of the applied voltage. While the results are similar to those obtained using the constant gm approach, the non-constant gm models introduce distortion into the output waveform. The output filter removes the majority of this distortion prior to reaching the load. However, the efficiency is less than that predicted by the constant gm ("tip of a sinusoid") analysis used here.

It should also be noted that the Class C amplifier topology examined here is suitable for amplification of AM modulated signals through modulation of the supply voltage. For a complete discussion of the amplitude modulation capabilities of Class C amplifiers the reader is referred to [Kraus80].

2.5 Class F Amplification

The final class of amplifier which employs the active device as a current source is the Class F amplifier. In Class F operation the goal is to prevent simultaneously imposing large current through and large voltage across the active device. The basic Class F amplifier topology is illustrated in Figure 2-12. The amplifier consists of a single active device driven as a current source and a load network exhibiting resonances at the fundamental as well as harmonics of the input signal frequency.

FIGURE 2-12 Class F Amplifier Schematic

The load network itself consists of two parallel tuned tank circuits, one tuned to the third harmonic of the input frequency ($L3, C3$) and the other tuned to the fundamental ($L1, C1$). The fundamental-tuned tank ensures a sinusoidal current in the load by providing a low impedance shunt path to ground for all harmonic currents.

The third harmonic tank provides a large impedance to any third harmonic component of drain current and low impedance to all other harmonics. This results in a drain voltage waveform containing both fundamental and third harmonic components and a drain current waveform consisting of the fundamental, second and all harmonics above the third. As such, power is only generated at the fundamental frequency.

If we assume that the phase and amplitude of the third harmonic drain current component can be controlled, the drain voltage for the Class F amplifier has the following form:

$$v_D = V_{DD} + V_{1P}\sin(\theta) + V_{3P}\sin(3\theta) \quad (2-21)$$

where V_{1P} and V_{3P} are the peak values of the fundamental and third harmonic components respectively. The sample waveforms for the Class F amplifier are illustrated in Figure 2-13 and show that the drain current is at its lowest level when the drain voltage is highest. Power dissipation (and hence efficiency) can be improved if during the period of drain current flow, the drain voltage could be flattened (ideally at zero volts).

FIGURE 2-13 Class F Amplifier Waveforms (Fundamental and 3RD Harmonic Only)

From (2-21) it is apparent that the extreme values of the drain voltage waveform occur at $\theta = \pi/2$ and $\theta = 3\pi/2$. In this regard, maximum flatness in the voltage waveform can be achieved if the even-order derivatives are set equal to zero at these points [Rabb96]. The odd-order derivatives of the drain voltage waveform is zero at these points (since $\cos(\pi/2)$ and $\cos(3\pi/2)$ are 0). The second derivative is:

$$\frac{d^2 v_D}{d\theta} = -V_{1P} \sin \theta - 9V_{3P} \sin 3\theta \quad (2-22)$$

substitution of $\theta=3\pi/2$ (the minimum point for $v_D(\theta)$) and setting (2-22) equal to zero yields:

$$0 = V_{1P} - 9V_{3P} \Rightarrow V_{3P} = \frac{1}{9}V_{1P} \quad (2-23)$$

In order for the drain voltage waveform to reach zero at $\theta=3\pi/2$ the condition in (2-23) must be met. Substitution of (2-23) into (2-21) and setting equal to zero yields:

$$\begin{aligned} V_{DD} - V_{1P} + V_{3P} &= 0 \\ V_{DD} - V_{1P} + \frac{1}{9}V_{1P} &= 0 \\ V_{1P} &= \frac{9}{8}V_{DD} \\ V_{3P} &= \frac{1}{9}V_{1P} = \frac{1}{8}V_{DD} \end{aligned} \quad (2-24)$$

The waveforms produced under these conditions are illustrated below:

FIGURE 2-14 Harmonic Components for Maximally Flat Drain Voltage Waveform

Fourier analysis of the drain current and voltage waveforms results in the following expression for the drain efficiency of the standard Class F amplifier [Kraus80]:

$$\eta = \frac{\pi V_{IP}}{4V_{DD}} = \frac{9}{8} \cdot \frac{\pi}{4} = 0.884 \quad (2-25)$$

The efficiency of the Class F power amplifier is significantly higher than the Class A and B amplifiers examined thus far. The efficiency is also good compared to that achievable with the Class C amplifier providing reasonable output power.

The preceding analysis considered only the fundamental and third harmonic components of the drain voltage. If additional harmonic components of drain current and voltage are considered, the theoretical efficiency of the Class F amplifier can be increased to 100%. The schematic in (2-15) illustrates how the increase in efficiency can be achieved.

FIGURE 2-15 Transmission Line Tuned Class F Amplifier

As per the standard Class F amplifier, the fundamental-frequency tuned circuit ($L1$, $C1$) provides a low impedance shunt to ground for all frequencies except the fundamental. The third harmonic tuned circuit has been replaced by a transmission line having an electrical length of $\lambda/4$ (where λ is the guided wavelength for the fundamental frequency in the material the transmission line is fabricated on). The purpose of the transmission

line is to transform the input port impedance of the tuned circuit (and R_L) to the required harmonic impedance at the drain. From Figure 2-13 we see that if the drain voltage can be made essentially square, exhibiting a minimum value close to zero over the period when the drain current flows, the power dissipation can be reduced to an insignificant level. As the Fourier components of a square wave consist of the DC, fundamental and odd harmonics (from 3 - ∞) the transmission line must transform the load impedance to the required harmonic impedance at the drain. Once again the parallel tuned circuit presents (ideally) infinite impedance at the fundamental and zero impedance to all other frequencies. It is a well known fact in microwave design that a $\lambda/4$ transmission line acts as an impedance inverter and a $\lambda/2$ line provides no impedance transformation [Pozar90]. The electrical length of the transmission line for harmonic frequencies is $n\lambda/4$ where n is the harmonic number. From this it is apparent that for the fundamental the impedance seen at the drain is zero, while for the odd harmonics the zero impedance of the tank circuit is transformed to an infinite impedance seen at the drain. For the even harmonics, the low impedance provided by the tank circuit is not transformed as $n\lambda/4$, for n even yields an integer multiple of $\lambda/2$. Thus the drain current consists of a DC component, the fundamental and even harmonics (see Figure 2-13). The drain voltage waveform contains

a DC component, the fundamental and odd harmonics. Under these conditions the efficiency of the Class F amplifier is 100%.

FIGURE 2-16 Typical Waveforms : Transmission Line Tuned Class F Amplifier

The standard (third harmonic resonator) Class F amplifier is the final configuration that operates the active device as a current source. The transmission line Class F with its square wave drain voltage allows the active device to operate as a switch. Operating the active device as a switch results in higher efficiencies. Two additional amplifier topologies which operate the active device as a switch are examined in the next sections.

2.6 Class D Amplification

As mentioned in regard to the transmission line tuned Class F amplifier, operation of the active device as a switch results in much higher efficiency than is possible when operating the device as a current source. The main reason amplifiers based on active switches are more efficient is due to the fact that the minimum voltage across the switch while current is flowing is many times smaller than the voltage required for correct operation of a

current source. In this regard, the Class D amplifier operates two active devices driven to operate as a two pole switch. The Class D amplifier is capable of providing switching action for either voltage or current. That is, either the drain voltage or drain current waveform is a square wave. A schematic for a transformer-coupled voltage-switching Class D amplifier is illustrated below.

FIGURE 2-17 Class D Amplifier: Voltage-Switching Version

The theoretical efficiency of the Class D power amplifier is 100%, as the devices operate with essentially zero voltage across them when conducting current.

A significant limitation of the Class D amplifier is the necessity for transformers on the input, to drive the transistors 180° out of phase, and at the output to generate the complete waveform (similar to a Class B amplifier). As the output waveforms are rich in harmonics, the transformers require large bandwidths to ensure their correct functioning. Design of these wideband transformers can be complicated, requiring transmission line designs rather than discrete components. The quality of on chip inductors and transformers is therefore a limiting factor in using transformer based amplifier topologies for power amplification. These issues are addressed further in Chapter 3 of this work.

Another limitation of the class D amplifier is that the parasitic capacitance of the active device and any stray circuit capacitance at the drain of the device is discharged to ground when the device turns on each cycle resulting in an increase in power consumption and reduced efficiency. As a result of these limitations the Class D amplifier is not considered a suitable candidate for the high-efficiency power amplifier topology for use in this research.

2.7 Class E Amplification

The Class E power amplifier uses a single active device driven as a switch and a specially designed passive load network. The use of a single device in a switching amplifier eliminates the requirement for complex (band-limiting) transformer structures and reduces the complexity of the design. The schematic for the basic Class E amplifier topology is illustrated in Figure 2-18.

FIGURE 2-18 Class E Amplifier Topology

The DC drain bias is supplied through an RFC, providing a source of constant current. The shunt capacitance in the load network (C_p) incorporates the parasitic output capacitance inherent in the active device as well as any additional capacitance to obtain the desired performance. The load network is specially designed such that its transient

response to the periodic switching of the active device produces the desired current and voltage waveforms (Figure 2-19) .

FIGURE 2-19 Typical Class E Waveforms

As the Class E amplifier uses the parasitic device capacitance in its operation, there is no reduction in efficiency due to discharge of this capacitance as was mentioned during the discussion of Class D switching amplifiers.

In the cursory analysis which follows (additional details will be provided in Chapter 4), the following assumptions are made:

1. the active device acts as an ideal switch
 - zero 'on' resistance,
 - infinite 'off' resistance, and
 - output capacitance which is independent of voltage.
2. the quality factor (Q) of the output circuit is sufficiently high such that the load current can be considered a sinusoid at the operating frequency.

Utilizing these assumptions the amplifier topology can be represented by the equivalent circuit of Figure 2-20.

FIGURE 2-20 Class E Amplifier Equivalent Circuit

From the equivalent circuit one can identify an ideal tuned circuit, consisting of L and C as shown, which (ideally) produces zero impedance at the fundamental and infinite impedance at all other frequencies. This tuned circuit, coupled with the additional reactance jX in Figure 2-20, corresponds to L_o and C_o in Figure 2-18. As a result of this ideal series resonator the voltage $v_I(\theta)$ is equal to the fundamental component of the drain voltage waveform $v_S(\theta)$.

When the switch (SW) is open, the current through the switch, $i_S(\theta)$ is zero and the shunt capacitor charging current, $i_C(\theta)$ is the difference between I_{DC} and $i_O(\theta)$. As the current through L_{DC} cannot change instantaneously, $i_C(\theta)$ equals current flowing in the switch immediately prior to the switch opening. When the switch is closed the voltage across the switch is zero and thus the current through C_P is zero. The switch current $i_S(\theta)$ is therefore $I_{DC} - i_O(\theta)$.

The components of the load network are chosen such that the transient response to the periodic operation of the switch results in $v_S(\theta)$ rising and then falling to zero during the

period when the switch is open. Any voltage existing across C_p at the instant the switch turns on will be instantaneously discharged to ground and power dissipation will increase because the energy stored in C_p is wasted.

The optimum condition is to have the voltage across the switch be exactly zero at the moment the switch turns on. In addition, having the slope of the voltage waveform equal to zero at the moment the switch turns on allows for some slight mis-tuning in the load components with little loss of efficiency [Sokal75A].

Determination of the voltage and current waveforms for the ideal Class E amplifier is somewhat difficult as the waveforms are not explicitly specified over the entire RF cycle [Kraus80]. A complete derivation of these equations can be found in Chapter 4.

The main reason for the high efficiency of the Class E amplifier is the fact that the device is operated as a switch, so that high voltage and current are not presented to the active device simultaneously, and also that the parasitic device capacitance is incorporated into the load network to minimize loss.

2.8 Why Choose Class E Amplification?

From all the power amplifier topologies examined in this chapter the Class E amplifier has the highest ideal efficiency along with the fewest number of components. Table 2-1 indicates the key properties of each of the amplifier classes for easy reference.

TABLE 2-1 Amplifier Class Characteristics

Class	Active Devices	Operational Mode	Efficiency	Components	Linearity
A	1	CS	50%	Simple	Excellent
B	2	CS	78.5%	Transformers	Crossover Distortion
AB	2	CS	50-78.5%	Transformers	Good
C	1	CS	78.5-90%	Simple	Nonlinear
D	2	Switch	100%	Transformers	Nonlinear
E	1	Switch	100%	Simple	Nonlinear
F	1	CS	88.4%	Simple	Nonlinear

The Class A amplifier topology while exhibiting excellent linearity suffers from the poorest efficiency. Classes B, and AB have slightly better efficiency; however, they require complementary devices or transformers to drive the inputs of the devices out of phase and for generating the complete output waveform. Class D amplifiers have a similar requirement for transformers - a difficult device to operate over wide bandwidths. The Class C amplifier exhibits high efficiency and is relatively simple to construct. The Class F and E amplifiers also exhibit high efficiency and consist of relatively few (and simple) components.

In this regard, this thesis work examines the Class E amplifier topology for implementation using silicon carbide MESFET devices (as examined in Chapter 3). In order to meet the drive waveform requirements for the Class E amplifier, a Class F driver amplifier will be incorporated. The following chapters of this thesis examine the design and implementation of the power amplifier in detail.

3.1 Technology Issues in Power Amplifier Design

In the design of a power amplifier the choice of the technology and the active devices to be employed are crucial to the success of the design. Obviously the technology and active devices must be selected in light of the final point of application in the cellular system. For handset applications, highly integrated (lower power) power amplifiers are required, as handset size and weight as well as the available power supply (batteries) provide fundamental design constraints. For base-station applications high power is a requirement. Base-station power amplifiers are generally discrete implementations having components capable of high-voltage operation. As the number of discrete components in a system increases the final cost, the base-station power amplifier is a significant expense.

While the need for efficiency is readily apparent in handset applications - the battery life depends on the efficiency of the PA - efficiency is also required in base-stations. From the service provider perspective, the power consumed by the base-station amplifiers is a significant cost [Kraus80]. In this regard, efficient power amplification is required at both ends of the cellular loop.

From a power amplifier design perspective, the main technology issues which require consideration are the properties of the metallization, the device breakdown voltages, and active device current handling capability.

3.2 Metallization Properties

Metal traces in most modern technologies have current density limitations to prevent electromigration, enhance reliability and increase mean time between failures (MTBF). Metallization in modern IC processes is selected to provide high conductivity (low parasitic resistance) and good current carrying capability. As an example, most modern silicon processes utilize aluminum metallization for the top level of metal. Aluminum is used because it is relatively inexpensive and can be used to form ohmic contacts with silicon. Gold, while exhibiting higher conductivity and lower series resistance than aluminum cannot be utilized in silicon processes as the contacts will diffuse into the silicon and create trap states in the middle of the energy band gap - a highly undesirable situation. In fact procedures are in place in most fabrication laboratories to prevent such gold contamination of a silicon process. Gallium Arsenide processes use gold as the metallization, as contamination is not an issue. The gold metallization exhibits a much higher current density than does aluminum. This situation allows GaAs power amplifier ICs to produce higher output powers than comparable silicon units. In addition to electromigration robustness, the metallization used in the process has a significant impact on the quality of on-chip filtering.

3.2.1 On-Chip Filtering Issues

It is important to consider the fact that all of the amplifier configurations outlined in chapter 2 contained some form of filtering to reduce the harmonic content in the load. While it is true that such filtering can be performed with 'off-chip' components, the desirable situation is to perform the filtering using 'on-chip' LC filters to reduce the component count, complexity, cost and product weight. The quality of the metallization used in the process plays a significant role in this aspect of power amplifier design as well. The quality of 'on-chip' spiral inductors formed using top level metallization is directly

affected by the material properties of the metallization. Inductors formed using aluminum (silicon processes) suffer from low Q (quality) factors, in the range of 2-10 depending on the process [Long95]. The effectiveness of 'on-chip' filtering is directly related to the quality of the filtering components. Again, the lower series resistance of the gold metallization of GaAs processes results in higher quality 'on-chip' inductors and thus better filtering. In addition, the semi-insulating substrate provided by the GaAs process improves the quality of on-chip filtering components by reducing the parasitic substrate capacitances and currents. Silicon processes with their aluminum metallization and conductive substrates suffer in comparison to GaAs. The main advantage of silicon is the maturity of most processes and the significantly lower cost than GaAs. In this regard, talented designers are devising novel methods of pushing the silicon technology to new limits of performance. In addition to metallization properties, the power amplifier designer is concerned with the properties of the active devices with respect to breakdown voltage and current handling capability.

3.3 Device Breakdown Voltages

As with all the amplifiers outlined in chapter 2 the output power provided is proportional to the supply voltage driving the amplifier. Thus in order to obtain large output powers, active devices capable of sustaining large voltage swings without suffering reverse breakdown are required. In this regard, the operating mode of the amplifier is crucial in determining which devices to use for a given output power. Amplifier topologies which exhibit higher voltage swings might not be desirable, as they require lowering the DC supply to prevent breakdown. This is the situation when designing a Class E amplifier topology for use in silicon bipolar IC processes. The low breakdown voltages of such processes (3-5V) and the optimum voltage across the device requires lowering the supply voltage with the corresponding reduction in power output. On the other hand, silicon

carbide devices exhibit very large breakdown voltages ($\sim 100\text{V}$) due to the high breakdown field strength. These devices are capable of operating at much higher supply voltages. As a result, the device breakdown voltage is a fundamental determinant in selecting the amplifier operating mode and hence topology.

3.4 Current Handling Capability

The type of amplifier topology also impacts the choice of the active devices used. For example the current source amplifiers (Class A, B, C, etc.) require the capability of driving large currents into a load in order to generate large output powers. In these situations, active devices exhibiting large transconductances are desired (i.e. bipolar transistors). For switching based power amplifiers, current drive is not the primary concern, but device switching performance is. It is well known that the FET classes of devices generally exhibit superior switching performance to that shown by bipolar transistors. FET devices being unipolar by nature have no charge storage effects, resulting in more controllability over the switching action. In addition FETs are capable of passing current equally well in either direction - a situation which is not possible for bipolars.

While both silicon and GaAs power amplifiers are in use in today's cellular systems, research is proceeding into the use of silicon carbide for use in high power microelectronics. Thus this thesis explores the use of silicon carbide in a combined Class F - Class E power amplifier.

3.5 Properties of Silicon Carbide (SiC)

Silicon carbide was discovered by accident by Jons Jacob Berzelius in 1824 during experiments to create artificial diamonds. Although the first SiC light emitting diode (LED) was produced in 1907, it was not until Lely developed the sublimation method for growing reasonable quality single crystal structures, in 1955, that SiC became more widely explored for use in electronic devices. Silicon carbide does not occur naturally in nature and is formed as a silicide of carbon. SiC crystals are formed in over 180 different crystal structures known as polytypes. The polytypes differ not in number of Si and C atoms but in their arrangement in the crystal lattice. The polytypes simply define the stacking order of the Si and C atoms in the lattice.

As one would expect, each different polytype exhibits unique electrical and optical properties. The two most common SiC polytypes are referred to as 4H and 6H. The H stands for the crystal structure (hexagonal in this case) and the number refers to the number of stacked layers occurring before the stacking pattern repeats [Moroc94]. The electrical properties of the more common SiC polytypes are compared with those Si and GaAs in Table 3-1. From the table one can see that silicon carbide exhibits much lower relative

TABLE 3-1 Material Properties Comparison : SiC to Common Semiconductors
[Neude85] [MacEl97]

Property	4H SiC	6H SiC	Si	GaAs
Band Gap [eV]	3.2	3.0	1.1	1.42
Relative Permittivity	9.7	9.7	11.9	13.1
Breakdown Field [V/cm]	3E6	3.2E6	0.6E6	0.6E6
Thermal Conductivity [W/cm-K]	4.9	4.9	1.5	0.46
Saturated Drift Velocity [cm/s]	2.0E7	2.0E7	1E7	0.8E7
Substrate Resistivity [Ω -cm]	1E15	1E15	3E3	1E7
Electron Mobility [$\text{cm}^2/\text{V/s}$]	800	370	1100	8500
Hole Mobility [$\text{cm}^2/\text{V/s}$]	115	90	420	400
Commercial Wafer Diameter [mm]	31.88	31.88	300	150

permittivity, much larger bandgap, on the order of five times the breakdown field of silicon or GaAs, and at least twice the saturated drift velocity of the most common semiconductors. While SiC exhibits a much lower carrier mobility than silicon, its other material properties more than compensate for high-voltage and/or high-temperature operations. These properties of SiC make it highly suited for use in base-station power amplifier designs.

Exhibiting a lower dielectric constant than silicon or GaAs, silicon carbide has lower parasitic device capacitances (to substrate) than a similar sized device fabricated in the other technologies. The implication here is that with smaller parasitic capacitances, the input and output impedances of the device will be higher, allowing easier matching for power transfer. The smaller parasitic capacitances also implies that the devices could be operated at higher frequencies. In addition, the smaller capacitances result in less coupling of substrate noise into the active device. The high substrate resistivity of the SiC devices also would significantly reduce substrate losses and any noise coupling from the substrate into the active devices.

The bandgap of SiC is on the order of three times that of silicon and over twice that of GaAs. The implication of the larger bandgap is that the SiC devices are capable of providing desirable semiconductor properties to a much higher temperature than devices fabricated in the other technologies. From a power amplifier perspective, the ability to function at elevated junction temperatures is required due the self-heating effects within the device. Power amplifiers commonly operate with large currents and the resulting joule heating raises the device temperature significantly. For large output power levels with silicon or GaAs amplifiers, cooling of the device is often required, increasing the final cost.

The high thermal conductivity of SiC also provides a benefit for power amplifier designs as it simplifies the heat dissipation problem. For large output power levels in silicon or

GaAs, large heat sinks are required to dissipate the heat produced in the device to maintain the junction operating temperature within acceptable limits. Silicon carbide on the other hand has three times the thermal conductivity of silicon and almost 11 times that of GaAs. In this regard the heat sinking requirements of SiC power amplifiers would be much simplified and in some cases eliminated all together. In addition, the high thermal conductivity of SiC will allow very high packing densities to be achieved as the heat produced in the small area can be dissipated easier than with Si or GaAs designs.

One of the most significant benefits that silicon carbide has to offer to power amplifier design is the extremely high breakdown voltage. While a modern silicon IC process for BJTs has a typical breakdown voltage (between base and collector) of from 3-5V a SiC MESFET exhibits breakdown voltages (between gate and drain) of over 100V. This order of magnitude increase in breakdown voltage implies that the SiC device can operate at very high supply voltage and thus produce high output power without the need to use high currents. This reduces to the fact that the SiC device can generate large output powers while maintaining reasonable impedance levels, simplifying the matching challenge. In addition, the large breakdown fields imply that the size of the device can be reduced significantly while operating at the same voltage levels. This implies a higher packing density may be achieved than in Si or GaAs. While packing density is not of primary concern for power amplifiers it is an important consideration for integrated applications which will surely be the subject of future research. Finally, the large breakdown voltages of the SiC devices are particularly suited for nonlinear power amplification techniques where the drain voltage excursions are much larger than the DC bias voltages. This is particularly applicable to Class E amplification, where the peak drain voltage can reach approximately four times the applied DC bias value.

The final property of interest in the design of power amplifiers is the saturated drift velocity of the technology. In SiC, the saturated drift velocity is twice as high as silicon

and three times that of GaAs. This translates into lower “on resistances” for the active devices - a desirable property for switching based power amplifiers. The large drift velocity also maximizes the f_T and f_{MAX} for the devices. This is important when operation the power amplifier in the microwave/ RF regime of the spectrum.

3.6 Structure of the SiC MESFET

Figure 3-1 illustrates a cross sectional view of a SiC MESFET. The structure is similar to MESFETs fabricated in other technologies. The device consists of a semi-insulating substrate of high resistivity to reduce substrate losses. A low doped P type layer provides for additional device isolation. Flow of majority carriers in the channel is controlled by the application of a negative potential to the Schottky gate (depletion mode device).

FIGURE 3-1 Physical Structure of a Silicon Carbide MESFET

Recent research comparing the modeled power densities for Si, GaAs and SiC MESFET type devices indicates the potential for SiC in power amplification applications. One

study [Weitz95] indicates that (under high-voltage bias conditions) SiC MESFETs exhibit by far the best results (Table 3-2).

TABLE 3-2 Modelled Power Densities for Various Technologies [Wietz95]

Property	Silicon	GaAs	Silicon Carbide
Drain Voltage [V]	8.4	8.3	105
Power Density [W/mm]	0.45	0.78	17.37

From this data we can understand the drive behind research into the use of silicon carbide for use in microelectronics - specifically for power amplification applications. While the prospects for silicon carbide appear bright the widespread use of this technology is not without its "teething problems".

3.7 Current Status of Silicon Carbide Technology

Currently the most significant impediment to the widespread use of silicon carbide technology is the inability to generate flawless single crystal structures so necessary for microelectronic applications. The main factor limiting the performance and manufacturability of silicon carbide devices is the formation of a structural defects known as micropipes.

Micropipes are small tubular voids in the silicon carbide crystal which run in a direction perpendicular to the polished surface of the wafer [Neude95]. These voids have been shown to be responsible for the premature failure of large scale SiC devices having areas greater than 1mm^2 . The failures resulted from junction breakdown at electric field levels far below the published breakdown field.

While the defect density has fallen in recent years (from 100s/cm^2 to a minimum of $5/\text{cm}^2$) it still prevents the reproducible formation of large SiC devices capable of handling

the large currents required when generating large output powers. While micropipe defects are present in all SiC devices, the defect density doesn't present a significant problem until the device size area is increased above 1mm^2 . This fact provides a significant impediment to expanding the use of SiC in high-power amplification applications.

While the cause of these defects is currently the subject of extensive research, it is estimated that 3-4 years will be required before micropipe defects can be eliminated from the SiC crystal structure [Palmo94].

3.8 Research Project Limitations Resulting from SiC

The choice to employ a developing (rather than a mature) technology in this research results in some limitations with respect to the achievable results. These are examined in the paragraphs which follow.

The devices utilized in this research were provided by a third party supplier to allow device characterization experiments to evaluate the silicon carbide technology. In this regard, individual die transistors were made available for experimental use. The implications of this are that amplifier device sizes could only be optimized to a certain extent (i.e. custom device sizing was not available), and that the amplifier topology would have to be based on a hybrid design approach as no additional components could be integrated on the transistor die. This necessitated board level design and implies that significant parasitic effects could be expected due to bond wires interconnecting the active devices. This also implies that lower output power levels can be achieved than would be possible if custom devices and/or multiple interconnected devices could be fabricated on a single die.

An additional limitation of using the third party supplied SiC devices is the lack of device models for the variety of microwave and RF circuit simulation programs. Unfortunately the only model available for the SiC MESFET devices used in this research was an HSPICE GaAsFET model based on the Curtice/Statz hyperbolic tangent model using a user defined VGST exponent [MetaS96].

Attempts were made to determine if the model data could be ported over to one of the GaAsFET models provided with Libra (HPEESOF), however this failed to produce reasonable results. Further inspection of available models and discussions with Hewlett Packard identified the fact that an entire block of model code would have to be written. As this was not the purpose of the project, and sufficient time was not available to write, test and debug the necessary model code the HSPICE model was used.

The implication of utilizing HSPICE for board level design is that while transmission lines can be modeled in HSPICE to some extent, complex microwave structures such as microstrip corners, bends and T junctions cannot be easily modeled. Complex transmission line structures would have to be simulated (in Libra for example) and lumped-element equivalent circuits would have to be developed for simulation in HSpice. As such the high-level amplifier simulations are not as comprehensive as those Libra could provide, as they could not easily incorporate all the additional parasitic effects that Libra easily models. In addition, transient simulations had to be used in HSPICE rather than the more convenient Harmonic Balance Frequency domain simulation tools available with Libra.

Design Methodology for a Class E Switching Power Amplifier

4.1 Introduction

The Class E amplifier has been shown to exhibit high-efficiency and relative simplicity (in terms of the number of components) and as a result has been chosen as the amplifier topology implemented in this research work. This chapter examines in detail the design methodology for Class E switching power amplifiers.

The analysis detailed here follows that provided by [Zulin87] and [Sowla96]. In this thesis, refinements and extrapolation are added to allow normalized design curves to be obtained. As in the previous analyses the following assumptions are made about the Class E amplifier under examination:

1. The active device operates as an ideal switch in that it exhibits zero 'on resistance', infinite 'off resistance' and no varactor capacitance effects. In addition the device is capable of withstanding negative voltages ($V_{DS} < 0$) and currents ($I_D < 0$).
2. The load current is essentially sinusoidal. This condition is approached for large values of quality factor (Q) for the series (L_o , C_o , R_L) load network,
3. Elements of the equivalent circuit are lossless, and
4. The switch duty cycle is 50%.

FIGURE 4-1 Basic Class E Amplifier (RFC in DC Supply Line)

The basic Class E amplifier consists of an RF choke in the drain supply lead, acting as a constant current source. The output load network (C_p , L_o , C_o , R_L) is designed to provide a suitable transient response to the periodic switching of the active device. The shunt capacitance C_p incorporates the parasitic device capacitance as well as any additional capacitance required to provide the necessary performance. Recall from Chapter 2 (Figure 2-20, on page 46) that the series resonant circuit (L_o , C_o) is not resonant at the fundamental operating frequency. It resonates at a slightly lower frequency, as L_o incorporates the additional series reactance (jX) to provide the necessary phase shift between the output voltage and the fundamental component of the drain voltage.

While the large majority of the previous papers on the subject of Class E amplifiers, [Rabb77], [Sokal75], [Sokal75A], [Kazim87] employ an RF choke in the drain supply lead, the analysis performed by Zulinski proves that use of an inductance exhibiting smaller reactance than the RFC provides larger output powers. The analysis which follows determines the time domain waveforms for an ideal switch Class E amplifier and

is based on analysis of the equivalent circuit of Figure 2-20, on page 46, repeated here for convenience.

FIGURE 4-2 Class E Amplifier Equivalent Circuit ($L_{DC} < L_{RFC}$)

4.2 Derivation of the Ideal Class E Design Equations

As mentioned previously, the derivation of the equations governing the operation of the Class E amplifier, follow the work performed by previous authors. An expanded derivation is included in this chapter to provide the foundation for understanding Class E amplifier operation, and to allow normalized design curves to be generated. The normalized design curves resulting from this work allow the designer to rapidly obtain first cut design parameters for a Class E amplifier which can be optimized through circuit simulation. In addition, the normalization process provides information on operating conditions for Class E amplifiers which provide maximum output power.

In amplifiers operating Class E, the input of the active device is driven with a signal which produces a fast switching response from the device (square wave drive). The assumption

of ideal performance of the switch implies that when the switch is closed the voltage across it is zero, and when the switch is open the current through it is zero. In this regard the voltage and current waveforms are not explicitly described over the complete RF cycle. As such, piecewise functions are obtained and the boundary conditions are evaluated to ensure the resulting waveforms are continuous. Analysis is conducted over one complete RF cycle, that is, for $0 < \theta \leq 2\pi$. Figure 4-3 illustrates typical waveforms for the ideal Class E amplifier. .

FIGURE 4-3 Ideal Class E Amplifier Waveforms Showing Input Drive

From the nomenclature on Figure 4-3, we can see that θ_1 assumes two distinct values dependent on which portion of the RF cycle we are analyzing. For analysis conducted during the off period ($0 < \theta \leq \pi$), θ_1 is assigned the value 0. For analysis during the on portion of the cycle ($\pi < \theta \leq 2\pi$), θ_1 is assigned the value 2π .

Referring to Figure 4-2, the series tuned circuit ensures that the load current and voltage are sinusoids at the fundamental operating frequency. Assuming the form of the output voltage, one obtains:

$$\begin{aligned} v_o(\theta) &= V_o \sin(\theta + \phi) \\ i_o(\theta) &= \frac{V_o}{R_L} \sin(\theta + \phi) \end{aligned} \quad (4-1)$$

where V_o is the peak output voltage across the load resistance R_L , and ϕ is the phase of the output waveforms.

The expression for the voltage developed across the switch can be derived by noting that while the switch is off:

$$i_c(\theta) = i_L(\theta) - i_o(\theta) \quad (4-2)$$

By substitution of the relevant expressions for the currents in (4-2), and by differentiating both sides of the resulting expression with respect to θ , we obtain:

$$\begin{aligned} \omega C_P \frac{d}{d\theta} v_s(\theta) &= \frac{1}{\omega L_{DC}} \int_{\theta_1}^{\theta} [V_{DD} - v_s(x)] dx + i_L(\theta_1) - \frac{V_o}{R_L} \sin(\theta + \phi) \\ \omega C_P \frac{d^2}{d\theta^2} v_s(\theta) + \frac{1}{\omega L_{DC}} \frac{d}{d\theta} v_s(\theta) &= \frac{V_{DD}}{\omega L_{DC}} - \frac{V_o}{R_L} \cos(\theta + \phi) \end{aligned} \quad (4-3)$$

where x is a dummy integration variable. The second expression in (4-3) can be solved for $v_s(\theta)$ using Laplace transform techniques, yielding:

$$\begin{aligned} v_s(\theta) &= V_{DD}(1 - \cos k\theta) \\ &+ \frac{k^2 X_{DC} V_o}{(1 - k^2) R_L} [\cos(\theta + \phi) - \cos\phi \cos k\theta + k \sin\phi \sin k\theta] \\ &+ k X_{DC} i_L(\theta_1) \sin k\theta \end{aligned} \quad (4-4)$$

$0 \leq \theta \leq \pi$

where:

$$k = \frac{1}{\sqrt{B \cdot X_{DC}}} = \frac{1}{\omega \sqrt{C_P L_{DC}}} = \frac{\omega_p}{\omega} \quad (4-5)$$

In (4-5), B is the susceptance of the shunt capacitor C_P , X_{DC} is the reactance of L_{DC} , ω is the operating frequency, and ω_p is the resonant frequency of L_{DC} and C_P .

From (4-4) it is apparent that the value of $i_L(\theta_1)$ (the current through the supply line inductor at the time the switch turns off) must be determined. A relationship between V_{DD} and $i_L(\theta)$ can be obtained by noting that while the switch is on $v_S(\theta) = 0$ and thus:

$$i_L(\theta) = \frac{1}{X_{DC}} \int_{\theta_2}^{\theta} V_{DD} dx + i_L(\theta_2) = \frac{V_{DD}}{X_{DC}} (\theta - \theta_2) + i_L(\theta_2) \quad \pi \leq \theta \leq 2\pi \quad (4-6)$$

An expression for $i_L(\theta_1)$ can be determined by substitution of $\theta = \theta_1 = 2\pi$ and $\theta_2 = \pi$ into (4-6) yielding:

$$i_L(\theta_1) = \frac{V_{DD}}{X_{DC}} (\pi) + i_L(\theta_2) \quad \theta_2 = \pi \quad (4-7)$$

In order to determine the value of $i_L(\theta_2)$ we proceed in the following manner. As Sokal has shown [Sokal75], optimum amplifier performance requires two conditions be met with respect to the voltage across the switch. First, the voltage across the switch must be zero at the time the switch turns on. This prevents power dissipation in discharging C_P through the switch. The second condition which must be met is that the slope of the voltage waveform is zero at the point when the switch turns on. This condition allows slight mistuning of components without a significant decrease in operating efficiency.

Kirchoff's law for the total current through L_{DC} yields:

$$i_L(\theta) = i_S(\theta) + i_C(\theta) + i_O(\theta) \quad (4-8)$$

where $i_S(\theta)$ is the current through the switch. Evaluating (4-8) at the instant of switch turn on ($\theta = \theta_2 = \pi$) one obtains:

$$\begin{aligned} i_L(\theta)|_{\theta=\pi} &= i_L(\theta_2) = 0 + \omega C_P \frac{d}{d\theta} v_s(\pi) + i_O(\pi) \\ i_L(\theta_2) &= \frac{V_o}{R_L} \sin(\pi + \phi) = -\frac{V_o}{R_L} \sin \phi \end{aligned} \quad (4-9)$$

Substitution of (4-9) into (4-6) yields the final expression for $i_L(\theta_1)$:

$$i_L(\theta_1) = \frac{V_{DD} \cdot \pi}{X_{DC}} - \frac{V_o}{R_L} \sin \phi \quad (4-10)$$

For the period when the switch is off ($\theta_1 = 0$), the current in L_{DC} is:

$$\begin{aligned} i_L(\theta) &= \frac{1}{X_{DC}} \cdot \int_{\theta_1}^{\theta} [V_{DD} - v_s(x)] dx + i_L(\theta_1) \\ &= \left[\frac{V_{DD}}{kX_{DC}} + \frac{V_o k \cos \phi}{(1-k^2)R_L} \right] \sin k\theta + \left[\frac{V_o k^2 \sin \phi}{(1-k^2)R_L} + i_L(\theta_1) \right] \cos k\theta - \frac{V_o k^2 \sin(\theta + \phi)}{(1-k^2)R_L} \end{aligned} \quad (4-11)$$

$0 \leq \theta \leq \pi$

During the period when the switch is on, the current in the shunt capacitor C_P is zero and the switch current $i_S(\theta)$ is given by the difference between $i_L(\theta)$ (for $\pi < \theta \leq 2\pi$) and the load current. As the voltage across the switch $v_S(\theta) = 0$ for $\pi < \theta \leq 2\pi$ we obtain:

$$\begin{aligned} i_S(\theta) &= i_L(\theta) - i_O(\theta) \\ &= \frac{1}{X_{DC}} \int_{\theta_2}^{\theta} V_{DD} dx + i_L(\theta_2) - \frac{V_o}{R_L} \sin(\theta + \phi) \\ &= \frac{V_{DD}}{X_{DC}} (\theta - \theta_2) + i_L(\theta_2) - \frac{V_o}{R_L} \sin(\theta + \phi) \end{aligned} \quad (4-12)$$

$\pi \leq \theta \leq 2\pi$

The current through L_{DC} ($i_L(\theta)$) during the period when the switch is closed is simply the first two terms in the third expression of (4-12). Using (4-6) to represent $i_L(\theta_2)$ in (4-12) with $\theta_2 = \pi$, we obtain:

$$\begin{aligned}
 i_L(\theta) &= \frac{V_{DD}}{X_{DC}}(\theta - \pi) + i_L(\theta_1) - \frac{V_{DC}\pi}{X_{DC}} \\
 i_L(\theta) &= \frac{V_{DD}}{X_{DC}}(\theta - 2\pi) + i_L(\theta_1) \quad \pi \leq \theta \leq 2\pi
 \end{aligned} \tag{4-13}$$

To obtain the DC component of $i_L(\theta)$, we take the average value of the piecewise continuous waveforms over the complete RF cycle.

$$\begin{aligned}
 I_{DC} &= \left[\frac{V_{DD}}{kX_{DC}} + \frac{V_o k \cos \phi}{(1-k^2)R_L} \right] \frac{1 - \cos k\pi}{2k\pi} + \left[\frac{V_o k^2 \sin \phi}{(1-k^2)R_L} + i_L(\theta_1) \right] \frac{\sin k\pi}{2k\pi} \\
 &\quad - \frac{V_o k^2 \cos \phi}{\pi(1-k^2)R_L} - \frac{V_{DD}\pi}{4X_{DC}} + \frac{i_L(\theta_1)}{2}
 \end{aligned} \tag{4-14}$$

It is readily apparent that all the design equations presented thus far are dependent on the value of the phase shift of the load current (ϕ). In order to determine the value for ϕ we rely on the conditions for optimum amplifier operation; $v_s(\theta)$ and $dv_s(\theta)/d\theta$ are both zero at the time of switch turn on ($\theta = \pi$). Using these conditions along with equation (4-4) and its derivative one obtains two expressions which are functions of $\sin \phi$ and $\cos \phi$.

The system of equations can be solved for $\cos \phi$ and $\sin \phi$ to yield expressions in terms of V_{DD} , B , k , V_o , and P_o :

$$\begin{aligned}
 \sin \phi &= \frac{-V_{DD} \cdot V_o B k (1 - k^2) (2 \sin k\pi + k\pi + k\pi \cos k\pi)}{4P_o k^2 \cdot (1 + \cos k\pi)} \\
 \cos \phi &= \frac{V_{DD} \cdot V_o B (1 - k^2) (2(1 - k^2)(1 - \cos k\pi) + k\pi \sin k\pi)}{4P_o k^2 \cdot (1 + \cos k\pi)}
 \end{aligned} \tag{4-15}$$

where:

$$P_o = \frac{V_o^2}{2R_L} \tag{4-16}$$

As the efficiency of the ideal Class E amplifier is 100% ($\eta = P_{out\ RF} / P_{in\ DC}$), the output power of the amplifier can be represented by:

$$P_o = P_{DC} = V_{DD} I_{DC} \quad (4-17)$$

Substitution of (4-14) and (4-15) into (4-17) results in a nonlinear expression in terms of output power (P_o), supply voltage (V_{DD}), shunt susceptance (B) and resonance ratio (k). The nonlinear expression (with P_o isolated) is:

$$\begin{aligned} P_o = \frac{V_{DD}^2 \cdot B}{4\pi k^2(1 + \cos k\pi)} \{ & (1 - \cos k\pi - 2k^2)[2(1 - k^2)(1 - \cos k\pi) + k\pi \sin k\pi] \\ & - [(2k^2 - 1)\sin k\pi - k\pi(1 - k^2)][2\sin k\pi + k\pi + k\pi \cos k\pi] \} \\ & + \frac{V_{DD}^2 \cdot B}{4\pi} [2 - 2\cos k\pi + 2k\pi \sin k\pi + (k\pi)^2] \end{aligned} \quad (4-18)$$

In utilization of (4-18) there are two schools of thought. The first is that since output power and supply voltage are specified parameters for practical designs, the designer substitutes the values for P_o and V_{DD} along with an estimate for the shunt susceptance (B) of the device. Under such circumstances, the positive root of (4-18) provides the value of resonance ratio (k) to be used in the design. The second method for using (4-18) is to attempt to obtain the maximum power possible from a given supply voltage and load resistance. This method requires knowledge of the value of k to use for maximum output power. The conditions for obtaining maximum power as a function of k will be examined in the next section.

Once the value of k is obtained from (4-18), the reactance value for L_{DC} is obtained using (4-5). The expression for the optimum load resistance R_L is found by using (4-15) and the relation $\sin^2 \phi + \cos^2 \phi = 1$. The resulting expression for R_L is:

$$R_L = \frac{8P_o k^4(1 + \cos k\pi)^2}{[k^2 \cdot (2\sin k\pi + k\pi + k\pi \cos k\pi)^2 + [2(1 - k^2)(1 - \cos k\pi) + k\pi \sin k\pi]^2](1 - k^2)^2} \quad (4-19)$$

To obtain the value of the residual reactance (X) one must first determine the value of ϕ , which can be represented using (4-15) as:

$$\phi = \text{atan}\left[\frac{\sin \phi}{\cos \phi}\right] = \text{atan}\left[\frac{-k(2 \sin k\pi + k\pi + k\pi \cos k\pi)}{2(1 - k^2)(1 - \cos k\pi) + k\pi \sin k\pi}\right] \quad (4-20)$$

Equation (4-20) illustrates that the phase of the output waveforms (ϕ) depends only on the resonance ratio (k).

From Figure 4-2, $v_1(\theta)$ is equal to the fundamental component of the drain voltage waveform $v_s(\theta)$ due to the filtering action of the ideal series resonant circuit L_o , C_o . As $v_1(\theta)$ is applied across $R_L + jX$ and the output current i_o flows in both R_L and jX , the value of X can be determined from a Fourier integral consisting of the quadrature component (of the fundamental) of the switch voltage. This integral for the residual reactance is:

$$X = \frac{1}{\pi} \int_0^\pi \frac{v_s(\theta) \cdot \cos(\theta + \phi)}{I_o} d\theta = \frac{R_L}{\pi V_o} \int_0^\pi v_s(\theta) \cdot \cos(\theta + \phi) d\theta \quad (4-21)$$

Equations (4-1) to (4-21) govern the operation of the ideal Class E amplifier. It is apparent from the expressions that the resonance ratio (k) plays a large role in the operating characteristics of the Class E amplifier. In this regard, one can separate the design equations into a function of k and a scaling factor. Having such 'normalized' design curves, the designer can simply scale the design to the specific frequency, supply voltage, etc. to obtain the necessary component values. In addition, the process of normalization establishes the operating points for maximum output power into a given load resistance and provides the designer with the knowledge of how the time domain waveforms vary with resonance ratio k . The normalization of the Class E design curves is a unique contribution of this thesis and was not performed by the previous authors. The following sections examine the normalization process in detail.

4.3 Normalization of the Design Equations.

The normalization of the Class E design equations provided in the previous section is undertaken to gain an understanding for how amplifier performance and component values depend on the resonance ratio (k). In addition, such normalization (or scaling) of the design equations provides the designer with the capability to produce starting points for new designs by simply scaling previous ones. In addition, optimum operating points for various amplifier configurations can be determined, evaluated and compared. The goal is to obtain a set of normalized plots detailing how the performance and component values for the ideal Class E amplifier vary with the resonance ratio (k). This analysis, has to the best of the author's knowledge, not been previously performed. As a result of the normalization process, additional information as to the optimum operating points for the Class E topology can be determined.

In order to obtain these design curves, the expressions for ϕ , output power, load resistance and peak output voltage (V_o) are separated into functions of k and scaling factors. These functions are then used in normalizing the time domain waveforms for currents and the switch voltage. The final result provides the designer with a scalable set of design curves for the ideal Class E amplifier.

For the purpose of comparing the resulting amplifier configurations, the design equations will be scaled such that the supply voltage and the load resistance are constant over the range of k considered. The variable k , is referred to as the circuits' resonance ratio as it is the ratio between the resonant frequency of L_{DC} and C_p and the operating frequency.

As the expression for ϕ , (4-20) is only a function of k , this expression requires no normalization. A plot of the variation of ϕ with k is provided in 4-4. Apparent from the

figure is the value of phi required for the RFC configured Class E amplifier of -32.48° (for $k=0$) which agrees with previous analysis [Rabb77].

FIGURE 4-4 Phi as a Function of Resonance Ratio (k)

Separation of the output power expression (4-18) results in:

$$\begin{aligned}
 P_o &= V_{DD}^2 \cdot B \cdot POF(k) \\
 POF(k) &= \frac{1}{4\pi} \left(\frac{T3 - T4}{T2} + T1 \right) \\
 T1 &= [2 - 2\cos k\pi + 2k\pi \sin k\pi + (k\pi)^2] \\
 T2 &= k^2(1 + \cos k\pi) \\
 T3 &= (1 - \cos k\pi - 2k^2)[2(1 - k^2)(1 - \cos k\pi) + k\pi \sin k\pi] \\
 T4 &= [(2k^2 - 1)\sin k\pi - k\pi(1 - k^2)][2\sin k\pi + k\pi + k\pi \cos k\pi]
 \end{aligned} \tag{4-22}$$

where the notation POF(k) represents the output power as a function of k. From (4-22) we can see that, as given, the expression for P_o is normalized with respect to B and V_{DD} and not V_{DD} and R_L as mentioned previously. However, this will be rectified shortly.

Using a similar procedure, the normalized optimum load resistance (see (4-19)) can be represented by:

$$R_L = \frac{P_o}{(V_{DD}B)^2} RLF(k)$$

$$RLF(k) = \frac{8P_o k^4(1 + \cos k\pi)^2}{[k^2 \cdot (2 \sin k\pi + k\pi + k\pi \cos k\pi)^2 + [2(1 - k^2)(1 - \cos k\pi) + k\pi \sin k\pi]^2](1 - k^2)^2} \quad (4-23)$$

Substitution of (4-22) into (4-23) results in a new expression relating R_L to the shunt susceptance B (for plot illustrating the relationship see Figure 4-5):

$$BR_L = POF(k) \cdot RLF(k) \quad (4-24)$$

FIGURE 4-5 $B \cdot R_L$ as a Function of Resonance Ratio (k)

Equation (4-22) can now be normalized in terms of V_{DD} and R_L instead of V_{DD} and B by substitution of (4-24) in place of B , yielding:

$$P_o = \frac{V_{DD}^2}{R_L} \cdot (POF(k))^2 RLF(k) \quad (4-25)$$

For the normalized case ($V_{DD}=1\text{ V}$ $R_L=1\Omega$), the variation of output power with resonance ratio k is plotted in Figure 4-6.

FIGURE 4-6 P_o as a Function of Resonance Ratio (k)

From Figure 4-6 it is readily apparent that maximum output power for a given load resistance occurs for a value of $k = 1.416$, indicating that the use of an RFC ($k=0$) is not desirable. In addition, the relationship between the shunt susceptance B , and the load resistance R_L , provides a constraint on the values of X_{DC} . The relationship between X_{DC} and R_L is provided in equation (4-26) and Figure 4-7.

$$X_{DC} = \frac{1}{Bk^2}$$

$$\frac{X_{DC}}{R_L} = \frac{1}{BR_L k^2}$$

(4-26)

FIGURE 4-7 X_{DC}/R_L as a Function of Resonance Ratio (k)

As the quality factor of the series tuned output network is assumed infinite, the output power is simply the square of the peak output voltage divided by two times the load resistance. As such the normalized peak output voltage waveform can be represented by:

$$\begin{aligned}
 V_o &= \sqrt{2R_L \cdot P_o} \\
 &= \sqrt{2 \frac{V_{DD}^2}{R_L} (POF(k))^2 RLF(k) R_L} \\
 &= V_{DD} \cdot POF(k) \cdot \sqrt{2 \cdot RLF(k)} \\
 &= V_{DD} \cdot VOF(k)
 \end{aligned}
 \tag{4-27}$$

From (4-27) one can see that the peak output voltage is directly proportional to the supply voltage (for a given value of k). This fact is useful in Class E amplifiers which are used in modulation schemes exhibiting envelope variations such as $\pi/4$ DQPSK, QPSK, etc. In such applications the modulated signal can be separated into an amplitude modulated component (the envelope variation) and a phase/frequency modulated component. The non-linear Class E amplifier amplifies the phase/frequency modulation efficiently and then the amplitude variations are applied through modulation of the power supply of the Class E stage. The linear relationship between V_o and V_{DD} prevents conversion of AM to PM within the amplifier. A plot illustrating the variation of normalized peak output voltage with respect to k is provided in Figure 4-8.

FIGURE 4-8 Peak V_o as a Function of Resonance Ratio (k)

Equation (4-10) for $i_L(\theta_1)$ describes the current through the supply inductor at the time the switch turns off. Normalization of $i_L(\theta_1)$ yields:

$$\begin{aligned}
 i_L(\theta_1) &= \frac{V_{DD} \cdot \pi}{X_{DC}} - \frac{V_o}{R_L} \sin \phi \\
 i_L(\theta_1) &= V_{DD} k^2 B \pi - \frac{V_{DD}}{R_L} VOF(k) \sin \phi \\
 i_L(\theta_1) &= \frac{V_{DD}}{R_L} [\pi k^2 POF(k) RLF(k) - VOF(k) \sin \phi] \\
 i_L(\theta_1) &= \frac{V_{DD}}{R_L} IL\theta_1 F(k)
 \end{aligned}
 \tag{4-28}$$

A plot of the relationship between $IL\theta_1 F(k)$ and k is provided in Figure 4-9.

FIGURE 4-9 $IL\theta_1$ as a Function of Resonance Ratio (k)

The normalized function for IDC is obtained in a similar manner using (4-14) and (4-28) with a plot of the relationship provided in Figure 4-10:

$$I_{DC} = \frac{V_{DD}}{R_L} IDC F(k)$$

$$IDCF(k) = T1 \cdot T2 + T3 \cdot T4 + T5$$

$$T1 = kPOF(k)RLF(k) + \frac{kVOF(k)\cos\phi}{(1-k^2)}$$

$$T2 = \frac{1 - \cos k\pi}{2k\pi}$$

(4-29)

$$T3 = \frac{k^2VOF(k)\sin\phi}{(1-k^2)} + IL\theta_1 F(k)$$

$$T4 = \frac{\sin k\pi}{2k\pi}$$

$$T5 = \frac{-k^2VOF(k)\cos\phi}{\pi(1-k^2)} - \frac{k^2\pi POF(k)RLF(k)}{4} + \frac{IL\theta_1 F(k)}{2}$$

FIGURE 4-10 IDC as a Function of Resonance Ratio (k)

Obtaining the time domain waveforms in terms of a scaling factor and a function of k continues in a similar fashion except that these functions also contain θ . These functions

are plotted with respect to θ with representative values of k used as a parameter. The normalized form for the voltage across the switch is obtained using (4-4) and substituting (4-28) for $i_L(\theta_1)$:

$$\begin{aligned}
 v_s(\theta) &= V_{DD} VSF(k) \\
 VSF(k) &= T1 + T2 + T3 \\
 T1 &= 1 - \cos k\theta \\
 T2 &= \frac{VOF(k)[\cos(\theta + \phi) - \cos\phi \cos k\theta + k \sin\phi \sin k\theta]}{POF(k)RLF(k)(1 - k^2)} \\
 T3 &= \frac{\sin k\theta \cdot IL\theta_1 F(k)}{k \cdot POF(k)RLF(k)}
 \end{aligned} \tag{4-30}$$

The plot of $v_s(\theta)$ as a function of k and theta is plotted in Figure 4-11 for representative values of k .

FIGURE 4-11 VSF(k) as a Function of theta for $k=[0.5, 1.1, 1.4, 1.7]$

The normalized form for the current in L_{DC} is obtained by normalizing the expressions for $i_L(\theta)$ in each operating region and then plotting the normalized curves in the applicable region of the RF cycle. The boundary condition between the two regions is evaluated to ensure that the resulting waveform is continuous. The normalized form for $i_L(\theta)$ while the switch is off (i_{Loff}) is determined from (4-11) as:

$$\begin{aligned}
 i_{Loff}(\theta) &= \frac{V_{DD}}{R_L} IL_{OFF} F(k) \\
 IL_{OFF} F(k) &= T1 + T2T3 + T4 \\
 T1 &= POF(k)RLF(k) \cdot k \sin k\theta \\
 T2 &= \frac{k^2 VOF(k)}{(1 - k^2)} \\
 T3 &= \left[\frac{1}{k} \sin k\theta \cos(\phi) + \cos k\theta \sin \phi - \sin(\theta + \phi) \right] \\
 T4 &= IL\theta_1 F(k) \cos k\theta
 \end{aligned} \tag{4-31}$$

Using (4-13) a normalized expression for $i_L(\theta)$ for the period the switch is on can be determined as:

$$\begin{aligned}
 i_{Lon}(\theta) &= \frac{V_{DD}}{R_L} IL_{ON} F(k) \\
 IL_{ON} F(k) &= [k^2 \cdot POF(k)RLF(k) \cdot (\theta - 2\pi)] + IL\theta_1 F(k)
 \end{aligned} \tag{4-32}$$

As (4-31) and (4-32) are only valid in their respective portions of the RF cycle and are assumed to be zero during the remaining portion of the RF cycle, the overall expression for $i_L(\theta)$ is just the sum of (4-31) and (4-32), evaluated at each value of θ . Both expressions provide the same result for $\theta = \pi$ and therefore the waveform is continuous. As a result, the normalized form for $i_L(\theta)$ can be represented as:

$$\begin{aligned}
 i_L(\theta) &= \frac{V_{DD}}{R_L} IL_{OFF} F(k) + \frac{V_{DD}}{R_L} IL_{ON} F(k) \\
 i_L(\theta) &= \frac{V_{DD}}{R_L} [IL_{OFF} F(k) + IL_{ON} F(k)] \\
 i_L(\theta) &= \frac{V_{DD}}{R_L} ILF(k)
 \end{aligned} \tag{4-33}$$

A plot of $ILF(k)$ as a function of resonance ratio k is illustrated for representative values of k in Figure 4-12.

FIGURE 4-12 $ILF(k)$ as a Function of θ for $k=[0.5, 1.1, 1.4, 1.7]$

It is apparent from Figure 4-12 that for certain values of k , the instantaneous current flowing in the supply line inductor is negative. The minimum point in the $i_L(\theta)$ curve occurs at a point equal to 39% of the RF period as established by Li and Yam [Li94]. From the figure it can be seen that as k increases past a certain point ($k=1.1597$) the current in the inductor is negative for a portion of the RF cycle. Since the maximum and minimum points are fixed in time, the increasingly negative current can result in an

increased rate of change of the inductor current and thus higher voltages across the switch during the off period. If the designer is not careful, damage to the active device may result from reverse breakdown. In fact, the expressions for $v_S(\theta)$ take this into account. From the designer perspective, if the difference between the maximum value of $v_S(\theta)$ and the value of the drive signal in the off state does not exceed the device breakdown voltage, the amplifier will function and no damage to the transistor will result.

Normalization of the remaining time domain current waveforms ($i_S(\theta)$, $i_C(\theta)$, and $i_O(\theta)$) proceeds in a similar fashion. As the expression for $i_O(\theta)$ appears in the other currents its normalized form is determined first. Substitution of (4-27) for V_o in (4-1), $i_O(\theta)$ becomes:

$$i_O(\theta) = \frac{V_{DD}}{R_L} VOF(k) \sin(\theta + \phi)$$

$$i_O(\theta) = \frac{V_{DD}}{R_L} IOF(k)$$
(4-34)

A plot illustrating the variation of output current for representative values of k is provided in Figure 4-13.

FIGURE 4-13 IOF(k) as a Function of theta for $k=[0.5, 1.1, 1.4, 1.7]$

From Figure 4-13 it is apparent that the maximum output power into the fixed load resistance (1Ω in the normalized curves) occurs (for the plotted values of k) at $k=1.4$.

The normalization for $i_s(\theta)$ is determined from (4-13) and (4-34) after substitution for X_{DC} and V_o as:

$$\begin{aligned}
 i_s(\theta) &= \frac{V_{DD}}{X_{DC}}(\theta - 2\pi) + i_L(\theta_1) - \frac{V_o}{R_L} \sin(\theta + \phi) \\
 i_s(\theta) &= \frac{V_{DD}}{R_L} ISF(k) \\
 ISF(k) &= k^2 POF(k) RLF(k)(\theta - 2\pi) + IL\theta_1 F(k) - VOF(k) \sin(\theta + \phi)
 \end{aligned} \tag{4-35}$$

A plot illustrating the relationship between the switch current and resonance ratio k is provided in Figure 4-14.

FIGURE 4-14 $ISF(k)$ as a Function of θ for $k=[0.5, 1.1, 1.4, 1.7]$

As the current flowing in the shunt capacitor is (in its most general form) $i_C = i_L - i_S - i_O$, the normalized form for $i_C(\theta)$ is obtained without any additional manipulations from equations (4-33) to (4-35) as (for plot of relationship see Figure 4-15):

$$\begin{aligned}
 i_C(\theta) &= i_L(\theta) - i_S(\theta) - i_O(\theta) \\
 i_C(\theta) &= \frac{V_{DD}}{R_L} ILF(k) - \frac{V_{DD}}{R_L} ISF(k) - \frac{V_{DD}}{R_L} IOF(k) \\
 i_C(\theta) &= \frac{V_{DD}}{R_L} [ILF(k) - ISF(k) - IOF(k)] \\
 i_C(\theta) &= \frac{V_{DD}}{R_L} ICF(k)
 \end{aligned} \tag{4-36}$$

FIGURE 4-15 $ICF(k)$ as a Function of θ for $k=[0.5, 1.1, 1.4, 1.7]$

The final expression requiring normalization is that for the residual reactance present in the series tuned output circuit (jX) in Figure 4-2, on page 62. From (4-21) with appropriate substitutions for V_o and $v_S(\theta)$ one can obtain:

$$\begin{aligned}
 X &= \frac{R_L}{\pi V_o} \int_0^\pi v_S(\theta) \cdot \cos(\theta + \phi) d\theta \\
 X &= \frac{R_L}{\pi V_{DC} VOF(k)} \int_0^\pi V_{DD} VSF(k) \cos(\theta + \phi) d\theta \\
 X &= \frac{R_L}{\pi VOF(k)} \int_0^\pi VSF(k) \cos(\theta + \phi) d\theta \\
 X &= R_L \cdot XF(k)
 \end{aligned} \tag{4-37}$$

The residual reactance is therefore simply the integral of the normalized voltage across the switch scaled proportionally with the load resistance. The relationship between X and the resonance ratio is illustrated in Figure 4-16.

FIGURE 4-16 $XF(k)$ as a Function of Resonance Ratio (k)

From Figure 4-16 it is apparent that for values of k between zero and one there is a significant residual reactance component (approximately 1). As X scales with R_L , this implies that for the lower values of k , X and R_L are of the same order of magnitude. This results in significant portion of the power available in the switch voltage waveform being used reactively in jX . As such the real output power (dissipated in the load) is less than optimum. In order to maximize the output power the designer must ensure the amplifier operates with a value of k which requires zero residual reactance ($k=1.412$). Also of note is the requirement for residual (capacitive) reactance for values of k exceeding 1.412.

Equations (4-22) to (4-37) provide the designer with normalized forms for the expression governing the ideal Class E power amplifier. The plots of the normalized functions provide the designer with the capability to quickly determine the component values for an ideal amplifier based on particular set of design constraints. Appendix A includes a complete set of normalized design curves for easy reference.

In reality we can never achieve the conditions of ideality upon which the preceding analysis is based, as will be discussed subsequently.

4.4 Issues Affecting the Validity of the Ideal Class E Analysis

In a real amplifier the active device operating as the switching element has finite on resistance, non-infinite off resistance and non-zero switching times. In addition, the output capacitances of real active devices are functions of the instantaneous applied voltages, introducing nonlinearity and time variation into the value of shunt capacitance (C_p). Consideration of these issues has generally been avoided in the previous analysis of Class E amplifiers, in order to simplify the problem and obtain tractable analytic expressions. The analysis is meant as a method of putting the designer in the "ballpark", followed by circuit simulations and optimization to refine the design.

In designing a Class E amplifier, one must determine the size of the active device to be used. This selection process is the result of a trade off between a large device (which minimizes on resistance but results in increased device capacitances) and a small device (which has smaller capacitances but larger on resistance). Simply put, there is a trade off between the input impedance of the device and the devices' switching performance. An additional consideration is the requirement to drive the Class E with a square wave input. As the devices' input capacitance increases there is an effective shorting of the higher

frequency components of the square wave. This limits the effectiveness of the Class E amplifier to conditions of lower power (at higher frequencies) or higher powers (at lower frequencies). The ability to obtain simultaneous high frequency and high output power is questionable.

The analysis also assumes that the load quality (Q) factor is infinite. This assumption simplifies the analysis in that only the fundamental of the drain voltage waveform reaches the load. The ideal amplifier, if provided with a load network having high loaded Q (Q_L), will not function correctly. The transient response of the load network doesn't allow the optimum conditions of $v_S(\theta) = 0$ and $dv_S(\theta)/dt = 0$ at switch turn on time to occur. As such, the amplifier has significant voltage across the switch at turn on time, and power dissipation increases. In order to achieve results which are in the realm of those provided by the ideal analysis, one must reduce the Q factor of the load network, insert an additional filter between the series tuned output network and the load, and adjust the rise and fall times on the input drive waveform. These aspects of the design will be examined in the design example outlined in the following section.

4.5 Design Example: Ideal Class E Amplifier

Now that expressions governing the operation on an ideal Class E amplifier have been derived and normalized, one must check to determine if the results of these expressions are in line with simulations.

In this regard, a test case was developed, to verify the expressions and graphical plots presented thus far with a HSpice simulation based on an ideal switch (not a transistor). As mentioned in section 4.2, there are two schools of thought in terms of using the design expression. The first is to design the amplifier based on design constraints with respect to supply voltage and output power. The second is to design based on obtaining the

maximum output power into a given load resistance based on the constraint of supply voltage. This design example is based on the second method. The test case amplifier was to operate at 835MHz into a 50 ohm load. The design procedure is as follows. To obtain maximum power into a 50 ohm load, we must determine the value of the resonance ratio k to use in the design. From Figure 4-6 one can see that the maximum output power occurs for k at approximately 1.4. Using the exact solution for the point of maximum output power gives $k=1.412$. Using the design curves (Figures 4-4 to 4-16) one obtains the following values for the design example using a desired k of 1.412.

TABLE 4-1 Design Values for $k=1.412$

Parameter	Figure	Equation	Normalized Value @ $k=1.412$	Normalizing Factor	Unnormalized Result
P_o	4-6	(4-25)	1.36	VDD^2/RL	3.3 Watts
B	4-5	(4-24)	0.6845	$1/RL$	13.7 mS
V_o	4-8	(4-27)	1.65	VDD	18.15 V
$IL(\theta_1)$	4-9	(4-28)	1.86	VDD/RL	409.2 mA
IDC	4-10	(4-29)	1.36	VDD/RL	299.2 mA
Φ	4-4	(4-20)	15.2 °	1	15.2 °
X	4-16	(4-37)	0	RL	0 Ω
$v_S(\theta)$ max	4-11	(4-30)	3.65	VDD	40.15 V
$i_S(\theta)$ max	4-14	(4-35)	3.61	VDD/RL	794.2 mA
$i_L(\theta)$ max	4-12	(4-33)	3.99	VDD/RL	877.9 mA
$i_L(\theta)$ min	4-12	(4-33)	-1.06	VDD/RL	-233.2 mA
$i_C(\theta)$ max	4-15	(4-36)	3.42	VDD/RL	752.4 mA
$i_C(\theta)$ min	4-15	(4-36)	-2.01	VDD/RL	-442.2 mA
$i_O(\theta)$ max	4-13	(4-34)	1.65	VDD/RL	363 mA

From the data in Table 4-1, the design plots and equations in this chapter, the component values for the Class E amplifier can be determined. The values for the components are as follows: $C_p=2.6\text{pF}$, $L_{DC} = 7\text{nH}$, and $RL=50\Omega$. The components L_o and C_o (refer to Figure 4-2) remain to be determined based on the designers selection of load quality factor (Q_L). Obviously, there is a trade-off to be made with respect to loaded Q .

4.5.1 Impact of Load Quality Factor (Q_L) on Amplifier Performance

If the selected component values for L_o , C_o , and R_L produce too high a loaded Q , long ringing transients can be expected. On the other hand, selecting Q_L too low will result in harmonic distortion in the load as harmonic currents are free to flow. Sokal has shown [Sokal80] that the minimum value for loaded Q is 1.7879. Simulations were conducted on the ideal Class E amplifier the component values determined in the previous section and various values of loaded Q . The values of loaded Q , component values and output power are tabulated in Table 4-2. Simulation plots (Figure 4-18) illustrate the impact of loaded Q on the time domain waveforms and the output power achievable.

TABLE 4-2 Impact of Loaded Q on Ideal Class E Amplifier

Q_L	L_o [nH]	C_o [pF]	P_{out} [W] ¹	$P_{in DC}$ [W]	Drain Efficiency η^2
50	476	0.076	1.03	1.1885	0.545
10	95.3	0.382	3.16	3.318	0.953
5	47.4	0.763	3.33	3.44	0.966
2	19.1	1.91	3.39	3.658	0.926

1. P_{out} is computed for the fundamental frequency in the output current.

2. η is computed as $P_{out}(RF) / P_{inDC}$

It is apparent from the table that selection of load Q significantly impacts amplifier performance. In addition, the selection of a 50Ω load limits the value of loaded Q which can be realized using standard surface mount components. For loaded Q higher than 5, the value for C_o becomes increasingly small. The impact of using such a low Q is that significant harmonic components can flow in the load if a filter stage is not included in the design. Figure 4-18 illustrates the simulation results when Q_L is higher and lower than optimum. In the event that Q_L is too high, the voltage across the switch falls below zero and thus the stored charge is dissipated when the active device turns on reducing efficiency. If Q_L is too low, the voltage across C_p cannot fall to zero before the switch

turns on, again reducing the efficiency. Simulations determined that for the 50Ω load, the optimum value of Q_L is ~ 5 . For amplifier operation with low values of loaded Q , a parallel LC filter should be installed in parallel with RL to reduce harmonic levels in the output to acceptable levels. In addition to the loaded Q of the amplifier, the transition time on the input has significant impact on amplifier performance.

FIGURE 4-17 Impact of Loaded Q on the Class E Amplifier

4.5.2 Impact of Drive Waveform Transition Times on Amplifier Performance

As the Class E stage is a switching amplifier it requires a driver with fast transitions to ensure efficient operation. Simulations were conducted on the ideal Class E amplifier

FIGURE 4-18 Impact of Drive Waveform Transition Times on the Class E Amplifier

using the optimum value of Q_L with different values of rise and fall times on the input

As we can see from Figure 4-18, the rise and fall time of the drive waveform has a significant effect on the amplifier's performance. Increasing the rise and fall time of the input waveform effectively increases the period of time the device is off resulting in an apparent increase in the duty cycle. As Sokal has shown [Sokal75] the maximum output power is obtained when using a 50% duty cycle. As a result, increased transition times on the input significantly reduce the output power and amplifier efficiency.

Now that we have evaluated the normalized design curves and shown that simulations (of the ideal Class E amplifier agree with the predications) the design of the driver stage can be examined.

5.1 Introduction

As mentioned in Chapter 2, the Class F amplifier achieves higher efficiency by controlling the harmonic content of the drain voltage and current waveforms to reduce the period of time when both exhibit large instantaneous values. In the standard Class F amplifier, the goal is to achieve a sinusoidal output at a higher power level than the input. Figure 5-1 illustrates the schematic for the standard Class F amplifier topology.

FIGURE 5-1 Class F Amplifier: Standard Topology

In the standard topology, two tuned circuits are provided to control the harmonic content of the drain waveforms. As a result of the fundamental (consisting of C1 and L1) and third harmonic tank circuits (C3 and L3), the drain of the device “sees” impedance at only the

fundamental and third harmonics of the input signal yielding a drain voltage waveform containing these harmonic components. The drain current flowing as a result of the current harmonics identified in Figure 5-1 exhibits a pulse like shape. From Figure 5-2 it is easy to identify the reason for the increased efficiency, the drain current is low (~ 0) during the period when the drain voltage is high.

FIGURE 5-2 Class F Amplifier Typical Waveforms

For the current application, driving a Class E amplifier, the standard Class F topology is not suitable. From the discussion in the previous chapter, the impact of the input signal rise time on the Class E amplifier performance is significant. The output of the Class F must resemble a square wave to ensure fast switching on the input of the Class E stage.

The topology illustrated in Figure 5-3, provides the means of generating an approximation to the desired square wave.

FIGURE 5-3 Class F Amplifier Topology for Square Wave Generation

The tuned circuits in the modified topology are both located on the drain and provide a high impedance at the fundamental and third harmonic. As a result, the current flowing in the load resistance consists of the fundamental and third harmonic components. As the tank circuits, provide (ideally) zero impedance at all harmonics other than the fundamental and the third, the drain and output voltage waveforms are approximate square waves.

Initially, it might seem that the use of a Class F amplifier to generate the necessary square wave drive for the Class E stage could be avoided through the use of digital logic or a diode based clipping circuit.

The main problem with using digital logic gates to generate the square wave drive is that the power dissipation in such a stage would be significant at higher frequencies. The power dissipated in such a circuit, consists of the power dissipated in charging and discharging the node and load capacitances for the gate and increases proportionally to the operating frequency and the square of the supply voltage. In addition, the input to the gate is a sine wave and results in large power dissipation during the switching operation of the

gate when both the pull-up and the pull-down devices are on. In addition, the current state of the silicon carbide technology available for this project, (die transistors, depletion mode only) makes the fabrication of any reasonable logic gate structure overly complex. In addition, the high-voltage nature of the technology implies that the switching power dissipation in such a device would be extremely high (the difference between a 5v and 20v supply results in 16 times the power dissipation). In light of these issues, the option of generating a square wave by means of digital logic was discarded.

The use of a diode based clipping circuit was also considered to generate the required square wave. The main drawback to this approach is that a significant amount of the power present in the input sine wave is wasted in the generation of the square wave. This is due to the necessity for a large amplitude input sine wave to provide fast rise and fall times for the clipped square wave. Figure 5-4 illustrates the situation for two sinusoidal input waves exhibiting different amplitudes and a sample circuit capable of generating the waveforms based on zener diodes. The first input wave has a low peak amplitude

FIGURE 5-4 Generation of a Square Wave Through Diode Clipping

(just above the clipping level for the diodes). We can see from the corresponding square wave plot (bottom panel), that the resultant “square” wave has large rise and fall times. The second input sine wave has a larger amplitude and the resulting square wave has much shorter transition times. The portion of the input wave which is wasted in the generation of the output is shaded in the figure. Fast transitions require a large input swing and resulting large power consumption. As a result of this, the use of a diode clipping circuit to generate the necessary square wave drive for the Class E amplifier was discarded. In addition, the present state of the silicon carbide technology does not provide for the diode structures necessary to create such a clipping circuit.

Use of a Class F amplifier to generate the required square wave input for the Class E stage doesn’t have the problems associated with the digital logic or diode clipping methods. The Class F amplifier is itself an efficient topology and can be fabricated using the available silicon carbide devices. The following sections examine the method for designing a Class F amplifier to generate a square wave and the difficulty in using a Class F amplifier to drive a square wave into a Class E amplifier.

5.2 Design of a Square Wave Generating Class F Amplifier

As previously mentioned, the task of the Class F amplifier is to generate the square wave drive for the Class E stage to provide fast switching and hence high efficiency. Since a square wave consists of odd harmonics of the switching frequency it raises the question as to how a square law device is capable of generating the desired harmonics. For all FET type devices (MOSFETs, JFETs, and MEFETs) the drain current (in the linear region) is proportional to the square of the voltage by which the device is turned on. In mathematical terms:

$$I_D \propto (V_{GS} - V_P)^2$$

$$I_D \propto (V_{DC} + V_{SIG} \sin \omega t - V_P)^2 \quad (5-1)$$

where $V_{GS} = V_{DC} + V_{SIG} \sin \omega t$ is the value of the drive signal on the device, V_{DC} is the DC bias value and V_P is the pinch voltage. Expanding (5-1), one obtains an expression containing a DC component, the fundamental and the second harmonic. No higher order harmonics are produced as a result of this analysis. In a real device, however inherent nonlinearities generate other harmonic current and voltage components. In addition, if the drive signal on the device is such that it leaves the linear region and drops into triode operation, drain current harmonic components can be significant. It is through these means that the Class F amplifier based on square law devices is capable of generating a square wave. Table 5-1 indicates the harmonic components generated as a result of driving a SiC MESFET device with various input signal amplitudes. For the simulations, the MESFET was biased for Class A operation with a supply voltage of 20V. For the device in question, the pinch voltage is -9.4V and the load resistance was set at 1k Ω . The DC bias current was set at 10mA. This results in a DC bias of 10V at the drain of the active device. It is apparent from the table that for small input signal amplitudes the device operates well into the linear region and the drain voltage contains minimal harmonic content.

TABLE 5-1 Harmonic Generation in a Square Law Device

Peak Drive Level	Drain Voltage Harmonic Components						
	1		2		3		Ratio V3/V1
	Magnitude	Phase	Magnitude	Phase	Magnitude	Phase	
0.1 V	0.799	166.5	5.005e-3	66.8	4.997e-5	-30.0	62.5e-6
0.5 V	3.982	166.3	1.238e-1	66.6	9.609e-3	175.1	2.41e-3
1.0 V	7.753	165.9	4.448e-1	70.6	9.021e-2	150.7	11.6e-3
1.6 V	9.932	167.7	4.716e-1	153.9	8.687e-1	144.3	87.4e-3

As the input signal rises to the point where the magnitude of the drain voltage swing approaches the DC drain bias level, the device falls into the triode regime and significant harmonic components are generated. Of specific concern is the amplitude and phase of the third harmonic relative to the fundamental. From the table we see that for an input signal of 1.6V peak, the device is driven hard enough that it operates in the triode region for a portion of the cycle. In this case the amplitude of the third harmonic exceeds that of the second and its magnitude is roughly 1/9th of the magnitude of the fundamental. In addition, the phase relationship of the two harmonics are reasonably close. This is the desirable situation for generation of a square wave.

A simulation was conducted using the modified Class F topology to ensure that it was capable of driving the square wave into a resistive load. The schematic for the test circuit is illustrated below with the component values indicated.

FIGURE 5-5 Square Wave Class F Driving a Resistive Load

The drive waveform $V_S = V_{BIAS} + V_{SIG} * \sin(2\pi ft)$, where f is 835MHz, $V_{BIAS} = -7.35V$ and $V_{SIG} = 1.6V$ peak. The tank circuits are tuned to provide a large impedance at 835 and 2505 MHz. The results of the simulation, showing the drain voltage and current waveforms along with FFT data for the waveforms, is shown in Figure 5-6. The drain voltage waveform has been “squared off” by the third harmonic component. We can see

from the figure that the drain voltage is at its maximum while the drain current is at its minimum accounting for higher efficiency. In addition, the FFT data clearly indicate the harmonic components of the drain voltage and that their relative magnitudes differ by a factor of ~ 9 (the desired value). The drain current waveform contains a DC component in addition to all harmonics exhibiting declining magnitudes.

FIGURE 5-6 Simulated Square Wave Class F Waveforms

While the Class F amplifier is capable of driving its square wave into a resistive load, most situations require the driving of a capacitive load (i.e. the input of another amplifier stage). In this case the topology must be adjusted to take into account the additional capacitance.

If we consider the impedance of the load circuit for the Class F amplifier in linear terms we can incorporate any load capacitance into the tank circuits as shown in Figure 5-7.

FIGURE 5-7 Load Impedance Seen by the Class F Amplifier

From a signal perspective, the twin tank circuits are in parallel with CDS. Assuming that CDS is linear (no varactor effects) and that the DC blocking capacitor is ideal, the tank circuits are also in parallel with RL and CL. Under these conditions the impedance seen by the drain of the active device can be maintained by reducing the value of both C1 and C3 by $(CDS + CL)$. In the event that the load capacitance is nonlinear, transient simulation is required to adjust the tank component values for optimum performance as the linear simplification provided above is no longer valid.

5.3 Difficulties Driving Non-Linear Capacitances With the Class F Amplifier

While it was shown in the previous section that driving a square wave into a resistive load or a linear reactive load is possible, by appropriate tuning of the tank resonances, driving a nonlinear load impedance is complicated. This section examines these issues in the design of the Class F and Class E amplifiers.

The input impedance of the Class E amplifier is difficult to determine for a variety of reasons. First is the fact that the input impedance is nonlinear. As the gate-source and gate-drain capacitances are depletion capacitances, their value is time dependent on the applied voltage. In this regard, the input impedance is time dependent. Secondly, we are concerned with the input impedance of the Class E amplifier, not at a single frequency but at “all” harmonics of the input frequency. Finally, the device is not unilateral and the load impedance at the drain is coupled back to the input. These issues combine to make the determination of the input impedance all but impossible.

Unlike small signal amplifiers, AC analysis will not provide the input impedance with any accuracy because it assumes the device is linear around the bias point. Small signal AC analysis is based on sweeping the input frequency (at a fixed amplitude) and measuring the Z matrix parameters. In the case of a square wave input, each harmonic component has a different amplitude and phase. Performing multiple AC analyses using the different components of the input square wave will not provide a suitable answer because the DC bias point cannot be correctly established in each case, as all the other harmonic components interact through the device nonlinearities to produce a time dependent bias point. For a power amplifier, the large signal swings exercise the active device over a large portion of its characteristics each cycle and thus a single bias point solution is not accurate. In effect the bias point is continuously shifting during the RF cycle.

As the input impedance is nonlinear, we cannot simply partition the input impedance into individual harmonic terminations. Superposition cannot be applied in this case. The question remains as to how to determine the input impedance. As Maas has explained [Maas88], a true input impedance for a nonlinear circuit cannot be defined due to the fact that the term impedance implies a ratio of V/I which is independent of voltage or current magnitude. However, he also points out that a quazi-impedance can be determined which relates voltage to current at a given input level and frequency. This is the method used in this thesis.

If we treat the amplifier as a one port “black box” and provide it with the required bias and input drive signals to place it in its operational mode, we can observe the current and voltage waveforms at its input as functions of time. Using the FFT we can reduce these time functions to their frequency domain equivalents. We take the ratio of the Fourier series components for voltage and current to determine the apparent quasi-impedance seen at each harmonic. The impedance levels are the apparent impedances at those harmonics due to any and all interactions within the nonlinearities of the device and are determined under the actual drive/operating conditions for the amplifier. This is much the same as looking at the global IV characteristics for the network, similar to what is done in harmonic balance analysis.

Using the methods outlined in Chapters 4 and 5 a Class E amplifier with its associated Class F driver stage was designed. The details of this design work are examined in the next chapter.

Design, Simulation and Measurement of the Class E & F Amplifier Stages

6.1 Introduction

This chapter describes the design process for the Class E and Class F amplifier stages using the methodology outlined in Chapters 4 and 5. First the specification for the final amplifier will be reviewed as will the active device and substrate material properties. The Class E amplifier design will then be covered including device sizing and simulation. The Class F amplifier design will then be described. The impact of parasitics on the design will be examined. Simulation data for the completed amplifier will then be provided followed by measured amplifier performance. Finally, the measured and simulated data will be compared and evaluated.

6.2 Active Device and Substrate Properties

In order to design the amplifier stages some information on the capabilities of the active devices and the substrate are required. The properties are fundamental in determining amplifier performance and are examined in the following sections.

6.2.1 Silicon Carbide MESFET Characteristics

Simulations of a unit size silicon carbide MESFET device were conducted to determine the IV characteristics for the device. Once this set of curves was available it could be scaled for use with larger devices.

The unit size MESFET consists of a single gate finger having a gate length of $0.7\mu\text{m}$ and a (finger) length of $250\mu\text{m}$. This device is referred to as a 1X250 device (1 finger X $250\mu\text{m}$). The simulated IV characteristics for this device are illustrated in Figure 6-1.

FIGURE 6-1 IV Characteristics for a 1X250 SiC MESFET

It is apparent from the figure that the pinch off voltage for the device is approximately -9V (negative as the SiC MESFET is depletion mode device). In fact, the pinch off voltage is -9.37V . The implication of a large pinch voltage is that for the Class E stage a large drive

signal swing is required to switch the device. In addition, this large signal swing must have a fast transition times to maximize the performance of the Class E stage.

An additional characteristic which provides a constraint on the supply voltage for the Class E amplifier is the device breakdown voltage. As mentioned in Chapter 3, the breakdown voltage between the drain and source is $\approx 100\text{V}$ for silicon carbide devices. We will use this information when we determine the active device sizes and the supply voltage in a following section.

6.2.2 TMM3 Board / Substrate Properties

The material properties of the substrate also impact the amplifier design. For this project the substrate material is TMM3, a ceramic thermoset polymer composite (doped teflon). TMM3 is used for high reliability microstrip applications. The substrate properties of concern are its thickness and dielectric constant, as these determine the parasitic capacitances and guided wavelength for signals on the board. Material properties for the TMM3 material are provided in Table 6-1.

TABLE 6-1 TMM3 Substrate Material Properties [Best97]

Property	Units	Value
Thickness	μm	375
Relative Dielectric Constant ϵ_r	---	3.27
Thermal Conductivity @ 25°C	W/cm/°K	68

The TMM3 substrate material is epoxied to an 6.4mm thick aluminum plate to provide a ground plane and heat sink. The aluminum plate also provides a rigid foundation for the substrate material to prevent any flexing as the substrate temperature changes.

As the design will employ individual transistor die, the die have to be mounted in a socket milled out of the substrate material. Figure 6-2 illustrates the method by which the SiC

transistor die will be attached to the TMM3 substrate material. From the views provided in Figure 6-2 it is apparent that the hybrid design will require that the terminals of the MESFET devices be bond wired to the transmission line tracks on the substrate material. This implies that bond wire inductances will be a significant component in the performance of the amplifier and will have to be accounted for in the design.

FIGURE 6-2 Attachment of SiC Transistor Die to TMM3 Substrate

As mentioned previously, the dielectric constant of the substrate material determines the guided wavelength of signals propagating on transmission lines formed on the substrate. In the Class F/ Class E topology chosen for this work the main frequencies of concern are the fundamental and third harmonic. The guided wavelength is determined at those frequencies using:

$$\lambda_G = \frac{c}{\sqrt{\epsilon_r} \times f_o}$$

$$\lambda_{G3} = \frac{\lambda_G}{3} \quad (6-1)$$

In (6-1), λ_G is the guided wavelength at the fundamental, λ_{G3} is the guided wavelength at the third harmonic, c is the speed of light (3e8m/s), f_o is the highest operating frequency in the band of interest (849MHz) and ϵ_r is the relative dielectric constant (3.27). Solving (6-1), we obtain $\lambda_G=195\text{mm}$ and $\lambda_{G3}=65\text{mm}$. From microwave theory we know that for transmission lines less than one tenth of a guided wavelength their distributed effects can be neglected. In this case, the distributed effects of the transmission lines can be neglected for lengths less than 19.5mm (@ 835MHz) and 6.5mm (@2505MHz). The design goal will be to keep transmission line lengths less than these values.

Now that we have available information on the IV characteristics for the active devices and the substrate material, the amplifier design can be examined. As the Class E amplifier stage is the heart of the high-efficiency amplifier, its design is analyzed first.

6.3 Class E Amplifier Design

In designing the high-efficiency amplifier, the data obtained in the design example in Chapter 4 provides the starting point. Using this information, a Class E amplifier is designed and optimized. Following this the Class F driver amplifier is designed to provide the proper switching drive to the Class E. The impact of board level capacitive and inductive (bonding) parasitics are also considered in the design. Finally, simulated data is provided for the amplifier, over the operating frequency range of 824-849MHz.

6.3.3 Amplifier Specifications

The design goal for the completed amplifier is to provide 1-3 watts of output power into a 50Ω load without power combining. In addition, the efficiency at which the output power is developed is important. In this work we strive to achieve the maximum output power into a 50Ω load at the highest possible efficiency.

Normally, the supply voltage and load impedance are provided as design constraints, however, as the goal is to exercise the technology and amplifier topology to see what it is capable of, the design attempts to obtain maximum output power into the 50Ω load. The ideal design data from Chapter 4 is repeated in Table 6-2 for convenience.

TABLE 6-2 Class E Design Values @ $k=1.412$

Parameter	Normalized Value @ $k=1.412$	Normalizing Factor	Unnormalized Result	Parameter	Normalized Value @ $k=1.412$	Normalizing Factor	Unnormalized Result
Po	1.36	VDD^2/RL	3.3 Watts	$v_{\zeta}(\theta)$ max	3.65	VDD	40.15 V
B	0.6845	$1/RL$	13.7 mS	$i_{\zeta}(\theta)$ max	3.61	VDD/RL	794.2 mA
Vo	1.65	VDD	18.15 V	$i_L(\theta)$ max	3.99	VDD/RL	877.9 mA
IL(θ1)	1.86	VDD/RL	409.2 mA	$i_L(\theta)$ min	-1.06	VDD/RL	-233.2 mA
IDC	1.36	VDD/RL	299.2 mA	$i_{\zeta}(\theta)$ max	3.42	VDD/RL	752.4 mA
Phi	15.2 °	1	15.2 °	$i_{\zeta}(\theta)$ min	-2.01	VDD/RL	-442.2 mA
X	0	RL	0 Ω	$i_{\zeta}(\theta)$ max	1.65	VDD/RL	363 mA

6.3.4 Supply Voltage Determination

From the choice of the load resistance of 50Ω , we can determine the supply voltage using any of the scaling factors from Table 6-2. Using the output power normalization factor, we obtain a supply voltage of 11V by $V_{DD} = \sqrt{\frac{3.3RL}{1.36}}$. The designer must then ensure that the selected supply voltage is within the breakdown capabilities of the device. From Table 6-2, the maximum drain voltage swing is $V_S(\theta) = 40.15V$ ($3.61 \times 11V$). As this value of V_S occurs when V_{GS} is $\sim -10V$, $V_{GD} = -50.15V$ which is well below the silicon carbide breakdown voltage of 100V.

In the event that the designer finds the computed value of the supply voltage results in a maximum drain voltage swing which approaches (or exceeds) the breakdown voltage, the load resistance must be reduced in order to operate at the maximum power point. This reduction in load resistance would normally be accomplished by using an impedance transforming network between the drain of the Class E transistor and the load resistance.

6.3.5 Active Device Sizing

In addition to determining if the load impedance and the supply voltage chosen are within the breakdown capabilities of the active devices, the designer must ensure that the device selected is capable of handling the current required. From the data in Table 6-2, the maximum value of current in the active device, $I_S(\theta)$, is 794.2mA. To provide some margin in the design the size of the transistor should be selected such that it can provide currents in excess of the ideal design value by $\approx 15\%$. This implies the necessity for an active device capable of handling 913 mA. From the IV characteristics for a unit size device (Figure 6-1), it is apparent that the maximum current is ≈ 76 mA for $V_{GS} = 0$. To obtain the desired value of 913 mA requires a device 12 times unit size. Fortunately, the

engineering samples contained 12X250 devices. While it would be possible for parallel combinations of smaller devices to be used to achieve the same result, the goal was to design the amplifier such that the impact of parasitics from bonding and board level interconnections were minimized. As a result, a single 12X250 device was employed in the Class E amplifier circuit.

6.3.6 Component Value Determination

The component values for the amplifier can be determined from the data in Table 6-2. The shunt capacitance is determined from $B=13.7\text{mS}$ and the operating frequency as $C_P = \frac{B}{\omega} = \frac{13.7\text{mS}}{2\pi 835\text{MHz}} = 2.6\text{pF}$. The value for the drain supply inductor (L_{DC}) is found from the value of C_P and the selected value of k to be $L_{DC} = \frac{1}{(k\omega)^2 C_P} = 6.98\text{nH}$. Table 6-3 provides a listing of the component values chosen for the Class E amplifier. It should be

TABLE 6-3 Component Values for Class E Amplifier

Component	Value	Figure	Equation
C_P	2.6pF	4-5	(4-24)
L_{DC}	6.98nH	4-7	(4-5)
L_o	22nF	Not Applicable	
C_o	1.7pF		
R_L	50		

noted that the data for L_o and C_o in Table 6-3 may be chosen based on the acceptable harmonic content in the load and the ability to provide filtering. However, one must ensure that the loaded value of Q is not too high or large ringing transients will result and efficiency will be reduced. A suitable value of loaded Q was found to be 5 (see Chapter 4). The loaded Q , (Q_L) can be determined using $Q_L = \omega L / R_L$. For a loaded Q of 5, the value of L_o is 47.4nH. The value of C_o for resonance at 835MHz is 0.76pF. This value of capacitance (while realizable with surface mount components) is of the same order as the

expected value of the board parasitics and was thus deemed unsuitable for use in the hybrid amplifier design. In addition, absolute component tolerances are such that for the small value components, the variation is more significant in terms of percentage, resulting in larger errors with frequency than would be present if a larger value was used.

As a result, the value of loaded Q was reduced to $Q_L=2.39$ to allow a reasonable value of L_o and C_o to be obtained while at the same time obtaining high efficiency. From the ideal simulations in Chapter 4, the drain efficiency for a Q_L of 2 was 92.6% vs 96.6% for Q_L of 5. For a loaded Q of 2.39, the value of L_o is 22.8nH and the value of C_o required for resonance at 835Mhz is 1.7pF.

It should be noted that due to the low value of loaded Q used, a harmonic filter tuned to the fundamental was required between the drain of the Class E transistor and the load. A simple filter (parallel LC) was used with component values determined so as to resonate at the mid band frequency of 835MHz, and have reasonable unloaded Q factors and self resonant frequencies above 2.5 GHz. These values were determined to be $L_f = 5.7\text{nH}$ $C_f=6.3\text{pF}$.

The final component to be determined is the residual reactance X . From the design curves in Chapter 4 we know that for $k=1.412$ (maximum output power) the residual reactance required is equal to zero, and thus no additional inductive reactance needs to be added to L_o . HSpice simulations were conducted on the amplifier, the results of which are detailed in the next section.

6.4 Simulation of the Class E Design

Using the component values outlined in the previous sections, simulations were conducted on the Class E amplifier. The circuit schematic is shown in Figure 6-3 .

FIGURE 6-3 Initial Class E Design Without Parasitics

HSpice time domain simulations were run to examine the operation of the Class E amplifier. The simulation waveforms are illustrated in Figure 6-4. It is apparent from the figure that the amplifier is operating correctly, and while the waveforms exhibit the classic Class E shape, the maximum values are less than those determined from the ideal switch simulations performed in Chapter 4 (refer to Figure 4-17, on page 90 for comparison). This is simply due to the imperfect switching performance of the active device.

The switch current and the shunt capacitor current exhibit spikes during the transitions due to the fact that the voltage across the switch at the moment of turn on (12ns) is positive. Close examination of the drain voltage waveform indicates that during the on period of the switch (12-12.6ns) the voltage rises. This is due to the finite 'on impedance' of the device. Choosing a larger device would reduce this resistance, however, the output capacitance of the device would increase. Of note is the output current waveform shown in the lowest panel in the figure. From this waveform (or rather the Fourier transform of it) we can compute the power output at the fundamental and the total harmonic distortion present.

While it is apparent that the waveform is almost sinusoidal (and thus contains minimum harmonic content) the total harmonic distortion numbers provide a clearer picture. The

FIGURE 6-4 Class E Amplifier Without Parasitics

output power, drain efficiency and total harmonic distortion THD are shown in Table 6-4

where drain efficiency is defined as: $\eta = \frac{P_{out_{RF}}}{P_{in_{DC}}}$. The total harmonic distortion is computed by HSpice using the expression[MetaS96]:

$$THD = \frac{100}{R_1} \sqrt{\sum_{m=2}^9 R_m^2} \quad (6-2)$$

where R_1 is the fundamental component, and R_m is the magnitude of the 2nd through 9th harmonic of the analysis frequency.

TABLE 6-4 Class E Amplifier Performance

Parameter	Units	Value
P _{out}	W	1.91
η	%	74
THD	%	5.6

The difference in output power between the ideal switch simulation and the same simulation using a MESFET is approximately 48%. In addition, the drain efficiency has declined by ~ 22% when using the MESET. As mentioned this is due to the imperfect nature of the MESFET switch and provides the baseline for further examination. Obviously, an active device will not exhibit the same performance as a macro-model of a perfect switch, and some loss is to be expected. Similar to the ideal switch-based Class E amplifier, the transistor based version will suffer performance degradation with increasing transition time on the input. This is examined in the following section where the Class F amplifier is designed.

6.5 Class F Stage Design

The design of the Class F is not nearly as formal as the Class E. Following the procedure identified in Chapter 5, one attempts to obtain a reasonable square wave drive into the Class E stage. In order to do this we need to understand the characteristics of the drive waveform that the Class E amplifier requires for optimum performance.

6.5.7 Characteristics of the Drive Waveform for the SiC Based Class E Design

In order to design the Class F driver stage to produce the correct waveform for the Class E stage, knowledge of the drive waveform is required. As the pinch off voltage for the devices is -9.37 volts, the ideal input drive for the Class E stage would swing from -12 volts or so (completely cut off) to just below ground (0V for the sake of discussion). This waveform must be driven into a low impedance input to the Class E stage and have reasonably quick rise and fall times.

In chapter 5 the design method for the Class F stage was discussed. In chapter 5 it was determined that a modified Class F topology (both tank circuits on the drain) could produce a replica of a square wave by proper control of the tank impedances and the input drive waveform. Chapter 4 illustrated the difficulties of operating a Class E stage with an input with rise and fall times which are a large percentage of the RF cycle. In effect the period the switch is off is longer, and an apparent change in duty cycle results in decreasing efficiency.

If we consider the components of the square waveform generated by the Class F stage we can quickly see that even under the best case, the transition times for the input to the Class E will be quite long in relation to the RF cycle. From Chapter 2 we know that the drain voltage expression for the Class F amplifier (with maximally flat waveforms) is of the form:

$$V_D = A \sin(\omega t) + \frac{A}{9} \sin(3\omega t) \quad (6-3)$$

for which the slope is $1.33A\omega$ at time ($t=0$).

As we know, the desired square wave signal at the input of the Class E is 12Vpp. This sets the value for VDD for the Class F to 6V, as its drain will swing from 0 to 2VDD. The

amplitude for the fundamental of the drain voltage waveform is $1.125 \cdot V_{DD}$ (from equation (2-2)) and the slope of the "square wave" will be $(1.33 \cdot 6.75 \cdot 2 \cdot \pi \cdot 835 \text{e}6) = 47.1 \text{V/ns}$. In order for the input signal to ramp over the full range (using this slope) one obtains a (minimum rise time) of $(12 / 47.1) \text{ns} = 255 \text{ps}$. The combined rise and fall time is (at best) 510ps or 42% of the period. As a result of this, the amplifier's performance will be considerably less than the values obtained using an ideal switching element with ideal drive. The simulations in Chapter 4 illustrate the impact of slow rise and fall times on amplifier performance. We can expect to see similar effects in the final amplifier as the switching times cannot be reduced below these values. While this limitation would apply to any technology, its impact on silicon carbide is particularly large. As SiC devices have such a large pinch voltage, operating the device as a switch is difficult as a result of the "square" wave's low rise time. Such difficulties would not arise however, for a SiC based Class A power amplifier as the active device is driven as current source and not a switch.

With knowledge of the required drive waveform's characteristics coupled with knowledge of what can be generated, we can now proceed with the design of the driver amplifier stage.

6.6 Design of the Class F Stage

The Class F driver stage must provide a square wave input to the Class E for efficient conversion of DC power to RF power. This section examines the design of the Class F stage.

Starting from the Class E amplifier stage we must determine the input impedance the Class F has to drive. The parallel tank circuits are shunted by the input impedance of the Class E stage. In addition, the MESFET device is not unilateral, that is its input is not free from capacitive coupling to its output. As a result the input impedance of the Class E

stage is difficult to determine. A large signal transient analysis was conducted and the ratio of the Fourier components of the input voltage and current waveforms was obtained. This provided a quasi-impedance for each harmonic based on the amplifier operating in the Class E regime. The impedance of the Class E stage was determined to be equivalent to 3Ω in series with 4pF at the fundamental, and 7Ω in series with 3pF at the third harmonic. As this low impedance would be difficult for the Class F stage to drive, the bias circuitry for Class E stage was adjusted in an attempt to tune out some of the capacitance.

In order to minimize the coupling from the input to the output of the Class F stage the device size was kept smaller than that used for the Class E stage. In addition, the choice of a smaller device would increase the input impedance, allowing easier matching to a 50Ω source. Based on this, the size for the Class F device was set at 1/6th the size of the Class E device, and a 2X250 device was used.

The initial circuit for the amplifier consisting of the Class E stage and the Class F driver is illustrated in Figure 6-5.

FIGURE 6-5 Amplifier Incorporating Class F Driver

Apparent from the schematic is the biasing circuit for the Class E stage, which uses a 8.2nH inductor to tune out the input capacitance of the Class E. The tank circuit values for the Class F stage proved to be suitable values to generate reasonable switching performance on the Class E stage. In addition, the parallel filter component values were adjusted to increase the capacitance and reduce the THD in the load by providing a lower impedance for the tank circuit at higher frequencies. Simulation results for the amplifier are provided in Figure 6-6.

FIGURE 6-6 Simulated Results for the Amplifier with Class F Incorporated

Also of note is the input matching network on the input of the Class F stage. While a brute force match to the 50Ω source is not the desired situation (as the majority of the input power is dissipated in the matching resistor), it was necessary as the input impedance of the completed amplifier contained a negative real part of -8Ω. This was determined to be due to the gate-drain capacitance of the Class F stage coupling the output to the input and causing a phase shift in the input current. This was verified by modifying the device models to remove the gate-drain capacitance. Under these conditions the input impedance contained a positive real part as the feedback coupling was removed. However, this modification was not available in the actual circuit realization. In this regard attempts were made to tune out the feedback capacitance however this was ineffective as the attempts at tuning resulted in high frequency oscillations.

From the simulation plots we can see that the incorporation of the Class F amplifier has resulted in a decrease in the amplifiers' performance. The voltage waveform across the switch has a lower amplitude and extends into the on portion of the RF cycle by approximately 600ps. As mentioned previously, this is due to the slower rise time the Class F amplifier is capable of generating. Power output, drain efficiency, THD and power aided efficiency (PAE) are computed for the amplifier. The PAE is computed using:

$$PAE = \frac{P_{out_{RF}} - P_{in_{RF}}}{P_{in_{DC}}} \quad (6-4)$$

The RF input power is computed based on the magnitude of the voltage swing at the gate of the Class F amplifier with the 50Ω resistor as a reference. The data for the completed amplifier (without parasitics) is provided in Table 6-5.

TABLE 6-5 Class E/F Amplifier Performance

Parameter	Units	Value
P _{out}	W	1.14
P _{inDC}	W	1.97
P _{inRF}	mW	42
η _E	%	62.3

TABLE 6-5 Class E/F Amplifier Performance

Parameter	Units	Value
η_{FE}	%	57.8
PAE	%	55.7
THD	%	2.18

From the data it is apparent that the slower input drive generated by the Class F stage has a significant impact on performance. The efficiency values represent the drain efficiency of the Class E without considering the DC power in the Class F (η_E) and the drain efficiency considering all DC input power (η_{FE}). Comparing the Class E drain efficiencies between the ideal drive and the Class F drive, we have a difference of 11.7%. We also notice that the output power has declined by 40% from the ideal drive case. This is apparent in the lower maximum values for the switch voltage and the output current. The impact of board level bonding parasitics will also degrade the amplifier performance from the ideal situation. These issues will be examined in the following section.

6.7 Parasitic Calculations

As the amplifier design in this work is a hybrid one, the board level bonding parasitics are significant and must be taken into consideration. Figure 6-2 illustrates the MESFET mounting sockets milled into the TMM3 substrate. These sockets were sized such that the required bonding wire would be as short as possible. The dimensions of the socket are 1mm x 2mm. The transistor die are about 1mm square (2X250 and 12X250). As a result, the bond wires were determined to be $\approx 40\text{mil}$ (1mm) long, providing roughly 1nH of inductance.

Board level parasitic capacitances were determined based on the dielectric constant for the TMM3 material and the size of the bonding regions on the board. These capacitances were determined to be in the <10fF range and were ignored in the simulations.

The capacitive parasitics on the transistor die themselves were much more significant. The higher dielectric constant resulted in larger capacitances which ranged from 20-300fF. The largest parasitic capacitances occurred on the source nodes, as the SiC MESFETs have a large source "manifold" to allow grounding of the device.

In the simulations the bond wire parasitics are by far the most difficult to deal with. They push the Class E design further from the ideal situation on which the equations are based. After extensive simulations it was determined that the source and drain nodes were the most sensitive to the bond wire parasitics.

Simulations were conducted taking into account individual parasitics in sequence to determine their impact. The circuit was found to be sensitive to the value of the bond inductors used. Simulations indicated that oscillations were possible for some values of bond inductances. After extensive simulations, a configuration was determined that produced no oscillation and resulted in reasonable performance. The bonding configuration consisted of 4 bondwires on the source (located at the corners of the die to minimize the inductance and the mutual coupling), 2 bondwires on the drain and a single bond wire on the gate.

Simulation plots for the completed amplifier after adjustments were made for the bonding parasitics are illustrated in Figure 6-7

FIGURE 6-7 Completed Class F/Class E Amplifier Incorporating Parasitics

The data extracted from the HSpice output file provides an indication of the amplifier performance change due to the parasitics (see Table 6-5).

TABLE 6-6 Class E/F Amplifier Performance with Parasitics

Parameter	Units	Value
Pout	W	1.13
PinDC	W	1.87
PinRF	mW	42
η_E	%	64.9
η_{FE}	%	60.2
PAE	%	57.97
THD	%	0.54

In fact we can see that there is a slight improvement in the amplifiers performance due to the bond wires. While this is true at the center frequency of the band of interest, the impact of the parasitics will be larger at higher frequencies.

Thus far we have only examined the amplifiers' capabilities at the design (center) frequency. In order to obtain a sense of the amplifier's capabilities over the range of operating frequencies from 824-849MHz, simulations were conducted and the power and efficiency data were extracted for plotting using Matlab. This data for Pout, PAE, DC

input power and peak output voltage are illustrated in Figure 6-8 as a function of supply voltage.

FIGURE 6-8 Simulated Amplifier Performance @ 824, 835 and 849MHz

From the figure, it is apparent that the amplifier performs well over the band of interest, especially for values of VDD at or below the design value. For operation at the design supply voltage (11V), the variation in the amplifier output power is $\approx 14\text{mW}$ while the simulated PAE varies by 0.8% over the same band. For values of supply voltage exceeding the design value, the performance of the amplifier at the upper band edge starts to decay. This is due to the larger impact of the parasitics at the higher frequency.

6.8 Board Level Design Issues

Upon completion of the amplifier simulations the substrate for the hybrid design remained to be completed. This task was completed by board level designers within Nortel. This

allowed the design to be completed quickly and accurately. As mentioned previously, the difficulty in determining the input impedance of the stages under operation lead to the design of two boards. One consisted of the configuration outlined in the schematic of Figure 6-5. The second board was identical except that the input matching network was designed to allow the input impedance to be measured under operating conditions. After this a standard matching network could be designed and installed. The board layouts are illustrated in Figure 6-9. The board layout was performed carefully to ensure that the

FIGURE 6-9 High-Efficiency Amplifier Layout Versions 1 and 2

transmission line lengths were less than the values provided in section 6.2.2. In addition, blind vias were placed over the entire substrate to provide a low inductance ground plane for the board.

The components utilized in the design were standard (0805) surface mount inductors (Coilcraft) and capacitors from AVX Corporation. These components were chosen as they provided reasonable Q values for the frequency range of operation. In addition to the standard surface mount components miniature trimmer capacitors were obtained for use as the shunt capacitance. The main reason for this was to allow for some post fabrication tuning of the circuit. The trimmer capacitors were A1 Series Trimmer Capacitors from Voltronics Corporation. These capacitors offered a high quality factor over the band of interest (exceeding 150 at 2.5GHz). For the 50 Ω load for the amplifier, it was determined that the input impedance of the measurement equipment would provide the necessary load. A total of three substrates had components epoxied to the substrate for use in testing the amplifier performance.

6.9 Measured Amplifier Performance

Three amplifiers identical to the schematic illustrated in Figure 6-5 were tested, first for DC bias operation and then at RF. Unfortunately, results were not promising. The test setup is illustrated in Figure 6-10.

FIGURE 6-10 Amplifier Test Measurement Setup

The three amplifier boards were tested for DC current draw to ensure that there were no short circuits created during component mounting on the board. The following table compares the simulated DC Bias condition and the actual DC bias conditions for the three amplifier boards:

TABLE 6-7 DC Bias Measurements

Amplifier	Class F DC Drain Current [mA]	Class E DC Drain Current [mA]	Class F Gate Bias Voltage [V]	Class E Gate Bias Voltage [V]
Simulation	78.3	74.8	-3.0	-7.0
Amp # 1	55.4	97.6	-3.0	-7.0
Amp # 2	11.5	8.3	-3.0	-7.0
Amp # 3	59.2	68.0	-3.0	-7.0

The DC bias measurements indicates that there is a problem in the test devices. Amplifier #2's current is extremely low indicating possible damage in the active devices themselves (possible victim of an ESD event). Amplifiers #1 and #3 provide currents that are in the same range as the simulation, however, they are not as close as one would expect them to be. Note also from the table that the bias operating point for the Class F has been adjusted from -6.0V to -3.0V (refer to Figure 6-5, on page 119) due to the inability of the signal generator to create the +16dBm source required to drive the Class F amplifier and generate the necessary harmonics.

The amplifiers were connected to the test setup in Figure 6-10 and the output power at the design frequency of 835MHz was measured. The output power measured was much smaller than the simulations indicated. During the measurement process, attempts were made to adjust the tuning on the amplifiers to improve the performance, with little success. The main difficulty in attempting to tune the amplifier is the inability to observe the drain voltage waveform to provide the basis for tuning. In addition to tuning using the variable trimmer capacitors, bias voltages were adjusted to determine if the performance could be improved. During the tuning process, one of the trimmer capacitors broke free of its epoxy on the board and the amplifier (#1) was unavailable for further testing. The data for amplifiers #2 and #3 are provided below to give insight into the testing difficulties:

TABLE 6-8 Amplifier #2 RF Data

VGF [V]	VGE [V]	VDF [V]	VDE [V]	IDF [mA]	IDE [mA]	Pout [dBm]	Pin [dBm]
-2.0	-7.0	6	11	11.5	8.3	1.89	13
-2.0	-6.0	6	11	11.6	30.7	12.43	13
-2.0	-5.5	6	11	11.8	48.1	14.22	13
-1.6	-5.5	6	11	15.3	48.1	14.2	13
-1.6	-5.0	6	11	16.8	79.2	15.4	13
-1.6	-5.0	6	13	16.5	88.2	16.12	13
-1.6	-5.0	6	15	16.5	93.1	16.7	13
-1.6	-5.0	6	19	17.9	105.1	18.2	13

TABLE 6-9 Amplifier #3 RF Data

VGF [V]	VGE [V]	VDF [V]	VDE [V]	IDF [mA]	IDE [mA]	Pout [dBm]	Pin [dBm]
-3.0	-7.0	6	11	56.8	48.4	0.3	13
-3.0	-7.0	6	11	68.5	43.3	1.6	13
-3.0	-6.0	6	11	55.7	109.0	2.94	13
-3.0	-6.0	7	11	61.92	107.4	3.8	13
-3.0	-6.0	8	11	67.5	106	4.6	13
-3.0	-5.0	9	16	66.3	197.3	5.23	13

Simulation results on the best amplifier of the two resulted in gains of 4-5dB rather than 47dB as was expected. Figure 6-11 and Figure 6-12 illustrate the spectrum analyzer plots for the amplifiers at maximum output.

FIGURE 6-11 Amplifier #2 Output Power

FIGURE 6-12 Amplifier # 3 Output Power

Unfortunately there was insufficient time to complete measurements on the second version of the amplifier and include this data in this work.

While the difference between measured and simulated data is significant there are a couple of possible explanations for the discrepancies. First and foremost, the devices used in this work are early version experimental devices provided to allow characterization and modeling efforts. Due to the nature of the devices (high-voltage and high-power) and the available lab equipment, only the smallest devices were characterized to generate the models. Larger devices could not be characterized at high voltage and thus their model parameters were scaled from the data available from the smaller devices. Unfortunately, this can lead to modeling inaccuracies for the device used in the Class E amplifier stage (12X250).

In addition, the pinch off voltage for these early engineering samples was not well controlled within the process. In fact, the manufacturer has indicated that the batch

performance was anomalous. Specifically, while the nominal value of V_p is -9.2V, the measured values for the devices used in the amplifiers exhibited V_p values between 30 and 40% lower (in magnitude) . This leads to severe deviation between the measured and simulated results. In addition, measurements on the subthreshold characteristics for the devices indicated that the test MESFETs only exhibited control over the drain current for 2-3 decades while a standard MOSFET device exhibits current control over 7-8 decades or more. This situation has implications for switching based power amplifiers as the lack of current control reduces the effectiveness of the switching operation.

While the measured results are less than expected, several conclusions and recommendations can be put forward as a result of this work.

7.1 Summary

As with any project many things were learned during the course of this research. It is the purpose of this chapter to provide the conclusions which can be drawn from this work and to identify recommendations for further study in this area.

To reiterate, the goals of this project were to:

- a) refine the design procedure for Class E high-efficiency power amplifiers.
- b) design a high efficiency Class E / Class F power amplifier operating in the 824-849 MHz band capable of providing 1-3 Watts of output power into a 50 Ω load without resorting to power combining techniques,
- c) evaluate the suitability of these amplifier classes for use in the RF regime, and
- d) evaluate the suitability of silicon carbide MESFET devices for use in Class E and Class F amplifier topologies for use in wireless (base-station) applications.

With respect to the first goal, this work has refined the design procedure by providing scalable design curves for use in determining Class E amplifier parameters and component values (Appendix A). Using these curves the designer can rapidly obtain component

values and ideal amplifier parameters for a 'first cut' design for use in optimization. While the simulation results for the high-efficiency amplifier were promising (output power over 824-849MHz from 1.1 to 1.25W from 11V supply), the measured results were not as significant. The design and simulation of the amplifier indicated that the Class F /Class E topology was a viable option for use in the RF regime. However, measured performance did not confirm this. Inadequacies in modeling of the circuit in the time domain are determined to be a significant contributor to the discrepancy between simulation and measurement. In this regard, the following conclusions can be drawn from the design of the Class E amplifier.

7.2 Conclusions

The use of Class E power amplifiers in the RF regime (at lower power levels) has been demonstrated by others [Sowla96] in integrated form with success. However the devices in this thesis cannot, at present, be fully integrated, and imply the necessity of board level implementation and require dealing with significant parasitic elements.

The current state of silicon carbide technology is such that wafers are extremely expensive. Integration of passive components is not yet cost effective. In this regard, silicon carbide lends itself well to high power, board level design but implies the necessity of dealing with significant parasitics introduced in simply bonding to the device. In light of this, the use of silicon carbide devices would be more effective in high-power applications where the impact of bonding parasitics is not as great (Class A linear amplification). Their use in higher efficiency amplifier topologies is going to be difficult, as this study shows. What is required to overcome this difficulty is the ability to integrate some of the passive elements surrounding the SiC MESFET on the same (SiC) substrate.

In this environment, transmission line effects can significantly impact system performance, dependent on the substrate/board material and the frequency of operation. In this thesis, the frequency of operation and the substrate material were such that the distributed effects of transmission lines could be neglected. This certainly will not be the case in all applications, especially as operating frequencies increase.

Overall, the implementation of a high-power, high-efficiency power amplifier (board level design) using the Class E/ Class F topology did not prove overly promising. The main reasons for this are assessed to be related to the inability of time domain simulations to capture the frequency domain aspects of the nonlinear operation of the amplifier. It is also important to note that the silicon carbide devices used in the design were initial engineering samples and had significant variability in critical parameters which was not incorporated in the model, as it was deemed anomalous behavior. As the process becomes more mature, the quality of devices is expected to improve dramatically.

One final note on the device modeling is that due to equipment limitations (current carrying capability of bias T networks), only the smaller MESFETs were measured and characterized. For the larger devices, the model data from the smaller devices was scaled. This can lead to inaccuracies in modeling the larger devices especially when they are operating under large signal conditions.

It is believed that if a model for the silicon carbide MESFET suitable for use with a harmonic balance simulator (such as Libra) was available, the results would have been very different. Under harmonic balance, the effects of transmission lines, component quality factor (Q) variation with frequency, and harmonic terminations could all be accounted for in the design. Board level parasitic elements also could be accurately determined after layout. As a result, the use of a time domain only (HSpice) simulator is not recommended for use in design of high-efficiency (nonlinear) amplifiers. The use of a

harmonic balance simulator is considered to be essential to obtain reasonable modeling of the circuit and hence, measured amplifier performance.

With respect to determining the suitability of Class F/ Class E amplifier use in the RF regime, it is apparent from the work of others [Sowla96], [Rabb77], [Zulin87], that at lower frequencies and or lower output power levels, the topology will provide reasonable results as the circuits' deviation from the ideal situation described in Chapter 4 is not too great. Increasing frequency and increasing power level combine to make it difficult to implement a Class E amplifier exhibiting reasonable performance.

The implementation of a Class F/ Class E amplifier using the silicon carbide MESFET devices proved to be difficult to achieve. This is not to say that the SiC technology is not suitable for power amplifier design. On the contrary, numerous researchers have in recent months designed linear power amplifiers using this technology with excellent performance. Class A and B amplifiers are normally quoted with high power densities. [Weitz96, Moore97].

7.3 Recommendations for Future Work

As a result of this research project, certain recommendations can be made for future study in the area of high efficiency amplifier design using silicon carbide devices.

While it was concluded that use of silicon carbide MEFSETs (in die form) might not be the best method for implementing a Class F /Class E amplifier, additional study in this area is recommended. In this regard, the first step would be to develop a model for use in the harmonic balance simulator Libra. This process would take some time, as model code has to be written and debugged to ensure that the devices are correctly modeled and that simulated results are correct. It is thought that the time spent on this aspect of the design would translate into significant improvement in the correspondence between the final simulated and measured performance of the amplifier. Such simulations are capable of taking into account frequency and time domain aspects of the circuit simultaneously. This is thought to offer a significant improvement over simple time domain simulation.

Another expansion to the current work would be to experiment with a Class E design in SiC which incorporated passive elements on the same substrate with the MESFET devices. This would reduce the impact of parasitic elements on the design and would allow for operations at higher frequencies. The main hurdle to this course is the present cost of the SiC wafer, which makes the integration of passive components very expensive (on chip inductors and capacitors consume large wafer areas).

One final recommendation for further work would be to compare the Class E amplifier design using advanced models for the silicon carbide devices with the same amplifier topology using a GaAs MESFET. Such examination could include the impact of self heating and thermal conductivity on the amplifier's performance's and would serve to highlight the comparative strengths of the two technologies for use in high-efficiency amplifiers.

References

- [Best97] E. Best, Personal Communication, 19 Mar 1997.
- [Kazim87] M.K. Kazimierczuk, K. Puckzko, *Exact Analysis of Class E Tuned Power Amplifier at any Q and Switch Duty Cycle*, IEEE Transactions on Circuits and Systems, Vol. CAS-34, No. 2, Feb. 1987, pp.149-159.
- [Kraus80] H.L. Krauss, C.W. Bostian, F.H. Raab, *Solid State Radio Engineering*, John Wiley & Sons, New York, 1980.
- [Li94] C.H. Li, Y.O. Yam, *Maximum Frequency and Optimum Performance of Class E Power Amplifiers*, IEE Proceedings Circuits Devices and Systems, Vol.141, No.3, June 1994, pp.174-184.
- [Long95] J.R.Long, M.A. Copeland, *Modeling, Characterization and Design of Monolithic Inductors for Silicon RFICs*, IEEE Journal of Solid State Circuits, Vol. 32, No. 3, Mar. 1997, pp.357-369.
- [MacEl97] T. MacElwee, Nortel Internal Presentation on SiC MESFETS July 1997.
- [Maas88] S.A. Mass, *Nonlinear Microwave Circuits*, Artech House, Norwood MA, 1988.
- [MetaS96] HSPICE User's Manual Software for IC Design, META Software, California, Release 96.1, 1996
- [Moore97] K.E. Moore et.al., *4H-SiC MESFET with 65.7% PAE at 850MHz*, IEEE Electron Device Letters, Vol. 18, No. 2, Feb. 1997, pp.69-70.
-

-
- [Moroc94] H. Morkoc, et. al. *Large-Band-Gap SiC, III-V Nitride, and II-VI ZnSe-based Semiconductor Device Technologies*, Journal of Applied Physics, Vol. 76 No. 3, August 1, 1994, pp. 1363-1398.
- [Mundr93] P.S. Mundra, T.L. Singal, R. Kapur, *The Choice of a Digital Modulation Scheme in a Mobile Radio System*, IEEE Vehicular Conference Proceedings, IEEE, New Jersey, 1993, pp. 1-4.
- [Neude85] P.G. Neudeck, *Progress Toward High Temperature, High Power SiC Devices*, Institute of Physics Conference Series No. 141, 1995, pp. 1-6.
- [Neude95] P.G. Neudeck, Recent Progress in Silicon Carbide Semiconductor Electronics Technology, Internet document: <http://www.lerc.nasa.gov/WWW/SiC/SiCReview.html> Updated Oct 1995.
- [Palmo94] J.W. Palmour et.al., *Silicon Carbide Substrates and Power Devices*, Proceedings of the 21st International Symposium on Compound Semiconductors, Bristol, UK., IOP Publishing, 1994.
- [Plett97] C. Plett, *Radio Frequency Integrated Circuit Design - Graduate Course Notes*, Carleton University, 1997.
- [Pozar90] D. Pozar, *Microwave Engineering*, Addison Wesley, New York, 1990.
- [Rabb77] F.H. Raab, *Idealized Operation of the Class E Tuned Power Amplifier*, IEEE Transactions on Circuits and Systems, Vol. 24, No. 12, Dec. 1977, pp. 725-735.
- [Rabb96] F.H. Raab, *Class-F Power Amplifiers with Maximally Flat Waveforms*, Green Mountain Radio Research Company, Vermont, TP95-9, 1996.
-

-
- [Sklar88] B. Sklar, *Digital Communications, Fundamentals and Applications*, Prentice Hall, New Jersey, 1988.
- [Sokal75] N.O. Sokal, A.D. Sokal, *Class E- A New Class of High-Efficiency Tuned Single Ended Switching Power Amplifiers*. IEEE Journal of Solid State Circuits, Vol. SC10, No. 3, Jun. 1975, pp.168-176.
- [Sokal75A] N.O. Sokal, A.D. Sokal, *High Efficiency Tuned Switching Power Amplifier*, United States Patent, # 3919656, Nov. 11, 1975.
- [Sokal80] N.O. Sokal, *Class E Switching-Mode RF Power Amplifiers*, RF Design, Intertec Publishing, Englewood, CO., Summer 1980, pp.33-39.
- [Sowla96] T.H. Sowlati, *Class E Power Amplifiers for Wireless Communications*, University of Toronto, Toronto Ontario, 1996.
- [Smith86] J. Smith, *Modern Communications Circuits*, McGraw Hill, New York, 1986.
- [Vende90] G.D. Vendelin, A.M. Pavio, and U.L. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*, John Wiley and Sons, New York, 1990.
- [Weitz95] C.E. Weitzel, *Comparison of SiC, GaAs, and Si RF MESFET Power Densities*, IEEE Electron Device Letters, Vol. 16, No. 10, Oct. 1995, pp.451- 453.
- [Weitz96] C.E. Weitzel et.al., *Silicon Carbide High-Power Devices*, IEEE Transactions on Electron Device, Vol. 43, No. 10, Oct. 1996, pp.1732-1739.
-

-
- [Zulin87] R.E. Zulinski, J.W. Steadman, *Class E Power Amplifiers and Frequency Mutlipliers with Finite DC-Feed Inductance*, IEEE Transactions on Circuits and Systems, Vol. 34, No. 9, Sept. 1987. pp.1074-1087.
-

Appendix A: Normalized Class E Design Curves

This appendix provides (in one location) the normalized design plots for the Class E amplifier. Refer to Chapter 4 for a complete derivation of the equations from which these plots are obtained. The Table below provides a quick reference of the scaling factors for the normalized curves. To obtain the desired value, determine the value of the data from the normalized plot (at the desired value of k) and multiply by the associated scaling factor. The figure and equation numbers refer to Chapter 4. The normalized value for $k=1.412$, is the value for maximum power output into a fixed load at fixed VDD.

Parameter	Figure	Equation	Normalized Value @ $k=1.412$	Normalizing Factor
Po	4-6	(4-25)	1.36	VDD^2/RL
B	4-5	(4-24)	0.6845	$1/RL$
Vo	4-8	(4-27)	1.65	VDD
IL(θ l)	4-9	(4-28)	1.86	VDD/RL
IDC	4-10	(4-29)	1.36	VDD/RL
Phi	4-4	(4-20)	15.2 °	1
X	4-16	(4-37)	0	RL
$v_S(\theta)$ max	4-11	(4-30)	3.65	VDD
$i_S(\theta)$ max	4-14	(4-35)	3.61	VDD/RL
$i_L(\theta)$ max	4-12	(4-33)	3.99	VDD/RL
$i_L(\theta)$ min	4-12	(4-33)	-1.06	VDD/RL
$i_C(\theta)$ max	4-15	(4-36)	3.42	VDD/RL
$i_C(\theta)$ min	4-15	(4-36)	-2.01	VDD/RL
$i_O(\theta)$ max	4-13	(4-34)	1.65	VDD/RL

FIGURE A-1 Normalized Φ

FIGURE A-2 Normalized $B \cdot RL$

FIGURE A-3 Normalized XDC/RL

FIGURE A-4 Normalized Output Power

FIGURE A-5 Normalized Output Voltage

FIGURE A-6 Normalized IL0

FIGURE A-7 Normalized IDC

FIGURE A-8 Normalized Switch Voltage $k=[0.5, 1.1, 1.4, 1.7]$

FIGURE A-9 Normalized Switch Current $k=[0.5, 1.1, 1.4, 1.7]$

FIGURE A-10 Normalized IL $k=[0.5, 1.1, 1.4, 1.7]$

FIGURE A-11 Normalized Output Current $k=[0.5, 1.1, 1.4, 1.7]$

FIGURE A-12 Normalized IC $k=[0.5, 1.1, 1.4, 1.7]$

FIGURE A-13 Normalized X

IMAGE EVALUATION TEST TARGET (QA-3)

APPLIED IMAGE, Inc
1653 East Main Street
Rochester, NY 14609 USA
Phone: 716/482-0300
Fax: 716/288-5989

© 1993, Applied Image, Inc., All Rights Reserved