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**GALLIUM ARSENIDE ANALOG CIRCUITS FOR HIGH-SPEED
ANALOG-TO-DIGITAL CONVERSION**

by

Peter Borkowski, B. Eng.

**A thesis submitted to the Faculty
of Graduate Studies and
Research in partial fulfillment
of the requirements for the degree of**

Master of Engineering

**Ottawa-Carleton Institute
of Electrical Engineering
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ABSTRACT

High-speed analog-to-digital (A/D) converters offer the means to interface receivers to high throughput digital signal processors. Essential elements in these converters, which define and limit accuracy, are sample-and-holds and voltage comparators. This thesis outlines the design, fabrication and evaluation of a sample-and-hold and two distinct comparators developed using one micron gallium arsenide (GaAs) depletion mode metal semiconductor field-effect transistor (D-MESFET) technology. The sample-and-hold, with a 600 pS acquisition time, exhibited a 16 dB improvement in clock feedthrough elimination compared to a conventional D-MESFET switch. A capacitive differencing comparator, adapted from nMOS circuitry, provided ± 30 mV sensitivity at 500 MHz operation and a differential amplifier, incorporating self-bootstrapped structures, displayed 16 dB of gain with a bandwidth of 200 MHz.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Analog-to-digital (A/D) conversion is the translation or transformation of continuous amplitude and time (analog) signals into discrete amplitude and time (digital) signals. The A/D converter is an essential interface present at the front-end of systems which perform digital processing of signals transmitted in analog form. Recently, digital signal processing (DSP) of information has become increasingly popular for several reasons. Decreased component count and reduced circuit complexity have brought down size and power consumed in systems. DSP also increases performance in systems through the use of linear digital filtering and Fourier Transform algorithms which provide greater selectivity and improved noise characteristics. There is little doubt that the demand for integrated DSP circuits has increased over the past decade.

The development of DSP systems is now being driven to increase the speed at which information is processed. High-speed signal processing has many applications in areas such as radar, communications, electronic warfare and electronic intelligence where improved data throughput rates provide fast and more reliable systems. Increased digital processing rates directly translates to requirements for high-speed, high accuracy A/D converters which are implemented to precede system blocks such as digital demodulators and demultiplexers.

The majority of A/D converters today are silicon based circuits

with a variety of converter architectures available. The parallel, or flash, A/D converter has emerged as a popular choice for speed applications. Today's silicon flash A/D's operate at 300 megasamples/s at 8 bits of resolution and 50 megasamples/s at 10 bits [1.1]. However, recent advances in gallium arsenide integrated circuit (IC) technology, which offers distinct speed advantages, promise even higher rates.

This thesis studies the necessary concepts for developing a high-speed A/D converter on gallium arsenide (GaAs) and presents designs of analog circuits required in the conversion process. These designs differ from those developed using conventional microwave analog techniques since they are wideband circuits which employ more transistors and less passive components in their structure. The circuits were designed using depletion-mode metal-semiconductor field effect transistor (D-MESFET) technology on GaAs and eliminate problems which have plagued performance of these A/D circuits.

1.2 THESIS OBJECTIVE

To achieve fast and reliable processing of wideband signals using integrated circuits, A/D converters operating at sample rates of 1 gigasample/s with resolutions of 8 bits or greater would be beneficial. To meet this requirement, an analytical look at A/D architectures and necessary circuit blocks must be taken. In most A/D configurations, two circuits required for conversion are the sample-and-hold and the comparator. However, progress in GaAs development of high rate, high accuracy converters has been hampered by the design of these elements. Specifically, clocking effects and process variation have limited their performance. The overall objective of this thesis work is to build

improved sample-and-hold and comparator circuits on GaAs which would be applicable to most A/D configurations, assess these components and suggest alternative measures for ongoing development.

1.3 THESIS OUTLINE

The structural breakdown of the contents of this thesis is given in Figure 1.1.

Figure 1.1. Thesis Structure.

The first two chapters offer an introduction to the necessary considerations for gallium arsenide analog-to-digital converters. Chapter 2 considers the high-speed aspects of conversion and begins with addressing a specific application for such a component in satellite on-board processing. Relevant A/D topics such as sampling, amplitude quantization and signal-

to-noise ratio inherent in the A/D process are then introduced. High-speed, wide bandwidth architectures for conversion are also reviewed and, finally, common circuit blocks are presented which find direct implementation into the above architectures.

In Chapter 3, gallium arsenide as a semiconducting technology is presented. A brief comparison to silicon to expose advantageous properties is provided followed by a more indepth treatment of GaAs integrated circuits. Circuit elements used in linear analog and digital ICs are outlined and this is preceded by a description of modelling GaAs circuit elements using SPICE. Presentation of a typical GaAs process flow for developing integrated circuits concludes the chapter.

Designs of a sample-and-hold and two comparator configurations are presented in Chapter 4. Characteristics of circuit elements are analyzed and proposed methods for improvement of adverse effects are explained. Areas of analysis for the sample-and-hold include clock-feedthrough minimization and amplifier bandwidth improvement. Gain improvement and process sensitivity are considered for the comparators.

The experimental results are provided in Chapter 5 for the three A/D converter subcircuit designs. Evaluation with respect to large signal characteristics, frequency response and clocking at gigasample rates is discussed and compared to the theoretical predictions.

An overview of the individual circuit performances is presented in the final chapter complemented with an estimation of A/D characteristics using these circuits. Recommendations for improvement of these components are provided and is followed by a discussion of future research activities which could be pursued in this area.

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- [1.1] Goodenough, F., "FOCUS ON FLASH A/D CONVERTERS", *Electronic Design*, pp. 131-140, July 14, 1988.

CHAPTER 2

HIGH-SPEED ANALOG-TO-DIGITAL CONVERSION

2.1 INTRODUCTION

Interfacing transmitted analog information systems to digital systems requires the use of analog-to-digital (or conversely digital-to-analog) converters. Although many conversion techniques have been available for years, a new breed of converters is required to interface with fast, high-accuracy digital processors. These analog-to-digital (A/D) converters would be used in many applications, one of which is on-board processing in digital satellite communication links. Satellite systems will greatly benefit from increases in digital signal processing (DSP) data rates and reliability will increase by processing information on-board as opposed to using the satellite simply as a transponder.

In designing analog-to-digital converters for such applications, various A/D characteristics must be understood in order to properly interface the converter into the digital processing scheme which has been developed. It is also necessary to assess various A/D architectures which would be appropriate for the application and recognize which circuit elements would benefit by higher speed operation; an advantage which GaAs can offer in an integrated circuit over silicon.

This chapter looks at analog-to-digital conversion and discusses relevant topics when considering A/D implementation using GaAs integrated circuit (IC) technology. The chapter begins with a discussion of a

potential application for a high-speed A/D converter in an FDMA/TDM satellite link. Signal conversion, signal representations and quantization noise inherent in the A/D conversion process are discussed. Analog-to-digital conversion architectures and circuit requirements are then reviewed.

2.2 ON-BOARD SIGNAL PROCESSING FOR SATELLITE FDMA/TDM COMMUNICATIONS

In past decades, satellite communication has mainly dealt with the transmission of telephone and video signals. Recently, the emergence of new satellite systems has transpired to handle new markets [2.1-2.2]. These systems primarily deal with digital transmission by private business networks of voice, data and video-conferencing and employ a limited form of on-board signal processing. Access to systems can be shared by users using frequency division multiple access (FDMA) or time division multiple access (TDMA) which allocate separate frequencies or time slots to respective users. Presently, the United States, with the Advanced Communications Technology Satellite (ACTS) program, as well as Europe and Japan are developing high capacity networks using satellite-switched, time-division multiple access (SS-TDMA) systems [2.3].

The satellite transmission of digital information is a viable communication means, but it must be cost-effective for commercial use. The SS-TDMA approach is not ideal when low cost is considered. A comparison of transmission technologies illustrates that TDMA systems allow high capacity links to be implemented but require a high effective isotropically radiated power (EIRP) on uplink [2.4]. This translates into high-cost, high-power

amplifiers and a high-gain antenna at the transmitting earth station. The alternative is to employ frequency division multiple access (FDMA) on uplink to the satellite. However, an entire FDMA system is not favourable since [2.4]:

- a) In FDMA systems, large backoff in the downlink amplifiers is required to reduce intermodulation of the carriers, while in TDMA the power efficiency of the downlink amplifiers is higher since they can operate close to saturation;
- b) FDMA cannot be used with dynamically scanned downlink beams;
- c) Satellite switching increases in complexity with FDMA systems.

Therefore, a satellite system configuration employing FDMA on uplink and TDM on the downlink would provide efficient, low-cost transmission of information. This configuration has been proposed in future systems as in the Hughes Communications Galaxy plan [2.5].

A FDMA/TDM link for a direct-to-user service has been proposed for Canada [2.4], as shown in Figure 2.1. The uplink coverage consists of 10 fixed spot beams covering various industrial centres with possible coverage in outlying areas. The fixed beams would operate in the K_a band (30/20 GHz) while outlying areas would utilize a separate antenna in the K_u band (14/12 GHz). The fixed beams could accommodate 24 channels, each having a bandwidth of 36 MHz, with one beam carrying 1-3 channels depending on traffic volume. Three parallel FDMA processing paths are implemented and utilize the same frequency spectrum, as shown in the spectral allocation of FDMA signals in Figure 2.2. Each channel is separated into 16 FDM slots containing one digital carrier in each slot. The carriers would be modulated by either QPSK or BPSK at rates of 3.088 Mbps or 1.544 Mbps. These rates, called the T1 rates, are becoming standard for corporate business communication services [2.6].

Figure 2.1 A Multibeam FDMA/TDM Satellite Link

Figure 2.2. The Uplink Spectral Allocation of FDMA Signals.

In Figure 2.1, each of the three processing paths undergoes similar processing, including low-noise amplification and downconversion to a common IF in the receiver. At this point, demultiplexing of the FDMA signals is performed involving separation of the channels and of the carriers within each channel. A total of $8 \times 16 = 128$ digitally-modulated signals after demultiplexing would require demodulation, using conventional QPSK or BPSK means. Finally, baseband processing is performed on the demodulated digital data using forward-error-correction, switching, time-division multiplexing and encoding prior to downlink TDM modulation.

The demultiplexing of FDMA signals can be performed using digital signal processing (DSP) or by surface-acoustic-wave (SAW) technology. SAW devices suffer from inherent large losses and lack dynamic range [2.7]. There are significant factors which motivate DSP schemes which include [2.8]:

- a) the ability to error correct transmitted information signals;

- b) elimination of redundancy in signal processing;
- c) development of efficient algorithms, such as the Fast Fourier Transform (FFT);
- d) increase in speed and density of digital integrated circuits.

The above factors have motivated work in the development of digital group transmultiplexers to convert FDM signals into TDM signals and vice-versa [2.9-2.10]. An essential element in these transmultiplexers is the A/D converter which digitizes incoming FDMA signals.

A possible architecture of the digital group demultiplexer to be implemented in the FDMA to TDM translation is shown in Figure 2.3 [2.4]. The FDMA input is sampled at a frequency higher than the minimum required for the input bandwidth plus the common IF. The minimum sampling frequency would be 288 MHz if all signals were translated to baseband for the FDMA input from Figure 2.2. The sampled signal is A/D converted and then subsampled into N demultiplexer outputs. The A/D converter must provide sufficient samples, such that each filter input will contain contributions from each FDMA slot and must have sufficient resolution for given signal-to-noise ratios (SNR). Twelve bit A/D's have been proposed in preliminary configurations. These contributions are applied to digital filters which produce real and imaginary coefficients at their output. A N-Point FFT processor performs the desired operation from the filter outputs to produce the demultiplexed signals.

Since the design of the A/D converter is of interest, principles involved in A/D development in a high-speed application must be considered.

Figure 2.3 An Architecture of a Digital Group Demultiplexer.

2.3 SIGNAL TRANSFORMATION IN ANALOG-TO-DIGITAL CONVERSION

Analog-to-digital converters transform continuous signals into discrete 'digital' form and the analog input waveforms must be quantized both in time and amplitude. Time quantization is determined by the Nyquist criterion, which sets a limit on the sampling frequency required to preserve signal information. For lowpass signals, the sampling rate must be at least twice the highest frequency component present in the input signal, which implies the condition:

$$\frac{2\pi}{T_s} > 2 \omega_A \quad (2.1)$$

where T_s is the sampling period and ω_A is the bandwidth of the information [2.11]. Sampling below the Nyquist rate results in aliasing of signals, shown in Figure 2.4, and original signal information cannot be recovered.

Figure 2.4 Signal spectra for: (a) continuous-time signals $A(t)$ and $B(t)$; (b) sampled-data signals obtained from $A(t)$ and $B(t)$

Similar conditions hold for bandpass signals. The uniform sampling criteria for bandpass signals states that sampling frequencies, producing alias copies, must satisfy:

$$\frac{2\pi}{T_s} > 2\omega_A \quad (2.2)$$

and

$$\frac{n\pi}{T_s} + \frac{\omega_A}{2} < \omega_c < \frac{\pi(n+1)}{T_s} - \frac{\omega_A}{2} \quad (2.3)$$

where ω_A is the information bandwidth, ω_c is the centre frequency of the information, and n is an integer [2.11]. The resulting operation provides copies which can be filtered to recover the input signal, shown in Figure 2.5.

Figure 2.5. Bandpass Signal Recovery From Sampling.

Amplitude quantization is performed by partitioning the continuous signal into discrete ranges, where analog values within a range are represented by the same digital code. For code lengths of N bits, the input waveform range is divided into 2^N quantization levels. The quantization of an input continuous waveform into binary form is illustrated in Figure 2.6.

Figure 2.6. The Quantization of a Continuous Signal in Time and Amplitude into Binary form.

Signal representation in digital format may take one of many forms depending on voltage reference levels. Codes which disregard polarity are more simple and include binary, binary-coded decimal (BCD) and gray codes. These codes represent the analog input usually from a normalized range of 0 to 1. The well-known binary code consists of bits, each having an arithmetic weighting, which can be labelled b_0 to b_{N-1} where b_0 is the least significant bit (LSB) and b_{N-1} is the most significant bit (MSB). A binary word can represent an equivalent analog value given by:

$$\begin{aligned}
 A &= K (2^{N-1} b_{N-1} + 2^{N-2} b_{N-2} + \dots + 2^0 b_0) \\
 &= K \sum_{i=1}^N 2^{N-i} b_{N-i}
 \end{aligned} \tag{2.5}$$

where A represents the analog value and K is a scale factor to account for signal amplification within the system [2.12]. Table 2.1 illustrates equivalent fractional representations in a binary code with a code length of 4 bits and $K = 1/16$.

FRACTION	CODE			
	MSB	Bit 3	Bit 2	LSB
0	0	0	0	0
1/16	0	0	0	1
1/8	0	0	1	0
3/16	0	0	1	1
1/4	0	1	0	0
5/16	0	1	0	1
3/8	0	1	1	0
7/16	0	1	1	1
1/2	1	0	0	0
9/16	1	0	0	1
5/8	1	0	1	0
11/16	1	0	1	1
3/4	1	1	0	0
13/16	1	1	0	1
7/8	1	1	1	0
15/16	1	1	1	1

Table 2.1. Fractional Four-Bit Binary Representation.

The above codes mentioned are called unipolar since they disregard polarity of the normalized magnitudes. Many signal processing systems, however, use bipolar representations since many numerical algorithms deal with signed numbers. These codes represent a range of amplitudes in both negative and positive directions. Bipolar codes utilize an extra "sign" bit and equivalent representations of the sign and magnitude, two's complement and one's complement codes are given in Table 2.2 [2.13].

Interpretation			
Binary Number	Sign and Magnitude	Two's-Complement	One's Complement
0 111	7/8	7/8	7/8
0 110	6/8	6/8	6/8
0 101	5/8	5/8	5/8
0 100	4/8	4/8	4/8
0 011	3/8	3/8	3/8
0 010	2/8	2/8	2/8
0 001	1/8	1/8	1/8
0 000	0	0	0
1 000	-0	-1	-7/8
1 001	-1/8	-7/8	-6/8
1 010	-2/8	-6/8	-5/8
1 011	-3/8	-5/8	-4/8
1 100	-4/8	-4/8	-3/8
1 101	-5/8	-3/8	-2/8
1 110	-6/8	-2/8	-1/8
1 111	-7/8	-1/8	-0

Table 2.2 Bipolar Fractional Representations.

2.4 ANALOG-TO-DIGITAL QUANTIZATION NOISE

When a sequence or word to be processed is obtained by sampling, the A/D conversion can only provide a sequence of finite length. Exact representation of the sampled signal cannot occur and the quantization error which is introduced can be treated as additive noise in the A/D process. An analysis of the effects of quantization due to rounding or

truncation allows the determination of word lengths required to achieve a desired signal-to-noise ratio (SNR) from the A/D conversion [2.13].

The block representation of sampling an analog signal is illustrated in Figure 2.7. Samples of the bandlimited analog signal, $x_a(t)$, are represented by $x_a(nT_s)$, where T_s is the sampling period. These samples are considered to have infinite precision, i.e. they are represented by an infinite number of bits. The quantizer, however, introduces an error sequence, $e(n)$, which adds to $x_a(nT_s)$ to form the sample sequence, $\tilde{x}(n)$, which has a finite word-length. The form of the quantizer depends on the number representation and whether rounding or truncation is used. In this analysis, samples are assumed to be rounded and represented by fixed point form of word length $(b+1)$ bits. In fixed-point representation, the analog input signal is normalized and confined to the region:

$$-\left(1 + \frac{2^{-b}}{2}\right) < x_a(nT_s) < \left(1 - \frac{2^{-b}}{2}\right) \quad (2.6)$$

The above condition must hold to avoid clipping of the input sample which would introduce additional distortion.

Figure 2.7. The Representation of Sampling an Analog Signal: (a) nonlinear model; (b) statistical model.

The effect of quantization, as shown in Figure 2.7, results in the equivalent representation:

$$\hat{x}(n) = x(n) + e(n) \quad (2.7)$$

where $x(n)$ is the exact sample and $e(n)$ is called the quantization error.

When rounding is performed, the range of $e(n)$ becomes:

$$-\frac{\Delta}{2} < e(n) \leq \frac{\Delta}{2} \quad (2.8)$$

where Δ is the quantization width and is equal to $\Delta = 2^{-b}$. The amplitude quantization range due to rounding is depicted in Figure 2.8.

Figure 2.8. Two's-complement Rounding of samples for $b = 2$.

Generally, the exact value of $e(n)$ is not known and therefore a statistical model must be used. The following common assumptions of $e(n)$ can be made [2.13]:

1. The sequence of error samples $\{e(n)\}$ is a sample sequence of a stationary random process.

2. The error sequence is uncorrelated with the sequence of exact samples $\{x(n)\}$.
3. The random variables of the error process are uncorrelated; i.e. it is a white-noise process.
4. The probability distribution of the error process is uniform over the range of quantization error.

These assumptions will generally hold and become more realistic when the input signal becomes more complex and traverses more quantization steps from sample-to-sample. With these assumptions in mind, the probability distribution function (pdf) of the quantization error, using rounding, is shown in Figure 2.9.

Figure 2.9. The Probability Density Function for Rounding.

The mean and variance of the quantization noise are:

$$m_e = 0 \quad (2.9)$$

$$\sigma_e^2 = \frac{\Delta^2}{12} = \frac{2^{-2b}}{12} \quad (2.10)$$

Relating the signal power to noise power using signal to noise ratio yields:

$$\frac{\sigma_x^2}{\sigma_e^2} = \frac{\sigma_x^2}{2^{-2b}/12} = (12 \cdot 2^{2b}) \sigma_x^2 \quad (2.11)$$

Using logs:

$$\begin{aligned} \text{SNR (dB)} &= 10 \log_{10} \left(\frac{\sigma_x^2}{\sigma_e^2} \right) \\ &= 6.02b + 10.79 + 10 \log_{10} (\sigma_x^2) \end{aligned} \quad (2.12)$$

Thus the signal to noise ratio increases by approximately 6 dB for each bit added to the word length.

One can use the above relation in determining the effects of scaling the input signal to reduce clipping and distortion as previously mentioned. By quantizing inputs $Ax(n)$ as opposed to $x(n)$ where $0 < A < 1$, the variance of $Ax(n)$ becomes $A^2\sigma_x^2$, and the SNR becomes:

$$\begin{aligned} \text{SNR} &= 10 \log_{10} \left(\frac{A^2 \sigma_x^2}{\sigma_e^2} \right) \\ &= 6b + 10.8 + 10 \log_{10} \sigma_x^2 + 20 \log_{10} A \end{aligned} \quad (2.13)$$

The above relation shows that one should exercise extreme caution in scaling input to avoid clipping, since by decreasing A in the range $0 < A < 1$ reduces the signal-to-noise ratio.

2.5 HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER ARCHITECTURES

With the availability of many A/D architectures, designers are faced with the task of choosing appropriate structures to suit their needs. The requirements of fast conversion rate, high resolution, low power consumption and small size are all advantageous; yet these properties are unlikely to be found in a specific configuration. The following will describe three architectures which may be implemented in high-speed applications, suitable for GaAs IC implementation [2.14]. These structures

can be classified as parallel, feedback and feed-forward (or combinations thereof). Slower A/D schemes, such as series networks, are not discussed.

2.5.1 Parallel (Flash) A/D Converter

The fastest architecture available is the parallel or flash A/D converter, shown in Figure 2.10 [2.15]. The structure is configured such that the input signal is compared with all possible quantization levels simultaneously. The comparison requires $2^N - 1$ comparators, where N is the word length, and a resistor ladder network which directly determines the quantization ranges. If the sampled input voltage at node A, from the sample-and-hold operation, is above the highest quantization voltage, all the comparators indicate that the sampled value is greater than their respective reference voltage. As the sampled voltage decreases, the comparators sequentially switch states down the ladder depending on the value at node A and values determined by the resistor ladder. The results of the comparison are fed to an encoder which produces the digital equivalent word. The conversion time is short and limited only by switching times of the comparators and of the gates within the encoder.

The disadvantages of the flash architecture are evident when higher resolution is required. The word length N increases with higher resolution and thus the number of comparators in the structure increases exponentially. For IC implementation, this consumes both chip area and power. In addition, the comparators will be required to detect lower differential input voltages and exhibit negligible hysteresis for a given input voltage swing. High comparator count also increases the input capacitance seen by the input signals thus requiring higher drive capability.

Figure 2.10. The Parallel (Flash) A/D Architecture.

2.5.2 Series Feedback (Successive Approximation) A/D Converter

Feedback arrangements can be utilized to reduce the number of comparators in an A/D configuration and a popular scheme used in this respect is the successive-approximation A/D converter[2.12]. The architecture is shown in Figure 2.11 and consists of a sample-and-hold, a single comparator, a digital-to-analog converter, a logic circuit and a register. The series feedback arrangement operates by performing a sequence of comparisons of a sampled input and with each test eliminating half of the remaining quantization range. In the first cycle, the logic control provides a digital word to the D/A converter which generates a reference voltage, V_x , of value:

Figure 2.11. The Block Configuration of a Series Feedback (Successive Approximation) A/D Converter.

$$v_x = \frac{v_{\text{ref}}}{2} \quad (2.14)$$

where v_{ref} is the D/A converter analog reference. The single bit comparator indicates whether v_x lies above or below the sampled input voltage. The logic circuit interprets this result, produces the most significant bit of the digital output word, and then updates the digital word to the D/A converter. In the next cycle, v_x becomes:

$$v_x = \frac{v_{\text{ref}}}{4} + b_{N-1} \frac{v_{\text{ref}}}{2} \quad (2.15)$$

and another comparison takes place to provide the next bit. This sequence continues until the entire N-bit word is generated, which takes at least N cycles, and is finally stored in the N-length bit register. Thus, only one single comparator is necessary in the conversion process which eliminates the many constraints inherent in the parallel converter.

The major drawback to the structure is that it is slower than the parallel A/D since it requires N cycles plus additional cycles for updating logic states. As resolution increases, more cycles are required and thus total conversion time increases linearly. Modifications to the above structure can be performed such that more than one bit can be generated per cycle resulting in a series-parallel feedback arrangement.

2.5.3 Feed-Forward A/D Converter

Feed-forward A/D converter: incorporate a pipeline structure to perform a sequential bit determination of the analog input signal as illustrated in Figure 2.12 [2.14]. The total conversion process requires N stages, where each stage determines one bit in the sequence and contains a sample-and-hold, comparator, D/A and storage register. The sample-and-hold maintains the previous stage analog signal for comparison with a reference stage voltage, V_{ri} , and for subtraction to eliminate quantization levels. The comparison determines whether the held voltage lies above or below V_{ri} and indicates to the D/A converter to establish a voltage for subtraction. The voltage which is fed to a subtractor eliminates half of the remaining quantization levels and the subtracted voltage then proceeds to the next stage. The delay in each stage requires storage of previously determined bits using registers.

2.6.1 Sample-and-Holds

Since A/D conversion requires a finite time to digitize a signal, it is necessary to maintain the sampled signal level during digitization. This avoids changes in input signal which could result in conversion errors. Sample-and-hold circuits utilize a control signal to acquire and track a varying analog signal during one state and then store this signal, for a predetermined time, during the other state. These characteristics are dependent on the application used. In data acquisition systems, sample-and-holds must be able to exhibit fast acquisition with minimal droop for short hold periods but in data distribution, extremely long hold times may be required.

Sample-and-hold circuits have various open-loop and feedback configurations [2.16]. A typical open-loop form for fast acquisition is shown in Figure 2.13. The analog input is sampled at predetermined intervals by the signal, V_ϕ , which allows the analog input to appear across a hold capacitor. After acquisition, the switch configuration opens and leaves the analog signal "held" across the capacitor, making it available to external circuitry via an output buffer.

Figure 2.13. An Open-loop Sample-and-Hold Configuration.

Performance characteristics of sample-and-holds determine its accuracy and speed. Desired properties in data acquisition systems include[2.16]:

- a) short acquisition time of input voltages to allow more time for digitization of the held signal;
- b) low sample-feedthrough/hold-step error during the sample-to-hold transition to minimize the analog error voltage from the sampling function;
- c) low droop rate of the held voltage to minimize the rate of decay with time in the hold mode;
- d) high hold-mode feedthrough attenuation to isolate held voltages from input voltages during the hold mode.

2.6.2 Comparators

All analog-to-digital converter configurations perform a signal comparison between an input signal and an established reference signal. The reference voltages may be constant, as those set-up by resistor ladders, or continuously updated, as those provided by digital-to-analog converters. Comparators detect differences in input voltages and produce large signal, logical outputs after a propagation delay time. In high-accuracy applications, such as high-resolution flash A/D's, comparators must be able to distinguish voltage differences in the 1 mV range.

Figure 2.14. Common Comparator Configurations.

Two common comparator configurations for IC implementation are shown in Figure 2.14 [2.17]. Both structures are usually followed by a latch which provides the necessary output signals to logic circuits. The first configuration in Figure 2.14 uses inverting stages, biased in the high-gain region, to amplify the difference in input voltages until the required output logic signal is obtained. Additional circuitry such as buffers and clocking configurations may be necessary to improve comparator accuracy. Considerable delay may result, however, when many gain stages are utilized for detection of small voltage differences. A more common comparator scheme is the differential amplifier structure shown in Figure 2.14. The basic element within the structure is the differential pair, which is shown in simplified form using FETs in Figure 2.15. The difference in input gate voltages manifests into unequal currents in the branches of the differential pair, producing a large differential output

voltage. Differential amplifiers are advantageous in that they provide high input impedance, large common-mode rejection (CMRR) and power supply rejection. Problems inherent with differential amplifiers usually involve matching of the input and load devices.

Figure 2.15. A FET Differential Amplifier.

2.6.3 Digital-to-Analog (D/A) Converters

Digital-to-analog (D/A) generally use intermediate results to aid in determining a segment of the final bit sequence in the A/D process or generate new conditions for future determinations. In feedback and feed-forward arrangements for A/D conversion, the D/A converter establishes reference voltages for comparison or subtraction with varying input voltages. Other uses for D/A converters include multipliers/dividers, phase shifters and digitally-controlled sources[2.16].

Digital-to-analog converters can be implemented using weighted resistors or appropriately weighted current sources. An R-2R D/A converter is shown in Figure 2.16[2.16] and is comprised of a voltage reference, a set of weighted resistors, switches and a summing circuit. The binary input sets conditions on the switches in the resistor array and each closed switch adds on incremental current, E_R/R_j , to the summing node at the input to the buffer amplifier. The output is proportional to the total current at the input and thus to the binary input. Figure 2.16 shows only one arrangement for the resistor and switches but other arrangements are available which decrease component count [2.16]. The switches are usually implemented using transistors and the summing amplifier can be an operational amplifier.

Figure 2.16. An R-2R Digital-to-Analog Converter.

When considering digital-to-analog converter specifications, the following properties are desirable[2.16]:

- a) high accuracy in conversion between digital inputs and analog output, in terms of integral nonlinearity, differential nonlinearity and monotonicity;
- b) low sensitivity to temperature deviation (gain drift and offset drift);
- c) fast settling time and glitch free transition;
- d) low power supply sensitivity.

2.6.4 A/D Logic Circuits

Logic circuits are required in all A/D converters as interfaces with either the various circuit elements within the architecture or the external digital logic which follows. Examples include: counters for incremental increases of quantization levels, encoders to transform outputs of comparators to the digital encoded sequence and logic control circuits for updating D/A conditions. These circuits can be designed using common logic gates established by the IC technology or with logic arrays and memory structures. In their design, consideration of size, power dissipation, device and circuit compatibility is necessary.

An example of an encoding circuit, for a 3-bit flash A/D structure, is shown in Figure 2.17[2.12]. The circuit utilizes both XOR logic functions and a programmable encoded array to establish the appropriate binary code from the results of the 2^N-1 comparator outputs.

Figure 2.17. Encoding Logic for a 3-bit Flash A/D.

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CHAPTER 3

GALLIUM ARSENIDE IC TECHNOLOGY

3.1 INTRODUCTION

The advantageous properties of GaAs have enhanced performance in various application areas, such as microwave and digital integrated systems. As a result, production of integrated circuits using gallium arsenide has increased over the last two decades. This is evidenced by the large number of semiconductor firms which have established GaAs production lines, shown in Table 3.1 [3.1]. This increase is primarily due to the improved quality of gallium arsenide material and processing which have yielded high performance, reliable devices in response to the demand for high-speed and radiation resistant circuits in military and commercial applications.

<u>Foundry</u>	<u>Location</u>
Adams-Russell	Burlington, MA
Anadigics	Warren, NJ
Ford Microelectronics	Colorado Springs, CO
Gain Electronics	Somerville, NJ
Gigabit Logic	Newbury Park, CA
Harris Microwave	Milpitas, CA
Honeywell Inc.	Richardson, TX
Hughes	Malibu, CA
ITT	Roanoke, VA
Pacific Monolithics	Sunnyvale, CA
Plessey III-V Group	Northamptonshire, UK
Raytheon	Northborough, MA
Sanders	Nashua, NH
Tachonics	Plainsboro, NJ
Texas Instruments	Dallas, TX
TriQuint	Beaverton, OR
Varian	Santa Clara, CA
Vitesse Electornics	Camarillo, CA

Table 3.1 Semiconducting Firms Involved in GaAs Processing.

This chapter reviews the aspects involved in GaAs integrated circuit technology. The first section begins with an introduction to some of the unique, beneficial physical properties of GaAs and compares the positive and negative aspects of GaAs with respect to Si. The various circuit elements used in design for fabrication of GaAs integrated circuits are then explained including diodes, transistors, resistors and capacitors. Modelling of these various elements is analyzed for computer simulation and the chapter concludes with a review of depletion-mode MESFET fabrication used to process the circuits in the upcoming chapters.

3.2 GALLIUM ARSENIDE VERSUS SILICON

When considering a semiconducting material for IC implementation, it is necessary to analyze the properties which make the semiconductor advantageous for use in certain application areas. Clearly, gallium arsenide exhibits unique properties compared to other semiconducting materials and has inspired a large degree of research activity. Since silicon has always been the dominant material in integrated circuit processing, it is useful to compare the properties of GaAs and Si. This section provides a brief explanation of the semiconducting advantages GaAs has over Si but is not intended, by any means, to be a thorough review. The section will also describe the aspects of each material in terms of performance when considering implementation in IC form.

3.2.1 Lattice Structure and Physical Properties

The physical properties of GaAs and Si stem from the crystal structure of the two materials. Gallium arsenide is a III-V compound

semiconductor with gallium and arsenide atoms arranged in a 'zincblende' lattice. The unit cell structure, shown in Figure 3.1, consists of two interpenetrating face-centred cubic sublattices displaced $(\frac{1}{4}, \frac{1}{4}, \frac{1}{4})$ in lattice coordinates with respect to one another. One sublattice consists of Ga sites while the other is occupied by As sites. The crystal structure for silicon, also shown in Figure 3.1 and called a diamond lattice, is similar to that of GaAs but all atoms are identical. Some of the unique physical and electrical properties of these semiconductors which result from their lattice structure are summarized in Table 3.2 [3.2].

a) Gallium Arsenide

b) Silicon

Fig. 3.1. The Lattice Structures of GaAs and Si.

	<u>GaAs</u>	<u>Si</u>	<u>Units</u>
Lattice Constant, a	5.65	5.43	Å
Density	5.317	2.328	g/cm ³
Atomic Density	4.42 x 10 ²²	5.0 x 10 ²²	atoms/cm ³
Atomic Weight	144.63	28.09	
Bulk Modulus	7.55 x 10 ¹¹	9.8 x 10 ¹¹	dyn/cm ²
Sheer Modulus	3.26 x 10 ¹¹	5.1 x 10 ¹¹	dyn/cm ²
Melting point	1238	1415	°C
Linear expansion coefficient	6.86 x 10 ⁻⁶	2.6 x 10 ⁻⁶	°K ⁻¹
Specific heat	0.35	0.7	J/g°K
Lattice Thermal Conductivity	0.46	1.5	W/cm°K
Dielectric Constant	13.1	11.9	
Bandgap	1.424	1.12	eV
Threshold field	3.3	60	KV/cm
Peak drift velocity	2.1 x 10 ⁷	6.5 x 10 ⁶	cm/s
Electron mobility (undoped)	8500	1500	cm ² /V.s
Hole mobility (undoped)	400	450	cm ² /V.s

Table 3.2 Physical Properties of GaAs and Si at 300°K

3.2.2 Electrical Properties

In comparing electrical properties, the behaviour of transport carriers in gallium arsenide and silicon when subjected to electric fields must be considered. When an electric field is applied to a semiconductor material, electrons will attain an additional velocity component superimposed on their thermal motion. This velocity component is called drift velocity, v_n , which differs comparatively in both materials. Experimental data measuring drift velocity versus electric field is shown in Figure 3.2 for GaAs and Si [3.3]. If the low field behaviour is initially considered, the figure indicates a linear relationship between drift velocity and field strength in the two semiconducting materials. In this case, v_n can be obtained by equating the momentum applied to an electron during free flight between collisions ($-q\xi\tau_c$) to the momentum gained in the same period ($m_n v_n$) [3.2]. This relation yields:

$$v_n = -\left[\frac{q \tau_c}{m_n}\right] \xi \quad (3.1)$$

where the negative sign indicates that electron motion is opposite to the applied electric field, ξ . In (3.1) m_n is the effective mass of electrons, q is electron charge and τ_c is the mean free time between collisions. The effective mass, m_n , differs from the mass of a free electron, m_0 , because of electron interaction with the periodic potential of the nuclei within the lattice.

Figure 3.2 Comparison of the Velocity-Field Characteristics for Electrons in GaAs and Si.

The proportionality factor between v_n and ξ is known as electron mobility, μ_n :

$$\mu_n = \frac{q \tau_c}{m_n} \quad (3.2)$$

Mobility, which is defined more specifically as the electron velocity per unit field gradient, is an important factor since it describes the degree electrons are influenced by an applied electric field. By taking the slopes in the low field region, the low field electron mobility, μ_n , is $8500 \text{ cm}^2/\text{V}\cdot\text{s}$ in undoped GaAs at 300°K and is approximately 6 times greater than in undoped Si ($1500 \text{ cm}^2/\text{V}\cdot\text{s}$). This low field property is responsible for the major electrical advantage GaAs has over Si.

Figure 3.2 also indicates the high field effects on drift velocity and how the behaviour in the two semiconducting materials differ. In silicon, the electron drift velocity increases monotonically to a saturated value of 6.5×10^6 cm/s while the velocity in GaAs reaches its maximum value, 2.1×10^7 cm/s at 3.3 kV/cm, and then decreases. This phenomenon simulates a 'negative resistance' effect and can be more clearly understood when band structures of the material is considered.

3.2.3 Band Structure

The band structure is significant in any semiconductor since carrier transport mechanisms are directly related to the energy-momentum (E-k) state of electrons and holes in the conduction and valence bands of the materials. The band structures, which relate electron energy to its momentum, are shown in Figure 3.3 for GaAs and Si in two dimensional (E-k) form and Figure 3.4 in three dimensional (E-k) form [3.4]. The figures show that each semiconductor has similar valence bands with energy maxima appearing at zero crystal momentum (Γ). However, the shape and locations of the conduction band minima differ since the energy band extrema in GaAs occur at zero crystal momentum (Γ) while the minimum in silicon occurs in the X reciprocal lattice direction [100]. Therefore, in silicon, electrons must experience both a change in energy and in crystal momentum to make the transition from valence to conduction bands. Consequently, GaAs is a direct-bandgap semiconductor and Si is an indirect-bandgap semiconductor.

Figure 3.3 Two-Dimensional Bandgap Representations of Silicon and Gallium Arsenide.

Figure 3.4. Three-Dimensional Bandgap Representations of Si and GaAs.

Characteristics of the band structure provide useful information about the semiconductor. For instance, the energy difference between the conduction band minimum and the valance band maximum is an important semiconductor property and is referred to as the energy bandgap, E_g . It defines the energy a valence electron must attain to become a conduction electron and is 1.42 eV at 300°K for GaAs and 1.12 eV for Si. A comparison of conduction bands also reveals a wider conduction band minima present in GaAs which is $\Delta E = 0.31$ eV above the Γ minimum in the L[111] direction. If conduction electrons acquire enough energy from the electric field, they can transfer from the lower energy minimum to the higher energy minimum. This transition causes a decrease in drift velocity at these field strengths as is indicated in Figure 3.2.

3.2.4 IC Implementation Considerations

Having described some specific electrical properties of GaAs and Si, a more general comparison concerning IC implementation is now provided. These pros and cons are summarized in Table 3.3 and followed by a brief outline of each property.

	<u>GaAs</u>	<u>Si</u>	<u>Units</u>
Resistivity (Max.)	10^8	$10^5 - 10^6$	ohm cm
Total Dose Failure Threshold	$>10^7$	$5 \times 10^{4*}$	rads
Operating Temp. Range	-200 to 200	-55 to 100	$^{\circ}\text{C}$
Speed Power Product	0.9	5	pJ
Defect Densities	1×10^5	10	cm^{-2}
Native Oxide	none	SiO_2	
Thermal Dissipation	0.45	1.5	W/cm^2

* Bipolar ECL

Table 3.3 Comparison of IC Implementation Properties for GaAs and Si.

a) Resistivity

Wafer resistivity in GaAs exceeds 10^8 ohm-cm as compared to 10^5 ohm-cm for Si [3.5]. This characteristic allows devices to be fabricated on semi-insulating GaAs material having low parasitic capacitances. The semi-insulating substrate also improves reliability due to the reduction of parasitic leakage paths responsible for circuit failure.

b) Radiation and Temperature Tolerances -

In terms of radiation, GaAs circuits exhibit higher total dose failure thresholds ($>10^7$ rads) compared to silicon technologies including bipolar and MOS circuits [3.6]. Due to intrinsic material properties, GaAs devices can withstand wider temperature variations with respect to their silicon counterparts. These properties make integrated circuits produced on GaAs attractive for space and military applications.

c) Speed-Power Product

Since channel electron mobilities are higher in GaAs, GaAs circuits can be 3-10 times faster than Si for similar power dissipations. High speed at low power is attractive specifically for digital applications.

d) Optoelectronic Properties

Due to the direct bandgap nature of GaAs as a semiconductor, it can detect, emit and convert optical signals into electrical signals. The simultaneous exploitation of electronic and optical properties of GaAs allows for the integration of optoelectronic systems on a single chip.

e) Defect Densities

Defect densities due to crystal growth are of the order of 10^4 times higher in GaAs than in Si [3.5]. Although the exact effect of this parameter are unknown, the presence of defects have been linked to the variation of electrical properties in GaAs devices. The trend to improve uniformity across a wafer is ongoing.

f) Stable Native Oxides

GaAs has no stable native oxide for passivation, as silicon has with SiO_2 . Consequently GaAs technology has to rely on thin film dielectrics, such as Si_3N_4 or SiO_2 , for integration. Metal-oxide semiconductors (MOS) devices using native oxides cannot be fabricated on GaAs.

g) Thermal Dissipation

Silicon has a higher coefficient of thermal conductivity (1.5 W/cm.K) at room temperature with respect to GaAs (0.55 W/cm. $^\circ$ K). Heat dissipation is much more critical in GaAs IC technology.

h) Fabrication and Handling

Silicon is a much more abundant substance, less costly to obtain than elemental gallium and arsenic. Due to the fragile nature of GaAs, it is also extremely difficult to handle. In the production of GaAs ingots, a

high constant pressure environment is required for the elemental As to react.

3.3 GALLIUM ARSENIDE CIRCUIT ELEMENTS

The advances in GaAs processing over the past two decades have produced the necessary circuit elements for design of integrated circuits. The development of these elements was made possible only by understanding the limitations and benefits of GaAs material properties as described in the previous section. These structures, used for the designs in the upcoming chapters, will now be presented.

3.3.1 Schottky Barrier Diodes

Diodes are utilized in circuits requiring signal switching or voltage level shifting. GaAs processes fabricate Schottky barrier diodes in planar form as shown in Figure 3.5. The diode incorporates the two major elements of many GaAs devices; the ohmic contact and the Schottky barrier contact. The ohmic contact is nonrectifying and provides a negligible resistance path to the active semiconductor layers. Ohmic contacts can be formed by depositing a Ni-Au-Ge metal composite on GaAs and then alloying the materials at a high temperature [3.7].

Figure 3.5 A Planar Schottky Barrier Diode.

A Schottky barrier contact is fabricated by deposition of Ti-Pt-Au material on active GaAs layers [3.7]. Under the Schottky metal contact, there exists a region which is depleted of carriers with a width which depends on voltage, metal and semiconductor properties. The depletion region width, assuming that an abrupt transition between depleted and undepleted regions exists, is defined by [3.2]:

$$W = \left[\frac{2\epsilon_s \epsilon_0}{q N_D} (V_{bi} - V - \frac{kT}{q}) \right]^{1/2} \quad (3.3)$$

where N_D is doping concentration, V_{bi} is the built-in voltage, V is the applied voltage, ϵ_s is the relative semiconductor permittivity and ϵ_0 is the permittivity of free space. Equation (3.3) is similar to that obtained with a p-n junction and thus indicates that the resulting structure exhibits the electrical behaviour of a diode. With no applied bias, a depletion region exists due to the built-in voltage, V_{bi} . For forward bias voltages, V , the depletion width decreases until forward breakdown while reverse biasing increases the depletion region until

reverse breakdown occurs. Since a region which is depleted of carriers exists, the structure also acts as an insulator between the metal and the surrounding undepleted semiconducting material. As a result, the device can be modelled as a parallel plate capacitor having a value:

$$C = \frac{\epsilon_s \epsilon_0 A}{W} \quad (3.4)$$

where A is the area of the Schottky metal contact.

3.3.2 Transistors

Many IC transistor devices have been developed using gallium arsenide because of the intensive, ongoing research performed to improve material properties, process and device characteristics. These transistors have properties which are process-dependent and the more complicated structures require extremely tight processing control. This section describes the more popular transistors used in design of GaAs integrated circuits [3.3] and then briefly introduces more complex heterostructure devices which improve circuit performance. The structures which are described include: the depletion metal-semiconductor field-effect transistor (D-MESFET), the enhancement metal-semiconductor field-effect transistor (E-MESFET), the high-electron-mobility transistor (HEMT), and the heterojunction bipolar transistor (HBT).

a) The Depletion-Mode MESFET

The best known of the GaAs IC transistors is the depletion-mode MESFET, shown in Figure 3.6. The D-MESFET has been utilized in a number of digital logic circuits including buffered FET logic (BFL), Schottky diode FET logic (SDFL), capacitor-coupled FET logic (CCFL) and source-coupled FET

logic (SCFL), and has been used as the active amplifying element in monolithic microwave integrated circuits (MMIC's) [3.8].

Figure 3.6. The Depletion-mode MESFET.

This device consists of an active, conducting channel formed by epitaxial growth of n-type GaAs layers on semi-insulating (S.I.) GaAs or by n-type ion implantation into a semi-insulating GaAs substrate. The channel is approximately 100 to 200 nanometers deep and has doping concentrations of approximately 10^{17} atoms per cubic centimeter. The channel is n-type to benefit from the high mobility of electrons in GaAs. Each end of the channel is defined by an ohmic contact source and drain region which provides a low resistance path to the channel. The passage of current between the drain and source contacts is controlled by a gate, typically 1 μm in length, which is placed directly on the active channel and forms a Schottky barrier contact. With a voltage bias between the drain and source contacts, the depletion region under the gate can be controlled by adjusting the gate voltage. As the gate voltage becomes more negative, the depletion width increases until the pinchoff voltage is reached and current flow between drain and source effectively stops.

Pinchoff voltages range from -0.7V to -2.5V depending on the IC process [3.3]. Since reverse biasing of the Schottky barrier gate is involved in normal operation, negligible gate current flows in the device and the MESFET represents a high input impedance device.

b) The Enhancement-Mode MESFET

The enhancement-mode MESFET, shown in Figure 3.7, is similar in structure to the D-MESFET except that the implanted depth and n-type doping concentration of the channel differ [3.8]. These properties are modified to raise the pinchoff voltage to 0 volts so that the Schottky contact depletion width is sufficient to cut off channel conduction. A positive applied bias is required for the onset of conduction. This voltage is

Figure 3.7 The Enhancement-mode MESFET.

limited to $+0.5\text{V}$ since gate voltages exceeding $+0.7\text{V}$ cause excessive gate currents to be drawn. The E-MESFET is used in direct-coupled FET logic (DCFL) circuits and although the logic swing is low, the device eliminates

the need for dual power supplies and consumes less power than D-MESFET logic structures since it does not require a source follower for level shifting [3.8]. The disadvantage of using the E-MESFET is that in its fabrication more stringent process control is required, since channel thicknesses must be less than 5 nm across the wafer to provide small variations in pinchoff voltages [3.3].

c) The High-Electron Mobility Transistor

The high-electron mobility transistor (HEMT), shown in Figure 3.8, is also commonly known as the two-dimensional electron-gas FET (TEGFET), the modulation-doped FET (MODFET) and the selectively doped heterostructure transistor (SDHT) [3.9]. The cross-section of the device reveals that it contains various layers of semiconducting material. Usually, each layer is grown by molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) which deposit very thin molecular layers of semiconducting material in a vacuum [3.10]. In the construction of the HEMT, an undoped GaAs layer, approximately 1 μm thick, is grown on semi-insulating GaAs. Next, a very thin layer of undoped AlGaAs and a highly doped AlGaAs layer are grown. The final layer is a heavily doped GaAs material for device contact fabrication.

Figure 3.8. The High-Electron Mobility Transistor.

The two materials, GaAs and AlGaAs, have different bandgaps (1.42 eV and 1.8 eV respectively), and when in contact, the conduction bands bend sharply at their interface. The high concentration of electrons in the AlGaAs conduction band diffuse into the undoped GaAs layer, and remain in a 'well' at the interface in what is referred to as the 'two-dimensional' electron gas region. Because the GaAs layer is undoped, the electrons present in this region have a higher mobility and their motion is not limited by scattering with donor ions. This non-restriction of electron movement gives the HEMT a higher speed advantage over MESFET devices. Both enhancement and depletion-mode devices are possible in HEMT form and the E-D combination will provide larger gate voltage swings ($\sim 1.0\text{V}$) compared to E-D MESFET structures [3.8]. The drawback with HEMT's lies in the high complexity of processing these transistors.

Fabrication of the HBT is its major downfall since MBE growth of thin semiconductor material must be performed in conjunction with ion-implantation for base-contact and device isolation regions.

3.3.3 Resistors

Resistors fabricated on GaAs can be divided into two general classes: active layer GaAs resistors and thin-film resistors.

a) Active Layer GaAs Resistors

The simplest method of resistor fabrication utilizes the resistivity of GaAs material itself. Resistors of this form are produced using the lithographic steps of device isolation and ohmic contact which are generally performed in most processes. A cross section of this resistor is shown in Figure 3.10 [3.3] and its numerical value is determined by the resistance of the GaAs material and the two contact resistances:

$$R = R_s \frac{L}{W} + 2 \frac{R_c}{W} \quad (3.5)$$

where R_s is the active layer GaAs sheet resistance ($\Omega/\text{sq.}$), R_c is the contact resistance per unit width, L is the distance between ohmic contacts and W is the resistor width. Typical sheet resistances range from 1000 ($\Omega/\text{sq.}$) for lightly doped GaAs to 125 ($\Omega/\text{sq.}$) for more heavily doped material [3.12].

Figure 3.10 An Active Layer GaAs Resistor.

Problems inherent with active layer GaAs resistors result from current handling and temperature effects. Resistors unable to handle the current passing through them experience current saturation which alters resistance when electric fields near the critical value are applied. When operating above the critical field, Gunn domain oscillations may also appear. High currents lead to temperature increases and since GaAs is a poor thermal conductor, heat will dissipate more slowly from high current drawing areas. However, the most critical temperature effect involves the temperature coefficients of the GaAs material, which are usually high, and result in significant resistance changes over wide temperature operation. Temperature coefficients of resistance for N^- and N^+ dopings are approximately $0.13\%/^{\circ}\text{C}$ and $0.07\%/^{\circ}\text{C}$ respectively [3.12]. These drawbacks may warrant the use of thin-film resistor structures.

b) Thin-Film Resistors

Thin-film resistors may be preferable in applications which require better matching and precision, greater isolation and less temperature dependence. These resistors are defined by a lift-off process, which deposits resistive material on the GaAs substrate. The materials

must be compatible with the process and must exhibit good adhesion to the GaAs substrate. Thin-film resistors, shown in Figure 3.11, have smaller and more exact resistivities and lower temperature coefficients of resistance than active layer GaAs resistors. The nichrome, NiCr, resistor is a common thin-film type and has a resistivity of $50 \Omega/\text{sq.}$ and a temperature coefficient of $0.0006\%/^{\circ}\text{C}$ [3.12]. The drawbacks of thin-film resistors are that more masking steps are required to incorporate them in a process and the parameters of resistivity and thickness must be tightly controlled to achieve a high degree of accuracy.

Figure 3.11 A GaAs Thin-film Resistor.

3.3.4 Capacitors

Capacitance can be implemented in GaAs IC technology with the use of various structures such as transmission line stubs, coupled interdigitated lines and Schottky diodes [3.7]. However, the most common capacitance structure is the metal-insulator-metal (MIM) capacitor, shown in Figure 3.12, since it produces large capacitances for blocking or bypass while utilizing a small area. MIM capacitors are a thin-film structure consisting of two metal plates separated by a dielectric. The two most

popular dielectrics are Si_3N_4 ($\epsilon_r = 7.5$) and SiO_2 ($\epsilon_r = 5$) since they are usually part of the IC process. The metal plates are usually thicker than twice the skin depth to yield adequate Q values for high frequency operation and must be smooth to minimize variation in effective plate area and eliminate subsequent defects in dielectric growth [3.7].

Figure 3.12 A Metal-Insulator-Metal (MIM) Capacitor.

Due to the parallel plate structure of MIM capacitors, the standard expression for determining capacitance applies and is given by:

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \quad (3.6)$$

where ϵ_r is the dielectric constant, ϵ_0 is the permittivity of free space, d is the distance between plates and A is the effective plate area. Capacitance values for MIM structures in most GaAs processes range from 50 to 300 pF/mm² [3.7] and the value provided by TriQuint is 275 pF/mm² [3.12]. Fringing fields at plate edges can increase the above capacitance values but the effect becomes less significant for larger geometries. One significant problem inherent with this structure is possible dielectric breakdown in areas where the dielectric passes over the edge of the bottom metal as seen in Figure 3.12. The problem can be

eliminated by using airbridge metal to step over these edges and provide the necessary connection to the top plate.

3.4 DEPLETION MODE DEVICE MODELLING

The establishment of large-signal models for circuit elements in computer-aided design (CAD) and optimization is essential in developing any reliable electronic circuit. Definition of models by component structure and material properties is preferred for proper characterization. However, component behaviour may be complex and accuracy may be limited to keep the number of computations in analysis at a reasonable level. Thus, a sufficiently accurate simulation tool must be chosen to deal with the type of circuit and features to be simulated. The SPICE (Simulation Program with Integrated Circuit Emphasis) program is a popular circuit simulation package which can provide approximate behaviour of GaAs D-MESFET process components [3.13]. This section describes appropriate SPICE models for Schottky barrier diodes and depletion mode transistors which were utilized for CAD purposes. Resistors and capacitors were simply given numerical values for simulation and could then be physically characterized for fabrication as mentioned in sections 3.3.3 and 3.3.4.

3.4.1 Schottky Barrier Diode Model

The schematic representation for the SPICE model of a Schottky barrier diode is shown in Figure 3.13 [3.14]. The model consists of a non-linear current source which defines the DC characteristics of the device, a capacitor in parallel to model charge-storage effects for

large signal behaviour and a resistance in series with the previous elements to account for the deviation of the diode current at higher levels of voltage bias.

Figure 3.13 The SPICE Model of a Schottky Diode.

The DC characteristics of the current source is graphed in Figure 3.14 [3.14]. The diode current, I_d , versus voltage, V_d , relationship for forward bias is modelled by the common diode equation:

$$I_d = I_s [e^{qV_d/nKT} - 1] \quad (3.7)$$

where I_s is the saturation current, V_d is the applied voltage and n is the ideality factor. Values for I_s and n can be obtained by measurement of the $\log I_d$ vs V_d characteristics. At higher levels of forward bias, the current will deviate from the logarithmic behaviour. This is due to the presence of ohmic resistance in the diode, R_s , which is usually estimated at various I_d values and then averaged. Figure 3.14 also illustrates the reverse bias behaviour of the Schottky barrier diode. For appropriate values, the exponential term from 3.7 becomes negligible and the current is simply $-I_s$. With sufficient

reverse bias voltage, reverse breakdown in the diode occurs where the reverse diode current increases rapidly. The voltage, V_B , defines the onset of reverse breakdown at which the reverse current attains a value of $-I_{BV}$.

Figure 3.14 Non-linear DC Characteristics of a Schottky Diode.

To model charge storage effects of the diode inherent with the depletion layer, the parallel capacitor is incorporated and is described by [3.14]:

$$C_d = C_{j0} \left[1 - \frac{V_d}{V_{bi}} \right]^{-M} \quad (3.8)$$

where C_{j0} is the zero bias depletion capacitance, V_{bi} is the built-in voltage and M is the grading coefficient (usually 0.5 for square root behaviour). This capacitance is directly related to equations 3.3 and 3.4 which define depletion capacitance. The zero bias depletion capacitance, C_{j0} , can be directly determined from measured results.

To illustrate typical values for diode SPICE models in a depletion mode GaAs process, Table 3.4 gives the parameter values discussed above for a TriQuint level shifting N⁺ diode [3.12].

R_s	900	[ohm· μ m]
I_s	2×10^{-15}	[A]
n	1.16	
I_{BV}	0.1	[μ A]
V_B	7	[V]
C_{jo}	2.2	[fF]
M	0.5	
V_{bi}	0.5	[V]
FC	0	

Table 3.4 TriQuint SPICE parameters for a N⁺ Level Shifting diode.

3.4.2 Depletion Mode MESFET Model

Since there is no direct MESFET model available in SPICE, modification to an existing model similar in both structure and operation is required. A modified version of the JFET model to account for the significant performance differences in the D-MESFET has been reported [3.15] and this model was utilized in the circuit simulations of Chapter 4. The equivalent circuit representation is shown in Figure 3.15 [3.12] and will now be outlined.

Figure 3.15 Equivalent MESFET Model for SPICE Simulation.

The drain current, I_{ds} , relationship to gate-source voltage, V_{gs} , and drain-source voltage, V_{ds} , must be characterized when determining the operating conditions of the D-MESFET. Measured behaviour of the device shows that current saturation in MESFETs occurs at lower voltages than the JFET SPICE model predicts, which is illustrated in Figure 3.16. The behaviour is due to the higher low-field mobility in n-type gallium arsenide. This early saturation effect can be compensated for by using a voltage controlled voltage source, E_{VGS} , applied to a conventional JFET as shown in Figure 3.15 [3.15]. The scaling parameter of this source, μ , shifts the corresponding knee voltages to appropriate values where early saturation occurs. The numerical value

Figure 3.16. Early Saturation Behaviour in D-MESFETs.

for μ can be obtained by the ratio of the measured knee voltage for the $V_{gs} = 0$ curve to the measured pinchoff voltage, V_p , assuming negligible source and drain resistances. The drain current equations, modified by μ , provide the large signal characteristics for the D-MESFET in the following form:

$$\begin{aligned}
 I_{ds} &= 0 && ; v_{gs} < V_p \quad (\text{pinchoff}) \\
 &= W\beta\mu \left[2(v_{gs} - V_p)v_{ds} - \frac{v_{ds}^2}{\mu} \right] (1 + \lambda v_{ds}) && ; \left[0 < \frac{v_{ds}}{\mu} < v_{gs} - V_p \right] \quad (3.9) \\
 &&& (\text{linear}) \\
 &= W\beta\mu^2 (v_{gs} - V_p)^2 (1 + \lambda v_{ds}) && ; \left[0 < v_{gs} - V_p < \frac{v_{ds}}{\mu} \right] \\
 &&& (\text{saturation})
 \end{aligned}$$

where β is the transconductance parameter, V_p is the pinchoff voltage and λ is the channel-length modulation parameter. The value of λ is a measure of the output conductance of the D-MESFET in the saturation region. The output conductance has been shown to be frequency dependent [3.16] and

has resulted in the development of two models by TriQuint, NDC and NAC, which modify λ for use in the appropriate frequency application. A comparison of these two models for I_{ds} versus V_{ds} is shown in Figure 3.17 [3.12].

Figure 3.17 Comparison of Large-Signal Characteristics of the D-MESFET at Two Frequencies.

Having defined the drain current control characteristics in (3.9), the remaining elements in the MESFET model in Figure 3.15 complete the characterization. The values of R_s and R_d represent ohmic resistance of the source and drain contacts respectively and are similar to the parasitic resistance found in the diode. The resistance, R_{in} , is another parasitic which models current flow down the width of the gate and defines the resistance associated with the gate metal. The capacitances C_{ds} , C_{gdfrg} and C_{gsfrg} represent constant parallel conductor capacitances between the gate, drain and source electrodes.

The final elements in the model are the two diodes appearing across the gate-drain and gate-source regions. These elements approximate the diode behaviour inherent with the Schottky gate. As with the Schottky

barrier diode, a charge depletion region is present under the gate when negative bias is applied which produces a gate capacitance. The amount of capacitance associated with charge depletion is voltage dependent and can be described in the same form as (3.8). Since the gate-drain and gate-source voltages will differ according to region of operation, their associated capacitances will differ which requires an independent diode for modelling. This completes the SPICE model of the depletion-mode MESFET and the parameter values for a 1 μm wide structure (appropriate for scaling) is given in Table 3.5 [3.12].

```
.SUBCKT FS1 1 2 3
RD 1 11 900
J1 11 66 33 J1Q 1
EVGS 66 33 6 33 .56
RIN 2 6 .128
RS 3 33 900
CDS 1 3 .4FF
CGDFRG 6 11 1FF
CGSFRG 6 33 1FF
DGD 6 11 DQ 1
DGS 6 33 DQ 1
RFX1 1 2 50MEG
RFX3 1 3 50MEG
RFX2 2 3 50MEG
.ENDS FS1
```

Table 3.5 TriQuint SPICE Subcircuit Parameters for a 1 μm D-MESFET.

3.5 GALLIUM ARSENIDE DEPLETION-MODE PROCESSING

In order to utilize the advantageous characteristics of GaAs, a reliable fabrication process must be available. The most mature and reliable GaAs IC manufacturing technology uses the depletion-mode MESFET process, which is suitable for microwave, analog and logic circuits. The lower number of critical mask steps in this process results in fewer lithographic related errors which improves yield and reliability. The

circuits described in Chapter 4 were all fabricated using D-MESFET technology by TriQuint Semiconductor. In describing this process, only a limited description is given which will be representative of depletion-mode fabrication steps.

Processing requires initial GaAs semi-insulating (S.I.) substrate material which is grown by two methods: the Horizontal Bridgman (HB) or the liquid encapsulated Czochralski (LEC) techniques [3.5]. The LEC method has become more popular recently since impurity density is an order of magnitude less in LEC grown wafers as opposed to HB grown wafers. The method of generating wafers by LEC is shown in Figure 3.18 [3.7]. Gallium and Arsenic are melted under a boric oxide (B_2O_3) liquid encapsulating layer in a crucible made of pyrolytic boron nitride (PBN). A GaAs seed is lowered through the B_2O_3 layer into the melt and slowly withdrawn while the seed and crucible are rotated. Characteristics of the GaAs crystal growth are determined from the pull rate and the rotational speeds. Once the ingots are sliced into wafers and polished, device processing can commence.

Figure 3.18 Liquid-Encapsulated Czochralski Growth of GaAs Wafers.

A step by step representation of the fabrication process is illustrated in Figure 3.19 [3.12] and will now be outlined:

- Step 1: Initially, a layer of Si_3N_4 is grown on the semi-insulating substrate to prevent emission of As during a subsequent annealing step. Photoresist is deposited and then exposed to define regions for N^- implantation. The light N^- doping of Si ions is implanted to define active channels, Schottky diodes and implanted resistors on the GaAs wafer.
- Step 2: A second N^+ ion implantation is performed to define transistor source and drain regions, ohmic contacts, Schottky diodes and implanted resistors. Photoresist is removed and a high temperature anneal follows for the activation of the implant species into the GaAs.
- Step 3: The process allows the generation of NiCr resistors for better matching, precision, greater isolation, and lower temperature coefficients of resistance. These thin-film structures are formed by a "lift-off" scheme, which deposits resistor metal (NiCr) and contact metal.
- Step 4: Areas of Si_3N_4 are removed in areas requiring ohmic contact to N^+ implanted regions. A Ni-Au-Ge ohmic metal composition is deposited and alloyed at a high temperature to provide least resistance to implanted drain/source regions.
- Step 5: A similar procedure, as in Step 4, is performed for Schottky barrier gate formation. A Ti-Pt-Au deposition over the channel regions and diodes occurs and is the most critical alignment step for uniform device performance.
- Step 6: The first metal interconnect is defined by this step. First level metal (1ME) is deposited for interconnection between ohmic,

gate and resistor metal by physical overlap. The 1ME metal constitutes the bottom electrode in metal-insulator-metal (MIM) capacitors.

Step 7: Si_3N_4 is deposited as the dielectric for MIM capacitors and areas for interconnect between 1ME and second level, airbridge (AB) metal are defined by dielectric vias.

Step 8: Masking of photoresist defines airbridge Vias to produce the effective capacitive area for MIM capacitors and interconnect to 1ME.

Steps 9 & 10: Second level metal (AB) provides a low capacitance/length interconnect due to the use of air as a dielectric medium. AB metal also forms the top electrode for MIM capacitors. A thin layer of Si_3N_4 is coated over all airbridge tracks to add rigidity to AB metal and effectively passivates the entire circuit.

a)

b)

c)

d)

e)

Figure 3.19 A Typical D-MESFET Process Flow

f)

g)

h)

i)

j)

Figure 3.19 (cont'd). A Typical D-MESFET Process Flow.

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CHAPTER 4

GALLIUM ARSENIDE ANALOG-TO-DIGITAL CONVERTER CIRCUIT DESIGNS

4.1 INTRODUCTION

Having discussed the characteristics of high-speed A/D conversion and the properties of gallium arsenide IC technology in the previous chapters, the designs of certain A/D subcircuits using GaAs circuit elements are now presented. The three designs are a sample-and-hold and two comparators: a capacitive differencing circuit and a differential amplifier configuration. The following sections describe the features of each design and construct a circuit configuration using depletion-mode MESFET technology. All designs are simulated with SPICE using the appropriate element models given in Chapter 3.

4.2 A SAMPLE-AND-HOLD CIRCUIT

The sample-and-hold was configured in the open-loop structure (Section 2.6.1) to facilitate high-speed sampling of signals. The design outline of this circuit is divided into two sections: the sampling switch and the output buffer amplifier.

4.2.1 The Sampling Switch

Regarding the circuit requirements outlined in Section 2.6.1, short acquisition time and sample feedthrough minimization were considered

important performance criteria in this design of the sample-and-hold. Fast acquisition, when sampling, can be provided by a single MESFET [4.1], as shown in Figure 4.1.

Figure 4.1. A D-MESFET Sampling Switch.

The sampling voltage, V_ϕ , is connected to the gate which controls current flow in the channel between the drain and source. For low gate-to-channel voltages, the depletion-mode MESFET allows passage of current between source and drain charging up the hold capacitor, C_h , while gate voltages below pinchoff deplete the channel of carriers and cause the MESFET switch to effectively 'open'. Opening the switch will cause the previous analog input, V_{in} , to appear across C_h . Considering that substantial current flows when the gate of the MESFET is forward biased ($> 0.7V$) and that no current flows with pinchoff, the 'ON' state input voltage range of this structure is:

$$V_{in} + V_p < V_\phi(\text{on}) < V_{in} + 0.7V \quad (4.1)$$

To turn 'OFF' the switch, pinchoff must occur and thus:

$$V_\phi(\text{off}) < V_{in} + V_p \quad (4.2)$$

These constraints limit the input voltage swing to a maximum of $(0.7 - V_p)$ for fixed clocked voltages [4.2].

To determine the speed of acquisition of this sampling structure, switching characteristics of the MESFET must be analyzed. For acquisition

of low amplitude input voltages, the difference voltage between drain and source will be small and the MESFET can be characterized as operating in its linear region. Assuming low channel length modulation, the channel current, i_{ds} , in linear region operation is given by equation (3.9):

$$i_{ds} = W\beta\mu \left[2(v_{gs} - V_p) v_{ds} - \frac{v_{ds}^2}{\mu} \right] \quad (4.3)$$

For small v_{ds} , the squared term can be ignored yielding:

$$i_{ds} = W\beta\mu \left[2(v_{gs} - V_p) v_{ds} \right] \quad (4.4)$$

Hence, the channel resistance of the MESFET becomes:

$$R_{ds} = \frac{1}{g_{ds}} = \frac{1}{\frac{\delta i_{ds}}{\delta v_{ds}}} = \frac{1}{W\beta\mu 2(v_{gs} - V_p)} \quad (4.5)$$

Equation (4.5) gives a resistance value of 31.5 ohms for a 100 μm wide gate ($v_{gs} = 0\text{V}$), with typical TriQuint FET parameters of $\beta = 1.77 \times 10^{-4} \text{ A/V}^2$, $\mu = 0.56$ and $V_p = -1.6\text{V}$. If parasitic source and drain resistances of 9 ohms each are added to this value, the resulting FET resistance agrees with simulations. Figure 4.2 shows the SPICE simulation of the voltage gain through a TriQuint 100 μm D-MESFET switch when loaded by 50 ohms. The resistor divider formula indicates the equivalent resistance to be 49 Ω . The gain decreases slightly with frequency due to the internal capacitances of the MESFET. Results from Equation (4.5) also indicate that as the v_{gs} voltage approaches V_p , the equivalent resistance increases. This characteristic is shown graphically in Figure 4.3 where the resistance of a 100 μm wide MESFET is compared with various v_{gs} values under simulated conditions.

Figure 4.2 Simulation for Determining the Equivalent Resistance of a 100 μ m D-MESFET.

Since the MESFET has a finite resistance in the 'ON' state, it takes a finite amount of time to charge the hold capacitance. An estimation of this acquisition time can be obtained when simplifying assumptions are made [4.3]. For signal acquisition, assuming linear operation of the MESFET and neglecting parasitic resistances initially, the currents in Figure 4.1 can be equated to yield:

$$i_{ds} = i_{out} = C_h \frac{\delta v_{out}}{\delta t} = W\beta\mu [2(v_{gs} - V_p)v_{ds}] \quad (4.6)$$

Substituting $v_{gs} = V_\phi - v_{out}$ and $v_{ds} = v_{in} - v_{out}$ and rearranging:

$$\delta t = \frac{C_h}{2W\beta\mu} \cdot \frac{\delta v_{out}}{v_{out}^2 + (V_p - V_\phi - v_{in})v_{out} + (V_\phi - V_p)v_{in}} \quad (4.7)$$

Figure 4.3 Equivalent Resistance of a 100 μm D-MESFET versus V_{gs}

Integrating both sides and assuming $v_{out}(t)$ at time $0 = 0$, one obtains:

$$t_{CH} = \frac{C_h}{2W\beta\mu (V_\phi - V_p - v_{in})} \ln \left[\frac{v_{in}(v_{out} + V_p - V_\phi)}{(v_{out} - v_{in}) \cdot (V_\phi - V_p)} \right] \quad (4.8)$$

where t_{CH} is the time required to charge the hold capacitor to v_{out} with an input voltage of v_{in} . For small signal settling, the denominator of the first term is similar to equation (4.5) and the entire first term can be approximated by the term $R_{ds}C_h$. If R_{ds} is modified to consider parasitic drain and sources resistances, equation (4.9) agrees well with simulated results. Figure 4.4 shows acquisition of a 100 mV input across a 330 fF hold capacitor to within 0.1% to be 147 pS which coincides with 154 pS from equation (4.8). Although the SPICE simulation is more accurate since it accounts for changing R_{ds}

values with voltage, equation (4.8) may be applied to initially determine acquisition time of the MESFET switch.

Figure 4.4 Acquisition of a 100 mV Input Step by a 100 μ m D-MESFET Switch

A problem with using the D-MESFET as a sampling switch is that excessive capacitive charges are injected into the channel during switching [4.2]. This effect can be illustrated by considering the simplified equivalent circuit representation shown in Figure 4.5. This "clock feedthrough" is due to the capacitive divider effect present both at the input and output of the switch due to the C_{gd} and C_{gs} components of the D-MESFET.

Figure 4.5. A Simplified Equivalent Circuit of the D-MESFET Sampling Switch.

If extremely fast clocking of the switch is assumed, the amount of amplitude induced noise at the output is given by:

$$\delta = \frac{\frac{1}{j\omega C_h}}{\frac{1}{j\omega C_h} + \frac{1}{j\omega C_{gs}}} \cdot \Delta V_\phi = \frac{C_{gs}}{C_{gs} + C_h} \cdot \Delta V_\phi \quad (4.9)$$

where ΔV_ϕ is the voltage swing at the gate. Depending on gate structure, hold capacitance, clock amplitude and risetime, the amount of feedthrough may be significant. In most applications this is intolerable and has warranted design of different structures [4.4]. A scheme, similar to NMOS design, can be used to compensate the feedthrough effect using FET's of the same structure [4.3]. The structure is shown in Figure 4.6 with associated clock signals.

Figure 4.6. Clock Feedthrough Compensation Using MESFETs.

The compensation method utilizes complementary clock signals and a short-circuited FET (equivalently a diode). Since the charge injected at the output due to V_ϕ is $\Delta V_\phi \cdot C_{gs}$, the short-circuited FET, of one-half the sampling MESFET width (since its C_{gs} and C_{gd} elements both contribute in charge transfer), will inject an opposite charge of $-\Delta V_\phi C_{gs}$. Since the scheme has not yet been reported in GaAs literature, the analysis and implementation of the structure would prove beneficial.

SPICE simulations have been performed on the switching characteristics of various D-MESFET switch configurations. The structures of a single MESFET, a 3-gate switch [4.4], and a fully compensated structure, which has short-circuited FETs at the input and output nodes, are shown in Figure 4.7a). The simulations, in Figure 4.7b), show the hold step errors of the various switches for a 1 GHz clocking rate when $V_{in} = 0$. The fully compensated structure is similar to that of Figure 4.6 but includes a charge injecting FET to compensate for feedthrough at the input. It is evident, from Figure 4.7, that the fully compensated switch with a one-quarter sampling width ratio at the input and one-half sampling width ratio at the output provided the best performance.

4.2.2 The Output Buffer Amplifier

With the sampling structure established, a suitable buffer amplifier is necessary to provide adequate isolation and drive to external circuitry. In choosing the appropriate amplifier, frequency response of each structure must be analyzed. The following discussion progresses through the frequency analysis of various dc coupled amplifiers [4.5] and arrives at an appropriate configuration.

Figure 4.7. Switching Characteristics of Various D-MESFET Switch Configurations.

The common-source amplifier is usually utilized as a buffer stage since voltage gain along with reverse isolation is available from the amplifier between the output and input. An active load in this amplifier, rather than a resistive load, decreases on-chip area and results in better large-signal performance for a given small-signal gain. The common-source inverting amplifier with active load is shown in Figure 4.8 along with its

small signal equivalent circuit. The small signal representation ignores the parasitic source, drain and gate resistances. The transfer function from the small signal representation determines the frequency response and is defined by:

$$A_I(s) = A_{vI} \left[\frac{1}{1 + s \frac{C_I}{g_I}} \right] \quad (4.10)$$

where A_{vI} = low frequency inverter gain

$$= \frac{-g_{m1}}{g_I} \quad (4.11)$$

$$g_I = g_{d1} + g_{d2} \quad (4.12)$$

$$C_I = C_{ds1} + C_{gd2} + C_{ds2} + C_{gd1} \left(1 + \left| \frac{1}{A_{vI}} \right| \right) + C_L \quad (4.13)$$

Figure 4.8. Common-Source Inverting Amplifier with Active Load.

From equation (4.10), the amplifier response is first order with a low frequency gain equal to $-g_{m1}/g_I$ and has single pole at g_I/C_I . This amplifying configuration suffers, however, in terms

of bandwidth since typical loads, such as other amplifier stages, significantly reduce the bandwidth. This becomes apparent when the input capacitance of this amplifier, which is comprised of C_{gs1} plus the Miller-effected capacitance $C_{gd1}(1+|A_{vI}|)$, is considered. When this capacitance becomes the load capacitance, C_L , it constitutes most of the pole capacitance, C_I , and greatly affects bandwidth.

Improvement in frequency response is easily achieved by buffering this amplifying stage with a common-drain source follower. The source follower buffer isolates the previous stage from the effects of capacitive loading and does not degrade the small signal gain significantly. The source follower in GaAs D-MESFET form is shown in Figure 4.9 with level shifting diodes to provide appropriate DC level shifting between stages. The frequency response of the source follower, excluding diode resistances, is given by:

$$A_S(s) = A_{vS} \left[\frac{1}{1 + s \frac{C_s}{g_{m3} + g_s}} \right] \quad (4.14)$$

where A_{vS} = low frequency source follower gain

$$= \frac{g_{m3}}{g_{m3} + g_s} \quad (4.15)$$

$$g_s = g_{d3} + g_{d4} \quad (4.16)$$

$$C_s = C_{ds3} + C_{gd4} + C_{ds4} + C_{gs3} \left(1 + \left| \frac{1}{A_{vS}} \right| \right) + C_L \quad (4.17)$$

Figure 4.9. Common-Drain Source Follower Buffer.

Analysis of cascading the inverting stage to the source follower stage has revealed that the overall frequency response improves in bandwidth [4.5]. The effect is that the poles of each circuit are strongly coupled by the gate-to-source capacitance of the source follower. The interaction of these real axis poles forms a complex pole pair and a second order response results. The small signal equivalent circuit of the combined amplifier is shown in Figure 4.10. Analysis of the frequency response produces a transfer function given by:

$$A_{IA}(s) = \frac{A_{VI} \cdot A_{VS} \left[1 + s \frac{C_{g2}}{g_{m3}} \right]}{As^2 + Bs + 1} \quad (4.18)$$

where A_{VI} , A_{VS} are equal to (4.11) and (4.15)

$$A = \frac{C_{g2} \cdot C_I + C_s \cdot C_I + C_s \cdot C_{g2}}{g_I \cdot (g_{m3} + g_s)} \quad (4.19)$$

Figure 4.10. Combined Inverting Amplifier.

$$B = \frac{g_{m3} \cdot C_I + g_s \cdot (C_I + C_{g2}) + g_I \cdot (C_{g2} + C_s)}{g_I \cdot (g_{m3} + g_s)} \quad (4.20)$$

The capacitances, transconductances and conductances associated with each term are defined in Figure 4.10. The response in (4.18) has a zero at $\omega = g_{m3}/C_{g2}$ which is higher than frequencies associated with the poles and thus can be ignored. The pole frequencies, s_1 and s_2 , are described by solving the characteristic equation $As^2 + Bs + 1 = 0$ and therefore have the form:

$$s_1, s_2 = \frac{-B \pm \sqrt{B^2 - 4A}}{2A} \quad (4.21)$$

Further improvement in frequency response is achieved by incorporation of active feedback in the amplifier [4.6]. A feedback FET, of approximately one quarter width of the inverting FET, is placed between the output and inverting stage, as shown in Figure 4.11. The effect of feedback on the poles of the circuit is to expand the pole location in the imaginary direction of the s -plane. This improves bandwidth but at the

expense of voltage gain. The new transfer function due to feedback becomes:

$$A_{FA}(s) = \frac{A_{VF} \cdot A_{VS} \left[1 + s \frac{C_{g2}}{g_{m3}} \right]}{A's^2 + B's + 1} \quad (4.22)$$

$$\text{where } A_{VF} = \frac{-g_{m1}}{g_I + g_{d5} + A_{VS} g_{m5}} \quad (4.23)$$

$$A' = \frac{C_{g2} \cdot C_I + C_s' \cdot C_I + C_s' \cdot C_{g2}}{(g_I + g_{d5})(g_{m3} + g_s) + g_{m3} g_{m5}} \quad (4.24)$$

$$B' = \frac{g_{m3} \cdot C_I + g_s (C_I + C_{g2}) + g_I (C_{g2} + C_s') + C_{g2} g_{m5}}{(g_I + g_{d5})(g_{m3} + g_s) + g_{m3} g_{m5}} \quad (4.25)$$

Figure 4.11. Feedback Inverting Amplifier.

Figures 4.12 and 4.13 provide a comparison of the DC bias characteristics and frequency response of the three amplifier configurations in Figures 4.8, 4.10, 4.11 with identical device widths and loads. Improvement in frequency response bandwidth is clearly evident in Figure 4.13. Implementation of the feedback buffer amplifier was decided for the sample-and-hold and final circuit structure of the sample-and-hold is shown in Figure 4.14.

Figure 4.12. SPICE Comparisons of DC Bias Characteristics for DC Coupled Amplifiers.

Figure 4.13. SPICE Comparisons of Frequency Response for DC Coupled Amplifiers.

2

OF/DE

2

METRO

Figure 4.14. Final Schematic of the Sample-and-Hold.

4.2.3 Device Widths in the Sample-and-Hold

The determination of the device widths in Figure 4.14 was performed with the following considerations:

- a) The DC bias point of the amplifier was established at 0V to facilitate sampling of signals centred at ground. The ratio of $(W_1 + W_3)/W_2$ is approximately 1 in this case;
- b) Internal capacitances of the amplifier were kept as small as possible. Therefore, values for $W_1 = 25 \mu\text{m}$, $W_2 = 30 \mu\text{m}$ and $W_3 = 5 \mu\text{m}$ were chosen;
- c) Source follower widths were comparable to inverting stage widths:
 $W_3, W_4 = 25 \mu\text{m}$;
- d) The sampling FET width of $100 \mu\text{m}$ was maintained to keep the equivalent resistance of the sampling switch low;
- e) Simulation results indicated that to minimize clock feedthrough,
 $W_{S1} = 50 \mu\text{m}$ and $W_{S2} = 25 \mu\text{m}$;
- f) An on-chip capacitor of $C_h = 330 \text{ fF}$ was implemented to improve clock feedthrough effects.

The summary of component values is given in Table 4.1.

<u>Device</u>	<u>Device Width (μm)</u>
W_S	100
W_{S1}	50
W_{S2}	25
W_1	25
W_2	30
W_3	25
W_4	25
W_5	5
D_{LS}	25

Table 4.1 Summary of Component Values for the Sample-and-Hold.

Of final note, the amplifier must be interfaced to a 50Ω test environment. To provide this interface, a $200 \mu\text{m}$ width D-MESFET is implemented in a source follower mode with its drain tied to V_{DD} . The configuration provides a 1 volt swing into 50 ohms from a 2 volt input drive. A constant -6.6 dB drop up to 10 GHz was observed in simulations.

4.3 A CAPACITIVE DIFFERENCING COMPARATOR

Circuits designed with depletion-mode GaAs devices suffer many difficulties which are similar to those experienced by silicon MOS designs. A major drawback in both of the technologies involves the large device parameter fluctuations which occur in IC processing. For example, threshold voltages for transistors differ from wafer to wafer and among devices on the same substrate which directly relates to limiting accuracy. When designing comparators on GaAs with high input sensitivity, circuit techniques used in silicon MOS design which compensate for effects caused by processing inconsistencies should be considered.

A high sensitivity comparator using n-channel MOSFETs has been reported and detects voltage differences in the 1 mV range [4.7]. The block representation of the scheme is shown in Figure 4.15. In terms of operation, the comparator initially generates the signal, ΔV_i , which can be either the difference in magnitude or algebraic difference of the input voltages V_{in} and V_{ref} , depending on the input differencing scheme used. The signal, ΔV_i , is generated using various clock signals and capacitors, which are not affected by process fluctuations as transistors are. This difference voltage is then applied to a high gain stage which is externally biased or self-biased into its high gain region. The overall desired effect is to cause the difference in input voltage to translate into a change in the bias point at the input of the high gain amplifier. The output of the high-gain amplifier provides the amplified difference of input signals to the latch input which is clocked at the appropriate time for storage. The advantage of this scheme is that the comparative difference in the input voltages is obtained with extremely low

device mismatch. The similarity of nMOS design and depletion-mode GaAs MESFET design justifies the implementation of this configuration on GaAs to observe if input sensitivity for comparators will improve.

Figure 4.15. A High Sensitivity Comparator Structure.

4.3.1 The Capacitive Differencing Input Stage

The capacitive differencing input block in Figure 4.15 was designed using D-MESFETs as switches in an algebraic differencing configuration [4.7] and is shown in Figure 4.16. Two complementary clock signals, ϕ_1 and ϕ_2 , along with the D-MESFET devices, provide switching of the input voltages to be compared. During ϕ_1 , node A is charged to the value of V_{ref} while node B is externally biased in the high-gain region of the gain stage. When ϕ_1 is released, ϕ_2 is applied and the input voltage, V_{in} , appears at node A. In switching, the voltage drop across the capacitor, C_c , must be maintained and thus the voltage potential at node B changes by an amount approximate to the change in potential at node A. If ideal clocking is assumed, the change in voltage at node B is defined by the equation:

$$\Delta V_B = \frac{V_{in} - V_{ref}}{1 + \frac{C_{str}}{C_c}} \quad (4.30)$$

where $(V_{in} - V_{ref})$ is the input voltage difference, C_c is the differencing capacitor and C_{str} is the stray capacitance at node B. The stray capacitance, C_{str} , is comprised of the input capacitance of the amplifying stage and the gate-to-source capacitance of the biasing MESFET. Equation 4.30 illustrates that a capacitor divider effect exists at node B and indicates that C_c must be made large enough not to degrade the voltage difference transferred from node A.

Figure 4.16. The Capacitive Differencing Input Block Using Algebraic Differencing.

SPICE simulations were performed to analyze the performance of the input differencing scheme. Figure 4.17 shows operation of the input stage using a 1 GHz square wave with 10 pS rise/fall times for clocking and a difference in input voltages of 100mV. MESFET widths were 100 μm to keep the equivalent 'on' resistance of the switches small (~ 50 ohms).

Values for capacitances and voltages in the simulation were: $C_L = 40$ fF, $C_C = 30$ pF and $V_{bias} = 0V$. The large voltage spikes at clock transition points were caused by clock feedthrough of the biasing MESFET since the feedthrough from the input sampling devices is collectively cancelled by symmetrical clocking using complementary signals. The spikes are irrelevant to overall performance since voltage levels are only of interest. The simulation indicates a percentage error in the transformation of the input difference to node B of 1.1% when $C_C = 30$ pF and $C_L = 40$ fF. The total stray capacitance is 89 fF in this case. With $C_C = 30$ pF and $C_{str} = 89$ fF, the error given by equation 4.30, which assumes ideal clocking, is 0.3% which agrees reasonably well with simulation. The effect of decreasing C_C is illustrated in Figure 4.18 and indicates that the percentage error in ΔV_{in} transferred increases but the clock coupling decreases as is expected. The rise/fall times of the voltages at nodes A and B when $V_{bias} = -0.5V$ are shown in Figures 4.19 and 4.20. The risetimes from 10-90% agree with first order approximation of $t_{10-90} = 2.2 RC$ where R is the equivalent 'on' resistance of the MESFET switch and C is the capacitance at the node. The rise and fall times were 31 pS and 17 pS respectively.

Figure 4.17. Input Stage Voltages at Nodes A & B at 1 GHz Operation.

Figure 4.18. Effect of Decreasing C_c .

Figure 4.19. Rise Times at Nodes A & B.

Figure 4.20. Fall Times at Nodes A & B.

4.3.2 The High Gain Amplifier

To implement the high gain amplifier stage, a modification to the simple inverting gain stage in Figure 4.8 can be performed. Usually, the maximum gain available from this single stage inverting amplifier is approximately 20 dB. By implementing a self-bootstrapped technique [4.8] to the individual D-MESFET devices at the input and load of the amplifying stage, as shown in Figure 4.21, the small signal gain of the amplifier can be improved. Self-bootstrapping involves connecting MESFETs of different widths in series and tying together the gates of these two devices. The technique maintains the current characteristics of the smaller MESFET and utilizes the larger device to increase the output impedance of the entire structure. By self-bootstrapping, the output impedance of a single FET can be increased to a value of $g_{m2}r_{d1}r_{d2}$ [4.1]. The increase in output impedance will lower the g_I term in equation 4.11 and thus improve gain. The frequency response of the high gain stage, compared to the stage in Figure 4.8, is defined as:

$$A_{HI}(s) = A_{VHI} \left[\frac{1}{1 + \frac{C_I}{s g_I}} \right] \quad (4.31)$$

A_{VHI} = low frequency self-bootstrapped inverter gain

$$= \frac{\frac{-g_{m1}}{\frac{g_{d3} g_{d4}}{g_{m4}} + \frac{g_{d2} g_{d1}}{g_{m2}}}}{g_I} = \frac{-g_{m1}}{g_I} \quad (4.32)$$

$$C_I = C_{gd4} + C_{gd2} \left(1 + \left| \frac{1}{A_{VHI}} \right| \right) + C_L \quad (4.33)$$

Figure 4.21. The Self-Bootstrapped Inverting Amplifier.

Figure 4.21 illustrates the configuration of the new high-gain amplifier and Figures 4.22 and 4.23 compare the DC characteristics and the frequency response of the self-bootstrapped amplifier to the inverting amplifier configuration given in Figure 4.10. An improvement of 20 dB in gain for the high gain amplifier is achieved up to 6 MHz where gain begins to decrease. The 3 dB bandwidth is significantly smaller in the high-gain structure due to the decrease in g_I as evident in equation (4.32). Since the gain was still comparable to the simple inverter above 200 MHz, implementation of the high gain amplifier was carried through.

Figure 4.22. Comparison of DC Characteristics of Self-Bootstrapped and Simple Inverting Amplifiers.

Figure 4.23. Comparison of Frequency Response of Self-Bootstrapped and Simple Inverting Amplifiers.

4.3.3 The Output Latch

As previously mentioned, a latch circuit is required to capture and store the amplified version of ΔV_i . A simple latch structure was implemented using digital logic cells provided by TriQuint [4.9] and its block configuration is shown in Figure 4.24. The latch is essentially a clocked D flip-flop where an output reset/set (RS) NOR latch provides complementary Q and Q-bar output signals. The entire circuit was easily implemented using TriQuint cells since single and dual gates allow AND-NOR structures to be created. The inverter and AND-NOR cells used, along with device widths, are shown in Figure 4.25.

Figure 4.24. A Simple D Flip-Flop Latch Structure.

Figure 4.25. TriQuint Cells Used in the Latch Structure.

Operation of the latch is simple. An input is applied at the D node and, with the aid of an inverter, this signal is provided to the RS latch in complementary form. Once propagation through the RS structure occurs, the clock signal ϕ_c is activated and the state defined by the input is stored. The latch provides some additional gain from input to output but it has a drawback that symmetrical switching of outputs does not occur in response to input voltages.

SPICE simulations of this latch structure are shown in Figure 4.26 and Figure 4.27. The DC characteristics in Figure 4.26 show the non-symmetrical switching thresholds of the latch. The input switching threshold for the Q -bar output is $-0.45V$ and the Q output is $-0.34V$. The gains at these thresholds also differ, as shown in Figure 4.26. The simulation shown in Figure 4.27 illustrates the propagation delay times through the latch at which storage of the latch state can be maintained by the ϕ_c signal. To store a high input requires 390 pS while storage of a low input occurs after 410 pS.

Figure 4.26. DC Characteristics of the Latch.

Figure 4.27. Propagation Delays Through the Latch.

The final circuit schematic for the capacitive differencing comparator is shown in Figure 4.28 with the device widths tabulated in Table 4.2. The sampling switches were 100 μm to minimize their effective 'on' resistances. Values for the amplifier were obtained by simulation to maximize gain but minimize input capacitance, while the value for C_C was determined for appropriate voltage transfer from node A to node B. The transistor widths for the latch were equivalent to the values given in Figure 4.25.

<u>Device</u>	<u>Device Value</u>
W _{S1}	100 μm
W _{S2}	100 μm
W _{S3}	100 μm
C _C	30 pF
W ₁	10 μm
W ₂	50 μm
W ₃	5 μm
W ₄	25 μm
W ₅	40 μm
D _{LS}	40 μm
W ₆	40 μm

Table 4.2 Summary of Component Values for the Capacitive Differencing Comparator.

Figure 4.28. Final Schematic of the Capacitive Differencing Comparator.

4.4 A DIFFERENTIAL AMPLIFIER COMPARATOR

The popularity of differential amplifiers as comparators in GaAs A/D converters is evident from the emphasis which has been placed on their design [4.10-4.11]. However, previous results have indicated that high gain and process insensitive designs are difficult to achieve. Recently, a differential amplifier which compensates for process variations using feedback for stability has been reported [4.12]. The differential amplifier presented here utilizes this structure but incorporates additional features to improve gain. This differential amplifier comparator, implemented with only D-MESFET devices, is shown in Figure 4.29. The amplifier consists of two input structures, with source terminals common, two active loads connected to the drains of the input FETs and a current source, which is gate biased via a level shifting network from one of the differential outputs. This level shifting network uses an additional diode to provide the required dc bias to the current source. The input devices steer portions of the available current from the current source, I_{SS} , through the two branches depending on the input voltage difference. In the design of this differential amplifier, the response to common and differential input voltage was analyzed to determine device widths.

4.4.1 Common Mode Half Circuit Analysis

To determine the input voltage operating range of the differential amplifier, its common-mode half circuit, shown in Figure 4.30, was be considered. The circuit allowed analysis of currents and voltages in the structure, when the input voltages are equal. This analysis determines the input range at which all transistors are operating in saturation which is the desired mode of operation for the differential amplifier. The current source

Figure 4.29. The Feedback Differential Amplifier.

Figure 4.30. The Common Mode Half Circuit of the Differential Amplifier.

must be in saturation to resemble a constant current source while the load and input structure allow maximum output differencing when operating in their saturated state.

In the transformation from Figure 4.29 to Figure 4.30, it can be noted that the input and load structures have doubled in width. This is required since the current entering the drain of the current source consists of equal contributions by both branches and thus can be represented by a single branch having devices double their width. This transformation differs from conventional analysis which halves the current source [4.13] because feedback is incorporated in biasing the current source and this feedback is not independent of the branches.

The specific input voltage, where all transistors will be in saturation is found by equating currents through the input and load and assuming the load enters saturation when $V_{ds} = V_{DD} + \mu V_p$. The input voltage at which all transistors begin operation in saturation can be determined as:

$$V_{in} = V_s' + V_p (1-K) \quad (4.34)$$

$$\text{where } K = \left[\frac{W_L (1 - \lambda \mu V_p)}{W_I (1 + \lambda (V_{DD} - V_s' + \mu V_p))} \right]^{\frac{1}{2}} \quad (4.35)$$

$$V_s' = V_{DD} - 5 V_{LS} \quad (4.36)$$

V_{LS} = voltage drop across a diode

During operation in saturation, the voltage at the source of the input device exhibits linear response. The voltages at node S can be obtained as above and is approximately given by:

$$V_s = V_{in} - V_p (1-K) \quad (4.37)$$

Analysis also illustrates that the range of saturation operation is limited. This results from the input device becoming forward biased at high input voltages and by the load and current source devices operating in their linear region for low inputs. It should be noted that to obtain the above behaviour, proper ratioing of load and current source devices is required. A ratio of 1 to 2 is necessary between the load and current source device to establish that all devices will operate in saturation. The width of the input device influences gain and differential response which is now considered.

4.4.2 Differential Mode Analysis

Differential mode analysis determines the dependence of the branch current on the differential input voltage and the analysis presented here addresses both large-signal low frequency response and small-signal behaviour. In both cases, simplifying assumptions were made to achieve analytical expressions for response and then simulations were performed to more accurately model the differential behaviour.

For large signal response, it was assumed that the load transistors are matched and that the output resistances of the input MESFET's and current sources are infinite. Voltages around the source loop in Figure 4.28 yield:

$$V_{i1} - V_{i2} = V_{gs1} - V_{gs2} \quad (4.38)$$

Assuming square law behaviour of the MESFET operating in its saturation region:

$$I_{di} = I_{DSS} \left(\frac{V_{gsi}}{V_p} - 1 \right)^2 \quad (4.39)$$

or

$$v_{gsi} = v_p \left[1 + \left(\frac{I_{di}}{I_{DSS}} \right)^{\frac{1}{2}} \right] \quad (4.40)$$

and substituting the above into (4.38) results in the following:

$$v_{id} = v_{i1} - v_{i2} = v_p \left[\left(\frac{I_{d1}}{I_{DSS}} \right)^{\frac{1}{2}} - \left(\frac{I_{d2}}{I_{DSS}} \right)^{\frac{1}{2}} \right] \quad (4.41)$$

where v_{id} is the differential input voltage. Noting the relation:

$$I_{d1} + I_{d2} = I_{SS} \quad (4.42)$$

and combining (4.41) into (4.42) provides the desired relationship between I_{d1} and v_{id} . Solving the quadratic for I_{d1} and substituting back into (4.42) gives:

$$I_{d1} = \frac{I_{SS}}{2} \left(1 + \frac{v_{id}}{v_p} \left[2 \frac{I_{DSS}}{I_{SS}} - \left(\frac{I_{DSS}}{I_{SS}} \right)^2 \left(\frac{v_{id}}{v_p} \right)^2 \right]^{\frac{1}{2}} \right) \quad (4.43)$$

$$I_{d2} = \frac{I_{SS}}{2} \left(1 - \frac{v_{id}}{v_p} \left[2 \frac{I_{DSS}}{I_{SS}} - \left(\frac{I_{DSS}}{I_{SS}} \right)^2 \left(\frac{v_{id}}{v_p} \right)^2 \right]^{\frac{1}{2}} \right) \quad (4.44)$$

Equations (4.43) and (4.44) provide an analytical expression for the branch currents in response to the differential input voltage and show that the incremental change in I_d is given by the second term in the above expressions.

The differential output voltage can now easily be obtained since:

$$v_{od} = v_{o1} - v_{o2} = \frac{I_{d2}}{g_1} - \frac{I_{d1}}{g_1} \quad (4.45)$$

Substituting (4.43) and (4.44) in (4.45) gives:

$$v_{od} = - \frac{I_{SS}}{g_1} \left(\frac{v_{id}}{v_p} \left[2 \left(\frac{I_{DSS}}{I_{SS}} \right) - \left(\frac{I_{DSS}}{I_{SS}} \right)^2 \left(\frac{v_{id}}{v_p} \right)^2 \right]^{\frac{1}{2}} \right) \quad (4.46)$$

Equations (4.43) to (4.46) characterize the differential behaviour, with simplifying assumptions, of the circuit in Figure 4.29 and provide an

approximate relationship on how the input to load ratio $\frac{I_{DSS}}{I_{SS}}$ will affect

differential performance. However, small signal analysis to determine gain response should also be considered prior to determining device widths.

To determine the gain characteristics of the differential amplifier, small signal analysis which is commonly used in differential pair response was adopted. Two parameters of importance are the differential mode gain, A_{dm} , and the common mode gain, A_{cm} . Using the small signal equivalent circuit for the differential amplifier, shown in Figure 4.31, analysis reveals that the differential gain of this configuration is given by:

$$A_{dm} = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = \frac{-g_m}{g_1 + g_d} \quad (4.47)$$

and the common mode gain is:

$$A_{cm} = \frac{v_{o1} + v_{o2}}{v_{i1} + v_{i2}} = \frac{-g_m g_s}{g_1 (2g_m + 2g_d + g_s) + g_d g_s} \quad (4.48)$$

The above parameters allow the determination of gain at a single-ended output from a single sourced input. The single-ended output gain is defined as:

$$A_{SE} = \frac{v_o}{v_i} = \frac{-A_{dm} + A_{cm}}{2} \quad (4.49)$$

Figure 4.31. Small Signal Equivalent Circuit of the Differential Amplifier.

Using the expressions above and verifying response with SPICE simulations, the ratio of load to input to current source device was determined to be 1:5:2. Increasing the input device width improves gain but results in a higher capacitance at the inputs which reduces bandwidth. However, in the same manner as the inverting amplifier could be improved in terms of gain by applying self-bootstrapped structures, the differential gain, A_{dm} , was improved by applying self-bootstrapped input and load devices. Thus, the resulting differential amplifier in Figure 4.29 was obtained.

SPICE simulations for common-mode, differential mode response and frequency response (for $V_{IP} = -0.75V$) were performed and are shown in Figures 4.32 to 4.34. The final device widths which were implemented in the differential amplifier structure are shown in Table 4.3.

<u>Device</u>	<u>Device Width (μm)</u>
W_{I1}	10
W_{I2}	50
W_{I3}	10
W_{I4}	50
W_{L1}	5
W_{L2}	25
W_{L3}	5
W_{L4}	25
W_{CS}	10
D_{LS}	10
W_1-W_4	40
D_1-D_2	40

Table 4.3 Summary of Component Values for the Differential Amplifier Comparator.

Figure 4.32. SPICE Simulation of the Common-mode Response for the Differential Amplifier.

Figure 4.33. SPICE Simulation of the Differential Mode, Response for the Differential Amplifier ($V_{IP} = -0.75V$)

Figure 4.34. SPICE Simulation of the Frequency Response for the Differential Amplifier ($V_{IP} = -0.75V$)

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CHAPTER 5

EXPERIMENTAL RESULTS

5.1 INTRODUCTION

The evaluation of gallium arsenide circuits operating at clocking rates exceeding 1 GHz is a challenging task. Fast transition, time-domain measurements experience problems related to interconnection to a 50 ohm test system, proper transmission line termination, transmission line coupling and power supply noise suppression, to name a few. This chapter presents the circuit performance of the designs described in Chapter 4, compares measurement with theory and discusses the limitations of the testing used for circuit evaluation.

5.2 CIRCUIT PREPARATION AND TEST EQUIPMENT

5.2.1 Test Fixture

After completion of the depletion-mode fabrication, the GaAs wafers are sliced into dies with dimensions of approximately 2 mm by 2 mm. The T47C2 die arrangement containing the various circuits designed in Chapter 4 is shown in Figure 5.1. To analyze these developed circuits, a test fixture or jig was designed to facilitate measurement of parameters in a 50 ohm, RF environment. The structure, which is shown in Figure 5.2, was designed with the use of the facilities at the Communications Research

Figure 5.1. The T47C2 Die Arrangement of Circuits.

Figure 5.2. The CRC Test Fixture Used for Circuit Evaluation.

Centre and provides the necessary interconnection of the bond pads on the die to the SMA cable connectors for measurement.

The test fixture is comprised of a brass enclosure which allows mounting of a 'RT Duroid' conductive plate which is 2 inches square in dimensions and has a polytetrafluoroethylene (PTFE) dielectric thickness of 5 mils. Microstrip transmission lines, 16 mils wide to ensure $Z_0 = 50$ ohms, and power supply lines are etched by photomasking the 1 oz copper side of the duroid. The transmission lines are equally spaced to avoid cross-coupling, equal in length for simultaneous delays and extend to the duroid boundary where SMA 'Radial' connectors make the 50 Ω transition from microstrip to SMA. Eight RF lines allow testing of multiple input/output structures. A square ground region appears at the centre of the etched conducting surface where the chip is mounted. This ground region is extended in various directions to allow termination of the transmission lines with 50 ohm chip resistors, as close as possible to the die, and to provide areas for decoupling of bias supply lines by chip capacitors. The electrical connection of the ground region to the bottom ground plane is obtained by milling out the central ground and dielectric regions on the conductive surface to die dimensions and mounting the chip with enough conductive silver epoxy to overflow onto the upper ground area. Once the resistors, capacitors and chip were mounted, in that order, the bond pads were connected to the transmission and power supply lines by thermocompression bonding with 0.7 mil gold wire.

Figure 5.3. A Typical Circuit Evaluation Test Set-Up.

5.2.2 Test Equipment

The test apparatus used for circuit evaluation is given in Table 5.1. Low frequency tests, up to 20 MHz, were performed with the function generator while high frequency measurements were obtained by the signal generators in conjunction with the pulse generators. Sampling oscilloscopes displayed the time domain behaviour of the circuits. Small-signal frequency performance was observed using the HP8505A network analyzer system. A typical test configuration is shown in Figure 5.3.

Function and Signal Generators

HP 3314A DC-20 MHz Function Generator
 HP 8656A 0.1-990 MHz Signal Generator
 Colby Instruments SG8000A Signal Generator

Pulse Generators

Colby Instruments PG 5000A Pulse Generator
 Colby Instruments CD 2A11 Clock Drivers

Network Analyzer

HP 8505A Network Analyzer 500 KHz - 1.3 GHz
 - Source/Converter
 - Frequency Control
 - Signal Processor
 HP 8501A Storage - Normalizer
 HP 8502A Transmission/Reflection Test Set

Power Supplies

Kikusui Model PWC 0620
 Kikusui Model PAB 18
 Anatek Model 50-10

Measurement

HP 3466A Digital Multimeter
 Tektronix 7704 Oscilloscope
 - 7S11 Sampling units
 - 7T11 Sampling sweep unit (10 ps resolution/div.)
 SMA RG174/U Cables

Table 5.1 List of Test Apparatus for Circuit Evaluation.

5.3 SAMPLE-AND-HOLD PERFORMANCE

The sample-and-hold circuit designed in Chapter 4 is shown in fabricated form in Figure 5.4. The photograph of the circuit indicates that the sample-and-hold consumes approximately 0.144 mm² of active area. In order to allow the output buffer to be individually tested without being affected by the sampling switch, an additional bond pad with an extended airbridge line was implemented at the input of the buffer, as indicated in the top right area of Figure 5.4. In terms of performance, the

Figure 5.4. Photomicrograph of the Sample-and-Hold Circuit.

sample-and-hold was characterized by analyzing operation during four states: sample, sample-to-hold transition, hold and hold-to-sample transition. Performance parameters within each of these states were measured and are now outlined.

5.3.1 Sample Operation

In the sample mode, the sampling switch was placed in the 'ON' state, since the gate-to-channel voltage was set equal to 0V, and the circuit operated simply as an input follower. Large signal characteristics were measured with the circuit in this state at various frequencies, as shown in Figure 5.5. Large signal response specifies the linear input voltage range of operation for various frequency conditions. Figure 5.5 a) illustrates that the DC response of this circuit, when a 100 Hz ramp input from -1V to +1V is applied, is inverting with gain centred at approximately 0 Volts. Parts b) and c) of the figure indicate the large signal behaviour at 100 MHz and 1 GHz and that the inverting behaviour remains undistorted at 100 MHz but not at 1 GHz. By decreasing the amplitude of the input sine wave at 1 GHz and noting when distortion is eliminated, a 540 mV input range at 1 GHz was possible. These results were obtained with a signal generator and sampling oscilloscope.

To observe small signal behaviour, the network analyzer with a frequency range of 500 KHz to 1.3 GHz was used. Figure 5.6 illustrates that small signal gain of 2 dB was measured for the circuit in the input follower state with a 3 dB frequency of 1.1 GHz. The bias conditions for the sample-and-hold corresponded to a small signal input centered around $V_{in} = 0$ volts.

Figure 5.5. Large Signal Response of the Sample-and-Hold at Various Frequencies in the Sample Mode.

Figure 5.6. Small Signal Frequency Response of the Sample-and-Hold in the Sample Mode.

Figure 5.7. Hold Step Error Resulting from the Sample-to-Hold Transition in the a) Uncompensated mode, b) Compensated Mode.

5.3.2 Sample-to-Hold Transition

The accuracy of sampling is limited by the sample-to-hold transition since error due to charge injection by the switch will directly affect the held voltage. Coupling of the clock signal at the switch was measured with and without the charge injection scheme described in the latter part of section 4.2.1. The $\overline{V_\phi}$ signal, used for the charge injection MESFET's in the switch, was simply connected to -2 volts in the uncompensated mode. The clocking voltages, V_ϕ and $\overline{V_\phi}$, were generated by the Colby PG5000A clock generator and exhibited a 200 ps rise and fall time for switching from 0 to -2 volts. The sample time and hold time were kept symmetrical in these measurements.

Figure 5.7 illustrates the hold step error produced at the output of the sample-and-hold switch during clocking when a DC input voltage of $V_{in} = 0$ volt was applied. The uncompensated switch produced a 250 mV hold step error while a 38 mV hold step error was obtained by the switch in the compensating mode. An improvement of 16.4 dB was shown by using charge injection in the sampling switch.

5.3.3 Hold Operation

In the hold mode, the sampling gate structure was effectively 'OFF' to isolate the held voltage from changes in the input voltage, V_{in} . Hold mode feedthrough attenuation is a measure of the isolation provided by the switch between the hold capacitor node and the input during the 'OFF' state. A feedthrough isolation of -32 dB was measured using the network analyzer as shown in Figure 5.8.

Figure 5.8. Hold Mode Feedthrough Isolation of the Sample-and-Hold.

Figure 5.9. Sample-and-Hold Acquisition of a 100 mV Step with a 200 pS Rise Time.

5.3.4 Hold-to-Sample Transition

The time duration to acquire the input voltage is defined by the hold-to-sample transition. This duration can be separated into the acquisition time and settling time in open follower configurations. The acquisition time is defined as the period which an input must be applied for sampling to a desired accuracy and essentially involves charging of the hold capacitor. Settling time includes the additional time required for the output of the amplifier to settle within a certain accuracy. The acquisition time and settling times for the sample-and-hold, shown in Figure 5.9, were 600 ps and 8 ns respectively.

In summary, the performance characteristics compared to post layout simulations are shown in Table 5.2. An overall comparison between compensating and non compensating operation for the sample-and-hold is illustrated in Figure 5.10.

<u>Parameter</u>	<u>Experimental</u>	<u>Simulated</u>	<u>Units</u>
Linear Input Voltage Range	540	600	mV
Small Signal Response			
Gain	2	5.6	dB
3 dB Frequency	1.1	1.3	GHz
Hold Step Error			
Uncompensated	250	340	mV
Compensated	38	44	mV
Hold Mode Feedthrough	-32	-30	dB
Acquisition Time	600	400	ps
Settling Time	8	1	ns
Power Dissipation	86	80	mW

Table 5.2 Sample-and-Hold Characteristics.

Scales
Vertical: 200mV/div
Horizontal: 10nS/div

a)

Scales
Vertical: 200mV/div
Horizontal: 10nS/div

b)

Figure 5.10. Comparison of Sampling a 10 MHz Sine Wave at 100 MSamples/sec in a) uncompensated mode operation b) compensated mode operation.

5.4 CAPACITIVE DIFFERENCING COMPARATOR PERFORMANCE

The capacitive differencing comparator from the T47C2 series of circuits was tested and found fully operational within the limits of the process. From the chip layout photo, shown in Figure 5.11, the circuit occupied an approximate area of 0.28 mm^2 . An additional bond pad was used in the layout to divide areas of this circuit, as in the sample-and-hold, and provided the means to check functionality of the high gain amplifier and latch separately. Once the characteristics of this section were determined, the input differencing block was included into the evaluation to determine entire circuit functionality.

5.4.1 High Gain Amplifier and Latch Characteristics

Using the additional bond pad, the switching characteristics of the high gain amplifier coupled to the latch were measured. The low frequency switching thresholds at the latch outputs are shown in Figure 5.12. With a 1 kHz ramp at the input, the figure illustrates the non-symmetrical output switching behaviour of the latch described in section 4.3.3. By utilizing a low amplitude square wave with adjustable offset, the switching thresholds at the high gain amplifier input were -0.48V for the Q output and -0.47V for the Q-bar output at 1 kHz.

Using the low amplitude square wave technique, the switching thresholds and sensitivity of this section versus frequency were determined. The sensitivity was defined as half the minimum peak-to-peak amplitude of the square wave required to produce stable latch outputs. Oscilloscope traces illustrating measured sensitivity at 1 GHz are shown in Figure 5.13. The overall results versus frequency are tabulated in Table 5.3 and are compared with theoretical simulations.

Figure 5.11. Photomicrograph of the Capacitive Differencing Comparator.

Figure 5.12. Low Frequency Input Switching Thresholds for the High Gain Amplifier and Latch.

Figure 5.13. High Gain Amplifier and Latch Sensitivities at 1 GHz.

Q Output

<u>Frequency</u> (MHz)	<u>Switching Threshold</u>		<u>Sensitivity</u>	
	Exp. (V)	Theory (V)	Exp. (mV)	Theory (mV)
1	-0.48	-0.497	5	0.40
2	-0.48	-0.497	5	0.40
5	-0.48	-0.497	5	0.40
10	-0.48	-0.497	6	0.40
20	-0.48	-0.497	7	0.54
50	-0.48	-0.497	8	1.09
100	-0.48	-0.497	8	2.13
200	-0.48	-0.497	12	4.50
500	-0.48	-0.497	30	15.8
1000	-0.48	-0.497	60	56.0

Q̄ Output

<u>Frequency</u> (MHz)	<u>Switching Threshold</u>		<u>Sensitivity</u>	
	Exp. (V)	Theory (V)	Exp. (mV)	Theory (mV)
1	-0.47	-0.496	6	0.88
2	-0.47	-0.496	6	0.88
5	-0.47	-0.496	6	0.88
10	-0.47	-0.496	6	0.88
20	-0.47	-0.496	7	1.17
50	-0.47	-0.496	7	2.39
100	-0.47	-0.496	8	4.77
200	-0.47	-0.496	9	10.8
500	-0.47	-0.496	50	45
1000	-0.48	-0.496	200	171

Table 5.3 Measured Sensitivity of the High Gain Amplifier and Latch Versus Frequency.

5.4.2 Input Clocking and Overall Operation

Having established the sensitivity of the high gain amplifier and latch, operation of the input differencing scheme was verified. Using clocking signals established by the Colby CA2A11 clock drivers which switch from 0V to -2V, the appropriate gates were driven to collectively translate the input difference to a change in bias point at the high gain amplifier input. To achieve proper operation, the clock signal, ϕ_4 , was delayed using a variable delay line to allow propagation of the voltage difference to reach the latch and define the proper state for storage. Figure 5.14 shows that the delay required by ϕ_4 , after ϕ_2 is activated, for proper latch storage was approximately 700 pS which can be compared to 640 pS achieved from simulation. These values differ from those given in Section 4.3.3 since these incorporate the time required for the input difference to propagate through the high gain amplifier as well.

The overall circuit functionality is observed in Figure 5.15. In the figure, a 10 MHz square wave with variable amplitude centred about 0 volts was compared to a reference voltage of 0 volts. With a clocking scheme operating at 500 MHz, the amplitude of the input square wave was lowered until the outputs would no longer latch. Figure 5.15 shows that for 500 MHz clocking, ± 150 mV provided stable latch outputs but at ± 60 mV, the Q-bar output became unstable which was expected from Table 5.3.

Figure 5.14. Clocking signals at 300 MHz for the Capacitive Differencing Comparator.

Figure 5.15. Input Voltage Sensing for 500 MHz Clock Operation of the Capacitive Differencing Comparator.

5.5 DIFFERENTIAL AMPLIFIER PERFORMANCE

The circuit performance of the differential amplifier was determined using various methods to characterize common mode and differential mode operation. Initial tests indicated that output response was not as expected and closer examination of the circuit layout revealed that an error had occurred resulting in via posts being omitted during fabrication at the gate of the 200 μm output driver MESFETs. The error was not serious in terms of overall operation but effectively caused the output current available to drive the 50 ohm load to be reduced by one-half. The photograph of the fabricated differential amplifier is shown in Figure 5.16 where the active area consumed was approximately 0.16 mm². Initially, testing of common mode response of the circuit was performed to determine input operating range, then the differential mode behaviour was characterized.

5.5.1 Common-Mode Operation

To determine an initial indication of the common mode input voltage range, a low frequency, large signal common-mode input voltage sweep was performed. With both inputs common, a 1 kHz ramp from -2.5V to +1.5V was applied which resulted in the output responses for the feedback output, V_{OF} , and the normal output, V_{OUT} , as shown in Figure 5.17. The output behaviour indicated that for voltages less than -1.92V both outputs were logically high implying that the current source is still in its linear region of operation. At -1.92V at the input, the current source enters saturation whereby constant current to the differential branches is provided which is the lower limit of the common mode range. Figure 5.17

Figure 5.16. Photomicrograph of the Differential Amplifier.

indicates that the V_{OUT} output does not drop abruptly to an expected equilibrium of 100 mV as was expected from simulation. These preliminary results indicate that a lower than expected gain was achieved by the structure. The final property which can be obtained from Figure 5.17 is that the input transistor becomes forward biased at an input voltage of approximately 1.5 Volts. This however is not the upper limit of the common mode range which is the onset of linear operation by the input device. This limit was determined by analysis of the differential mode behaviour.

Figure 5.17. Common Mode Voltage Behaviour for the Differential Amplifier.

5.5.2 Differential Mode Operation

Over the common mode input range indicated above, large signal differential response was measured by biasing the V_{IP} input at various voltages and applying a $2 V_{pp}$ triangular wave, centered at V_{IP} , to the V_{IN} input. The differential behaviour of the normal output, V_{OUT} , is shown in Figure 5.18 for V_{IP} reference voltages of +0.5V, 0V, -1.5V and -2V. For reference values of 0V and -1.5V, the output exhibits strong differential switching at the reference voltage crossover points, while values of +0.5V and -2V for reference voltages exhibited poor differential response indicating that these references lie out of the common mode range. Additional voltage reference tests indicated that the upper limit for differential response was the 0V value, which defines the transition of the input device from saturation to linear behaviour and is the upper limit of the common mode input voltage range. Thus, the common mode input voltage for this differential amplifier was tested to be -1.92V to 0V.

To measure the differential mode frequency response, the network analyzer was set to sweep the frequency range of 1 MHz to 1 GHz. The measured results, shown in Figure 5.19, indicate that the differential amplifier had a 16 dB differential mode gain and a 3 dB bandwidth of 200 MHz.

a) $V_{ip}=+0.50\text{ V}$ b) $V_{ip}=0\text{ V}$ c) $V_{ip}=-1.50\text{ V}$ d) $V_{ip}=-2.0\text{ V}$ All ScalesVertical: V_{in} : 1 V/div V_{out} : 200 mV/divHorizontal: 200 μ s/div

Input Gnd: 1 div from trace top

Output Gnd: bottom of trace

Figure 5.18. Large Signal Differential Response for the Differential Amplifier.

Figure 5.19. Differential Mode Frequency Response of the Differential Amplifier.

5.6 DISCUSSION

Successful operation of all three A/D subcircuits was achieved. However, some discrepancies in all three sets of measurements had occurred, when experimental results were compared to simulations. After evaluation of the sample-and-hold, it was noted that frequency response and settling time differed from expected values. Both gain and bandwidth were below simulated figures, which can be attributed to the fact that the transconductance, g_m , and the conductance, g_d , were not as predicted. Lower gain will result from lower than expected g_m and R_{ds} values (from equations 4.11 and 4.15) which is consistent with the limitations described by Triquint for their devices. Triquint indicates that g_m decreases more gradually with decreasing I_D than its SPICE model predicts while the model also predicts a higher R_{ds} than actually is present. The lower gain, due to the above deviations, had also directly affected the absolute values obtained for the hold step errors. It should be noted, however, that the measured relative improvement of using charge compensation in this circuit compared well to simulated figures. In terms of bandwidth, inaccuracies in modelling C_{gs} and C_{gd} are likely to be the main contribution to mismatch with measured values. The Triquint model does not accurately predict C_{gs} and C_{gd} at all bias conditions and their measured values appear higher due to lower bandwidth and high acquisition time measurements. Establishing the degree to which these parameters differ from the average values requires complete modelling of the process parameters and device structures.

The only remaining parameter which differs from simulations of the sample-and-hold is the settling time. The longer settling time was likely

due to mismatch of the output impedance of the driving buffer FET to the 50 Ω test environment. With a 200 μm FET, the impedance value was approximately 13 Ω when the sample-and-hold was input biased at 0 V. This impedance will directly produce distortion and cause ringing when used as a source driving a 50 Ω transmission line. This mismatch in impedance was not properly modelled in the SPICE simulations.

Upon measurement of the capacitive differencing comparator and differential amplifier, it was observed that good agreement in switching thresholds and common mode range were experienced. However, both circuits had suffered in terms of gain. Since both structures had incorporated the self-bootstrapped technique for gain improvement, a common gain degradation in circuits using self-bootstrapped MESFETs had resulted. Experience with these structures in reference [4.8] has shown that measured gain was less than predicted and the decrease was attributed to trap related effects of the GaAs material on g_m and by gate leakage effects of this structure. Although these effects may have occurred in device measurement in this work, a more detailed analysis of the self-bootstrapping MESFET to determine modelling parameters is required.

As a final note, measured parameters were limited by accuracy of the test equipment and experimental setup. Noise levels at the lower voltage inputs for sensitivity measurement were a limiting factor along with the accuracy of the DC voltage offset at higher frequencies. However, special care was applied in all setups to produce well calibrated measurements.

CHAPTER 6

CONCLUSIONS

6.1 SUMMARY

The objective of developing improved sample-and-hold and comparator circuits on gallium arsenide was successfully accomplished in this thesis work. The understanding of the circuit requirements and GaAs IC technology itself, provided the means for development of these essential blocks to facilitate operation near gigasample per second rates.

A sample-and-hold with 600pS acquisition time and incorporating a novel technique to improve clock feedthrough by 16 dB, compared to a single D-MESFET switch, was demonstrated. A DC coupled feedback amplifier with greater than 1 GHz 3 dB bandwidth was implemented in this structure. Experimental results agreed with theory which verified the validity of the analytical expressions developed for predicting clocking effects, acquisition and frequency response. Improvements in the sample-and-hold may include incorporating equal width clock compensating devices rather than devices ratioed 1:2 at the input and output nodes, respectively, and eliminating the on-chip capacitor for faster acquisition. An alternative switching arrangement may also be implemented to widen the linear input voltage range.

A novel, capacitive differencing technique, for voltage comparison, was demonstrated to operate at 500 MHz with ± 30 mV resolution which could

be directly implemented in a 6-bit A/D flash converter. The comparator allows a wide input range for comparison and minimizes process dependent problems at the input, such as hysteresis. The circuit could be enhanced by redesign of the latch, to reduce size and power, and by improving the high gain amplifier in terms of bandwidth. Although response was near predicted results, better characterization of the self-bootstrapping technique is required.

The differential amplifier designed in this work could be implemented in a 4-bit flash A/D configuration. A 16 dB gain in differential mode operation was shown which did not agree with expected results. As in the capacitive differencing comparator, a method to analyze the behaviour of a self-bootstrapped structure is necessary to more accurately model response. A knowledge of the degree of variance in circuit operation due to process inconsistencies would also be beneficial but characterizing a large sample of these circuits is required in this regard.

6.2 FUTURE STUDIES

Since analog gallium arsenide circuit design has received less attention than its microwave and digital counterparts, many areas for future work can be pursued. The switching arrangement for the sample-and-hold would benefit from the consideration of alternative structures. During this work, new schemes have been reported which improve linear input range and clock feedthrough [6.1]. Research in faster

acquisition mechanisms for switching would also be useful. Improved integrated switches have direct application in switched-capacitor circuits and in microwave designs. DC coupled amplifier design using gallium arsenide elements is another research topic which can be investigated. Improved structures along with better device characterization would allow amplifiers with wider bandwidth and higher gain to be developed. Advances in this area have also been recently published [6.2-6.3].

With respect to the circuits developed in this thesis, analysis in structural design, processing and alternative technologies would be of benefit. Feedback arrangements for the sample-and-hold and use of advanced processes such as enhancement/depletion and heterojunction bipolar transistors in the comparators would aid in decreasing size, power consumption and circuit sensitivity are all requirements for development of wide bandwidth, high resolution A/D converters.

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- [6.2] Ahlgren, D.J., Ku, W.H., "GAIN-BANDWIDTH PROPERTIES OF A CLASS OF MATCHED FEEDBACK AMPLIFIERS", IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-35, No. 4, Apr. 1987, pp. 361-369.

- [6.3] Imai, Y., Nato, N., Ohwada, K., Sugeta, T., "DESIGN AND PERFORMANCE OF MONOLITHIC GaAs DIRECT-COUPLED PREAMPLIFIERS AND MAIN AMPLIFIERS", IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-33, No. 8, Aug. 1985, pp. 686-692.

APPENDIX A
LISTING OF CIRCUIT SIMULATIONS
USING SPICE

** CIRCUIT: T47C2 SAMPLE-AND-HOLD
 ** FILE: SAMHLD.ACI

** SUBCIRCUIT DEFINITIONS **

* NAC TRIQUINT 5 MICRON FET MODEL

.SUBCKT FS5 1 2 3
 RIN 2 6 0.24
 RS 3 33 180
 RD 1 11 180
 CDS 1 3 0.8FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 5
 DCGS 6 33 D1F 5
 DCGD 6 11 D1F 5
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS5

* NAC TRIQUINT 25 MICRON FET MODEL

.SUBCKT FS25 1 2 3
 RIN 2 6 0.8
 RS 3 33 36
 RD 1 11 36
 CDS 1 3 2.8FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 25
 DCGS 6 33 D1F 25
 DCGD 6 11 D1F 25
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS25

* NAC TRIQUINT 30 MICRON FET MODEL

.SUBCKT FS30 1 2 3
 RIN 2 6 0.94
 RS 3 33 30
 RD 1 11 30
 CDS 1 3 3.3FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 30
 DCGS 6 33 D1F 30
 DCGD 6 11 D1F 30
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS30

* NAC TRIQUINT 50 MICRON FET MODEL

.SUBCKT FS50 1 2 3

RIN 2 6 1.5
 RS 3 33 18
 RD 1 11 18
 CDS 1 3 5.3FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 50
 DCGS 6 33 D1F 50
 DCGD 6 11 D1F 50
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS50

* NAC TRIQUINT 100 MICRON FET MODEL

.SUBCKT FS100 1 2 3
 RIN 2 6 2.9
 RS 3 33 9
 RD 1 11 9
 CDS 1 3 10.3FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 100
 DCGS 6 33 D1F 100
 DCGD 6 11 D1F 100
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS100

* NAC TRIQUINT 200 MICRON FET MODEL

.SUBCKT FS200 1 2 3
 RIN 2 6 1.45
 RS 3 33 4.5
 RD 1 11 4.5
 CDS 1 3 20.6FF
 CGSFRG 6 33 2FF
 CGDFRG 6 11 2FF
 J1 11 66 33 J1F 200
 DCGS 6 33 D1F 200
 DCGD 6 11 D1F 200
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS200

* COMPENSATED SWITCH MODEL

.SUBCKT CSW100 1 2 3 4
 X1 1 4 1 FS25
 X2 1 3 2 FS100
 X3 2 4 2 FS50
 .ENDS CSW100

* TRIQUINT 3 DIODE LEVEL SHIFTER (25 MICRON)

.SUBCKT LSN3 1 2

D1 1 11 NP2 25.5
 D2 11 12 NP2 25.5
 D3 12 2 NP2 25.5
 .ENDS LSN3

**** NAC TRIQUINT PROCESS ACTIVE DEVICE MODELS ****

.MODEL J1F NJF(LAMBDA=0.0625 VTO=-0.90 BETA=1.77E-4 IS=1E-30)
 .MODEL D1F D(IS=1E-15 N=1.16 CJO=1.1FF VJ=0.5 M=0.5 FC=0.0)
 .MODEL NP2 D(IS=1.6E-13 N=1.27 RS=950 BV=2V IBV=0.1UA CJO=2.8FF
 + VJ=1.0 M=0.5 FC=0.0)
 .MODEL NP2H D(IS=1.07E-13 N=1.27 RS=1235 BV=2V IBV=0.1UA CJO=3.36FF
 + VJ=1.0 M=0.5 FC=0.0)
 .MODEL NP2L D(IS=2.4E-13 N=1.27 RS=680 BV=2V IBV=0.1UA CJO=3.36FF
 + VJ=1.0 M=0.5 FC=0.0)
 .MODEL NMF D(IS=2.0E-15 N=1.16 RS=900 BV=7V IBV=0.1UA CJO=2.2FF
 + VJ=0.5 M=0.5 FC=0.0)

**** MAIN CIRCUIT ****

VDD 100 0 DC +4V
 VSS 99 0 DC -4V
 VIN 1 0 DC 0V
 RS 1 2 50
 X1 2 5 3 4 CSW100
 VSA 3 0 PULSE (0V -2V 1NS 100PS 100PS 25NS 50NS)
 VSAN 4 0 PULSE (-2V 0V 1NS 100PS 100PS 25NS 50NS)
 CL 5 0 0.33PF
 X2 6 5 0 FS25
 X3 6 8 0 FS5
 X4 100 6 6 FS30
 X5 100 6 7 FS25
 X6 7 8 LSN3
 X7 8 99 99 FS25
 X8 100 8 9 FS200
 RL 9 0 50

**** OUTPUT CONTROL ****

.OPTIONS LIMPTS=250
 .WIDTH IN=80 OUT=80
 .TRAN .01NS 2NS
 .PRINT TRAN V(9) V(1)
 .END

**** CIRCUIT: T47C2 CAPACITIVE DIFFERENCING COMPARATOR**

**** FILE: CDCOMP.ACI**

**** SUBCIRCUIT DEFINITIONS ****

*** NAC TRIQUINT 5 MICRON FET MODEL**

.SUBCKT FS5 1 2 3
 RIN 2 6 0.24
 RS 3 33 180
 RD 1 11 180
 CDS 1 3 0.8FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 5
 DCGS 6 33 D1F 5
 DCGD 6 11 D1F 5
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS5

*** NAC TRIQUINT 10 MICRON FET MODEL**

.SUBCKT FS10 1 2 3
 RIN 2 6 0.38
 RS 3 33 90
 RD 1 11 90
 CDS 1 3 1.3FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 10
 DCGS 6 33 D1F 10
 DCGD 6 11 D1F 10
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS10

*** NAC TRIQUINT 13 MICRON FET MODEL**

.SUBCKT FS13 1 2 3
 RIN 2 6 0.464
 RS 3 33 69.2
 RD 1 11 69.2
 CDS 1 3 1.6FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 13
 DCGS 6 33 D1F 13
 DCGD 6 11 D1F 13
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS13

*** NAC TRIQUINT 20 MICRON FET MODEL**

.SUBCKT FS20 1 2 3

RIN 2 6 0.66
 RS 3 33 45
 RD 1 11 45
 CDS 1 3 2.3FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 20
 DCGS 6 33 D1F 20
 DCGD 6 11 D1F 20
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS20

* NAC TRIQUINT 25 MICRON FET MODEL

.SUBCKT FS25 1 2 3

RIN 2 6 0.8
 RS 3 33 36
 RD 1 11 36
 CDS 1 3 2.8FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 25
 DCGS 6 33 D1F 25
 DCGD 6 11 D1F 25
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS25

* NAC TRIQUINT 36 MICRON FET MODEL

.SUBCKT FS36 1 2 3

RIN 2 6 1.108
 RS 3 33 25
 RD 1 11 25
 CDS 1 3 3.9FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 36
 DCGS 6 33 D1F 36
 DCGD 6 11 D1F 36
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS36

* NAC TRIQUINT 36 MICRON DUAL-FET MODEL

.SUBCKT FSU36 1 2 3

RIN 2 6 1.108
 RS 3 33 0.001
 RD 1 11 25
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 36
 DCGS 6 33 D1F 36

DCGD 6 11 D1F 36
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FSU36
 .SUBCKT FSL36 1 2 3
 RIN 2 6 1.108
 RS 3 33 25
 RD 1 11 25
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 36
 DCGS 6 33 D1F 36
 DCGD 6 11 D1F 36
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FSL36
 .SUBCKT FSD36 1 2 3 4
 X1 1 2 10 FSU36
 X2 10 3 4 FSL36
 CDS 1 4 3.9FF
 .ENDS FSD36

* NAC TRIQUINT 40 MICRON FET MODEL

.SUBCKT FS40 1 2 3
 RIN 2 6 1.22
 RS 3 33 22.5
 RD 1 11 22.5
 CDS 1 3 4.3FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 40
 DCGS 6 33 D1F 40
 DCGD 6 11 D1F 40
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS40

* NAC TRIQUINT 50 MICRON FET MODEL

.SUBCKT FS50 1 2 3
 RIN 2 6 1.5
 RS 3 33 18
 RD 1 11 18
 CDS 1 3 5.3FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 50
 DCGS 6 33 D1F 50
 DCGD 6 11 D1F 50
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG

.ENDS FS50

* NAC TRIQUINT 100 MICRON FET MODEL

.SUBCKT FS100 1 2 3

RIN 2 6 2.9

RS 3 33 9

RD 1 11 9

CDS 1 3 10.3FF

CGSFRG 6 33 1FF

CGDFRG 6 11 1FF

J1 11 66 33 J1F 100

DCGS 6 33 D1F 100

DCGD 6 11 D1F 100

EVGS 66 33 6 33 0.56

RFX1 1 2 50MEG

RFX2 2 3 50MEG

RFX3 1 3 50MEG

.ENDS FS100

* NAC TRIQUINT 200 MICRON FET MODEL

.SUBCKT FS200 1 2 3

RIN 2 6 1.45

RS 3 33 4.5

RD 1 11 4.5

CDS 1 3 20.6FF

CGSFRG 6 33 2FF

CGDFRG 6 11 2FF

J1 11 66 33 J1F 200

DCGS 6 33 D1F 200

DCGD 6 11 D1F 200

EVGS 66 33 6 33 0.56

RFX1 1 2 50MEG

RFX2 2 3 50MEG

RFX3 1 3 50MEG

.ENDS FS200

* HIGH GAIN LOAD

.SUBCKT HGL 1 2 3

X1 1 2 4 FS25

X2 4 2 3 FS5

.ENDS HGL

* HIGH GAIN DRIVER

.SUBCKT HGD 1 2 3

X1 1 2 4 FS50

X2 4 2 3 FS10

.ENDS HGD

* TRIQUINT 3 DIODE LEVEL SHIFTER (24 MICRON)

.SUBCKT LSN24 1 2

D1 1 11 NP2 24.5

D2 11 12 NP2 24.5

D3 12 2 NP2 24.5

.ENDS LSN24

* TRIQUINT 3 DIODE LEVEL SHIFTER (40 MICRON)

.SUBCKT LSN3 1 2

D1 1 11 NP2 40.5

D2 11 12 NP2 40.5
 D3 12 2 NP2 40.5
 .ENDS LSN3

* F10 INVERTER
 .SUBCKT F10 1 2 3 4
 X1 10 1 0 FS20
 X2 3 10 10 FS13
 X3 3 10 11 FS36
 X4 11 2 LSN24
 X5 2 4 4 FS36
 .ENDS F10

* F11 NAND-NOR
 .SUBCKT F11 1 2 3 4 5 6
 X1 10 1 0 FS20
 X2 10 2 3 0 FSD36
 X3 5 10 10 FS13
 X4 5 10 11 FS36
 X5 11 4 LSN24
 X6 4 6 6 FS36
 .ENDS F11

* LATCH
 .SUBCKT LATCH 1 2 3 4 5 6
 X1 1 10 5 6 F10
 X2 4 2 10 3 5 6 F11
 X3 3 1 2 4 5 6 F11
 .ENDS LATCH

**** NAC TRIQUINT PROCESS ACTIVE DEVICE MODELS ****

.MODEL J1F NJF(LAMBDA=0.0625 VTO=-0.90 BETA=1.77E-4 IS=1E-30)
 .MODEL D1F D(IS=1E-15 N=1.16 CJO=1.1FF VJ=0.5 M=0.5 FC=0.0)
 .MODEL NP2 D(IS=1.6E-13 N=1.27 RS=950 BV=2V IBV=0.1UA CJO=2.8FF
 + VJ=1.0 M=0.5 FC=0.0)
 .MODEL NP2H D(IS=1.07E-13 N=1.27 RS=1235 BV=2V IBV=0.1UA CJO=3.36FF
 + VJ=1.0 M=0.5 FC=0.0)
 .MODEL NP2L D(IS=2.4E-13 N=1.27 RS=680 BV=2V IBV=0.1UA CJO=3.36FF
 + VJ=1.0 M=0.5 FC=0.0)
 .MODEL NMF D(IS=2.0E-15 N=1.16 RS=900 BV=7V IBV=0.1UA CJO=2.2FF
 + VJ=0.5 M=0.5 FC=0.0)

**** MAIN CIRCUIT ****

VDD 100 0 DC 4V
 VSS 99 0 DC -4V
 VIN 1 0 DC 0.1V
 VREF 2 0 DC 0V
 VP1 3 0 PULSE (-2V 0V 0.5NS 100PS 100PS 1NS 2NS)
 VP2 4 0 PULSE (0V -2V 0.5NS 100PS 100PS 1NS 2NS)
 X1 1 3 5 FS100
 X2 2 4 5 FS100
 CC 5 6 30PF
 X3 6 7 8 FS100
 VP3 8 0 PULSE (-0.494V -2.494V 0.5NS 100PS 100PS 1NS 2NS)
 X4 9 6 0 HGD
 X5 100 9 9 HGL

X6 100 9 10 FS40
X7 10 11 LSN3
X8 11 99 99 FS40
X9 11 12 13 14 100 99 LATCH
VP4 12 0 DC 0V
X10 100 13 15 FS200
X11 100 14 16 FS200
RL1 15 0 50
RL2 16 0 50

**** OUTPUT CONTROL ****

.OPTIONS LIMPTS=250
.WIDTH IN=80 OUT=80
.TRAN .01NS 2NS
.PRINT TRAN V(15) V(16) V(11) V(6)
.END

**** CIRCUIT: T47C2 DIFFERENTIAL AMPLIFIER (LOCAL FEEDBACK)**

**** FILE: DIFAMP.ACI**

**** SUBCIRCUIT DEFINITIONS ****

*** NAC TRIQUINT 5 MICRON FET MODEL**

.SUBCKT FS5 1 2 3

RIN 2 6 0.24

RS 3 33 180

RD 1 11 180

CDS 1 3 0.8FF

CGSFRG 6 33 1FF

CGDFRG 6 11 1FF

J1 11 66 33 J1F 5

DCGS 6 33 D1F 5

DCGD 6 11 D1F 5

EVGS 66 33 6 33 0.56

RFX1 1 2 50MEG

RFX2 2 3 50MEG

RFX3 1 3 50MEG

.ENDS FS5

*** NAC TRIQUINT 10 MICRON FET MODEL**

.SUBCKT FS10 1 2 3

RIN 2 6 0.38

RS 3 33 90

RD 1 11 90

CDS 1 3 1.3FF

CGSFRG 6 33 1FF

CGDFRG 6 11 1FF

J1 11 66 33 J1F 10

DCGS 6 33 D1F 10

DCGD 6 11 D1F 10

EVGS 66 33 6 33 0.56

RFX1 1 2 50MEG

RFX2 2 3 50MEG

RFX3 1 3 50MEG

.ENDS FS10

*** NAC TRIQUINT 25 MICRON FET MODEL**

.SUBCKT FS25 1 2 3

RIN 2 6 0.8

RS 3 33 36

RD 1 11 36

CDS 1 3 2.8FF

CGSFRG 6 33 1FF

CGDFRG 6 11 1FF

J1 11 66 33 J1F 25

DCGS 6 33 D1F 25

DCGD 6 11 D1F 25

EVGS 66 33 6 33 0.56

RFX1 1 2 50MEG

RFX2 2 3 50MEG

RFX3 1 3 50MEG

.ENDS FS25

*** NAC TRIQUINT 40 MICRON FET MODEL**

.SUBCKT FS40 1 2 3

RIN 2 6 1.22
 RS 3 33 22.5
 RD 1 11 22.5
 CDS 1 3 4.3FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 40
 DCGS 6 33 D1F 40
 DCGD 6 11 D1F 40
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS40

* NAC TRIQUINT 50 MICRON FET MODEL

.SUBCKT FS50 1 2 3
 RIN 2 6 1.5
 RS 3 33 18
 RD 1 11 18
 CDS 1 3 5.3FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 50
 DCGS 6 33 D1F 50
 DCGD 6 11 D1F 50
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS50

* NAC TRIQUINT 100 MICRON FET MODEL

.SUBCKT FS100 1 2 3
 RIN 2 6 2.9
 RS 3 33 9
 RD 1 11 9
 CDS 1 3 10.3FF
 CGSFRG 6 33 1FF
 CGDFRG 6 11 1FF
 J1 11 66 33 J1F 100
 DCGS 6 33 D1F 100
 DCGD 6 11 D1F 100
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS100

* NAC TRIQUINT 200 MICRON FET MODEL

.SUBCKT FS200 1 2 3
 RIN 2 6 1.45
 RS 3 33 4.5
 RD 1 11 4.5
 CDS 1 3 20.6FF
 CGSFRG 6 33 2FF
 CGDFRG 6 11 2FF
 J1 11 66 33 J1F 200

DCGS 6 33 D1F 200
 DCGD 6 11 D1F 200
 EVGS 66 33 6 33 0.56
 RFIX1 1 2 50MEG
 RFIX2 2 3 50MEG
 RFIX3 1 3 50MEG
 .ENDS FS200

* HIGH GAIN LOAD
 .SUBCKT HGL 1 2 3
 X1 1 2 4 FS25
 X2 4 2 3 FS5
 .ENDS HGL

* HIGH GAIN DRIVER
 .SUBCKT HGD 1 2 3
 X1 1 2 4 FS50
 X2 4 2 3 FS10
 .ENDS HGD

* TRIQUINT 2 DIODE LEVEL SHIFTER (10 MICRON)
 .SUBCKT LSN2 1 2
 D1 1 11 NP2 10.5
 D2 11 2 NP2 10.5
 .ENDS LSN2

* TRIQUINT 3 DIODE LEVEL SHIFTER (40 MICRON)
 .SUBCKT LSN3 1 2
 D1 1 11 NP2 40.5
 D2 11 12 NP2 40.5
 D3 12 2 NP2 40.5
 .ENDS LSN3

* TRIQUINT 4 DIODE LEVEL SHIFTER (40 MICRON)
 .SUBCKT LSN4 1 2
 D1 1 11 NP2 40.5
 D2 11 12 NP2 40.5
 D3 12 13 NP2 40.5
 D4 13 2 NP2 40.5
 .ENDS LSN4

** NAC TRIQUINT PROCESS ACTIVE DEVICE MODELS **

.MODEL J1F NJF(LAMBDA=0.0625 VTO=-0.90 BETA=1.77E-4 IS=1E-30)
 .MODEL D1F D(IS=1E-15 N=1.16 CJO=1.1FF VJ=0.5 M=0.5 FC=0.0)
 .MODEL NP2 D(IS=1.6E-13 N=1.27 RS=950 BV=2V IBV=0.1UA CJO=2.8FF
 + VJ=1.0 M=0.5 FC=0.0)
 .MODEL NP2H D(IS=1.07E-13 N=1.27 RS=1235 BV=2V IBV=0.1UA CJO=3.36FF
 + VJ=1.0 M=0.5 FC=0.0)
 .MODEL NP2L D(IS=2.4E-13 N=1.27 RS=680 BV=2V IBV=0.1UA CJO=3.36FF
 + VJ=1.0 M=0.5 FC=0.0)
 .MODEL NMF D(IS=2.0E-15 N=1.16 RS=900 BV=7V IBV=0.1UA CJO=2.2FF
 + VJ=0.5 M=0.5 FC=0.0)

** MAIN CIRCUIT **

VDD 100 0 DC 4V
 VSS 99 0 DC -4V

VIP 1 0 DC -1.75V
VIN 2 0 -1.75V AC 1V 0
X1 100 4 4 HGL
X2 100 5 5 HGL
X3 4 1 3 HGD
X4 5 2 3 HGD
X5 3 7 8 FS10
X6 8 99 LSN2
X7 100 4 6 FS40
X8 6 7 LSN4
X9 7 99 99 F140
X10 100 5 9 FS40
X11 9 10 LSN3
X12 10 99 99 FS40
X13 100 10 11 FS100
RL1 11 0 50

**** OUTPUT CONTROL ****

.OPTIONS LIMPTS=250
.WIDTH IN=80 OUT=80
.AC DEC 50 1MEG 10000MEG
.PRINT AC VDB(11) VP(11)
.END

END

1|4|09|90

FIN