

Robust Subthreshold CMOS Voltage-Controlled Frequency Synthesizer for Wireless Dosimeter Application

by

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Abstract

Detailed study of MOSFET behavior in the subthreshold region of operation is conducted with the 0.13 μm CMOS IBM technology. High sensitivity of subthreshold CMOS circuits to process variations is addressed. Two body-biasing circuits for stabilizing the subthreshold current of n-channel (NMOS) and p-channel (PMOS) devices are introduced. These stabilization schemes are applied to a voltage-controlled frequency synthesizer (VCFS) operating in the subthreshold region to design a robust, high resolution and ultra-low power (ULP) signal processing unit (SPU). The intended application is a wireless dosimeter, which converts radiation doses in the range of -900 mV to 0 to pulses with varying frequencies. Simulation results show a linear frequency vs. sensitivity response, generating pulses with 50% duty cycle for all inputs. The SPU yields a maximum error of 210 mV or 24% (6 Gy), minimum resolution of 15 KHz/Gy, minimum bandwidth of 805 KHz and maximum power consumption of 1.72 μW .

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Dedication

This dissertation is dedicated to...

my lovely parents, sisters and brother

for their unconditional love, patience, and support.

**In the Name of God,
the Compassionate, the Merciful**

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List of Acronyms

CBB	Conventional Body Bias
CMOS	Complementary MOS
CoC	Current Over Capacitance
CPU	Central Processing Unit
DBB	Dynamic Body Bias
DG-MOSFET	Double-Gate MOSFET
DML	Dual Mode Logic
DTMOS	Dynamic Threshold MOS
EDP	Energy Delay Product
FBB	Forward Body Bias
FG-MOSFET	Floating-Gate MOSFET
MCML	MOSFET Current Mode Logic
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NDBB	NMOS Dynamic Body Bias
NMOS	N-channel MOS
PDBB	PMOS Dynamic Body Bias
PDP	Power Delay Product
PMOS	P-channel MOS
PVT	Process Voltage Temperature
RF	Radio Frequency
RFID	Radio Frequency Identification
RO	Ring Oscillator
SBB	Swapped Body Bias
SPU	Signal Processing Unit
SRAM	Static Random Access Memory
ST	Schmitt Trigger
ST-BB	Static Body Bias
STRO	Schmitt Trigger Ring Oscillator
STSCl	Subthreshold Source Coupled Logic
ULP	Ultra-Low Power
VCCM	Voltage-Controlled Current Mirror
VCFS	Voltage-Controlled Frequency Synthesizer
VLSI	Very Large Scale Integrated
VT-Sub-CMOS	Variable-Threshold Subthreshold CMOS

Chapter 1. Introduction

As the demand for ultra-low power (ULP) applications continue to grow, subthreshold complementary MOSFET (CMOS) circuits have become a subject for researchers. These circuits typically operate with less than a quarter of the supply voltage required for conventional CMOS circuits operating in superthreshold. Many design optimization techniques have been explored by researchers to reduce the power consumption of analog and digital circuits. However, the most convenient way of doing this is to reduce the supply voltage as it has a square relationship with the energy dissipation of the circuit. In subthreshold circuits, the supply is reduced to levels where transistors operate with a gate-source voltage less than their threshold. Transistors use the subthreshold current, which has the greatest contribution to leakage in commonly used superthreshold circuits, as their driving force. This small current is governed by a different equation than the saturation current. Consequently, new issues are encountered in the subthreshold region. Some of these problems include low speed and high sensitivity to process, voltage and temperature (PVT) variations.

Wireless biomedical sensors are one of the most important ULP applications of subthreshold circuits [1]. They are composed of many parts such as power harvesting, sensing, read circuitry, signal processing and radio frequency identification (RFID) functions. Since sensors generally operate at a very low speed, the signal processing unit (SPU) is a suitable candidate for subthreshold operation. However, design challenges associated with subthreshold circuits should carefully be addressed. Robustness enhancement and decreasing sensitivities to process variations at minimal energy cost are essential for such applications.

1.1. Motivation

Wireless dosimetry is a portable ULP biomedical application, where power consumption is the major design criterion rather than speed. Blood bags that contain irradiated blood using X or Gamma radiation, require dose measurement for medical purposes. Previous designs have advanced as far as measuring dose using color tags or wired electronic circuits. Color tags depend on human eyes for measurement, and thus lack accuracy. Moreover, wired circuits are not portable and occupy a lot of space. Therefore, a wireless design for dose measurement is an enhancement to previous solutions in terms of portability and precision. On the basis of this motivation, the wireless dosimeter project was established as a collaboration between Carleton University and Best Medical Canada. The energy harvesting unit and Floating-Gate MOSFET (FG-MOSFET) sensor embedded in read circuitry have been previously developed by two other team members [2] [3]. A signal processing unit is to be designed to convert sensed voltage levels into a pulse train.

Using a wireless approach instead of the previous techniques for dosimetry introduces a major challenge. Since the radio frequency (RF) energy harvesting unit provides limited energy per time to all blocks, power constraint becomes a primary issue. Consequently, minimum energy dissipation becomes the major design specifications of the SPU. Subthreshold CMOS circuits use the most fundamental method of decreasing voltage supply to minimize energy dissipation. Therefore, subthreshold design becomes a perfect candidate for the SPU design.

Although subthreshold circuits benefit from minimum power consumption, they suffer from high sensitivity to process variation. This problem occurs due to the exponential relationship between subthreshold current and the threshold and gate-source voltage. Researchers have found different solutions to this problem. Logic families such as MOSFET current mode logic (MCML), dynamic-threshold CMOS (DT-CMOS) and variable-threshold subthreshold CMOS (VT-sub-CMOS) are introduced for improving the robustness of digital subthreshold circuits [4] [5] [6]. Modeling techniques to predict process variations and statistical application-dependant methods to select the supply and threshold voltage have been suggested [7] [8]. Moreover, appropriate device choice, such as Double-Gate (DG) MOSFET, for enhanced robustness has been suggested [9]. Model-

ing MOSFET process steps that affect process variations, such as plasma-induced damage, has also been completed [10].

While researchers have suggested some solutions to parameter variability problems for subthreshold circuits, several issues remain. Specific logic families are being introduced for improving the robustness of digital components rather than analog circuits, such as oscillators. Process variation prediction using statistical modeling or choosing a robust device is not helpful when restricted to a certain technology for implementation. Moreover, enhancing process steps is costly and impossible to impose when only a certain process is available. Therefore, minimizing subthreshold current sensitivity to process variations using a circuit design approach at minimal energy cost constitutes a promising research topic.

1.2. Thesis Objectives

The general purpose of this thesis is to introduce a novel method to increase the robustness of subthreshold circuits and demonstrate the feasibility of using subthreshold CMOS circuit design techniques for ULP wireless sensor signal processing applications using the 0.13 μm IBM CMOS technology.

The specific objectives of this work are as follows:

1. Investigate subthreshold circuit design, their benefits, and challenges, as well as sensor signal processing for wireless applications.
2. Explore operation characteristics of MOSFETs in 0.13 μm IBM CMOS technology in the subthreshold regime and use design techniques for speed and robustness enhancement.
3. Design, optimize, fabricate and test a subthreshold voltage-controlled frequency synthesizer (VCFS) signal processing unit to convert measured radiation doses to pulses with different frequencies for a wireless dosimeter.
4. Introduce a novel circuit design method to increase the robustness of subthreshold circuits and reduce their sensitivity to process variations. Apply this technique to the VCFS to enhance the robustness of the proposed SPU.

1.3. Thesis Outline

After this introductory chapter, the second chapter begins with background information of theory of MOSFET characteristics in the subthreshold region. Furthermore, a comprehensive literature review for subthreshold operation and wireless sensor signal processing is completed.

MOSFET subthreshold operation in 0.13 μm IBM technology is further explored in Chapter 3 using Cadence Virtuoso. Chapter 4 presents a detailed design of the proposed subthreshold SPU for the wireless dosimeter using theoretical calculations and simulation results for each block. Chapter 5 explains the layout procedure and implementation along with the testing strategy and results.

Chapter 6 introduces a novel circuit solution to decrease the MOSFET's sensitivity to process variations in the subthreshold region of operation. This method includes an NMOS circuit for body biasing of NMOS transistors and a PMOS circuit designed to bias the body of PMOS transistors. It is applied to the previously designed VCFS to produce a more robust SPU design.

Final remarks, conclusions and future work based on the results of this thesis are proposed in chapter 7.

Chapter 2. Review of CMOS Circuit Design in the Subthreshold Region and Wireless Sensor Signal Processing

CMOS transistors could be used in three main regions of operation: saturation, linear and subthreshold. Each of these areas has its own set of rules along with advantages and disadvantages. Subthreshold circuit design is suitable for low frequency electronic circuits that are power limited. Therefore, it lends itself to biomedical applications, such as wireless dosimetry, where power consumption is the main concern. A major block of the wireless dosimeter is signal processing, since the sensed data needs to be converted to meaningful information for the receiver.

In this regard, this chapter is divided into three sections: the first part explains the theory of subthreshold circuits by expanding on the current-voltage relationship, capacitances and leakage. Furthermore, the benefits and challenges associated with subthreshold circuits are explored. The next section reviews the latest advances on CMOS circuit design in the subthreshold region. The last part of the chapter explores the recent progress on ULP sensor signal processing circuits for wireless applications.

2.1. MOSFET in the Subthreshold Region

MOSFET is a four-terminal symmetrical device as shown in Figure 1. NMOS transistors contain doping areas within a p-substrate, while PMOS devices are formed on an n-substrate. The MOSFET terminals are gate (G), source (S), drain (D) and body or bulk (B). There is no physical difference between drain and source terminals, hence the symmetry [11]. Channel width (W) and length (L) are the main design parameters of MOSFETs that affect current and capacitance. It should be noted that all formulas in this chapter are written for NMOS devices. The relations for PMOS transistors can be extracted easily using absolute values of all currents and voltage parameters.

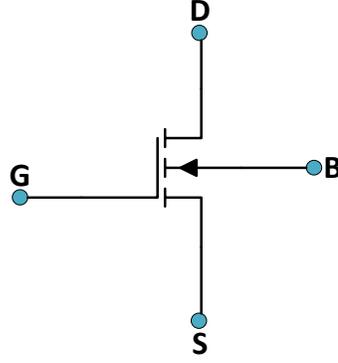


Figure 1 MOSFET device and its gate, drain, source and body terminals.

2.1.1 MOSFET Current

Probably the most common MOSFET current model in electronic texts is the Shockley model [12]. However, this model is only valid for long channel devices, where saturation occurs due to the pinch-off effect. For short channel devices, such as the 0.13 μm technology used for this thesis work, velocity saturation becomes the deciding factor [11]. Thus, a more precise alpha-power law model is introduced [13]:

$$I_{ds} = \begin{cases} \beta v_T^2 e^{1.8} e^{\frac{V_{gs} - V_{th}}{nv_T}} \left(1 - e^{-\frac{V_{ds}}{v_T}}\right) & V_{gs} < V_{th} \text{ (Subthreshold)} \\ P_c \frac{\beta}{2} (V_{gs} - V_{th})^\alpha \cdot \frac{V_{ds}}{V_{dsat}} & V_{gs} > V_{th}, V_{ds} < V_{dsat} \text{ (Linear)} \\ P_c \frac{\beta}{2} (V_{gs} - V_{th})^\alpha & V_{gs} > V_{th}, V_{ds} > V_{dsat} \text{ (Saturation)} \end{cases} \quad (2-1)$$

where:

$$V_{dsat} = P_v (V_{gs} - V_{th})^{\alpha/2} \quad (2-2)$$

$$\beta = \mu C_{ox} \frac{W}{L}, C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad (2-3)$$

$$n = 1 + \frac{C_{dep}}{C_{ox}} \quad (2-4)$$

$$v_T = \frac{KT}{q} \quad (2-5)$$

and P_c , P_v and α are technology-dependant parameters that can be found using curve fitting of the DC plots. Parameter μ defines the mobility of mobile charges, C_{ox} is the gate-oxide capacitance per unit area, t_{ox} is the oxide thickness and ϵ_{ox} represents the permittivity of SiO_2 . The gate-source, drain-source, drain-source saturation and threshold voltages are presented by V_{gs} , V_{ds} , V_{dsat} and V_{th} respectively. Capacitance per unit area of the depletion layer under the gate is shown by C_{dep} . The thermal voltage, temperature, temperature coefficient and electron charge are defined by v_T , T , K and q in order. The subthreshold slope factor is denoted by n . This factor varies according to the depletion region and is typically in the range of 1.3-1.7. It can further be re-written as [14]:

$$n = 1 + \frac{C_{dep}}{C_{ox}} = 1 + \frac{\epsilon_{Si}/W_{dep}}{\epsilon_{ox}/t_{ox}} \approx 1 + 3 \frac{t_{ox}}{W_{dep}} \quad (2-6)$$

Looking back at the subthreshold current equation in (2-1), it can be observed that as V_{ds} exceeds some multiples of v_T , the current becomes independent of drain-source voltage. Moreover, unlike the linear and saturation currents, the subthreshold current has an exponential relationship with V_{th} , V_{gs} and v_T . Therefore, smallest changes in either one of these voltages can cause a significant change in the subthreshold current. Consequently, the sensitivity to PVT variations has increased. As a result of the exponential voltage – current relationship, I_{ds} - V_{gs} slope can be expressed on a semi-logarithmic scale using (2-1) as:

$$\frac{\partial(\log_{10} I_{ds})}{\partial V_{gs}} = (\log_{10} e) \frac{1}{nv_T} \quad (2-7)$$

The inverse of the above equation is called the *subthreshold slope*, S , which is one of the important figures for subthreshold operation [15]:

$$S = nv_T \ln(10) \approx 2.3v_T \left(1 + 3 \frac{t_{ox}}{W_{dep}} \right) \quad (2-8)$$

where W_{dep} is the maximum depletion layer width. Depending on the technology, S is typically in the range of 70-100 mV/dec [15]. Ideally, the subthreshold slope should be as small as possible to minimize leakage when a transistor is off.

2.1.2 MOSFET Threshold Voltage

The threshold voltage of MOSFET is an important parameter that determines whether the device is in the subthreshold or superthreshold regime. The MOSFET threshold voltage, V_{th} , can be modelled using the equation below for superthreshold operation [12]:

$$V_{th} = V_{th0} + \gamma \left(\sqrt{|2\phi_F + V_{sb}|} - \sqrt{|2\phi_F|} \right) \quad (2-9)$$

where V_{sb} is the source-body potential, V_{th0} is the zero- V_{sb} threshold voltage. The body-effect coefficient is denoted by γ , and $2\phi_F$ is the approximate potential drop between surface and bulk across the depletion layer when $V_{sb} = 0$. However, V_{th} can be approximated with linear equation in the subthreshold region, as below [1]:

$$V_{th} = V_{th0} - \lambda_{ds}V_{ds} - \lambda_{bs}V_{bs} \quad (2-10)$$

Where V_{bs} is the bulk-source potential and V_{th0} is given by [16]:

$$V_{th0} = V_{fb} + \psi_{st} + \frac{Q_{dep}}{C_{ox}} \quad (2-11)$$

and λ_{ds} and λ_{bs} are known as the drain-induced barrier lowering (DIBL) and body effect coefficient for a MOSFET operating in the subthreshold region. These coefficients can be extracted using simulations for a given technology. The flat-band voltage, V_{fb} , and surface potential at the edge of threshold, ψ_{st} , are both constant for a technology. The depletion region charge that changes depending on transistor sizing is shown by Q_{dep} . For an NMOS transistor operating in the subthreshold region, increasing the body-source voltage increases the current. The opposite holds for PMOS devices. Therefore, using proper dynamic body-biasing techniques, the transistor current can be stabilized in response to process variations.

2.1.3 MOSFET Capacitances

MOSFET capacitances have important effects on the delay and power consumption of device. Figure 2 shows the capacitances between every two terminals of a MOSFET. These capacitances can be grouped into gate-oxide and diffusion (junction) capacitances [14]. The drain-source capacitance is negligible [14]. Figure 3 presents the breakdown of junction capacitances into bottom and sidewall components using geometric representation of MOSFET.

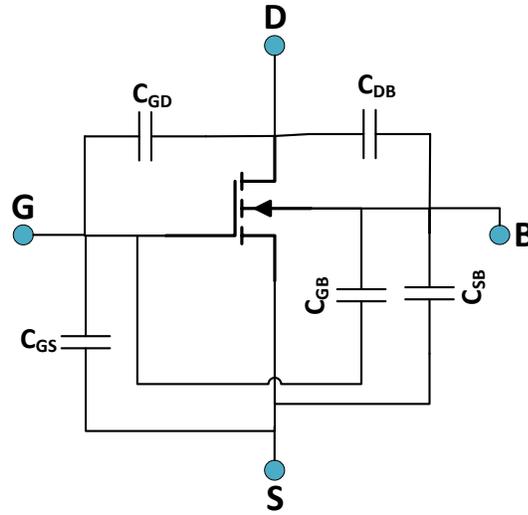


Figure 2 MOSFET Capacitances.

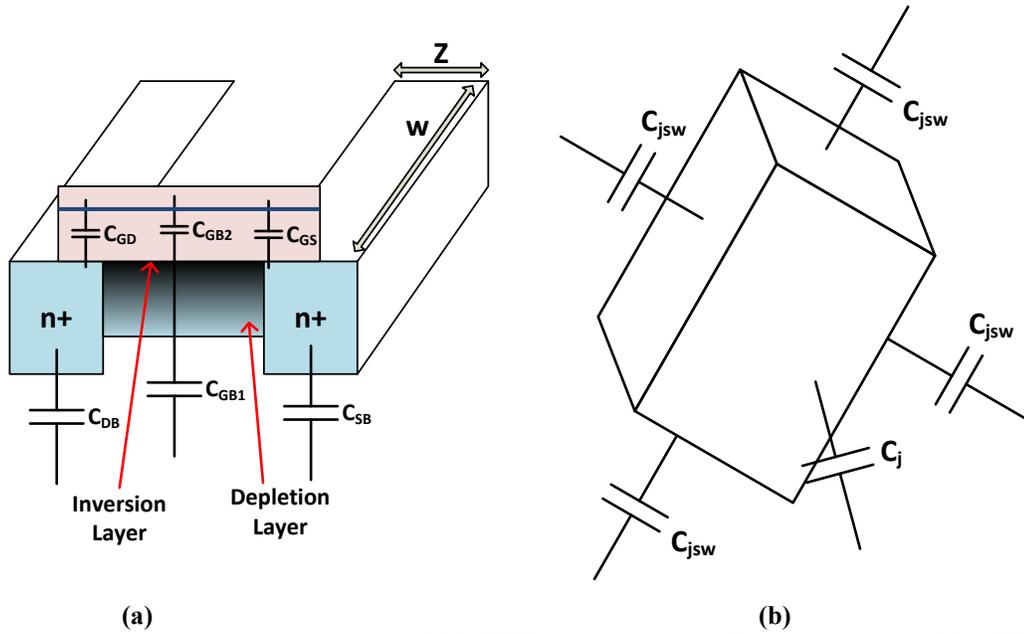


Figure 3 a) Geometric representation of MOSFET Capacitances b) Decomposition of MOSFET capacitances.

The capacitances shown in Figure 2 and Figure 3 can be calculated as below [11]:

- C_{GB1} : Oxide capacitance between gate and the channel:

$$C_{GB1} = C_{ox}WL = WL \frac{\epsilon_{ox}}{t_{ox}} \quad (2-12)$$

- C_{GB2} : Depletion capacitance between channel and the substrate:

$$C_{GB2} = C_{dep}WL = WL \frac{\epsilon_{si}}{W_{dep}} \quad (2-13)$$

- C_{GS} , C_{GD} : Gate capacitances to source/drain due to overlap of gate poly with source/drain. They are estimated in MOSFET models by $C_{gsov}W$ and $C_{gdov}W$ respectively.
- C_{SB} , C_{DB} : Junction capacitances between source/drain and the substrate and can be written as:

$$C_{SB} = C_{DB} = C_j A + C_{jsw}(Perim - W) + C_{jswq}W \quad (2-14)$$

where:

$$A = WZ, \quad Perim = 2(W + Z) \quad (2-15)$$

and A and $Perim$ denote the area and perimeter of the drain/source. Capacitance per unit area between the bottom junction and substrate is expressed by C_j . Capacitance per unit length between the 3 sidewalls of the junction and the bulk that are not facing the channel is shown by C_{jsw} . Capacitance per unit length between the side of the junction facing the channel is symbolized by C_{jswq} . Components of junction capacitances are functions of the source/drain voltages. For example, C_j can be expressed as [12]:

$$C_j = C_{j0} \left(1 + \frac{V_R}{\psi_b} \right)^{-M_j} \quad (2-16)$$

where C_{j0} is the junction capacitance at zero bias, M_j is the junction grading coefficient. The built-in voltage is ψ_b and V_R denotes the reverse voltage across the junction.

Table 1 summarizes the approximation of total capacitances in the three operating regions of MOSFETs. As it can be seen, in the subthreshold region of operation, overlap capacitances are decreased, while the oxide capacitance is increased.

Table 1 MOSFET total capacitance approximation.

Capacitance	Expression		
Total Junction Capacitance	$C_j A + C_{jsw}(Perim - W) + C_{jswq} W$		
Region of Operation			
	Subthreshold	Triode	Saturation
C_{GS}	$C_{gsov} W$	$C_{GB1}/2 + C_{gsov} W$	$2C_{GB1}/3 + C_{gsov} W$
C_{GD}	$C_{gdov} W$	$C_{GB1}/2 + C_{gsov} W$	$C_{gdov} W$
C_{GB}	$\frac{C_{GB1} C_{GB2}}{C_{GB1} + C_{GB2}}$	0	0

2.1.4 MOSFET Leakage Currents

Leakage currents are responsible for static power consumption in electronic circuits. Static power loss occurs when the circuit is in idle mode. Generally, in superthreshold circuits, the major leakage is the subthreshold current [1]. Subthreshold circuits, however, take advantage of this leakage current for their operation.

The three main sources of leakage in MOSFETs operating in the subthreshold mode the order of significance are:

1. *Gate Oxide Tunneling Leakage (I_G)*: the current due to the electric field across the gate oxide. This field creates electron tunneling from gate to the substrate or source and drain [17]. This current increases exponentially with the oxide thickness and becomes significant for technologies smaller than 100nm [14].
2. *Reverse-biased Junctions Leakage (I_{junc})*: The leaking current via the reverse biased connection between the source/drain and the body terminal. Its magnitude is highly dependent on the doping concentration and area of the source/drain and well diffusions [17].
3. *Gate-Induced Drain Leakage (I_{GIDL})*: The tunneling current at the drain edge caused by the high electric field in the drain junction of MOSFET [17]. This field is due to halo doping in the vicinity of the drain junction.

The doping is done to control punch-through and DIBL in nano-scale technologies [15].

Leakage currents in the subthreshold region can become significant for small technologies. Consequently, it is compulsory to reduce leakage for digital VLSI subthreshold circuits. Researchers have explored different methods to do so for a variety of subthreshold applications. Some of these solutions are explored in the literature in 2.3.

2.2. CMOS Subthreshold Circuits: Benefits and Challenges

Subthreshold circuits are designed based on the simple concept of decreasing the supply voltage in order to reduce the energy consumption. The dynamic energy and power consumptions of a CMOS circuit are governed by [14]:

$$E_{DY} = CV_{DD}^2 \quad (2-17)$$

$$P_{DY} = CV_{DD}^2 f \quad (2-18)$$

where supply voltage, dynamic energy and power are represented by V_{DD} , E_{DY} and P_{DY} respectively. Total capacitance is C and frequency of the circuit is symbolized by f . As the above formulas suggest, lowering V_{DD} has a subsequent squared decrease on the total dynamic energy and power. This is the main reason why subthreshold circuits are a subject of interest for ULP applications. Some of these applications include wireless sensors, implantable devices/networks, ambient intelligence, wearable computing, smart grids and plant monitoring and static random access memories (SRAM) [1]. The optimum supply voltage value for subthreshold operation is application-dependant. For example, if the main design limitation is minimal sensitivity to process variations, V_{DD} has to be selected for maximum robustness. For ULP applications, V_{DD} has to be decreased as far as other design specifications to minimize power consumption.

Another significant benefit of subthreshold circuits is their decreased leakage current and static power loss. The static power consumption of a CMOS circuit, P_{ST} , is given by [14]:

$$P_{ST} = V_{DD}I_{Leak} \quad (2-19)$$

where I_{Leak} is the total leakage current of the circuit. Using smaller supply voltage values for subthreshold circuits leads to a linear decrease in static power consumption. This

holds true assuming an equal leakage current for subthreshold and superthreshold circuits. However, the leakage current for subthreshold circuits is also decreased, resulting in further static energy saving. Subthreshold current is the main source of leakage in superthreshold circuits. This leakage component, which governs subthreshold operation, is much larger than other leakage currents discussed in 2.1.4 [17].

Although subthreshold circuits are superior to superthreshold ones in terms of power consumption, they do have drawbacks and challenges. The main concerns with subthreshold design are low speed and high PVT variations. Since the subthreshold current is much smaller than the saturation or triode one, the speed of the circuit is significantly reduced. Furthermore, the exponential relationship between V_{th} , V_{GS} , v_T and the subthreshold current results in high sensitivities to PVT variations. Variation of the threshold voltage due to process is the main reason for subthreshold current's dependency on the process [14]. These variations are caused by ion implantation that is a stochastic process. This process step determines the number and location of dopant atoms within the channel or halo region [14].

When using subthreshold circuits with neighboring superthreshold ones, designing an additional block is imposed. Since subthreshold circuits use smaller V_{DD} , their output cannot be connected to superthreshold blocks without voltage level adjustments. Therefore, the need for level shifters for these subthreshold circuits arises. Additional circuitry for subthreshold circuits results in more complexity and space.

Researchers have suggested some solutions for subthreshold circuit design challenges. Some of the recent advancements on these topics will be investigated in the next section. Table 2 Summarizes the benefits and challenges of subthreshold circuit design.

Table 2 CMOS subthreshold circuit design benefits and challenges.

CMOS Subthreshold circuit design benefit	CMOS Subthreshold circuit design challenge
Low dynamic power consumption	Low speed
Low static power consumption and leakage current	High sensitivity to PVT variations
	May have need for additional circuitry such as level shifter

2.3. Literature Review: CMOS Circuit Design in the Subthreshold Region

To overcome the challenges of designing subthreshold circuits, researchers have suggested different solutions design challenges of Table 2. Different techniques, such as logic styles, device choice, circuit level enhancements and design optimization methods have been suggested for that purpose. This section reviews some of the recent progress on overcoming some of the issues associated with CMOS circuit design in the subthreshold region.

2.3.1 CMOS Logic Families in the Subthreshold Region

Soeleman introduced VT-Sub-CMOS and subthreshold DTMOS logic styles [6]. Results show superior robustness and tolerance to temperature and process variations as well as yielding higher speed compared to regular logic families. However, due to body biasing of the NMOS transistor, both circuits can only be implemented using the triple-well process. Figure 4 to Figure 6 show the VT-Sub-CMOS, its stabilization circuit and Sub-DTMOS logic respectively. The body-biasing scheme used for the VT-Sub-CMOS family is complicated. The number of stages of the charge pump depends on the capacitive load imposed by the circuit under stabilization. Most importantly, the body-biasing circuit's proper operation for both NMOS and PMOS devices is not clarified. The threshold voltage of NMOS and PMOS devices has an opposite relationship with body-source voltage as discussed in 2.1.2. Consequently, designing a common stabilization scheme for both devices is questionable. There is also no theoretical analysis demonstrating the improvements of the suggested logic styles.

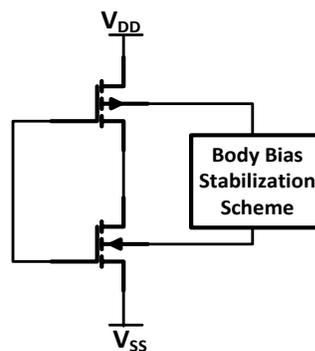


Figure 4 VT-Sub-CMOS logic family [6].

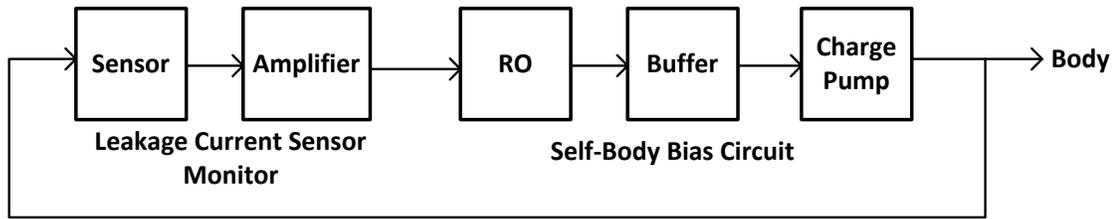


Figure 5 VT-Sub-CMOS stabilization circuit [6].

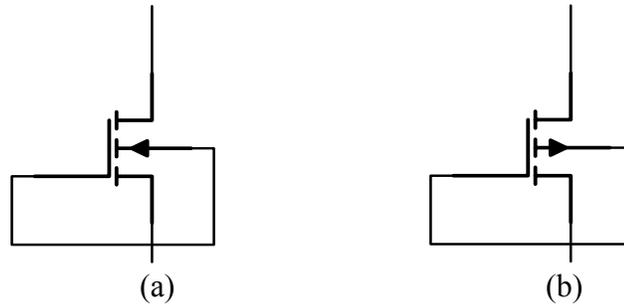


Figure 6 a) DT-NMOS b) DT-PMOS logic family [6].

Tajalli suggests a novel approach for subthreshold circuit implementation using the subthreshold source coupled logic (STSCCL) [18]. The logic style is presented in Figure 7. Varying the tail bias current results in linear down-scaling of the power consumption and operating frequency. Simulations using 0.18 μm CMOS technology show that the current can be decreased up to 10 pA using a voltage supply of 300 mV, resulting in a power-delay product (PDP) of less than 1 fJ. Some disadvantages of this logic style are increased complexity and area due to the bias circuit. Recent research shows particular interest in the current-driven SCL and MCML logic families for the subthreshold region due to increased robustness and minimum power consumption [4] [19] [20] [21] [22].

Kaizerman introduces the dual-mode-logic (DML) for subthreshold circuits, featuring an alternation between static and dynamic modes of operation [23]. In the static mode, the circuit consumes very low power as required. When operating in dynamic mode however, there is an increase in speed and energy consumption. Figure 8 represents two types of topologies (type A and type B) for the proposed logic. Simulation for 100 stage chains in two different structures (type A followed by type B or AB, type A followed by an Inverter, or AI) are completed in the 80 nm technology. Results show 10x speed improvement compared to static CMOS and improved robustness in oppose to dy-

dynamic logic. Furthermore, DML shows 2.2x and 5x less energy dissipation in oppose to static CMOS and domino logics.

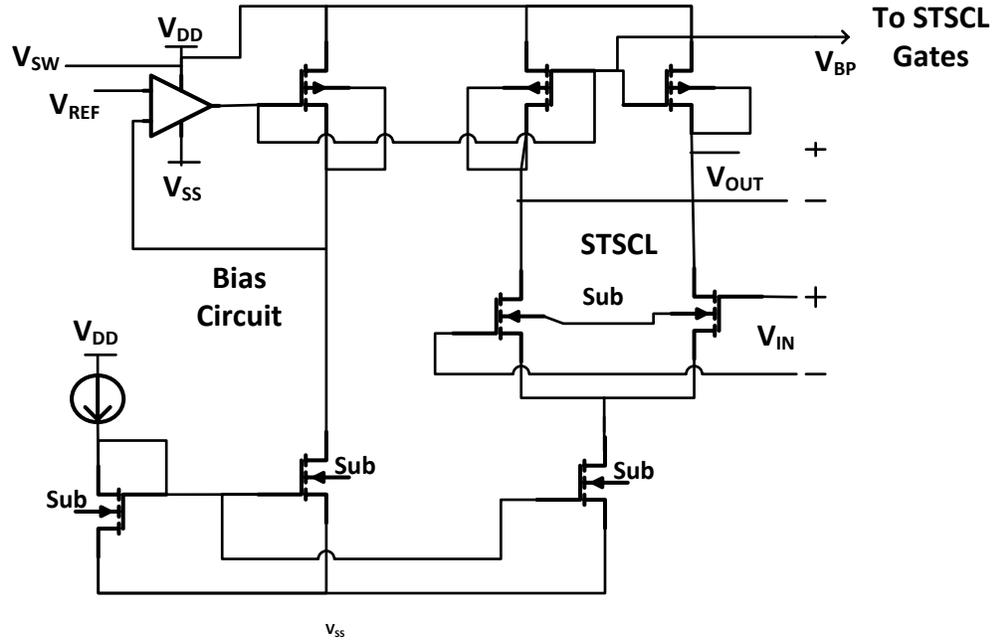


Figure 7 STSCL logic family with replica bias circuit [18].

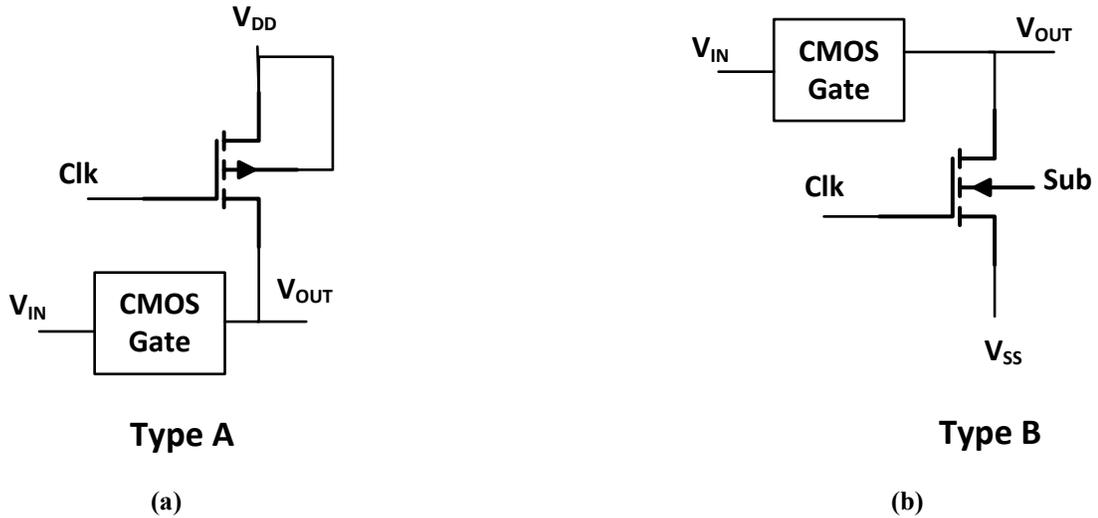


Figure 8 a) Type A DML b) Type B DML logics [23].

2.3.2 Increasing the Speed of Subthreshold Circuits

Kean has proposed a new optimized sizing strategy, modifying the logical effort method for subthreshold circuits [24]. Experimental results using the ISCAS benchmark circuits show a performance improvement of about 13.5% compared to conventional logical effort method. In this new sizing method, the stack transistors are resized according to an added factor of α .

Muker and Shams have proposed a new method for increasing subthreshold frequency of operation by using parallel transistor stacks [25]. Transistor sizing has been done by considering the inverse-narrow width effect (INWE), which results in lower threshold voltage. Transistor channel widths that maximize current to capacitance (CoC) ratio individually or in parallel stacks have been used. Simulation results show speed improvement of almost 2.85x compared to conventional circuits for a ring oscillator in the 65 nm technology.

Ramezankhani has done extensive research on delay improvement for subthreshold circuits for his M.Sc. thesis. He introduces a method based on the relationship between channel length and capacitance to find the optimum channel length for minimum delay [26]. The effectiveness of the CoC method for channel length is verified by investigating different CMOS technologies and expanding on serial and parallel structures. Furthermore, implementing a ring oscillator (RO) shows 95% improvement in operating frequency over regular minimum sized CMOS logic. In addition, a 32-bit carry-look-ahead adder (CLA) demonstrates 50%, 20% and 60% improvements in delay, energy and energy-delay product (EDP) respectively. Nabavi has applied the CoC method to find the optimum channel width for delay improvement of subthreshold circuits for his M.Sc. thesis [27]. Results are verified by simulating a 19-stage RO and 4-bit comparator using the 90 nm CMOS technology showing 26% and 40% speed improvement respectively.

Serial implementation of ultra-low power subthreshold circuits as shown in Figure 9 is explored [28]. By implementing a 32-bit serial adder in the 22 nm technology, the author shows 40% active energy saving, 15x active power and 32x leakage power reduction. This paper shows that one of the significant benefits of serial implementation for subthreshold circuits is significant reduction of sleep mode energy dissipation. This loss accounts for a majority of active energy leakage in ULP applications such as biosensors.

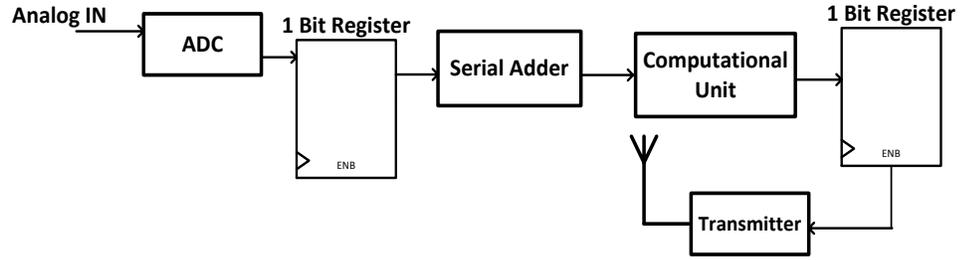


Figure 9 Fully serial implementation of a digital circuit suitable for robust and fast subthreshold design [28].

2.3.3 Decreasing Sensitivities to PVT Variations for Circuits Operating in the Sub-threshold Region

An appropriate choice of device and technology can be done to reduce process variations for subthreshold circuits. Vaddi suggests that double gate silicon-on-insulator (DGSOI) devices show better performance, robustness and PVT variation insensitivity compared to bulk connected CMOS circuits [29]. By implementing a RO in 32 nm technology using DGSOI and bulk subthreshold CMOS circuits, 60-70% improvement in PDP and 50% enhancement of tolerance to PVT variation is demonstrated.

Fuketa introduces an adaptive performance technique using two on-chip variation sensors for robustness enhancement of subthreshold circuits [30]. Figure 10 shows the proposed sensor circuit that controls speed and power dissipation by generating a warning signal, called timing-error predictive (TEP FF). Implementing a subthreshold adder using 65 nm process shows compensation of PVT variations and 46% improvement of power consumption. This approach is a precise way of sensing and cancelling process variations and ensuring high robustness. However, it involves high complexity and cost.

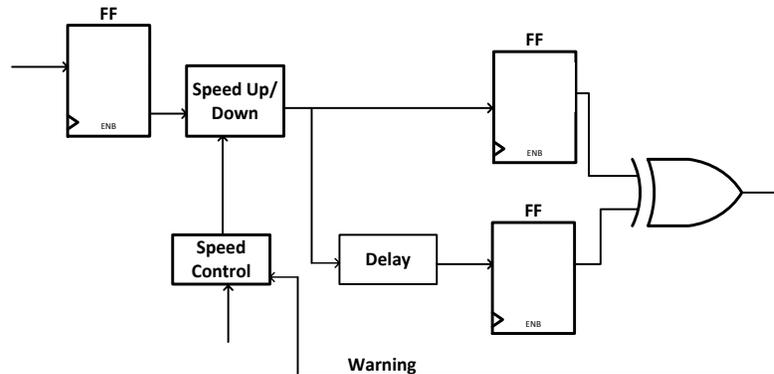


Figure 10 Speed and power dissipation control circuit [30].

Radfar proposes a novel body-biasing method for process and temperature variation compensation as well as dynamic voltage scaling (DVS) for EDP improvement [31]. This method involves designing two body-biasing circuits for NMOS (NBB) and PMOS (PBB) transistors using the 65 nm process as shown in Figure 11. Theoretical analysis for process variation probability is confirmed using post-layout HSPICE simulations for an 8-bit adder. Voltage-scaling from 0.8 V to 0.3 V is applied. Considering temperature changes of -15 to 75°C, 23% of improvement in EDP is demonstrated for the adder compared to the zero-biased design. The body-biasing circuits include three stages: 1) voltage reference generator providing the next stage with a process/temperature-independent V_{gs} proportional to V_{DD} . 2) M_3 is a PVT-dependent transistor, while M_4 is PVT-invariant using large channel length and width. Using appropriate sizing of these transistors, a forward body bias (FBB) is generated at V_{X2} . 3) PVT-independent buffer stage using large inverters. The output of this stage is connected to NMOS/PMOS body.

A number of ambiguities and problems exist with the above design. Firstly, it is not clarified as to how large channel width and length leads to PVT-independency in the subthreshold region. Further simulations in chapter 3 of this thesis work contradict this fact for the 0.13 μm technology. Moreover, M_2 is a low-threshold transistor that can only be implemented using multi-threshold processes, which increases the cost.

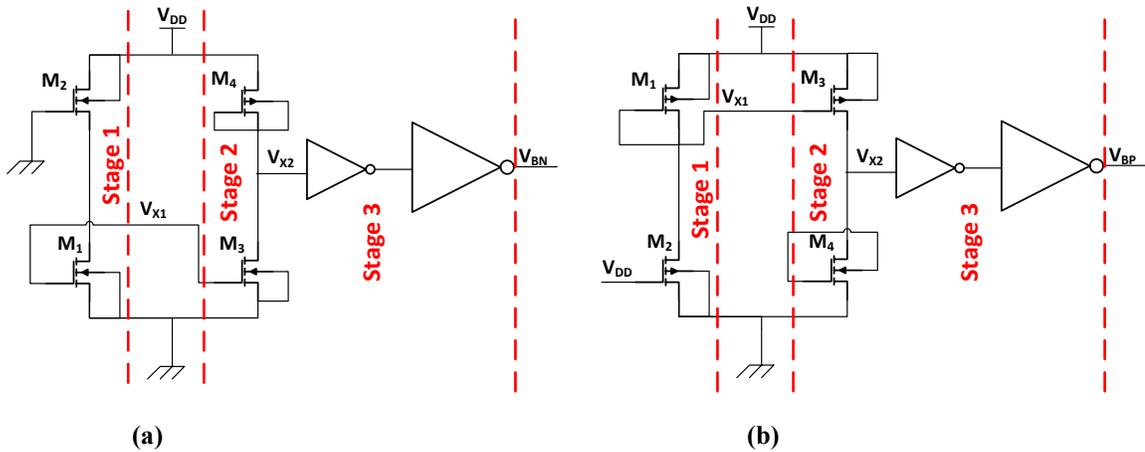


Figure 11 a) NBB b) PBB circuits designed using FBB to enhance robustness and EDP [31].

Another researcher suggests the use of a bootstrapped driver body-biasing technique to enhance the writing cycle of a subthreshold 8-transistor static ram (8T-SRAM) under process variations [32]. Capacitive boosting is also used for subthreshold circuit

interconnects to reduce delay variations due to PVT fluctuations [33]. Ultra-dynamic voltage scaling (UVDS) is used to design a process-tolerant 8x8 finite impulse response (FIR) filter using the 0.13 μm technology [34]. Analytical techniques for modeling the statistical distribution of subthreshold leakage and threshold variations are used to predict sensitivities to process fluctuations [7] [8]. Chang has proposed an asynchronous design method to decrease PVT variations for subthreshold circuits [35].

2.3.4 Additional Circuit Required for Subthreshold Circuit Design

Level shifters are the main additional circuit that needs to be implemented for some subthreshold circuits. However, other extra blocks, such as PVT variation monitoring sensors, might be required for robust operation [30]. A subthreshold circuit cannot drive a superthreshold one as it operates using a much lower supply voltage. Thus, if the output of a subthreshold circuit is connected to a superthreshold one, a level shifter in between the two is essential. Figure 12 shows a dual-supply level shifter (DSL), which is discussed widely in literature for performance enhancement [36].

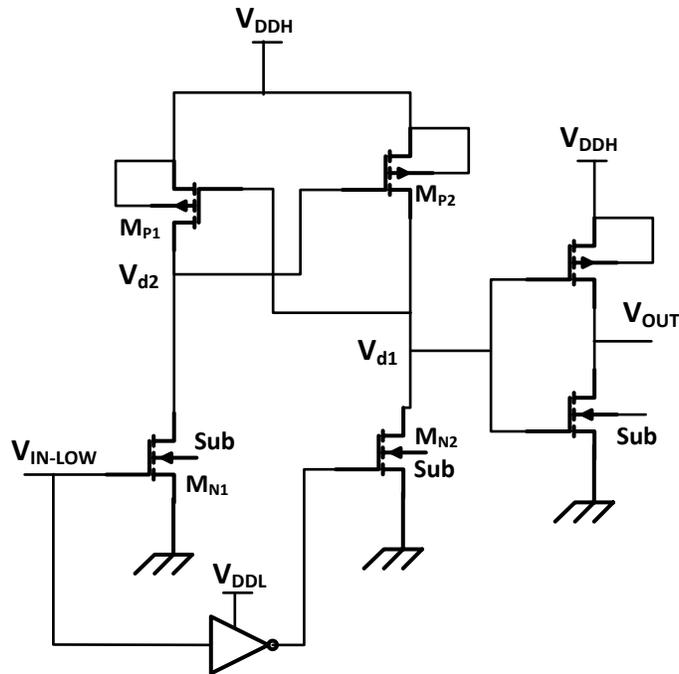


Figure 12 Conventional level shifter [36].

Three novel level shifters, one of which is shown in Figure 13, are introduced using DTMOS logic [36]. The dynamic threshold concept is used to improve the performance and decrease the power consumption of previously designed level shifters. Hasanbegovic suggests a new level shifter structure in 90 nm technology using multi-threshold CMOS (MTCMOS) design techniques [37]. This level shifter, which is shown in Figure 14, operates at a maximum frequency of 1 MHz using a 180 mV supply voltage. Moreover, it has an additional enable/disable feature allowing static power saving. This structure increases the robustness and speed at an expense of higher dynamic power consumption and area. Other techniques, such as using a wide-range Wilson-current mirror hybrid buffer, single supply design, sizing and threshold voltage selection are used for robustness, power and speed enhancement of existing level shifters [38] [39] [40] [41].

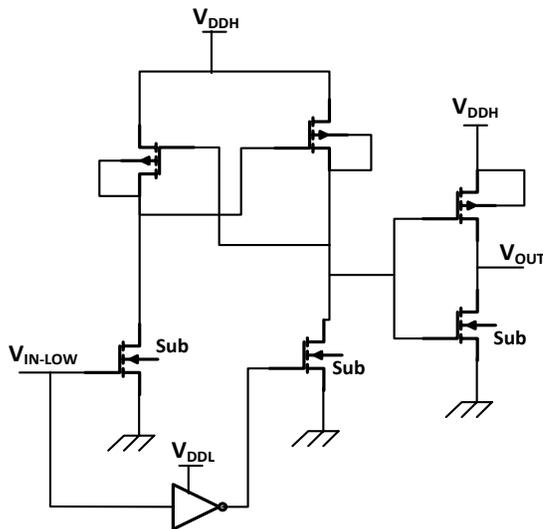


Figure 13 Novel level shifter using DTMOS for the top PMOS devices [36].

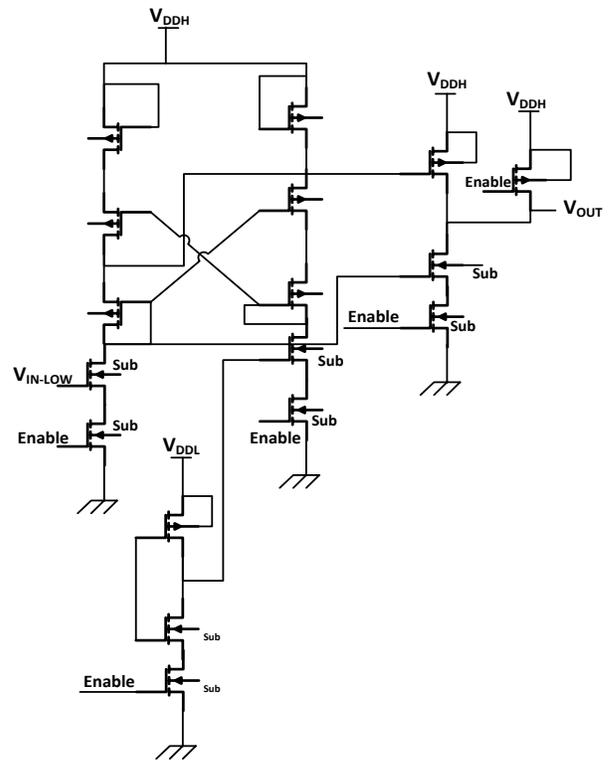


Figure 14 A level shifter using MTCMOS design technique [37].

2.4. Literature Review: Wireless Sensor Signal Processing

Haider suggests a compact ultra-low power signal processing unit for biosensor applications [42]. This SPU consists of a data generator, impulse generator and a buffer for driving a 200 ohms antenna. The block diagram of the proposed SPU is shown in Figure 15. The SPU is implemented in the 0.35 μm technology using a V_{DD} of 700mV and operates in weak inversion region of MOSFET. Consequently, the power consumption has decreased significantly compared to CMOS implementations in the saturation region.

The data generator block shown in Figure 16 contains an implanted sensor and converts the sensed current to a pulse train. This block consists of a voltage-controlled ring oscillator, whose frequency is governed by the sensed current. Furthermore, the impulse generator block of Figure 17 transforms the resulting pulses to narrow-pulse-width impulse signals. The impulse generator is added as the sensed signal needs to be transmitted outside the biological environment. The buffer simply drives the antenna load. Power consumption of the data generator block for different sensor current values are shown in Table 3. The data generator consumes a maximum power of 1.79 μW . The SPU consumes a maximum power of 649 μW . The major problem with this design is robustness. The SPU's sensitivity to process variations, which could cause an undesirable change in the output frequency, is not addressed. Robustness enhancements are completed as part of this thesis work to design a robust, ULP signal processing unit.

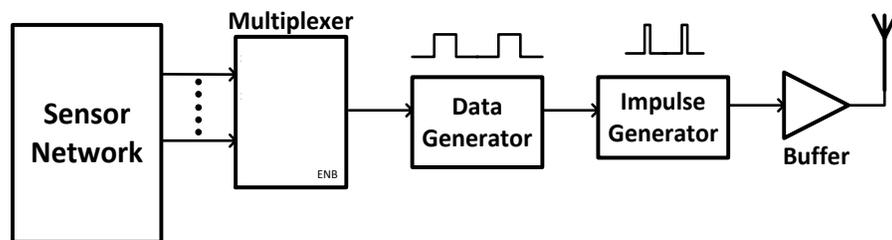


Figure 15 Block diagram of a signal processing unit [42].

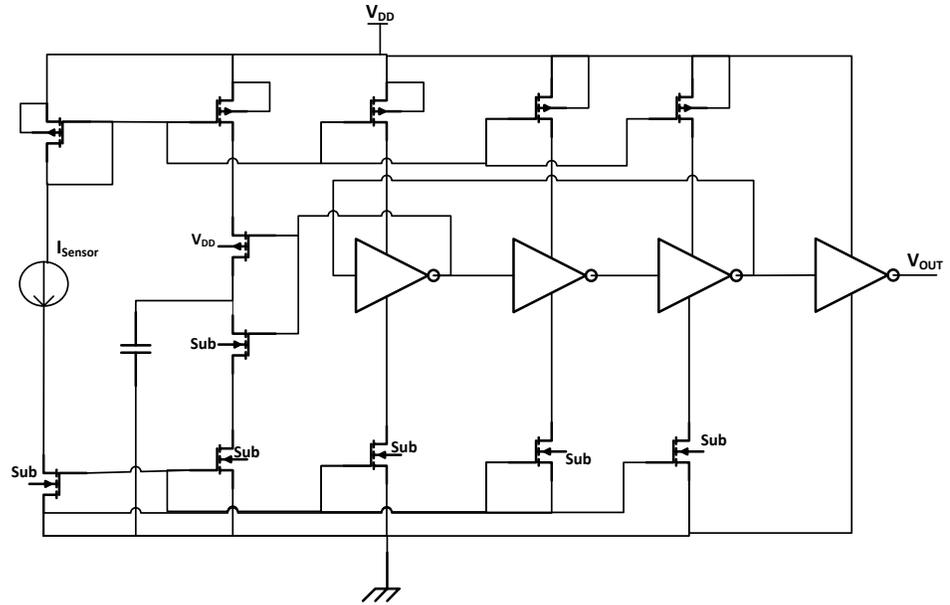


Figure 16 Data generator block [42].

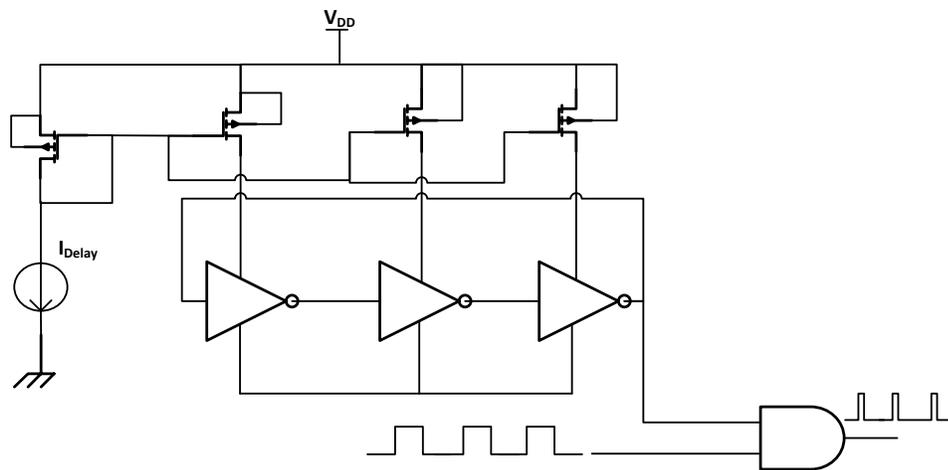


Figure 17 Impulse generator block [42].

Table 3 Power consumption of a proposed signal processing unit's data generator block [42].

Sensor Current (μA)	Output Data Frequency (KHz)	Power (μW)
0.01	1.65	0.11
0.05	5.99	0.13
0.1	10.1	0.18
0.2	18.28	0.31
0.3	25.75	0.43
0.4	32.85	0.48
0.8	51.63	0.92
1	60.28	1.79

Teo introduces an ULP sensor node for wireless health monitoring system using the 0.18 μm CMOS technology [43]. The SPU part consists of an amplifier (AMP), analog to digital converter (ADC) and a digital signal processing (DSP) block. The SPU as well as the RF interface are turned ON or OFF using a control unit for minimum power consumption. Ultra-low power RF analog signal processing has also been used in sensor platforms [44]. Cai suggests a compact one-bit serial processing CPU architecture using the coordinate rotation digital computer (CORDIC) algorithm for sensor signal processing applications [45]. This general purpose CPU is designed to implement basic logical and arithmetic functions. Another author has proposed an ULP subthreshold sensor processor with an energy dissipation of 2.6 pJ/Inst [46]. The processor consists of a complex instruction set computing (CISC) micro-architecture to cancel process variations in subthreshold operation. This micro-architecture contains an 8-bit arithmetic logic unit (ALU), 32-bit accumulator, a unified instruction and data memory.

2.5. Summary

MOSFET theory and operation in the subthreshold region were analyzed in this chapter. Furthermore, the benefits and challenges of CMOS subthreshold circuits were explored. Minimum leakage, static and dynamic power consumption are the major benefits of subthreshold circuit design. However, they do suffer from low speed, high sensitivity to PVT variations and potential need for additional circuitry. Recent solutions for these problems were investigated in the literature. There are few circuit solutions for decreasing subthreshold current sensitivity to process variations. These circuits are either involved with high complexity and energy consumption or are intended for digital gates. Hence, an efficient circuit design technique for improving the robustness of MOSFETs operating in subthreshold for analog applications remains as a gap. Moreover, a paper survey on wireless sensor signal processing, was completed. Therefore, the first thesis objective is achieved. Using the presented background knowledge, a robust and ultra-low power SPU is designed in the following chapters for wireless dosimeter applications.

Chapter 3. MOSFET Operation in the Subthreshold Region using the 0.13 μm CMOS Technology

MOSFET behavior in the subthreshold region needs to be carefully analyzed using simulations before designing the ultra-low power SPU. For this purpose, this chapter is divided into two main sections. The first part examines the threshold characteristics of transistors for different body bias configurations. The second section investigates current behavior of MOSFETs in the subthreshold region for the same structures. Both threshold and current characteristics are investigated for different process corners. All simulations in this thesis are completed using Cadence Virtuoso 6 and the 0.13 μm IBM CMOS technology. Moreover, these simulations are completed using the typical-typical (TT) process corner, unless mentioned otherwise.

3.1. MOSFET Threshold Behavior in the Subthreshold Region using 0.13 μm Technology

The nominal supply voltage for MOSFETs using the 0.13 μm IBM CMOS technology to operate in saturation is 1.2 V. In order to extract device characteristics in subthreshold region, the maximum V_{DD} value for subthreshold operation is required. Simulations show that V_{th0} is about 341.6 mV and 369.8 mV for minimum size NMOS and PMOS devices respectively. Thus, $V_{DD}=300$ mV is chosen as the maximum subthreshold supply voltage. The subthreshold and supethreshold supply voltages are 300 mV and 1.2 V respectively for all simulations in this chapter, unless mentioned otherwise.

3.1.1 MOSFET Body-Bias Configurations

There are four main types of body connections that can be used for NMOS and PMOS devices operating in the subthreshold region as shown in Figure 18:

1. Body is connected to the substrate for NMOS and V_{DD} for PMOS. (conventional body bias - CBB)
2. Body is connected to V_{DD} for NMOS and ground for PMOS. (swapped body bias - SBB)
3. Body is connected to the gate. (dynamic threshold - DTMOS)
4. Body is connected to a body-biasing circuit that generates a voltage. If the voltage is fixed, we refer to it as static body-biasing (ST-BB). If the voltage changes depending on process variations to enhance robustness, dynamic body-biasing (DBB) is used to represent the technique.

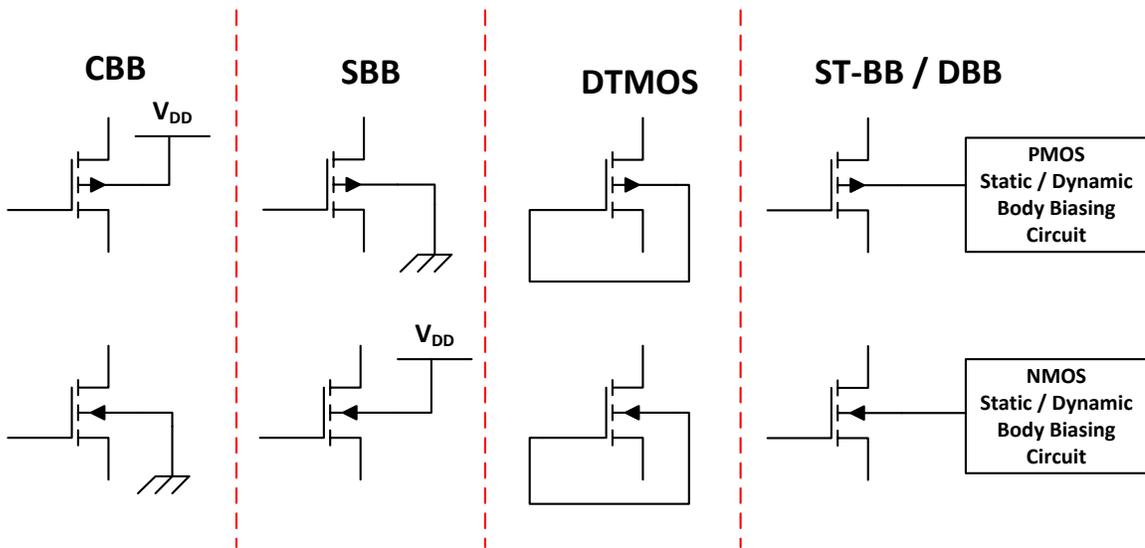


Figure 18 CBB, SBB, DTMOS and ST-BB / DBB NMOS and PMOS body-biasing configurations.

With the exception of the last type, which is discussed in Chapter 6, the other configurations will be analyzed for robustness, power consumption and speed in this section. In addition to the above structures, some transistors use body-source or body-drain connections when a series of devices are connected in a stack. However, these structures are not analyzed in this chapter, as serial stacks are not relevant to the topic of this thesis and the SPU application. If any configuration other than the 1st one is used, triple-well process is required for NMOS implementation. This can lead to extra cost and chip space.

3.1.2 MOSFET V_{th} vs. V_{bs} , V_{th} vs. V_{ds} Characteristics in the Subthreshold Region

Figure 19 shows the test benches used to obtain the threshold vs. body-source voltage characteristics for NMOS and PMOS devices. Tripple-well NMOS transistor is used for

all simulations where the NMOS body is not connected to the substrate. Minimum size transistors are used for the DC simulation used to extract these characteristics. Setting $|V_{gs}| = |V_{ds}| = 300$ mV and sweeping the body voltage from 0-300 mV, the plots of Figure 20 are obtained. As it was expected according to equation (2-10), a linear relationship exists between V_{th} and V_{bs} . The slope of this line is the λ_{bs} coefficient. Using the graphs of Figure 20, λ_{bs} is obtained as about -0.17 for NMOS and 0.18 for PMOS.

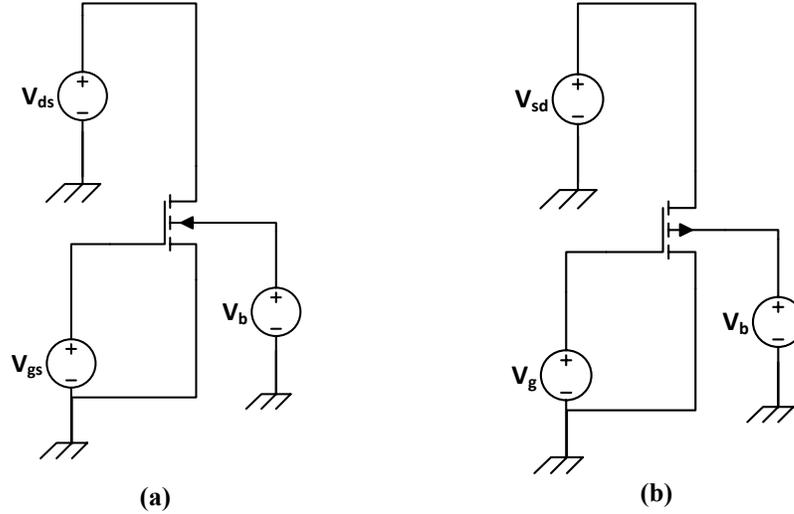


Figure 19 DC characteristic test bench for a) NMOS b) PMOS.

The V_{th} vs. V_{bs} plots reveal important information regarding different body-bias configurations. For NMOS transistors, threshold voltage decreases as V_{bs} increases. Thus, the fastest configuration is SBB, where the NMOS body is connected to V_{DD} . DTMOS reaches the same speed as SBB when switching occurs and V_{gs} reaches the supply voltage.

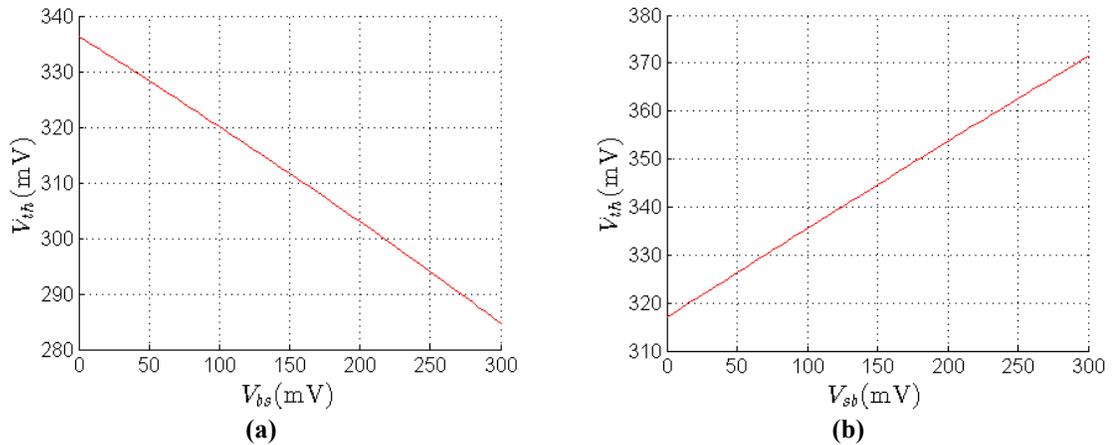


Figure 20 V_{th} vs. V_{bs} for a) NMOS b) PMOS. $|V_{gs}|=|V_{ds}|=300$ mV, $W=160$ nm, $L=120$ nm.

The relationship between drain-source and threshold voltages is also important. To have a comparison between different body-bias structures, the gate and drain of transistors are connected. Since the threshold voltage is independent of V_{gs} , this will not affect the V_{th} vs. V_{ds} relationship. The test benches used for this simulation are shown in Figure 21. For the CBB structure, $V_b = 0$ is used, while for the SBB configuration body voltage is set to 300 mV. For the DTMOS structure, the V_b test voltage is removed and the gate is connected to the drain. The source voltage is set to 0 and V_{DD} for the NMOS and PMOS transistors respectively. Sweeping the drain voltage from 0-300 mV, the plots of Figure 22 are obtained.

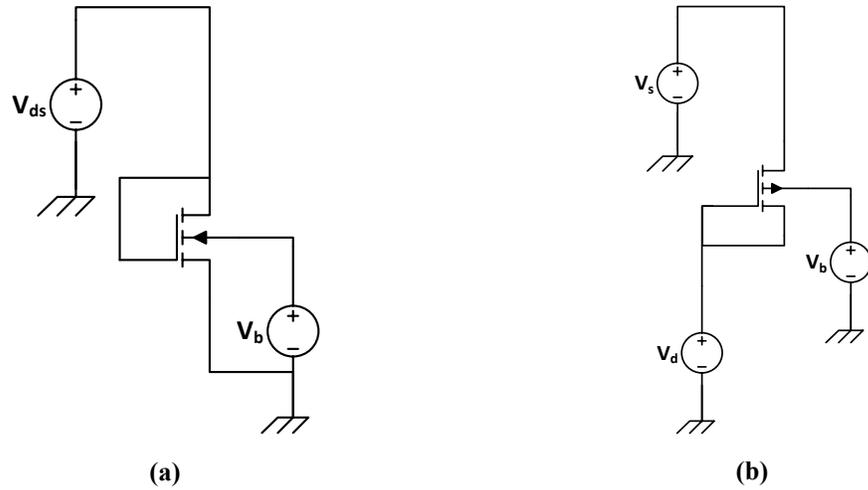


Figure 21 V_{th} vs. V_d test bench for a) NMOS b) PMOS.

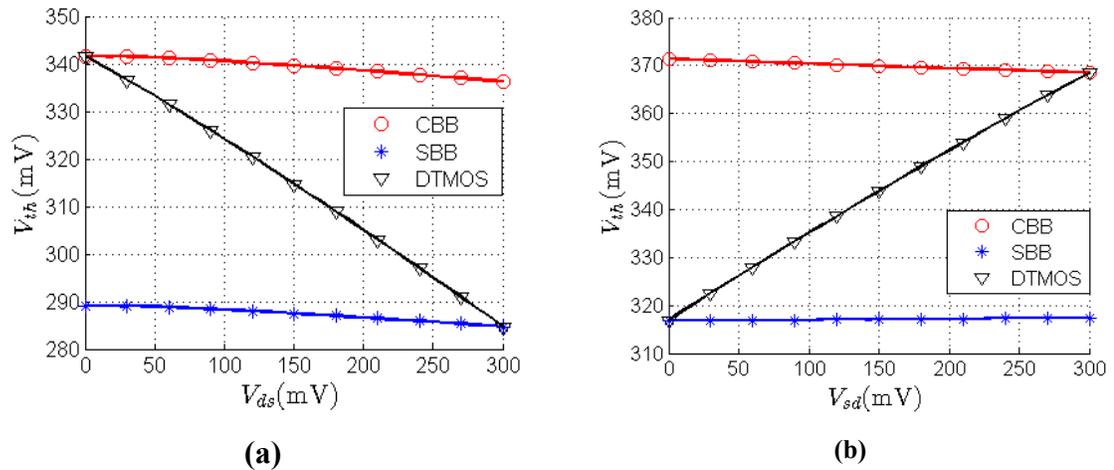


Figure 22 V_{th} vs. V_{ds} for CBB, SBB, DTMOS configurations of a) NMOS b) PMOS. $W=160$ nm, $L=120$ nm.

As it can be seen in the above plots, the threshold does not change significantly in response to changes in V_{ds} for the CBB and SBB structures. However, it changes linearly for the DTMOS configuration, resulting in higher sensitivity to voltage variations. The slope of this line, λ_{ds} , is about -0.19 for DTNMOS and 0.17 for DTPMOS. However, DTMOS configurations consume lower static power, as they have a higher threshold compared to SBB transistors during idle mode.

3.1.3 MOSFET V_{th} vs. W , V_{th} vs. L Characteristics in the Subthreshold Region

The threshold voltage depends on the channel width and length for all MOSFET operating regions. First, the relationship between V_{th} and W using minimum L is investigated in the subthreshold region. Next, the V_{th} vs. L plots are produced using minimum channel width. The test bench of Figure 19 is used for this purpose. Figure 23 and Figure 24 show the threshold relationship with channel width and length for CBB and SBB configurations. Since $|V_{gs}|$ and $|V_{ds}|$ are set to 300 mV, DTMOS structure is not included. However, SBB configuration for this simulation is equivalent to a DTMOS transistor when fully ON.

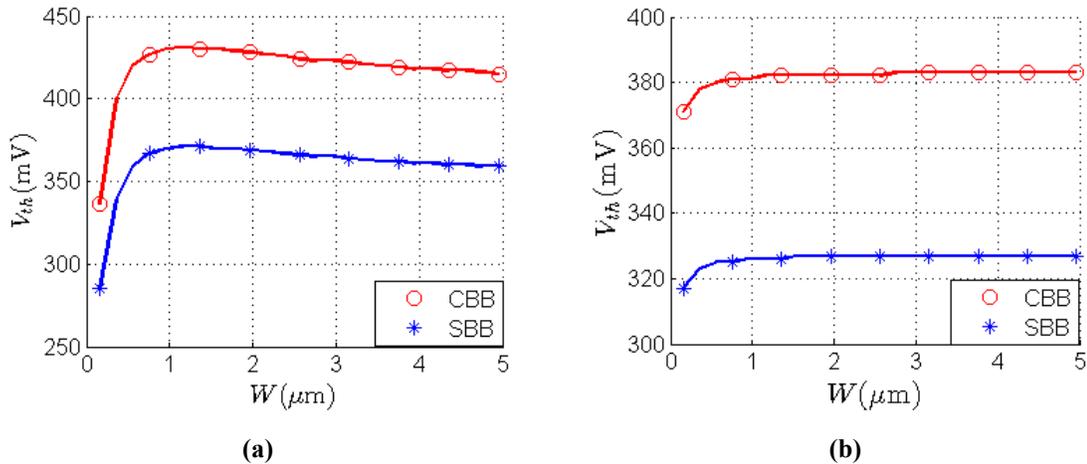


Figure 23 V_{th} vs. W for CBB and SBB configurations of a) NMOS b) PMOS, $|V_{gs}|=|V_{ds}|=300$ mV, $L=120$ nm.

As shown in Figure 23, V_{th} increases rapidly between channel widths of 160 nm-1 μm for NMOS transistors due to the INWE [26]. For larger channel widths, the threshold has a linearly decreasing trend with a small slope. For PMOS, the threshold has a slight increase from minimum channel width to W of about 500 nm. For larger values of W , the

threshold remains constant. For both NMOS and PMOS transistors, V_{th} decreases exponentially as L increases. However, the threshold drop is larger when the channel length increases slightly from 120 nm to 220 nm. This happens due to the reverse short channel effect (RSCE) [26]. The above trends are the same for CBB and SBB configurations of NMOS and PMOS transistors. However, the threshold is lower for every respective channel width or length using SBB structures as expected.

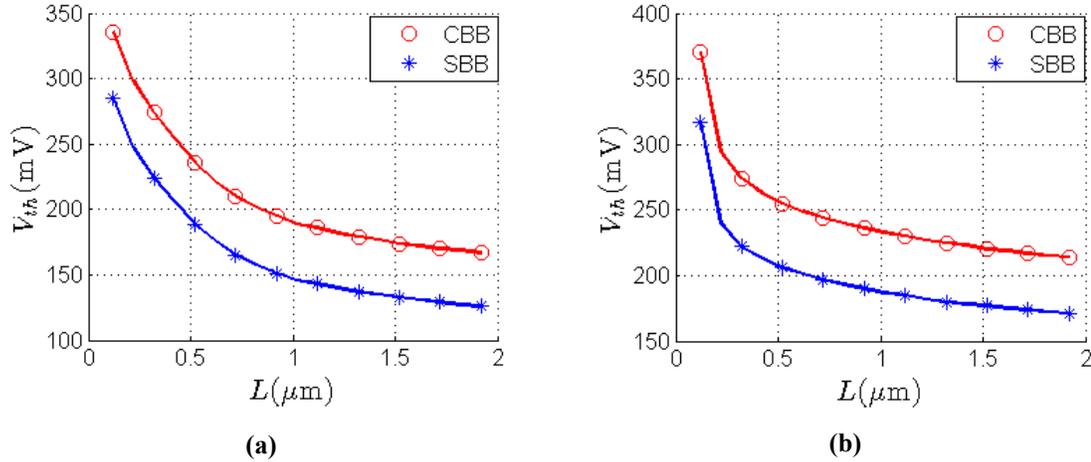


Figure 24 V_{th} vs. L for CBB and SBB configurations of a) NMOS b) PMOS, $|V_{gs}|=|V_{ds}|=300$ mV, $W=160$ nm.

3.1.4 MOSFET Threshold Sensitivity to Process Variations in the Subthreshold Region

In order to investigate different body-bias structures for robustness, the threshold variations in response to process fluctuations needs to be analyzed. In Cadence, there are four process corners in addition to TT used for the simulations of the previous sections; FF, SS, FS and SF process corners refer to: fast NMOS / fast PMOS, slow NMOS / slow PMOS, fast NMOS / slow PMOS and slow NMOS / fast PMOS respectively. Figure 25 shows the threshold vs. body voltage of minimum sized NMOS and PMOS devices using different process corners. Since only one type of transistor is used for each simulation, either FF or FS and SF or SS can be used for NMOS. Similarly, FF and SF as well SS and FS can be exchanged for PMOS simulations. For single transistors, typical, fast and slow are denoted using T, F and S. The plots of Figure 25 demonstrate an interesting result. The λ_{b_s} coefficient remains almost constant for all process corners. Thus, the body

voltage affects the transistor's threshold voltage (i.e. current) equally and independent of process variations. This result can be used to stabilize the transistor's threshold using a proper dynamic body-biasing structure. Moreover, these plots show that the threshold voltage can vary greatly due to process variations. For example, for a minimum size NMOS using a body voltage of 0, λ_{bs} can change from 270 – 369 mV. For minimum size PMOS, the changes are even greater with a range of 247 – 362 mV. This can in turn cause a significant drift in the MOSFET current.

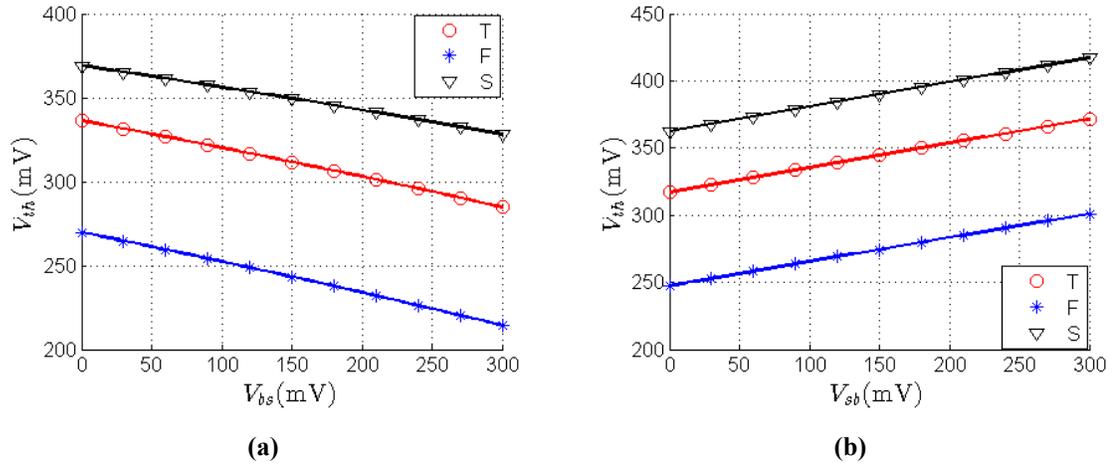


Figure 25 V_{th} vs. V_{bs} for different process corners for a) NMOS b) PMOS. $|V_{gs}|=|V_{ds}|=300$ mV, $W=160$ nm, $L=120$ nm.

Figure 26 and Figure 27 show the threshold vs. channel width for CBB and SBB NMOS and PMOS configurations for different process corners. Looking at these plots, the maximum threshold variations for CBB and SBB NMOS are 120 mV and 119 mV respectively. Similarly, the maximum change in V_{th} for CBB and SBB PMOS are 116 mV and 115 mV. Therefore, SBB and CBB configurations almost yield equal threshold sensitivity to process variations for minimum channel length devices. Furthermore, it can be noticed that for all configurations, variations start to decrease for channel widths greater than 2 μm . However, the changes in threshold due to process fluctuations are never fully cancelled. The curves corresponding to different process corners will be almost parallel after a certain large channel width, thus yielding a constant threshold variation. The minimum change in threshold for CBB and SBB configurations of NMOS and PMOS transistors were obtained as 55.4, 55.3, 37 and 34.4 mV respectively using $W=5$

μm . Since V_g had to be set similar to V_{th} vs. W plots in the previous sections, DTMOS was analyzed when fully ON (equivalent to SBB) using $V_{gs} = V_{ds} = 300 \text{ mV}$.

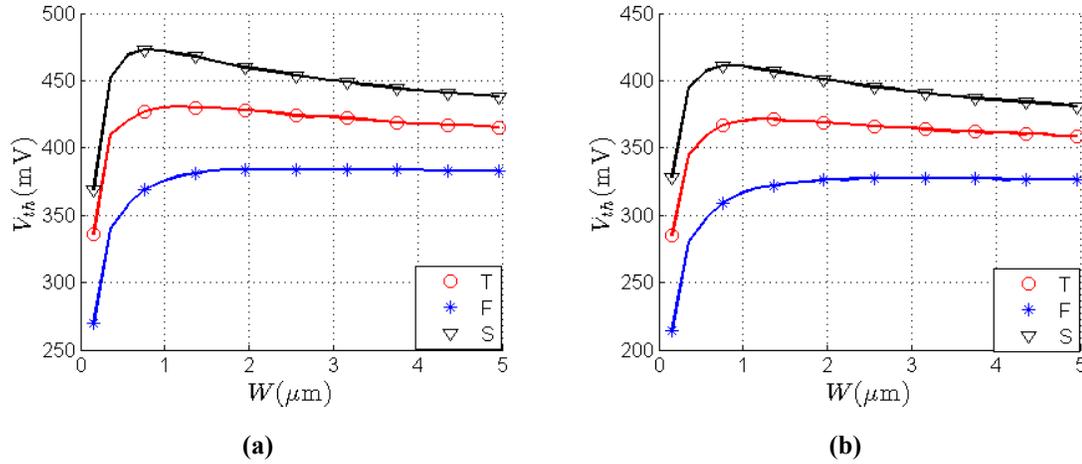


Figure 26 V_{th} vs. W using T,F,S process corners for an NMOS in a) CBB b) SBB configuration. $V_{gs} = V_{ds} = 300 \text{ mV}$, $L = 120 \text{ nm}$.

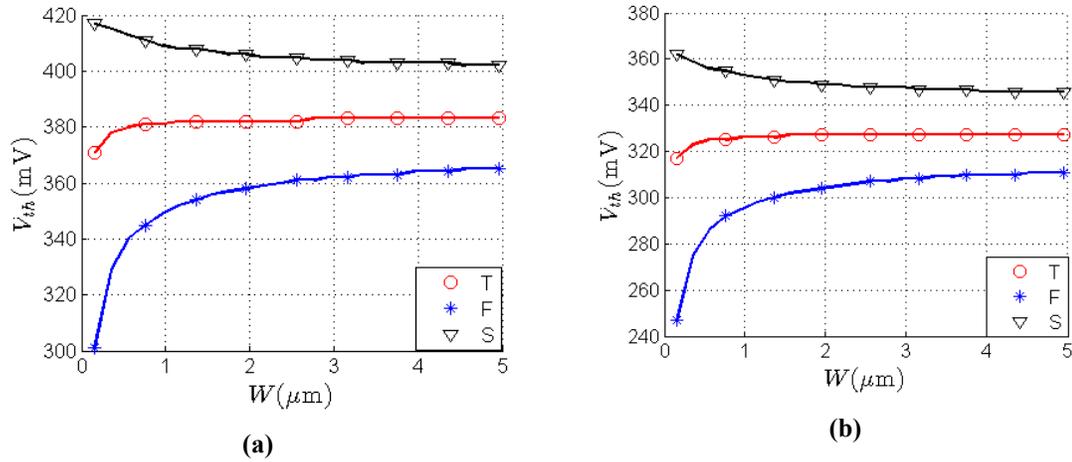


Figure 27 V_{th} vs. W using T,F,S process corners for a PMOS in a) CBB b) SBB configuration. $|V_{gs}| = |V_{ds}| = 300 \text{ mV}$, $L = 120 \text{ nm}$.

Similar plots are produced for V_{th} vs. different channel lengths using minimum W as presented in Figure 28 and Figure 29. These plots show that for NMOS, channel lengths greater than 1 μm results in much less variations in threshold. Similarly, channel length values greater than about 300 nm show smaller threshold variation for PMOS devices.

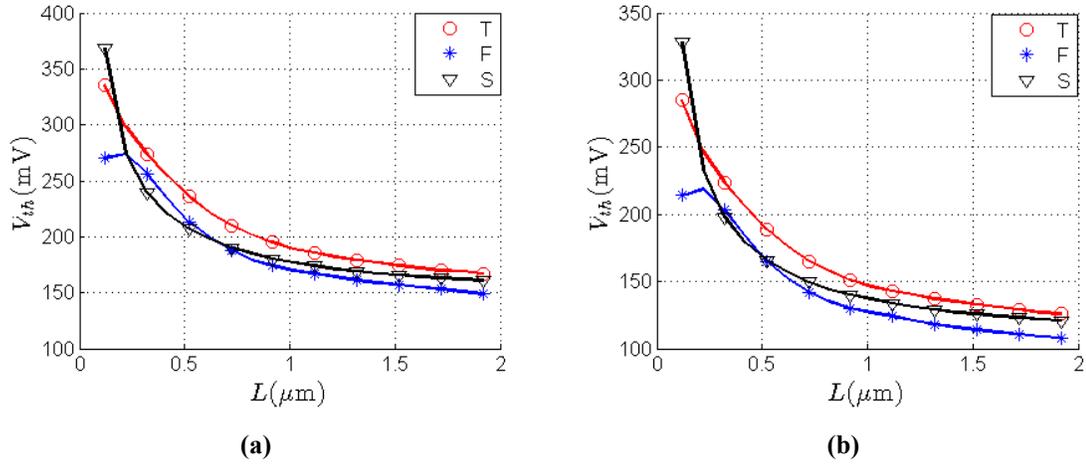


Figure 28 V_{th} vs. L using T,F,S process corners for an NMOS in a) CBB b) SBB configuration. $V_{gs}=V_{ds}=300\text{ mV}$, $W=160\text{ nm}$.

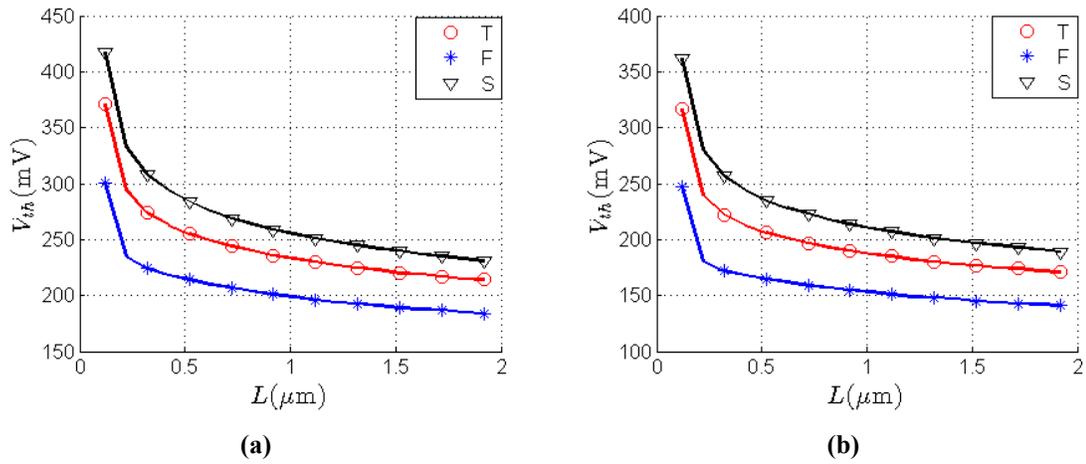


Figure 29 V_{th} vs. L using T,F,S process corners for a PMOS in a) CBB b) SBB configuration. $|V_{gs}|=|V_{ds}|=300\text{ mV}$, $W=160\text{ nm}$.

The maximum variations in threshold for CBB and SBB structures of NMOS are 11.1 mV and 13.1 mV respectively. For PMOS transistors, CBB yields a maximum of 56.4 mV and SBB results in 57.2 mV change in threshold voltage. Therefore, CBB is slightly less sensitive to process variations in terms of threshold voltage. Moreover, comparing these minimum variation values with those of previous simulations for different channel widths, great improvement can be observed for NMOS. Increasing the channel length of NMOS in oppose to its channel width results in about 5 times less threshold sensitivity to process variations. For the PMOS transistor however, increasing the channel width results in slightly better performance in this regard.

3.2. MOSFET Current Behavior in the Subthreshold Region using 0.13 μm Technology

3.2.1 MOSFET I_{ds} vs. V_{bs} , I_{ds} vs. V_{gs} Characteristics in the Subthreshold Region

The test benches of Figure 19 are used to obtain the MOSFET current relationship with gate-source and bulk-source voltages in the subthreshold region. Minimum size transistors are used for both simulations. Figure 30 shows the resulting I_{ds} vs. V_{bs} curves. These plots are important, as they represent the subthreshold current's correlation with the threshold. Since V_{th} has a linear relationship with V_{bs} , it can be concluded that a relationship similar to the ones of Figure 30 exists between I_{ds} and V_{th} . These plots show that the current has a semi-exponential relationship with the body-source voltage. The correlation between the two is steeper than linear, yet not exponential. Consequently, the body bias greatly affects a transistor's strength when operating in the subthreshold region.

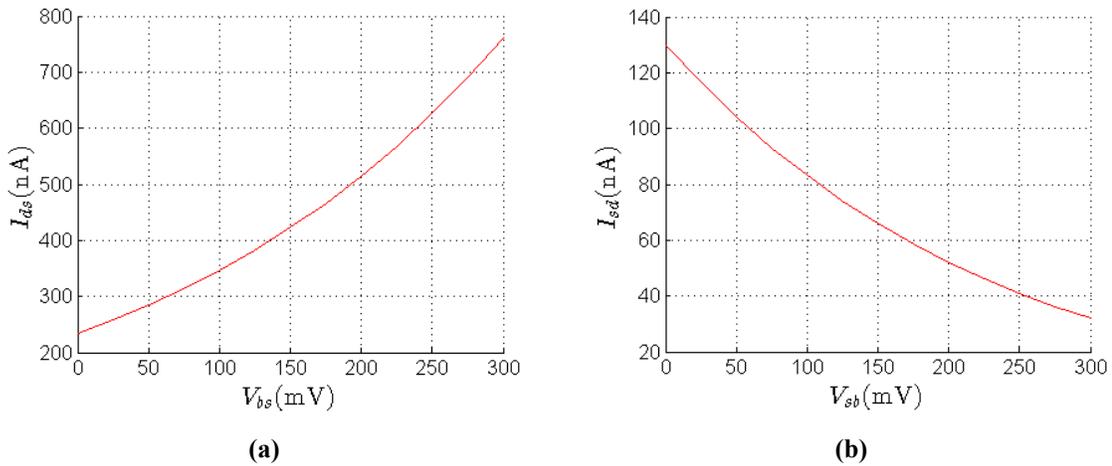


Figure 30 I_{ds} vs. V_{bs} for a) NMOS b) PMOS. $|V_{ds}| = |V_{gs}| = 300$ mV, $W = 160$ nm, $L = 120$ nm.

Figure 31 shows the I_{ds} vs. V_{gs} plots for CBB, SBB and DTOMOS configurations of NMOS and PMOS transistors. These plots show that the SBB structure has the highest speed as it yields the largest current for different gate-source voltages. However, the SBB and DTOMOS configurations almost yield the same current for $|V_{gs}| > 250$ mV. Therefore, they almost have equal strengths when the transistor starts to turn ON. However, since DTOMOS has less current for smaller gate-source voltage values, it involves less static power consumption compared to SBB.

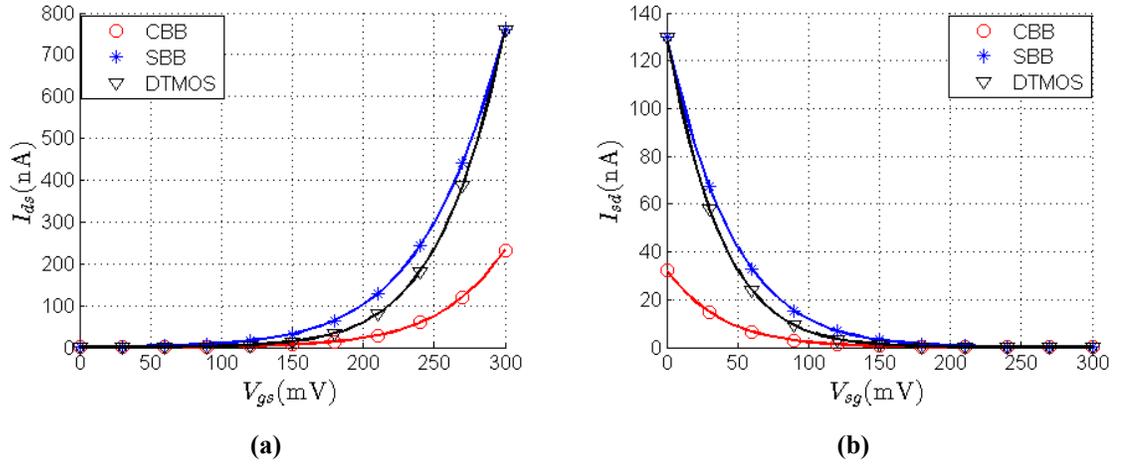


Figure 31 I_{ds} vs. V_{gs} for CBB, SBB, DTMOS configurations of a) NMOS b) PMOS. $|V_{ds}|=300$ mV, $W=160$ nm, $L=120$ nm.

3.2.2 MOSFET I_{ds} vs. W , I_{ds} vs. L Characteristics in the Subthreshold Region

The same test benches as the previous section can be used to obtain the subthreshold current's relationship with channel width and length. Figure 32 shows the I_{ds} vs. W plots for the CBB and SBB configurations of NMOS and PMOS transistors.

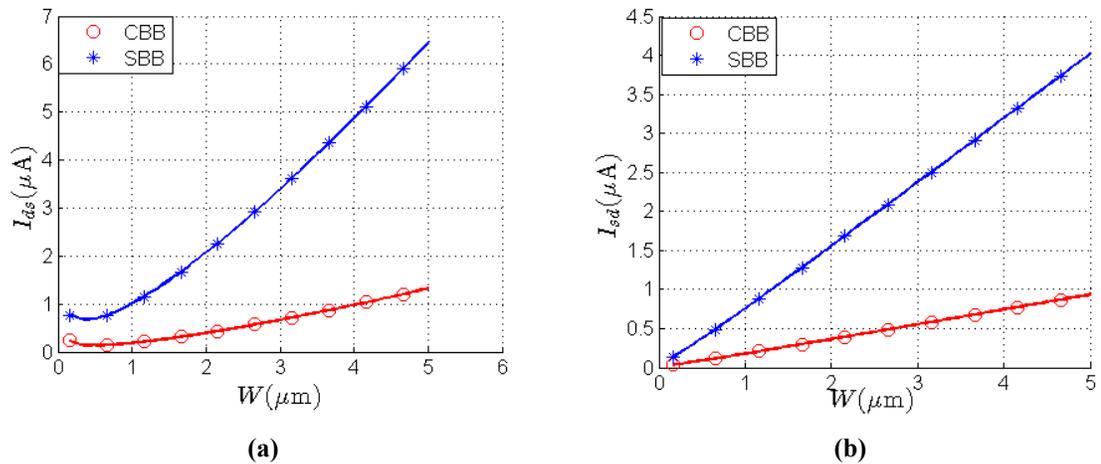


Figure 32 I_{ds} vs. W for CBB, SBB configurations of a) NMOS b) PMOS. $|V_{ds}|=|V_{gs}|=300$ mV.

Figure 33 presents the I_{ds} vs. W plots for the same structures used for current vs. channel width simulations. For both plots, gate-source and drain-source voltages are set to 300 mV.

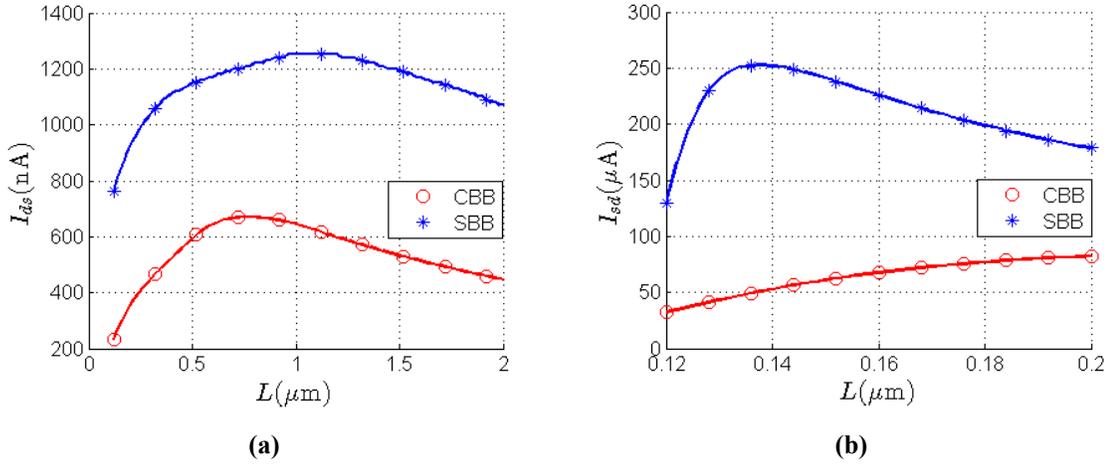


Figure 33 I_{ds} vs. L for CBB, SBB configurations of a) NMOS b) PMOS. $|V_{ds}| = |V_{gs}| = 300 \text{ mV}$.

The NMOS plots show that the subthreshold current for both CBB and SBB configurations does not follow equation (2-1) for all channel widths and lengths. Depending on the body-bias structure, I_{ds} forms a “valley” for a channel width range of about 160 nm – 1 μm for NMOS. This is due to the INWE as observed in 3.1.3 for NMOS transistors. Furthermore, the NMOS current plot shows a “hill” for a range of channel lengths. This behavior occurs as a result of the RSCE as investigated previously in 3.1.3 for NMOS devices. PMOS plots do not follow the trend for various channel widths regardless of the body-biasing method. However, they have a similar I_{ds} vs L plot for the CBB configuration. Both devices have an optimum channel length and width in terms of delay. For example, a CBB NMOS with a channel length of 1 μm produces more current than one using minimum L . Moreover, a minimum size SBB NMOS produces more current than one using the same body bias configuration, but a larger channel width of 500 nm. However, the main design criteria for the wireless dosimeter are power consumption and robustness, rather than speed.

3.2.3 MOSFET Current Sensitivity to Process Variations in the Subthreshold Region

Changes in MOSFET threshold due to process variations were investigated in 3.1.4. These variations also affect the transistors current. The subthreshold current sensitivity to process variations should be examined for different transistor sizing, body-bias structures and supply voltages. Using these observations, W , L and V_{DD} as well as body-biasing

scheme can be selected for operational robustness of the VCFS in the subthreshold region.

The current vs. channel width and length plots of 3.2.2 are re-produced for different process corners using the same settings and structures. The results are shown in the plots of Figure 34 to Figure 37. As it is clear in these plots, SBB configurations show less current sensitivity to process variations. In other words, as the body voltage of the transistor increases, it becomes more robust with regards to process fluctuations. Furthermore, it is clear that larger transistor lengths show great improvement in robustness for all structures. Therefore, to decrease sensitivity to process variations, the channel should be increased instead of the channel width.

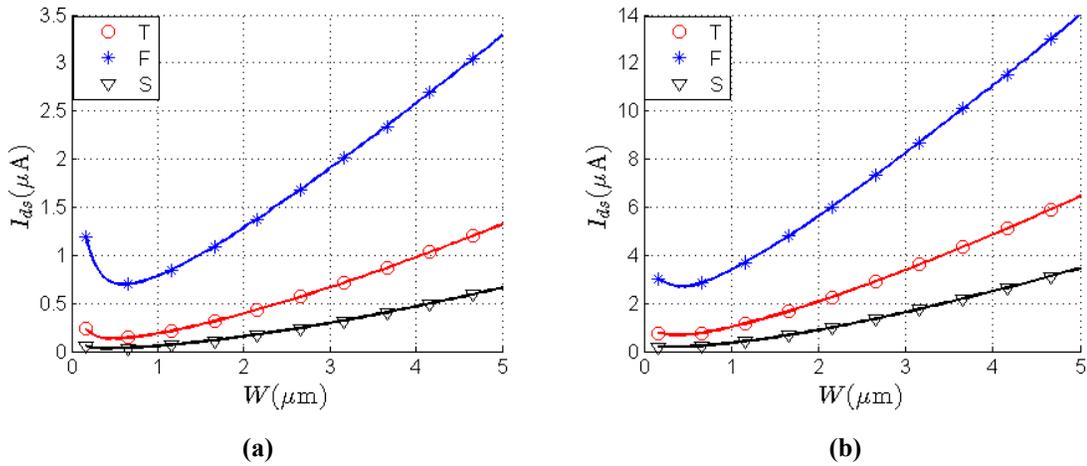


Figure 34 I_{ds} vs. W using T,F,S process corners for an NMOS in a) CBB b) SBB configuration. $V_{gs}=V_{ds}=300\text{ mV}$, $L=120\text{ nm}$.

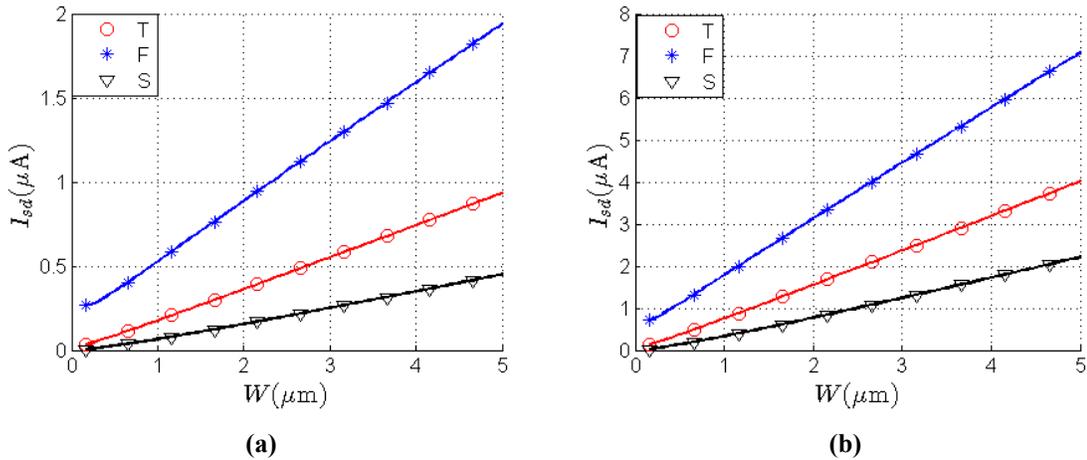


Figure 35 I_{sd} vs. W using T,F,S process corners for a PMOS in a) CBB b) SBB configuration. $|V_{gs}|=|V_{ds}|=300\text{ mV}$, $L=120\text{ nm}$.

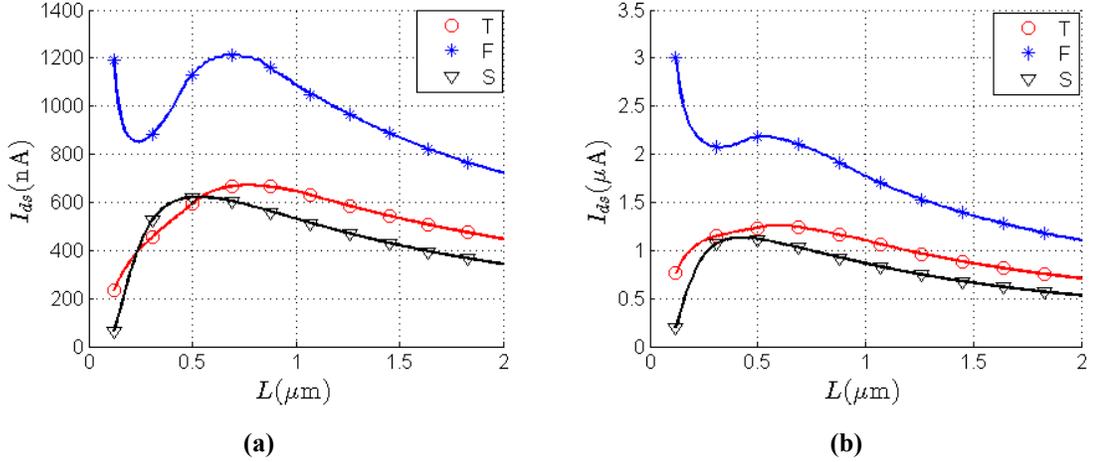


Figure 36 I_{ds} vs. L using T,F,S process corners for an NMOS in a) CBB b) SBB configuration. $V_{gs}=V_{ds}=300\text{ mV}$, $W=160\text{ nm}$.

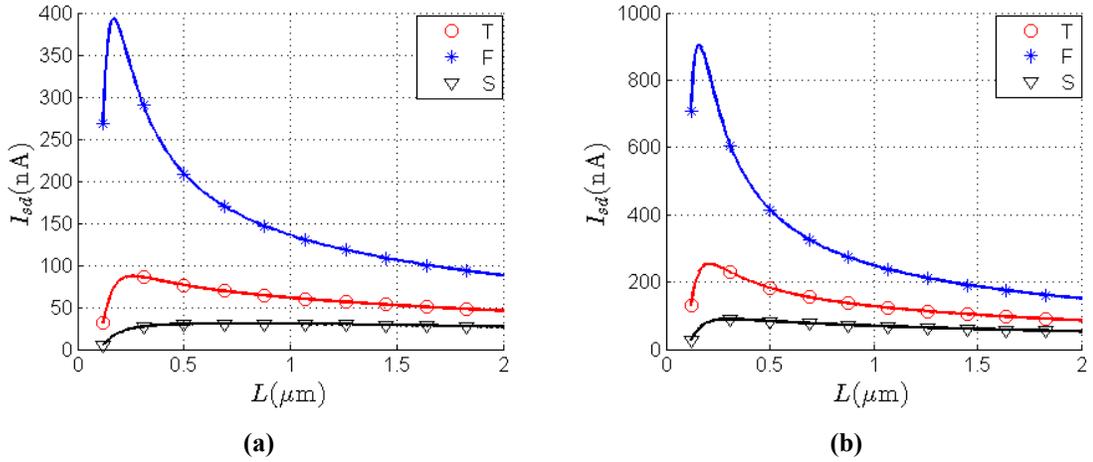


Figure 37 I_{sd} vs. L using T,F,S process corners for a PMOS in a) CBB b) SBB configuration. $|V_{gs}|=|V_{ds}|=300\text{ mV}$, $L=160\text{ nm}$.

The subthreshold supply voltage has to be selected for minimum sensitivity to process variations. Therefore, the I_{ds} vs. L and I_{ds} vs. W characteristic simulations are repeated for V_{DD} values of 250 mV, 200 mV and 150 mV for NBB devices. The current values for the following transistor sizes are recorded:

1. Channel widths of 160 nm, 500 nm, 1 μm , 2 μm and 4 μm , all using minimum L of 120 nm. These channel widths are significant since for CBB structures using T process corner: 160 nm is the minimum width, 500 nm yields minimum current for NMOS and the other two show behavior of larger widths for robustness. The plots show that channel widths larger than 4 μm almost yield the same current sensitivity for all test cases.

2. Channel lengths of 240 nm, 640 nm, 1 μm and 2 μm , all using minimum W of 160 nm. These channel lengths are significant, since for CBB structures using T process corner: 240 nm yields the maximum current for PMOS and 640 nm yields the maximum current for NMOS. The data corresponding to minimum channel length and width is already included in 1. Thus, 120 nm is omitted here. Current's sensitivity to process variations does not decrease significantly for channel lengths greater than 2 μm . Moreover, larger channel lengths greatly decrease the current. Thus, using larger channel lengths forces us to use channel widths greater than 4 μm for the VCFS. This results in power consumption overhead and is not suitable for the VCFS circuit.

The results for the simulations using the above parameters are recorded in Table 4 and Table 5. The shaded region denoted by "Maximum Variation" contains important information for these tables. The data in this column is calculated by dividing the maximum current in each row for a specific device (using certain W , L and V_{DD}) by the minimum. The ideal value for this parameter is 1 when current sensitivity to process variations is zero.

Table 4 CBB transistor's subthreshold current at T,F,S process corners for different values of W and V_{DD} using minimum W , $|V_{ds}|=|V_{gs}|$. The shaded column shows increased sensitivity for smaller channel widths with regards to both NMOS and PMOS.

W ($L=120$ nm)	I_{ds} (nA)						Max. Variation $\frac{I_{ds-max}}{I_{ds-min}}$	
	$V_{DD} = 300$ mV							
	T		F		S		NMOS	PMOS
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS		
160 nm	233	32.2	1190	268	61.9	5.56	19.22	48.20
500 nm	133	89.2	706	352	32.3	27.2	21.86	12.94
1 μm	187	179	787	530	57.5	66.4	13.69	7.98
2 μm	395	365	1290	889	155	156	8.32	5.70
4 μm	981	745	2580	1590	468	350	5.51	4.54
	$V_{DD} = 250$ mV							
	T		F		S		NMOS	PMOS
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS		
160 nm	71.4	8.23	448	85.9	17.7	1.37	25.31	62.70

500 nm	34.8	22.3	198	96.8	8.39	6.59	23.60	14.69
1 μm	47.1	44.4	205	140	14.5	16.1	14.14	8.70
2 μm	97.9	90.4	326	230	38.5	37.8	8.47	6.08
4 μm	241	184	645	406	162	85.2	3.98	4.77
	$V_{DD} = 200 \text{ mV}$							
	T		F		S			
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
160 nm	20.3	1.99	141	22.7	4.93	0.33	28.60	68.79
500 nm	8.92	5.29	51	23.5	2.18	1.37	23.39	17.15
1 μm	11.7	10.5	50.8	33.5	3.66	3.82	13.88	8.77
2 μm	23.9	21.4	78.8	54.5	9.50	8.98	8.23	6.07
4 μm	58.3	43.6	154	95.8	28	20.2	5.50	4.74
	$V_{DD} = 150 \text{ mV}$							
	T		F		S			
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
160 nm	5.60	0.472	40	5.45	1.36	0.114	29.41	47.81
500 nm	2.28	1.24	12.8	5.45	0.565	0.370	22.65	14.73
1 μm	2.91	2.45	12.4	7.7	0.921	0.899	13.46	8.57
2 μm	5.84	4.98	18.9	12.5	2.35	2.11	8.04	5.92
4 μm	14	10.2	36.5	21.9	6.81	4.75	5.36	4.61

Table 5 CBB transistor's subthreshold current at T,F,S process corners for different values of L and V_{DD} using minimum W , $|V_{ds}|=|V_{gs}|$. The shaded column shows increased sensitivity for smaller channel lengths with regards to PMOS devices.

L ($W=160$ nm)	I_{ds} (nA)						Max. Variation $\frac{I_{ds-max}}{I_{ds-min}}$	
	$V_{DD} = 300 \text{ mV}$							
	T		F		S			
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
240 nm	397	86.5	851	344	409	23.6	2.14	14.58
640 nm	592	76.3	1130	208	621	29.9	1.91	6.96
1 μm	646	61.2	1090	136	531	30.3	2.05	4.49
2 μm	447	45.8	721	87.9	343	26.7	2.10	3.29
	$V_{DD} = 250 \text{ mV}$							
	T		F		S			
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
240 nm	131	26.3	312	139	142	6.16	2.38	22.56
640 nm	235	26	500	88.4	217	8.74	2.35	10.11
1 μm	309	23.2	561	60.8	262	10.1	2.14	6.02

2 μm	232	19.1	396	41.8	180	10.2	2.2	4.02
	$V_{DD} = 200 \text{ mV}$							
	T		F		S			
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
240 nm	37.3	6.72	95.2	44	41.5	1.47	2.29	29.93
640 nm	74.7	6.99	177	29.1	94.7	2.14	4.75	13.60
1 μm	119	6.77	237	21.3	105	2.65	3.17	8.04
2 μm	98.9	6.13	183	15.8	77.7	2.95	2.36	5.36
	$V_{DD} = 150 \text{ mV}$							
	T		F		S			
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
240 nm	9.98	1.59	26	11.5	11.1	0.34	2.61	33.63
640 nm	20.5	1.65	51.7	7.67	27.3	0.49	2.52	15.69
1 μm	36.6	1.64	79.9	5.83	33.5	0.61	2.39	9.54
2 μm	33.4	1.56	67.5	4.58	26.7	0.71	2.53	6.49

The data of Table 4 and Table 5 show a great change in the subthreshold current due to process variations for all transistor sizes and supply voltages. The minimum current variation is 1.91 times (191%), which is still a significant value. Furthermore, Table 4 shows that as the NMOS and PMOS devices get larger in width, current sensitivities to process variations decreases. For $W > 1 \mu\text{m}$, different supply voltages almost result in the same current variations. However, for smaller channel widths, 300 mV is the most robust for both NMOS and PMOS transistors. Although using larger channel widths for CBB structures results in enhanced robustness, it also increases power consumption significantly as shown in the current vs. W plots. Moreover, larger channel widths still result in significant change in current due to process variations. Thus, it is not desired for the ULP voltage-controlled frequency synthesizer to use $W > 1 \mu\text{m}$.

Table 5 shows that as L increases, current variation due to changes in process becomes smaller for PMOS transistors. Moreover, V_{DD} of 300 mV yields the least variations for PMOS devices. For NMOS, the robustness for devices using $L > 120 \text{ nm}$ are almost the same. Comparing Table 4 with Table 5, it can be concluded that increasing the channel length instead of the width reduces the sensitivity to process variations significantly. However, a major problem remains with using L as the design parameter. As the plots of Figure 36 and Figure 37 suggest, the channel length resulting in maximum current (peaks

of the hills in the plots) change depending on the process corner. Furthermore, the RSCE has a more significant and unpredictable influence on the transistor's current compared to the INWE. For example, Figure 36 shows that for the fast process corner, there is a different current behavior compared to other process corners, with a peak and a valley. In addition, simulations show that this effect is more significant for $V_{DD} < 300$ mV. Therefore, it is not as robust to use L as the design parameter in oppose to W . Moreover, a voltage supply of 300 mV is the best choice for robust subthreshold operation using smaller channel width as the design parameter (specifically for smaller channel widths). For other values of channel width and length, $V_{DD}=300$ mV yields almost the same sensitivity to process variations. Consequently, it is the best choice for the subthreshold supply voltage for operational robustness.

The current vs. channel length plots show that for the fast process corner, the current decreases significantly for PMOS transistors with $L > 240$ nm. Since PMOS is slower than NMOS, increasing L enforces a much greater channel width for proper switching of the circuit. The same affect is imposed on PMOS devices if L is increased for NMOS. Increasing the channel length of NMOS transistors result in larger current up to a length of about 1 μm , depending on the process corner. Although this current starts to decrease for $L < 1$ μm , it remains larger than current corresponding to minimum length up to channel length of about 3 μm (or even larger depending on process variations). It should be noted that using transistor fingers or parallel stacks to obtain larger current is not desired. The reason is that it results in larger changes in current due to process variations. Therefore, once again it is proven that increasing channel length is suitable for neither NMOS nor PMOS transistors for the VCFS application. Due to the above reasons, minimum channel length should be used for power consumption, switching speed and robustness concerns.

Since $V_{DD}=300$ mV showed an overall better performance with regards to robustness, it is selected as the subthreshold supply voltage. Next, the current values for the same channel widths are extracted for SBB NMOS and PMOS devices for all process corners. The results are recorded in Table 6. Similar to Table 4 and Table 5, the maximum variation column is shaded. Comparing the data of Table 4 and Table 6, it is observed that SBB configuration results in less current sensitivity to process variations for

different channel widths. This decreased variation is more significant for PMOS transistors. As it was previously seen, DTMOS results in less static power consumption compared to SBB. Moreover, DTMOS configurations yield the same speed and robustness as SBB for V_{gs} values close to V_{DD} . Therefore, the best choice is to use smaller width transistors using DTMOS configuration to simultaneously increase the robustness and decrease the power consumption.

Table 6 SBB transistor's subthreshold current at T,F,S process corners for different values of W and L , $|V_{ds}|=|V_{gs}|=300$ mV. The shaded column shows increased sensitivity for smaller channel widths with regards to both NMOS and PMOS devices. It also shows enhanced robustness over CBB transistors.

W ($L=120$ nm)	I_{ds} (μA)						Max. Variation $\frac{I_{ds-max}}{I_{ds-min}}$	
	Typical		Fast		Slow		NMOS	PMOS
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS		
160nm	0.76	0.13	3.01	0.71	0.2	0.03	15.2	25.29
500nm	0.67	0.38	2.71	1.12	0.18	0.14	14.97	8.12
1 μm	1.02	0.76	3.4	1.79	0.35	0.33	9.66	5.36
2 μm	2.08	1.56	5.64	3.14	0.89	0.78	6.32	4.05
4 μm	4.88	3.20	11.1	5.78	2.5	1.73	4.44	3.34

3.3. Summary

The behavior of MOSFETs operating in the subthreshold region using the 0.13 μm CMOS IBM technology kit was explored using simulations. The threshold and current relationship with V_{gs} , V_{bs} , W and L were investigated. Furthermore, threshold and current variations due to process fluctuations were examined for different transistor size and supply voltages. All these analyses were completed for CBB, SBB and DTMOS configurations of NMOS and PMOS transistors. It is concluded that selecting DTMOS configuration, V_{DD} of 300 mV, minimum L and $W < 1$ μm results in balanced power consumption and robustness for the VCFS to be designed in the next chapter. However, simulations show that the current sensitivity to process variations is still significant. Current stabilization is later improved in Chapter 6 using dynamic body-biasing circuits. The information of this chapter is applied to the VCFS in the next chapter for testing using the present methods for robustness and power efficiency enhancement. Thus, the second objective of this thesis work is fulfilled.

Chapter 4. Ultra-Low Power Sensor Signal Processing Unit Design

The sensor signal processing unit is one of the main blocks of the wireless dosimeter. It converts the sensed dose into a pulse train with different frequencies. The wireless dosimeter is first investigated at a system level and the SPU design specifications are extracted. Furthermore, this chapter presents the design of each part of the SPU using theoretical analysis as well as simulations. The voltage-controlled frequency synthesizer within the SPU operates in the subthreshold region. Thus, findings of the previous chapter regarding enhanced robustness and minimum power consumption in the subthreshold region are used.

4.1. System Level Analysis

The first step in any engineering design project is to understand the problem and its design specifications. This task is completed for the wireless dosimeter and SPU design using a system level approach.

4.1.1 *Wireless Dosimeter at System Level*

As discussed in Chapter 1, this work is partly a collaboration research project for wireless dosimetry. Figure 38 shows the signal processing unit and its neighboring blocks with their inputs and outputs. The energy harvesting unit provides all blocks with sufficient power using RF power scavenging. The FG-MOSFET sensor, which is embedded in an OPAMP read circuitry, measures the dose and converts it to a DC voltage in the range of -0.9 V to 0 V. The SPU receives this DC voltage and outputs pulses with different frequencies. These pulses should have an amplitude of about 1.2 V to turn the transmitting switch (a transistor operating in saturation) ON and OFF. The pulses are required to have either a decreasing or increasing frequency in response to higher dose levels (i.e. higher input voltage to the SPU).

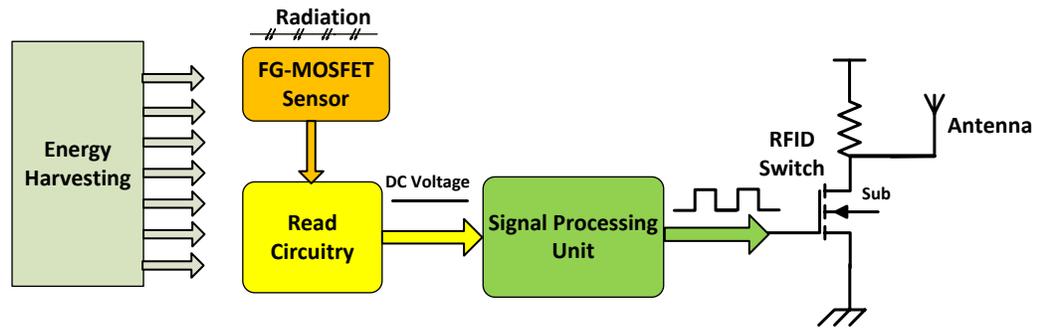


Figure 38 Wireless dosimeter transceiver system level block diagram.

4.1.2 Signal Processing Unit Design Specifications

The design specifications of the SPU are listed and explained below:

1. Latest testing of the FG-MOSFET sensor and read circuitry using thick-gate PMOS transistors shows a sensitivity of about 34.6 mV/Gy. Radiation is done using a Gamma Ray Cesium 137 source. In order to fully irradiate a blood bag, about 25 Gy is required. Thus, if the output of the OPAMP has a shift of approximately 875 mV, the blood bag is fully irradiated. Since the 25 Gy is not an exact number, we will look at the -900 mV – 0 range to have a safety margin. Consequently, the SPU needs to output pulses that have a significant change in frequency for about every 35 mV of increase at its input. Previous work done in weak inversion region of operation using 0.35 μm technology shows a change of at least about 4 – 20 KHz for every sensitivity measurement [42]. Since the receiver is yet to be designed, an accurate specification for the resolution cannot be assigned. However, a limitation for the receiver can be proposed. Consequently, we will take 1 – 4 KHz/Gy as the minimum resolution of the SPU. The minimum and maximum frequency changes restrict the quantizer design at the receiver. Since frequency modulation is adopted, the pulses corresponding to different dose measurements need to have the same duty cycle.
2. Recent sensor testing shows that the sensitivity listed in specification 1 is linear up to a voltage of about -300 mV that is about 17 Gy of radiation. After that point, it starts to become flat logarithmically. The frequency vs. input plot of the SPU

should be linear to signify the dose vs. characteristic of the read circuit for every measurement. Furthermore, the pulse train produced by the SPU is used to switch a transistor operating in saturation for transmission. Thus, it should have an amplitude of about 1.2 V.

3. The signal processing unit should consume minimum power. The reason is that the energy harvesting unit can provide limited energy per time. Testing results of the energy harvesting unit shows that a peak power of about -12 dBm, or 63 μ W, can be produced with 49.7% efficiency [3]. However, this is provided assuming that the SPU consumes minimal power in the scale of subthreshold operation. Thus, the power consumption of the SPU needs to be much smaller than 63 μ W. For convenience, less than 5% of the 63 μ W power budget, or 3.15 μ W, is taken as the power constraint.
4. A major design specification of the SPU is robustness. It needs to provide an accurate frequency per each input voltage in accordance to specifications 1 – 3. Thus, the SPU has to be robust in response to PVT variations.

Table 7 summarizes the design specifications of the wireless dosimeter signal processing unit.

Table 7 Signal processing unit design specifications.

Wireless dosimeter property	SPU design specification
35 mV/Gy radiation sensitivity	Minimum resolution of 1-4 KHz/Gy, Same duty cycle for all inputs.
V_{out} vs. radiation of sensor embedded circuit needs to be signified and translated by SPU. Transmission is done using a transistor operating in saturation.	Frequency vs. V_{in} should be linear. Output pulse should have an amplitude of 1 - 1.2 V.
Wireless energy harvesting provides 63 μ W for the wireless dosimeter.	Power consumption <3.15 μ W (sub-threshold circuit)
Accurate translation of sensed dose.	Operational robustness in response to PVT variations.

4.1.3 Signal Processing Unit at System Level

The SPU is to be designed to operate in the subthreshold region of MOSFETs. Thus, the SPU can be divided to three major blocks as shown in Figure 39. The sensor is modelled with a DC voltage source. The sensed dose is shifted using a DC shifter for the purpose of biasing a varactor or current mirror. The main block of the system is the voltage-controlled frequency synthesizer, which consists of a Schmitt Trigger (ST), ring oscillator (RO), either a varactor or voltage controlled current mirror (VCCM) and buffer (simply two inverters in series). This block outputs a pulse train with different frequencies and operates in the subthreshold region. The frequencies are generated using a ring oscillator. A Schmitt Trigger is embedded within the ring oscillator to decrease the noise sensitivity of the VCFS. The subthreshold level pulses cannot switch a transistor operating in saturation as discussed in the design specifications. Thus, a level shifter is to be designed as the last block of the SPU as shown in Figure 39.

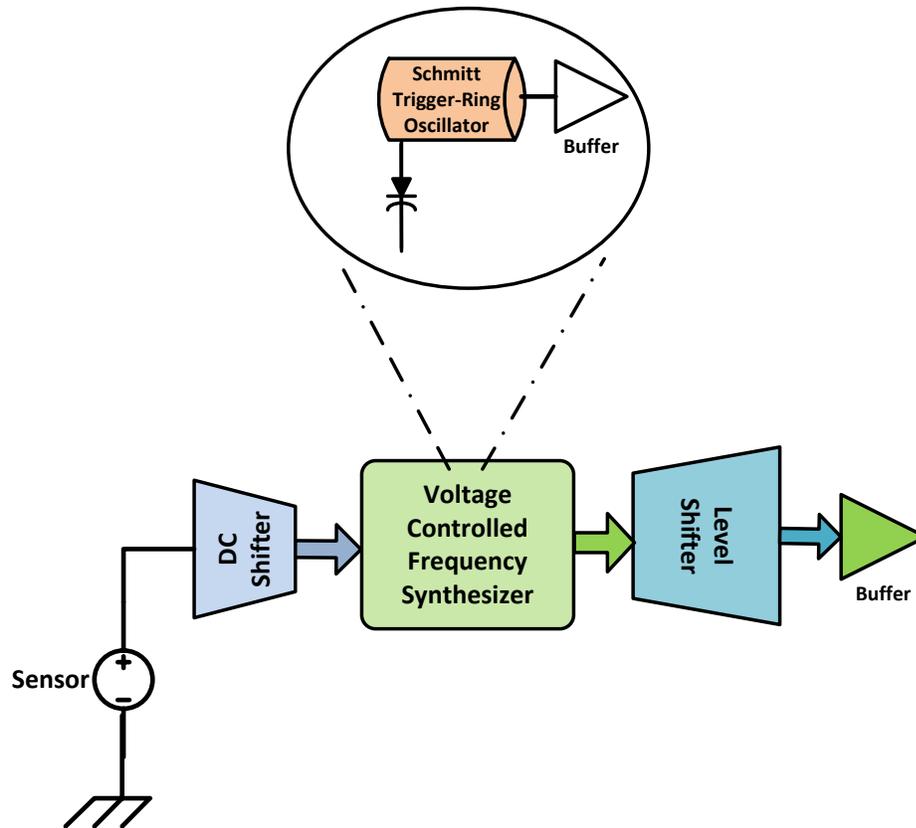


Figure 39 Subthreshold signal processing unit system level block diagram.

The frequencies generated by the VCFS can depend on the input using one of the following methods:

1. Voltage-controlled current mirror, charging / discharging a capacitor at one of the oscillator nodes.
2. Varactor with one end connected to an oscillator node and the other end to output of the sensor circuit.

The remainder of this chapter explains the design procedure of each sub-system of the SPU in detail using theory and simulations.

4.2. DC Shifter and Varactor

4.2.1 Theory

As discussed in the previous section, there are two ways of generating input-voltage-dependant frequencies for the VCFS. If the first technique is adopted, the sensed voltage can be applied to the gates of NMOS and PMOS transistors of a subthreshold current mirror. Thus, the input voltage needs to be shifted to a range of 0 – 300 mV. If the second option is used, the voltage is required to be between -500 mV and 1 V to change the capacitance of a varactor. If a VCCM is used, additional problems are imposed. Firstly, different voltages need to be applied to the gates of NMOS and PMOS devices of the current mirror. Moreover, these transistors should be carefully sized to yield a duty cycle of 50% at the output pulse. Since the transistor currents change in response to process variations, this task becomes difficult. These problems are not associated with the varactor and only a 500 mV shift in the input voltage is required. Therefore, a varying capacitor option is more convenient and will be adopted for the VCFS design.

To produce a scaled voltage for the varactor, the simplest structure to use is a chain of diode-connected PMOS transistors as shown in Figure 40. The sensed voltage that is the output of the read circuit is connected to the drain of the first PMOS in the chain. All the PMOS devices have a gate- drain connection. The source of the previous PMOS is connected to the drain of the next and the source of the last PMOS in the chain is connected to V_{DD} of 1.2V. The output, V_{sensed_scaled} , is obtained from one of the nodes (A, B, C, in Figure 40), which yields the desired voltage range for the varactor. This PMOS chain will not consume significant power if the number of transistors as well as their sizing is selected for operating in deep subthreshold region. However, the major

drawback of this circuit is static power consumption, since it is ON during the idle mode of the VCFS.

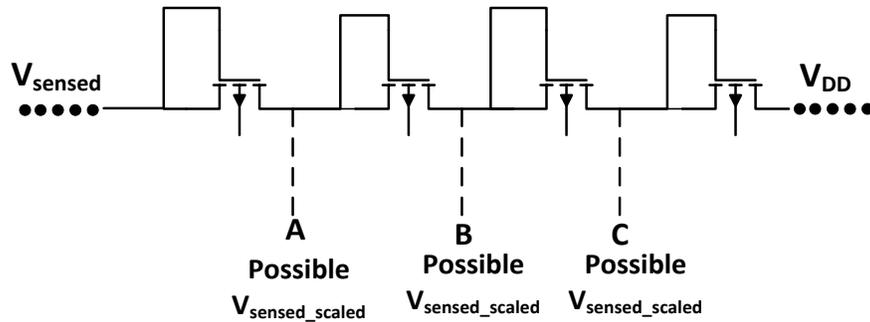


Figure 40 DC shifter structure.

4.2.2 Simulations

The 0.13 μm IBM CMOS technology kit offers the “NCAP” as a varying capacitor with robust operation and a wide range of capacitance. The varactor’s capacitance is changed depending on the voltage difference between its terminals. The capacitance range is dependant on parameters, such as RX width, PC length, number of gates (X) and RX repetition (Y). Figure 41 shows the test bench for the NCAP varactors.

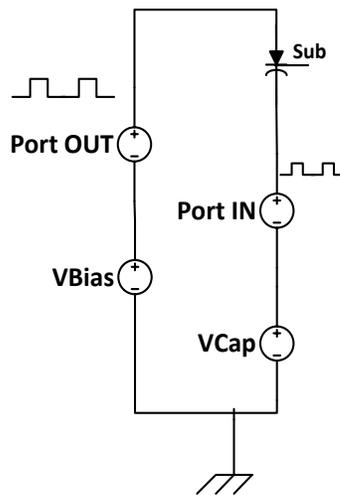


Figure 41 NCAP Varactor test bench.

The input and output ports in the test bench are set to pulses with a period of 5 μs , pulse width of 2.5 μs and rise/fall times of 100ns. These settings are chosen as the sensed voltage and VCFS oscillator node are both pulses during transient state. Simulations show that the DC shifter output involves small oscillations in the range of about 50 mV

rather than being a DC signal. Thus, the input port representing the output of the DC shifter is given an amplitude of about 50 mV. The output port that represents the VCFS node, is assigned an amplitude of 300 mV. Two DC voltage sources are used: V_{bias} representing a DC bias, and V_C , a control voltage modeling the output of the sensor embedded circuit. These sources are connected to the corresponding varactor ends. The V_{bias} source can be eliminated if the low and high voltages of the output port are set to 0 and 300 mV respectively.

Figure 42 shows the Capacitance vs. V_C for an NCAP varactor using the following design parameter values: RX Width=3.5 μm , PC length=300 nm, # of gates(X)=# of RX repetition=24. As this plot shows, the most significant changes of the capacitance occur for input voltages of 0 – 500 mV (6.15pF - 2.77pF). Moreover, the capacitance does not vary significantly for $V_C < 0$ or $V_C > 0.5$ V. Thus, the sensed dose should be shifted to 0 - 500 mV. To minimize the effect of transistor capacitances (typically in the range of 100 – 500 fF for the technology) on the VCFS's oscillation frequency, the varactor is sized to yield a capacitance range in the scale of pF. Transistor capacitances change due to transistor size, process variations and DC operating point as discussed in Chapter 2. As a result, if these capacitors affect the oscillation frequency, the circuit is not robust.

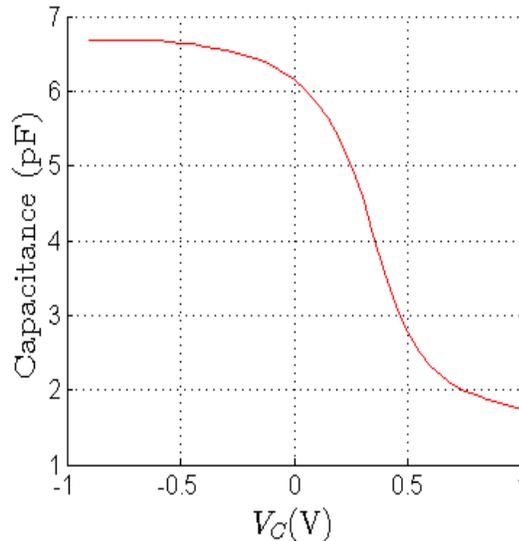


Figure 42 Capacitance vs. V_C for NCAP varactor using RX Width=3.5 μm , PC length=300 nm, # of gates(X)=# of RX repetition=24.

The DC shifter transistors should be forced to operate in the subthreshold region for minimum power consumption. Thus, 7 transistors are connected in series for the

shifter as shown in the test bench of Figure 43. The transistors are all sized using minimum W (160 nm) and L (120 nm). All the transistor bulks are connected to V_{DD} and the gate of the third transistor closest to V_{in} is chosen as the output. This choice has been made by the aid of simulations as this node almost yields the varactor voltage range. Sweeping the input from -900 mV to 0 and running DC simulations, the plots of Figure 44 are obtained for typical, fast and slow process corners. As the plots show, the circuit shifts the input voltage linearly within the 0 – 500 mV range as desired. The shifted voltage range is -70.6 – 486 mV, -83.1 – 477 mV and -61.8 – 498 mV for the T, F and S process corners respectively. These values are fairly close to the 0 – 500 mV range. Process variations have minimum effect on the DC shifter output range.

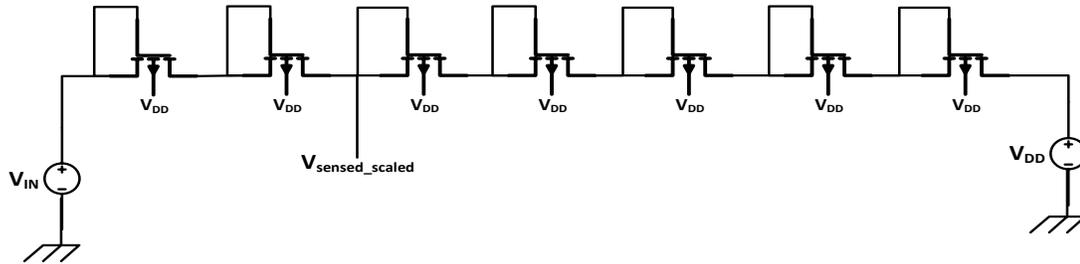


Figure 43 DC shifter test bench.

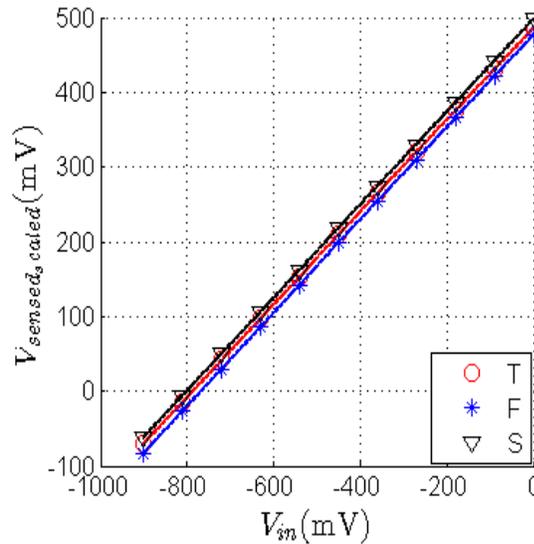


Figure 44 DC shifter output for different process corners.

4.3. Subthreshold Schmitt Trigger

Subthreshold circuits are more prone to noise due to their low operating current compared to superthreshold ones. Therefore, a simple ring oscillator will not be sufficient for the sensor SPU, which has neighboring superthreshold circuits. A Schmitt Trigger circuit can be embedded within the ring oscillator to decrease the noise sensitivity of the subthreshold VCFS.

4.3.1 Theory

The Schmitt Trigger, shown using the symbol of Figure 45 (a), operates based using positive and re-generative feedback and has two main properties [11]:

1. Responds to a slowly changing input with a fast transition at the output.
2. Has a voltage-transfer characteristic with different switching thresholds for the positive-to-negative and negative-to-positive transitions as demonstrated in Figure 45 (b). The switching thresholds for the low-to-high and high-to-low transitions are denoted by V_{M+} and V_{M-} respectively, and the difference between the two is called the hysteresis of the Schmitt Trigger.

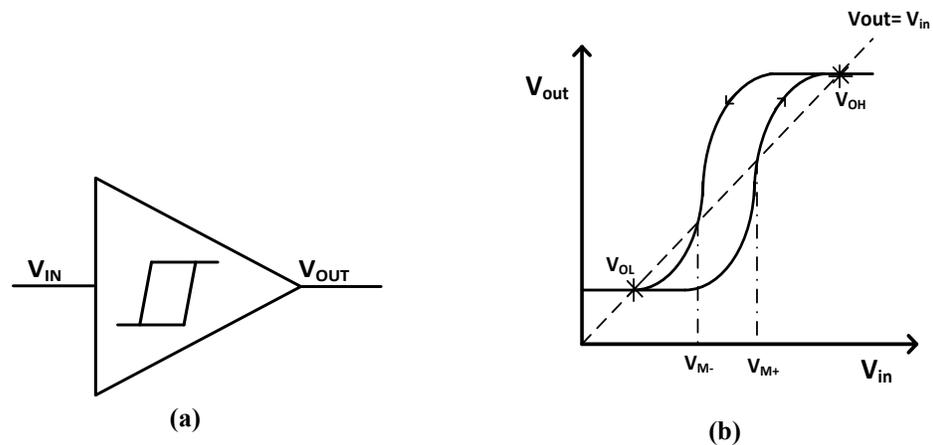


Figure 45 a) Schmitt Trigger Symbol b) Schmitt Trigger voltage-transfer characteristic [11].

The above two properties of the ST circuit result in two major advantages: noise suppression and fast signal transition yielding a sharp edged pulse. The most convenient Schmitt Trigger circuit suggested in popular texts is shown in Figure 46 [11]. The most important property of the ST is the hysteresis width. This width is the noise margin of the circuit. Researchers have proposed methods to increase the hysteresis width of Schmitt

Trigger circuits. For example, designing an adjustable hysteresis width ST using additional inverters or differential circuit design have been suggested [47] [48]. However, most of these techniques have been applied to Schmitt Triggers operating in superthreshold. An ULP Schmitt Trigger operating in the subthreshold region has been suggested using DTMOS devices and feedback paths to the bulks of the transistors [49]. However, the circuit is designed for high switching speed and sensitivity to process variation is not enhanced.

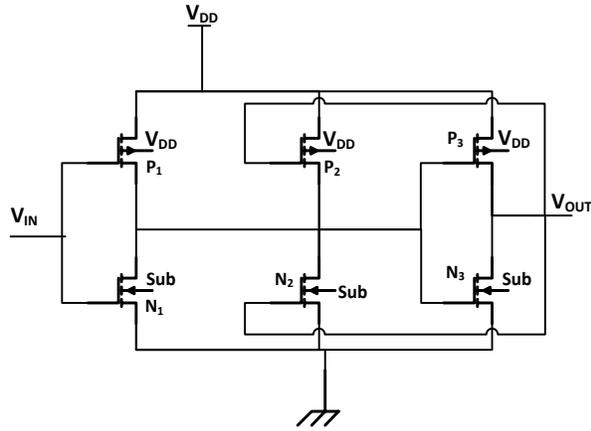


Figure 46 Conventional CMOS Schmitt Trigger [11].

In order to design a robust ST circuit suitable for the subthreshold signal processing unit, the operation of the ST circuit of Figure 46 needs to be understood. Assume that V_{in} is initially zero for the low-to-high transition, so that the output voltage is zero. The feedback loop turns the PMOS transistor, P_2 , ON, while N_2 is OFF. The input signal now connects the two PMOS transistors in parallel (P_1 and P_2) as a pull-up network. Thus, an inverter together with the NMOS transistor, N_1 , is created. As a result, the pull-up power is stronger as the two PMOS transistors are opposing only one NMOS device. This moves the threshold voltage (V_{M+}) upwards. Once the inverter switches, the regenerative feedback mechanism turns P_2 OFF as well as activating N_2 , creating an extra pull-down device. Consequently, the transition has become faster. Similarly, for the high-to-low switching, the pull-down network originally consists of N_1 and N_2 in parallel fighting the PMOS device P_1 and reducing the switching threshold, V_{M-} .

To have a deeper understanding of the ST circuit operating in the subthreshold region, a mathematical analysis is also required. For the positive switching threshold, the

two PMOS transistors, P_1 and P_2 are opposing N_1 . Therefore, at the switching point, the sum of P_1 and P_2 currents is equal to that of N_1 . However, if it is assumed that the input changes instantly, the P_1 current can be neglected. Therefore, for the low-to-high transition, the main contention is occurring between N_1 and P_2 . To calculate V_{M+} , V_{gs} of N_1 should be set to V_{M+} , while V_{sg} of P_2 is equal to $V_{M+} - V_{DD}$. Furthermore, the switching threshold is defined as where $V_{in}=V_{out}=V_{M+}$. As a result, V_{ds} for N_1 is V_{M+} , while it is $V_{DD} - V_{M+}$ for P_2 . Equating the two currents using the subthreshold current formula of (2-1), we have:

$$\begin{aligned} & \mu_n C_{oxn} \left(\frac{W}{L}\right)_{N1} v_{Tn}^2 e^{1.8} e^{\frac{V_{M+} - V_{thn}}{n_n v_{Tn}}} \left(1 - e^{-\frac{V_{M+}}{v_{Tn}}}\right) \\ & \approx \mu_p C_{oxp} \left(\frac{W}{L}\right)_{P2} v_{Tp}^2 e^{1.8} e^{\frac{V_{DD} - V_{M+} - V_{thp}}{n_p v_{Tp}}} \left(1 - e^{-\frac{V_{DD} - V_{M+}}{v_{Tp}}}\right) \end{aligned} \quad (4-1)$$

Typical values for the thermal voltage are in the 25 – 30 mV range for the 0.13 μm technology. V_M will be at least 150 mV in the worst case where the hysteresis width is zero for V_{DD} of 300 mV. Therefore, the $\left(1 - e^{-\frac{V_{M+}}{v_{Tn}}}\right)$ and $\left(1 - e^{-\frac{V_{DD} - V_{M+}}{v_{Tp}}}\right)$ terms are almost equal to one and can be neglected. Thus, taking natural logarithm from both sides, we have:

$$\begin{aligned} & \ln\left(\mu_n C_{oxn} \left(\frac{W}{L}\right)_{N1}\right) + 2\ln(v_{Tn}) + \frac{V_{M+} - V_{thn}}{n_n v_{Tn}} \approx \\ & \ln\left(\mu_p C_{oxp} \left(\frac{W}{L}\right)_{P2}\right) + 2\ln(v_{Tp}) + \frac{V_{DD} - V_{M+} - V_{thp}}{n_p v_{Tp}} \end{aligned} \quad (4-2)$$

Re-arranging the above to isolate for V_{M+} , the following relationship for the low-to-high switching threshold is obtained as:

$$\begin{aligned} V_{M+} \approx & \frac{A \left(\ln\left(\mu_p C_{oxp} \left(\frac{W}{L}\right)_{P2}\right) + 2 \left(\ln(v_{Tp}) - n(v_{Tn}) \right) - \right)}{C} - \\ & \frac{A \left(\ln\left(\mu_n C_{oxn} \left(\frac{W}{L}\right)_{N1}\right) \right) - B}{C} \end{aligned} \quad (4-3)$$

$$\begin{aligned} A &= n_n v_{Tn} n_p v_{Tp} \\ B &= n_n v_{Tn} V_{thp} - n_p v_{Tp} V_{thn} - n_n v_{Tn} V_{DD} \\ C &= n_n v_{Tn} + n_p v_{Tp} \end{aligned}$$

Similarly, for the high-to-low switching threshold V_{M-} , P_1 and N_2 will be fighting to pull the voltage down and their currents are almost equal assuming a step signal at the input. Thus, V_{M-} can be estimated as:

$$\frac{A \left(\ln \left(\mu_p C_{oxp} \left(\frac{W}{L} \right)_{P1} \right) + 2 \left(\ln(v_{Tp}) - n(v_{Tn}) \right) - \ln \left(\mu_n C_{oxn} \left(\frac{W}{L} \right)_{N2} \right) \right) - B}{C} \quad (4-4)$$

Looking at equation (4-3), it is evident that as $\left(\frac{W}{L}\right)_{P2}$ increases, V_{M+} also becomes larger. Similarly, equation (4-4) shows that as $\left(\frac{W}{L}\right)_{N2}$ becomes larger, the high-to-low switching threshold decreases. Therefore, the larger the second stage inverter, the wider the hysteresis width, which is desired for the Schmitt Trigger circuit. However, as it was mentioned in 3.2, transistor sizing in the subthreshold regime is not the same as super-threshold. Increasing W or decreasing L does not necessarily increase the current. Therefore, increasing the strength of the second stage inverter is a more precise conclusion. Ideally, V_{M+} and V_{M-} should be V_{DD} and 0 respectively for highest switching speed and largest noise margin.

The current relations of the second and first stage inverters decide the hysteresis width. Thus, these current ratios are the main design criteria of the ST:

$$\rho = \frac{IDS_{P2}}{IDS_{N1}}, \quad \sigma = \frac{IDS_{N2}}{IDS_{P1}} \quad (4-5)$$

If ρ and σ become too large, N_1 and P_1 will never be able to overcome the current strengths of second stage transistors. Consequently, switching will not occur. Therefore, the maximum value for these ratios can be determined as the point where switching occurs and ρ and σ are as large as possible. For enhanced robustness, the worst case process corner has to be considered. The following design steps have to be followed for the ST design in the subthreshold region:

1. Size N_1 and P_2 such that they have minimum current. Use minimum L for all transistor sizing for robustness.
2. Set-up the test bench for a Schmitt Trigger circuit with two inverters at the input and output sized like N_1 and P_1 .

3. Use DC simulation and sweep V_{in} from V_{DD} to 0 (output of the input inverter goes from low-to-high). Size P_2 to obtain the highest value for V_{M+} using the TT process corner. Using the current values of P_2 and N_1 , calculate ρ .
4. Sweep V_{in} from 0 to V_{DD} (output of the input inverter goes from high-to-low). Size N_2 to obtain the lowest value for V_{M-} using the TT process corner. Using the current values of N_2 and P_1 , calculate σ .
5. Find the minimum current for N_1 using the slow process corner. Calculate the amount of current that P_2 needs at its fast process corner to yield the same ρ ratio. Next, find the appropriate channel width and transistor size for P_2 accordingly. If decreasing the size of P_2 still did not yield ρ , increase the strength of N_1 using current characteristic curves.
6. Using DC simulations, find the minimum current for P_1 using the slow process corner. Calculate the current that N_2 needs at its fast process corner to yield the same σ ratio. Next, find the appropriate channel width and transistor size for N_2 accordingly. If decreasing the size of N_2 did not yield σ , increase the strength of P_1 using current characteristic curves.

As it was discussed in chapter 3, subthreshold DTMOS transistors, which have a body-gate connection, have higher speed and lower sensitivity to process variations. Dynamic threshold MOSFETs also have lower leakage in the subthreshold region. Therefore, the first and third stage inverter devices will be designed using DTMOS configuration. Using DTMOS, these transistors can use smaller channel widths, decreasing their capacitance and reducing power consumption. It should be noted that the second stage inverter of the ST cannot be designed using DTMOS. The reason is that DTMOS logic leads to more current, thereby forcing the first stage transistors to become much larger. Furthermore, the gates of N_2 and P_2 are connected to the output of the ST as feedback path. Thus, connecting these gates to bulks can disrupt the circuit's operation according to simulations.

4.3.2 Simulations

Figure 47 shows the schematic for the Schmitt Trigger circuit test bench. V_{DC} is used for DC simulations involving the hysteresis and V_{tran} for the transient response. Previous

chapter demonstrated that 300 mV is the best choice of subthreshold supply voltage (V_{DD_Subth}) for robust subthreshold operation using $W < 1 \mu\text{m}$ and minimum L for the 0.13 μm technology. Therefore, it is used for all subthreshold circuits involved in this work. Simulations show that an inverter with $W_N=500 \text{ nm}$ and $W_P=1 \mu\text{m}$ yields a switching threshold of 150 mV, which is half of the 300 mV supply voltage. Therefore, all devices, including the input and output inverter, are sized using these values. The first and second stage ST transistors will be resized to obtain the widest hysteresis width following the outlined design steps. As it can be observed in Figure 47, the first and third stage inverters of the Schmitt Trigger are designed using DTMOS logic to increase switching speed and robustness.

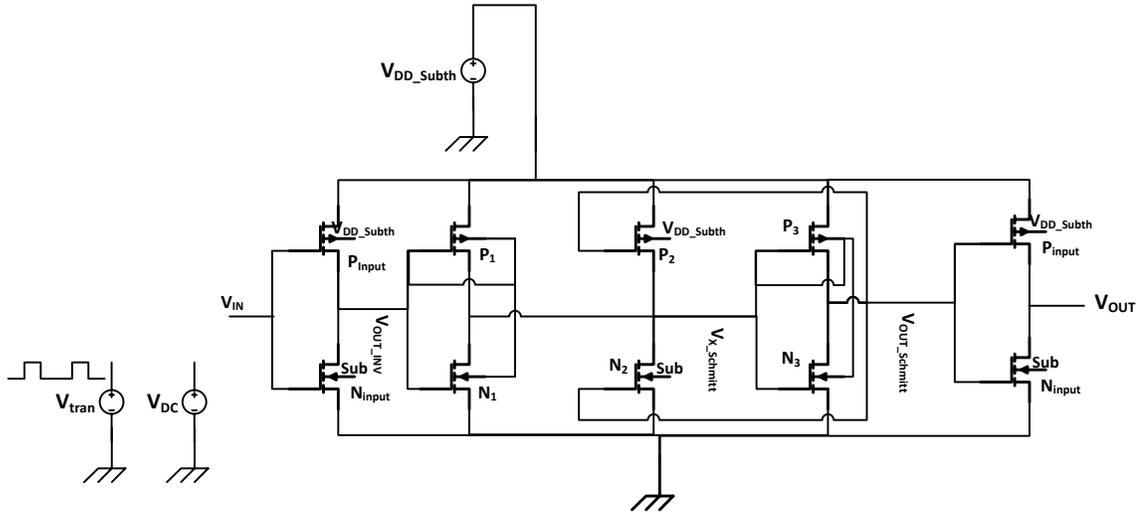


Figure 47 Schmitt Trigger circuit test bench.

Steps 1 and 2 of designing the Schmitt Trigger circuit are completed as 500 nm and 1 μm are chosen for the default channel width of all the NMOS and PMOS devices at first. Following the design procedure to step 3, a sweep for V_{DC} from 300 mV-0 is completed. The maximum value for V_{M+} is obtained as 299 mV using $W_{P1}=5 \mu\text{m}$. Figure 48 (a) demonstrates this result, where V_X denotes the output of first stage inverter and $V_{out_input_inv}$ represents the output of input inverter (as shown in Figure 47). The switching threshold is the intersection of outputs of the ST (V_{M+}) and the input inverter at the high-to-low switching point. As the plot shows, the output of the Schmitt Trigger becomes high with a sharp edge when $V_{out_input_inv}$ is 299-300 mV. The current ratio ρ can now be calculated by extracting the currents of a CBB PMOS with $W_{P2} = 5 \mu\text{m}$, and a

SBB NMOS transistor (DTMOS at switching moment) with $W_{N1} = 500$ nm ($L = 120$ nm for all):

$$\rho = \frac{934.082 \text{ nA}}{692.342 \text{ nA}} \approx 1.35$$

Similarly, for the high-to-low switching, a DC sweep of 0-300 mV using the DC voltage source is completed according to step 4. The PMOS device of the second stage inverter is now increased to $5 \mu\text{m}$ for maximum V_{M+} . After running parametric sweeps, it is found that with $W_{N2} = 3.9 \mu\text{m}$, V_{M-} is 0-1 mV as shown in Figure 48 (b). The current ratio σ can now be calculated by taking the currents of a CBB NMOS with $W_{N2} = 3.9 \mu\text{m}$, and a SBB PMOS with $W_{P1} = 1 \mu\text{m}$:

$$\sigma = \frac{945.466 \text{ nA}}{753.584 \text{ nA}} \approx 1.26$$

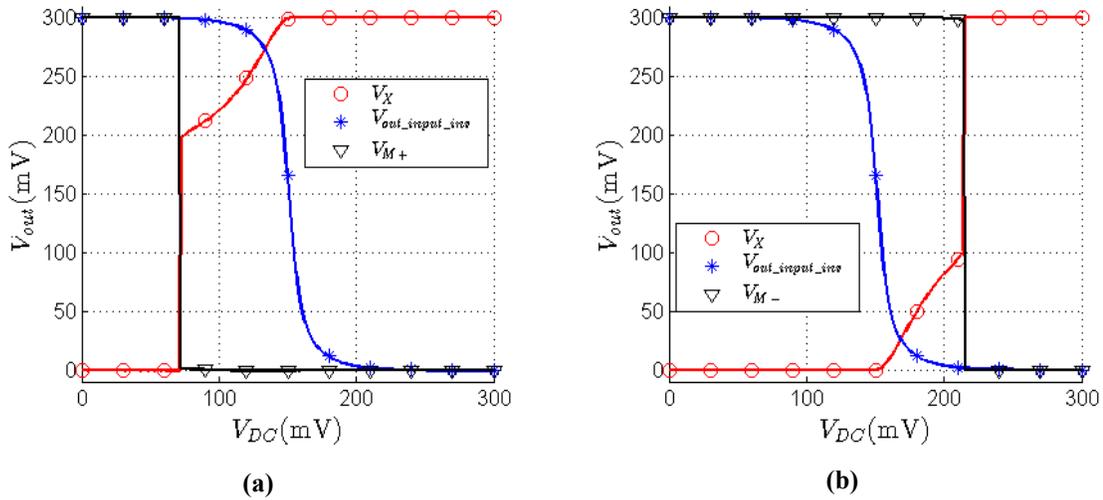
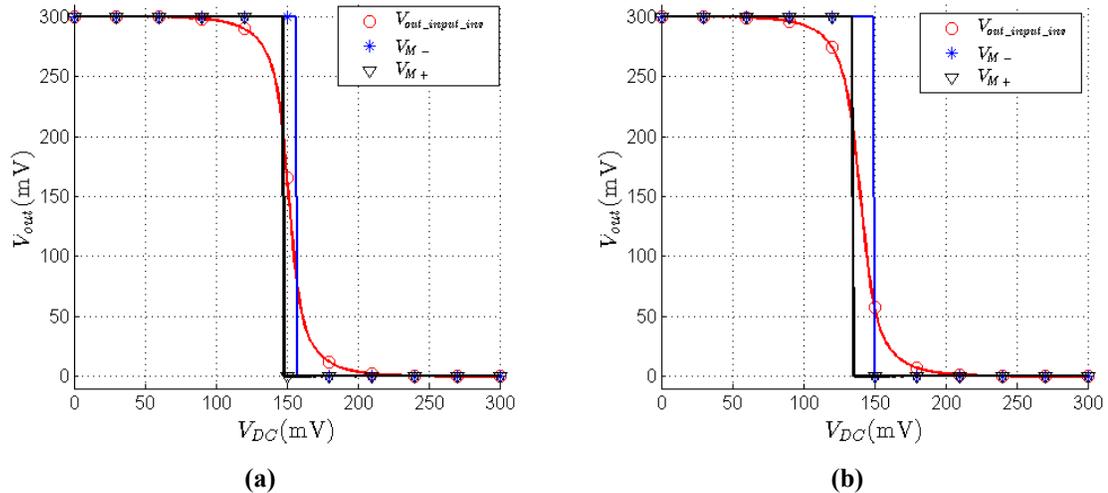


Figure 48 Finding maximum values for a) ρ by plotting maximum V_{M+} b) σ by plotting minimum V_{M-} for the Schmitt Trigger at TT process corner.

The next steps in the ST design process involve testing at different process corners and re-sizing transistors for robust operation. Following the 5th design step for the low-to-high switching, the worst case happens at the SF process corner. If the second stage PMOS is too strong, while the first stage NMOS is too weak, switching cannot occur. Thus, N_1 and P_2 have to be resized to maximize V_{M+} at the SF process corner. Using SBB I_{ds} vs. W curve for NMOS, It is found that N_1 ($W_{N1} = 500$ nm) yields a current 194.79 nA at the slow corner. Consequently, P_2 ($W_{P2} = 5 \mu\text{m}$) needs to have a maximum current of 262.77 nA at the fast corner. Simulation shows that using a minimum sized

PMOS with $W_{P2} = 160$ nm will result in maximum V_{M+} with a safety margin at 288.84 mV for the SF process corner.

For the high-to-low switching, the worst case occurs for the FS process corner. This is because if the second stage NMOS becomes too fast, while the first stage PMOS is too slow, σ exceeds its maximum value resulting in no switching. Therefore, using I_{ds} vs. W for a SBB PMOS, it was found that P_1 yields a current of 329.68 nA at the slow process corner. To maintain a σ of 1.26, N_2 needs a current of 413.74 nA at the fast process corner. Simulation shows that this current is smaller than the minimum value a CBB NMOS would yield with $V_{DD} = 300$ mV. Thus, the PMOS has to become wider in order to keep the current ratio. Using I_{ds} vs. W , it is found that the PMOS needs to be at least 1.2 μm . The high-to-low switching showed more sensitivity to process variations. Therefore, $W_{P2} = 1.5$ μm and $W_{N1} = 640$ nm (NMOS width yielding minimum current at fast corner) were selected for robustness. With the new sizing, V_{M-} becomes about 13.38mV at the FS process corner, which is close to the minimum value of 0 with a safety margin similar to the low-to-high switching design. Thus, the ST design is completed. Figure 49 shows the ST hysteresis for TT, FF, SS, FS and SF process corners.



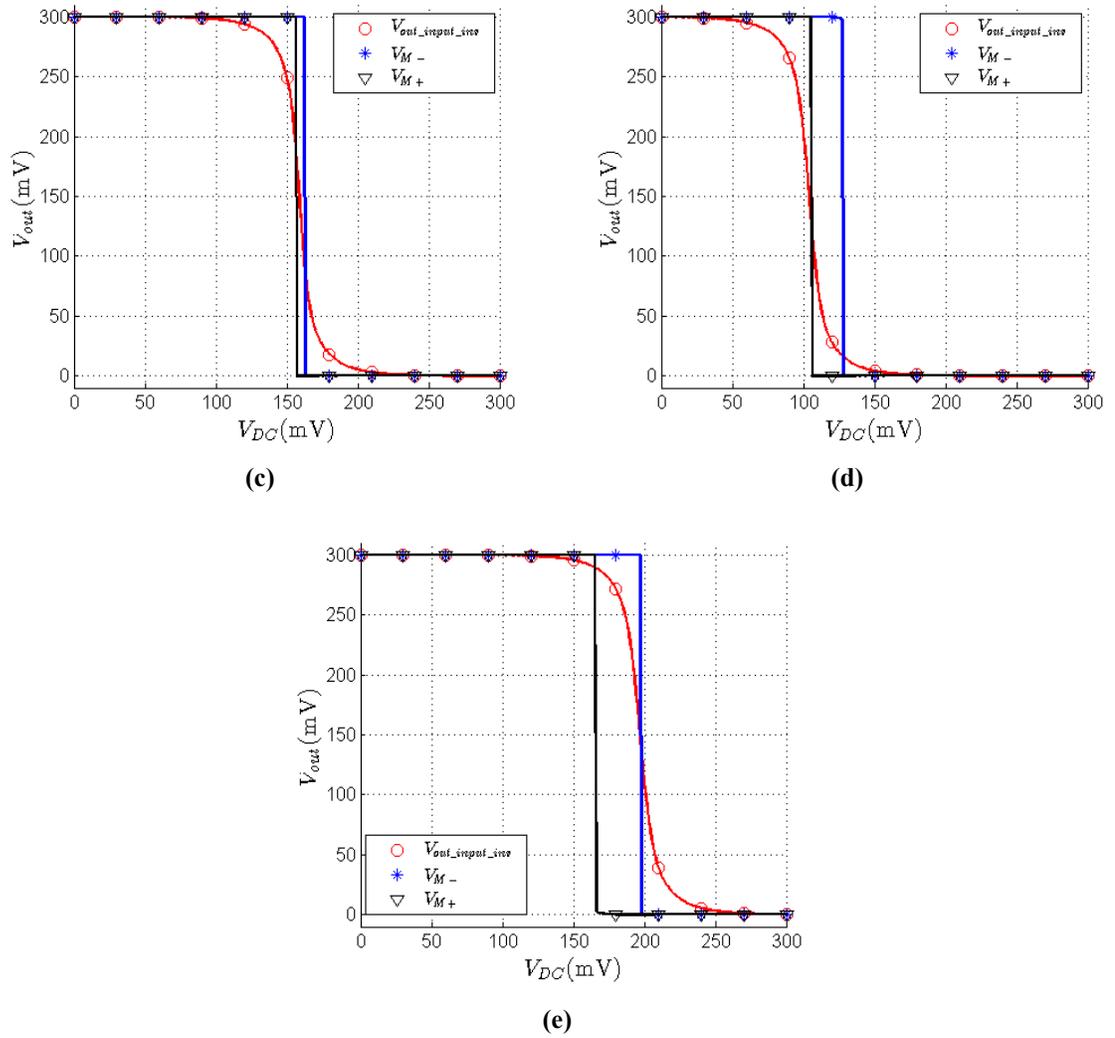


Figure 49 Schmitt Trigger hysteresis after re-sizing for robust subthreshold operation. a) TT b) FF c) SS d) FS e) SF process corners.

Table 8 reports the transistor sizing for the Schmitt Trigger design. Table 9 summarizes the values of V_{M+} and V_{M-} for different process corners. As it can be seen in Table 9, V_{M+} has decreased significantly to minimize V_{M-} in the FS process corner and visa-versa. Both of these modifications were made to sacrifice hysteresis width or noise margin for robustness and process variation tolerance. The noise margin values of Table 9 together with the plots of Figure 49 show that the hysteresis width changes significantly due to process variations. This is the major problem associated with the Schmitt Trigger, which can in turn affect the VCFS. This issue is later addressed in Chapter 6 using a dynamic body-biasing technique for the ST transistors.

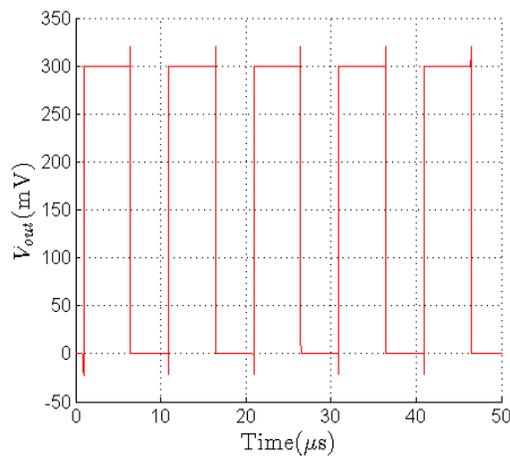
Table 8 Schmitt Trigger transistor sizing.

Design parameter	Value (μm)
L	0.12
$W_{inputN}=W_{N1}=W_{N3}$	0.5
$W_{inputP}=W_{P3}$	1
W_{P1}, W_{N2}, W_{P2}	1.5, 0.64, 0.16

Table 9 Switching threshold values of the Schmitt Trigger for different process corners.

Process Corner	V_{M+} (mV)	V_{M-} (mV)	Noise Margin (mV)
TT	200.01	85.54	114.47
FF	208.65	57.97	150.6
SS	187.11	86.18	100.93
FS	126.25	13.38	112.87
SF	288.84	139.76	190.24

Transient simulations are required to obtain the delay and frequency of the circuit for different process corners. A pulse supply voltage with a period of 10 μs , pulse width (PW) of 5 μs , rise and fall times (RT, FT) of 500 ns and amplitude of 300 mV is applied to the ST. Figure 50 shows the transient output of the Schmitt Trigger for TT process corner. Running the same simulation for other process corners, it can be observed that the pulses have almost the same frequency as the input signal.

**Figure 50 Schmitt trigger transient response to an input pulse with period=10 μs , PW= 5 μs , RT/FT=500 ns - TT corner.**

A problem associated with the Schmitt Trigger design is the positive and negative glitches at the high-to-low and low-to-high transitions. These glitches that are due to short circuit current and delay between the first and last stage inverters, cause additional power consumption. Table 10 summarizes the rise and fall times of the transient response of the ST circuit using an input pulse with a period of 2 μ s, PW of 1 μ s and RT/FT of 200 ns for different process corners. Table 10 demonstrates that the RT/FT of the ST output pulse are much less than that of the input. This result was expected, as the Schmitt Trigger responds to a slowly changing input with a fast transition at the output.

Table 10 Rise and fall times of the Schmitt Trigger output for different process corners in response to an input pulse with period=2 μ s, PW=1 μ s, RT= FT=200 ns.

Process Corner	Rise time (ns)	Fall time (ns)
TT	4.22	23.12
FF	3.03	15.69
SS	13.42	70.25
FS	9.92	40.54
SF	13.32	51.98

Lastly, transient simulations show that the Schmitt Trigger can operate up to a frequency of about 1.25 MHz. This result was obtained by gradually decreasing the pulse period and width in the transient simulation test bench. It was observed that the pulse cannot be smaller than 800 ns in period, generating an output pulse of 1.25 MHz in frequency for all process corners. It should be noted that at this frequency, the Schmitt Trigger still produces a sharper output in response to a slowly changing input (i.e. the rise/fall times of the output pulse are less than that of the input). The Schmitt Trigger consumes a power of about 8.38 nW at the maximum frequency using the worst process corner.

4.4. Subthreshold Voltage-Controlled Frequency Synthesizer

The VCFS is the main block of the SPU and converts the measured dose to a specific frequency. The DC shifter scales the input voltage, generating a capacitance value at the va-

factor. This varactor is connected to a node within a ring oscillator containing a ST circuit (STRO). The STRO together with the varactor is referred to as the VCFS.

4.4.1 STRO

To design the VCFS pulse generator, first a ring oscillator using the previously designed Schmitt Trigger has to be tested. The Schmitt Trigger can be embedded in a ring oscillator as shown in Figure 51. A transient simulation using an initial node condition of $V_{out_ring_osc}=0$ is completed. Figure 52 shows the output of the STRO for the FS and SF process corners.

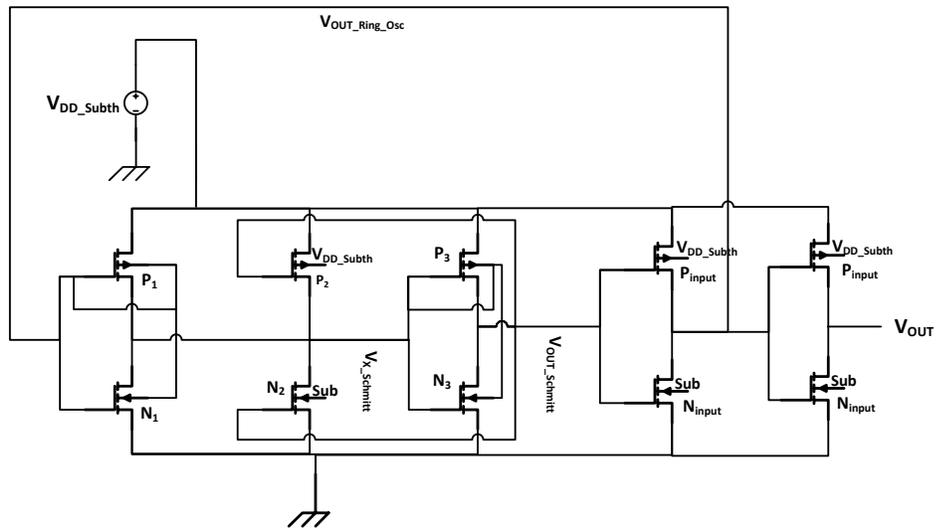


Figure 51 STRO test bench.

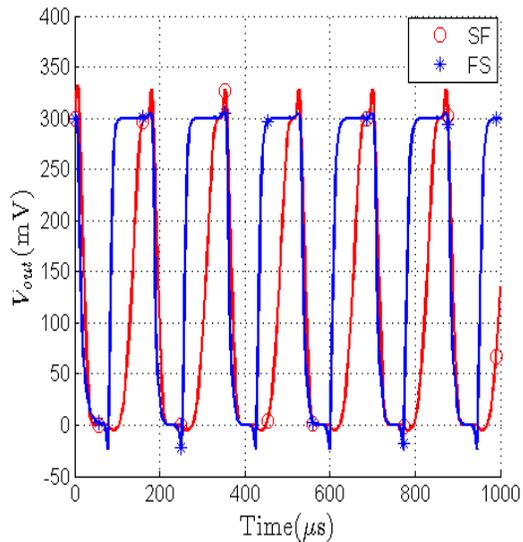


Figure 52 STRO output for SF, FS process corners.

The output frequency of the STRO for the TT, FF, SS, FS and SF process corners is 14.75 MHz, 49.03 MHz, 4.62 MHz, 10.71 MHz and 5.78 MHz respectively. Figure 52 shows that the duty cycle and pulse shapes for the STRO output change due to process variations. Furthermore, all of the pulses contain spikes at the switching edges due to the short circuit current as seen in Figure 52. These problems were previously encountered for the Schmitt Trigger circuit's transient response. However, the main problem arises in the significant frequency shift as the result of process variations. This problem will be further analyzed in the next sections and is solved in Chapter 6.

4.4.2 VCFS

Figure 53 shows the schematic of the voltage-controlled frequency synthesizer with the DC shifter.

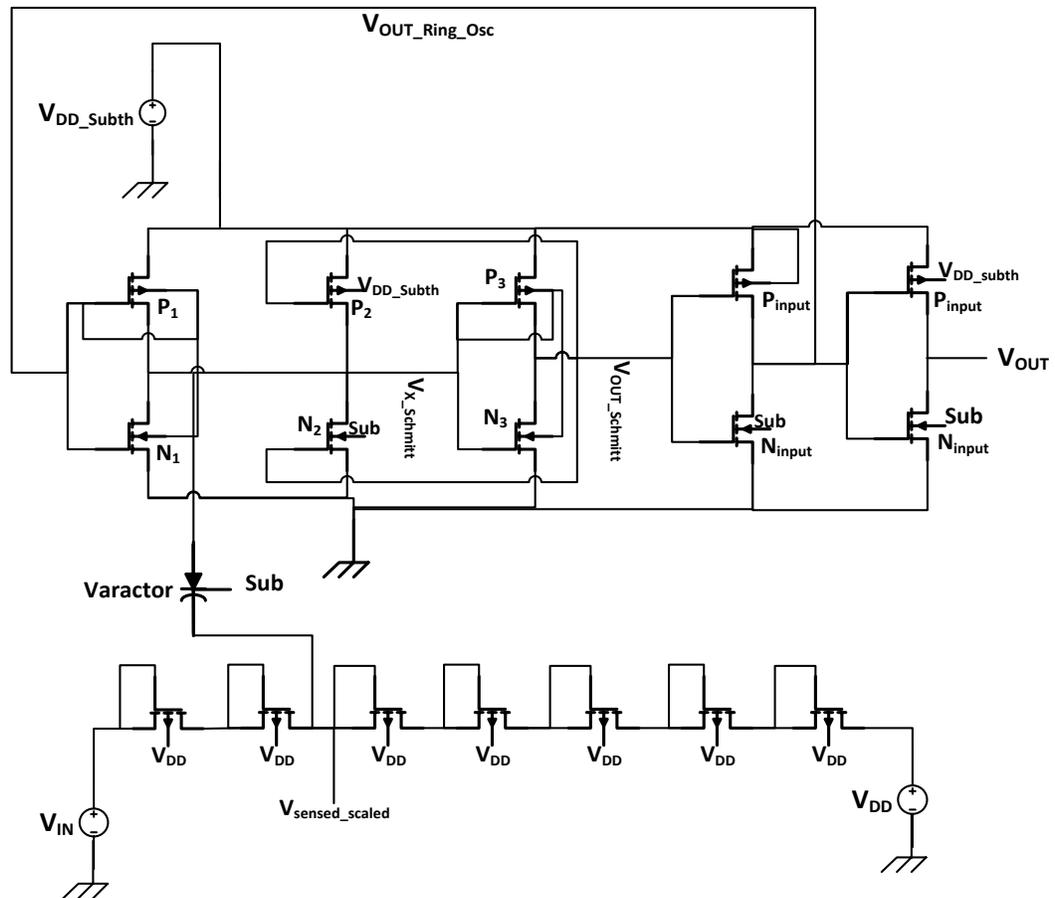


Figure 53 Voltage-controlled Frequency Synthesizer Pulse Generator test bench.

As it can be seen in Figure 53, one end of the varying capacitor is connected to the output of the DC shifter, while its other side is connected to the $V_{X_schmitt}$ node of the STRO. Simulations showed that if the capacitor is connected to any other node within the RO, it will cause disturbance and oscillation start-up difficulties. To test the VCFS, a transient simulation is completed with an initial condition of setting the output of the oscillator to zero. Moreover, the output of the sensor is modelled with a DC voltage source ranging from -900 mV to 0. The capacitance decreases as the input voltage increases. Thus, an increasing frequency response to the sensed dose is expected.

Figure 54 shows the output of the DC shifter for different process corners and input values of -900 mV and 0. This plot shows that the output of the shifter can vary from -200 mV to -80mV for $V_{in} = -0.9$ V, and 330-450 mV for $V_{in} = 0$, depending on the process corner. This shows a significant shift compared to the intended 0 – 500 mV range. Furthermore, the shape and frequency of V_{sensed_scaled} is strongly dependent on the process corner, which leads to frequency shifts at the output due to process variations. The output of the DC shifter is not a DC signal as intended, as one end of the varactor is connected to the VCFS. However, the variations in amplitude are much greater than expected. This can be due to fluctuations of V_{sensed_scaled} due to sensitivity of the VCFS to process variations.

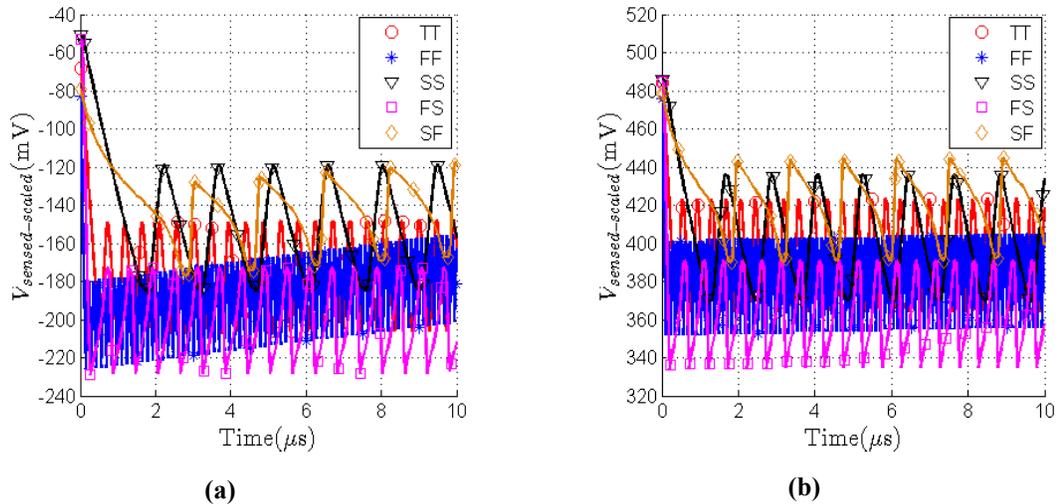


Figure 54 DC shifter output when connected to VCFS at different process corners for a) $V_{in} = -0.9$ V b) $V_{in} = 0$.

Figure 55 and Figure 56 show the pulse train produced by of the VCFS for the FF and SF process corners using $V_{in} = -900$ mV and $V_{in} = 0$ for each corner respectively. The frequency difference due to process variations is greatest between these two process corners as seen in the plots.

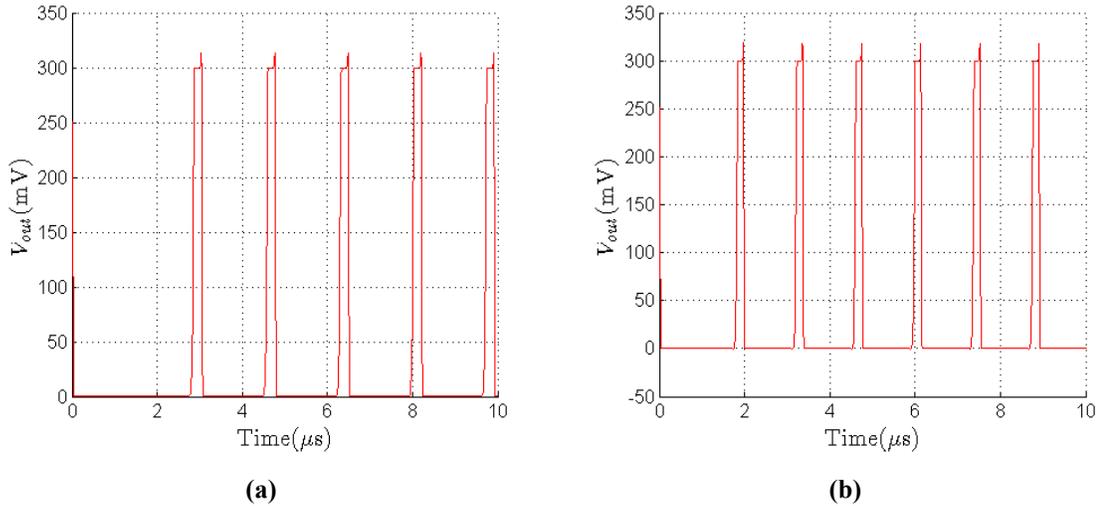


Figure 55 VCFS output pulse train, SF process corner for a) $V_{in} = -0.9$ V b) $V_{in} = 0$.

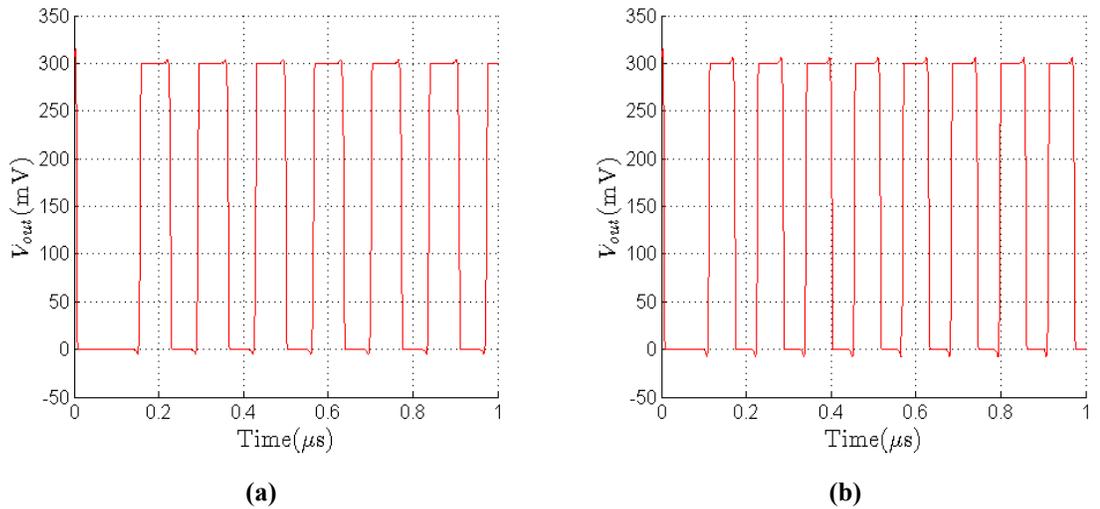


Figure 56 VCFS output pulse train, FF process corner for a) $V_{in} = -0.9$ V b) $V_{in} = 0$.

Furthermore, simulation results for all process corners shows that the VCFS yields pulses with the following frequencies for the TT, FF, SS, FS and SF corners using $V_{in} = -0.9$ V: 2.18 MHz, 7.37 MHz, 688.7 KHz, 1.677 MHz and 588.7 KHz. The output voltage frequencies for $V_{in} = 0$ for the same process corners in order are: 2.64 MHz, 8.76 MHz, 836.2 KHz, 1.98 MHz and 719.5 KHz. Comparing these frequencies with the ones obtained for the STRO circuit, it can be observed that the frequency variations due to

process fluctuations are significantly reduced. This reduction is due to using a large value of capacitance using the varactor and cancelling the transistor capacitive effects on the output frequency. However, the variations in frequency are still significant. Therefore, the robustness problem still exists and this will be addressed in Chapter 6. Figure 57 shows the frequency vs. V_{in} plot of the VCFS for the TT, FF, SS, FS and SF corners.

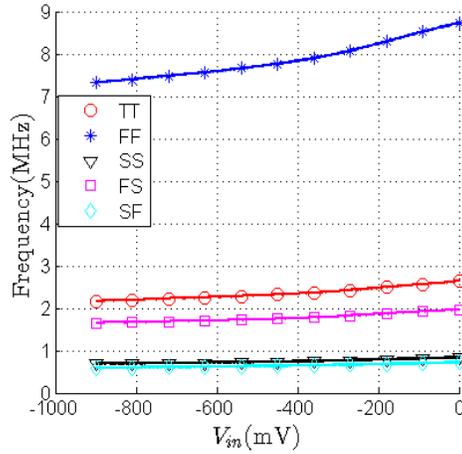


Figure 57 VCFS Frequency vs. V_{in} plot for different process corners.

The frequency vs. V_{in} plot linear for dose measurements corresponding to input values smaller than -400 mV. Therefore, a frequency dependency of dose measurement has been achieved. However, the relationship is not linear for larger inputs and relies on the process corner. For example, Figure 58 shows the non-linearity effect of the frequency vs. V_{in} plot for the SS process corner when the input exceeds -400 mV. Thus, the linearity specification is not met for all dose measurements.

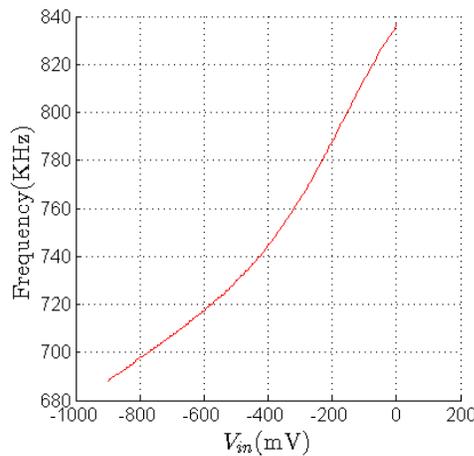


Figure 58 VCFS Frequency vs. V_{in} plot for SS process corner showing non-linearity for $V_{in} > -0.4$ V.

4.5. Level Shifter and SPU Design

The level shifter is required to adjust the height of the pulse train to activate a switch operating in superthreshold. This switch can only operate by receiving a pulse with an amplitude of about 1.2 V, rather than the 300 mV subthreshold level produced by the VCFS. Recent research progress on subthreshold-to-superthreshold level shifters was investigated in Chapter 2. The conventional level shifter of Figure 12, which is a differential cascode voltage switch, operates based on positive feedback provided by the cross-coupled half-latch PMOS transistors. The NMOS pair, M_{N1} and M_{N2} , receive the subthreshold voltage and its inverse respectively. When the input voltage is low, M_{N2} turns ON, pulling V_{a1} low. Subsequently, M_{P1} turns ON, charging V_{a2} and turning M_{P2} (which was ON in the previous cycle when V_{in} was high) OFF. As a result, the output voltage goes high and is charged to the superthreshold voltage supply, V_{DDH} . Similarly, when V_{in} is high, M_{N1} conducts, discharging V_{b2} and turning ON M_{P2} . M_{P2} charges the voltage at b_1 , which turns M_{P1} OFF, and as a result V_{out} is pulled down to zero.

As the above explanation of the level shifter operation suggests, there is a contention between M_{N2} and M_{P2} when V_{in} is low, and among M_{N1} and M_{P1} when V_{in} is high. Since the NMOS transistors are operating in the subthreshold region, their strength is less than their respective PMOS transistor. As a result, switching can become a problem if these transistors are too weak. However, the positive feedback helps add to the strength of the NMOS transistors. However, the NMOS transistors need to be strong enough to kick off oscillation, otherwise the loop gain will not be larger than 1 to create regenerative feedback. Consequently, the NMOS transistors have to be sized much larger than the PMOS ones for the regenerative feedback to be activated.

The bulk connections of the transistors and the dynamic threshold concept can be used to strengthen the NMOS devices without increasing their size. If the NMOS transistors are designed using DTMOS logic, their current drawing ability will increase. Similarly, if the body of the PMOS transistors are connected to a voltage lower than V_{DD} , it could generate positive feedback. It should be understood that the PMOS transistors will also operate in subthreshold temporarily when the circuit is changing states. As a result, there are different configurations that can be used depending on the body connection of the NMOS and PMOS devices. The bulks can be connected to either the substrate, V_{DDL} ,

V_{DDH} or the gate. The optimum configuration can be achieved by using simulations with Cadence.

Simulations show that a robust option is to design NMOS devices using DTMOS, while connecting the PMOS bulks to $V_{DDL}=300$ mV. This structure pulls the 300 mV amplitude pulse up to 1.2 V without sensitivity to process variations. Moreover, using this configuration, the NMOS and PMOS transistors can be sized with minimum width of 160 nm. However, the NMOS and PMOS channel lengths have to be increased to 800 nm and 1 μ m respectively for proper switching for all process corners. Figure 59 shows the schematic for this level shifter. The output inverter used in the level shifter contains an NMOS with minimum width and a PMOS with a channel width of 500 nm while both devices use minimum length. This sizing results in equal strength of both devices operating in saturation, thereby resulting in a switching threshold of half of V_{DDH} (0.6 V).

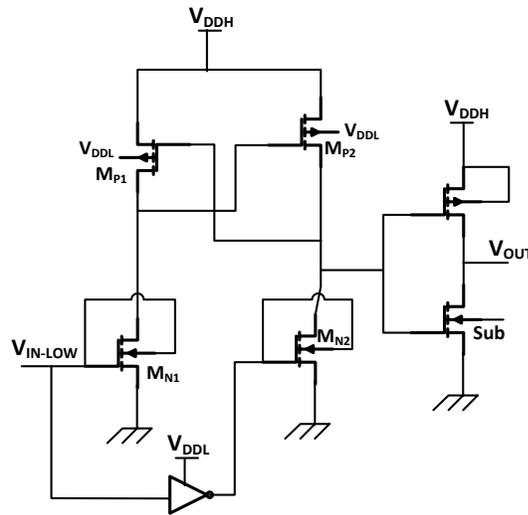


Figure 59 Level shifter schematic used for the SPU.

In order to test the level shifter, it has to be connected to the subthreshold VCFS designed in the previous section. Figure 60 shows the test bench for the SPU that includes the DC shifter, VCFS and the level shifter. Different parts of the SPU are outlined in the test bench for clarity.

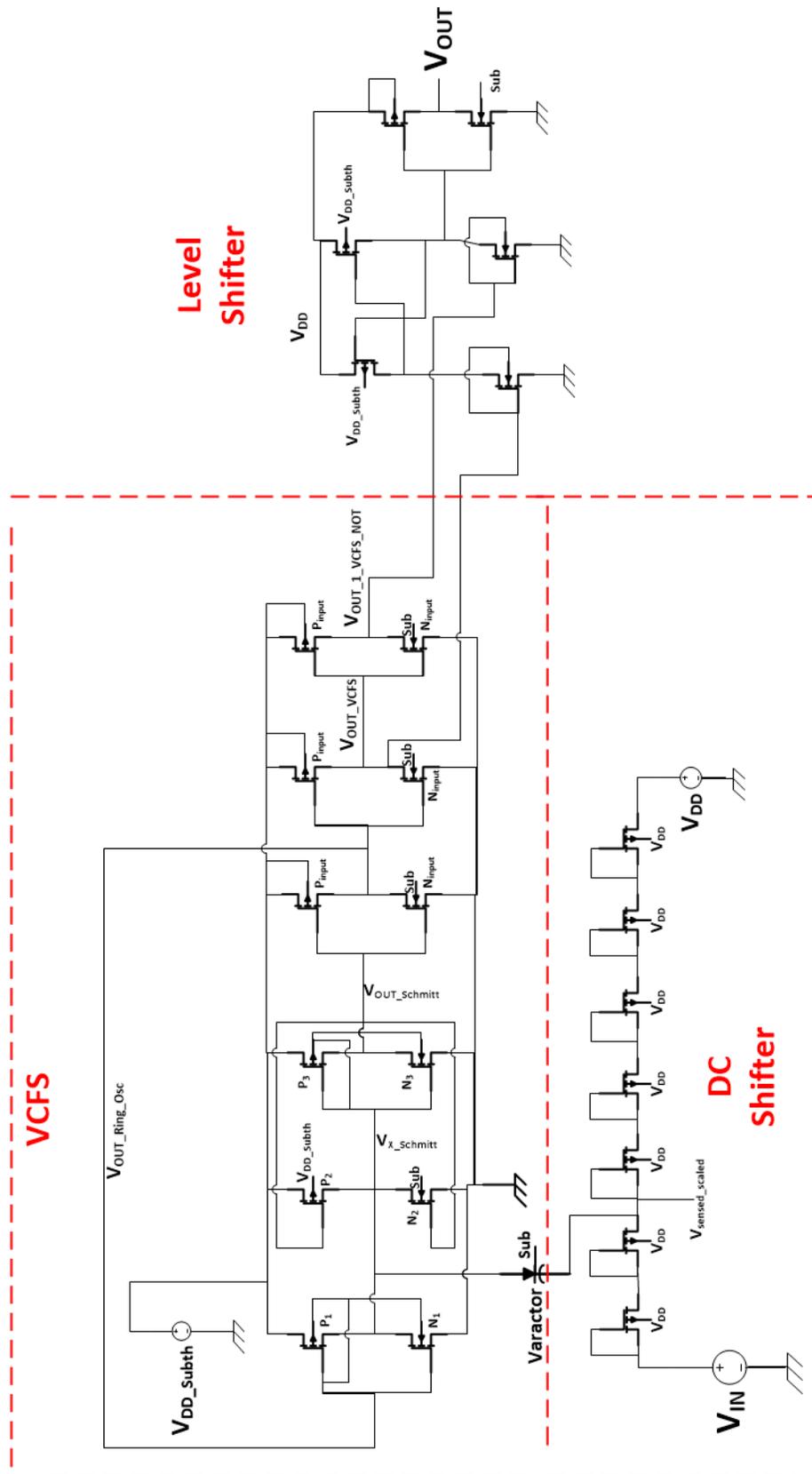


Figure 60 SPU schematic.

Figure 61 shows the level shifted output voltage pulse for input voltages of -900 mV and 0 respectively using the TT process corner. As it can be seen in these plots, the subthreshold pulse is boosted to 1.2 V and both pulses almost have the same frequency and width. The simulation was run for all process corners and different inputs and similar results were achieved. Figure 62 shows the output pulse of the VCFS for SF and FS process corners. The simulation was run for all process corners and different inputs and similar results were achieved. Figure 62 shows the output pulse of the VCFS for SF and FS process corners.

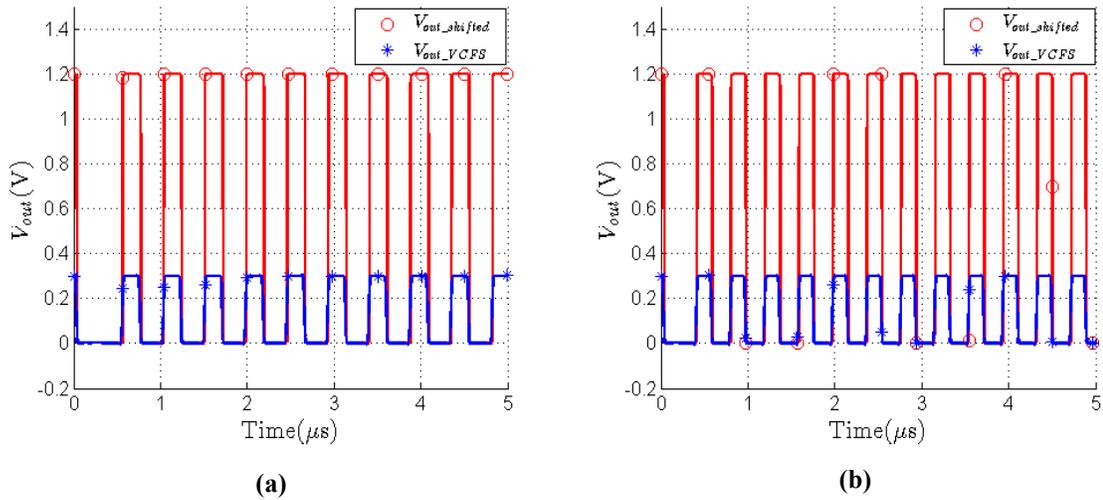


Figure 61 SPU output pulse train with/without level shifter for TT process corner with input of a) -900 mV b) 0.

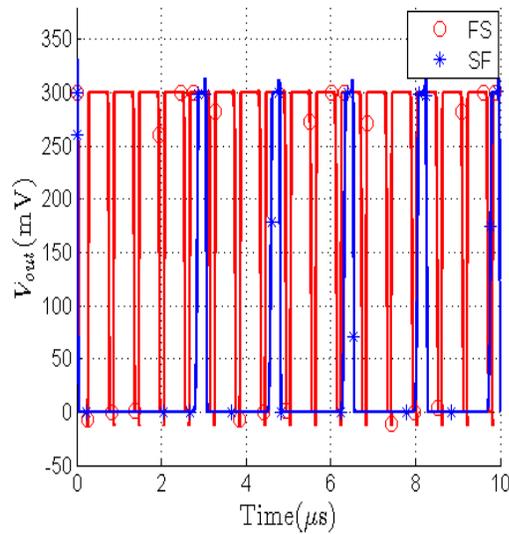


Figure 62 VCFS output pulse train for SF,FS process corners using $V_{in} = -0.9$ V.

As it can be seen, the duty cycle of the pulse can vary from about 10 – 90%. Since the dose measurement is being mapped using frequency, the pulse widths should all be

the same as specified earlier in Table 7. Moreover, a 90% duty cycle can lead to producing a DC signal rather than a pulse after implementation. Thus, the duty cycle specification is not met. Once again, the present SPU is proven to be highly sensitive to process variations, a situation that will be resolved later in this work.

The frequency vs. V_{in} plots for the SPU for different process corners are very similar to those showed in Figure 57 for the VCFS and thus will be omitted. However, the frequency data as well as the bandwidth and resolution for each process corner are summarized in Table 11. A step-size of 70 mV that is equivalent to 2 Gy of dose measurement, is used. As the data in Table 11 shows, the minimum resolution is about 3.5 KHz/Gy, which is within design specifications. However, the resolution and bandwidth change significantly due to process variations. This problem is later addressed in Chapter 6 using DBB circuits for the VCFS.

Table 11 Frequency values, resolution and bandwidth for the SPU for different process corners.

V_{in} (mV)	Frequency				
	TT (MHz)	FF (MHz)	SS (KHz)	FS (MHz)	SF (KHz)
-900	2.11	7.06	671	1.60	563
-830	2.13	7.12	677	1.61	572
-760	2.15	7.18	684	1.63	581
-690	2.17	7.24	690	1.64	588
-620	2.19	7.31	697	1.65	597
-550	2.22	7.38	705	1.67	606
-480	2.24	7.45	713	1.69	615
-410	2.26	7.54	724	1.71	624
-340	2.31	7.65	736	1.74	634
-270	2.35	7.79	750	1.77	646
-200	2.41	7.95	767	1.81	660
-130	2.46	8.12	784	1.85	675
-60	2.51	8.29	801	1.88	691
0	2.63	8.73	837	1.96	722

Bandwidth (KHz)	520	1670	166	360	159
Minimum Resolution (KHz/Gy)	10	30	3.5	5	4.5

The last step is to calculate the power consumption of the signal processing unit for different process corners. The P vs. V_{in} plot for all process corners is shown in Figure 63. These plots show rapid and unexpected changes in the power consumption for the TT and SS process corners. This result is probably due to high sensitivity of the VCFS, and more specifically, the Schmitt Trigger, to process variations. These spikes can be due to short circuit current, that is swiftly increased for some input values such as -400 mV. The short circuit current problem was previously observed for the Schmitt Trigger. Nonetheless, as Figure 63 shows, the circuit could have a maximum power consumption of about $2.50 \mu\text{W}$, which is smaller than the $3.15 \mu\text{W}$ specifications. Thus, an ultra-low power SPU circuit has been designed. Table 12 summarizes the design parameters used for the SPU at schematic level.

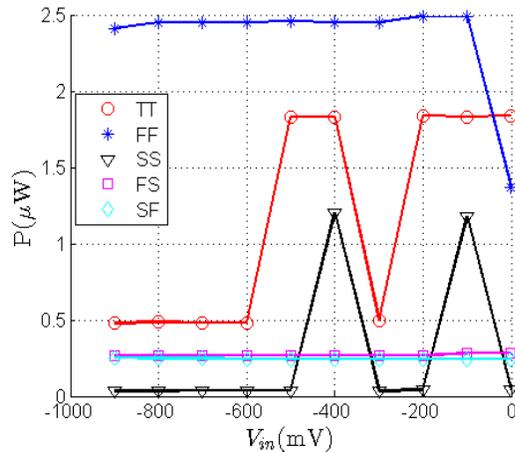


Figure 63 Power consumption of the SPU for different process corners and input voltages.

Table 12 Design parameters used for the SPU at schematic level simulation.

Block	parameters
DC shifter	$W_p=160 \text{ nm}$, $L_p=120 \text{ nm}$
Varactor	RX Width= $3.5 \mu\text{m}$, PC length= 300 nm , # of gates(X)=# of RX repetition= 24 , minimum capacitance= 1.868 pF , maximum ca-

	capacitance=6.701 pF,
Schmitt Trigger	$W_{P1}=1.5 \mu\text{m}$, $W_{P2}=160 \text{ nm}$, $W_{P3}=1 \mu\text{m}$, $W_{N1}=W_{N3}=500 \text{ nm}$, $W_{N2}=640 \text{ nm}$, $L=120 \text{ nm}$
RO output inverters	$W_P=1 \mu\text{m}$, $W_N=500 \text{ nm}$, $L=120 \text{ nm}$
Level shifter	$W_N=W_P=160 \text{ nm}$, $L_N=800 \text{ nm}$, $L_P=1 \mu\text{m}$
Level shifter output inverter	$W_P=500 \text{ nm}$, $W_N=160 \text{ nm}$, $L=120 \text{ nm}$
$V_{DD}=1.2 \text{ V}$, $V_{DD_Subth}=300 \text{ mV}$	

4.6. Summary

The signal processing unit, consisting of the DC shifter, VCFS and level shifter was designed and simulated using Cadence Virtuoso and the 0.13 μm CMOS technology. Each block was analyzed in theory, simulated and optimized separately for different process corners. An original theoretical analysis was completed for the Schmitt Trigger operating in subthreshold. This analysis was used to size the transistors and use dynamic threshold configurations for increasing robustness with the aid of simulations. However, these adjustments were not sufficient and the Schmitt Trigger, as well as the VCFS, showed high sensitivity to process variations. The designed SPU converts the sensed dose to pulses with different frequencies. As the input voltage increases from -900 mV to 0, the frequency also increases. The frequency vs. input voltage plot shows a linear response for $V_{in} < -400 \text{ mV}$. However, linearity is disturbed for larger dose measurements. The minimum resolution is about 3.5 KHz/Gy, which is within the design specification. The SPU consumes a maximum power of 2.5 μW of power that is also within design conditions. However, the frequency band changes significantly due to process variations. The originality of this design lies in the use of dynamic threshold transistors to the VCFS. However, this design still suffers from lack of linearity and robustness. These issues are addressed and solved in Chapter 6 using a novel dynamic body-biasing technique applied to the VCFS.

Chapter 5. Implementation and Testing of the Ultra-Low Power Sensor Signal Processing Unit

In the previous chapter, the signal processing unit was simulated using Cadence and the 0.13 μm CMOS IBM technology kit. It was observed that the input that is a DC voltage ranging from -900 mV to 0 depending on the dose, was converted to a pulse train with a variable frequency and an amplitude of 1.2 V. The next step is to accurately implement this circuit design on a chip. After the chip is implemented, it can be tested using an appropriate procedure. This chapter presents the layout and testing results of the ULP signal processing unit.

5.1. Ultra-Low Power Sensor Signal Processing Unit Implementation

5.1.1 *Adding Enable, Pins, ESD protection and RC Clamp to the SPU*

Before laying out the SPU, some adjustments need to be made to the previous design at schematic level. These adjustments include adding pins, a NAND gate to replace the inverter followed by the ST to add an enable signal and replacing the DTMOS/SBB NMOS devices with triple-well transistors. Moreover, an RC clamp and ESD protections should be added to protect the chip from static charges after implementation.

The enable signal should be added to minimize the power consumption of the SPU. The signal processing unit needs to operate only when new sensing has occurred. This enable signal can be produced by a control block that can be added to the wireless dosimeter in the future. Thus, the inverter that receives the Schmitt Trigger output can be replaced by a NAND gate. This gate has one of its inputs connected to the ST circuit output and the other one to the enable signal. If enable is high, the Schmitt Trigger output is inverted, otherwise the output of the VCFS is zero and oscillation will not occur.

Figure 64 shows the NAND gate schematic test bench and the resulting voltage transfer characteristic by sweeping V_{in} from 0 – 300 mV. As it can be seen, the output is

identical to that of an inverter with a switching threshold of 150 mV. The NMOS transistors are minimum sized, while the PMOS devices are using $W = 1 \mu\text{m}$. One of the PMOS transistors is a SBB configuration to increase its speed and avoid a larger channel width as shown in Figure 64.

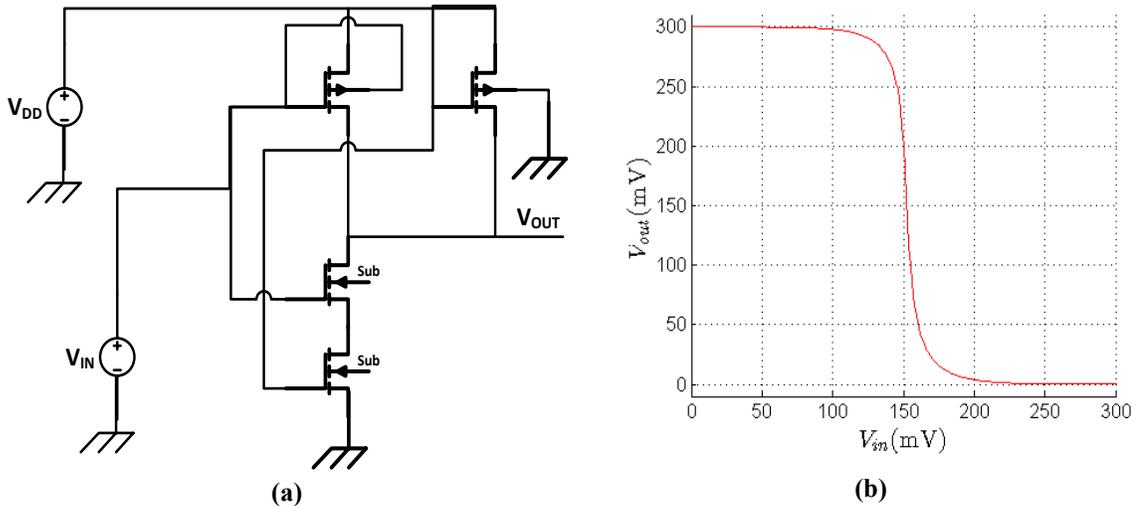


Figure 64 NAND gate used for enable signal a) test bench b) DC voltage transfer characteristic.

All pins that are required for testing need to be added to the SPU for layout. Moreover, each pin that is connected to a transistor gate needs an ESD protection. The superthreshold V_{DD} pin has to be connected to an RC clamp in addition to ESD, to prevent static charge damages to the chip. Since all these connections add to the parasitics of the circuit, not all nodes can be monitored for testing. However, using simulations, the maximum number of nodes and pins can be collected for testing. The SPU pre-layout schematic can be seen in Figure 65, while Figure 66 shows the pins, ESD and RC clamp connections. Triple-well NMOS transistors have been used for the DT NMOS devices as shown in the schematic.

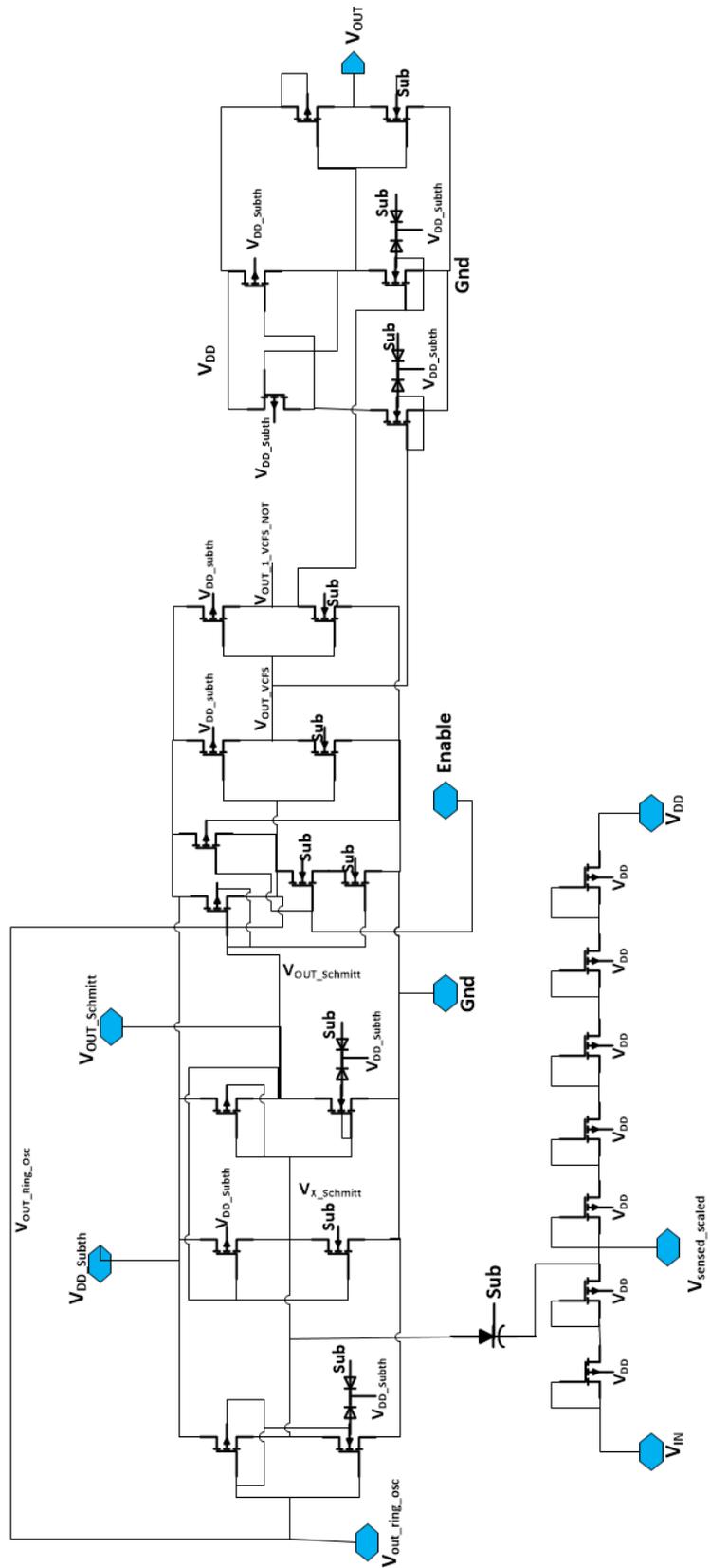


Figure 65 SPU pre-layout schematic.

circuit proceeded to fabrication in order to verify the extent of process variations and validate the soundness of subthreshold models and overall design methodologies.

5.1.2 SPU Layout

The layout is a difficult task involving multiple steps and challenges. However, it is conducted following five major steps:

1. Import the devices from schematic and connect them using minimum number of metal layers according to layout rules for the 0.13 μm CMOS process.
2. Run Caliber DRC until no errors, except ones related to metal fill, appear. If there are errors, step 1 has to be repeated.
3. Run Assura LVS to check layout vs. schematic matching. If there are any errors, steps 1 and 2 have to be repeated in order.
4. Complete the metal fill and re-run Caliber DRC and Assura LVS tests respectively until they pass.
5. Extract the layout to create the extracted view. The extracted view of the circuit can be simulated and tested for assurance with the additional parasitics capacitances.

The final layout is sent to IBM Mosis via CMC for fabrication after completing the above steps. Layout considerations depend on factors such as region of operation, frequency of the circuit channel width and length and adopted process. A number of devices used in the layout, such as the DC shifter PMOS transistors, are minimum sized. Since the minimum size devices have no contacts in their layout view in Cadence for this technology, the contacts had to be added manually. The routing procedure should also be completed manually to use a minimum level of metal layers and keep the design simple and easy to debug. This was difficult at parts, as there are many design rules regarding the minimum space between different metal layers as well as metal layer areas, etc. However, since the design area that was granted for the chip (1 mm \times 1.5 mm), is much larger than what is required, the routing was much simpler compared to industrial VLSI applications. Another important concern was to keep the metals as thin as possible at most parts to avoid additional parasitics. However, for some sections of the circuit, the area of the metals had to be enlarged to make sure there is a valid connection. Furthermore, the con-

tacts used to connect different metal layers were used in a group of at least 4 to make sure a connection exists after fabrication. One of the most important layout concerns was the location of the bon-pads. The bon-pads used for the input/output (I/O) pins had to be placed properly to ease the testing procedure using probes. In general, the placement of the devices is important, as it helps simplify the routing process. The final layout was completed using a space of $555.53 \mu\text{m} \times 572.55 \mu\text{m}$ using 9 pins as shown in Figure 68. Figure 69 to Figure 72 show the layout of different parts of the SPU in more detail.

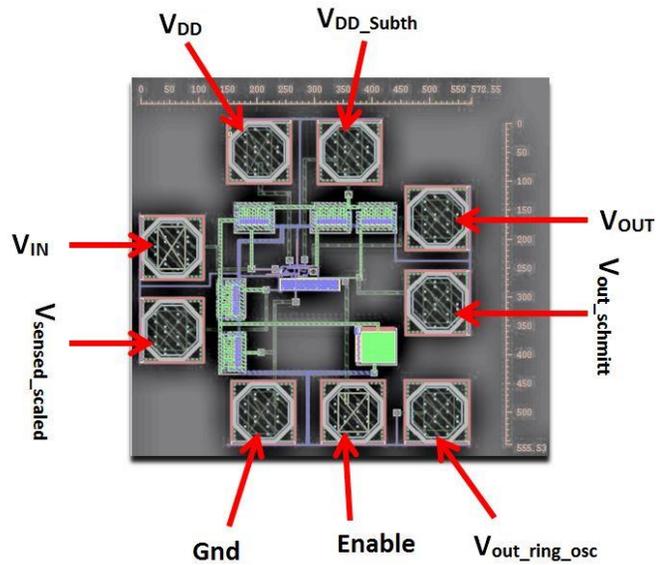


Figure 68 SPU final layout using $555.53 \mu\text{m} \times 572.55 \mu\text{m}$ chip space.

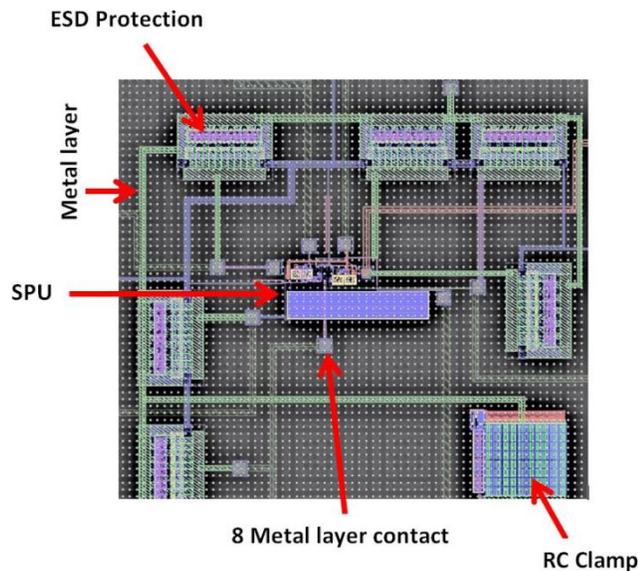


Figure 69 SPU, ESD and RC Clamp layout.

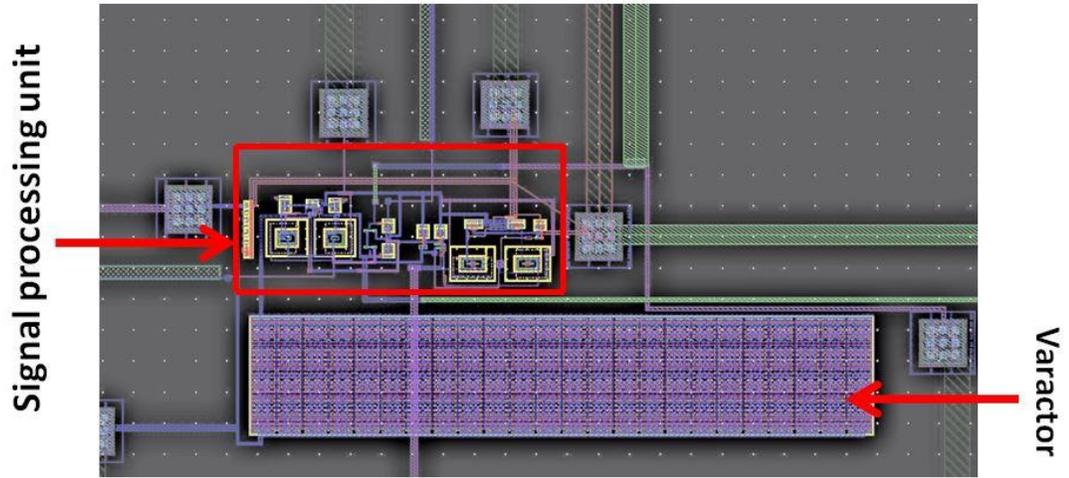


Figure 70 SPU and Varactor layouts.

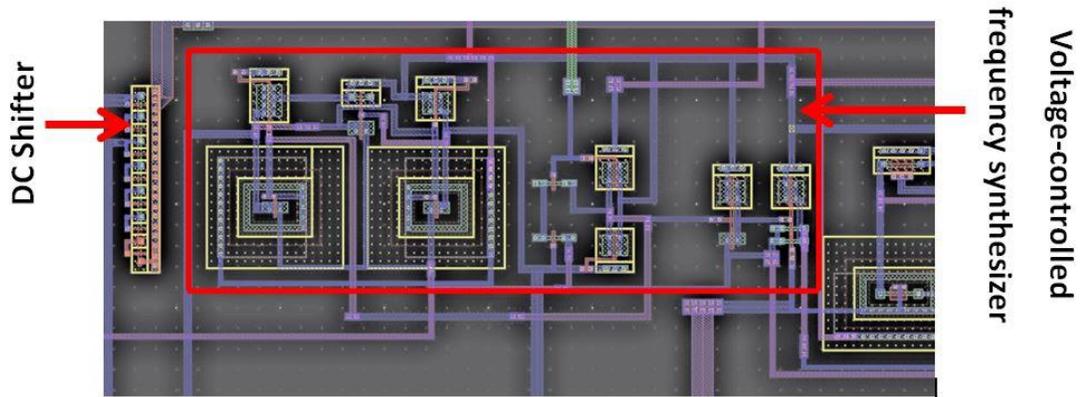


Figure 71 DC Shifter and VCFS layouts.

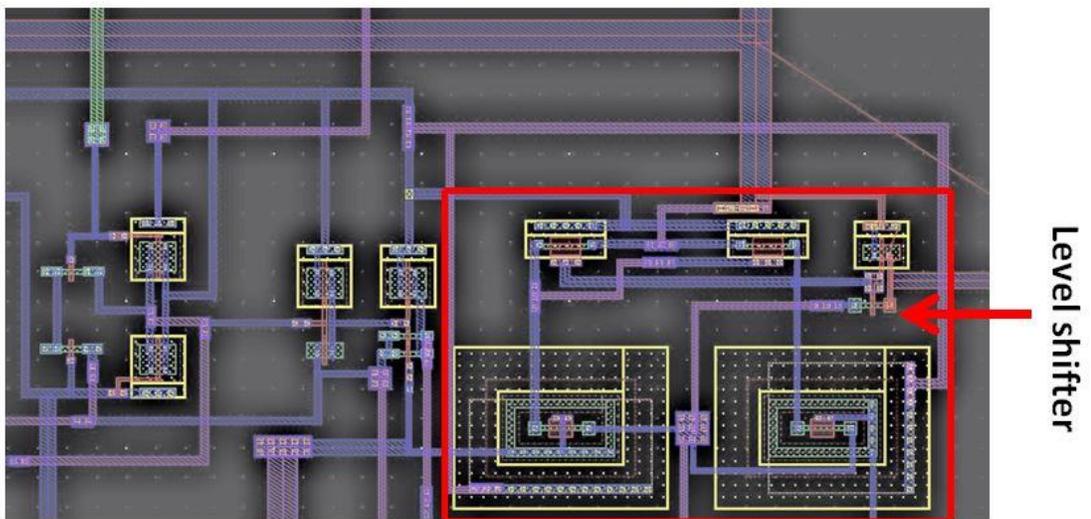


Figure 72 Level shifter layout.

5.1.3 SPU Extracted View Simulation Results

The SPU is extracted as shown in Figure 73 and Figure 74. The next step is to repeat the transient simulations of 4.4 and obtain the Frequency vs. V_{in} plot for different process corners using extracted view and including layout parasitics.

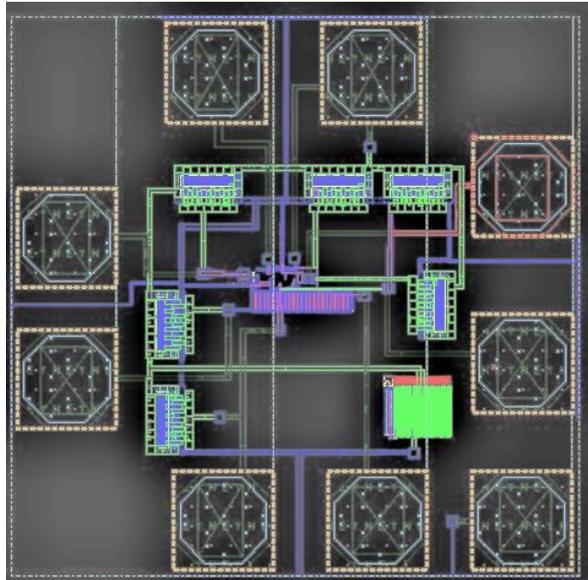


Figure 73 SPU Extracted view 1.

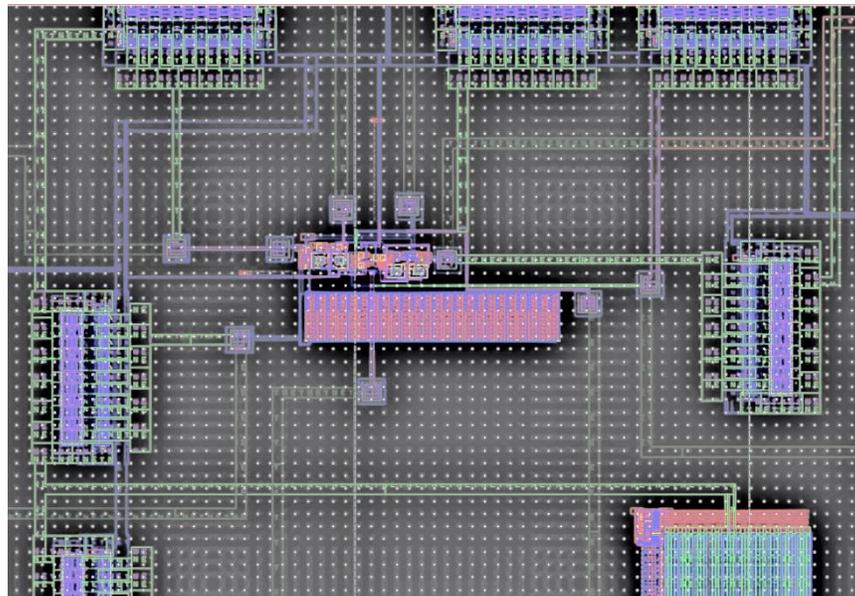


Figure 74 SPU Extracted View 2 (zoomed in SPU).

The test bench of Figure 67 is used for completing post-layout SPU simulations. Figure 75 shows the Frequency vs. V_{in} plots for the TT, FF, SS, SF and FS process corners after sweeping the input voltage from -900 mV to 0.

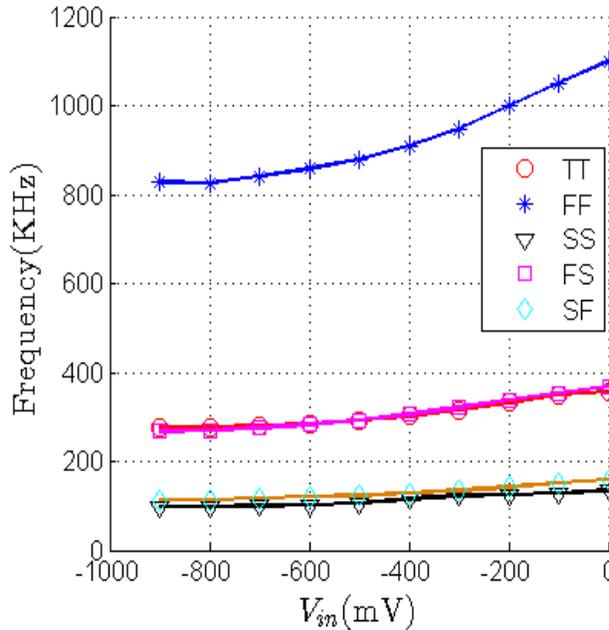


Figure 75 SPU extracted simulation, Frequency vs. V_{in} plot for different process corners.

As it can be seen in the above plots, there is almost no change in frequency for $-900 \text{ mV} < V_{in} < -800 \text{ mV}$, which is about 2.85 Gy of dose measurement. Comparing the frequency values of the above plots with the pre-layout results of 5.1.1, further decrease in frequency bands can be seen as a result of additional parasitics. Similar to the results of 5.1.1 and 4.4, the frequency bands change depending on the process corner. This problem is addressed and solved in Chapter 6.

Post-layout transient simulations show that for the SS and FS process corners, the output is almost a DC signal for input voltages greater than -500 mV and -200 mV respectively. The duty cycle of the pulses appear to change significantly due to process variations. A similar problem was observed for schematic level simulations. Figure 76 shows the output pulse train for the SS and FS process corners using $V_{in} = -500 \text{ mV}$ and $V_{in} = -200 \text{ mV}$ respectively. The output pulse for both process corners getting close to a DC value as the duty cycle is reaching a 100%. This occurs due to the slowness of the PMOS

transistors of the ring oscillator, which are responsible for the zero cycle of the pulse, in the SS and FS process corners.

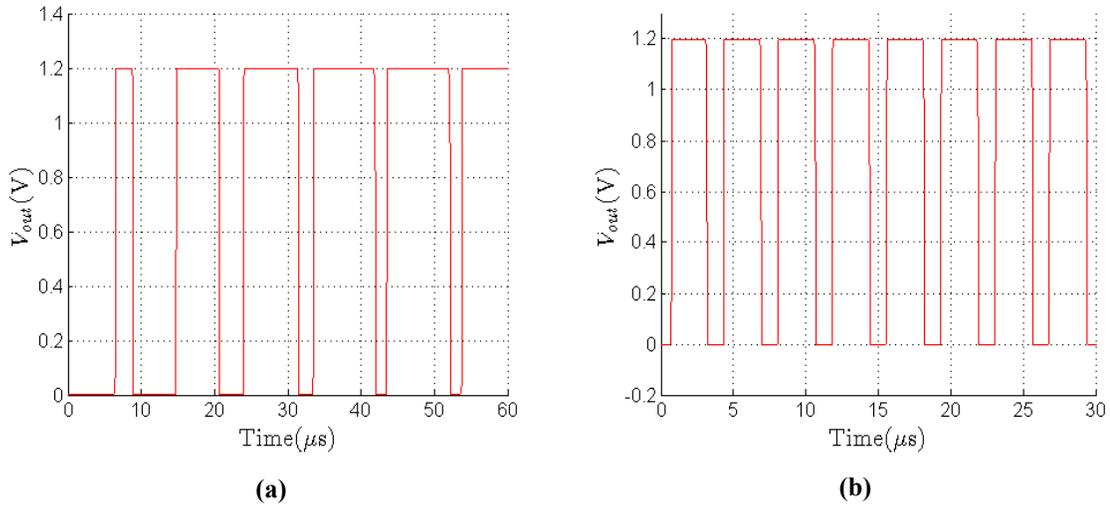


Figure 76 SPU extracted simulation, V_{out} for TT process corner for a) $V_{in} = -900$ mV b) $V_{in} = 0$.

5.2. Testing Results of the SPU

Testing of the SPU chip is completed using three DC voltage sources for V_{DD} , V_{DD_Subth} and V_{in} as shown in Figure 77. Moreover, an oscilloscope for monitoring V_{out} , a probe station (if the chip is not bond-wired) and different types of wires are required. Figure 78 shows some of the chips used for testing glued on glass for testing using probe station as well as bond-wired ones on a breadboard.

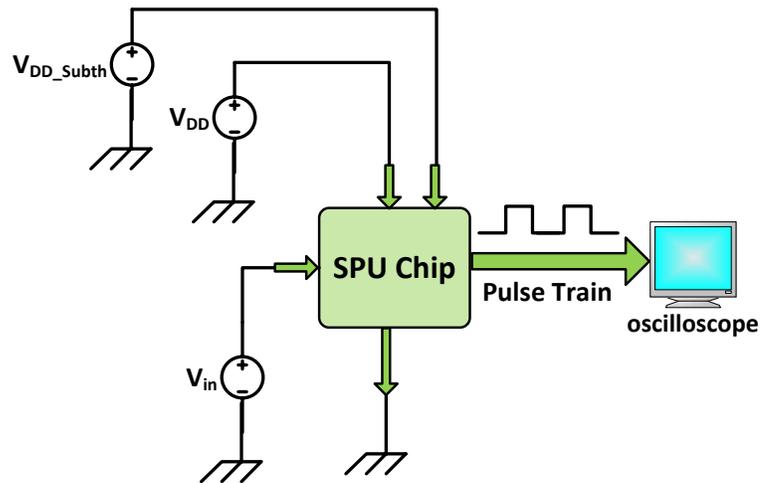


Figure 77 Testing setup for the SPU chip.

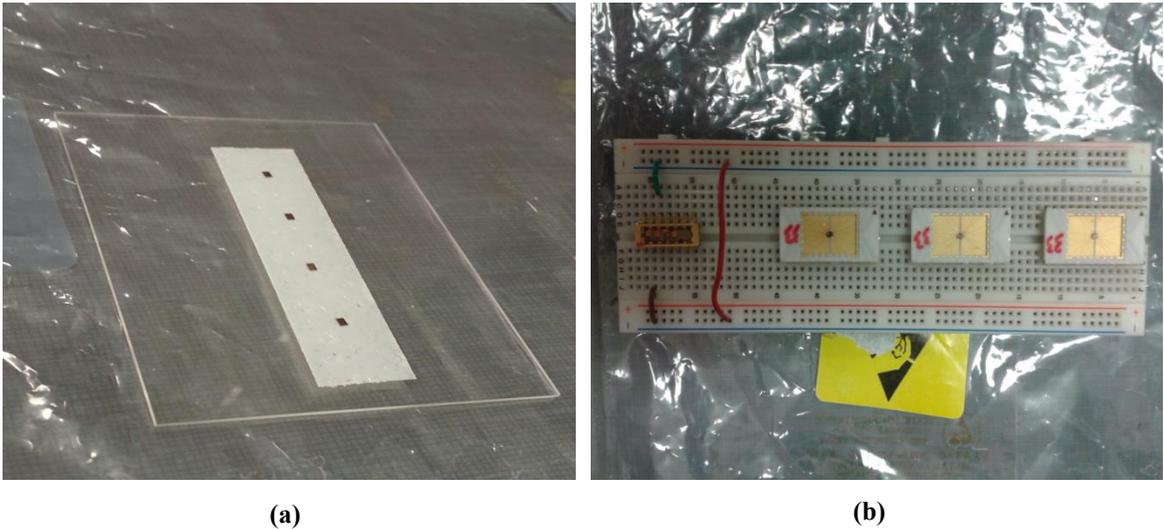


Figure 78 SPU chips a) glued on glass for testing using probes b) bond-wired and placed on bread-board for testing.

A total of 10 chips were tested, half of them bond-wired and the other half using probes. The bond-wiring method eases the testing procedure, as using probes is lengthy and difficult. Moreover, probes can damage the chip if not used very carefully. However, bond-wiring introduces additional parasitics to the circuit.

After completing the testing, circuit functionality was observed for half of the chips as shown in Table 13. The SPU generated a pulse train with an increasing frequency for input voltages in the range of -900 mV to -600 mV. The output pulse for one of the test cases is presented in Figure 79. Comparing the testing result frequencies with those of post layout simulations in the frequency vs. V_{in} plot of Figure 75, interesting conclusions can be drawn. It can be observed that the testing results are very similar to those for SF and FS process corners. Hence, the feasibility of the subthreshold model for the 0.13 μm technology is demonstrated. The SF and FS process corners can also result in the highest variations in the pulse train duty cycle, which could have partly been the reason for lack of oscillation for the other half of the chips. These chips produced a DC voltage of 1.2 V for all input voltages despite using different values of V_{DD} and V_{DD_Subth} . A problem associated with the circuits that produced a pulse train was stability. The pulses were noticeably noisy and disappeared after some time by converging to a DC signal. For some of the input voltages in Table 13, the frequency could not be recorded due to this

reason. Therefore, the circuit did not have a stable response and it seemed that the loop gain was not enough for oscillation. One reason could be sizing of the transistors of the VCFS. These transistors were sized close to minimum width and length. Consequently, the loop gain and current generated was not enough to overcome the overall capacitance and parasitics to produce oscillation. Furthermore, these transistors are very sensitive to process variations as previously observed in schematic level simulations as well. Testing results show that the VCFS sensitivity to process variations is somewhat more severe with the additional parasitics, resulting in no oscillation for some of the chip samples. However, through testing results, the validity of sensitivity to process variations associated with subthreshold circuits previously investigated at simulation level is confirmed.

Table 13 SPU chips test results.

	Frequency (KHz) for $V_{in}=-900$ mV	Frequency (KHz) for $V_{in}=-800$ mV	Frequency (KHz) for $V_{in}=-700$ mV	Frequency (KHz) for $V_{in}=-600$ mV
Bond-wired chips				
Chip #1	65.6	92.1	110.4	
Chip #2	55.5		91.7	122.3
Probed chips				
Chip #1	100.9	141.1	205.8	
Chip #2	413.4		621.5	688.4
Chip #3	301.8	433.5	506.8	587.3

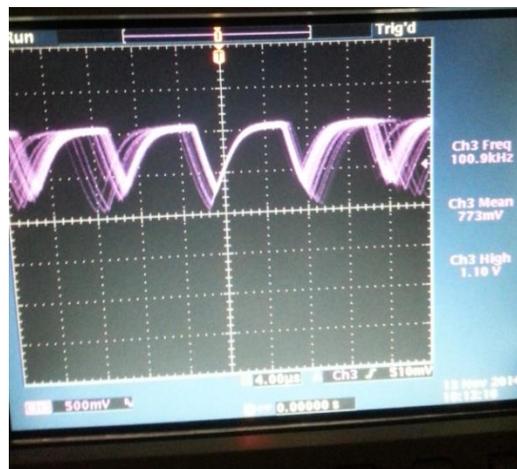


Figure 79 V_{out} for one of the SPU Chip testing samples (Probed, Chip #1, $V_{in}=-900$ mV).

Another problem with the design is the body biasing of the DC shifter transistors. The bulks of all these PMOS devices were connected to V_{DD} . However, their source and drain voltages could vary anywhere between $-0.9\text{ V} - 1.2\text{ V}$ depending on V_{in} . This could lead to forward biasing of the B-S diode, which could cause breakdown of the bond. The V_{sensed_scale} pin was monitored for some of the chips. The DC shifter produced an almost constant and very noisy voltage between -50 and 50 mV for all input voltages.

The voltage source used for V_{DD_Subth} , drew a large amount of current between $100\text{ }\mu\text{A} - 300\text{ }\mu\text{A}$ during testing. This means that there was a short circuit in one of the ring oscillator branches. If an NMOS or PMOS transistor within the VCFS was fabricated as too slow or fast, it could have caused problems for the ST, thereby disturbing the oscillation. In chapter 4, the Schmitt Trigger transistors were sized so that the circuit produced a hysteresis for all process corners. However, this resulted in smaller hysteresis widths for some process corners. Consequently, the circuit became more prone to noise. These issues are solved in the next chapter to design an ULP and robust SPU using the necessary enhancements.

5.3. Summary

In this chapter, layout and testing of the ultra-low power SPU were completed after designing at schematic level in Chapter 4. The circuit was simulated using the extracted view with the additional layout parasitics. After implementation, 10 chips were tested. It was observed that half of the samples produced a pulse train for $-0.9\text{ V} < V_{in} < -0.6\text{ V}$ with variable frequencies. Results were similar to those obtained for the post-layout simulations using the SF and FS process corners. Therefore, the feasibility of the design model used for subthreshold operation and designing the ULP SPU is confirmed. However, it was observed that the circuit did not oscillate for the remainder of the chips by producing a constant DC voltage at 1.2 V . The problems associated with the testing were found to be small sizing of the VCFS devices, body biasing of the DC shifter transistors and high sensitivity to process variations. These problems are addressed and solved in the next chapter to implement a robust and ultra-low power sensor SPU for a wireless dosimeter. Hence, the third objective of this thesis work is completed.

Chapter 6. Dynamic Body Biasing to Decrease Frequency Sensitivity of the VCFS Operating in the Subthreshold Region to Process Variations

As explained in previous chapters, high sensitivity to process variation is the main challenge associated with subthreshold circuits. The previously designed VCFS operating in the subthreshold region produces different frequencies depending on process fluctuations. For example, for a dose measurement of -900 mV, the output pulse frequency could vary from 588.7 KHz to 7.37 MHz. In this chapter, two novel circuits are proposed for dynamic body biasing of NMOS and PMOS transistors. This DBB technique significantly reduces the subthreshold current's sensitivity to process variations. The DBB circuits are further applied to the VCFS. Using this adjustment and other enhancements to the previous approach, a robust and ultra-low power SPU is designed for wireless dosimetry.

6.1. DBB Technique for Process Variation Tolerance

In Chapter 3, it was observed that body biasing of NMOS and PMOS transistors has a linear effect on their threshold. Increasing V_{bs} of NMOS transistors decreases their V_{th} resulting in greater current. For PMOS devices, the opposite holds true. Therefore, if the body voltage of transistors can be biased dynamically in response to process variations, the subthreshold current can be stabilized. For NMOS transistors, V_{bs} should decrease for the fast process corner and increase for the slow. For PMOS devices, the opposite mechanism has to be applied. This concept was previously adopted by some researchers to improve the robustness of subthreshold circuits [6] [31]. However, the designed circuits are assumed to be at least partly independent of process variations using large transistor sizing or using other assumptions. Moreover, the designed schemes use both NMOS and PMOS transistors for dynamic body biasing of each device. Since NMOS and PMOS transistors

have the opposite behavior with regards to body biasing, this can decrease the feasibility of the previous proposed methods.

Figure 80 shows the block diagram of the DBB technique. The NMOS body is biased using an NMOS circuit, while the PMOS bulk is connected to a PMOS body-biasing scheme. These body-biasing circuits are sensitive to process variations, but result in enhanced robustness of the circuit operating in the subthreshold region.

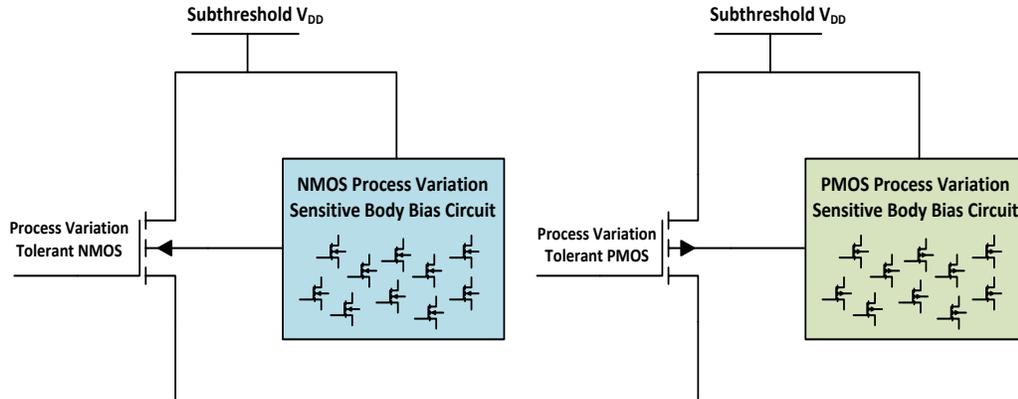


Figure 80 Block diagram of proposed dynamic body-biasing technique for decreasing current sensitivity of NMOS / PMOS transistors to process variations.

The proposed technique for reducing current sensitivity to process variations for MOSFETs operating in the subthreshold region is as follows:

1. Find the NMOS transistor size that can potentially become process variation tolerant using DBB. Keep L minimum and sweep for W to find the minimum channel width where three different body voltages can yield a single current for all process corners (typical, fast, slow). Repeat the same simulation for different channel lengths and minimum W .
2. Repeat step 1 for PMOS.
3. Design an NMOS circuit that can produce the three different body voltages found in step 1 for the respective NMOS transistor at T, F and S process corners. There are a number of steps and conditions to design the NMOS dynamic body-biasing circuit (NDBB). These steps are explained in detail in 6.3.

4. Apply the output of the NDBB circuit to the NMOS transistor of step 1. Run DC simulations to find the current plot for T, F and S process corners. The current should almost merge for all corners.
5. Repeat steps 3 and 4 for PMOS. The details of design conditions and steps of the PMOS dynamic body-biasing circuit (PDBB) are explained in 6.3.

The above steps are completed in order to reduce process variations for circuits operating in subthreshold. Furthermore, the NDBB and PDBB circuits are applied to the VCFS to improve the robustness of the SPU. It should be noted that all simulations are done using $V_{DD_Subth}=300$ mV for enhanced robustness as discussed in Chapter 3.

6.2. Sizing NMOS and PMOS Transistors to be Potentially Process Variation Tolerant using Dynamic Body Biasing

The test bench of Figure 81 (a) is used for the sizing of NMOS for potential enhanced robustness. The channel length is set to minimum and $V_{gs}=V_{ds}=0.3$ V. Sweeping V_{body} from 0 to 300 mV for different process corners, V_{bs} vs. I_{ds} plots for different channel widths is obtained. The goal is to find the minimum W where the three current plots for T,F and S process corners intersect using three body voltages. Simulations show that the minimum channel width where this occurs is $4 \mu\text{m}$ for NMOS as demonstrated in in Figure 81 (b).

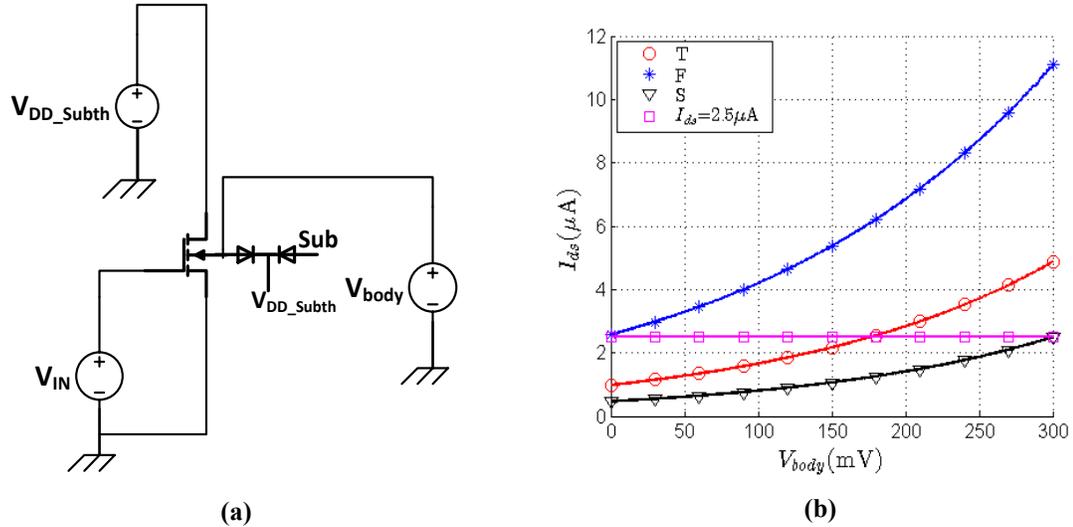


Figure 81 a) Test bench used for DBB NMOS sizing b) V_{body} vs. I_{ds} plot using ideal body voltage source for T, F and S process corners for NMOS using $W=4 \mu\text{m}$, $V_{gs}=V_{ds}=0.3$ V.

As it is shown in Figure 81 (b), using body voltages of 0, 176.6 mV and 300 mV for the F, T and S corners yields a single current of about 2.5 μA . Thus, if minimum channel length is used, the minimum W for process variation tolerant NMOS design is 4 μm . The same simulation was completed for different channel lengths using minimum W . As seen previously in Chapter 3, larger channel length leads to smaller sensitivity to process variations. However, simulations show that the changes in the current of NMOS transistors using larger channel lengths are not large enough to overcome process variations. Increasing the channel width and length at the same time produced the same result. Therefore, minimum channel length and $W = 4 \mu\text{m}$ is chosen for the potential process variation tolerant NMOS device. Hence, the first step of the DBB design scheme is completed.

A test bench similar to that of Figure 81 (a) can be used to repeat design step 1 for PMOS. Setting the channel length to minimum, $V_{sg} = V_{sd} = 0.3 \text{ V}$ and sweeping V_{body} from 0 to 300 mV, the minimum W is found to be 2.5 μm as shown in Figure 82. Using this channel width, a current of about 1 μA is obtained using V_{body} of 300m V, 137.34 mV and 0 for the F, T and S process corners respectively.

Due to the same reasoning previously stated for NMOS, the channel length for PMOS cannot be increased for dynamic body biasing. Therefore, the potential process variation tolerant PMOS device using the 0.13 μm technology has a channel width of 2.5 μm and minimum L .

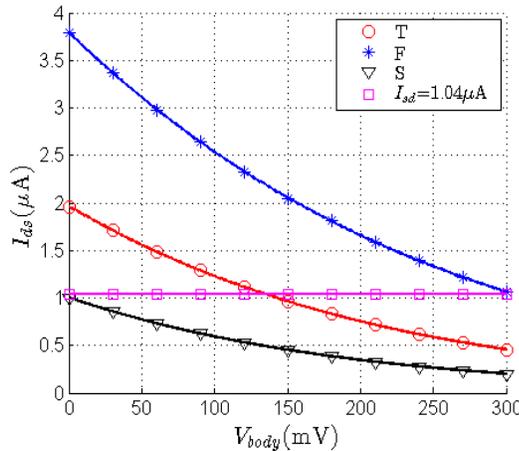


Figure 82 V_{body} vs. I_{sd} plot using ideal body voltage source for T, F and S process corners for PMOS with $W=2.5 \mu\text{m}$, $V_{sg} = V_{sd} = 0.3 \text{ V}$.

6.3. Dynamic NMOS & PMOS Body-Biasing Circuits

6.3.1 Dynamic Body Biasing and Process Variations in Theory

Before designing the dynamic body-biasing circuits, a potential scheme using this technique is investigated in theory. To precisely analyze the effect of process variations on transistors operating in the subthreshold region, statistical study of random processes conducted with process manufacturing is required. However, since this is beyond the scope of this thesis, a more approximate analysis is done as follows: Assume I_{D1} is the current of an NMOS transistor at the typical process corner using a body voltage of V_{bs1} . Moreover, take I_{D2} is the current of the same size transistor that is either faster or slower than the typical device using V_{bs2} as its body voltage. We have:

$$I_{D1} = \mu_1 C_{ox} \frac{W}{L} v_T^2 e^{1.8} e^{\frac{V_{gs} - V_{th0} + \lambda_{bs} V_{bs1}}{nv_T}} \left(1 - e^{-\frac{V_{ds}}{v_T}} \right) \quad (6-1)$$

$$I_{D2} = \mu_2 C_{ox} \frac{W}{L} v_T^2 e^{1.8} e^{\frac{V_{gs} - V_{th0} \pm \Delta V_{th0} + \lambda_{bs} V_{bs2}}{nv_T}} \left(1 - e^{-\frac{V_{ds}}{v_T}} \right) \quad (6-2)$$

As it can be seen in equation (6-2), the mobility and threshold voltage of the transistor is changed due to process variations. In order to overcome these changes, we should have $I_{D1} = I_{D2}$ using V_{bs2} . Thus, we have:

$$\mu_1 e^{\frac{V_{gs} - V_{th0} + \lambda_{bs} V_{bs1}}{nv_T}} = \mu_2 e^{\frac{V_{gs} - V_{th0} \pm \Delta V_{th0} + \lambda_{bs} V_{bs2}}{nv_T}} \quad (6-3)$$

$$\ln(\mu_1) + \frac{V_{gs} - V_{th0} + \lambda_{bs} V_{bs1}}{nv_T} = \ln(\mu_2) + \frac{V_{gs} - V_{th0} \pm \Delta V_{th0} + \lambda_{bs} V_{bs2}}{nv_T} \quad (6-4)$$

Isolating equation (6-3) for V_{bs2} leads to:

$$V_{bs2} = \frac{nv_T (\ln(\mu_1) - \ln(\mu_2)) + \lambda_{bs} V_{bs1} \mp \Delta V_{th0}}{\lambda_{bs}} \quad (6-5)$$

Equation (6-5) tells us that a body-biasing circuit is required, where V_{bs} is adjusted dynamically in response to changes in the mobility and threshold voltage. Consequently, a body-biasing circuit affected by process variations can be used to adjust the body voltage of the transistor and stabilize its current. However, this body-biasing circuit needs to be purely NMOS for NMOS and consist of only PMOS transistor for PMOS devices. This is due to the fact that NMOS and PMOS transistors have different current behaviors

in response to body biasing. The body-biasing circuits need to produce a V_{bs} similar in form to V_{bs2} in equation (6-5).

6.3.2 NDBB Circuit Design

The NDBB should satisfy the following conditions to stabilize the current of NMOS transistors with $W=4\ \mu\text{m}$, $L=120\ \text{nm}$ in response to process variations:

1. Consist of only NMOS transistors.
2. Cover a range of 0-300 mV for fast to slow process corners. The body voltage should be 0, 176.6 mV and 300 mV for the F, T and S corners.
3. Yield higher voltages for slow processes and lower output levels for faster counterparts.
4. Its output should have a mathematical form similar to equation (6-5).

Since a wide range of change in voltage is required for body biasing of the transistor, an inverter could be a possible body-biasing circuit. However, there are two major problems with the conventional CMOS inverter: firstly, it consists of both NMOS and PMOS transistors. The second problem with the CMOS inverter is its high slope during switching. Hence, the output could become unpredictable or change dramatically with a small change at the input.

A fully NMOS inverter can be used, where the pull-down device receiving the input at the gate is an NMOS. The NMOS inverter's pull-up network consists of a gate-drain (enhancement) or gate-source (depletion) connected NMOS load. In addition to having a lower switching slope, the NMOS inverter does not charge the output to V_{DD} for typical or fast process corners. If sized properly, when the NMOS transistors are slower than typical, the switching threshold moves up. Consequently, the output could be charged up to V_{DD} for the S process corner. In addition, using proper transistor sizing, the switching threshold becomes smaller for faster implementations, thereby charging the output to a voltage level less than typical. Hence, the NMOS inverter seems to be a potential circuit for body biasing of NMOS transistors, as it satisfies all NDBB conditions. Since a single NMOS inverter does not provide the required range of change in voltage, a chain of 3 inverters in series is adopted as shown in Figure 83.

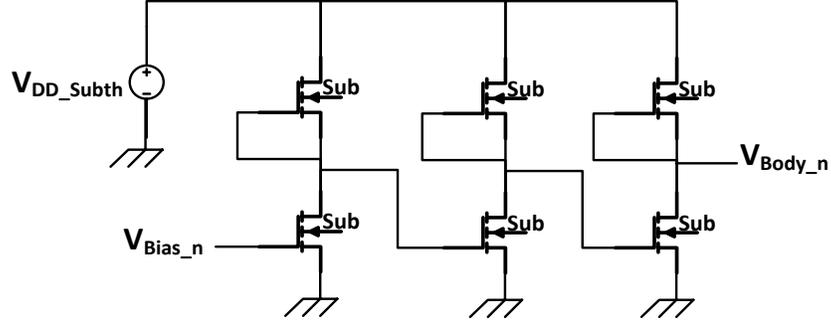


Figure 83 NMOS dynamic body-biasing (NDBB) circuit.

The depletion load was used for the inverter, since simulations showed that the enhancement load could not satisfy the second condition for the body-biasing circuit (unless sized very large in width).

The explained qualitative analysis shows that the NMOS inverters satisfy the first three conditions for an NMOS body-biasing circuit. However, an approximate mathematical analysis also needs to be completed to confirm the fourth NDBB condition. Assume I_{Da} , I_{Db} and I_{Dc} are the currents of the first, second and third inverters and V_{bias} is the bias voltage applied to the first inverter. Let V_X , V_Y and V_{body} represent the output of the first, second and third inverters respectively. All the inverters are sized similarly. The transistor closer to V_{DD} in each inverter is shown using subscript 2 for different parameters, and the other device with subscript 1. Lastly, the $\left(1 - e^{-\frac{V_{ds}}{v_T}}\right)$ term in the current equation is omitted for simplicity of the calculations. Hence, we have:

$$\begin{cases} I_{Da} = \mu_1 C_{ox1} \frac{W_1}{L} v_T^2 e^{1.8} e^{\frac{V_{bias} - V_{th01}}{nv_T}} \\ I_{Da} = \mu_2 C_{ox2} \frac{W_2}{L} v_T^2 e^{1.8} e^{\frac{-V_{th02} - \lambda_{bs2} V_X}{nv_T}} \end{cases} \quad (6-6)$$

$$\begin{cases} I_{Db} = \mu_1 C_{ox1} \frac{W_1}{L} v_T^2 e^{1.8} e^{\frac{V_X - V_{th01}}{nv_T}} \\ I_{Db} = \mu_2 C_{ox2} \frac{W_2}{L} v_T^2 e^{1.8} e^{\frac{-V_{th02} - \lambda_{bs2} V_Y}{nv_T}} \end{cases} \quad (6-7)$$

$$\begin{cases} I_{D3} = \mu_1 C_{ox1} \frac{W_1}{L} v_T^2 e^{1.8} e^{\frac{V_Y - V_{th01}}{nv_T}} \\ I_{D3} = \mu_2 C_{ox2} \frac{W_2}{L} v_T^2 e^{1.8} e^{\frac{-V_{th02} - \lambda_{bs2} V_{body}}{nv_T}} \end{cases} \quad (6-8)$$

From equation (6-6) we have:

$$\mu_1 C_{ox1} W_1 e^{\frac{V_{bias} - V_{th01}}{nv_T}} = \mu_2 C_{ox2} W_2 e^{\frac{-V_{th02} - \lambda_{bs2} V_x}{nv_T}} \quad (6-9)$$

Isolating (6-8) for V_x , we have:

$$\ln(\mu_1 C_{ox1} W_1) + \frac{V_{bias} - V_{th01}}{nv_T} = \ln(\mu_2 C_{ox2} W_2) - \frac{V_{th02} + \lambda_{bs2} V_{body}}{nv_T}$$

$$V_x \approx \frac{nv_T (\ln(\mu_2 C_{ox2} W_2) - \ln(\mu_1 C_{ox1} W_1)) + V_{th01} - V_{th02} - V_{bias}}{\lambda_{bs2}} \quad (6-10)$$

From equation (6-7) we have:

$$\mu_1 C_{ox1} W_1 e^{\frac{V_x - V_{th01}}{nv_T}} = \mu_2 C_{ox2} W_2 e^{\frac{-V_{th02} - \lambda_{bs2} V_y}{nv_T}} \quad (6-11)$$

Isolating (6-11) for V_y , we have:

$$V_y \approx \frac{nv_T (\ln(\mu_2 C_{ox2} W_2) - \ln(\mu_1 C_{ox1} W_1)) + V_{th01} - V_{th02} - V_x}{\lambda_{bs2}} \quad (6-12)$$

Inserting V_x from (6-10) into (6-12), we have:

$$V_y \approx V_{bias} \quad (6-13)$$

With a similar analysis using equations (6-8) and (6-12), V_{body} can be isolated as below:

$$V_{body} \approx \frac{nv_T (\ln(\mu_2 C_{ox2} W_2) - \ln(\mu_1 C_{ox1} W_1)) + V_{th01} - V_{th02} - V_{bias}}{\lambda_{bs2}} \quad (6-14)$$

Comparing equations (6-4) and (6-13), it can be seen that they are of the same form. However, three conditions below should be satisfied for the extreme process corners (S and F):

$$\begin{cases} n(\mu_2 C_{ox2} W_2) - \ln(\mu_1 C_{ox1} W_1) = \ln(\mu_{DUT1}) - \ln(\mu_{DUT2}) \\ V_{th01} - V_{th02} = \Delta V_{th0DUT} \quad (fast) \\ V_{th02} - V_{th01} = \Delta V_{th0DUT} \quad (slow) \\ V_{bias} = \lambda_{bs2} V_{bsDUT1} \end{cases} \quad (6-15)$$

where $DUT1$ denotes the device under test that is not affected by process variations (TT operation) and $DUT2$ represents the transistor affected by process variations. If the above conditions are satisfied, the suggested circuit can be used to decrease current sensitivity of an NMOS operating in subthreshold to process variations. Next, sizing of the NDBB transistors has to be completed using simulations. An ideal DC voltage source is used for

V_{bias_n} in the NDBB circuit of Figure 83. Sweeping V_{bias_n} from 0 – 300 mV, the output, V_{Body_n} , is plotted for the T, F and S process corners. The right sizing for NDBB transistors is found when for a specific V_{bias_n} , an output of about 0, 176.6 mV and 300 mV is produced for the T, F and S corners. This condition was specified in design step 3 of section 6.3.1. After running multiple simulations and re-sizing the transistors, the V_{Body_n} vs. V_{bias_n} plot of Figure 84 is obtained for the T, F and S process corners. As shown in Figure 84, using a bias of about 97.77 mV, the required body voltages for T,F and S process corners are produced. These body voltages can be applied to an NMOS with $W=4\ \mu\text{m}$ and $L=120\ \text{nm}$ for current stabilization.

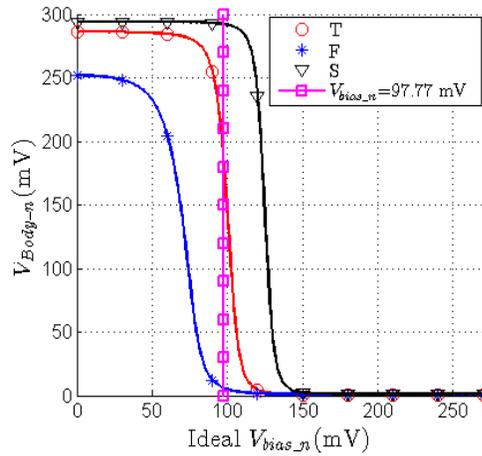


Figure 84 NDBB V_{Body_n} vs. Ideal V_{bias_n} for T, F, S process corners.

A simple voltage divider circuit as shown in Figure 85 (a) can be used for to produce V_{bias_n} of 97.77 mV. Figure 85 (b) shows the DC bias voltage produced by this circuit for different process corners after proper sizing. The lower NMOS device in the bias generator circuit is in SBB configuration to avoid using larger channel width. As it can be seen in Figure 85 (b), the bias voltage is in the 88 – 114 mV range depending on the process corner. Simulations for the next design steps show that this error margin is acceptable.

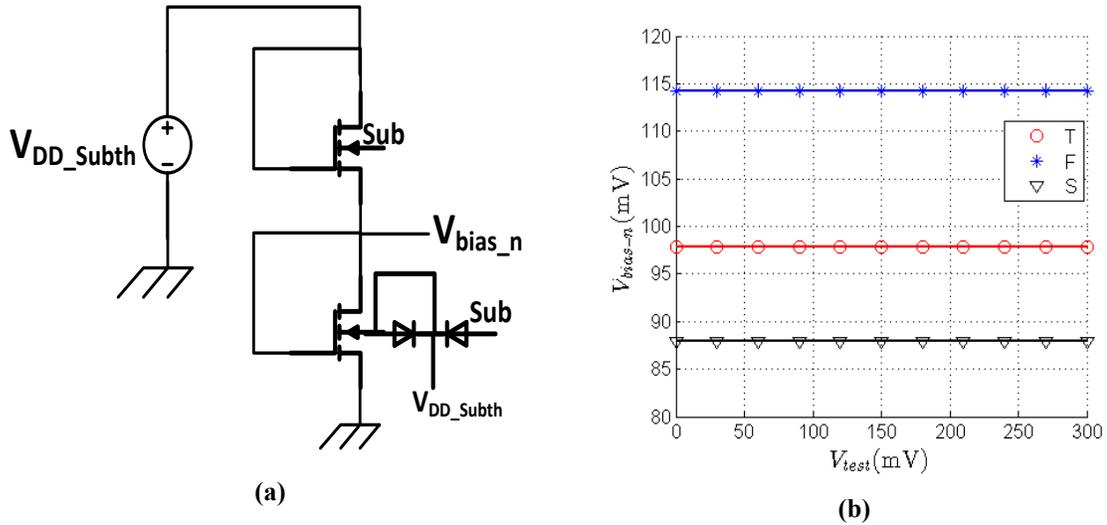


Figure 85 a) NDBB bias generator circuit b) V_{bias_n} for T, F, S process corners.

The next step is to find the body voltage produced by the NDBB using the bias generator circuit. An arbitrary test voltage is swept from 0 – 300 mV in order to plot V_{Body_n} for T, F and S process corners as shown in Figure 86. As it can be seen, V_{Body_n} is about 2.11 mV, 176 mV and 293 mV for the F, T and S process corners. These values are very close to those found in section 6.2 for a potential process variation tolerant NMOS device with $W=4\ \mu\text{m}$ and $L=120\ \text{nm}$.

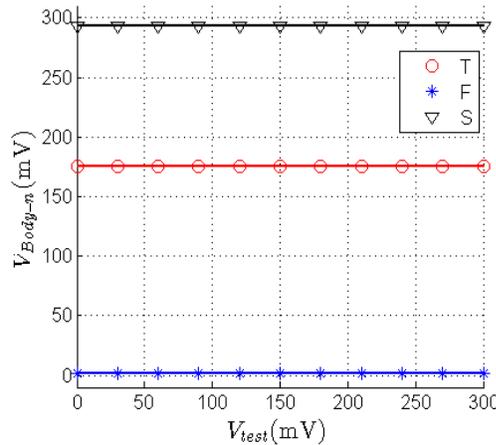


Figure 86 V_{Body_n} produced by NDBB using bias generator circuit for T, F, S process corners.

The last step is to test the NDBB circuit on an NMOS with $W=4\ \mu\text{m}$ and $L=120\ \text{nm}$ using the test bench of Figure 87. Figure 88 shows the I_{ds} vs. V_{gs} plot of the DBB NMOS for T, F and S process corners. This plot shows that the subthreshold current for all process corners has almost merged within a range of 2.4 – 2.5 μA for $V_{gs}=300\ \text{mV}$.

Therefore, the NMOS is become process variation tolerant and the NDBB circuit has been successfully designed.

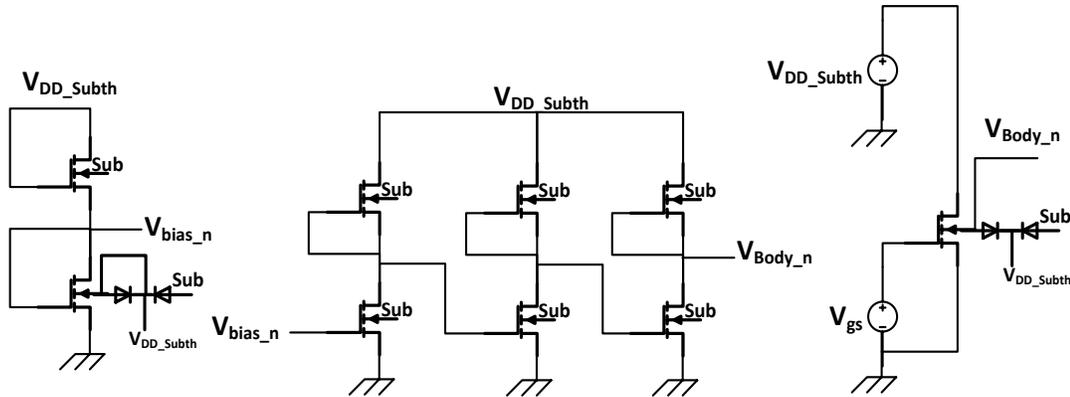


Figure 87 Test bench for testing NDBB circuit on an NMOS with $W=4 \mu\text{m}$ and $L=120 \text{ nm}$.

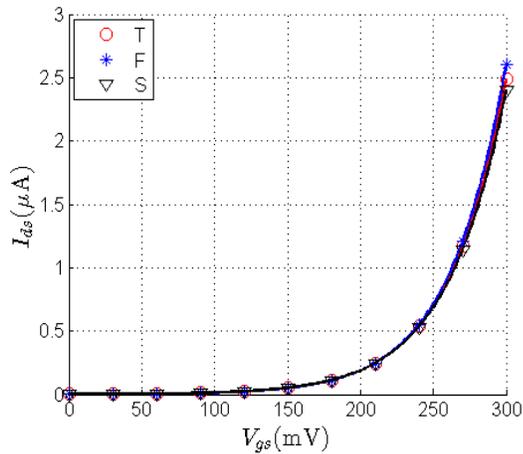


Figure 88 I_{ds} vs. V_{gs} plot of DBB NMOS transistor using $W=4 \mu\text{m}$ and $L=120 \text{ nm}$ for T, F, S process corners.

Table 14 lists the transistor sizing used for the NDBB circuit. The channel width of the transistor connected to V_{DD_Subth} for each sub-circuit is shown using W_1 .

Table 14 Transistor sizing for NDBB circuit.

V_{bias_n} generator	V_{Body_n} generator
$W_1 = 160 \text{ nm}, W_2 = 2.7 \mu\text{m}, L = 120 \text{ nm}$	$W_1 = 12 \mu\text{m}, W_2 = 500 \text{ nm}, L = 120 \text{ nm}$

6.3.3 PDBB Circuit Design

The PMOS dynamic body-biasing circuit is designed using the same concept as the NDBB. The only differences are that PMOS transistors are used instead of NMOS, and that body biasing has the opposite effect on PMOS devices. The PDBB circuit consists of three PMOS inverters with depletion mode load connected in series as shown in Figure 89.

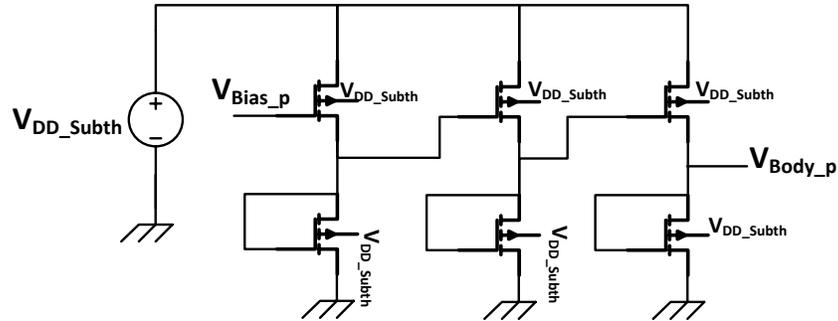


Figure 89 PMOS dynamic body-biasing (PDBB) circuit.

Following the DBB design scheme, first the value for V_{bias_p} is found to produce the appropriate body voltage for the T, F and S process corners. Using an ideal DC voltage source for V_{bias_p} and sweeping from 0-300 mV, V_{Body_p} is plotted for T, F and S process corners as shown in Figure 90. As the plot shows, using a bias voltage of about 191.8 mV, V_{Body_p} is obtained as 297.9 mV, 137.34 mV and 4.86 mV. These values are very close to the expected body voltages required.

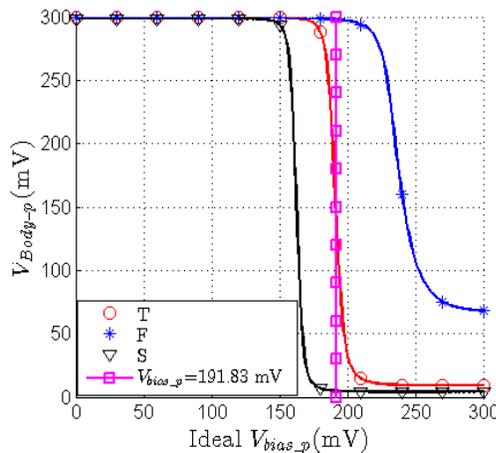


Figure 90 PDBB V_{Body_n} vs. Ideal V_{bias_n} for T, F, S process corners.

Similar to the NMOS bias generator, a PMOS voltage divider shown in Figure 91 (a) is used to produce $V_{bias_p}=191.83$ mV. Using a test voltage to plot the output of the bias generator, V_{bias_p} is obtained in the range of 182 – 198 mV for different process corners as shown in Figure 91 (b). Further simulations show that this range is tolerable.

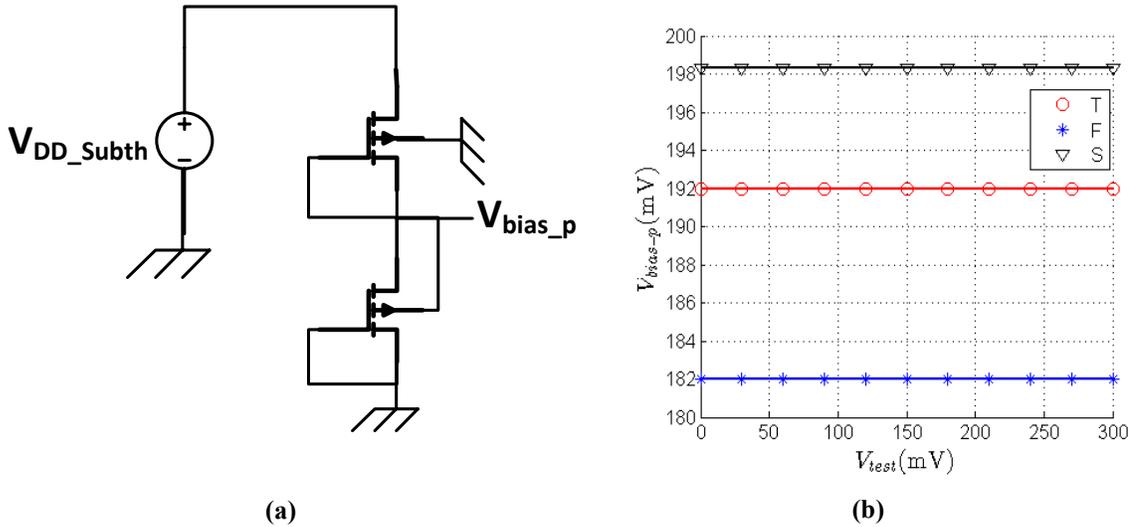


Figure 91 a) PDBB bias generator circuit b) V_{bias_p} for T, F, S process corners.

It should be noted that the body connections in the bias generator circuit are adopted to optimize transistor sizing for both devices. Using the generated bias, V_{Body_p} is produced for all process corners as shown in Figure 92. As this plot shows, V_{Body_p} is produced as 299 mV, 135 mV and 0.5 mV for F, T and S process corners, which are almost the required body voltages.

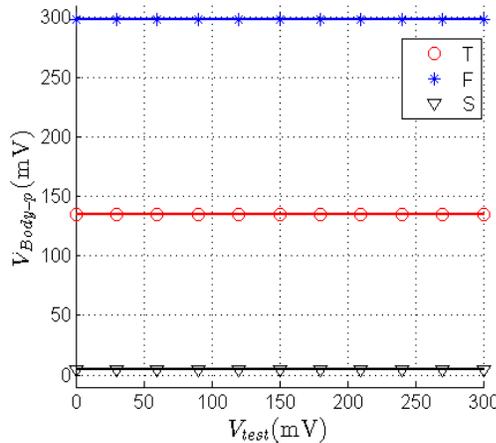


Figure 92 V_{Body_p} produced by PDBB using bias generator circuit for T, F, S process corners.

The last step of designing the PDBB circuit is to confirm its operation by applying its output to the body of a PMOS device with $W=2.5\ \mu\text{m}$ and $L=120\ \text{nm}$. For this purpose, the test bench of Figure 93 is used. This test bench is used for plotting I_{sd} vs. V_g when $V_{sd}=300\ \text{mV}$ as shown in Figure 94. The current merges for all process corners within a range of $976\ \text{nA} - 1.07\ \mu\text{A}$ when $V_{sg}=0.3\ \text{V}$. Thus, a robust DBB PMOS transistor with minor changes in current due to process variations is designed. Table 15 lists the design parameters for the PDBB circuit. The channel width of the transistor connected to V_{DD_Subth} for each sub-circuit is shown using W_1 .

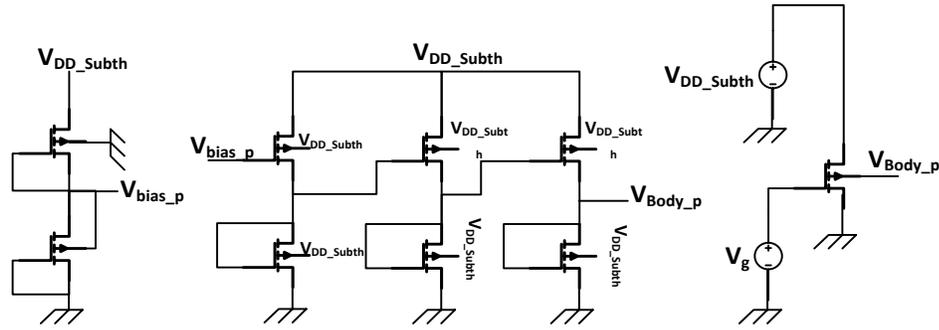


Figure 93 Test bench for testing PDBB circuit on a PMOS with $W=2.5\ \mu\text{m}$ and $L=120\ \text{nm}$.

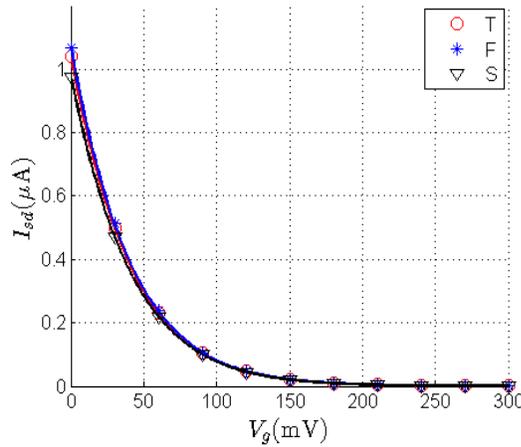


Figure 94 I_{sd} vs. V_g plot of DBB PMOS transistor using $W=2.5\ \mu\text{m}$ and $L=120\ \text{nm}$ for T, F, S process corners.

Table 15 Transistor sizing for the PDBB circuit.

V_{bias_p} generator	V_{Body_p} generator
$W_1 = 640\ \text{nm}$, $W_2 = 320\ \text{nm}$, $L = 120\ \text{nm}$	$W_1 = 160\ \text{nm}$, $W_2 = 6\ \mu\text{m}$, $L = 120\ \text{nm}$

6.4. Process Variation Tolerant VCFS and Sensor SPU Design using NDBB and PDBB Circuits

After designing the NMOS & PMOS body-biasing circuits, they can be applied to the VCFS block of the sensor SPU to increase robustness. The design steps outlined in Chapter 4 are repeated for the SPU with dynamically body biased transistors. In addition, minor adjustments to the DC shifter and varactor are made for further improvement of the SPU design. However, the level shifter does not need to be re-designed as it is already process variation tolerant. Similar to the previous SPU design, $V_{DD}=1.2$ V and $V_{DD_Subth}=300$ mV.

6.4.1 Robust Subthreshold Schmitt Trigger using NDBB and PDBB Circuits

The design steps of the Schmitt Trigger are listed previously in 4.3. To re-design the Schmitt Trigger circuit using the NDBB and PDBB circuits, a similar design approach has to be followed with some exceptions. Firstly, the NMOS and PMOS transistors have to use finger widths of 4 μm and 2.5 μm respectively. Furthermore, DBB technique is adopted for all transistors of the ST circuit for robustness. The bodies of all NMOS transistors are connected to the output of the NDBB circuit, while the bulks of all PMOS devices are biased using the output of the PDBB. Lastly, the optimum values of ρ and σ current ratios explained in 4.3.2 cannot be found or deployed precisely here. The reason is that transistor widths can only be increased using more fingers. The widest possible hysteresis and current ratios can be found using simulations.

The number of fingers for all NMOS and PMOS transistors is chosen as 1 and 2 respectively at first. Using parametric simulations, the number of fingers can be adjusted to find the optimum hysteresis width. Figure 95 shows the Schmitt Trigger test bench using the body-biasing circuits. Sweeping the input DC voltage from 0 – 300 mV for high-to-low and from 300mV – 0 V for low-to-high switching, the optimum hysteresis can be found for different process corners. Figure 96 shows the simulation results for the TT, FF, SS, FS and SF process corners.

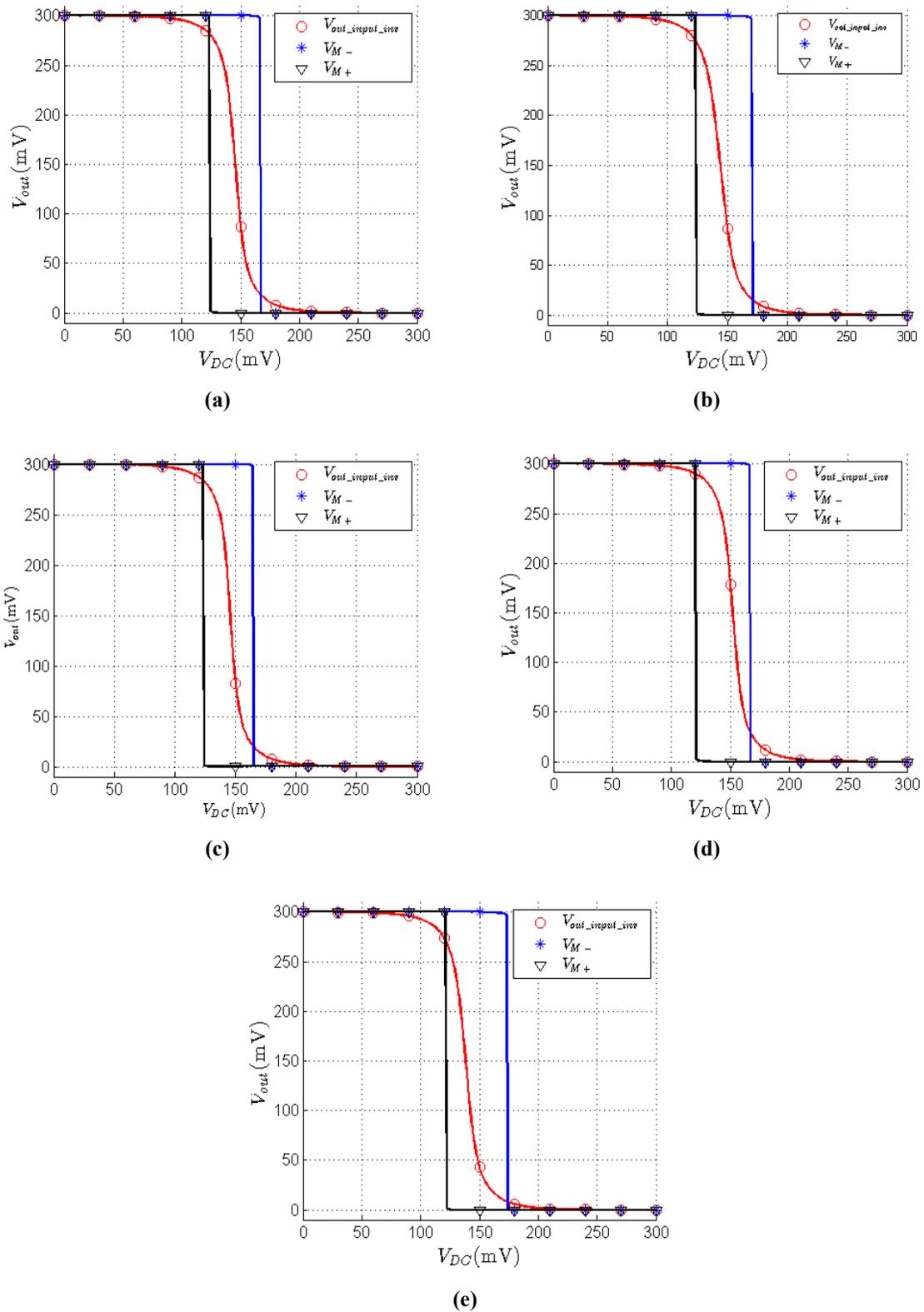


Figure 96 Schmitt Trigger hysteresis using NDBB and PDBB circuits for robust subthreshold operation. a) TT b) FF c) SS d) FS e) SF process corners.

Table 16 summarizes V_{M+} and V_{M-} values for each process corner extracted from Figure 96. Comparing the hysteresis plots above with the ones of Figure 49 in 4.3.2 as well as switching threshold values of Table 16 with Table 9, interesting results can be found. It is observed that the hysteresis width (noise margin) is much wider for the new design using dynamic body biasing. The minimum hysteresis width for the improved design is 262.06 mV, while for the old ST circuit it is at most 190.24 mV. Moreover, the maximum variation in hysteresis width is only 2.51 mV using dynamic body biasing. The previous ST yields a hysteresis width error of 89.31 mV. Dividing the maximum variations by minimum hysteresis width, the enhanced ST only yields an error of 1% due to process variations. Hence, the dynamic body-biasing method has led to significant improvement of the Schmitt Trigger operation with regards to robustness and noise margin.

Table 16 Switching threshold values of the new Schmitt Trigger using body-biasing circuits for different process corners.

Process Corner	V_{M+} (mV)	V_{M-} (mV)	Noise Margin (mV)
TT	281.07	18.13	262.94
FF	275.87	13.44	262.43
SS	283.43	18.90	264.53
FS	290.44	28.38	262.06
SF	271.65	8.12	263.53

Table 17 summarizes the transistor sizing used for the dynamically body biased Schmitt Trigger operating in the subthreshold region. F_N and F_P refer to number of fingers for NMOS and PMOS transistors, which are 4 μm and 2.5 μm in width.

Table 17 Design parameters for the new Schmitt Trigger circuit using dynamic body-biasing circuits.

Design parameter	Value
L	120nm
F_N, F_P width	4 μm , 2.5 μm
$F_{N1} = F_{N2} = F_{N3} = F_{inputN}$	1
$F_{inputP} = F_{P2} = F_{P3}$	2
F_{P1}	3

The next step is to run a transient simulation for the Schmitt trigger, just as done in Chapter 4. The goal is to find the maximum operating frequency of the circuit, as well as RT and FT parameters. Similar to the old design, an input pulse with a period of 2 μs , PW of 1 μs and RT/FT of 200 ns is applied to the circuit. The rise/fall times of the Schmitt Trigger output are recorded in Table 18. It can be seen that the rise/fall times at the output are much less than that of the input. Thus, the ST is responding to a slowly changing input with a sharp pulse at the output. Comparing the values of Table 18 with those of Table 10, it can be seen that the RT/FT of the ST using DBB technique have increased, with the exception of the SS process corner. However, this has been done at the expense of decreasing the positive and negative spikes at the output as it is shown in Figure 97. Hence, short circuit current and static power consumption has decreased at the expense of delay.

Table 18 Rise and fall times of the Schmitt Trigger output for different process corners in response to an input pulse with $P=2\mu\text{s}$, $PW=1\mu\text{s}$, $RT=200\text{ns}$, $FT=200\text{ns}$.

Process Corner	Rise time (ns)	Fall time (ns)
TT	27.03	33.87
FF	45.66	32.66
SS	24.22	34.95
FS	22.94	54.05
SF	57.98	27.03

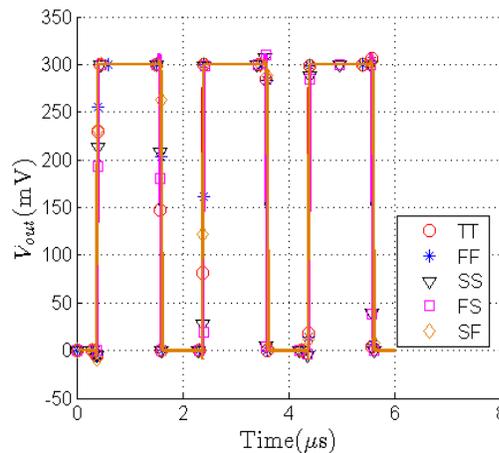


Figure 97 Schmitt Trigger output using NDBB and PDBB circuits in response to input pulse with period=2 μs , $PW=1 \mu\text{s}$, $RT=FT=200 \text{ ns}$ for different process corners.

Decreasing the period of the input pulse, it is observed that the maximum frequency of operation for the Schmitt Trigger is about 2 MHz. This means that up to a frequency of 2 MHz, the output pulse responds sharply to the input. This value is larger than the one obtained for the Schmitt Trigger of Chapter 4 (1.25 MHz). The increase in frequency is due to the larger transistors as well as the DBB circuits, which adjusts the transistor's strength if implemented using a slow process. Simulations also show that for the worst process corner, the ST consumes about 108.75 nW of power at its maximum frequency of operation. This value is much larger than the 8.38 nW power consumption of the previous design. Thus, the ST circuit using DBB has become more robust at the cost of more dynamic power consumption.

6.4.2 Robust Subthreshold VCFS using NDBB and PDBB Circuits

After re-designing the ST, the VCFS can be tested using the DBB circuits and an ideal capacitor placed at the output of the RO as shown in Figure 98. In the previous design, the capacitor could not be connected to this node due to the small size of the transistors and loading limitation. As a result, the varactor was connected to the output of the first stage inverter of the ST ($V_{X_schmitt}$). Loading the ST node could cause problems, as it adds delay to the Schmitt Trigger operation. This could possibly have been a cause behind the carrying duty cycles and frequencies of the previously designed VCFS. If the capacitor is placed at the output of the RO, the output inverter governs the charging/discharging procedure. Consequently, the frequency and duty cycle of the VCFS is controlled by a single inverter rather than a complicated Schmitt Trigger. However, both configurations are tested using simulations with the dynamic body-biased VCFS to choose the best structure in terms of robustness.

Figure 99 shows the Frequency vs. Capacitance (2 - 12 pF) plot when the ideal capacitor is connected to the outputs of the RO and $V_{X_schmitt}$ respectively for all process corners. As it can be seen in these plots, the frequency variations are much larger when the capacitor is connected to $V_{X_schmitt}$. Therefore, the varactor should be connected to the output of the ring oscillator for enhanced robustness.

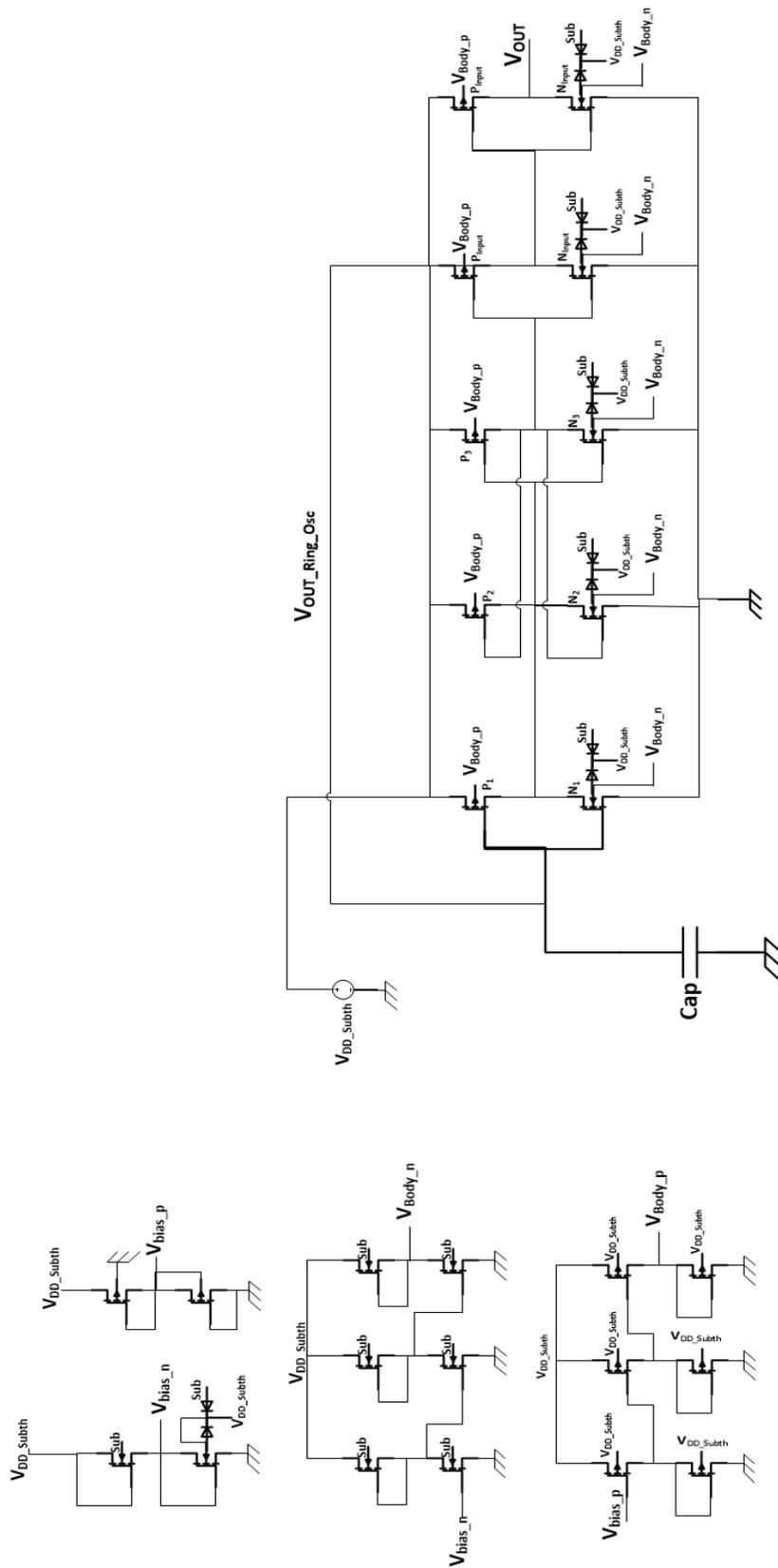


Figure 98 VCFS test bench using ideal capacitor and DBB circuits.

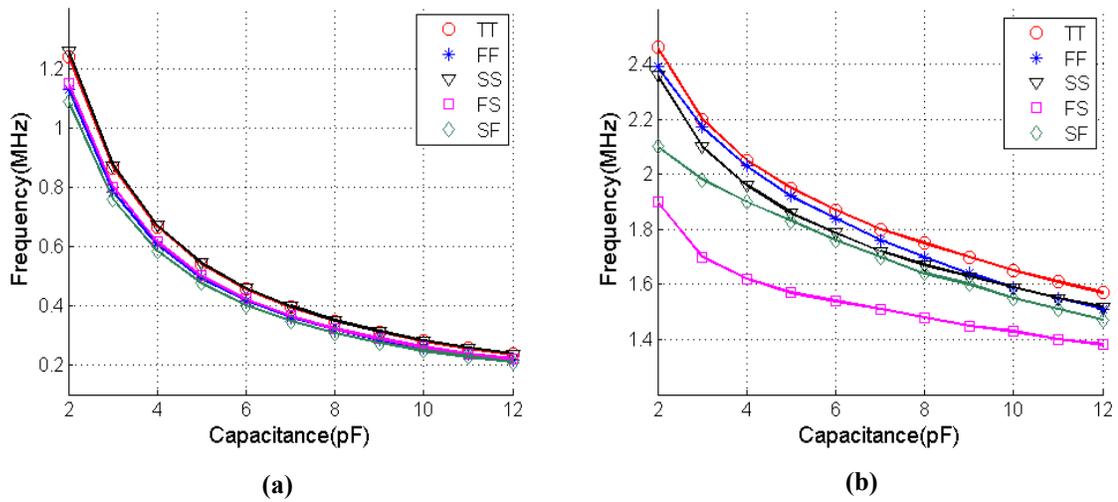


Figure 99 VCFS using DBB circuits Frequency vs. Capacitance plots with ideal capacitor at a) output of RO b) output of first stage ST inverter ($V_{X_schmitt}$) for different process corners.

Table 19 lists the output pulse frequency for different capacitances and process corners obtained by Figure 99 (a). The data in Table 19 show that the variations in frequency are almost the same for all capacitance values. However, the frequency vs. capacitance plot shows a linear relationship only for capacitances smaller than 3 pF. As previously stated in design specifications of the SPU, the frequency vs. dose measurement plot should be linear for all dose measurements. Hence, it is best to choose a varactor with a maximum capacitance of 3 pF. Table 19 shows that the maximum variations in frequency is about 12% (dividing maximum by minimum frequencies for different process corners) for the enhanced VCFS. Therefore, the enhanced VCFS using dynamic body-biasing shows superior linearity and robustness over the previous design in Chapter 4.

Table 19 Frequency values extracted from the plot of Figure 99 a).

Capacitance (pF)	Frequency (MHz)				
	TT	FF	SS	FS	SF
2	1.24	1.13	1.26	1.15	1.09
4	0.664	0.604	0.671	0.615	0.583
6	0.455	0.416	0.460	0.422	0.401
8	0.347	0.318	0.350	0.322	0.307
10	0.280	0.258	0.283	0.260	0.248
12	0.235	0.217	0.238	0.219	0.209

6.4.3 Robust Ultra-Low Power Sensor SPU for Wireless Dosimetry

After re-designing the ST and VCFS using the DBB circuits, the signal processing unit can now be re-designed. However, slight adjustments have to be made to the DC shifter and varactor. The level shifter is not re-designed as it was proven to be robust in the previous design. The DBB circuits are not suitable for transistors connected in series, as their drain-source voltage does not go from rail-to-rail. As a result, the PDBB circuit cannot be applied to the bulks of the DC shifter transistors.

The DC shifter designed in Chapter 4 had a major problem, which was observed after implementation and during testing. The bulks of all PMOS transistors were connected to 1.2 V, which could lead to a very high body-source voltage for some transistors in the chain depending on V_{in} . Thus, it is best to connect the body of all transistors to their source as shown in Figure 100. This prevents V_{sb} from becoming too large as well as equalizing the strengths of all transistors, thereby decreasing sensitivity to process variations.

Another problem with the design of Chapter 4 was the type of varactor used to generate pulses with different frequencies. Simulations show that a differential NCAP varactor shown in Figure 101 decreases the VCFS's sensitivities to process variations. This varactor has four terminals: one connected to the output of the DC shifter (V_{sensed_scaled}), the second connected to the output of the ring oscillator ($V_{OUT_Ring_osc}$), third connected to ground and the last one to the substrate.

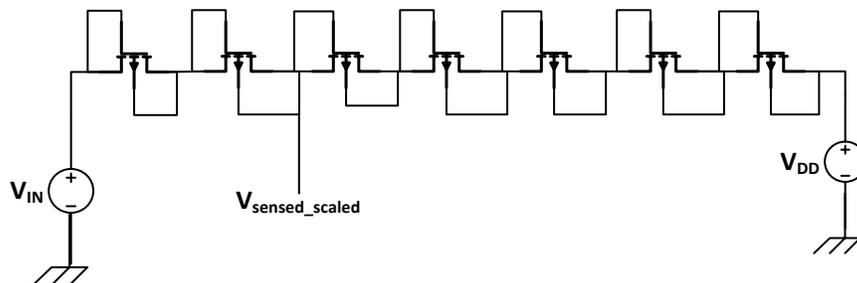


Figure 100 DC Shifter block used for the new SPU design.

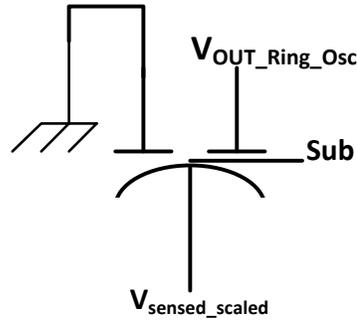


Figure 101 Differential NCAP Varactor used for the new SPU design.

Figure 102 shows the signal processing unit using the body-biasing circuits. Different parts of the SPU are outlined in the figure for clarity. As it can be seen in Figure 102, the gate (drain) of the fourth transistor in the DC shifter closest to the V_{in} is chosen for the varactor connection. The reason as that simulations showed it resulted in the best response in terms of frequency range, linearity and robustness. Using the test bench of Figure 102, transient simulations are completed similar to Chapter 4 to obtain necessary plots for the sensor SPU.

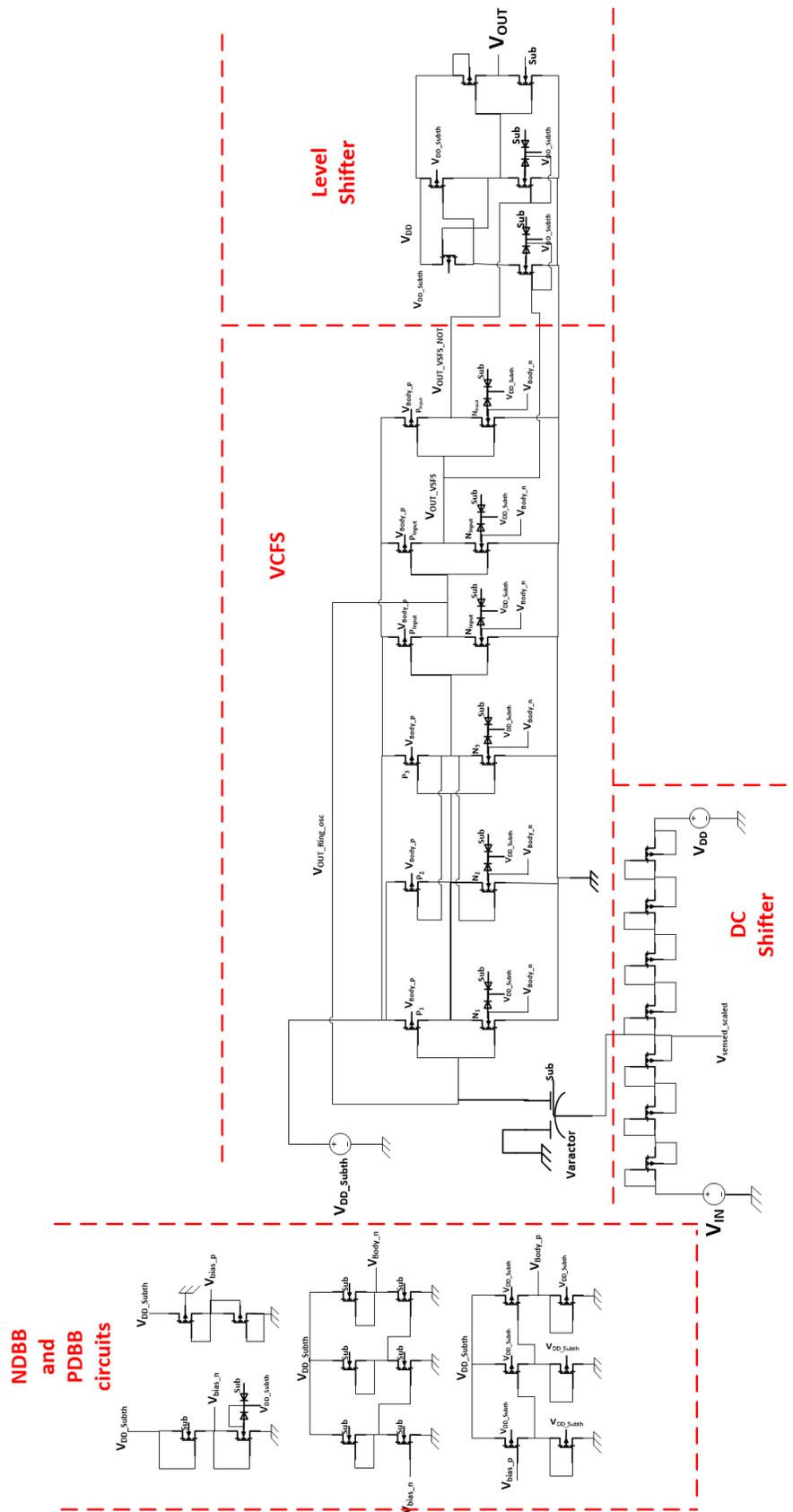


Figure 102 Robust SPU using NDBB and PDBB circuits.

Figure 103 shows the output of the DC shifter for input values of -900 mV and 0 and different process corners. As it can be seen in the plot, V_{sensed_scaled} varies from about 0 – 150 mV for $V_{in} = -900$ mV and 500 – 620 mV for $V_{in} = 0$ mV. Comparing this plot with that of Figure 54 in Chapter 4, significant decrease in variations of shape and values for different process corners can be observed. Moreover, these values are closer to the 0 – 500 mV intended range for the varactor compared to the previous design.

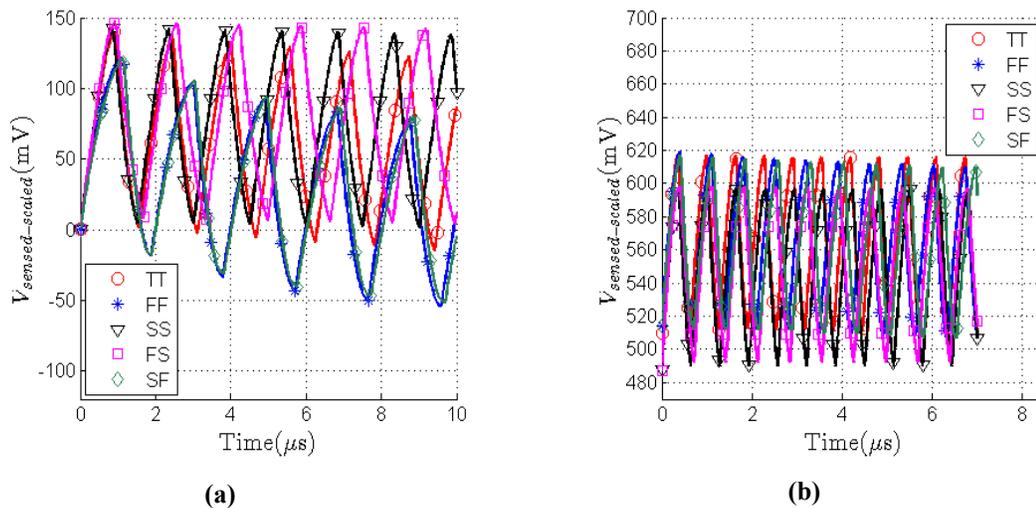


Figure 103 DC shifter output when connected to DBB VCFS at different process corners for a) $V_{in} = -0.9$ V b) $V_{in} = 0$.

Figure 104 shows the frequency vs. V_{in} plot for the SPU using NDBB and PDBB circuits for all process corners. Table 20 lists the different frequency values extracted from the plot of Figure 104 with a step size of 70 mV that is equivalent to about 2 Gy of dose. As it shown in the plot of Figure 104 using a red circle and dashed line, the SPU has about 210 mV, or 6 Gy of dose, error at the worst case. This happens between the two process corners further apart, which are SS and SF. For example, the dose corresponding to an $V_{in} = -900$ mV for the SS corner is equivalent to that of $V_{in} = -690$ mV for the SF corner as shown using the red circle in the plot and dashed line in the plot. Since the total dose range is about 25 Gy, this design yields about 24% of error in sensitivity translation. This shows great improvement compared to the older design in Chapter 4, where the frequency band for each process corner was totally different and the error was 100%. (e.g.

the frequency for $V_{in} = -900$ mV could change from 588.7 KHz to 7.37 MHz). Therefore, the suggested novel body-biasing circuits have resulted in increased robustness of the circuit. The 6 Gy sensitivity detection error is tolerable can be removed after calibration of the chips. Hence, the fourth design specification of the ULP sensor SPU listed in Table 7 has been fulfilled with an acceptable accuracy.

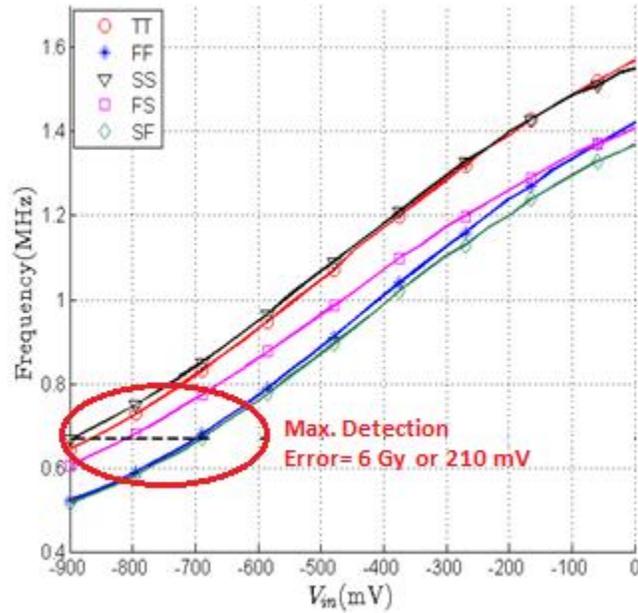


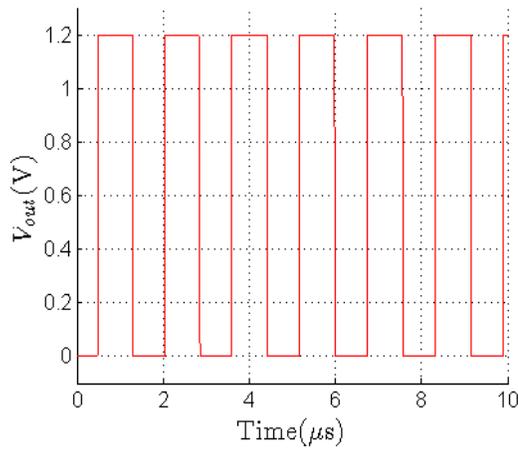
Figure 104 Frequency vs. V_{in} plot for SPU using DBB technique for all process corners.

Table 20 Frequency values obtained from the plots of Figure 104.

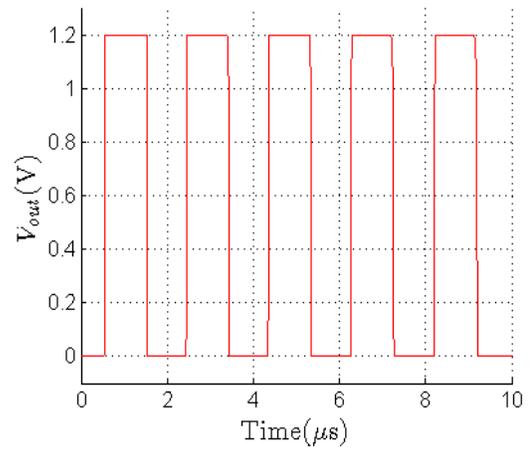
V_{in} (mV)	Frequency (MHz)				
	TT	FF	SS	FS	SF
-900	0.645	0.522	0.667	0.605	0.516
-830	0.697	0.564	0.721	0.654	0.558
-760	0.761	0.619	0.782	0.710	0.611
-690	0.831	0.679	0.851	0.773	0.670
-620	0.907	0.749	0.926	0.840	0.738
-550	0.989	0.830	1.01	0.912	0.816
-480	1.07	0.912	1.09	0.986	0.895
-410	1.16	0.998	1.17	1.06	0.976
-340	1.24	1.08	1.25	1.13	1.06

-270	1.32	1.16	1.33	1.20	1.13
-200	1.39	1.24	1.40	1.26	1.20
-130	1.46	1.31	1.46	1.32	1.27
-60	1.52	1.37	1.51	1.37	1.33
0	1.57	1.42	1.55	1.41	1.37
Bandwidth (KHz)	925	898	883	805	854
Minimum Resolution (KHz/Gy)	20	18.9	17	15	18.4

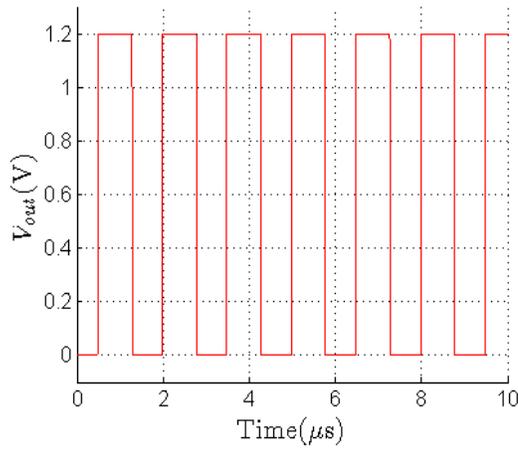
The curves of Figure 104 also show that the frequency vs. dose measurement is almost linear for all process corners and input. Consequently, the linear specification has also been met successfully. Linearity of the frequency vs. dose measurement was only observed for input voltages smaller than -400 mV for the previous SPU design. The minimum resolution of the SPU is about 15 KHz/Gy, which is much greater than the specified 1 – 4 KHz/Gy minimum range, hence satisfying the resolution condition. The resolution obtained for the enhanced SPU is also much greater than the 3.5 KHz/Gy conducted with the initial design in Chapter 4. The minimum bandwidth of the signal processing unit is 805 KHz, which offers a wide range for detecting sensitivity. As a result, values smaller than 1 Gy can also be detected. Figure 105 shows the output pulse train of signal processing unit for input of -900 mV and different process corners. As it can be seen in the above plots, the duty cycle of the pulses are not effected significantly by process variations. The pulse train shows similar results for other input voltages and dose measurements. Using the body-biasing circuits, all pulses yield a duty cycle of about 50%, thereby satisfying the duty cycle design specification of the SPU. This is also another significant improvement compared to the previous SPU design, where the duty cycle varied between 10 – 90%.



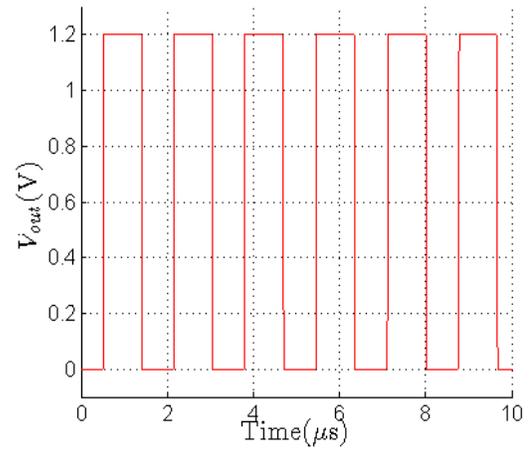
(a)



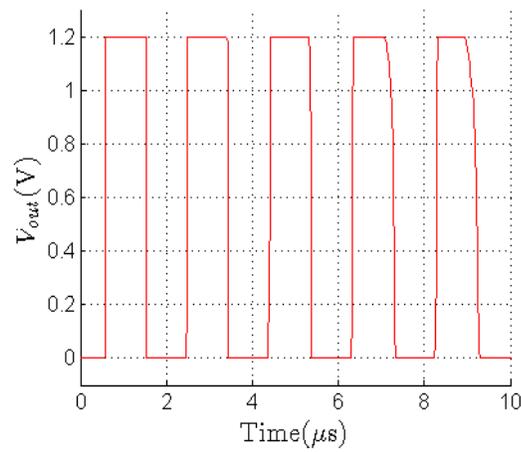
(b)



(c)



(d)



(e)

Figure 105 Output pulse train of SPU using DBB technique for $V_{in} = -0.9$ V using a) TT b) FF c) SS d) FS d) SF process corners.

The last step is to present the power consumption of the signal processing unit. Figure 106 shows the average power consumption for different process corners. As it can be seen in the plot, the circuit consumes a maximum power of 1.72 μW . This is less than the maximum value of about 2.5 μW obtained for the initial SPU design in Chapter 4. Moreover, it is smaller than 3.15 μW , which is the design specification. In addition, the power consumption plot for the previous design showed unexpected peaks for some input voltages and process corners due to high sensitivity to process variations. Such a behavior is not observed for the enhanced signal processing unit. Thus, the sensor SPU has become more robust with decreased power consumption, increased resolution, improved linearity and extended bandwidth. Table 21 summarizes the design parameters used for the final design of the signal processing unit.

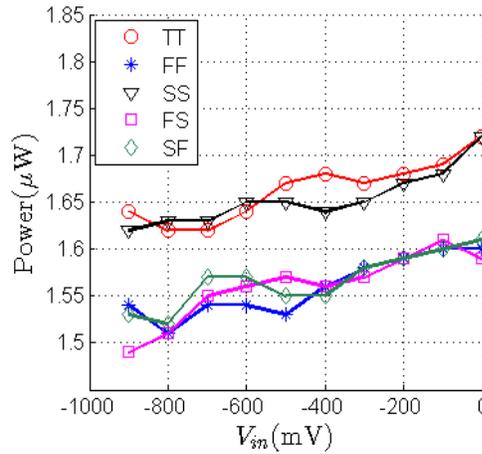


Figure 106 Power consumption of the DBB SPU.

Table 21 Design parameters for the final SPU design with enhanced robustness using DBB technique.

Block	Parameters
DC shifter	$W_p=160$ nm, $L_p=120$ nm
Varactor	RX Width=10 μm , PC length=10 μm , # of gates=20, , minimum capacitance=1.08 pF, maximum capacitance=5.51 pF,
Schmitt Trigger	$F_{P1}=F_{P2}=2$, $F_{P3}=3$, $F_{N1}=F_{N2}=F_{N3}=1$, F_p size=2.5 μm , F_N size=4 μm , $L=120$ nm
RO output inverters	$F_p=2$, $F_N=1$, F_p size=2.5 μm , F_N size=4 μm , $L=120$ nm
Level shifter	$W_N=W_p=160$ nm, $L_N=800$ nm, $L_p=1$ μm
Level shifter output inverter	$W_p=500$ nm, $W_N=160$ nm, $L=120$ nm
bias generator for NDBB	$W_1 = 160$ nm, $W_2 = 2.7$ μm , $L=120$ nm

NDBB	$W_1 = 12 \mu\text{m}, W_2 = 500 \text{ nm}, L = 120 \text{ nm}$
bias generator for PDBB	$W_1 = 640 \text{ nm}, W_2 = 320 \text{ nm}, L = 120 \text{ nm}$
PDBB	$W_1 = 160 \text{ nm}, W_2 = 6 \mu\text{m}, L = 120 \text{ nm}$
$V_{DD} = 1.2 \text{ V}, V_{DD_Subth} = 300 \text{ mV}$	

To summarize the improvements relating to the design of the SPU of this chapter, a comparison with the schematic design of Chapter 4 is given in Table 22. The modifications done in this chapter have made the design superior for all design specifications. The major advantage is the enhanced robustness using the NMOS and PMOS body-biasing circuits used to stabilize the subthreshold current. This has resulted in operational robustness of the SPU with minimum error in the output frequency, which could be overcome with appropriate calibration procedures. The final design also consumes less power and preserves a duty cycle of 50% for all process corners. Thus, the modified SPU using NDBB and PDBB techniques meets all design specifications. Hence, the final objective of this thesis has been successfully fulfilled.

Table 22 Comparison of initial and final ULP sensor SPU designs for different specifications.

Design specification	Initial SPU design (#1)	Final SPU design (#2)	Superior design
Robustness – Maximum Error	25 Gy – 100%	6 Gy – 24%	#2
Minimum Resolution	3.5 KHz/ Gy	15 KHz/Gy	#2
Minimum Bandwidth	159 KHz	805 KHz	#2
Linearity	Linear for $V_{in} < -0.4 \text{ V}$	Almost Linear for all V_{in}	#2
Duty cycle of output pulse train	Duty cycle varies between 10% - 90% depending on process corner	Duty cycle about 50% for all process corners and input voltages	#2
Maximum Power Consumption	2.50 μW	1.72 μW	#2

6.5. Summary

A novel dynamic body-biasing method was introduced using an original theoretical analysis and with the aid of simulations using Cadence. The minimum channel width for potential process variation tolerant transistors using the 0.13 μm technology was found to be 4 μm for NMOS and 2.5 μm for PMOS. Both devices use minimum channel length of 120 nm. Two novel body-biasing circuits were designed to stabilize the currents of these transistors for different process corners. The NDBB circuit consists of three NMOS inverters in series and an NMOS bias generator. Similarly, the PDBB is made of three back-to-back PMOS inverters and a PMOS bias generator. NDBB is designed to stabilize the current of NMOS devices, while PDBB is intended for PMOS transistors by generating a dynamic body bias.

The proposed dynamic body-biasing method was applied to the Schmitt Trigger and VCFS circuits. Simulation results show significant improvement with regards to robustness for both circuits. The Schmitt Trigger circuit yields only 1% of error in hysteresis width, while the VCFS produced a maximum of 12% fault in produced frequency due to process variations. The previous DC shifter designed in Chapter 4 was modified by connecting the transistor bulks to their sources rather than V_{DD} . This adjustment was done to prevent a high body-source voltage for the DC shifter transistors. In addition, the previous NCAP varactor was replaced by a differential one to increase robustness. With these modifications, the SPU was re-designed and simulated. Simulation results show great superiority over the previous design of Chapter 4 with regards to all design specifications. The SPU shows significant robustness enhancement with a sensitivity detection error of 24% or 210 mV (6 Gy) of dose measurement. In addition, it yields a minimum resolution of 15 KHz/Gy, minimum bandwidth of 805 KHz and maximum power consumption of 1.72 μW . The frequency produced by the VCFS shows almost a linear relationship with sensitivity for all process corners and inputs as required. Moreover, the output pulse train has a duty cycle of about 50% for all input voltages and process corners as intended. Therefore, all design specifications of the ULP sensor SPU are met with an acceptable precision. Hence, the last objective of this thesis work is successfully achieved.

Chapter 7. Conclusions

7.1. Summary

MOSFET operation in the subthreshold region was analyzed theoretically. Furthermore, the benefits and challenges associated with subthreshold circuits were investigated. High current sensitivity to process variations was found to be a major problem of subthreshold circuits, which degrades their robustness. Recent advancements on addressing subthreshold circuit challenges were explored. Moreover, research developments on ultra-low power sensor signal processing for wireless applications were studied. Hence, the first objective of this thesis was fulfilled.

MOSFET subthreshold behavior using the 0.13 μm CMOS IBM technology was then analyzed thoroughly using simulations with Cadence. MOSFET current and threshold characteristics with regards to V_{gs} , V_{bs} , V_{ds} , W and L parameters were investigated for CBB, SBB and DTMOS configurations. Furthermore, changes in threshold voltage and current due to process variations were investigated for these body-bias configurations. These variations were examined for different W , L and V_{DD} values for each type of body-biasing structure. The resulting observations were used for transistor sizing and body biasing in designing the ULP sensor SPU. Moreover, V_{DD} of 300 mV was chosen for robust subthreshold operation. Through these steps, the second thesis objective has been met.

The wireless dosimeter was studied at a system level and the design specifications for the SPU were extracted. These specifications include consuming less than about 3.15 μW of power and accurately translating the dose measurement via a linear frequency vs. sensitivity response. Furthermore, a minimum resolution in the range of 1 – 4 KHz/Gy was found to be required. Since power consumption was the main limitation of the SPU, CMOS circuit design using the subthreshold region of operation was adopted. However, sensitivity to process variations, which decreases the robustness of these circuits, had to be addressed.

The sensor signal processing unit was divided into the following sub-sections to convert dose measurements to frequency:

1. DC shifter to shift the $-900\text{ mV} - 0\text{ V}$ dose to $0\text{ mV} - 500\text{ mV}$ in order to change the capacitance of a varactor.
2. Voltage-controlled frequency synthesizer, consisting of a STRO and varactor, to produce different frequency pulse train. This block is designed using a subthreshold supply voltage of 300 mV . It consists of a Schmitt Trigger within a ring oscillator operating in the subthreshold region to improve the noise immunity of the circuit.
3. Level shifter to amplify the subthreshold pulses to superthreshold amplitude for transmitting the frequency through a switch operating in superthreshold.

Each block of the SPU was designed and optimized. Previous techniques suggested for robustness enhancement, such as DTMOs configurations, were used in the VCFS. After obtaining schematic transient simulation results for the initial SPU design, the layout was completed and the chip was implemented. However, both schematic and post-layout simulation results showed significant change in the generated frequency due to process variations. Furthermore, the duty cycle of the output pulse varied greatly due to process fluctuations. In addition, the frequency vs. dose plot was not linear for the full input range for different process corners. After chip implementation, these problems were also observed during testing. However, a functional circuit was demonstrated in which a change in frequency was observed during testing for input levels of -900 mV to -600 mV . A total of 10 chips were tested and results showed further problems such as oscillation failure due to low loop gain and high sensitivity to process variations. These results proved that SBB and DTMOs body-biasing techniques are not sufficient to ensure a robust VCFS. By simulating, implementing and testing the ULP signal processing unit, the third thesis object is completed.

After observing the initial circuit limitations, the design was modified using a novel dynamic body-biasing technique suggested for CMOS circuits operating in the subthreshold region. The minimum channel width for potential process variation tolerant transistors was found to be $4\text{ }\mu\text{m}$ for NMOS and $2.5\text{ }\mu\text{m}$ for PMOS using minimum

channel length. The body-biasing circuits for each of these NMOS and PMOS transistors were designed and simulated. Designing these circuits included a number of steps, starting with an original theoretical analysis. The dynamic NMOS body-biasing circuit consisting of three NMOS inverters in series and an NMOS bias generator was introduced. Similarly, a PMOS dynamic body-biasing scheme with three back-to-back PMOS inverters and a PMOS bias generator was presented. The NDBB and PDBB circuits were applied to the potential process variation tolerant devices, resulting in almost no current sensitivity to process fluctuations.

The dynamic body-biasing circuits were further applied to the Schmitt Trigger and voltage-controlled frequency synthesizer. Simulations results showed significant robustness improvement for both circuits. The ST showed a maximum deviation of 1% in noise margin, while the VCFS produced a maximum of 12% error in output pulse train frequency. The VCFS using dynamic body-biasing was employed in the sensor signal processing unit. In addition, slight modifications were made to the previously designed DC shifter as well as the varactor. As a result, the SPU design was modified for improved performance in terms of robustness and other design specifications. The SPU was optimized and simulated at schematic level. Final simulation results showed a maximum error of 210 mV (24%) or 6 Gy of dose. Furthermore, the SPU yields a minimum resolution of 15 KHz/Gy, minimum bandwidth of 805 KHz and maximum power consumption of 1.72 μ W. The frequency vs. dose characteristic translates the sensor's sensitivity almost linearly for all input voltages and process corners. In addition, pulses with 50% duty cycle for all dose measurements were produced regardless of the process corner. Therefore, all design specifications of the SPU are met with an acceptable error margin. Using dynamic body biasing, a robust, noise immune, high resolution and ULP signal processing unit was designed for wireless dosimeter applications. Hence, the final thesis object is successfully attained.

7.2. Contributions

The following are the major contributions of this thesis:

1. Design, optimization, fabrication and testing of an original subthreshold signal processing unit for the wireless dosimeter.

2. Investigation of threshold and current sensitivities to process variations for MOSFETs operating in the subthreshold region with different body-biasing configurations. This task was completed using theoretical analysis and simulations using the 0.13 μm CMOS technology.
3. Introduction of a novel dynamic body-biasing method to increase the robustness of CMOS circuits operating in the subthreshold region. Two novel body-biasing circuits, NDBB and PDBB, are proposed for NMOS and PMOS devices, respectively.
4. Application of the proposed body-biasing scheme to the Schmitt Trigger and voltage-controlled frequency synthesizer, yielding in simulation a robust, high resolution and ultra-low power signal processing unit for wireless dosimeter applications.

7.3. Future work

There are several research directions that can be taken in order to continue the work presented in this thesis:

1. Layout, implementation and testing of the final SPU design as well as the NDBB and PDBB circuits.
2. The voltage-controlled frequency synthesizer was designed to be robust against process variations. However, temperature and voltage variations were not discussed and can be analysed in the future for increased robustness.
3. The SPU uses two supply voltages: a superthreshold one that is used by other parts of the wireless dosimeter, and a subthreshold V_{DD} for the VCFS. An ULP and robust voltage regulator needs to be designed to produce the 300 mV subthreshold supply.
4. The introduced body-biasing method requires transistors that are larger than minimum size and have high capacitance. Moreover, body biasing requires triple-well NMOS transistors, which occupy much more space than bulk NMOS devices. Thus, this method is mostly suitable for analog circuits, such as the work of this thesis, rather than VLSI digital chips.

Studying and suggesting ways to increase the robustness of large scale digital circuits operating in the subthreshold is an on-going research topic.

5. The level shifter used in the signal processing unit was the most conventional one used by researchers. Suggesting and applying a more enhanced level shifter with less power consumption and higher speed can be done.
6. If MOSFETs operating in the subthreshold region show sensitivity to radiation, the sensor can be embedded into the signal processing unit. This results in significant power saving and space. MOSFET sensitivity to radiation in the subthreshold region and the possibility of merging the sensor, readout circuit and SPU can be investigated.
7. Varactors occupy much more space than transistors. Investigating other ways to accurately convert dose measurement to frequency using CMOS circuit design in the subthreshold region can be studied.
8. The purposed NDBB and PDBB circuits can be applied to other applications of CMOS circuits operating in the subthreshold region for enhanced robustness.

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