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"DEVELOPMENT OF GaAs CHARGE-COUPLED DEVICES"

by

Robert I. James, B.Eng.

**A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfilment of
the requirements for the degree of**

Master of Engineering

**Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Carleton University
Ottawa, Ontario
March, 1993
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submitted by Robert James, B.Eng.
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the degree of Master of Engineering

Thesis Supervisor

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ABSTRACT

The design, fabrication and operation of GaAs cermet- and capacitive-gate charge-coupled devices (CCDs) is described. Performance trade-offs in the design of GaAs CCDs for signal processing applications are evaluated in terms of physical design parameters (mark/space ratio) and substrate material specifications. An in-depth examination of the influence of the cermet-gate structure on device performance is provided. The incorporation of this structure has been shown to improve the charge transfer efficiency and dynamic range of the CCD, thereby extending the bandwidth and range of useful operation of these devices. Experimental characterization of the charge transfer efficiency and dynamic range has been performed at clock frequencies up to 1 GHz; this upper limit is imposed by available test circuitry. These devices exhibit transfer efficiency in excess of 0.996 at 1 GHz with a sensitivity of -30 dBm and approximately 40 dB of dynamic range. The demonstration of fair performance of a cermet-gate CCD fabricated on a MESFET-compatible substrate indicates the potential for successful monolithic integration of these devices with GaAs D-MESFET circuitry.

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LIST OF SYMBOLS

ϕ_b	Schottky barrier height
λ	Wavelength
ψ	Channel potential (V)
ρ	Charge density
ϵ	Charge transfer inefficiency of a single electrode
ϵ_s	Semiconductor permittivity (F/cm)
η	Activation efficiency
Ω	Ohms
π	Pi = 3.141592
ϕ_x	Phase x clock electrode (for x = 1 to 4)
$\text{\AA}$	Angstroms
$^\circ$	Degrees
μm	Microns
δQ	Change in quantity of charge
δV	Change in potential
A	CCD output amplitude
ABME	Air bridge metal definition mask
ABVI	Air bridge via definition mask
A_i	Amplitude of CCD input signal
Al	Aluminum
A_o	CCD amplitude scaling factor
Ar	Argon
As	Arsenic
Au	Gold
Baume	Unit of measure for specific gravity
BBD	Bucket Brigade Device
BNR	Bell-Northern Research
C	Coulombs or degrees Celsius
CCD	Charge-Coupled Device
C_d	Depletion capacitance
cermet	Ceramic metal
CF_4	Carbon tetrafluoride
CGAS15	CCD mask set designator
CGCCD	Capacitive-gate Charge-Coupled Device
C_{gm}	Granular metal capacitance
cm	Centimetre

CMCCD	Cermet-gate Charge-Coupled Device
CMET	Cermet etch definition mask
cos	Cosine
Cr	Chromium
CRC	Communications Research Centre
CTE	Charge Transfer Efficiency
C-V	Capacitance-Voltage
dB	Decibel
dBm	Decibels above 1 milliWatt of power
DC	Direct Current
DI	De-ionized (water)
D-MESFET	Depletion-mode MESFET
DRAM	Dynamic Random Access Memory
E_i	Input signal to CCD filter
E_o	CCD filter output signal
ehp	Electron-hole pair
ETF	Engineering Test Fixture
F	Farads
FATFET	FET with a gate which has been extended in length
F_c	Clock frequency
FDA	Floating Diffusion Amplifier
FET	Field Effect Transistor
FLME	First level metal definition mask
F_s	Signal frequency
Ga	Gallium
GaAs	Gallium Arsenide
GATE	FET gate and clock electrode definition mask
Ge	Germanium
GHz	Gigahertz
G_x	Gate x (for $x = 1, 2, 3$)
H_2	Hydrogen
H_2O	Water
H_2O_2	Hydrogen peroxide
HCl	Hydrochloric acid
HDTV	High Definition Television
HEMT	High Electron Mobility Transistor
HF	Hydrofluoric acid
HMDS	Photoresist adhesion promoter
I	Current

IC	Integrated Circuit
I_d	Diode current
I/P	Input
IPA	Iso-propyl alcohol
I_s	Diode saturation current
ITO	Indium Tin Oxide
I-V	Current-Voltage
k	Boltzmann's constant = 1.38×10^{-23} J/K
kÅ	Kilo-Angstrom
KAuCN	Potassium-gold-cyanide
kHz	Kilohertz
L_g	CCD cell gap length
mA	Milliampere
MESA	Transport channel mesa etch mask
MESFET	Metal-Semiconductor Field Effect Transistor
MHz	Megahertz
MMIC	Monolithic Microwave Integrated Circuit
MOCVD	Metal-Organic Chemical Vapor Deposition
MOS	Metal-Oxide-Semiconductor
M/S	Mark / Space
MSR	Mark-to-Space Ratio
n	Diode ideality factor
N_2	Nitrogen
N_A	Acceptor carrier concentration (atoms/cm ³)
N_D	Donor carrier concentration (atoms/cm ³)
NH_4OH	Ammonium hydroxide
Ni	Nickel
nm	Nanometre
ns	Nanosecond
N_s	Sheet carrier concentration
N_i'	Implant fluence
N_t	Number of single-electrode transfers
O	Oxygen
OHMC	Ohmic contact definition mask
O/P	Output
PC	Personal computer
PCM	Process control monitor
PECVD	Plasma Enhanced Chemical Vapor Deposition
PPM	Precision Photomask Limited

PR	Photoresist
Pt	Platinum
q	Electronic charge = 1.609×10^{-23} Coulombs
R_D	Reset drain
RF	Radio frequency
R_G	Reset gate
R_{gm}	Granular metal series resistance
rpm	Revolutions per minute
R_s	Series resistance or Hall coefficient
RTA	Rapid Thermal Anneal
SAG	Self-aligned gate
Se	Selenium
SEM	Scanning Electron Microscope
Si	Silicon
SIMS	Secondary Ion Mass Spectroscopy
Si_3N_4	Silicon nitride
SLR	Single Lens Reflex
Sn	Tin
T	Transport channel thickness (μm) or temperature (K)
TDI	Time Delay and Integration
Te	Tellurium
TFT	Titanium etchant
Ti	Titanium
Ti-W	Titanium-Tungsten
TLM	Transmission line model
TRIUMF	Tri-University Meson Facility
t_x	Time x (for $x = 1, 2, 3, \dots$)
UHF	Ultra High Frequency
UV	Ultraviolet
V	Volt or Voltage
V_{bi}	Built-in voltage (V)
VCR	Video Cassette Recorder
VdP	Van derPauw
VHF	Very High Frequency
V_p	Pinchoff voltage (V)
W	Depletion region depth (μm) or Tungsten
W_k	CCD Transfer function weights
X_j	Junction depth (cm)
z	Z-transform operator

CHAPTER 1

INTRODUCTION

This thesis examines the development of GaAs charge-coupled devices (CCDs). To introduce this topic, a basic description of the device and its operation is offered and the original development of silicon CCDs and their applications is described. Next, the advantages of GaAs CCDs and their niche applications are presented to introduce the motivation for the work which led to this thesis. This introduction concludes with an outline of the thesis organization.

1.1 DESCRIPTION, INITIAL DEVELOPMENT AND APPLICATIONS OF THE CCD

While a detailed description of the operation of the CCD is reserved for chapter two, the basic operation of this device can be summarized as follows. A charge-coupled device is used to sample an applied electrical (or optical) signal, shift the discrete charge packets (which result from the sampling operation) through a sequence of distinct transfer cells and then recover the original (delayed) signal at the output of the device.

The concepts underlying the charge-coupled device (CCD) were first developed in 1970 as a result of efforts by Boyle and Smith of Bell Labs [1.1] to produce a semiconductor analog to the magnetic bubble memory. Their work produced a charge transfer device whose structure consisted of a closely packed array of MOS capacitors

with diodes at the input and output ports on a silicon substrate. Since MOS fabrication techniques were fairly well established, fabrication of these devices was realized shortly thereafter.

The apparent simplicity of the CCD concept and initial silicon processing techniques led many researchers to propose and develop numerous applications of CCDs as imaging devices and semiconductor memories. Applications in signal processing soon followed, where the initial development of shift registers led to time-delay and integration (TDI) filter processing and then more complex transversal filters. The application of CCDs in these areas is considered in more detail in the following sections.

1.1.1 Memory Devices

As previously stated, the CCD was originally intended as a semiconductor memory device. For this application, charge is transferred serially to a given cell within a large MOS capacitor array and then confined within that cell by maintaining an appropriate bias on the surrounding capacitor electrodes to trap the signal charge within a potential well. When addressed, the charge would be clocked serially to the readout node. The concept of a capacitor array as an addressable memory element led researchers to the development of the Dynamic Random Access Memory (DRAM) cell. Since DRAM memory can be addressed randomly rather than serially, the advantages of the DRAM soon led to the demise of the CCD as a memory element.

1.1.2 Imaging

Much of the early excitement generated by the development of the CCD was due to its potential use in electronic imaging applications. The CCD imagers used in the Hubble Space Telescope as well as in VCR, HDTV and even many SLR cameras all reflect the success of this technology.

In its application as an imaging device, the clock electrodes are generally made of a highly conductive, transparent material such as polysilicon or indium-tin-oxide (ITO). Light incident on the semiconductor surface will generate electron-hole pairs (ehp) within the substrate. The minority charge carriers (electrons for p-type silicon) will then be integrated over an imaging time frame and then stored in an appropriately biased potential well. At the end of the imaging period, the charge is clocked to the readout register as quickly as possible to reduce the possibility of smear induced by ehp generation within the substrate during the readout phase. Large imaging arrays can be implemented by performing the readout operation in two stages. The signal charges of all pixel rows are first read out simultaneously to an output buffer which is physically separate from the imaging area. These data are then multiplexed and then read out serially during the following imaging time frame to an external buffer for subsequent processing. Such imaging arrays can now be fabricated using the mature silicon processes developed for the multi-Mbit DRAM memory cells. In fact, imaging areas greater than one square inch are presently used for HDTV recording.

1.1.3 Signal processing

The most obvious application of a charge transfer device is that of a shift register. The ability to control the amount of delay between the input and output simply by varying the clock rate adds considerable flexibility to a circuit design.

Of more interest to systems designers, though, is the feasibility of integrating complex signal processing functions using charge-coupled devices. The transfer function of most analog filters can be written in the general form

$$E_o = \sum_{k=0}^{N-1} W_k \cdot E_i(t-kT)$$

where E_o is the output signal, $E_i(t-kT)$ represents the input signal E_i delayed by k times the delay period T and W_k are the weights assigned to the delayed components of the input signal. With some modification to the transfer electrode structure, this response can be integrated using CCDs in either a serial-in/parallel-out (SI/PO) configuration (i.e. as a transversal filter) or by using the CCD in a parallel-in/serial-out (PI/SO) time delay and integration (TDI) mode, as illustrated in figure 1.1 (after [1.2], figure 3-20). In either case, the delay terms $E_i(t-kT)$ are acquired by tapping the CCD transfer array at appropriate intervals (usually after every delay stage) and either sensing the current size of the delayed charge packet or injecting charge into the array for subsequent delay and integration. The weights W_k can either be integrated into the CCD structure or added externally for greater flexibility (using any of several published techniques such as those documented in [1.3] or [1.4]). The summation is accomplished by integrating the delayed charge packets at the output node. Using these techniques, CCD filters for

$$E_o = \sum_{k=0}^{N-1} W_k \cdot E_i(t-kT)$$

SI/PI Simultaneous Summation
(Transversal Filter)

PI/SI Progressive Summation
(Time Delay and Integration)

Figure 1.1 : 2 CCD implementations of an analog filter transfer function (after [1.2], figure 3-20).

signal processing applications can be integrated with great flexibility, meeting the demands of most adaptive filter requirements. Since the CCD is an analog device, it does not require the pre-processing (i.e. analog to digital conversion and subsequent DAC) necessary with digital signal processor (DSP) filter implementations. Thus, considerable savings in circuit area can be realized using charge-coupled device technology.

1.2 REQUIREMENT AND ADVANTAGES OF GaAs CCDs

As signal processing technology began to mature, requirements were established for complex signal processing functions with extremely wide bandwidths. To meet these requirements, CCDs fabricated on gallium arsenide (GaAs) substrates were proposed as early as 1972 [1.5] in an attempt to harness the superior electrical characteristics inherent to GaAs. Some of these advantages can be summarized as follows.

1. The mobility of electrons travelling through a GaAs substrate can be greater than five times that of silicon at low to medium electric fields. Since higher mobility leads to higher electron velocities, the transit time of a given charge packet across an interelectrode gap will be proportionately less. For a CCD which is operated in such a way that the maximum frequency is limited by the device transit time, a GaAs CCD will operate significantly faster than a similar CCD fabricated on a silicon substrate.

2. Since the higher electron mobility of GaAs devices is achieved at low electric fields, the superior electron velocities are achieved with lower clock power dissipation.

3. With current growth techniques, the GaAs substrate can easily be rendered semi-insulating. This reduces the stray capacitance of the device with consequent performance advantages. The semi-insulating substrate also provides natural device isolation; fabrication is thus easier because channel stops do not need to be created. Additionally, the low substrate capacitance implies a high charge / voltage conversion efficiency for better sensitivity than is available with silicon CCDs.

4. For military or space applications, the radiation hardness of GaAs Schottky diode-based circuitry is superior to that of silicon MOS devices [1.6], [1.7].

In spite of the potential advantages of GaAs CCDs, processing immaturity prevented the realization of a GaAs CCD until 1977 [1.8]. Since then, a number of laboratories have demonstrated GaAs CCDs ([1.9], [1.10], [1.11] and [1.12] among others). These CCDs use a Schottky gate structure instead of MOS capacitors so that many of the problems associated with the older silicon technology (potential build up of oxide charge, surface states and blooming) are not relevant to the buried channel GaAs Schottky-barrier CCD.

Using GaAs technology, record speeds for CCDs were soon realized. These devices have been shown to be operational at clock rates up to 4.2 GHz [1.13] and have shown excellent transfer efficiencies of 0.9999 at lower clock rates. While the performance of these devices has been impressive, several problems still remained to be solved, as discussed below.

The operational requirements for GaAs CCDs generally dictate that the CCD transport layer be made of a thick, lightly doped layer (typically 1 micron of $1-5 \times 10^{16} \text{ cm}^{-3}$). (The layer requirements for GaAs CCDs are discussed in more detail in chapter two of this thesis (device design).) Any support circuitry for this device using standard GaAs MESFET technology would require a substrate doping of typically 2×10^{17} , 0.3 microns thick. The incompatibility between these requirements has prevented the monolithic integration of CCDs with their associated support circuitry.

Secondly, close examination of the potential distribution of a GaAs CCD reveals that a potential trough exists in the substrate region below the interelectrode gaps [1.14] and is especially significant for gap lengths greater than 1 micron. Such a potential trough will degrade charge transfer in the channel direction because part of the signal charge packet will become trapped in this deeper potential well during the transfer sequence. The charge may be released at a later time to introduce distortion in the output signal.

A solution to these problems was first demonstrated by Higgins et al. at the Rockwell International Microelectronics Research and Development Center with the introduction of the resistive gate CCD [1.15]. Their device structure was novel in that a resistive cermet film was deposited over both the gate metallizations and the inter-electrode gaps to provide a linear variation of the surface potential in the inter-electrode gap region. While a detailed analysis of the effect of this film is given in the next chapter of this thesis, the advantages of such a device can be summarized easily.

The active layer requirements of capacitive-gate CCDs (CGCCDs; so called to distinguish these devices from the resistive- or cermet-gate CCD, denoted CMCCD) were driven by the need to provide high fringing fields in the substrate in the regions of the inter-electrode gaps. Since an electric field in the gap region of a CMCCD is ensured by the potential variation across the cermet film, the substrate requirements can be relaxed to enable the development of CCDs on FET-compatible substrates. Since this field can be shown to be monotonic [1.16], potential troughs in the gap region are eliminated so that better transfer efficiency at a given frequency is obtained. Similarly, the electron transit time for a given transfer inefficiency is reduced so that higher frequency operation can be achieved. The gapless nature of these devices implies that the region in which the signal charge is confined will extend into the gap between

electrodes. This increases the effective cell size to provide a higher dynamic range. Finally, since the CMCCD can be fabricated using thinner active layers, it should be more immune to bulk trapping effects.

The development of a VHF/UHF agile bandpass filter which provides 60 dB of dynamic range for low, high and bandpass filter operations at a 1.0 GHz sampling rate [1.17], a GaAs detector array/multiplexor which multiplexes the outputs of 32 photodiodes at a 1.0 GHz clock rate [1.18] and components of a wideband data acquisition system [1.16] using cermet-gate charge-coupled devices all serve to verify the relevance and capabilities of this technology.

1.3 THESIS MOTIVATION AND OVERVIEW

The present work is an attempt to first reproduce the success of other researchers using the GaAs cermet-gate CCD structure, to examine some of the trade-offs involved in the design and operation of these devices and then to investigate the potential for monolithic integration of GaAs CCDs with their support circuitry for signal processing applications. This work has been broken down into three distinct tasks. The definition and resolution of each of these tasks is assigned to a chapter of this thesis as follows.

An analysis of the operation and design of GaAs CCDs forms the basis for the second chapter. Performance trade-offs in the design of these devices are evaluated in terms of substrate material specifications and physical design parameters (transfer cell design, including the mark-to-space ratio, as well as the structures and circuitry

necessary for the injection and detection of signal charge). The influence of alternate processing options such as the cermet-gate structure are also examined. This chapter concludes with a description of a mask set which was conceived to investigate some of the trade-offs involved in CCD design.

In chapter three, fabrication processes for capacitive-gate, cermet-gate and self-aligned gate CCD technologies are described. These processes were developed to fabricate GaAs CCDs at the Microelectronics Facility of the Communications Research Centre (CRC). Where significant process development and enhancements were necessary to fabricate these devices, this work is presented.

Chapter four describes the work which was performed for the electrical characterization of the CCDs fabricated at CRC. The measurement setup, DC and RF characterization techniques and the results are described in detail. Substantial effort has also been performed to validate the measurement setup and techniques; this work is also described.

Finally, the design, fabrication and evaluation of these devices are summarized in chapter five. This chapter also includes some concluding remarks and considerations for future work.

CHAPTER 2

DEVICE DESIGN

This chapter is intended to present and discuss many of the issues relevant to the design and operation of charge-coupled devices. First, a description of the operation of CCDs is given to illustrate the device structure and requirements. Next, design issues are considered; issues to be examined include the choice of transport channel material parameters, geometric concerns and the design of circuitry used for the injection and sensing of the signal charge. Additionally, some alternative technologies used to form the transport electrode structures will be presented, as they impact the design choices. The chapter will conclude with the description of a mask set which was designed to quantify the influence of some of the design parameters.

2.1 CCD OPERATION

As described previously, a CCD designed for signal processing applications samples an input electrical signal, transfers the resultant charge packet through a long array of transfer cells and then allows the delayed signal to be coupled to external circuitry. For these operations, three distinct regions of a CCD can be identified; these are the charge input, transfer and sensing regions shown in figure 2.1. The operation of each of these regions is considered in more detail as follows.

Figure 2.1 : Cross-section of a charge-coupled device

2.1.1 Charge input

The charge input region of the CCD consists of an input ohmic contact and two Schottky gate contacts, labelled I/P, G_1 (gate 1) and G_2 (gate 2), respectively in figure 2.1. This structure is used to inject and meter a fixed amount of charge into the charge transfer region of the substrate. When the device is biased appropriately (injection techniques and biasing arrangements are discussed in more detail in section 2.2.3.1), the size of the injected charge packet is linearly proportional to the voltage difference applied between G_1 and G_2 . Thus the CCD operates as an analog device with high linearity and broad dynamic range.

2.1.2 Charge transfer

To understand the charge transfer mechanism, some preliminary concepts must be reviewed. When a potential is applied to any of the clock electrodes (which are fabricated as Schottky contacts on the GaAs substrate), an associated change in the surface potential of the substrate in the vicinity of that electrode will occur; this change is almost directly proportional to the applied voltage. Local increases in the potential of a substrate are referred to as 'potential wells'; the depth of this well corresponds to the channel potential of this region with respect to the potential of the (unbiased) substrate. Thus, an increase in the potential applied to one of the clock electrodes will increase the depth of the corresponding potential well. The clock electrodes are designed to be close enough together that the associated potential wells couple. Since mobile charge (electrons for the n-type GaAs substrates used) will accumulate in the region of highest potential, charge transfer can take place between adjacent CCD cells simply by modulating the relative potential well depths with appropriate timing.

The actual transfer of charge from the input region through the CCD can be described as follows, with reference to figure 2.2. Once the charge packet has been injected into the substrate, it is initially confined to a potential well formed beneath the G_2 electrode (immediately adjacent to the first clock electrode, as shown in the figure). In this position, it is available for charge transfer. At time t_1 , the voltage of the first clock electrode is raised to create a deep potential well beneath ϕ_1 while ϕ_2 is maintained at a low potential. The charge moves into the charge transfer region by means of both drift and diffusive processes and is momentarily confined below the first ϕ_1 electrode by the potential barrier of ϕ_2 at time t_2 .

Figure 2.2 : Illustration of the charge transfer sequence through a CCD:
 (a) potential diagrams as a function of time;
 (b) timing diagrams for the clock electrodes.

At time t_2 , the potential of ϕ_2 is raised so that the $\phi_1 - \phi_2$ potential wells couple; charge begins to flow from ϕ_1 to ϕ_2 at time t_4 when the potential minimum below ϕ_2 is equal to that of ϕ_1 . At time t_5 , the potential at ϕ_1 is reduced so that the remainder of the charge begins to move from ϕ_1 to the deeper potential well of ϕ_2 . The transfer is complete at time t_6 with the charge isolated from the input to complete the first transfer operation. In the same manner, periodic clock waveforms are used to confine and

transfer the charge through the remainder of the transfer region. Note that if a four-phase clock system is used (such that each electrode is activated with clock pulses which have a relative phase separation of 90 degrees from those of its neighbours), there will always be one completely depleted region between each charge packet to prevent the charge from flowing back towards the input node.

2.1.3 Charge sensing

Once the charge packet has arrived at the last electrode of the charge transfer region, the final stage of the CCD will move the charge packet to the output node where it is converted to an output voltage and then amplified. The output region consists of 2 Schottky contacts and 2 ohmic contacts to form the output diode and field effect transistor (FET) shown in figure 2.1. The reset drain (R_d) and gate (R_g) of the output circuitry are biased in such a way that the FET resets the potential of the output ohmic contact node immediately prior to the arrival of the signal charge packet. Proper biasing of the G_3 electrode will draw the charge from the potential well below the final ϕ_4 clock electrode to the output node. A voltage which is linearly proportional to the size of the charge packet appearing at the output node will then be sensed by an output amplifier and buffer stage. This buffered output signal can then be coupled directly to the next stage of a larger chip or fed to an off-chip amplifier for examination or further processing. The design and operation of the output stage are considered in more detail in section 2.2.3.2.

This completes the description of the operation of charge-coupled devices. The next sections qualitatively describe the design and optimization of the transport channel

material parameters and various aspects of the device geometry, including the input injection and output sensing structures.

2.2 DESIGN CONSIDERATIONS

2.2.1 Transport channel material parameters

The design of a CCD begins with an analysis of the electrostatic potential within the transport channel of the CCD. The potential distribution profile is used to evaluate the design trade-offs in the choices of the transport channel doping characteristics and the geometry of the transport electrode structure.

The potential distributions are calculated by solving Poisson's equation (which defines the channel potential ψ in terms of the charge density ρ , as shown in equation 2.1) subject to the appropriate boundary conditions. While a rigorous solution is beyond the scope of this thesis, previously published results are presented which adequately illustrate the required concepts. (The reader is referred to [2.1], [2.2] and [2.3] for an in-depth discussion of modelling charge transfer within a CCD.)

$$\nabla^2 \psi(x,y) = \frac{\rho(x,y)}{\epsilon_s} \quad (2.1)$$

Figure 2.3 (after Deyhimy et al., [2.4]) shows an approximate solution for the potential profile below and between two consecutive clock electrodes within the transport channel of a capacitive-gate CCD. For this profile, both electrodes are held at the same potential and it is assumed that there is no signal charge within the channel. The potential contours around the edges of the electrodes give rise to an electric field within the gap regions; carrier drift within this 'fringing field' represents one of the main processes by which charge is transferred between successive charge storage regions. Note that for the capacitive-gate structure shown, the substrate potential in the interelectrode gap region is more positive than the potential in the region below the clock electrodes. Thus, a potential trough exists (with a corresponding null in the fringing field) which will trap charge passing through this region of the interelectrode gap. As the gap size increases, the coupling between adjacent 'potential wells' will diminish until a maximum gap size is reached whereby the potential wells are completely uncoupled and the fringing fields are not sufficient to enable the transfer of a packet of charge. This maximum gap size corresponds (to a first approximation) to the lateral extent of the depletion regions from the electrodes on either side of the gap.

If we consider the edge of the gate electrode as a point metal-semiconductor contact, then for a given applied bias, the substrate in the vicinity of the contact will be depleted to a depth proportional to the net substrate charge (including ionized donors) in the depleted regions, both laterally and vertically. Note that if we neglect surface charge, any signal charge within the channel and we assume the substrate is uniformly doped to a depth beyond the depletion region depth, then the substrate will be depleted laterally to the same extent that it is depleted vertically. Under these assumptions, the maximum depletion region depth will represent one-half of the gap size beyond which

Figure 2.3 : Approximate two-dimensional representation of the potential within the channel of a GaAs charge-coupled device (after Deyhimy et al. [2.4]). Labelled contours indicate the potential in volts.

charge transfer would be seriously degraded. Thus, to examine the effect of channel doping and thickness, potential contours represented by the depletion region boundaries can be calculated to illustrate the appropriate trends.

The depletion region widths as a function of bias have been calculated for two typical substrate specifications; these results are shown in Table 2.1. This table also lists an assumed maximum gap size beyond which charge transfer would be degraded; this value corresponds to twice the maximum depletion width. These calculations assume

Table 2.1 : Depletion width as a function of doping concentration and applied voltage.

Doping Concentration (cm ⁻³)	Applied Voltage (V)	Depletion Width (μm)	Assumed Maximum Gap Size (μm)
2×10^{16}	0	0.26	0.52
	2	0.45	0.90
	4	0.59	1.18
	6	0.70	1.40
2×10^{17}	0	0.08	0.16
	2	0.14	0.28
	4	0.19	0.38
	6	0.22	0.44

that there is no charge stored within either the semiconductor bulk or interface trap states, the substrate is uniformly doped and that the layer interfaces are abrupt. Under these conditions, the depletion region width of a GaAs Schottky barrier can be calculated as [2.5]:

$$W = \sqrt{\frac{2\epsilon_s}{qN_d} \left[V_M - V - \frac{kT}{q} \right]} \quad (2.2)$$

where W = Depletion region depth (cm);

ϵ_s = GaAs permittivity (F/cm);

q = Electronic charge = 1.602×10^{-19} C;

N_d = Donor concentration (cm^{-3});

V_{bi} = Built-in voltage (V);

V = Applied voltage (V); and

kT/q = Thermal voltage = 0.0259 V (@300K)

From the data in Table 2.1, it can be seen that the excursion of the depletion region (potential well depth) into the gap region decreases as the channel doping increases. Thus, to maintain a given charge transfer efficiency when higher doped substrates are required, shorter gaps (or deeper channels) become necessary. Since gap lengths of less than 1 micron cannot be defined easily with standard lithographic techniques, considerations of yield limit the minimum practical gap length to 1 micron. To ensure adequate coupling between adjacent cells which use longer gaps, the channel doping must be reduced.

Deeper within the substrate, the potential trough illustrated in figure 2.1 is significantly reduced; the improved coupling between adjacent potential wells results in more uniform fringing fields within the gap [2.6]. Thus, for a substrate with a given carrier concentration, charge transfer should improve as the channel thickness increases. The channel thickness cannot be increased arbitrarily either, however. The pinchoff voltage of the substrate (proportional to the square of the channel thickness, as shown in equation 2.3) determines the power requirements of the clock drivers and other associated support circuitry. High power requirements for the support circuitry will increase the cost of the components and induce additional problems associated with side-gating and thermal effects. The channel thickness is usually estimated such that the pinchoff voltage does not exceed approximately 6V.

The pinchoff voltage is given by [2.7] as

$$V_p = \frac{q N_d X_j^2}{2 \epsilon_s} \quad (2.3)$$

where V_p is the pinchoff voltage (V) and X_j is the junction depth (cm) (with a maximum value corresponding to the channel thickness), all other parameters having been previously defined. Note that this equation assumes that the channel layer can be considered to be highly doped with respect to the underlying buffer layer and that the charge density within the channel is essentially independent of thickness (the epitaxially-grown substrates can be considered uniformly doped).

Finally, the dynamic range of the device is also influenced by the channel parameters. A theoretical discussion of the charge handling capability of GaAs CCDs as a function of gap length, channel doping and thickness is given in reference [2.8]; some experimental results are presented in [2.1].

To summarize, there are several requirements which must be satisfied in the choice of the CCD transport layer characteristics. These requirements are:

1. The doping profile must be sufficient to ensure that fringing fields extend completely across the inter-electrode gap in the region of the substrate through which the signal charge will transfer.
2. The pinch-off voltage of the channel must be low enough that the power requirements for quadrature clock drivers and other support circuitry can be met without great difficulty.

3. Further constraints may be imposed by the required dynamic range of the device; the maximum charge handling capability is proportional to both the doping density and the channel thickness [2.1].

Consideration of these criteria has shown that thick, lightly doped channels should be used to ensure good transfer efficiency. However, since these layers are not compatible with standard FET technology, integration of CCDs with FET drive and buffer circuitry cannot be easily accomplished. This incompatibility led to the incorporation of the cermet-gate CCD, as described in the introduction to this thesis.

The cermet film acts as a continuous voltage divider between adjacent electrodes so that the surface potential varies monotonically across the inter-electrode gap. A comparison of the potential within the substrate of a CGCCD and a cermet-gate CCD (CMCCD) is illustrated in figure 2.4 (after ref [2.9]). Note the presence of the potential trough in the gap between adjacent electrodes for the CGCCD which has been eliminated using the CMCCD structure.

Since the cermet establishes an electric field across the gap regions of the transport channel, the channel specification requiring the establishment of fringing fields may now be relaxed. Thus, fabrication of CCDs using thin, highly doped channels compatible with MESFET processes can be realized. Since a greater dynamic range can be achieved (for a given pinch-off voltage) with thin, highly doped channels [2.10], the dynamic range of CCDs fabricated using FET-compatible transport channels should prove to be at least as good as those fabricated using more conventional CCD layer structures.

Figure 2.4 : Illustration of the potential within the channel of (a) a capacitive-gate CCD and (b) a cermet-gate CCD with bias applied to the gate electrodes.

For the fabrication of CCDs used for this thesis research, two options have been exercised with respect to the doping of the transport channel. The first layer specification is established to provide a basis for comparison with CCDs which had been previously fabricated at CRC; these included a charge transport channel which was doped to a level of 2×10^{16} atoms/cm³ 1.0 micron thick. The second specification called for wafers with a transport channel layer doped 2.5×10^{17} to a depth of 0.25 microns to be compatible with the D-MESFET process at CRC.

2.2.2 Transport cell structure

The next step in the design of a charge-coupled device is to define the transport cell configuration. The configuration defines both the materials which will be used to establish the required potentials (i.e. the Schottky contact metallization) within the substrate and the cell layout geometry. The cell geometry is discussed in section 2.2.2.1; some materials options are discussed in section 2.2.2.2.

2.2.2.1 Transport cell geometry

A complete definition of a transport cell requires five parameters; the parameters to be considered are the clock electrode (gate) length, the inter-electrode gap length, the total cell width, the number of cells per pixel and the number of pixels comprising the CCD (i.e. the total CCD length). The design of CCDs generally requires intimate knowledge of the processing capabilities of the foundry, as device performance (maximum frequency, CTE, dynamic range) must be traded off against ease of fabrication. Some of the trade-offs are described below.

2.2.2.1.1 Gate/gap length

The high-frequency performance of the CCD is mostly affected by the lengths of the electrodes and inter-electrode gaps. As the total length of the cell is reduced ($1 \text{ clock electrode (gate)} + 1 \text{ inter-electrode gap} = 1 \text{ cell}$), transit times through the device become smaller leading to higher frequency performance. However, smaller cells place stringent demands on the lithographic processes used to define the transport electrodes; device yield decreases alarmingly as a function of the reduction in either gate or gap size.

The main geometric design parameter of relevance for estimation of the device performance is the mark-to-space ratio (MSR), which is defined as the ratio of the gate length to the gap length. For a given set of material parameters and total cell size, three regimes can be defined which relate the device performance to the MSR.

A. $MSR < X_1$: For low MSR (i.e. long interelectrode gaps), the transfer efficiency is limited by the formation of potential troughs within the gap regions, as discussed previously.

B. $MSR > X_2$: When the MSR is large and the gaps are small enough that they preclude the formation of potential troughs, the gate length proves to be the limiting factor for high frequency device performance. Since the surface potential in the region below the gate is pinned by the applied voltage, there is no lateral potential variation in this region. Hence, charge transport is accomplished by diffusive processes without the benefit of an electric field to enhance the transfer of charge. If this region becomes long in relation to the distance through which the charge packet will be able to diffuse within the allowed time (1/4 of the clock cycle), then part of the charge packet will not be transferred within the requisite time and the transfer efficiency is degraded.

C. $X_1 < MSR < X_2$: In this region, it is presupposed that the gaps are fairly small such that potential troughs within the gap regions are not significant. Similarly, the gate lengths are short enough that, for the clock frequency of interest, the charge packet will be able to diffuse across the gate length within the allowable time frame. Thus, this regime represents an optimum set of conditions for charge transfer.

The values X_1 and X_2 are complicated functions of the material parameters. They can either be determined by theoretical analysis and computer simulation of charge transport phenomena or by data analysis of transfer efficiency measurements of a number of CCDs with different geometrical parameters. In this work, the latter approach has been adopted to gain some insight into the magnitude of these parameters.

2.2.2.1.2 Cell width

Since the volume of the semiconductor channel beneath the clock electrodes defines the charge storage capacity, the total gate electrode area will determine the maximum achievable dynamic range for a given transport channel specification. The choice of whether to implement the required area with increased electrode width or length will depend upon the trade-off between performance and ease of fabrication, as the potential for lithographic error also increases directly with the width of each cell. Since the gate and gap lengths are generally fixed by other performance requirements, the width is chosen such that the total gate electrode area is sufficient to meet the dynamic range requirements of the device.

2.2.2.1.3 CCD length

For a CCD with non-ideal CTE, any signal which is transferred through a number of CCD stages will undergo some degradation. This signal degradation increases exponentially with the number of transfers, as indicated in the equation used to define CTE [2.24]:

$$A = A_0 \exp \left[-N_t (1 - CTE) \left[1 - \cos \left(\frac{2\pi F_s}{F_c} \right) \right] \right] \quad (2.4)$$

In this equation, A is the CCD output amplitude in volts, A_0 is a constant voltage proportional to the input amplitude and non-frequency-dependent losses, N_t is the number of single electrode transfers, CTE is the charge transfer efficiency and F_s and

F_s represent the signal and clock frequencies, respectively. Thus, for minimum signal distortion, a CCD should be designed to have the smallest possible number of transfer stages which meet the system requirements. For filter applications, the number of pixels used will be determined by the number of coefficients required for the minimum resolution of the desired filter transfer function.

2.2.2.1.4 Number of cells per pixel

The clocking scheme (which defines the required number of cells per pixel) to be used for the CCD will depend on the processing technology available and the availability of suitable clock driver circuitry. CCDs have previously been designed with 2,3,4 and n-phase clocks. In general, the smaller the number of clock phases which are used, the smaller the number of clock electrodes which must be successfully fabricated.

As shown earlier in figure 2.2, the use of a four-phase clocking system guarantees that there will always be at least one depleted region between each successive charge packet. Thus, isolation of successive charge packets can be assured to prevent signal distortion which arises when two or more signals intermix. One of the drawbacks associated with this system is the requirement for air bridges or some other cross-over interconnect technique to form the connections between electrodes of adjacent stages.

Many two-phase clock systems have also been devised [2.11, 2.12] as adaptations from the earlier four-phase designs. Each two-phase electrode covers the equivalent of two transfer cells. In a typical design, the gate over every second transfer cell is recessed to establish regions of varying surface potentials under each electrode. The change in potential creates a built-in field which moves charge from the input towards the output

side of the electrode. Thus, while the clock pulses are used to move the charge from one group of two cells to the next, the built-in field serves to prevent the charge packets from moving backwards on the next clock cycle by confining them behind a potential barrier on the output side of the electrode.

While two-phase drivers would be easy to obtain, the maximum dynamic range of these devices is a function of the barrier height which is imposed between the two sides of a cell. The additional processing complexity associated with the creation of potential wells below alternate gates uniformly across a wafer did not make up for the benefit of not requiring cross-over interconnections.

In comparison to the four-phase clock system, the use of three-phase clocks will degrade the charge confinement while still requiring a cross-over interconnect process. While accurate, stable high-frequency quadrature clock drivers are not common, they can be fabricated using 90- and 180-degree phase-shifting techniques. Since a three-phase clock driver circuit cannot easily be subdivided into symmetric components, the procurement or fabrication of three-phase drivers would be considerably more difficult than either two- or four-phase clock driver circuits.

This completes the list of geometric considerations relevant to the design of the charge transport cell. Before the cell design can be completed, however, consideration must be given to the materials which are used to form the Schottky diodes of the individual transport cells on the GaAs substrate. Three materials are considered here: these are Ti/Pt/Au, Ti/Pt/Au on cermet (SiO/Cr) and ITO (Indium/Tin/Oxide).

2.2.2.2 Transport cell structure: materials

2.2.2.2.1 Standard Schottky metallization

The capacitive gate CCDs use a metallization consisting of 300Å titanium, 1000Å platinum and 3000Å gold for the formation of Schottky contacts on GaAs. Gold is used for the bulk of the contact because it combines the properties of very low sheet resistance with high barrier height on n-type GaAs. The titanium interlayer is used to improve the adhesion of gold on GaAs while the platinum acts as a diffusion barrier to prevent the gold from diffusing through the GaAs substrate under high current stress. Thus, the platinum interlayer is used to improve the reliability of the Schottky diodes [2.13]. This metallization scheme has been adopted as the standard FET gate and Schottky diode metallization of a number of commercial foundries [2.14], as well as the Communications Research Centre (CRC) where the devices were ultimately fabricated.

2.2.2.2.2 Cermet-gate metallization

The advantages of using a ceramic/metal (cermet) film within the gaps of a CCD have been described in a preceding section. Cermet-gate devices have been designed such that a cermet film is deposited in a continuous sheet across the top of the transport channel mesa. The standard Schottky diode metallization described above is then evaporated in the appropriate pattern to form the clock electrodes on top of the cermet film. Thus, a structure is defined which consists of a metal (Ti/Pt/Au) contact on a cermet/GaAs Schottky diode. The properties of this diode are examined further as follows.

A typical conduction model for Schottky diodes consists of a resistance R_s in series with a distributed network which itself consists of an ideal diode (represented here by the parallel combination of its depletion capacitance C_d and small-signal conductance g_d) and the impedance (a parallel combination of a resistance R_{cm} and capacitance C_{cm}) of the contact metal. This model is shown in figure 2.5. For standard metallization schemes, the influence of the parallel resistance R_{cm} and capacitance C_{cm} shown in the model can usually be neglected [2.15]. In the case of granular metal films (of which cermet is an example), the resistance and capacitance of the metal film can be comparable to that of the barrier and cannot be neglected. Low frequency (10 KHz) measurements of the model parameters of a structure which is similar to that used for the present work have been performed by LeNoble [2.2] and yield the parameters shown in Table 2.2 (note that the values have been scaled to the gap length). Parameters of the equivalent ideal diode shown in the model of figure 2.5 have been measured and are also listed in Table 2.2. These parameters are based on a fit to the standard diode conduction equation [2.16]:

$$I_d = I_s \left[\exp \left(\frac{qV_d}{nkT} \right) - 1 \right] \quad (2.5)$$

where I_d = Diode current (A);

I_s = Saturation current (A);

q = Electronic charge = 1.602×10^{-19} C;

V_d = Diode voltage (V);

n = Ideality factor;

T = Absolute temperature (K); and

k = Boltzmann's constant = 1.381×10^{-23} J/K.

Figure 2.5 : Schottky diode conduction model

The barrier height ϕ_B is calculated from the saturation current; R_p (the inverse of the small-signal conductance g_d) is derived from the slope of the diode current-voltage (I-V) characteristic. Table 2.2 lists most of the diode parameters as measured before and after a 10-second anneal at 400° Celsius in a rapid thermal annealing (RTA) oven. The changes in the cermet Schottky diode as a result of thermal annealing include a significant increase in the Schottky barrier height (with a corresponding reduction in leakage current) and an improvement in the ideality factor, as has been previously reported [2.17]. A possible explanation for these changes follows from the fact that the barrier heights of metal-semiconductor junctions are known to be surface-state dominated [2.18]. Thermal processing may then be expected to increase the barrier height by annealing out the defects which give rise to these states. This explanation is supported by the observation that the barrier height increases directly with the annealing temperature in the range between 250 and 500 degrees Celsius. The large series resistance represents the bulk resistance of the cermet film.

While this analysis has been performed for a structure in which the cermet underlies the Ti/Pt/Au contacts, a design option exists whereby the contacts can be defined before the deposition of the cermet. While the implications of this change are not clear,

Table 2.2 : Cermet-GaAs Schottky diode model parameters

parameter	value	
	pre-anneal	post-anneal
R_{cm} (K $\Omega/\mu\text{m}$)		55
C_{cm} (pF/ μm)		0.8
C_d (fF/ μm)		15
n	1.262	1.228
ϕ_B (V)	0.605	0.643
I_s (nA)	2.19	0.490
R_s (Ω)	229	475
R_p (M Ω)	2.20	15.30

several comments regarding this structure may be made. When the former structure is used, the complex nature of the cermet impedance implies an equivalent RC time constant which will affect the shape of the signal applied to the top electrode, as sensed at the GaAs surface. This time constant will act to increase both the rise and fall times of the clock signal. Since the transfer efficiency is sensitive to the shape of the applied signal, increasing as a function of pulse fall time (for a constant pulse repetition rate) while remaining relatively insensitive to the pulse rise time [2.19], the application of the clock waveforms to the top of the cermet film rather than the GaAs surface is expected to result in performance enhancements. Ultimately, however, the actual decision as to the position of the cermet should be made based on the achievable barrier height (which determines the leakage current) of the resulting junction.

2.2.2.2.3 Indium Tin Oxide (ITO)

An alternative gate process involves the replacement of the standard Ti-Pt-Au gate metallization with a transparent metal such as Indium-Tin-Oxide (ITO). Since ITO has a high transmittance in the wavelengths of the visible spectrum, a CCD with ITO gates could be used as an optical detector. CCD performance can then be evaluated both in terms of its charge transfer properties and its potential for use in imaging applications. Due to time constraints, this topic has not been pursued as part of this thesis.

This completes the list of design considerations relating to the transport cell structure. The design of the input and output circuitry is considered in the next section.

2.2.3 Input and output circuitry

The choice of cell width and minimum gap spacing have already been determined as part of the charge transport cell considerations. The remaining design parameters relevant to the input cell include the number and size of the input gates used to control the charge injection and the doping of these diodes. Design of the output cell is usually limited to the choice of architectures to be used for the sensing of the signal charge. The geometrical design of the output node generally follows that of the input region.

2.2.3.1 Input injection

Charge injection into the CCD transport channel can be performed in a number of ways. All of the common techniques rely on the use of a number of input diodes to control the amount of charge which is allowed to enter the transfer region of the device. A study of a number of input injection techniques [2.20] has shown that a modified version of the 'potential equilibration' technique provides the best linearity among the techniques tested for both surface and buried-channel CCDs. With this method, two input gates are used; the input signal is applied to the second gate while the first is held at a fixed DC potential. In the standard technique (illustrated in figure 2.6), the ohmic contact potential is initially set such that G_1 is reverse-biased. Charge injection is accomplished by pulsing the ohmic contact negatively so that the G_1 and G_2 diodes become momentarily forward biased. A charge packet proportional to the capacitances of each of the diodes will fill the potential wells created within the substrate beneath each gate electrode. In so doing, the substrate potentials of the adjacent diodes will tend to reach equilibrium. When the ohmic contact potential is reset back to its high state, excess charge spills back to the ohmic contact, so that the amount of charge available for transfer will be proportional to the difference in potential between G_1 and G_2 .

In the course of this work, it has been found that the application of a positive DC bias to the input ohmic contact allows sufficient leakage current to inject a full well of charge through the input diodes. Since the ohmic contact does not have to be pulsed in this regime, a potentially large source of high frequency noise is eliminated. This enhancement has the added benefit of simplifying the measurement apparatus.

Figure 2.6 : Potential equilibration charge injection technique.

Techniques employing a single input gate have also been considered. In such schemes, the signal is applied to either the ohmic contact or the Schottky gate. The alternate electrode is pulsed appropriately to inject charge into the substrate. Because of the nonlinear capacitance-voltage relationship in either forward or reverse-bias modes, these techniques suffer from strong non-linearities in the signal to charge conversion process.

Thus the optimum input cell design employs an ohmic contact and two input gates. From the previous analysis, it is apparent that the size of the injected charge packet will always be smaller than the full well capability of the G_2 diode. Thus, in order to inject

a full well of charge into the transfer region, the length of gate G_2 should be greater than the length of the transfer gates.

The spacing between gates G_1 , G_2 and ϕ_1 should be as small as possible so that the potential barriers between the input gates are minimized. Strong coupling between the G_1 and G_2 potential wells will promote linearity in the charge injection process. Similarly, strong coupling between G_2 and ϕ_1 is also necessary to ensure that the charge is completely transferred to the transfer region.

The final design parameter to be considered is the doping of the input diodes. For process simplicity, these diodes are usually designed to have the same doping profile as the transfer channel. Higher doping can also be produced by selective ion implantation to improve the dynamic range of the device by allowing the injection of a larger charge packet.

2.2.3.2 Output sensing

The standard output sensing region consists of a Schottky gate (referred to as G_3) adjacent to the last transfer electrode and an ohmic contact through which the charge within the substrate can be extracted.

Two modes of operation are possible using this structure. One operating mode calls for G_3 to be initially held at a low reference potential. Just after the charge packet arrives in the region below the final ϕ_1 electrode, G_3 is pulsed to a voltage higher than ϕ_1 so that the charge packet moves to the output diode. One of the drawbacks of this scheme is that harmonic generation from the pulse applied to G_3 will represent a source

of high frequency noise and degrade the linearity of the output signal. To resolve this problem, another operating mode is possible whereby the pulse on the output gate is replaced with a fixed DC potential. This technique has been found to be equally effective in sensing the charge packet, although quantitative comparisons have not been performed. In either mode of operation, the potential barrier represented by G_3 acts to decouple the clock pulses from the output node. The output ohmic contact is used to tune the capacitance of the output node to achieve optimum charge-to-voltage conversion linearity.

Another output sensing technique allows for a Field Effect Transistor (FET) and output amplifier circuitry to be integrated into the output node in a floating diffusion amplifier (FDA) arrangement [2.21]. In this technique, the FET gate is normally held at a negative potential so that the FET channel is pinched off. Shortly before the arrival of the signal charge, the FET gate is pulsed so that the output node assumes the potential of the FET drain. The FET is then turned off to isolate the output node from the drain before the arrival of the signal charge. As the electronic charge packet arrives, its presence will be sensed as a negative change (proportional to the output capacitance) in the potential of the output node. This potential is then capacitively coupled to the output buffer / amplifier stage for detection and analysis.

The design of the output circuitry completes the design of charge-coupled devices. Geometries of the input injection, charge transfer and charge sensing regions of a typical CCD are illustrated in the micrograph of figure 2.7. The GaAs CCD shown in this figure uses two four-micron-long input gates with 1-micron spacing for charge injection and a four-phase clocking scheme with a mark to space ratio of 3/2 in the

Figure 2.7 : Micrograph of a CCD showing (a) the input injection, (b) transfer and (c) output sensing regions of the device.

transfer region. The geometric design is completed with a four-micron-long output gate and a reset FET with a 1-micron gate length for output sensing.

2.3 CGAS15 CCD MASK DESCRIPTION

To investigate these and other CCD design possibilities, a series of experiments was conceived by other researchers (O. Berolo, G. Millar and D. Davidson) of CRC to investigate some of the parameters relevant to CCD performance. In these experiments, the electrical parameters (CTE, maximum frequency of operation, dynamic range) used to characterize charge-coupled devices can be measured as a function of variations in device geometry, input and output circuitry and various other processing options, including the use of self-aligned gate (SAG) and cermet-gate structures. These experiments have been integrated onto a set of masks by which the devices may be fabricated in-house at CRC. This mask set (hereafter referred to as the CGAS15 mask set) has been fabricated by Precision Photomask Limited (PPM) with a one-micron minimum design rule to allow the definition of 1-micron CCD gate and gap lengths. This section will describe the experiments which have been incorporated onto the CGAS15 mask set.

2.3.1 Variations in CCD geometry

On this mask, all CCDs have been designed with a channel width of 100 microns. Similarly, four-phase clocking has been selected for all devices because of the availability at CRC of a high-speed quadrature clock driver and air bridge fabrication technology. Variations on other aspects of the device geometry include the following:

CCD length: CCDs have been designed with 32, 50, 64 and 128 cells in order to examine the relationship between the number of cells and the electrical parameters such as transfer efficiency and maximum frequency of operation.

Gate length: The gate length is varied from 3 to 6 microns in an effort to increase the dynamic range of the CCD by increasing the volume of semiconductor material beneath the gates. Trade-offs are expected to result, especially in terms of transfer efficiency and the maximum frequency of operation as the dynamic range is increased. This experiment will quantify these trade-offs.

Mark/space ratio (MSR): In this experiment, the mark/space ratio is varied from 1/4 to 2/3, 3/2 and 4/1 to examine the relationship between the CCD electrical parameters and the MSR. The cell size has been kept constant to provide a basis for comparison with other results.

2.3.2 Alternate gate structures

SAG: The Self-Aligned Gate (SAG) process was conceived to reduce the interelectrode gap lengths down to the submicron region (typically 0.3-0.5 microns). The shorter gap sizes will result in shorter transit times between successive gates. The transfer inefficiency is also expected to decrease because the reduced cell size means a lower probability of encountering electron traps within the substrate and the reduced transit time will provide a lower probability of electron recombination. This should translate into a higher operating frequency for a given transfer efficiency or a higher transfer efficiency at any given frequency.

Cermet-gate: A mask is included in the set whereby a cermet film can be defined in the charge transfer region of the CCD either above or beneath the gate electrodes. This cermet film is designed to smooth out abrupt field gradients which would improve the charge transfer efficiency by reducing the potential troughs in the interelectrode gap regions. The use of cermet should allow the fabrication of high performance CCDs with relaxed lithographic requirements.

2.3.3 Input and output circuitry

Input injection: This experiment is designed to examine the effect of altering the doping profile of the input diode (G_1). Changes to the doping of this diode will affect the amount of charge which can be injected into the CCD during a given clock cycle.

Output sensing: CCDs have been designed with a number of options relating to the detection of the signal charge. The basic output cell consists of a single G_s output diode. A reset FET has also been integrated at the end of most of the CCDs to spill the non-signal charge which can accumulate within the channel as a result of feedthrough from the clock pulses. This output sensing technique, as described previously, forms the standard output cell. Variations to this design have been incorporated as follows.

Output buffer/amplifier: As the output signal of a CCD is typically fairly low, amplification of the output signal is generally necessary before any further signal processing can be performed. To examine the benefits of monolithic integration of the CCD with an amplifier stage (i.e. to investigate the use of the FDA architecture described previously) some of the CCDs have been designed such that the CCD output ohmic contacts are connected, via breakable air bridge lines, to both a standard output pad and an output amplifier stage. This stage, consisting of a differential amplifier driving a unity gain buffer, is shown in the schematic of figure 2.8. The effectiveness of either output sensing technique can be assessed by breaking either air bridge line with a DC probe tip.

Reset FET: On some devices, the reset FET has been left out, to examine the insertion loss of this portion of the device.

G_s electrode: Other devices have been designed without a G_s electrode. This was done to allow the development of alternate output sensing techniques.

Figure 2.8 : Schematic of analog output circuitry.

2.3.4 Signal processing experiments

In addition to the experiments which were intended to investigate various processing and geometric design options, several tiles have been included to develop potential system applications of GaAs CCDs. These devices have not been characterized as part of this thesis project. For the sake of completeness and to illustrate the work which may yet be performed using the devices which have been fabricated, these experiments are described briefly as follows.

Crosstalk: Two arrays of three CCD elements each will be used to determine the extent of crosstalk between successive array elements. This experiment will serve as a preliminary investigation in determining the extent of problems peculiar to CCD arrays fabricated on GaAs. The impact of these problems would be assessed with respect to the use of the CCD in signal processing and imaging applications.

Control electrodes: A CCD has been designed in which two independent 'control' gates are integrated into the CCD gate geometry. These gates can be used to inject signal charge at different points along the channel. Data from this experiment can be used as a basis for a study which will examine the integration of signal processing functions with GaAs CCDs.

In addition to the CCDs, the mask contains the following tiles:

- a four-phase clock IC (which could be used to drive the CCD); and
- a process control monitor (PCM) which is used to characterize the substrates and monitor the success of various processes. The process control monitor contains the following elements:
 - 2 transmission line models (TLMs) [2.22] which are used to monitor the ohmic contact and sheet resistances of the CCD channel and the FET active regions.
 - 4 large area diodes which can be used to measure capacitance-voltage (C-V) and diode characteristics. The C-V data are used to extract the doping profile of the CCD channel and FET active layers. One of these diodes is also used to extract the characteristics of the cermet / GaAs junction.
 - 9 Van der Pauw (VdP) [2.23] structures which are used to determine the sheet resistances of all applicable combinations of the ion implants for the CCD channel, FET channel and n+ cap layers as well as that of the cermet film and the semi-insulating substrate.
 - Patterns used to measure the sheet resistances of the ohmic contact and Schottky gate metals as well as the metals used to define the first and second level interconnections.

- Patterns used to examine the resistance and integrity of the contact between the first and second level metal layers.
- An alignment key which is used to ensure correct alignment is maintained between successive process steps on each wafer.

A photomicrograph of the complete CGAS15 reticle is shown in figure 2.9.

This completes the description of the operation and design of the GaAs charge-coupled devices. The completion of the design and procurement of a set of masks which was designed to quantify the influence of some of the design options makes it possible to fabricate GaAs CCDs at the Microelectronics Facility of CRC. The fabrication process whereby a number of CCDs have been produced for evaluation forms the basis for the next chapter.

Figure 2.9 : Fabricated reticle produced from the CGAS15 mask design.

CHAPTER 3

CCD FABRICATION AND PROCESS DEVELOPMENT

The previous chapter described the design of the charge-coupled device and concluded with a description of a mask set which was conceived to test some of the design concepts. This chapter will describe the use of this mask set to fabricate high performance CCDs.

3.1 STANDARD PROCESS STEPS

The description of the CCD fabrication process which forms the basis for this chapter refers to a number of standard processes which are commonly used in semiconductor fabrication. In order to avoid repetition, these processes (photoresist definition, liftoff and etch steps) are described in the following paragraphs and will be referred to throughout this chapter.

3.1.1 Photoresist definition

Photolithography is the process whereby a pattern defined on a mask is transferred to a polymer on the surface of the substrate. This polymer then acts to mask the

substrate during subsequent process steps such as etching, metal deposition or implantation. Polymers which are generally used exhibit properties such that their resistance to certain chemicals can be modified by exposure to a given wavelength (usually ultra-violet) light. Thus, the generic name used for this class of polymers is photoresist (PR). The standard process used to transfer a mask image is illustrated in figure 3.1 and described as follows.

In the first step, several drops of a photoresist (PR) are deposited in the centre of the sample. The sample is spun (typically 4000 to 5000 rpm) so that centrifugal force distributes a uniform coat of PR approximately 1.0 to 1.5 μm thick on the substrate. The PR is then baked to stabilize the resist. Next, a mask is obtained which is transparent in areas corresponding to the pattern to be transferred and is otherwise completely opaque. The PR is exposed to ultraviolet radiation (typically, $\lambda = 300\text{-}450\text{ nm.}$) through this mask and then baked again. Ultraviolet light sensitizes the PR to a developer solution so that, in the next step, the PR in the exposed areas can be removed. Note that the inverse of the mask pattern is now defined in photoresist on the surface of the wafer. The substrate is then cleaned to prepare the surface for the next processing step.

Note that the process which was described used a dark field mask (so named because when viewed on the mask, the desired pattern appears clear (transparent) surrounded by a dark field (background)) and a positive polarity PR. The inverse of this pattern can also be defined either by using a light field mask (in which the desired pattern appears dark on a clear background) or by using a negative polarity photoresist. Negative resists are also sensitive to UV light; the light tends to harden the PR so that the unexposed regions develop easier than the exposed regions. All four combinations of mask contrasts and PR polarities are commonly used in semiconductor processing.

PHOTORESIST LIFTOFF PROCESS

STEP 1 : Spin photoresist (PR) uniformly over the substrate.

STEP 2 : Expose the PR to UV light through a dark field mask.

STEP 3 : Develop the PR to remove the exposed resist.

STEP 4 : Evaporate the desired metallization.

STEP 5 : Dissolve the remaining PR to lift off the excess metal.

Figure 3.1 : Illustration of the photoresist definition and liftoff processes.

A list of the masks used for the fabrication of CCDs is provided in the Appendix.

3.1.2 Liftoff

Liftoff is the name given to the most common process used to define metal lines on semiconductor substrates. A description of the liftoff process continues from where the PR definition is completed.

For the liftoff process, the bake, exposure and development parameters of the photoresist definition stage are optimized to produce a PR profile in the exposed regions with negatively sloping sidewalls similar to those shown in step 3 of the liftoff process illustration (figure 3.1). Metal is then evaporated uniformly over the substrate to cover both the PR and the exposed surface regions of the sample. Note that if the metal thickness is less than approximately half of the total PR thickness, there will be a discontinuity in the metal coverage over the wafer, as shown in the illustration. Next, the wafer is immersed in a solution (typically hot acetone) which dissolves photoresist. The discontinuity will allow the acetone to seep under the metal to attack the PR. The PR then dissolves and the excess metal 'lifts off' and is washed away in the acetone to leave evaporated metal on the substrate in the mask pattern. This liftoff process is generally assisted by ultrasonic agitation which improves the penetration of the solvent beneath the metal film. Finally, the wafer is cleaned to remove any residual PR or solvents.

3.1.3 Etch processes

For etch processes (such as the mesa etch used for the isolation of the transport channel), a light-field mask is generally used with a positive polarity photoresist. After development, this combination will leave the majority of the substrate exposed to the etchant while the desired features are protected with PR. The etch can then be performed without damaging sensitive areas of the substrate. After the etch, the resist is stripped in solvents such as either acetone or a commercially available solvent such as J-100 photoresist stripper.

This completes the description of some of the standard processes. The application of these processes for the fabrication of GaAs CCDs follows.

3.2 CCD FABRICATION PROCESS

The process described in this chapter is used to fabricate cermet-gate charge-coupled devices. This baseline process (illustrated in figure 3.2) includes 9 photolithographic steps, two levels of interconnect metal and requires two dielectric layers. The only process modifications required to fabricate standard capacitive-gate CCDs is to omit the dielectric-aided liftoff of the cermet film and subsequent dielectric etch steps. Additional process development was also performed to develop a self-aligned gate (SAG) process. While this process showed considerable promise, time constraints prevented the fabrication of self-aligned gate CCDs.

STEP 1 : Mesa etch to buffer layer.

STEP 2 : Implant dopants for FET channels and contact regions.

STEP 3 : Deposit Cr:SiO (cermet) layer.

STEP 4 : Define, liftoff and alloy ohmic contacts.

STEP 5 : Define, liftoff and sinter clock electrodes and FET gates.

STEP 6 : Deposit dielectric to glassivate the surface.

STEP 7 : Define and liftoff first level metal for interconnections

STEP 8 (not shown) : Define air bridge posts and plate air bridges.

Figure 3.2 : Illustration of the cermet-gate baseline fabrication process.

In addition to the actual CCD fabrication process, the remainder of this chapter describes the processing options which were considered and the process development which was required to successfully produce working charge-coupled devices.

3.2.1 Substrate Preparation

The first process step to be performed for any GaAs substrate is a 'standard clean'. This cleaning procedure is designed to remove any grease, fingerprints, dust, etc. which may have accumulated on the wafer during travel or storage.

The 'standard clean' process consists of :

- 5 min rinse in hot trichloroethane;
- 5 minute rinse in hot acetone;
- 5 min rinse in hot iso-propyl alcohol (IPA);
- 5 min rinse in de-ionized (DI) water; and
- blow dry with compressed N_2 gas.

3.2.2 Dopant incorporation

Once the wafer has been properly cleaned, the steps which will define the doped regions of the CCD are performed. This section will review the doping requirements of charge-coupled devices and will then detail the development of the processes

required to define these regions and their isolation to form the charge transfer and FET channels.

There are three layers of distinctly doped regions required to complete the fabrication of CCDs using the CGAS15 mask set. The first layer forms the channel for the CCD charge transport. Two options have been exercised with respect to the doping of this layer. The first layer specification is established to provide a basis for comparison with CCDs which had been previously fabricated at CRC; these included a charge transport channel which was doped to a level of 2×10^{16} atoms/cm³, 1.0 μ m thick. The second transport channel specification is 2×10^{17} atoms/cm³, 0.3 μ m thick; this is designed to be compatible with the process used to fabricate MESFETs at the Microelectronics Facility of CRC.

The second layer required for the fabrication of CCDs forms the channel regions of the MESFETs used in the output circuitry. This layer was designed to match the FET channel doping profile of commercially available MESFETs fabricated by TriQuint Semiconductor Inc., shown in figure 3.3.

Finally, a thin, highly doped n⁺ layer is required to aid in the formation of ohmic contacts. This third layer is doped 2×10^{18} atoms/cm³, 0.15 μ m thick.

3.2.2.1 Mesa isolation

To satisfy these layer requirements, two sets of GaAs semi-insulating substrates were obtained from Epitronics Corporation with the layer structures grown by MOCVD shown in table 3.1. The remainder of the dopant layer requirements will be filled by

Figure 3.3 : Doping profile of TriQuint M81T MESFET

ion implantation, as discussed in the next section.

Note that the layer structure of the standard CCD wafer contains an n^+ layer while the FET-compatible wafers do not. Since a requirement already exists to perform an n^+ implant on these wafers, this layer is superfluous on the standard CCD wafers and is removed in the first processing step.

Next, photoresist is patterned using the MESA light field mask to cover the areas which will form the CCD charge transfer region. The remainder of the surface is then

Table 3.1 : Typical layer structures of the original substrates used for CCD fabrication.

Device type	layer	Carrier concentration (cm ⁻³)	Depth (μm)
"Standard" CCD :	3	2×10^{18}	0.15
	2	2×10^{16}	1.00
	1	$< 1 \times 10^{14}$	2 - 3
"FET-Compatible" CCD :	2	2×10^{17}	0.25
	1	$< 5 \times 10^{14}$	2 - 3

etched through to the buffer layer using (HF : H₂O₂ : H₂O) ≡ (1:3:8) to leave mesas through which the charge transport will take place. Note that the semi-insulating substrate provides electrical isolation between devices. In addition to the CCD channel, the MESA mask delineates the patterns to be used for the alignment of subsequent implants and ohmic contacts.

Formation of the CCD channel is now complete and electrical isolation has been provided to minimize sidegating or inter-device crosstalk.

3.2.2.2 Ion implantation

The remaining required layers, as described previously, are formed by ion implantation. The choice of dopant ion as well as the implant and activation conditions are described as follows.

The first step involved in ion implantation is to choose the dopant ion. Silicon was chosen as the dopant atom due to its light weight (which will cause less damage to the lattice during the implant process), its low diffusivity (which will prevent the ion from moving appreciably from its predicted range during the anneal) and its ease of implantation and activation. The Si^{30} isotope was selected because of the ease with which the mass spectrometer can isolate this isotope from the remainder of the isotopes in the source gas.

To choose the implant energy and fluence, a commercial software package was obtained (PROFILE Code [3.1]) which calculates the electronic and nuclear stopping powers of a wide range of targets upon selected ions. The software fits the predicted ion range, straggle and other parameters to a Pearson IV distribution function to calculate the atomic density as a function of depth for a variety of implant conditions. The implant conditions were optimised to obtain doping profiles as similar as possible to the desired profiles shown in figure 3.4.

In an attempt to limit the damage which may occur near the surface of the wafer as a result of the implant, the implantation was performed through a 400Å thick layer of silicon nitride (Si_3N_4), deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) in a Plasmatherm 700 Series reactor. This layer was itself masked by a thick

coat of photoresist in which windows were lithographically defined in the regions to be implanted (masks EDIM and NPIM for the FET channel and n' implant regions, respectively). The nitride cap serves two purposes. First, the nuclear stopping power of the nitride film will reduce the range of the implanted ions to bring the peak of the implant profile nearer to the semiconductor surface. The more uniform ion distribution which results (shown in figure 3.4) is more amenable to analytic simulation. Secondly, the use of the nitride cap provides a means to remove the PR which has been implanted by secondary ion knock-on into the exposed surface of the cap layer. Since the nitride cap can easily be removed in buffered hydrofluoric acid (BHF), the PR is simply washed away when the nitride is dissolved.

The Si^{30} ions were implanted (at a 10 degree offset angle to prevent channeling) at the Bell-Northern Research (BNR) laboratories in Ottawa, Ontario. The simulated implant profiles, along with the target profiles and the multiple implant parameters, are shown in figure 3.4.

3.2.2.3 Implant activation

Once the dopant ions have been implanted into the substrate, the implant is activated using a high temperature anneal process which allows the implanted ions to move onto lattice sites. This reorganization will also cure the damage caused by the energetic bombardment of the lattice by the implanted ions during the implant. Incomplete annealing will leave lattice damage which will increase electron scattering and reduce the effective electron mobility with a corresponding increase in the resistivity of the substrate. Thus, the success of the implant process depends, to a large degree, upon the extent of the activation of the implants. Since this is a critical process

IMPLANT PROFILES FOR CGAS15 CCDs

Si-30 implanted into GaAs through 400Å Si₃N₄ cap

Figure 3.4 : Implant profiles for CGAS15 CCDs.

in the fabrication of charge-coupled devices, a determined effort was made to establish the optimum conditions and parameters necessary for the successful activation of these ion implants. The next few paragraphs will describe the development of this process and will present its results.

A review of available literature indicated that one of the most effective techniques used to activate implants is by rapid thermal annealing [3.2], [3.3]. The basic rapid thermal anneal (RTA) process is quite simple; the wafer to be processed is first placed inside the quartz chamber of the RTA oven. Tungsten-halogen lamps placed

immediately above and below the chamber heat the chamber very quickly (typically 30 degrees/second) to the desired temperature, maintain this temperature for a user-specified period of time and then allow the wafer to cool back to room temperature. The lamp intensity is computer controlled to ensure reproducible results. Gas (8% H₂ in Ar) flowing across the surface of the wafer throughout the anneal cycle provides temperature uniformity across the wafer and allows for some control (by changing the pressure and flow rate of the gas) over the heating and cooling rates of the wafer.

There are, however, a number of complicating factors. GaAs substrates are generally annealed at temperatures in the vicinity of 900°C. In excess of approximately 600°C, the GaAs lattice begins to dissociate [3.4]. Since arsenic evolves from the GaAs substrate considerably faster than does gallium [3.5], the stoichiometry of the substrate surface is altered. As arsenic evolves from the surface, the surface will become Ga-rich to leave the surface p-type to ruin the effect of the implantation.

While several approaches exist to circumvent this problem, the technique of choice to prevent the evolution of arsenic from the substrate is to perform the anneal under an overpressure of arsine gas. This overpressure is established by enclosing the wafer inside a susceptor made out of a porous material (such as graphite) in which arsenic is highly soluble. This susceptor is saturated with arsenic immediately prior to the anneal by processing a 'sacrificial' undoped GaAs wafer in the same time/temperature regimen as the implanted wafer. When the wafer is heated, arsenic evolves from this substrate and will impregnate the susceptor. Thus, after this pre-anneal cycle, the susceptor should contain as much arsenic as will evolve under the anneal conditions. Then, when the implanted wafer is placed in the oven and annealed, the arsenic should

evolve from both the susceptor and the wafer at similar rates. Thus, an arsine overpressure is established to prevent further dissociation of the implanted wafer.

For this process, several susceptors were designed and fabricated from high purity (semiconductor grade) graphite and were conditioned at high temperature to stabilize the surfaces which would be in proximity to the wafers. The heating and cooling rates of the RTA chamber were then fixed at the maximum recommended rates and the RTA system software was modified to obtain flat temperature profiles at a number of steady state temperatures within the range of interest.

A series of experiments was then conducted to determine the optimum anneal time and temperature. For these trials, a number of semi-insulating wafers were also implanted at BNR with the specifications listed in table 3.2. Following the sheet implant, the dielectric cap was removed and the wafers were quartered. Implant anneals were performed over the temperature range 800 to 940 degrees Celsius and for times between 6 and 30 seconds using the anneal procedure described previously. Next, Au-Ge-Ni ohmic contacts and Ti-Au Schottky contacts were patterned on the substrates using the standard liftoff process. The Hall mobility and doping profile (established from differential capacitance-voltage measurement data) of each quarter were evaluated to characterize the substrates and to gain some indication of the activation efficiency. These results are presented below.

The activation efficiency is defined to be the ratio of the number of ions which become electrically active after annealing to the number of ions which were implanted into the substrate. There are several ways to experimentally characterize this measure. One technique is to measure the Hall mobility of the substrate from a Van der Pauw

Table 3.2 : Implant parameters for implant anneal experiments

ion :	Si ³⁰
fluence :	$5 \times 10^{12} \text{ cm}^{-2}$
energy :	150 KeV
tilt angle :	10 deg from perpendicular
substrate :	SI GaAs covered by 400Å Si ₃ N ₄

test structure, as described in [3.7]. The sheet carrier concentration can be determined as

$$N_s = \frac{1}{q R_s} \quad (3.1)$$

where N_s is the sheet carrier concentration, R_s is the Hall coefficient and q = electronic charge = 1.609×10^{-19} Coulomb.

The activation efficiency for the sample can then be given as [3.2]:

$$\eta = \frac{N_s}{N_s'} \quad (3.2)$$

where N_s' is the fluence used for the implant.

A second method which can be used to gain some indication of the activation efficiency is to compare the doping profile evaluated from differential C-V measurements (as measured using a suitable test structure such as a FATFET) to the expected doping profile of the implant. Since the PROFILE software described earlier

has been shown [3.8] to agree very closely to SIMS measurements of implanted ion distributions over a wide range of implant conditions, the PROFILE data are taken to represent the expected implant profile. Integration of the two profiles as a function of substrate depth should give a relative measure of the number of ions which are electrically active as compared to the number which are expected to be within the substrate. The ratio of these numbers should yield a measure of the activation efficiency.

The activation efficiency, measured using the first technique described above, is plotted as a function of anneal temperature for a 6-second anneal and as a function of time for 850 and 880°C anneals in figures 3.5 and 3.6. Results of carrier profiles extracted from C-V data for some of the test samples are shown in figure 3.7. The doping profile predicted using the PROFILE software is also plotted for comparison on this graph. These data indicate that the optimum anneal temperature is 850°C while the optimum time at 850°C is 15 seconds.

As a result of this process development, subsequent ion implants were activated at a temperature of 850°C for 15 seconds using the RTA process.

3.2.3 Cermet deposition

Once the active regions have been completely defined, the first processing step to be performed is the deposition of the cermet film. Cermet is deposited at this point for two reasons. Since, as has been discussed previously, improved CCD performance is obtained when the gates are fabricated on top of the cermet film, the cermet must be

Figure 3.5 : Implant activation as a function of anneal temperature.

defined before the gate metal is evaporated. Secondly, it has been shown that the cermet must be annealed in order to improve both the diode characteristics of the cermet-GaAs junction and the sheet resistance of the cermet film. Since the ohmic contact anneal regimen has been shown to be adequate to anneal the cermet, the wafer can be spared an additional thermal treatment by annealing both the ohmic contacts and the cermet at the same time. Thus, the cermet is deposited immediately prior to the formation of the ohmic contacts. This section will describe the cermet film deposition process.

Figure 3.6 : Implant activation as a function of anneal time.

The cermet film is deposited on the substrate using a magnetron-enhanced sputtering process developed by M. LeNoble et al. of the Tri-University Meson Facility (TRIUMF) in Vancouver, B.C. The use of the magnetron eliminated much of the heating which is usually associated with electron bombardment of the target during sputter deposition. Since photoresist generally would not survive the intense bombardment and the heat which is developed as a byproduct of the standard sputter process, the use of magnetron-enhanced sputtering permits the use of a photoresist liftoff process to define patterns in sputtered films.

Figure 3.7 : Activated dopant profiles : RTA ion implant anneal tests.

A dielectric-aided liftoff process was chosen for the cermet definition. For this process, 4000Å of silicon nitride (Si_3N_4) was deposited by PECVD on the substrate. Next, the light field CGAS15 CMET ETCH mask was patterned using image reversal (i.e. negative polarity) photoresist. The dielectric was selectively etched in a CF_4 plasma through the photoresist mask using a Technics model 750 Planar Etch II plasma generating system. Since this is an isotropic etch process, the nitride will be undercut to leave a photoresist overhang, as shown in figure 3.8. Thus the appropriate profile for proper liftoff is obtained. The wafers were then brought to TRIUMF where they were first rinsed in 10% HCl to remove any native oxides which may have formed on

DIELECTRIC-AIDED LIFTOFF PROCESS

STEP 1 : Deposit silicon nitride uniformly over the substrate.

STEP 2 : Define PR in desired pattern.

STEP 3 : Plasma etch the nitride to undercut the PR.

STEP 4 : Evaporate the desired metallization.

STEP 5 : Dissolve the remaining PR to lift off the excess metal.

STEP 6 : Remove the remaining nitride using buffered HF.

Figure 3.8 : Illustration of the dielectric-aided liftoff process.

the surface of the wafer in transit. 2000Å of cermet (45% Cr, 55% SiO) and 300Å of Ti-W (80% Ti) were then sputtered on the substrate and the residue lifted off using solutions containing hot acetone, trichloroethane and iso-propyl alcohol. The wafers were cleaned, profiled (to measure the thickness of the sputtered films) and then brought back to CRC for further processing.

3.2.4 Ohmic contact development

The next process step involves the formation of the ohmic contacts necessary for the injection and sensing of the signal charge, as well as for the source and drain contacts for the FET output circuitry.

At this point in the process, the substrate is covered with silicon nitride in all areas in which the cermet film was not sputtered. This film has to be removed prior to the evaporation of the ohmic metallization. Thus, the first step of the ohmic contact fabrication process is to etch the silicon nitride in a CF_4 plasma using the Technics Planar-Etch II plasma generator for 10 minutes. While this process was successful in removing the nitride film, it was also found to remove the Ti-W film which had been sputtered on top of the cermet. Investigations into different etch procedures (both wet and dry processes) were conducted in an effort to find an etchant or etch process which would remove the nitride without affecting the Ti-W. Unfortunately, these investigations proved fruitless.

3.2.4.1 Substrate preparation

In preparation for the ohmic metal deposition, care must be taken to ensure that the surface is free of any surface contamination (excess photoresist, residues of previous process byproducts such as gallium oxide, etc.). Such contaminants will degrade the contact resistance and may even prevent the formation of ohmic contacts. Hence, the first step in the ohmic contact fabrication is to prepare the surface of the wafer for the subsequent ohmic metal evaporation.

A number of cleaning procedures were investigated, as outlined below. Their effectiveness is assessed by evaluating the success of ohmic contacts which were fabricated on the different samples after the completion of the prescribed cleaning procedure.

To this effect, a GaAs wafer was cleaned and then covered with 4000Å Si_3N_4 in an attempt to reproduce the process to be used for the CCDs. This film was then patterned and etched to expose the substrate in the ohmic contact pattern. The wafer was diced into 4 quarters and the quarters subjected to the following treatment:

SAMPLE	TREATMENT
(A)	5 second rinse in buffered HF
(B)	oxygen plasma ash (descum) followed by 20 sec rinse in HCl
(C)	oxygen plasma ash (descum) and 20 second rinse in 10% NH_4OH
(D)	No clean. (This wafer was used as a control to verify the requirement of cleaning the substrate prior to metallization.)

Figure 3.9 : I-V curves of 2 closely spaced ohmic contacts fabricated after the substrate cleaning procedures listed in Table 4.2.

The quality of ohmic contacts formed on these samples was characterized, subjectively, in terms of the linearity of the I-V curve measured between closely spaced ohmic contacts and the adhesion of the ohmic metal to the substrate. The effect of these cleaning procedures can be seen in figure 3.9 where the I-V curves have been reproduced. The final results have been tabulated in table 3.3.

Table 3.3 : Ohmic contact characterization after surface preparation.

Sample	Cleaning Procedure	Linearity	Adhesion
A	buffered HF	G	F
B	descum, HCl	G	G
C	descum, NH_4OH	E	E
D	none	P	G

LEGEND: E: Excellent, G: Good, F: Fair, P: Poor

Based upon these results, subsequent wafers were subjected to a descum and then a 20 second etch in ammonium hydroxide (NH_4OH) before the evaporation of the metals which will form the ohmic contacts.

3.2.4.2 Metallization

The formation of an ohmic contact requires a local substrate doping on the order of $2 \times 10^{19} \text{ cm}^{-3}$. To accomplish this, a mixture of several metals is usually used for the

formation of the ohmic contact. One of these metals is chosen to act as a strong dopant in GaAs (typically Si, Se, Ge, Sn, or Te for n-type contacts) while the other acts as an encapsulant to make contact to successive metallizations or bond wires.

Researchers have investigated many different combinations of metals for potential use in the formation of ohmic contacts [3.9]. The Au-Ge mixture is chosen because, when alloyed, gallium will diffuse out of the substrate into the gold while the germanium, a good n-type dopant in GaAs, diffuses onto the gallium sites of the substrate to provide the required substrate doping for a good ohmic contact. Nickel is added to the ohmic metallization because it enhances the diffusion of Ge into GaAs and also acts to preserve the surface morphology of the resultant mixture by preventing the Au-Ge alloy from balling up [3.10].

This Au-Ge (12% Ge by weight) eutectic system has emerged among a majority of researchers as the metallization of choice because it has consistently produced superior ohmic contacts. For these reasons, 360Å Ge, 2000Å Au and 200Å Ni were evaporated immediately following the descum/ NH_4OH rinse.

3.2.4.3 Alloy

The final step in the formation of ohmic contacts involves alloying the ohmic metallization, as mentioned previously. Traditionally, Au-Ge-Ni ohmic contacts are alloyed in a furnace for 5 minutes at 450 degrees Celsius. However, a review of the available literature has indicated that superior ohmic contacts may be obtained by rapid

thermal processing of the ohmic contact metallization in place of the conventional furnace alloy [3.11].

Thus, in order to maximize the quality of the ohmic contacts, investigations were begun in the use of the Rapid Thermal Anneal (RTA) system to alloy ohmic contacts. In an effort to optimize this process, a matrix of experiments was performed in which ohmic contact metallization was defined in transmission line model (TLM) [3.12] patterns on a number of n^+ GaAs substrates. These substrates were then alloyed in the RTA over a wide range of temperatures. The contact resistance (in ohms for a 60 μm wide contact) was measured and then plotted as a function of alloy temperature for a 10 second alloy cycle. These results have been reproduced as figure 3.10. The graph indicates that a threshold exists below which the contact has not been completely alloyed. When the metal is alloyed at temperatures above this threshold (i.e. somewhat over-alloyed), the contact resistance increases gradually until a point is reached at approximately 450 degrees Celsius at which the metal starts to bubble and the resulting poor adhesion prevents measurements from being taken. This effect is ascribed to arsenic evolution from the GaAs substrate [3.13]. Further investigation showed that increasing the alloy time causes the metal to be over-alloyed in the same way as a slight increase in alloy temperature (i.e. contact resistance increases slightly while the metal adhesion becomes poorer with alloy times greater than 30 seconds).

Based upon these results, ohmic contacts were subsequently alloyed in the RTA oven for 10 seconds at 405 degrees Celsius.

Figure 3.10 : Results of ohmic contact development.

3.2.5 Gate / clock electrode formation

Once the ohmic contacts have been formed, the gates forming the CCD clock electrodes and FET output circuitry are fabricated. (Note that for purposes of process development only, the terms 'gate' and 'clock electrode' are used interchangeably.) As mentioned earlier, two processes were investigated to define the CCD gates. For the baseline process, the standard Schottky gate metallization consisting of 300Å titanium, 1000Å platinum and 4000Å gold was patterned using the liftoff process described

previously. The gates are then sintered at 350° Celsius for 3 minutes to complete the standard process.

Process development was also performed to develop a self-aligned gate (SAG) process. This process, along with some of the process results, is described in the following section. For reference, the process is illustrated in figure 3.11.

3.2.5.1 Self-Aligned Gate (SAG) process

In the first step of the SAG process, a sheet of gate metal is evaporated uniformly across the surface of the gate region. Next, PR is defined to mask the areas in which every second clock electrode will be formed. A wet chemical etch is then used to etch the exposed gate metallization. Since this etchant will attack the exposed sidewalls of the etched metal, the etch proceeds laterally as well as vertically to underetch the PR. A second evaporation of gate metal follows to form the alternate gates. In the final step, the PR and excess gate metal is lifted off to leave the gate pattern shown in the SEM micrographs of figures 3.12(a) and (b). Note that the submicron (approximately 0.5 μ m) inter-electrode gaps are formed solely as a result of the undercut of the PR by the etchant; fine lithography is not required.

While this process showed considerable promise, it was dropped in favor of the standard process for three reasons. Since the two gate processes are incompatible, the use of the SAG process precludes the fabrication of the devices with the standard gate structure. Since only 4 of 27 possible CCDs per reticle have been designed with the SAG structure, the yield (in terms of both the number of usable devices and the amount of information which could be garnered from them) would be relatively quite low.

Illustration of the Self-Aligned Gate Process

STEP 1 : Evaporate gate metal on GaAs substrate.

STEP 2 : Define PR for self-aligned gate etch.

STEP 3 : Etch gate metal.

STEP 4 : Evaporate second gate metallization.

Step 5 : Liftoff PR and excess gate metal.

Figure 3.11 : Illustration of the Self-Aligned Gate (SAG) Process.

Secondly, as illustrated in figures 3.11 and 3.12, the physical geometries of adjacent clock electrodes fabricated using the SAG process are different. This feature of the process adds an extra element of uncertainty in attempting to define the CCD performance in terms of the cell geometry. Finally, since time did not allow the fabrication of CCDs using both gate processes, the standard process was chosen.

The remainder of this section will focus on the process modifications required to enhance the standard gate process.

3.2.5.2 Standard gate process

The first lot of devices from the CGAS15 mask set produced a total yield of only a few devices. DC probing showed that some of the clock electrodes on many of the devices were shorted. There were two factors contributing to this phenomenon.

The most readily apparent problem was that the chips had not been protected with photoresist during scribing and dicing operations so that the pressure exerted directly on chip caused some of the air bridges to collapse. The collapsed bridges then caused shorts between successive first level metal lines. This mistake was corrected in later runs.

A more serious problem was that many of the gates were shorted together by an effect known as 'wings' on the edges of the gates. Wings are caused by a build-up of gate metal on the sides of the photoresist walls during evaporation. When the PR is removed during the gate metal liftoff, this build-up is left behind, attached to the edge

Figure 3.12 : SEM micrographs illustrating the results of the SAC process.

Figure 3.13 : Gate metal liftoff (a) using the original PR profile which leaves wings; and (b) using the PR process which was developed to eliminate wings.

of the gate as illustrated in figure 3.13(a) and the SEM micrographs of figure 3.14. During subsequent handling, these wings often collapse across the interelectrode region to cause a short between adjacent gates. Two process modifications were developed to eliminate this problem, as discussed below.

3.2.5.2.1 Photoresist profile modification

The first process enhancement was to modify the PR profile to reduce the possibility of having metal build up along the sides of the PR. An overhang can be created, as shown in figure 3.13(b) to move the PR walls out of the path of the evaporated metal while preserving the desired linewidth. This is accomplished by hardening the surface of the PR using a chlorobenzene soak process so that the bottom of the PR develops more rapidly than the surface.

Figure 3.14 : SEM micrographs of 2 micron gates with wings.

OF / DE

PM-1 3 1/2"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

This process was developed by careful examination of many of the parameters used to control the gate PR formation. The use and method of application of HMDS (a PR adhesion promoter) was investigated; photoresist thickness, exposure time, chlorobenzene soak time, bake parameters and the developer type, dilution and development time were all optimized to yield the gate PR profile shown in figure 3.15(a). Figure 3.15(b) shows the resultant 1 micron gate after gate metal evaporation and liftoff. Note the absence of 'wings'.

The profile shown in figure 3.15 was achieved during development testing using a 1 micron gate FET mask. Unfortunately, the use of this process met with variable results when it was tried with the CGAS15 gate mask. The problem arises because the CGAS15 mask set includes a wide range of CCD device geometries, from mark-to-space ratios (the ratio of gate length to gap length) of 4/1, 1/1 and 1/4 microns. Proper PR development to accomodate both four and one micron gate lengths with a one micron gap is both challenging and critical.

The objective of the chlorobenzene process was to make the surface less soluble to the developer than the underlying PR. Unfortunately, the lower soluble area of the surface is thick enough that the development time of the overhang is significantly longer than that of the remaining PR. Since large areas develop quicker than small areas, the surface of the large (4-5 micron wide) gates will develop out before the surface of the 1 micron gates. It has been seen that the remainder of the wider gates will then develop out before the surface of the thinner gates has been broken. Thus, to ensure that the thin gates are completely developed, it is necessary to significantly overdevelop the wider gates. However, as these gates overdevelop, the undercut which

Figure 3.15 : (a) Resultant PR profile after chlorobenzene process modification; and (b) 1 μm gate which results from the metallization and liftoff of the PR profile shown in (a).

forms the overhang becomes more pronounced until, in the extreme, the gap between gates is completely eroded, as illustrated in figure 3.16. Note that a single 128 pixel device has 515 gates; the loss of a single interelectrode gap would short two of the clock electrodes to cause a catastrophic device failure.

In order to make the development times more equal, it is necessary to reduce the amount of time taken to develop the surface layer with respect to the total development time. This will tend to minimize the effect of the difference in the amount of time taken before development has progressed an appreciable amount between the various devices. This can be done by either reducing the depth of the overhang or increasing the total PR thickness so that the development time of the overhang is a less significant fraction of the total development time. To this effect, the spin speed of the PR was reduced to increase the film thickness and the chlorobenzene soak time was reduced to provide a thinner overhang. The final metallized gate PR profile for a 1 micron gate is shown in figure 3.17. Note that because of the significant overhang, this profile should not result in wings.

3.2.5.2.2 Gate metal etch

The second process modification devised to eliminate the gate wings was to perform a slight etch of the gate metal before liftoff, in an attempt to etch away the thin (typically 300Å) metal coat which had built up along the PR wall. This is done before liftoff so that the rest of the substrate is protected by the PR from the effects of the etchant. To this effect, experiments involving two different gold etchants were performed to determine if an etch could remove approximately 300Å of gold in a time frame sufficient to allow good control of the etch depth. A cyanide-based commercial

Figure 3.16 : Illustration of the difference in PR development for long and short gate lengths on the same mask.

Figure 3.17 : Final metallized profile of 1 μm gates.

gold etchant (Technistrip) was tried first. Using the recommended etch procedure, the etch rate was found to be too high to yield reliable etches of only a few hundred Angstroms. Efforts were then spent to determine the effects of cooling the etchant or diluting it to reduce the etch rate. These efforts did not produce satisfactory results as the etch became unreliable. An iodine-based etchant was then tried. Investigations showed that this etchant removed approximately $300\text{\AA}$ within the first 10 seconds and then did not etch significantly for the next minute. This was considered ideal in that it allowed a considerable amount of process latitude. Since etch times greater than 10 seconds appear to degrade the surface of the gold, an etch time of 10 seconds was chosen.

In the course of performing these etch tests, the gold on some of the samples was completely etched away. When the remaining metal was lifted off, wings were still evident. Thus, it became apparent that an etch of each of the components of the gate metallization was necessary to ensure the wings were eliminated. Thus, investigations were begun into platinum and titanium etches. First, a commercial solution (TFT) used to etch titanium was found. This HF-based solution was found to etch the 300Å thick titanium interlayer used for the gate metallization in 4-5 seconds without apparent deleterious effects to the other metallizations. Next, a solution used to etch platinum (25% HNO₃, 75% HCl) was found. Preliminary testing showed that this solution etched GaAs considerably faster than it did platinum and was thus deemed unsuitable. Since the use of platinum as part of the gate metallization was intended only to enhance the long term stability of the devices and does not otherwise contribute to the device performance (at least in the short term in which the device performance will be evaluated), it was decided that the use of platinum posed a source of more potential harm than good and was discontinued. Thus, a 10 second etch in a 5% KI:I₂ gold etchant solution followed by a 5 second etch in TFT (Ti etchant) were incorporated into the gate process immediately prior to performing the liftoff.

As a result of these process modifications, gate wings were virtually eliminated; subsequent device yield improved significantly. A micrograph of a 32-bit capacitive-gate CCD with 1 µm gate and gap lengths realized using this process is shown in figure 3.18.

Figure 3.18 : Micrograph of a 32-bit GaAs capacitive-gate CCD with 1 μm gate and gap lengths.

3.2.6 Dielectric and first level metal (FLME) deposition

Once the gates have been fabricated, a blanket deposition of Si_3N_4 is performed. This dielectric cap (2000Å Si_3N_4) is deposited by PECVD as a means of protecting the gates from the vigorous process steps to follow and as a glassivation for the exposed active regions of the output circuitry.

With the dielectric cap in place, processing of the first level metal (FLME) can commence. First level metal is used to define the output bonding pads and to provide the interconnections between device elements which do not require a crossover. In this process, PR is first defined using the standard liftoff technique. Next, silicon nitride (which is now exposed in the FLME pattern) is etched in a CF_4 plasma to ensure that the first level metal makes contact with the underlying Schottky gate or ohmic contact metal. The surface is etched lightly in 10% NH_4OH for 30 seconds to remove any residual surface oxide. Next, 300Å of titanium and then 4000Å of gold are evaporated onto the substrate and lifted off using the standard liftoff process. In the final step, the wafer is cleaned in preparation for the air bridge formation.

3.2.7 Air bridge formation

The final processing step of the CGAS15 CCD process involves the deposition of the second level of metallization. Second level metal is fabricated in the form of an air bridge; so called because the metal line is suspended over air supported by two air bridge posts in the fashion of a bridge, as shown in figure 3.19. This metal layer is used to connect any two points where it would be necessary to cross over a metal line

Figure 3.19 : Typical air bridge supported by two posts.

created using one of the earlier metal layers. Additionally, since the adhesion of bond wires which were bonded to the thick plated gold of the ABME metallization (which is typically several microns thick) has been found to be superior to those bonded to first level metal alone, air bridge metal is also plated over the output bonding pads.

The formation of air bridges requires 2 masks (air bridge vias (ABVI) and air bridge metal (ABME)) and several distinct processing steps, as described below and illustrated in figure 3.20.

First, PR is patterned using the ABVI dark field mask to define the positions of what will become the air bridge posts. 300Å Ti and 2000Å Au are then evaporated to form the seed layer for the subsequent air bridge plating operation. Note that this metallization is NOT lifted off. The air bridges are then defined by patterning a thick layer of PR using the ABME dark field mask. Since this PR defines the clearance between the air bridges and the bridged structures, it must be very thick - typically 5-10 μm . Next, electrodes are attached to an area of the wafer in which the seed layer is

AIR BRIDGE PROCESS ILLUSTRATION

STEP 1 : Pattern PR for air bridge spans on GaAs substrate

STEP 2 : Evaporate Ti-Au seed layer.

STEP 5 : Remove air bridge span PR.

STEP 3 : Pattern PR for air bridge spans.

STEP 6 : Etch exposed Ti-Au seed layer.

STEP 4 : Plate Au to form air bridge spans.

STEP 7 : Remove remaining PR to leave completed air bridge.

Figure 3.20 : Illustrated air bridge process.

exposed. The substrate is then placed in a potassium gold cyanide (KAuCN) solution in which the pH and specific gravity are maintained at 6.0 and 18° Baume, respectively. A current is forced through the seed layer to enable the electrochemical reaction which results in the plating of gold onto the areas exposed to the solution. At a current level of 3 mA, gold is plated for 30 minutes at a rate of 1.67 $\text{kÅ}/\text{minute}$ for a total gold thickness of 5 microns. The ABME PR is then removed to expose the remainder of the thin Ti/Au seed layer. In the next process step, the seed layer is removed using the KI-I_2 gold etchant and TFT titanium etchants described earlier. Finally, the remaining ABVI PR is stripped to leave the plated gold bridging successive air bridge posts. SEM micrographs of the resulting air bridges are shown in figure 3.21.

This completes the processing required for the fabrication of charge coupled devices from the CGAS15 set of masks. Evaluation and characterization of these devices is discussed in the next chapter.

Figure 3.21 : SEM micrographs of air bridges connecting successive clock phase 1 electrodes for (a) the SAG process and (b) the standard CCD gate process with $MSR = 1/4 \mu m$.

CHAPTER 4

CCD EVALUATION

With CCD fabrication complete, the devices are ready for evaluation. This chapter will describe the initial DC evaluation as well as the test setup and measurement techniques which are used for the subsequent RF characterization. The results of the characterization effort will then be discussed in terms of the device geometry and transport channel doping parameters.

4.1 DC EVALUATION

Immediately following CCD fabrication, a DC evaluation of the CCDs is performed to select the devices which will operate satisfactorily at higher frequencies. Tests which are performed at this stage include

- Verification of the input and output diode operation (G_0 , G_2 and G_3);
- Check for short circuits between adjacent gates G_1 and G_2 ; G_2 and ϕ_1 ; ϕ_1 and G_3 ;
- Check for short circuits between all combinations of the four clock electrodes taken two at a time; and
- Evaluation of the CCD as a FET using the input and output ohmic contacts for the source and drain contacts. The input diode (G_0) and the four clock electrodes are connected as gates to verify that it is possible to modulate the depletion width of the substrate using these terminals

Following the DC parametric tests, the wafer is scribed using a Tempress semi-automatic scribe, mounted on a piece of sticky plastic film and then diced. The film is then stretched to separate the devices. The individual devices are mounted in TriQuint MLC-44/24 packages using Able Bond conductive silver epoxy (Able Bond model 84-ILMIT). A Westbond thermal compression wire bonder (model 7416-15A-26-32-34-45) is then used to attach an 18 μm gold bond wire to connect each contact pad with one of 24 signal termination lines on the inside of the package. The packages are then mounted on TriQuint MLC-44/24 Engineering Test Fixtures (ETFs) for RF characterization.

A 32-bit GaAs cermet-gate charge-coupled device (shown prior to being mounted and bonded in the TriQuint package) is shown in figure 4.1. The TriQuint engineering test fixture used to evaluate the device performance is shown in figure 4.2.

4.2 MEASUREMENT SETUP AND VALIDATION

4.2.1 Measurement setup and bias conditions

An important preamble to CCD characterization at RF frequencies is to establish a test setup and to validate the setup by verifying proper CCD operation. The test setup is shown schematically in figure 4.3; biasing conditions for the test circuitry are described in the following paragraphs.

Figure 4.1 : A 32-bit GaAs cermet-gate charge-coupled device prior to being mounted and bonded.

Figure 4.2 : TriQuint MLC-44/24 Engineering Test Fixture.

Figure 4.3 : CCD measurement setup.

The first step in establishing the test conditions is to determine the pinchoff voltage of the substrate. This is achieved by connecting the input and output ohmic contacts to the source and drain inputs of a low frequency curve tracer and applying a forward bias so that current flows between the two contacts. Application of a negative potential to one of the clock electrodes will begin to deplete the substrate to close off the conduction channel. The pinchoff condition is achieved when the current is completely cut off (i.e. reduced to 0); the voltage required to cut off the current is referred to as the pinchoff voltage.

The clock pulses are supplied by means of an RF signal generator (Airborne Instruments Laboratory RF power source - Type 125) which drives a commercially available (OmniSpectra part no. 2094-6401-00) passive quadrature power divider. Thus, the clock pulses are in fact sinusoids whose amplitude is controlled by means of a variable attenuator at the output of the signal generator. Studies of the influence of the clock pulse shape have shown that while the CCD performance does not depend on the rise time of the clock pulse, the transfer efficiency has been seen to improve with increasing fall time [4.1]. Longer pulse fall times effectively increase the amount of time available for the last remnant of the charge packet to be transferred. Thus, the use of sinusoidal clock signals (which can be considered as pulse trains with relatively long rise and fall times) may not necessarily limit the CCD high frequency performance.

The peak-to-peak clock amplitude is optimized under several constraints. The clock amplitude should provide an electric field within the gap region which optimizes the electron velocity during the transfer. Secondly, the clock swing must be great enough that the potential barrier (created when the clock signal is in the low or 'off' state) is sufficient to completely prevent any transfer of charge. Finally, the maximum clock

amplitude is limited by the pinchoff voltage; any voltage greater than this value would increase the leakage current of the diode without altering the depletion region depth. In consideration of these constraints, the peak-to-peak clock amplitude is set to be equal to the pinchoff voltage of the substrate.

Next, the input and output ohmic contacts are biased positively to the magnitude of the pinchoff voltage. This is done to prevent the Schottky diodes which form the clock electrodes from ever becoming forward biased; such a situation would cause current injection into the CCD to distort the signal.

The signal is applied at the input gate G_2 . Since the injected charge packet size will be proportional to the voltage difference between G_2 and G_1 , the bias on G_1 is set to the level corresponding to the 'off' or lowest potential state of the signal which will be applied to G_2 . This will inhibit the injection of charge when the input signal is off to allow the CCD to operate with the best possible dynamic range.

At the output node, a DC bias is also applied at G_3 . While this bias is set to adjust the capacitance of the output node, there are several constraints upon its magnitude. First, the potential of G_3 must be greater than the minimum potential which will be applied to ϕ_4 . This will ensure that a charge packet appearing at ϕ_4 will be transferred from the region below ϕ_4 to the output when ϕ_4 is at its lowest potential. This potential must also be low enough to ensure that the G_3 diode is in deep depletion. As the depletion region becomes wider, the output capacitance (inversely proportional to the depletion width) becomes smaller. Thus, since $\delta V = \delta Q / C$, the charge-to-voltage conversion efficiency is improved. Finally, this reverse bias must not be so great that leakage current through this diode distorts the output signal.

This completes the establishment of the CCD test station. A typical response from a CCD when tested under these conditions is shown in figure 4.4. In this figure, the input appears as the upper trace; the lower trace represents the CCD output seen at the output of an inverting amplifier stage.

$F_{clk} = 500 \text{ MHz}$

Scales:

input (upper): 1.0 V/div;

output (lower): 0.2 V/div;

time: 20 ns/div

Figure 4.4 : Typical CCD Response (32-bit GaAs cermet-gate CCD with $M/S = 4/1$).

4.2.2 Measurement setup validation

An examination of the CCD geometry shows that a signal may be propagated from the input to the output of a CCD through a number of paths. When the device is operated correctly, the input signal meters the amount of charge which is injected into the substrate. The charge packet is then transferred through the substrate under appropriately clocked electrodes to be sensed at the output node. Alternatively, the

signal may propagate along the cermet film which connects G_2 , the clock electrodes and G_3 . This signal may be injected into the substrate at G_3 and then sensed at the output node without having undergone any clocked charge transfer operation. Other possible paths include electromagnetic propagation whereby the bond wires which serve to connect the CCD to the package will serve as antennas by which signals (at appropriate frequencies) may be broadcast and received; crosstalk between adjacent signal lines within either the package or test fixture used to mount the CCD may also allow the signal to bypass the semiconductor substrate. Finally, the signal may propagate through the DC bias lines to the output node.

One technique by which the test setup can be validated is to examine the delay between the input and output signals. When the signal is transferred by means of the applied clock pulses, the signal will appear at the output after a delay corresponding to the number of charge transfers multiplied by the transfer rate. While the propagation delay through any other means is indeterminate, correct CCD operation may be verified by comparing the expected with the actual signal propagation delay.

Thus, to validate the measurement setup, a low frequency impulse was applied to the input diode (G_2) of a 32-bit CCD as well as to one channel of an oscilloscope. The output of the CCD was then examined using a second channel of the same oscilloscope in order to perform time delay measurements. An effort was made to match the cable delays along the input and output paths so that the measured delay represented an accurate portrayal of the delay through the CCD. After the application of a 500 MHz clock and appropriate bias, the CCD response is shown in figure 4.5. Note that the theoretical delay is

$$\text{DELAY} = [\text{No of transfers}] \times [\text{transfer rate}] / [\text{number of clock phases}]$$

$$= [1 + 4 \times 32 + 1] \times [1/500 \times 10^6] / 4 = 65.5 \text{ ns}$$

The measured delay from the oscilloscope trace shown in figure 4.5 indicates 65.4 (± 2) ns. This agrees well with the predicted value to validate the measurement setup and test conditions.

Figure 4.5 : Response of a 32-bit CCD to an impulse function; the CCD input is on the upper trace (channel 3), the CCD output is shown on the lower trace (channel 4).

4.3 CCD CHARACTERIZATION TECHNIQUES

Losses within a CCD can be separated into a number of broad classes. One such division may distinguish the frequency-dependent losses from the fixed (or non-frequency dependent) losses. Fixed losses generally arise in the conversion of charge to voltage and vice-versa. A measure of these fixed losses can be obtained by plotting the output signal against the input signal for given clock and signal frequencies. The sensitivity and dynamic range of the device are both limited by these fixed losses.

Frequency-dependent losses arise due to incomplete charge transfer, charge trapping and non-linearities in either the input or output circuitry. The use of high quality components should minimize the influence of the test circuitry. Charge trapping effects are dominated by trap levels which arise at semiconductor interfaces; since charge transport in GaAs CCDs occurs within the bulk substrate (i.e. away from the interfaces), charge trapping phenomena are usually considered to be negligible. Frequency dependent losses are then attributed to incomplete charge transfer. A measure of these losses is the charge transfer efficiency (CTE) which expresses the percentage of the charge packet which is successfully transferred through an individual cell. The CTE is the most commonly used figure-of-merit for CCD characterization, and can be derived as shown below [4.2], [4.3].

The transfer efficiency is defined by considering the impulse response $H(t)$ of a CCD in the presence of incomplete charge transfer. First, consider a single transfer cell which, under clocked operation, transfers a fraction $(1-\epsilon)$ of the input signal during each

application of the clock. The output of such a system is a discrete-time function which can be represented by the following difference equation :

$$A_o(t) = (1 - \epsilon) A_i(t - T) + \epsilon(1 - \epsilon) A_i(t - 2T) + \epsilon^2 (1 - \epsilon) A_i(t - 3T) + \dots + \epsilon^N (1 - \epsilon) A_i(t - NT) \quad (4.1)$$

where A_i and A_o represent the input and output signals, respectively, of the CCD; and ϵ is the average transfer inefficiency of a single cell. Since this function is both linear and time-independent, the response can be analyzed using standard digital filter analysis techniques (i.e. representation in the Z-domain) [4.4]. Thus, the response is converted using the appropriate z-transform and simplified so that the impulse response can be expressed in closed form as

$$H(z) = z^{-1} \left[\frac{1 - \epsilon}{1 - \epsilon z^{-1}} \right] \quad (4.2)$$

where $H(z)$ is the z-domain representation of the transfer function of the CCD. This result can then be extended to obtain the impulse response of a CCD with N transfer stages as

$$H_N(z) = [H(z)]^N \quad (4.3)$$

which can be expanded and then re-written in the form

$$H_N(z) = z^{-N} \exp [N\epsilon(z^{-1} - 1)] \quad (4.4)$$

To examine the response of this system to an input signal of frequency f_s , the Laplace transform is used to obtain the impulse response in the frequency domain as

$$H(f_s) = \exp \left[N \epsilon \left(\cos \frac{2\pi f_s}{f_c} - i \sin \frac{2\pi f_s}{f_c} - 1 \right) \right] \quad (4.5)$$

where f_s and f_c are the input signal and clock frequencies, respectively. The magnitude of this impulse response can be considered to represent the portion of the amplitude attenuation of a charge packet which can be attributed to incomplete charge transfer; thus

$$\left| \frac{A_o}{A_i} \right| = \exp \left[-N \epsilon \left(1 - \cos \frac{2\pi f_s}{f_c} \right) \right] \quad (4.6)$$

The charge transfer efficiency of a CCD can be characterized using the frequency response method described by Vanstone et al. [4.5]. Using this technique, the CCD is operated using a given clock frequency (f_c) under the bias conditions described previously. The input signal is swept in frequency from 5 MHz to the Nyquist limit (corresponding to one half of the clock frequency) at a constant input amplitude. The CCD response is observed in the frequency domain by plotting the spectral response as a function of signal frequency. This data is downloaded to a PC for subsequent processing; a least-squares fit routine is used to eliminate the fixed losses from the data and then extract the CTE, as given in equation 4.7, shown below. The spectral response of a cermet-gate CCD which was tested at a clock frequency of 500 MHz with a -10 dBm input signal is shown in figure 4.6. The result of the least-squares fit to equation 4.7 is also indicated on the graph to show the excellent agreement which is obtained.

Spectral Response of a Cermet-Gate CCD

CERMET-GATE 32-BIT CCD (M/S: 3/2)

Figure 4.6 : Spectral response of a cermet-gate CCD.

Final Form of CTE Equation:

$$A_o = A \exp \left[-N_t (1 - CTE) \left\{ 1 - \cos \left(\frac{2\pi f_s}{f_c} \right) \right\} \right] \quad (4.7)$$

where A_o = output amplitude;

A = A_i - (non-frequency dependent (fixed) losses);

N_t = no of single electrode transfers;

f_s = signal frequency;

f_c = clock frequency; and

CTE = $1 - \epsilon$ = Charge Transfer Efficiency.

It should be noted that the authors of this characterization technique claim that the method should be accurate within 20 to 30%. Some effort was made during the CTE extraction to ensure that the extracted transfer efficiency figure of merit represented the minimum performance of these devices. Actual performance capability of these devices is believed to be much better than is indicated by the figure of merit. The use of this method to indicate relative performance potential is considered to be quite accurate.

In order to gain a better perspective on the use of the CTE as a performance indicator, two photographs illustrating the time-domain response of a 32-bit GaAs cermet-gate CCD have been taken. These photographs are reproduced in figure 4.7, where the input signal is shown on the upper trace; the CCD response is shown on the lower trace of each photograph. In both tests, the input signal is a pulse output of a frequency division (divide-by-16) of the clock frequency. For illustration purposes, the CCDs have been made to operate in a 'digital' mode where the channel was completely saturated for an input signal greater than a preset threshold. The upper photograph represents the response of the device with the clock frequency set to 500 MHz. The abrupt difference in the output signal level between the 'on' and the 'off' states of the input indicates good transfer efficiency. In fact, the transfer efficiency of this device has been measured to be 0.998. The lower photograph represents the response of the same device when operated at $f_c = 1$ GHz.

CTE = 0.998

$F_{\text{clk}} = 500 \text{ MHz}$

Scales:

input (upper): 1.0 V/div;

output (lower): 0.5 V/div;

time: 10 ns/div

CTE = 0.992

$F_{\text{clk}} = 1 \text{ GHz}$

Scales:

input (upper): 1.0 V/div;

output (lower): 0.5 V/div;

time: 5 ns/div

Figure 4.7 : CCD Time-domain response comparison: effect of transfer inefficiency for a 32-bit GaAs cermet-gate CCD with $M/S = 4/1$.

When comparing the two photographs, note that at 500 MHz, there are 9 clock cycles in which signal charge is evident, 7 without signal charge (the difference is due to a pulse duty cycle, at the threshold level, of slightly greater than 50%). At 1 GHz, signal charge is apparent in 10 consecutive clock cycles. The extra signal which appears at the trailing edge of the pulse corresponds to a charge packet which could not transfer in the requisite time; part of the charge packet was left behind during a previous transfer stage and was then swept through the device on the application of the next set of clock pulses. Thus, the degradation in the trailing edge of a signal is evidence of lower transfer efficiency. The CTE for the device operated under these conditions was calculated to be 0.992. The agreement between the frequency-domain calculation of the transfer efficiency and the time-domain response validates the usefulness of the CTE as a figure-of-merit to indicate relative CCD performance.

4.4 RESULTS

Once the measurement setup and techniques had been validated, a number of GaAs CCDs were tested to examine the influence of the cermet-gate structure on device performance as a function of device geometry and substrate specifications. The devices are tested with clock frequency between 500 MHz and 1 GHz; this limit is imposed by the useful operating range of the quadrature power divider. In most cases, the devices work quite well at 1 GHz and are expected to be operable at much higher frequencies.

4.4.1 CTE comparison: capacitive vs cermet-gate CCDs

Figure 4.8 shows the extracted charge transfer efficiency (CTE) of two 32-bit GaAs CCDs as a function of clock frequency. The data marked with circles represent the performance of a cermet-gate device; the data marked with squares represent the performance of a standard capacitive-gate CCD (so-called to distinguish them from the cermet-gate CCDs).

As the clock frequency increases, less time is available for the charge packet to travel from a given cell to an adjacent cell. Intuitively, one would expect that as the time available for transfer is reduced, more charge will be left behind after each transfer and the transfer efficiency should decrease. The data illustrated in figure 4.8 support this trend. The sharp drop in CTE above 800 MHz for the cermet-gate CCD performance is believed to be attributed to the impedance mismatch between the 50 ohm quadrature power divider used to generate the four-phase clocks and the complex impedance represented by the Ti-Au/cermet/GaAs Schottky diode. The mismatch will cause reflections which will effectively reduce the clock amplitude seen at the GaAs surface. A reduction in the clock amplitude will reduce the inter-cell potential well excursion; the strength of the fringing fields within the gap regions will be reduced to degrade charge transfer.

It should be noted that in the range of testing, the cermet-gate devices exhibited higher transfer efficiency than the CCDs which did not have cermet.

Figure 4.8 : CTE vs clock frequency for 32-bit cermet and capacitive-gate CCDs (MSR=4/1).

4.4.2 Dynamic range performance comparison

In order to gain an appreciation for the sensitivity and dynamic range of GaAs CCDs which would be achievable at RF frequencies, the device was operated with a 1-GHz clock frequency and a 70-MHz sinusoidal input signal whose amplitude could be varied from +10 dBm to -69 dBm. The output was observed on a spectrum analyzer which

was set to track the 70 MHz tone. A marker was used to provide a continuous readout of the output power as the input power was varied. This test was performed for a number of devices; the results for 32-bit GaAs CCDs with a cermet-gate and a capacitive-gate structure with Mark/Space Ratio (MSR) = 4/1 are illustrated in figure 4.9.

These results indicate that the devices have a sensitivity better than -30 dBm and a dynamic range of approximately 40 dB. Some roll-off in linearity is evident at very high input power levels, as the charge transport region becomes saturated. The difference between the results for the two devices can be attributed to two phenomena. The cermet film will increase the dynamic range of a CCD because the presence of the fringing fields within the gap regions implies that the charge storage region beneath each electrode will extend further laterally (into the gap regions) than for the non-cermet CCD. The second phenomenon which contributes to the difference between the measured results arises from a fabrication defect such that the G_1 and G_2 input diodes of all of the cermet-gate CCDs were shorted together. The apparent result would be to double the area of the input diode; hence the input capacitance is also doubled. As explained previously, this should improve the voltage-to-charge packet conversion ratio so that the sensitivity is expected to improve. Additionally, the larger input diode should store more charge. Thus, under test conditions where the input region limits the charge-handling capability, (the charge transport capacity of the CCD is actually limited by the minimum charge storage ability of the three regions of the device), the dynamic range of the CCD will be improved. The penalty for this improvement in sensitivity and dynamic range is expected to be the maximum frequency of operation. As the input capacitance increases, the CCD response to high-frequency signals will degrade. However, the performance limitations (in terms of high speed response) have been

Figure 4.9 : Dynamic range performance comparison of two 32-bit GaAs CCDs with $MSR=4/1$ at $F_{clk} = 1.0$ GHz.

shown to be beyond the measurement capability of the test setup presently used. Further experiments are currently being performed to quantify the effects of this defect.

4.4.3 Summary of results of CTE measurements for other devices

A number of other devices have also been evaluated at RF frequencies. CCD performance (particularly CTE) has been evaluated with the devices operating at a clock frequency of 1 GHz. The device specifications and their respective performance indices are listed in Table 4.1.

The first four entries in Table 4.1 represent the results of an experiment which was intended to illustrate the degradation in performance as a function of the ratio between the gate and gap lengths of the clock electrode cells, termed the Mark/Space Ratio (MSR). As the MSR decreased (corresponding to an increase in gap length), the CCD performance was expected to deteriorate because of the difficulty in establishing the requisite electric fields across the increasingly large gap regions. When these devices were tested, it was found that the CTE did not vary with the MSR. This result is attributed to the use of a thick, lightly doped transport channel which could be completely depleted laterally across the gap regions. This result indicates that for this choice of substrate, the gap lengths are not the limiting factors which determine the device performance.

The next three entries are intended to illustrate the performance of cermet-gate CCDs. Operation of 32 and 64-bit cermet-gate CCDs has been verified, with excellent results. Since the definition of CTE implies the transfer efficiency per individual transfer, the CTE figure of merit is expected to be independent of the number of transfer cells. This concept is borne out by the results presented in the table.

Table 4.1 : CCD Performance Summary

Transport Channel Specification	Gate Structure	Number of Bits	M/S	CTE ($F_{clk} = 1 \text{ GHz}$)
'Standard' $2 \times 10^{16} \text{ cm}^{-3}$; $1.0 \text{ } \mu\text{m}$	Capacitive	32	4/1	.995
	Capacitive	32	3/2	.995
	Capacitive	32	2/3	.996
	Capacitive	32	1/4	.996
'Standard' $2 \times 10^{16} \text{ cm}^{-3}$; $1.0 \text{ } \mu\text{m}$	Cermet	32	4/1	.995
	Cermet	32	3/2	.993
	Cermet	64	4/1	.996
'FET-compatible' $2.5 \times 10^{17} \text{ cm}^{-3}$; $0.25 \text{ } \mu\text{m}$	Cermet	32	4/1	.981

These results are consistent with the published findings of other researchers. Previously published results of devices which are similar to the capacitive gate CCDs reported here claim CTE between 0.994 and 0.999 at clock frequencies up to 1 GHz [4.6, 4.7]; this seems to be a practical frequency limit for testing these devices. A recent publication indicates from performance simulation that CCDs with the same transport channel specifications (albeit with smaller 0.4 micron gaps) should operate with $\text{CTE} = 0.999$ up to 3.3 GHz [4.8]. While the results of the cermet-gate CCDs are not directly comparable to any other published results, 'gapless gate' cermet CCDs have been

shown to be operable up to 4.2 GHz; CTE of these devices has been evaluated to be 0.99 at 2.5 GHz [4.9].

Finally, a cermet-gate CCD has been fabricated on a substrate which includes epitaxial layers which are compatible with the in-house FET process at CRC. Note that this choice of substrate ($N_D = 2.5 \times 10^{17} \text{cm}^{-3}$, 0.25 μm thick) should preclude the operation of capacitive-gate CCDs, because the inability to completely deplete the gap region would leave significant potential troughs to prevent charge transfer. The use of a cermet-gate structure overlying the CCD transport channel has allowed us to demonstrate successful operation of this device with fair performance up to the limits of our test equipment, at a clock frequency of 1 GHz.

The performance of the devices fabricated on the FET-compatible substrate was not as good as those fabricated on the standard CCD substrate for reasons relating to the doping dependency of the leakage current through the cermet-GaAs Schottky barrier diode. As the diode curves illustrated in figure 4.10 suggest, the devices which were fabricated on the highly doped channel exhibited significantly greater leakage current than the other devices. Leakage through the gates of these devices was found to overwhelm the relatively small signal charge packets present in the channel so that the signal became difficult to detect.

Thus, the use of the cermet has been found to improve the performance of GaAs CCDs by allowing integration of CCDs on FET-compatible substrates. It has also been shown that the incorporation of a cermet film does not degrade the performance of CCDs when their performance has been shown to not be limited by the extended gap regions.

Figure 4.10 : Comparison of the leakage current of various GaAs Schottky diodes.

CHAPTER 5

SUMMARY

5.1 CONCLUSIONS AND RECOMMENDATIONS

The motivation for GaAs CCD development was reviewed in the first chapter of this thesis. The subsequent chapters described the device design, fabrication, operation and RF evaluation of a number of GaAs CCDs. This work is summarized as follows.

5.1.1 Design

The issues which must be considered in the design of high-performance charge-coupled devices were described and qualitatively analyzed in chapter two. The first design issue to be resolved is the choice of the substrate parameters (carrier concentration and thickness) to be used for the transport channel. It was found that thick, lightly doped channels (typically $2 \times 10^{16} \text{ cm}^{-3}$, $1 \text{ }\mu\text{m}$ thick) should be used to ensure good transfer efficiency for CCDs which use capacitive gate structures. Monolithic integration of such structures with D-MESFET support circuitry is, however, not possible because MESFETs are generally fabricated on thin, highly doped substrates (typical carrier concentration is $2.5 \times 10^{17} \text{ cm}^{-3}$, $0.25 \text{ }\mu\text{m}$ thick). If compatibility with FET processing is required, the deposition of a resistive cermet film within the inter-electrode gaps was found to establish a monotonic fringing field within the gap regions

of the transfer cells. Thus, the substrate requirement which specifies that the carrier concentration be low enough to establish fringing fields completely across the gap regions may be relaxed to permit the adoption of FET-compatible layer structures.

GaAs substrates on which both the standard CCD transport channel layer structure (described previously) and the 'FET-compatible' layer structure had been grown by MOCVD were procured for the fabrication of both capacitive and cermet-gate CCDs.

Next, a number of considerations were discussed with respect to the geometric design of the CCD transport cell. Implications of the choices of gate and gap lengths, cell width, number of cells per pixel and the total number of cells forming the CCD were discussed qualitatively. It was found that in general, the design of CCDs requires an intimate knowledge of the processing capabilities of the foundry, as device performance must be traded off against ease of fabrication. Furthermore, it was found that these trade-offs may be relaxed by adopting alternate processing methods. Preliminary investigations of the self-aligned gate (SAG) process showed promise as a means of defining fine (submicron) lines without incurring added lithographic definition complexity. Similarly, the use of a resistive film in the inter-electrode gap regions, as described previously, will reduce the performance penalties associated with long inter-electrode gap lengths. Thus, the gap lengths of cermet-gate devices could be increased to ease the lithographic tolerances of the low-yield clock electrode definition process. This development should allow the fabrication of CCDs with relatively long inter-electrode gaps for higher yield without sacrificing device performance.

Additionally, design techniques to optimise the linearity of the charge injection and sensing operations were discussed. It was found that optimum charge injection is

accomplished using a variation of the 'potential equilibration' technique which requires an input ohmic contact and two Schottky diodes fabricated on the transport channel layer. In this technique, the input signal is applied to the second diode while the first is held at a fixed DC potential to control the full well charge packet size. Design options have also been considered to investigate variations on output sensing techniques.

In order to quantify some of the design trade-offs, a number of design options were implemented on the CRC CGAS15 mask set so that charge-coupled devices could be fabricated at the Microelectronics Facility of the Communications Research Centre. This mask set and a number of the experiments which can be performed using the devices fabricated from this mask set were also described in chapter two.

5.1.2 Fabrication

GaAs cermet-gate CCDs were fabricated using a 9 mask process at the Communications Research Centre. The complete fabrication process and the required process development were described in the third chapter.

The transport channels were formed using both MOCVD and ion implantation. The implant parameters (species, fluence and dose) were calculated to match the epitaxially grown CCD transport channel layers described previously. Additional dopant incorporation for FET channels and ohmic contact regions was also performed by ion implantation. Si^0 was selectively implanted for each of the three implant steps through masks of Si_3N_4 and photoresist at the BNR laboratories in Ottawa, Ontario. The

implants were activated using a black body re-radiation process from a carbon susceptor in a Rapid Thermal Anneal (RTA) oven. During the anneal process, arsenic evolution from the GaAs substrate was suppressed by creating an arsenic overpressure within the susceptor used to anneal the wafers. Activation efficiencies in excess of 60 percent were calculated based on Hall mobility measurement data. For the MOCVD-grown layers, a mesa etch was performed so that the semi-insulating GaAs substrate would provide isolation between devices.

Next, a cermet film was deposited by magnetron RF sputtering at the TRIUMF facility in Vancouver, B.C. A dielectric-aided liftoff process was developed to assist the definition of this film. Evaluation of test structures on the mask indicated that the cermet-GaAs junction exhibits rectifying properties; diode parameters for the equivalent cermet-GaAs Schottky diode were measured as $\phi_B = 0.64\text{V}$, $n = 1.23$, $I_s = 0.49\text{nA}$ and $R_s = 475\Omega$. In the following process step, a Au-Ge-Ni eutectic metallization was evaporated in the ohmic contact regions of the device. The RTA was then adapted and a process developed and characterized to provide ohmic contacts with low contact resistance to the n^+ implanted regions of the CCD wafers.

Following the ohmic contact definition, a fine line liftoff process was developed in order to successfully define clock electrode patterns consisting of 512 (128 bits $\times$ 4 electrodes/clock cell) $1\text{ }\mu\text{m}$ long electrodes, each of which is separated by a $1\text{ }\mu\text{m}$ gap. Clock electrodes were patterned using this process; the substrate was subsequently glassivated with Si_3N_4 to protect the fragile gate regions. Next, Ti-Au was defined to form the contact pads and (first level) interconnects between the devices and the contact pads. Finally, air bridges were used to form the cross-over (second level) interconnects between every fourth clock electrode, to build up the contact pad metallization prior

to bonding and to connect the devices to one of several configurations of output circuitry to complete the CCD fabrication process.

5.1.3 Operation

Once the fabrication process was complete, preliminary DC testing was performed to determine the gate and ohmic contact integrity. Screening criteria used to select devices included the pinch-off voltage and saturation current of the transport channel when the CCD was operated as an ultra-long FET. Selected devices were finally mounted and bonded in 24-pin packages to test for functionality in preparation for RF characterization.

A modified version of the potential equilibration charge injection technique was used to inject charge into the transport channel. Quadrature (four-phase) clock signals were applied to the gate electrodes to enable the transfer of charge from the input region to the charge sensing region of the CCD. At the output, a single diode was used to help decouple the clock feedthrough from the signal. The voltage of the output node was then coupled directly to either an oscilloscope (for time-domain measurements) or a spectrum analyzer (for frequency domain characterization). Correct operation of the CCD was confirmed by examining the delay experienced by a narrow pulse which was injected into the transfer region of a 32-bit CCD and then clocked (at $F_{clk} = 500$ MHz) to the output node. The transfer delay was confirmed to be approximately $32 \times (1/500 \times 10^6)$ seconds to verify the measurement setup and techniques.

5.1.4 Evaluation

In order to establish performance criteria, losses within a CCD were analyzed and categorized into two broad classes: these are the frequency dependent losses and the fixed (i.e. non-frequency-dependent) losses. Fixed losses were characterized by the sensitivity and dynamic range of the device, as measured by plotting the output power against the input signal power. Frequency dependent losses were characterized by the charge transfer efficiency (CTE). The CTE was evaluated by performing a least-squares fit of the spectral response of the CCD to an equation which was derived to represent the theoretical transfer efficiency of a single transfer stage. The use of the CTE parameter as an indicator of relative charge transfer performance was verified by establishing commonality between the time-domain response and the CTE figure of merit. Excellent transfer efficiencies of 0.998 at $F_{clk}=500$ MHz and 0.996 at $F_{clk}=1$ GHz (which represents the maximum clock frequency achievable with the present test setup) were measured to verify the high frequency performance capability of these devices.

Finally, a number of CCDs which were fabricated with different transport channels, gate structures and cell geometries were evaluated for purposes of performance comparison. Performance trends, indicated by the sensitivity, dynamic range and CTE figures of merit, are summarized below.

- The CTE of capacitive-gate CCDs which use a thick, lightly-doped transport channel did not vary with mark-to-space ratio for clock frequencies up to 1 GHz. This indicates that the gap length (for $L_g = 1$ to $4 \mu\text{m}$) is not the factor which limits capacitive-gate CCD performance for this choice of substrate at these frequencies.

- For a given cell geometry, the transfer efficiency did not vary with the total CCD length, as the length was increased from 32 to 64 pixels. This confirms that longer devices can be fabricated with excellent high frequency performance. This result also verifies the formulation of the transfer efficiency as a measure of the average loss per single stage transfer operation.
- Cermet-gate CCDs were found to exhibit comparable or higher transfer efficiency, better dynamic range and sensitivity than CCDs which were fabricated with capacitive-gate structures (for constant MSR and channel specifications), at the cost of increased process complexity.
- The use of the cermet-gate structure has allowed the demonstration of fair performance up to $F_{\text{clk}} = 1$ GHz of a CCD which was fabricated on a substrate compatible with the CRC D-MESFET process. This demonstration establishes the viability of the future monolithic integration of CCDs with MESFET signal processing and driver circuitry.

5.2 CONSIDERATIONS FOR FUTURE WORK

5.2.1 Evaluation of the remaining CCD design options from the CGAS15 mask set

Departmental restrictions regarding the amount of time to be expended on a Master's thesis have not allowed the author to investigate all of the experiments available on the CGAS15 mask set. In fact, a significant amount of work remains to be performed before the possibilities inherent within this mask set are exhausted. Since several process runs of CCDs have already been fabricated, a number of experiments are currently available for evaluation. Some of the experiments which remain include:

- an evaluation of the devices intended to investigate the potential for the integration of high frequency signal processing functions using CCDs;
- an examination of the CCD performance as a function of other aspects of the cell geometry such as changing the gate length (to vary the total cell size); and
- an investigation into the effects of modifying the doping concentration of the input diodes and the use of some of the alternate output sensing arrangements.

Additionally, continued investigation of other processing options such as the self-aligned gate (SAG) process and the use of ITO contacts should prove interesting.

5.2.2 Extended RF performance evaluation

One of the limitations of the present work was that the RF evaluation was limited by available test equipment to the clock frequency range between 500 MHz and 1 GHz. The upper frequency limit was not sufficient to illustrate the performance degradation which is expected to occur as the time required for a charge packet to transfer across a given cell geometry approaches the maximum available transit time, which is limited by the clock frequency and pulse shape. Since a recent evaluation of a CCD with a HEMT-based transport channel structure has verified charge transfer operation at clock frequencies up to 16.4 GHz [5.1], it is evident that the upper frequency performance limits of these devices have not yet been fully exploited. Higher frequency performance verification will, however, require more complicated clock circuitry to generate the required power at microwave frequencies. Thus, alternate clocking arrangements (such as a simpler two-phase clock) need to be considered.

Along with higher frequency performance evaluation, a significant amount of work may be required to verify the validity of current CCD performance characterization techniques at microwave frequencies.

5.2.3 Reduction of the leakage current of the cermet/GaAs junction

As described in the previous chapter, the factor which currently limits the performance of cermet-gate CCDs fabricated on FET-compatible substrates is the leakage current of the cermet-GaAs contact. Thus, in order to respond to the requirement for the integration of CCDs with MESFET support circuitry for microwave

frequency signal processing applications, the leakage current of the cermet-GaAs Schottky diode must be reduced. To investigate the potential performance capability of these devices, the leakage current of currently fabricated devices can be reduced by cooling the substrates. High performance operation of these devices at room temperature, however, will require an investigation of alternate contact materials to provide a resistive gate structure with a higher barrier height to a GaAs FET-compatible substrate than is currently possible with 45% Cr : 55% SiO.

Alternatively, the diode leakage current may be reduced by forming the clock electrode Schottky contacts on an AlGaAs layer on top of the transport channel. Since the barrier heights of Schottky diodes fabricated on $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ are higher than similar diodes fabricated on GaAs (due to the lower electron affinity of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ with respect to GaAs), the leakage current of the former diodes will be correspondingly lower. Integration of the resulting CCDs with GaAs/AlGaAs-based high electron mobility transistors (HEMTs) should result in excellent performance.

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APPENDIX : CGAS15 MASK LAYERS

This appendix lists the mask layers included on the CGAS15 mask set. The first 9 layers listed are required for the baseline cermet-gate CCD process. Other layers are optional, as indicated below.

LAYER #	LAYER NAME	CONTRAST (LF / DF)	FUNCTION
1	MESA	LF	Transport channel isolation
2	NPIM	DF	N ⁺ implant for ohmic contacts
4	EDIM	DF	N implant for FET channels
15	CMET	LF	Cermet definition
5	OHMC	DF	Ohmic contact definition
7	GATE	DF	Gate (Schottky) metal definition
9	FLME	DF	First level interconnect metal
10	ABVI	DF	Air bridge vias
11	ABME	DF	Air bridge metal spans
22 (* 1)	SAGE	DF	Self-aligned gate etch
8 (* 2)	DIEL	DF	Dielectric etch
12 (* 2)	PASS	DF	Passivation
13 (* 3)	ALIK	LF	Alignment key

* 1 : Optional layer, used only for the SAG process.

* 2 : Not used.

* 3 : Used only when the charge transport channel is defined by ion implantation. Otherwise, alignment information is provided by the MESA mask.

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