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An FM Receiver Based on a Δ - Σ Frequency Discriminator

by

Theodore G. Pantazopoulos, B. Eng.

A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of

Master of Engineering

Department of Electronics

Carleton University
Ottawa, Ontario
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**"An FM Receiver Based on
a Δ - Σ Frequency Discriminator "**

submitted by Theodore G. Pantazopoulos, B.Eng.
in partial fulfillment of the requirements for
the degree of Master of Engineering

Thesis Supervisor

Chair, Department of Electronics

Carleton University
February 1996

Abstract

A Digital Signal Processing back end for use in a Δ - Σ frequency discriminator based radio receiver is presented in order to validate the use of this type of frequency discriminator in a radio receiver for digital FM signals. The use of adaptive filtering algorithms in order to arrive at a filter response that will maximize the bit error performance of the receiver in the presence of non-white (shaped) quantization noise is investigated.

Through simulation, an LMS algorithm based filter with a decision feedback section is shown to improve the bit error rate performance of the receiver as the filter converges. The RLS algorithm is used as a tool to design a fixed filter for a Δ - Σ discriminator based receiver. The design of a hardware test bed for a transmitter and receiver is described and the finished hardware is used to demonstrate the viability of using a Δ - Σ frequency discriminator as part of a radio receiver for digital FM signals.

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Chapter 1:

Introduction

1.0) : Introduction

There is presently a trend towards a higher level of VLSI integration for digital radio receivers, including a greater reliance on digital signal processing (DSP) rather than analog signal processing. Such a reliance implies the need for higher speed, lower power A/D conversion in the receiver. This thesis is based on the potential use of a new type of A/D conversion, based on delta-sigma (Δ - Σ) noise shaping techniques, as part of the receiver.

Δ - Σ A/D conversion in its simplest form results in a high speed oversampled one bit digital bitstream, which must be decimated and processed digitally. The form of Δ - Σ A/D conversion considered here is unusual in that it is fundamentally a frequency to digital converter, i.e. a frequency discriminator, (see figure 1.1) and thus is suitable for FM receivers. This form of frequency discriminator is the result of earlier work at Carleton University [1] but its application in an FM receiver has not been considered in detail before this thesis.

In order to process the digital bitstream from the Δ - Σ frequency discriminator in a near-optimal manner, adaptive filtering techniques could be employed in the DSP part of

Figure 1.1 : Concept of Frequency-to-Digital Converter

Figure 1.2 : Adaptive Receiver based on Frequency-to-Digital Converter

the proposed receiver architecture either to design a fixed filter to follow the discriminator or to modify the characteristics of a filter with variable coefficients. In addition, the use of decision feedback techniques could help to mitigate the effects of inter-symbol interference (ISI) from previous symbols (see figure 1.2).

This thesis presents an investigation into the use of adaptive filtering techniques to process digital signals derived from Δ - Σ A/D converters, including the Δ - Σ frequency discriminator as an example. The Δ - Σ discriminator is used at the intermediate frequency (IF) stage of the radio receiver to obtain a digital measure of frequency deviation which is then processed by a digital predetection filter. The adaptive algorithms are used in the receiver to optimize the tap weights of the predetection filter such that the bit error rate (BER) is minimized. The emphasis is on the use of the recursive least squares (RLS) algorithm to arrive at a set of tap weight coefficients for a predetection filter with fixed coefficients. The resulting digital filter is then used to process a digital signal derived from a Δ - Σ frequency discriminator A/D converter whose input embodies GFSK type modulation. The least-mean-squared algorithm (LMS) is shown through simulation to reduce the bit error rate of a GFSK-type receiver as the filter adapts to the received signal.

Using RLS, the goal is to arrive at the optimum filter that will minimize the bit error rate (BER) of the digital signal in the presence of quantization noise and premodulation filter-induced inter-symbol interference (ISI). This filter is then implemented in hardware and tested with bitstreams from a real Δ - Σ frequency discriminator.

Through simulation, it is shown that a filtering strategy composed of an LMS based filter with a decision feedback section can improve the bit error rate. The LMS algorithm can be readily implemented in a low-power silicon technology and represents a possible solution for the detection of GMSK signals in the additive white Gaussian noise (AWGN) channel with slow, flat fading as is encountered in DECT receivers. The algorithm is not intended to be used in applications where a linear receiver is required, such as GSM.

1.1) Survey of the Previous Art

Frequency modulation techniques were originally employed for the transmission of analog signals for voice communication. By employing large frequency deviations, FM demodulation could be performed reliably using a variety of analog techniques. Such techniques were realized using simple analog circuits and relied heavily on the threshold effect inherent in FM systems in order to provide acceptable performance.

The use of limiter-discriminator detection has been discussed at some length in the literature [2]. The particular circuit techniques used in the previous art to realize the discriminator were analog in nature (see figure 1.3a) and thus required component matching or tuning to achieve satisfactory performance, particularly in the context of analog modulation. For analog frequency modulation with large modulation indices, such circuits resulted in satisfactory performance.

For the case of modulation techniques for digital signals, frequency shift keying has been employed in the previous art, without premodulation filtering. The absence of premodulation filtering combined with the use of wide frequency deviations permitted acceptable BER performance to be obtained using simple limiter-discriminator circuits followed by a decision circuit composed of compromise low-pass filter and a level slicer (see figure 1.3(b)).

As the number of applications and associated users of radio communications expands, it has become evident that in order to accommodate this growth there is a requirement for

Figure 1.3(a) : Analog Frequency Discriminator

Figure 1.3(b) : Limiter-Discriminator Receiver

Figure 1.3(c) : Digital Receiver Based on Δ - Σ Discriminator

modulation techniques that can be used to transmit the same or greater amounts of data while occupying less bandwidth. This has led to the development of a great number of "spectrally efficient" digital modulation techniques. These techniques include modulation of amplitude and/or phase as well as filtering of the data and/or the modulated signal.

Consistent with the goal of improved spectral efficiency for digital signals, frequency modulation techniques such as minimum-shift keying (MSK) [3] have been suggested. MSK uses a modulation index of $h=0.5$ in order to improve spectral efficiency. A further improvement in spectral efficiency can be obtained by the use of a Gaussian lowpass filter before the modulator to modify the data pulse shape [4]. The use of MSK improves spectral efficiency while allowing a variety of demodulation techniques to be employed [3], [5], [6]. Such demodulation techniques include the techniques referred to in the above paragraphs [7], but with performance that is inferior to that which is obtainable with more sophisticated DSP.

1.2) Approach of the Thesis

The advent of high speed, low power VLSI technology has permitted implementation of the digital signal processing algorithms in a reliable, cost-effective manner. Digital signal processing techniques can be used to incorporate sophisticated signal processing algorithms in order to obtain reliable signal performance while retaining spectral or power efficiency in communication links.

Before performing extensive digital signal processing on digital FM signals, a circuit technique is required to obtain an accurate digital measure of the instantaneous frequency deviation (or equivalently, the phase trajectory) of the signal. The two techniques that have gained prominence in the literature are the balanced quadricecorrelator and the arctangent detector. Although these techniques have provided satisfactory results, they require separate linear A/D converters with the accompanying penalties of increased power consumption and limited dynamic range, and they require low input frequencies to achieve satisfactory performance.

In order to obtain a digital measure of the frequency deviation, Beards and Copeland [8] devised a frequency discriminator which operates on the principle of performing an analog to digital conversion on the time required for zero crossings to occur in the FM signal. For small frequency deviations relative to the center frequency, the discriminator is highly linear in frequency and hence provides an accurate digital representation of the frequency deviation of the input signal. This is the realization of the combined frequency discriminator and A/D converter shown in figure 1.3(c).

Given that an accurate digital representation of the frequency deviation is available, the appropriate digital filtering and detection algorithms may be chosen and implemented. The filtering stage will typically be composed of a Wiener filter, which in the presence of white noise is simply a filter with an impulse response matched to the transmitted pulse shape. In the case of non-white noise, the matched filter is no longer optimum in a minimum mean-squared error sense. If a premodulation filter has been used that adds ISI, then some additional requirements are placed on the filter since the individual pulses are no longer independent of each other.

It is also important to note that the conversion from the bandpass FM signal to a measure of the frequency deviation cannot be performed using a linear circuit network [7]. The application of a signal corrupted by (bandlimited) AWGN to a non-linear network causes fundamental changes in the statistics of the noise process and hence the noise at the output of the discriminator can no longer simply be assumed to be white. In fact, it may no longer even be assumed to be stationary.

The Δ - Σ frequency discriminator, just as any A/D converter with finite resolution, produces quantization noise. Statistically, the quantization noise is non-white and is deliberately made that way in an effort to separate the baseband signal from the quantization noise in the frequency domain. In a statistical sense, such an action is equivalent to decorrelating the signal and the quantization noise. In higher order Δ - Σ

converters such as the discriminator used in this thesis, which is second order, the baseband signal and the noise have the potential to be highly uncorrelated [8].

Many Δ - Σ converters employ a two level quantizer, resulting in a digital output which is either a '0' or a '1'. Although this results in very coarse quantization when considered on a sample-by-sample basis, the sampling rate employed is many times greater than the rate required by the Nyquist theorem. A higher resolution, multi-bit representation can be obtained by filtering the output of the converter. The filtering effectively band-limits the digital signal and therefore permits the filtered digital signal to be sampled at a rate much lower than the sample rate of the converter. The ability to sub-sample the digital signal after filtering is a consequence of the fact that band-limiting the signal increases the correlation between samples when taken at the oversampled rate. The practice of sub-sampling or "decimation" must be performed judiciously though, since any residual out-of-band power will be aliased back into the baseband when the signal is sampled at the lower rate.

The choice of filter characteristics will depend on the characteristics of the desired signal and the desired sampling rate. If the objective is to accurately reconstruct the transmitted signal, the final sampling rate will have to be at least twice the nominal bandwidth of the original signal. Such a filtering strategy does not take into account the characteristics of the noise with which the signal may be corrupted. Hence, although the filter will accurately reproduce the desired signal, the noise that resides in the same frequency band of the signal may cause the signal-to-noise ratio (SNR) of the composite signal to fall below some acceptable value. In an effort to quantify the effects of this type of signal corruption, the mean-squared error is often used as a criterion. By minimizing the mean squared error, the optimum Wiener filter solution is arrived at.

In the context of the present work, we do not seek to reproduce exactly the transmitted waveform, but to recover the value of the data processed by the premodulation lowpass filter in the transmitter. The optimum filter must therefore combat both the effects of

Figure 1.4 : Δ - Σ Discriminator Based Receiver

noise and ISI due to the premodulation lowpass filter. Only one output sample per data symbol is required. The statistics of the received signal are cyclostationary in the short term, with period equal to the symbol period. Therefore the output of the filter will be valid only at one specific instant per symbol period (see figure 1.4).

1.3) Thesis Overview

The thesis first expands on the general overview provided in chapter 1 by providing more in-depth background material in chapters 2, 3 and 4.

Chapter 2 reviews Gaussian minimum shift keying by describing a general class of digital FM signal known as continuous phase frequency shift keying (CPFSK). The discussion then goes on to describe how minimum shift keying and GMSK are special cases of the broad class of CPFSK signals.

Chapter 3 reviews techniques that can be used for the demodulation and detection of digital FM signals. The review covers techniques that employ either analog or digital circuitry at various levels of sophistication. The review is limited to techniques that are useful for detecting digitally modulated FM signals. The Δ - Σ discriminator is also included in the review as a candidate for the demodulation of digital FM signals.

Chapter 4 reviews adaptive filtering techniques and presents the relevant equations in what is hoped to be their most useful form. Both the LMS and RLS algorithms are described.

Chapter 5 presents the results of the simulation of a Δ - Σ frequency discriminator model and simulation of the discriminator model with an adaptive filter processing the bitstream from the discriminator. Relevant results from both LMS and RLS techniques are compared and then finally an LMS based DFE is also simulated.

Chapter 6 describes the design of a hardware test bed used to perform filtering of the bitstream from a board level Δ - Σ frequency discriminator. The hardware testbed is used to test the performance of a discriminator-based receiver using filter coefficients designed using simulations of the Δ - Σ frequency discriminator and an adaptive filter.

Chapter 7 presents conclusions and provides recommendations for future work.

Chapter 2:

Gaussian Minimum Shift Keying

2.1) Introduction

The type of modulation used in several of the proposed personal communication standards is Gaussian-filtered Minimum Shift Keying (GMSK), [4]. This type of modulation is highly desirable from an implementation perspective since it is a constant envelope modulation scheme. This allows for the use of non-linear amplification with its associated power efficiency without the consequence of spectral regrowth that is incurred when using modulation schemes that do not possess a constant envelope.

Figure 2.1 : GMSK Modulator (Continuous Phase)

In principle, GMSK is a modulation that is relatively straightforward to implement. A representative GMSK modulator is shown in figure 2.1. As can be seen from the figure, the individual data bits are filtered by the premodulation lowpass filter (LPF) and applied to a voltage controlled oscillator (VCO). The modulation sensitivity of the VCO must be chosen to satisfy the peak frequency deviation requirements of the modulation and the VCO must exhibit good long term stability of the nominal frequency. Although GMSK modulators are not covered in detail in this document, the reader is referred to the paper by Riley and Copeland [11] which presents a novel circuit technique to generate GMSK as well as references to other techniques.

This chapter provides an overview of digital frequency modulation by first examining a broad class of modulation known as constant-phase frequency shift keying (CPFSK). Minimum shift keying (MSK) is then identified as a particular case of CPFSK. GMSK is then described as MSK with Gaussian premodulation filtering and the effects of the addition of the filter are highlighted.

2.2) Continuous-Phase Frequency Shift Keying

Continuous-phase frequency shift keying (CPFSK) is a digital frequency modulation scheme in which the frequency of the carrier is increased or decreased by a discrete amount in order to represent a corresponding data symbol. In general, it is possible that the frequency of the carrier attains M different levels in order to uniquely represent any one of M different possible data symbols. The frequency deviation (f_d), of the carrier for a given symbol, I_n , is equal to:

$$f_{d,n} = \frac{\Delta f}{2} I_n, \quad I_n = \pm 1, \pm 2, \dots, \pm(M-1)$$

where Δf is the frequency separation between adjacent levels. In this work, the number of levels considered will be limited to $M=2$. The case of $M=2$ is commonly referred to as binary CPFSK.

As implied by the name, CPFSK is a special case of frequency shift keying in which the phase of the modulated signal is continuous. Instantaneous changes in the phase of the modulated signal waveform are not permitted to occur and hence, the derivative of the phase of the signal is finite at all times although not necessarily differentiable at all times, depending on the data pulse shape applied to the modulator. For instance, if the data are passed through a filter whose impulse response is a square pulse, the frequency will change instantaneously causing a phase step at the instant of the data transition; the phase will remain continuous though.

The continuous phase property implies that the frequency of the signal is shifted by the modulation pulse stream with the constraint that the phase does not change instantaneously (i.e. the derivative of the phase remains finite). CPFSK can be described by equation 2.1 as shown below,

$$s(t) = A \times \text{Re}(e^{j(2\pi f_c t + \phi(t) + \phi_o)}) = A \cos(2\pi f_c t + \phi(t) + \phi_o) \quad (2.1)$$

where f_c is the carrier frequency in Hertz, $\phi(\tau)$ is the "excess phase" (in radians) produced by the modulation and ϕ_o is an arbitrary starting phase.

The excess phase produced by the modulation, starting at time $t=0$, is the integral of the baseband signal $f(t)$ used to modulate the frequency of the carrier as described by equation 2.2.

$$\phi(t) = 2\pi \int_0^t f(\tau) d\tau \quad (2.2)$$

It can therefore be seen that due to the integration, the baseband frequency modulating waveform $f(t)$ need not be continuous for the phase of the CPFSK waveform to retain continuity.

A convenient expression for the baseband frequency modulating waveform is

$$f(t) = \frac{h\pi}{T} \sum_n I_n b(t - nT) \quad (2.3)$$

The form of $f(t)$ shown above distinctly shows the modulating index, h , and the data symbols, I_n , as well as the impulse response of the baseband filter, $b(t)$.

2.3) Minimum Shift Keying

Before delving into the details of GMSK, it is useful to examine MSK modulation first in order to understand how they are related. The MSK modulation scheme was first described by Doelz and Heald [12] and later summarized by Pasupathy [13]. Minimum shift keying is a form of continuous phase, frequency shift keying (CPFSK) with a modulation index, h , of 0.5 where the modulation index is defined as :

$$h = \frac{\text{frequency deviation}}{\text{symbol rate}}$$

For MSK, the impulse response of the baseband filter is described by:

$$b(t) = 1; 0 < t \leq T, \quad 0; \text{otherwise} \quad (2.4)$$

A system suitable for producing MSK is shown in figure 2.2. As can be seen from the figure, the data symbols, I_n , are represented by impulses spaced T seconds apart, therefore making the symbol rate of the transmitter equal to $\frac{1}{T}$ symbols/second. The data symbols are filtered by the baseband pulse shaping filter $b(t)$ and used to control the output frequency of a variable frequency oscillator (VFO) with a sensitivity of $\frac{h\pi}{T}$.

2.3.1) Properties of Minimum Shift Keying

In this section a number of properties of MSK will be reviewed and summarized in order to lay the foundation for a comparison with GMSK.

Figure 2.2: MSK Modulator

Given that the modulation index of MSK is 0.5, the maximum deviation from the carrier center frequency can be derived by evaluating $f(t)$ for this value of h :

$$f(t)_{h=0.5} = \frac{\pi}{2T} [\text{rad/sec}] = \frac{1}{4T} [\text{Hz}] \quad (2.5)$$

The frequency deviation from the carrier center frequency is therefore one quarter of the symbol rate (in Hz) for MSK. This leads to a maximum mark-space frequency difference, Δf , of

$$\Delta f = \frac{1}{2T} \quad (2.6)$$

i.e., one half of the symbol rate. Therefore we take note that the peak frequency deviation is a fixed proportion of the symbol rate for a given modulation index, although only the special case of $h=0.5$ has been cited above.

The next property to be examined is the excess phase of MSK. The excess phase produced by MSK modulation in one symbol interval is given by equation 2.7.

$$\phi(T) = \int_0^T f(\tau) d\tau \quad (2.7)$$

Using this equation and the expression for the baseband frequency modulating waveform (equation 2.3), we can evaluate the excess phase produced by MSK in one symbol interval can be evaluated :

$$\phi(T) = \int_0^T \frac{\pi}{2T} |I_n| b_n(\tau) d\tau = \pm \frac{\pi}{2T} \int_0^T 1 d\tau = \pm \frac{\pi}{2} \quad (2.8)$$

It can therefore be concluded that the excess phase produced during one symbol of an MSK modulated signal is $\pi/2$ radians of phase lead or lag depending on the symbol which

Figure 2.3 : Signal Constellation and Phase Trajectory of MSK

was sent. This is easily visualized by observing the signal constellation of a GMSK signal. Such a signal constellation and the associated phase trajectory is shown in figure 2.3.

It should also be observed from figure 2.3 that since the excess phase changes by $\pm \pi/2$ between each adjacent symbol, adjacent symbols are orthogonal in Hilbert space. A more physical interpretation of this is the observation that adjacent symbols are not sent on the same plane in two-dimensional space; if symbol n is sent on the Q-channel, then symbol $n+1$ is sent on the I-channel.

Further insight into this phenomenon can be gained by writing the representation of MSK in its complex components :

$$s(t) = \text{Re}(e^{j\omega_c t} e^{j(\varphi(t) + \varphi_o)}) = \cos(\varphi(t) + \varphi_o) * \cos(\omega_o t) - \sin(\varphi(t) + \varphi_o) * \sin(\omega_o t)$$

Which can be written as :

$$s(t) = s_I(t) * \cos(\omega_o t) + s_Q(t) * \sin(\omega_o t)$$

The baseband In-phase and Quadrature components of MSK can therefore be written as:

$$s_I(t) = \cos(\varphi(t) + \varphi_o)$$

and,

$$s_Q(t) = -\sin(\varphi(t) + \varphi_o)$$

If for simplicity, φ_o is set to zero, it can be shown that the expressions for the I and Q waveforms can be written as:

$$s_I(t) = \sum_n I_{2n} \cos\left(\frac{\pi t}{2T}\right) \quad \text{and} \quad s_Q(t) = \sum_n I_{2n+1} \sin\left(\frac{\pi t}{2T}\right)$$

where: I_{2n} represents the even-numbered bits of the sequence I_n
 I_{2n+1} represents the odd numbered bits of the sequence I_n

It is therefore observed that MSK may be viewed as a form of I-Q modulation wherein the bits are sinusoidally filtered and sent in alternation on the I and Q channels. Note that the duration of the alternating bits is $2T$ on each channel, thus retaining the overall bit rate of $1/T$. This form of alternately transmitting bits on the I and Q channels is commonly referred to as Offset-keyed Quadrature Phase Shift Keying (OKQPSK or OQPSK), of which MSK is a special case due to the sinusoidal filtering.

2.4) Gaussian Filtered Minimum Shift Keying

In the case of MSK, the modulation was shown to be a special case of CPFSK in which the frequency was keyed between $f_o + \frac{4}{T}$ and $f_o - \frac{4}{T}$. The change in frequency was instantaneous and the excess phase produced during each symbol interval was sufficient to ensure orthogonality in Hilbert space.

In an effort to increase the spectral efficiency of MSK, it has been suggested [14] that instead of performing instantaneous changes in frequency, the change in frequency should be performed in a continuous manner. The particular case to be examined here is that of using Gaussian filtering on the frequency keying signal in order to perform smoother frequency transitions, resulting in improved spectral efficiency.

In performing the Gaussian premodulation filtering on the signal, we replace the baseband filter, $b(t)$, that is used for MSK with a Gaussian filter, $g(t)$. The impulse response of the Gaussian filter is normalized in order to retain the property:

$$\int_{-\infty}^{+\infty} g(t) dt = T.$$

The instantaneous frequency of the Gaussian filtered MSK is given by

$$f(t) = \frac{1}{2T} \sum I_n g(t - nT)$$

and hence the modulation index, h , of $\frac{1}{2}$ is preserved.

By using the premodulation lowpass filter, the fixed frequency deviation and the fixed phase deviation per symbol of MSK are not necessarily maintained. If the pulse $g(t)$ is not limited to a duration of T , adjacent symbols will overlap resulting in inter-symbol interference. In order to more fully understand the underlying cause of the symbol overlap, the family of Gaussian pulses will be examined in further detail.

It has been shown [15] that the CPFSK form of the signal can not be rewritten in the OQPSK form of MSK.

2.4.1) Gaussian Lowpass Filters

Let us briefly examine the family of Gaussian pulse shapes used in CPFSK systems. The impulse response of a Gaussian lowpass filter is described as follows:

$$g(t) = \frac{1}{2} \left[\operatorname{erf} \left(\pi * B_b T * (t + 0.5) \sqrt{2/\log 2} \right) - \operatorname{erf} \left(\pi * B_b T * (t - 0.5) \sqrt{2/\log 2} \right) \right]$$

The parameter $B_b T$ is a normalized index of the duration of the pulse. By varying the $B_b T$ product, a family of Gaussian pulse shapes can be obtained. A representative family of

Figure 2.4(a) : Impulse Response of Gaussian Filters **Figure 2.4(b) : Frequency Response of Gaussian Filters** **Figure 2.4(c) : Power Spectrum of GMSK**

such pulses is shown in figure 2.4(a). As can be seen from the figure, when the B_bT product is decreased, the pulses tend to be longer in duration causing increasingly pronounced ISI. This can be readily observed by noting the [non-zero] value of $g(t)$ at $t/T = \pm 0.5$.

In order to illustrate the effect of the B_bT product on the spectrum of the baseband pulses, the spectrum of a family of Gaussian pulses is shown in figure 2.4(b). It can be observed from the figure that the power spectrum of the pulses rolls off more quickly as the B_bT product is decreased.

Figure 2.5(a) : Baseband Modulating Signal for 0.5 GMSK

Figure 2.5(b) : I and Q Representation of 0.5 GMSK

When such pulses are applied to a frequency modulator, the increased smoothness of the longer pulses causes the frequency and hence the phase of the modulated signal to change more slowly. This leads to a more compact frequency spectrum and hence improved spectral efficiency. The computed single sided power spectral density of the modulated signal for $B_bT = 0.5$ is illustrated in figure 2.4(c).

Although it is difficult to write an expression for GMSK in the complex I and Q form, it is relatively straightforward to generate one on a computer or in the laboratory. Figure 2.5(a) shows a baseband signal with $BT=0.5$; the associated baseband I and Q representation is shown in figure 2.5(b). As can be seen from the figure, the I and Q trajectories are dependent not only on the baseband modulating signal, but on each other. In other words, the state of I and Q at the k^{th} sampling instant will depend on the state of the baseband modulating waveform at the k^{th} sampling instant and on the state of I and Q at the $k-1^{\text{th}}$ sampling instant. A more general way to state this result is to say that this modulation scheme has "memory".

It can also be noted from the figure that with $B_bT = 0.5$, the I and Q "eyes" are fully open. The impact of this is that there is no premodulation filter induced ISI encountered in the I and Q modulation. For this reason, it is often suggested in the literature [4] that GMSK be coherently detected.

Differential and discriminator detection techniques will encounter premodulation filter induced ISI as can be seen from figure 2.5(a). In such cases the detected estimate of the transmitted symbol will be biased by the preceding symbol and the following symbol in the transmitted data stream.

2.5) Conclusions

In this chapter the salient features of minimum shift keying have been reviewed. The effect of performing Gaussian filtering on the symbol stream was then examined. It was shown that MSK produces an excess phase of $\frac{\pi}{2}$ and it was stated that by applying

Gaussian filtering to the baseband pulse stream to produce GMSK, the spectral occupancy of the modulated signal can be reduced. These properties have made GMSK a popular modulation scheme for emerging personal communication systems.

The next chapter will reveal a number of ways that the FM signal can be demodulated and the transmitted symbols can be detected.

Chapter 3:

Demodulation and Detection of Digital FM Signals

3.1) Introduction

This chapter provides an overview of techniques that can be used to demodulate and detect CPFSK signals. The focus will be mainly on digital techniques that are suitable for narrowband signals, since such signals are currently of much interest within the personal communications field. The discussion will further be restricted to non-coherent techniques since these do not require carrier recovery circuits. The issue of carrier recovery and its effect on the performance of the receiver system will therefore not be addressed here.

Techniques used in the previous art will be reviewed first. These techniques have been divided into three categories: (a) the matched tone filter technique, (b) direct conversion, and, (c) frequency discriminator techniques. It will be seen that the discriminator approach directly provides a measure of frequency deviation and has the advantage of straightforward simplicity. The technique which is the subject of the thesis, which is itself a discriminator approach, will then be described and shown to be of higher relevance than the previous discriminator approaches, particularly in a VLSI context.

Although all of the techniques of the previous art that are described herein are also capable of analog implementation, their digital counterparts will be highlighted in order to retain the overall digital receiver context of this thesis.

3.2) Matched Tone Filter Demodulator

This type of receiver uses a bank of filters that are matched to the frequencies of the corresponding symbol being transmitted. Such a receiver is illustrated in figure 3.1. Each tone filter in the receiver has at its output an envelope detector which produces an output which is proportional to the correlation between the received signal and the impulse response of the filter. A decision is made at the sampling instant by choosing the symbol that corresponds to the filter with the greatest output power.

Figure 3.1 : The Matched Tone Filter Demodulator

In order to digitally implement such a receiver, the intermediate frequency (IF) must be low enough to reliably perform Nyquist rate sampling on the bandpass FSK signal. The filtering can be performed in dedicated DSP hardware at the A/D sampling rate. The envelope detection can be performed at a lower sampling rate since the signal at the output of the filter will be bandlimited and can therefore be sub-sampled. In a 1-2 GHz microwave radio application this will typically require more than one IF stage to accommodate the low input frequency requirement of the A/D converter. The multiple IF stages each require filtering and gain to compensate for the filter insertion losses. In addition, the IF stages may require automatic gain control (AGC), depending on the dynamic range of the A/D converter.

If this receiver is to be implemented with only one IF stage, the nominal frequency selected will tend to be relatively high due to limitations in the image rejection of the filter preceding the first mixer. Techniques such as IF sub-sampling and bandpass A/D

conversion have been proposed to accommodate the use of a high IF, but these types of A/D converters will require proportionately more power to operate.

An additional requirement for this type of receiver is that the nominal frequency of the local oscillator will have to be precisely controlled in order for the signaling frequencies of the modulation to fall within the passband of the matched filters..

3.3) The Direct Conversion Receiver

In an attempt to alleviate the image frequency filtering problem and eliminate the need for any IF circuitry, the direct conversion receiver was proposed. This particular receiver eliminates these problems by mixing the RF signal immediately down to baseband in quadrature as shown in figure 3.2. In this manner, the bandpass filters of the previous receiver become lowpass filters.

Although the direct conversion receiver may appear attractive at first, it also has a number of limitations due to technological difficulties. First of all, most of the gain in the receiver must be at the RF frequency in order to overcome the flicker noise contributed by the mixers near dc. In order to attain the high RF gain required, more than one RF amplifier is usually used. This is done for several reasons, one reason is that the high gain required is not usually attainable from one stage at such high frequencies, and even if it can be accomplished, it is difficult to isolate the input of a given stage from the output sufficiently

Figure 3.2 : A Typical Direct Conversion Receiver

to avoid parasitic oscillations from occurring. By using multiple amplifier stages, the gain may be distributed among them and measures may be therefore taken to isolate each stage. This will help to avoid oscillation of the amplifier line-up due to coupling from the output to the input. The amplifier stages can also be individually designed in order to optimize a certain characteristic for each stage. For example, the emphasis in the first amplifier is usually placed on noise performance and in later stages it is usually placed on high dynamic range. Hence, the simultaneous requirement for high gain, low noise figure and a large dynamic at high frequencies tends to make the design of the front end quite difficult and relatively expensive.

These are several reasons why in normal practice the direct conversion receiver is not often used to convert directly from RF to DC in one stage. Instead, the receiver will usually contain an intermediate frequency (IF) strip, where most of the signal path gain is present. The intermediate frequency is chosen to obtain the maximum possible image rejection from the filter in the RF stage and for the low cost amplification available at the lower frequency of operation. Another benefit of using the IF strip is that although the gain requirement will remain about the same, the isolation inherent in providing portions of the gain at two different frequencies helps avoid parasitic oscillation.

Another difficult challenge in implementing a direct conversion receiver is that of balancing the gain and phase of the I and Q signal paths relative to each other. Such balancing requires that the two mixers have identical gain. In order to achieve the necessary phase balance requires that the LO signal is properly split into quadrature components. At RF frequencies this is difficult to do within very few degrees since passive quadrature hybrids are only matched to within about 5 degrees and the frequency of the LO is too high to employ any known digital technique except emitter coupled logic which requires an impractically large amount of power in mobile applications.

An additional point worthy of noting is that in the direct conversion receiver, the local oscillator (LO) input and the received signal (RF) input to each of the pair of quadrature

mixers will be at the same frequency. This places an additional requirement on the mixers that they be well balanced internally to eliminate any DC offsets due to self-mixing of the LO. The effect of DC offset at the output of the mixers is to bias the receiver decisions in a manner dependent on the polarity of the offset. This can be compensated for in a wideband FSK receiver by designing the FIR filters after the A/D converter to have transmission zeroes at DC to block the offset. If narrowband FSK is used, the zeroes in the filter response may degrade the receiver performance by causing amplitude distortion.

3.4) Frequency Discriminators

Another approach to the detection of FSK signals is that of passing the IF signal through a frequency discriminator which produces a digital measure of the deviation of the received signal from some nominal frequency. The nominal operating frequency of the discriminator is determined by design and is typically coincident with the center frequency of the IF stage. The signal from the output of the discriminator is then filtered, decimated and sampled at the symbol rate. A threshold detection is then performed in order to decide which symbol was most likely transmitted.

There are a number of frequency discriminator techniques devised that are suitable for digital implementation. A number of techniques including the one used in the present work are described in this section.

3.4.1) The Balanced Quadricorrelator

The balanced quadricorrelator (sometimes also referred to as the dual differentiator [16]) uses two differentiators in a balanced configuration. A typical implementation is shown in figure 3.3.

In order to analyze the operation of the quadricorrelator, recall that the instantaneous frequency of a signal is the time derivative of its phase. The phase can be written as :

$$\theta = \arctan\left(\frac{Q}{I}\right)$$

Figure 3.3 : The Balanced Quadricorrelator

and taking the derivative of this term it can be shown that :

$$\omega = \frac{IQ' - Q'I'}{I^2 + Q^2}$$

If the signal is hard limited prior to application to the quadricorrelator, the denominator term will be constant. Since the expression in the numerator is identical to the output of the quadricorrelator, it will therefore will be proportional to the frequency of the input signal.

The drawbacks of this type of frequency discriminator include the requirement for a low IF frequency if a low cost A/D convertor is to be used and complications arising from the design of the differentiators [16]. It should also be noted that the design of the multipliers can be simplified considerably if the A/D convertor samples the signal at four times the IF frequency [27].

3.4.2) The Arctangent Demodulator

Another frequency discriminator that is amenable to digital implementation is that of taking the arctangent of the I and Q channels of the signal to derive the phase and differentiating the phase to arrive at the frequency. A simplified configuration of the technique is shown in figure 3.4.

Figure 3.4 : The Arctangent Demodulator

As can be seen from the figure, a correction filter is typically required after the differentiator in order to compensate for discontinuities arising from phase transitions from $-\pi$ to $+\pi$ and vice-versa. The correction filter is simply an FIR transversal filter with the coefficients properly chosen to correct for the aforementioned phase transitions. The derivation of the coefficient values is outlined in the literature [16].

The main challenge in implementing such a discriminator in hardware lies in calculation of the arctangent, since the arctangent function is a relatively difficult mathematical operation to perform numerically. A typical solution is that of using the quantized I and Q signals to address a ROM [5]. The most significant N bits of I and Q can be used to address the memory locations within a ROM with 2N address bits. As the number of bits, N, is reduced, the distortion of the resulting demodulated signal will increase. In order to economize on the size of the ROM, quadrant expansion techniques which take advantage of the sign of the I & Q samples can be utilized. In this manner, the size of the ROM can be reduced by a factor of four, since this then requires that only one quadrant is stored in the ROM.

If the table look-up technique is to be used to implement the arctangent function, then the I and Q samples must be scaled. This can be performed in the IF stage by hard limiting the amplitude of the signal before doing the quantization and I-Q conversion. This ensures that the ROM will be appropriately addressed, independent of the received signal strength.

As in the case of the balanced quadricorrelator, a low IF frequency is required for economy in the A/D convertor and the Same economy in the multipliers can be realized by sampling at four times the IF frequency.

3.4.3) The Δ - Σ Frequency Discriminator

In order to realize high resolution A/D converters using technologically simple circuits, the technique of Δ - Σ modulation is frequently used [10]. The Δ - Σ D/A converter achieves high resolution through the combined use of over-sampling and noise shaping which moves the quantization noise spectrum away from the baseband where the signal of interest lies and into the higher frequency bands where it can subsequently be filtered out.

A variation on the Δ - Σ technique which allows the conversion of an analog frequency to a digital bitstream was recently proposed [1]. The technique permits a simple structure to be used to convert the frequency of an analog signal to a high resolution digital representation. The structure itself in its second order form is shown in figure 3.5. The advantage of this approach relative to the previously discussed discriminator techniques is that it permits, for a given resolution, a higher IF to be used while preserving the property of low power consumption. It can be argued that the techniques of the previous art were

Figure 3.5 : Second Order Δ - Σ Frequency Discriminator

fully digital and were therefore easier to implement, but such an argument is not justified since it was assumed that the signal had already been digitized when discussing them. Such a digitization implied the use of an A/D converter prior to the digital discriminator, and for the same (high) IF frequency such a converter would consume power in addition to that which was consumed by the discriminator circuits.

The salient details of the operation of the Δ - Σ frequency discriminator will be briefly reviewed here, following closely on the description provided by Beards [1].

The input IF signal to the frequency discriminator (f_m) is divided down by the dual modulus divider (DMD) by a factor of either N or $N+1$. The phase of the signal from the DMD is then compared to that of the reference signal (f_{ref}). If the phase of the divided-down IF signal leads the phase of the reference, a positive pulse will be emitted by the PFD, the duration of which is proportional to the amount of phase lead detected. If f_m lags in phase relative to the reference, then a negative pulse is emitted from the PFD with duration proportional to the phase lag. These pulses are used to steer a charge pump that produces I_{out1} which in turn adds or removes charge from a capacitor (C_1).

If the voltage across C_1 exceeds a certain threshold, implying that the phase of f_m is leading, it will cause the limiter (threshold detector) to switch which will in turn cause the DMD to divide by $N+1$. When the DMD divided by $N+1$ it will cause the divided-down IF signal phase to lag by one period of the IF signal, thus removing the phase lead from the IF signal and causing it to lag the reference signal. The lag caused by the $N+1$ divide ratio will cause the PFD to remove charge from C_1 until such time that the limiter is made to switch and force the divider modulus to N causing the divided-down IF signal to once again build up a phase lead relative to the reference.

The conversion from frequency to phase by the DMD/PFD circuits embodies the first integration in the loop. The second integration in the loop is performed by the charge pump which follows the PFD, thus resulting in a second order loop. The required inner

loop of the Δ - Σ modulator is performed with the charge pump that is controlled by the output of the quantizer. The inner loop charge pump produces a current I_{out2} which adds or removes charge from the capacitor C_1 .

3.5) An Example of a Δ - Σ Discriminator Based FM Receiver

In order to place the Δ - Σ discriminator in an application context, a brief example of a Δ - Σ discriminator based receiver is presented here.

A simple receiver employing the Δ - Σ discriminator is shown in figure 3.6(a). As can be seen from the figure, the discriminator accepts an IF signal which it demodulates and converts to a Δ - Σ bitstream. The Δ - Σ bitstream is then processed by a comb decimation

Figure 3.6(a) : A Simple Receiver Based on the Δ - Σ Discriminator

Figure 3.6(b) : Eye Diagram Obtained from the Receiver for 313.5 kHz GFSK

filter and two FIR filters that operate at the decimated rate. Although this receiver architecture is rudimentary, it demonstrates the concept of a Δ - Σ discriminator in a receiver application. The concept of this receiver was adapted from the one described in a recent paper [5] where an arctangent receiver was used. The original objective was to demonstrate that the Δ - Σ discriminator could be used instead.

This receiver was assembled and tested as a fourth year undergraduate project under the authors guidance [17]. It was put to work again for this thesis in order to partially demonstrate the functionality of a simple receiver based on the Δ - Σ frequency discriminator. The resulting eye diagram obtained for the receiver for an input with 313 kHz GFSK modulation is shown in figure 3.6(b). As can be seen, an adequate eye opening is obtained using simple filtering techniques. The simplicity of these filter techniques relies on decimation taking place in the comb filter. Decimation leads to some aliasing of higher frequency signals into the baseband, hence corrupting the desired baseband signal to some, albeit small, degree. Later in this thesis, more complex filtering strategies will be used to avoid decimation until after all of the filtering is completed in an effort to obtain superior results.

3.6) Conclusions

This chapter has presented a review of several receiver architectures and highlighted their salient characteristics. It was shown that none of the receiver architectures reviewed here can be considered optimum for all applications; it is important to choose the receiver architecture that best suits the application at hand.

A number of discriminator techniques were also reviewed in this chapter. Although all of the techniques were capable of providing a digital measure of frequency deviation (as required in an FM receiver), they were all relatively complex to implement (high parts count) and often relied on matched components for maximum performance. The Δ - Σ frequency discriminator was also reviewed and shown to be a simple component which is very suitable for VLSI implementation. Such a discriminator implementation requires a

great deal of skill at the design and physical layout stage, but can then be cheaply and consistently reproduced in very large production quantities. The VLSI fabrication process inherently provides the required component matching and the simplicity of the circuit keeps the cost down since it does not require a lot of area on silicon. A fully integrated version of the Δ - Σ discriminator relieves the radio system designer of the burden of matching analog components or compensating for these mismatches using DSP techniques. The low cost of the Δ - Σ discriminator, its high frequency of operation and its potential to provide high resolution make it suitable for a wide variety of applications.

At the time of this thesis, an appropriate fully integrated version of the discriminator was not available, so as a proof of concept a printed circuit board implementation of the discriminator was used instead.

Chapter 4:

Adaptive Filtering of Δ - Σ Converted Signals

4.0) Introduction

In this chapter the use of adaptive filtering techniques to process Δ - Σ converted signals in the context of digital communication receivers is examined. The particular emphasis is on filtering bitstreams derived from the Δ - Σ frequency discriminator although the techniques can be used for ordinary Δ - Σ converted signals. Finally the application of adaptive filtering techniques to a Δ - Σ discriminator based receiver is proposed for the design of fixed filters or variable coefficient filters to process the bitstream from the discriminator. The overview is limited to presenting the algorithms in their most basic and useful form. The detailed derivations of the various algorithms are referenced for the interested reader.

4.1) Detection of the Transmitted Symbols

Subsequent to obtaining a digital measure of frequency deviation, it is necessary that the demodulated signal be used in some way to arrive at a decision as to which symbol was most likely transmitted. Such a decision may be made on a symbol-by-symbol basis, where each symbol is detected separately, or a decision may be made over several symbols, where the objective is then to decide which particular sequence of symbols was sent. In this work, the former approach is used to arrive at the estimate of the transmitted symbol.

In the current work, the objective is to detect digital symbols that have been transmitted as GMSK with $B_bT=0.5$. The digital representation of the transmitted signal from the Δ - Σ

Figure 4.1 : A Typical Discriminator Receiver

frequency discriminator will include shaped (non-white) quantization noise, thermal noise and ISI due to the Gaussian premodulation lowpass filter. The predetection filter will therefore have to cope with all of these impairments in a manner that will achieve an acceptable bit error rate (BER). An acceptable BER will be assumed to mean 10^{-3} since this is the value prescribed in the European Telecommunication Standards Institute (ETSI) specification for the Digital European Cordless Telephone (DECT) standard [18].

A common approach to symbol detection as used in a frequency discriminator receiver is illustrated in figure 4.1. As can be seen from the figure, the discriminator output is typically processed by a compromise matched filter before hard decisions are made as to the most likely value of the transmitted symbol $d(k)$. The matched filter is used in an attempt to maximize the signal to noise ratio (SNR) at the output of the filter $y(k)$.

The transfer function of a matched filter is given by :

$$C_{opt} = \frac{S_{xx}(f)}{S_{NN}(f)} \quad (4.1)$$

Where $S_{xx}(f)$ is the power spectral density of the desired signal and $S_{NN}(f)$ is the power spectral density of the additive noise. Such a filter is optimum in a maximum SNR sense if the duration of the received pulse is confined to one symbol interval. This filter may not provide adequate performance if the objective is to estimate the value of a symbol that is part of a sequence of transmitted pulses that overlap. The impulse response of the optimum matched filter will then depend on the value of all of the symbols that partially overlap with the current symbol.

If instead of maximizing the SNR at the output of the system, the objective is to minimize the error between the output of the receiver system and the original transmitted signal, an error function can be defined as :

$$\varepsilon(k) = d(k) - y(k) \quad (4.2)$$

The optimum filter can then be chosen to minimize the mean square value of this error (MSE) function. To this end, the mean square error function is defined as :

$$MSE = E[\varepsilon^2(k)] = E[\{d(k) - Y(k)\}^2] \quad (4.3)$$

The optimum filter function in a MSE sense in the presence of noise with power spectral density $S_{NN}(f)$ is given by :

$$C_{opt}(f) = \frac{S_{xx}(f)}{S_{xx}(f) + S_{NN}(f)} \quad (4.4)$$

The filter that minimizes the error in a mean squared sense is known as the optimum Wiener filter [19].

The above solution assumes that the statistics of the signal and noise are stationary; that is to say that $S_{xx}(f)$ and $S_{NN}(f)$ are not functions of time. In the event that the statistics of the signal and the noise are non-stationary, the time variations can be explicitly shown by writing equation (4.4) as :

$$C_{opt}(f) = \frac{S_{xx}(f,t)}{S_{xx}(f,t) + S_{NN}(f,t)} \quad (4.5)$$

In the present work, it is assumed that the statistics of the signal are cyclostationary since the signal consists of a sequence of symbols transmitted at the symbol rate f_s . The noise

Figure 4.2 : Receiver Incorporating Adaptive Filtering

will not be assumed to be stationary and hence will require either a time variation of the filter characteristics in order to maintain optimality or a time averaged solution.

Therefore two uses of adaptive filtering algorithms can be proposed :

- 1) To arrive at a compromise fixed filter by applying adaptive filtering algorithms to a simulated bitstream and incorporating the resulting filter response into digital filter with a fixed response
- 2) To adjust the response of a variable filter in real time while the receiver is receiving signals in an actual operating environment.

The first approach will result in a filter response that minimizes the error at the output of the digital filter for some fixed input conditions. This approach can be used to arrive at a filter response that could not be easily obtained using closed form expressions such as equation (4.4). Arriving at filter responses using closed form expressions is difficult when the spectral density of the noise is difficult to describe as is the case with Δ - Σ modulated bitstreams.

In order to implement the second approach, and hence address the time variations on the statistics of the noise in real time, there must be a way of changing the impulse response of

the filter in sympathy with the variations in the signal to noise ratio. Under conditions of high SNR, most of the error will be due to ISI and hence the filter will attempt to minimize ISI. Under conditions of low SNR, the adaptive filter will attempt to minimize the noise variance at its output. The filter should therefore be able to adapt to the variations in the signal to noise ratio at the input to the discriminator.

Therefore, if the filter can change in time to accommodate changes in the characteristics of the input signal, it may therefore be assumed that the baseband subsystem of the receiver will take the form shown in figure 4.2. This receiver structure shows a proposed baseband architecture that alleviates some of the limitations of a compromise filter alone.

With this baseband signal processing approach, it is possible to simultaneously filter quantization noise and thermal noise and to eliminate ISI. Furthermore, by exploiting the capability of the filter to adapt to the statistics of the received signal, it is possible for the statistics to be changing in time while retaining optimality, provided that the filter can track the changes quickly enough. The hardware to implement such a filter system will be very complicated though and will typically require a full custom VLSI implementation.

4.2) Adaptive Filtering Techniques

In this section, two techniques for optimizing the coefficients of a digital finite impulse response (FIR) filter will be reviewed: the least mean-squares (LMS) algorithm and the recursive least squares (RLS) algorithm. The two techniques will be reviewed separately and then will be compared in terms of tracking performance, complexity, stability and overall relevance in the context of this work.

As an introduction to the problem of determining the optimum tap weights for a digital FIR filter, the "normal equations" will be briefly reviewed in this section. For a more thorough review the interested reader is referred to [20], [21].

Figure 4.3 : Digital Finite Impulse Response Filter

As can be seen from figure 4.3, the filter accepts input samples $x(k)$ and stores the n most recent samples in a shift register of length n . In order for the filter to form an output result it scales the n samples according to their respective tap weights and sums the individual weighted samples to produce the output $y(k)$. Therefore the output of the filter can be expressed as:

$$y(k) = \sum_{l=0}^{N-1} x(k-l)c(l) \quad (4.6)$$

alternatively, it can be expressed in vector form as :

$$y(k) = \mathbf{W}'\mathbf{X}(k) \quad (4.7)$$

where the information vector $\mathbf{X}$ is described by :

$$\mathbf{X}(k) = [x(k) \ x(k-1) \ x(k-2) \ \dots \ x(k-N+1)]' \quad (4.8)$$

and the tap weight vector $\mathbf{C}$ is described by :

$$\mathbf{C}' = [c_0 \ c_1 \ c_2 \ \dots \ c_{N-1}] \quad (4.9)$$

The index k refers to the k^{th} input sample and N refers to the duration of the impulse response.

It can be shown [21] that the optimum tap weight vector is given by:

$$\mathbf{C}_{ss}^o = \mathbf{R}_{ss}^{-1} \mathbf{P}_{ss} \quad (4.10)$$

where $\mathbf{R}_{ss}$, the autocorrelation matrix, is described by :

$$\mathbf{R}_{ss} = \sum_{k=N-1}^{L-1} \mathbf{X}(k) \mathbf{X}'(k) \quad (4.11)$$

and $\mathbf{P}_{ss}$, the cross correlation vector is described by :

$$\mathbf{P}_{ss} = \sum_{k=N-1}^{L-1} \mathbf{X}(k) d(k) \quad (4.11)$$

Although the optimum tap weight coefficients may be determined directly by inverting $\mathbf{R}_{ss}$ and multiplying by $\mathbf{P}_{ss}$, in practice $\mathbf{C}_{ss}^o$ is usually computed using other methods [21] including those described in the following two sections.

4.2.1) The Least Mean-Squares Algorithm

The Least Mean Squares (LMS) algorithm is a search technique that incorporates an approximation to the gradient of the error surface in order to minimize the mean square error function. The minimization of the error function is performed by adjusting the tap weight coefficient vector as the search progresses.

The gradient of the instantaneous squared error $G(k)$ with respect to the tap weight vector $\mathbf{C}(k)$ can be estimated directly from the input sample vector $\mathbf{X}(k)$ and the desired output d as follows :

$$\mathbf{G}(k) = \nabla_{\mathbf{C}}[e^2(k)] = 2e(k) \bullet \nabla_{\mathbf{C}}e(k) \quad (4.12)$$

$$= 2e(k)\nabla_C[d(k) - C'X(k)] \quad (4.13)$$

$$= -2e(k)\{\nabla_C[d(k)] - \nabla_C[C'X(k)]\} \quad (4.14)$$

By noting that $d(k)$ and $X(k)$ are independent of $C(k)$, the expression for $G(k)$ may be simplified as follows :

$$G(k) = -2e(k)X(k) \quad (4.15)$$

Using the instantaneous gradient, an algorithm can be developed which approximates a true gradient search. The resulting algorithm is known as the Least Mean Squares (LMS) algorithm. The update formula for the LMS algorithm is summarized below :

$$C(k+1) = C(k) - \mu G(k) \quad (4.16)$$

$$= C(k) + \mu e(k)X(k) \quad (4.17)$$

Figure 4.4 : LMS Adaptive Filter

The above technique provides a simple method to update the tap coefficients. The overall procedure for the LMS algorithm is as follows ;

i) Compute the filter output :

$$y(k) = C'(k)X(k) \quad (4.18)$$

ii) Determine the error :

$$e(k) = d(k) - y(k) \quad (4.19)$$

iii) Update the tap weight vector :

$$C(k+1) = C(k) + \mu e(k)X(k) \quad (4.20)$$

The LMS algorithm is therefore seen to be relatively simple to implement. This is evident from the block diagram of an adaptive filter incorporating the LMS algorithm which is shown in figure 4.4. This ease of implementation accounts for its widespread use. The other main advantage of LMS is its numerical stability that allows the computations to be carried with only modest arithmetic precision and still approach a valid solution for the tap coefficient vector.

The main problem with the LMS algorithm is slow convergence. The speed of convergence must be traded off against the minimum squared error attained. These properties are controlled by the step size μ . As the step size is increased, the rate of convergence is increased but the minimum error attained in steady state is larger than that which could have been attained with a smaller step size. Also, as the step size is increased beyond a certain point, the algorithm may become unstable.

4.2.1.1) LMS Based Filters with Decision Feedback

The performance of a linear LMS based filter may be enhanced in some cases with the addition of a decision feedback section, often referred to as a decision feedback equalizer (DFE) in the literature. When the two filter sections are combined, the linear filter is referred to as the "feedforward" filter. The decision feedback section takes previous

Figure 4.5 : LMS Adaptive Filter with Decision Feedback Section

decisions, $d(k)$, and uses them as input samples to a filter section, the output of which is added to the output of the feed forward filter section. This concept is illustrated in figure 4.5. The decision is then made based on the sum of the two filter section outputs. The DFE accepts input samples at the symbol rate. The tap weight updates to both filters must therefore be performed at the symbol rate when a DFE is used.

The decision feedback section eliminates any ISI from previous symbols which tends to bias the current decision. This will tend to reduce the amount of steady-state error after the filter converges. The DFE also tends to speed the rate of convergence since it reduces the ISI very quickly with just a few taps. If the feedforward filter alone was used to reduce ISI, it would require the adjustment of many taps, hence slowing the convergence of the filter. The DFE reduces ISI by predicting the amount of ISI using previously detected symbols to produce a contribution to the summer at the output of the feedforward filter that cancels the ISI. The major caveat that must be observed when using a DFE is that when a symbol is detected incorrectly it causes the DFE to produce a signal which enhances ISI instead of canceling it. This may cause rapid deterioration in the bit error rate once a single bit error is made until such time as the signal quality

improves. The reason why a DFE is still desirable in light of this problem is that the DFE lowers the signal-to-noise ratio (SNR) threshold at which a given level of BER occurs.

The mathematics describing the operation of the DFE are quite involved and beyond the scope of this work. The interested reader is referred to the book by Proakis [24] and the many references contained in that book.

4.2.2) The Recursive Least Squares Algorithm

The Recursive Least Squares (RLS) algorithm is a computationally efficient technique used to directly solve the normal equations and hence to arrive at the tap weight coefficient vector that minimizes the least square error. The efficiency of the RLS algorithm derives from avoiding the inversion of the autocorrelation matrix R_k . Instead of updating and inverting the autocorrelation matrix, the inverse of the autocorrelation matrix is updated and used directly. As will be shown, the autocorrelation matrix (or, its inverse) do not need to be known initially when the algorithm is started; a simple initial value can be used and the actual matrix can be built at each step as the algorithm is repeated.

In order to arrive at a computationally efficient way to solve the normal equations, a way to avoid inverting the autocorrelation matrix is required. To this end, the "ABCD lemma" for matrices is invoked :

$$(A + BCD)^{-1} = A^{-1} - A^{-1}B(DA^{-1}BC^{-1})^{-1}DA^{-1} \quad (4.21)$$

where A, B, C and D are equated as follows :

$$A = R_k \quad (4.22)$$

$$B = X(k) \quad (4.23)$$

$$C = 1 \quad (4.24)$$

$$D = X'(k) \quad (4.25)$$

Since the update formula for R_k is as follows :

$$R_k = R_{k-1} + X(k)X'(k) \quad (4.26)$$

Using the lemma, an update formula for R_k^{-1} may be written as :

$$R_{k+1}^{-1} = R_k^{-1} - \frac{R_k^{-1} X(k) X'(k) R_k^{-1}}{1 + X'(k) R_k^{-1} X(k)} \quad (4.27)$$

It can therefore be seen that with this approach it is not ever necessary to determine or invert R_k . Instead, equation (4.27) is used to update R_{k+1}^{-1} directly using R_k^{-1} and the $k+1^{\text{th}}$ input sample vector. With R_{k+1}^{-1} available at all times, the matrix inversion never has to be performed. This of course assumes that some value for R_k^{-1} exists when the update process is started. Since R_k^{-1} may not be known when the process is started, it is possible to use an initial value of R_k^{-1} of the form:

$$R_{\text{initial}}^{-1} = kI_N \quad (4.28)$$

where k is a large positive scalar constant and I_N is an $N \times N$ identity matrix.

A further enhancement to the RLS algorithm can be made by introducing exponential data weighting. The weighting is introduced by modifying the definitions of R_k and P_k as follows :

$$R_k = \sum_{l=N-1}^{k-1} \rho^{k-l-1} X(l)X'(l) \quad (4.29)$$

$$P_k = \sum_{l=N-1}^{k-1} \rho^{k-l-1} X(l)d(l) \quad (4.30)$$

In effect, the exponential data weighting emphasizes the most recent input data when calculating the moments of the signal, thereby assisting the algorithm in tracking non-stationary signals since the most recent data more closely reflects the current statistics of the signal. By diminishing the effect of older data the algorithm can also readily correct

for past singularities in the auto correlation matrix such as when the matrix is initialized as described by equation (4.28). For these reasons, the weighting factor, ρ , is sometimes also referred to as the "forgetting" factor.

The weighting factor, ρ , is a positive constant with value close to unity. As the value of ρ approaches unity the memory of the algorithm approaches infinity. An effective time constant or averaging period for the algorithm is defined by $1/(1-\rho)$.

The RLS algorithm may now be summarized as the following step-by step procedure :

i) Compute the apriori output $y(k)$

$$y(k) = \mathbf{C}_k^o \mathbf{X}(k) \quad (4.31)$$

ii) Compute the error $e_o(k)$

$$e_o(k) = d(k) - y(k) \quad (4.32)$$

iii) Compute the filtered information vector $\mathbf{Z}_k$:

$$\mathbf{Z}_k = \mathbf{R}_k^{-1} \mathbf{X}(k) \quad (4.33)$$

iv) Compute the normalized error power, q :

$$q = \mathbf{X}^t(k) \mathbf{Z}_k \quad (4.34)$$

v) Update the tap weight vector, $\mathbf{C}$:

$$\mathbf{C}_{k+1}^o = \mathbf{C}_k^o + \frac{e_o(k) \mathbf{Z}(k)}{\rho + q} \quad (4.35)$$

vi) Update $\mathbf{R}_k^{-1}$:

$$R_{k+1}^{-1} = \frac{1}{\rho} \left[R_k^{-1} + \frac{z_k z_k^T}{\rho + q} \right] \quad (4.36)$$

This step-by-step procedure was implemented in a Matlab script in order to perform the simulations presented in chapter 5.

4.2.3) Relevance of the Two Algorithms

The LMS algorithm requires on the order of N multiplications per iteration where N is the number of taps in the filter. The RLS algorithm requires on the order of N^2 calculations per iteration. It can therefore be concluded that the RLS algorithm is N times more computationally intensive than the LMS algorithm. Furthermore, if the LMS algorithm is used and μ is selected to be a power of 2, the multiplications may be implemented by shifting the bits in the error signal $\log_2 \mu$ to the right thereby eliminating any multiplications. One may therefore ask why one would use the RLS algorithm when it is so much more computationally expensive.

In order to answer this question, the approach used by Treichler [21] will be presented here. The RLS algorithm can be described in terms of the LMS algorithm by defining an accelerated LMS algorithm. The updates for the accelerated LMS algorithms proceed as follows :

$$C(k+1) = C(k) + \mu e(k) A_k X(k) \quad (4.37)$$

The A_k term is a matrix that will steer the coefficient vector toward the optimum solution based on the information vector $X(k)$.

In order to make this update equation equal to the RLS update equation, the following equivalences are made :

$$\mu = \frac{1}{1+q} \quad (4.38)$$

$$A = R_k^{-1} \quad (4.39)$$

Where q and R_k^{-1} are defined by equations (4.34) and (4.36), respectively.

The RLS algorithm may therefore be viewed as an LMS algorithm with superior tap weight updates. The updates performed by the RLS algorithm provide the correct direction and the right step size required to reach the optimum solution. This implies that the RLS algorithm determines the point on the error surface that will provide the optimum solution for a given error signal $e(k)$ and input vector $X(k)$. The LMS algorithm on the other hand merely follows the path of steepest descent for a given error signal $e(k)$ and input vector $X(k)$ which may not necessarily steer the tap weight vector toward the optimum solution during a given step.

4.3) Conclusion

The techniques described in this chapter allow the optimization of a filter function to be performed starting from some initial estimate of what a useful filter function may be. The final filter function arrived at once these algorithms converge is a filter function that will minimize some measure of error between the output of the filter and the desired filter output.

In the next chapter these techniques will be applied through simulation techniques to filter signals from a Δ - Σ modulator that represents a Δ - Σ frequency discriminator. The steady state error achieved with both the LMS and the RLS algorithms is shown and the utility of the two techniques in a digital receiver is discussed.

Chapter 5 :

Simulation Results

5.1) Introduction

Previous chapters have looked at Gaussian filtered FM, the operation of the Δ - Σ frequency discriminator and adaptive filtering algorithms. In this chapter, all three of these elements are combined in order to perform a number of simulation exercises. The simulation exercises were performed firstly in order to model the Δ - Σ frequency discriminator. Secondly, the bitstreams obtained from the discriminator model with a Gaussian filtered signal at its input are used to examine the behavior of adaptive filters when processing Δ - Σ modulated bit streams. Both least mean-squares (LMS) and recursive least-squares (RLS) algorithms are simulated.

In the context of radio applications, a digital receiver incorporating an LMS based filter with a decision-feedback equalizer (DFE) is simulated. The filter processes a bitstream that is derived from a cascade of a frequency discriminator and a Δ - Σ modulator. The objective of this particular exercise is to determine if some improvement in BER performance is attainable by performing adaptive filtering after the frequency discriminator.

5.2) The Δ - Σ Discriminator Model

The Δ - Σ discriminator is modeled as a frequency to bits converter that accepts an analog frequency variable at its input and converts the analog representation to a 1-bit digital representation, while also applying noise shaping to the bitstream. The noise shaping is used to change frequency distribution of the quantization noise such that the quantization

Figure 5.1 : Simulation Model of Δ - Σ Frequency Discriminator

noise is redistributed from the low frequency part of the spectrum to higher frequencies. Since the signal of interest is a lowpass signal, this technique allows a higher resolution output to be obtained after the output of the Δ - Σ converter is filtered since there will be very little quantization noise within the bandwidth of the desired signal. A block diagram of the Δ - Σ discriminator simulation model is shown in figure 5.1. This model is consistent with the analysis performed by Beards [1].

The input signals applied to the simulation model of the discriminator had to be scaled such that the ratio of the frequency deviation of the input signal to the maximum allowable frequency deviation of the board-level discriminator was maintained. This was done so as to emulate, as accurately as possible, the performance of the board-level discriminator to be used in the hardware exercise. For example, consider a discriminator with a 10 MHz clock frequency and a dual modulus divider (DMD) having divide ratios of $N/N+\delta$. The symbol delta (δ) represents a fraction of the 10 MHz clock, and thus defines the maximum allowable input range of the discriminator. The maximum peak-to-peak frequency deviation at the input of a discriminator with a 10 MHz clock will therefore be equal to $10 \cdot \delta$ MHz. Thus, for $\delta=1$, the maximum peak-to-peak frequency deviation would be 10 MHz. For $\delta=0.5$, the maximum would be 5 MHz. Although the maximum values have been established here, it is important to remember that in practice, one can only use approximately half of the maximum input range and still obtain good noise shaping and hence adequate baseband signal to noise ratio at the output.

The next important consideration is that the discriminator model has an input range of ± 1 , therefore requiring that the input frequency signal be scaled or normalized with respect to $\delta \cdot f_{ref}$. An example of the frequency scaling is provided here for the case of tone modulation with a peak-to-peak deviation of 200 kHz and a discriminator circuit with a reference clock frequency, f_{ref} , of 10 MHz and a frequency resolution of $\delta=1$. For this case the discriminator will provide a total input range of 10 MHz. In this case the ratio of the total peak-to-peak frequency deviation to the maximum discriminator input range will then be equal to :

$$f'_{in}(k) = \frac{f_m(k)}{10,000,000Hz}$$

where :

$f_m(k)$ is the desired input frequency in the discrete time variable, k

$f'_{in}(k)$ is the normalized version of $f_m(k)$

The simulation model of the discriminator was implemented in the Matlab simulator and was run for various input frequency patterns. As an example, the results of simulating the discriminator with an input frequency pattern representing sinusoidal modulation with a modulating frequency of 100 kHz and a peak deviation of 200 kHz deviation are shown in figure 5.2. This simulation is useful in that it allows one to observe the noise shaping behavior of the Δ - Σ discriminator, particularly in the baseband since the tone modulation does not obscure the shape of the quantization noise spectrum as would a broadband modulation.

The entire frequency spectrum of the simulation results are shown in figure 5.2(a). It can be seen that the quantization noise spectral density rises with increasing frequency. The quantization noise at low frequencies is of particular importance if baseband signal are to be resolved. As can readily be observed in figure 5.2(b) the input tone is approximately 35 dB above the quantization noise at 100 kHz. If the low frequency noise spectral density of the discriminator is low enough, then the baseband signals can be digitized to high degree

Figure 5.2(a) : Simulated Power Spectrum of Discriminator Output with 100 kHz Sinusoidal FM at the Input

Figure 5.2(b) : Zoomed-In View of Simulated Discriminator Output Spectrum with 100kHz Sinusoidal FM at the Input

of resolution. These simulated results will be compared to the measured results from the hardware discriminator which will be presented in chapter 6.

The next simulations were performed with Gaussian Filtered Frequency Shift Keying (GFSK) signal at the input of the discriminator. The GFSK modulation used had a normalized bandwidth of $B_b T = 0.5$. The results of these simulations for modulation indices

Figure 5.3(a-d) : Power Spectral Density of the Noise-Free Input Signal and the Output Bitstream for Various Modulation Indices

of $h = 8, 4, 2, 1$ are shown in figure 5.3(a-d), respectively. In these figures the dashed line represents the spectrum of the baseband Gaussian filtered modulation and the solid line represents the total spectrum of the modulation and the noise added by discriminator

model. It can be observed from the composite spectrum that the frequency of the intersection between the spectrum of the signal and the spectrum of the quantization noise occurs at a lower frequency as the modulation index is decreased. For modulation indices of 0.5, the signal could not be adequately discerned when modeling the discriminator for $\delta=1$. This is due to the fact that the amplitude of the desired signal at the output of the discriminator decreases by 6 dB each time the modulation index is halved. Therefore it is desirable to use a high modulation index or a smaller δ when possible. Within the framework of current digital personal communication receiver specifications (such as DECT) values of $h=1/2$ are typically used so it is more useful to reduce δ to some smaller value.

5.3) Simulation of a Baseband System

The first system to be simulated was a baseband system consisting of a pseudo-random bit stream (PRBS) generator, a Gaussian pulse shaper, a Δ - Σ frequency discriminator and an adaptive filter. A block diagram of the system that was simulated is illustrated in figure 5.4. This simulation was used to verify the operation and convergence of the adaptive algorithm when presented with the input signal and the quantization noise only; simulation of the system in the presence of thermal noise is discussed later in this chapter. The simulations of the baseband system were performed in order to compare the LMS and

Figure 5.4 : Baseband System with Sample Rate Filter Updates

RLS algorithms when designing a fixed filter to process the Δ - Σ noise shaped bitstream in a receiver.

5.3.1) Baseband System with LMS Filter Adaptation

The first simulation of the baseband system that was performed used a pseudo-random bit sequence generator and a Gaussian pulse shaper as the transmitter. The receiver was simulated using the Δ - Σ discriminator model and an adaptive filter that incorporated the LMS algorithm. The tap weights of the filter were updated once for each output sample of the discriminator. In order to form the error signal, the output of the adaptive filter was compared to the output of the Gaussian pulse shaper. In this manner the objective of the filter adaptation was to reduce the mean-squared error introduced by the quantization noise for every input sample. The oversampling rates were varied in order to assess the impact of the oversampling rate on the filter convergence.

The effect on filter convergence for over sampling ratios of 32, 64 and 128 for a step size of $\mu=0.001$ are illustrated in figure 5.5. It can be observed from the figure that as the oversampling ratio is increased, the time required for the filter to converge to steady state also increases. In addition to this, the initial error is larger for the higher oversampling rates. The longer convergence time observed for larger oversampling ratios can be explained by the fact that the impulse response of the adaptive filter spanned 3 symbol intervals for each case, regardless of the oversampling ratio. Therefore the impulse responses for oversampling rates of 32, 64, 128 spanned 96, 192 and 384, sample periods, respectively. The larger number of tap weights associated with the longer impulse responses resulted in larger solution spaces which for the same step size took a longer time for the LMS algorithm to find the minimum error. The larger initial error is due to the fact that the initial error was the sum of the contribution of each of the taps and hence for a larger number of taps the initial error tended to be greater.

The final residual error achievable when varying the length of the adaptive filter through the value of the oversampling ratio is a trade-off. With a smaller oversampling ratio and

(a) Error vs Iteration with N=32

(b) Error versus Iteration with N=64

(c) Error versus Iteration with N=128

Figure 5.5 (a-c) : Error versus Iteration Results of LMS Based Filter Simulations

hence fewer taps, the quantization noise in the baseband is greater and hence the filter requires a sharper roll-off. These are contradicting requirements since sharp filter roll-offs require more taps. If the oversampling ratio is increased, the amount of quantization noise in the baseband is less, somewhat easing the amount of cut-off required from the filter. The number of taps can become excessive though, leading to uncoupled modes [21] that cause the tap coefficients to oscillate about some steady state value. This pattern of this oscillation is a function of the input data and will contribute to the error at the output of the filter. In the worst case scenario, a filter that has too many taps, it will tend not to converge at all and thus render the system useless.

5.3.2) Baseband System with RLS Filter Adaptation

The same baseband system simulated in the previous section was resimulated using the RLS algorithm for filter adaptation. The intent was to determine if the additional computation demanded by the RLS algorithm was warranted by any improvements in rate of convergence and residual error. Even if the RLS algorithm could not be directly implemented in a low-cost receiver handset, it could be used to design a digital filter with fixed tap coefficients that could be used in conjunction with a Δ - Σ discriminator. The fixed filter obtained in this manner could be used to filter the quantization noise of the discriminator in a manner that allows accurate reproduction of the baseband pulse stream.

To this end, filter convergence was examined for oversampling rates of $N=32, 64, 128$. The results are plotted in figures 5.6, 5.7 and 5.8. As can be seen from the figures, the RLS algorithm converges much more quickly than the LMS algorithm and achieves a significantly smaller residual error. This is readily evident when comparing to the results in figure 5.5 where it can be seen that the LMS algorithm took on the order of 10^4 iterations to converge to a final steady state error whereas the RLS algorithm took less than 500 iterations for all three oversampling ratios simulated. Figures 5.6-8(b) show that the residual error obtained using RLS was of the order 10^{-3} which is much smaller than obtainable using LMS.

(a) Error versus Iteration **(b) Zoomed-In View of Steady-State Error** **(c) Final Tap Weight Vector Impulse Response****Figure 5.6 (a-c) : Results of RLS Based Filter Adaptation Process for $N=32$**

(a) Error versus Iteration

(b) Zoomed-In View of Steady-State Error

(c) Final Values of Tap Weight Vector Impulse Response

5.7 (a-c) : Results of RLS Based Filter Adaptation Process for $N=64$

(a) Error versus Iteration

(b) Zoomed-In View of Steady-State Error

(c) Final Values of Tap Weight Vector Impulse Response

5.8 (a-c) : Results of RLS Based Filter Adaptation Process for N=128

Due to the complexity of the RLS algorithm these simulations took several times longer to simulate than did the simulations using the LMS algorithm even though fewer iterations of the RLS algorithm were performed. The extra computation paid off though as the final residual error reached with the RLS algorithm was much smaller than that which was obtained with the LMS algorithm. This points to the usefulness of using the RLS algorithm to design fixed filters for applications such as this one where the input to the filter is corrupted by noise with a power spectral density that is colored.

The final impulse response values are shown in figures 5.6-8(c). In each case the impulse response attained was shaped similar to a sinc function, which indicates that the filters tended to have sharp roll-offs. The impulse response attained for $N=64$ will be implemented in hardware and used to process actual bitstreams from the hardware discriminator. The corresponding frequency response of the filter to be used is shown in figure 5.9. The details on the hardware and the results obtained using these filter coefficients to process a real bitstream will be discussed in chapter 6.

Figure 5.9 : Frequency Response of Filter with Coefficients as Shown in Figure 5.7(c), ($N = 64$).

Figure 5.10 : Simulation Model for Discriminator Based Radio System Including the Effects of Additive Noise and IF Filtering

5.4) Simulation of the Receiver in the Presence of Thermal Noise

In order to examine the behavior of the adaptive filter in the context of a discriminator based radio back-end, a simulation model of a system including a signal source, a noise source, a bandpass filter and a frequency discriminator model was compiled and run. A block diagram of the system is shown in figure 5.10.

As can be seen from figure 5.10, the baseband Gaussian pulse stream representing the amount of frequency deviation is converted to an In-phase and Quadrature representation (I&Q) by the f2iq block. The f2iq block takes the baseband pulse stream and converts it to a complex phase representation. In this manner the thermal noise can be added directly to the I and Q channel; adding the noise directly to the frequency representation while preserving the desired statistics of the noise would have been far more complicated.

With the noise added, the I and Q signals are filtered by identical bandpass filters. The bandpass filters are centered at dc and have a bandwidth that is specified when the simulation is run. The I and Q signals are then converted back to a frequency representation by the iq2f block. The frequency representation of the signal is then applied to the Δ - Σ discriminator model where it is converted to a noise shaped bitstream.

In the case of a real radio with an adaptive filter in the receiver, the receiver may have no knowledge of what symbol was sent. There the filter updates must be made based on hard decisions made at the receiver. Thus, the adaptive filter used in this section will use a decision directed filter updating scheme where the multi-bit output of the filter, $y(k)$, will be compared to the decision $d(k)$ made at the output of the limiter. This is illustrated in figure 5.11 which shows that the bits from the discriminator are first processed in the feedforward filter after which the output of the decision feedback filter is subtracted to form the decision variable $y(k)$. The value of $y(k)$ is passed onto a limiter which makes a one bit decision $d(k)$ as to what the value of the received symbol is, either +1 or -1. The value of $y(k)$ is then subtracted from the decision $d(k)$ to form the error $e(k)$ which is used to update the filter taps via the LMS algorithm as discussed in Chapter 4. The operating assumption here is that most of the decisions made using the initial filter tap coefficients are correct before the adaptation process begins. Then, as the adaptation process progresses, the number of errors will decrease. The decrease in the number of errors is the justification for making the filter adaptive.

As with any discriminator based receiver, the IF filtering that takes place before the resulting signal is applied to the discriminator is critical. Any noise that is not removed during the IF filtering is enhanced by the discriminator. The effect of the noise is to cause jitter in the location of the zero-crossings of the signal. Such jitter is evenly distributed

Figure 5.11 : Baseband System with Symbol Rate, Decision Directed Filter Updates and Decision Feedback Filter

when the input noise is white, causing a noise distribution that is white in phase. Since the action of the frequency discriminator is such that it differentiates the phase, this will cause the additive noise power to increase with frequency, starting at zero Hertz.

The noise contribution that exists within the same bandwidth as the transmitted signal cannot be filtered out. This portion of the noise will corrupt the signal in a manner that cannot be alleviated by any filtering after the discriminator.

There is also another important consideration when choosing an IF filter for a discriminator based receiver, that of phase linearity. A filter with non-linear phase within the pass-band of the desired signal will cause distortion in the signal which will alter the position of the zero crossings. This is due to the fact that nonlinear phase is equivalent to a group delay response that is not constant; different frequency components of the signal will experience different delays as they pass through the filter.

Filters that possess flat group delay are generally those with a finite impulse response (FIR). A popular type of filter that meets this requirement is a transversal surface acoustic wave (SAW) filter. In this simulation exercise the IF filter is modeled as a FIR filter of order 240, i.e. the impulse response spans 240 sample periods. This is a close approximation to SAW filter technology and allows for the simulation of the discriminator based receiver as it would be used in practice.

The simulation model of the discriminator based receiver is shown in figure 5.11.

Although in practice the input to the discriminator will be at some high IF frequency, the model used translates the entire IF section down to baseband I and Q components.

In order for such a simulation to be meaningful, the signal to noise ratio for the particular simulation being carried out must be determined. In a digital communication system though, the signal to noise ratio is normally expressed as the ratio of the energy transmitted per bit divided by the noise power spectral density. This quantity is typically

known as E_b/N_o . The energy and noise calculations performed to arrive at this ratio are typically normalized to a load of 1Ω . The energy per bit can therefore be written as :

$$E_b = \int_{-\infty}^{+\infty} g^2(t) dt$$

In the context of a discrete time system such as this simulation, the noise has to be carefully determined. White noise is included in such a system by adding samples of a random process to the samples of the signal during the simulation. The random process is characterized by a mean and a variance. The mean in this case will be zero but the variance is the parameter which must be controlled in order to control the amount of noise allowed into the system. The approach taken in these simulations was to keep this signal level constant and vary the noise power in order to achieve a desired value of E_b/N_o .

Assessing the signal energy is made relatively straightforward by the fact that we are dealing exclusively with constant envelope signals in this work. The modulated signal can be described as a rotating vector on the complex plane described by the equation :

$$R(t) = \cos(\theta(t)) + j \cdot \sin(\theta(t))$$

The RMS power dissipated into a 1Ω load by a complex phasor such as this one is known to be equal to :

$$P_s = \frac{\|R\|^2}{2} = 1 \text{ Watt}$$

The energy per bit will therefore be equal to :

$$E_b = \int_0^T P_s dt = T$$

As the vector rotates around the complex plane its speed of rotation (i.e. its angular frequency) is modulated by the baseband pulse stream $g(t)$, but its magnitude remains

Figure 5.12 : Phasor Diagram of Constant Envelope Signal

constant. This concept is illustrated in figure 5.12. Using the constant E_b value which is equal to T , the noise can then be scaled with respect to T in order to arrive at a desired value of E_b/N_o .

Arriving at the simulation parameters for the noise required more effort. The parameter of the pseudo-noise process that was varied in order to arrive at a desired E_b/N_o was the variance. The variance, σ^2 , can be thought of as the total noise power within the bandwidth of the noise. In order to arrive at the variance required to achieve a desired value E_b/N_o , the relationship of the variance to the desired value of E_b/N_o had to be established. The variance is equal to the total noise power contained in a bandwidth of f_s . This can be written as :

$$\sigma^2 = \int_{-f_s/2}^{+f_s/2} \frac{N_o}{2} df = \frac{N_o}{2} f_s$$

The above equation can be rearranged to yield N_o in terms of σ^2 and f_s :

$$N_o = \frac{2\sigma^2}{f_s}$$

The sampling frequency can be related to the symbol period, T_s , by the oversampling ratio, N , as follows :

$$f_s = \frac{N}{T_s}$$

The noise spectral density can therefore be written as :

$$N_o = \frac{2\sigma^2 T}{N}$$

This expression for N_o can be combined with the expression for E_b to yield :

$$\frac{E_b}{N_o} = \frac{N}{2\sigma^2}$$

This expression allows one to visualize the considerations for simulating systems such as the present one. As the oversampling ratio, N , is increased for a given noise variance, the fixed noise power will be distributed over a wider bandwidth. Therefore, in order to maintain a fixed value of E_b/N_o for the noise variance, σ^2 , must be scaled along with the oversampling ratio, N . With this consideration in mind, the simulation model was designed so that for any desired combination of N and E_b/N_o , the variance of the noise is scaled accordingly without any user intervention.

In order to code this, the noise variance had to be written in terms of the desired value of E_b/N_o and N . This is done by rearranging the equation for E_b/N_o to yield σ^2 explicitly :

$$\sigma^2 = \frac{N}{2(E_b/N_o)}$$

It is also important to note that E_b/N_o is usually expressed in decibels, and must therefore converted back to a linear ratio before using the above equation

In order to determine how well the discriminator based receiver will perform in the presence of additive noise, a number of simulations were run at various values of E_b/N_0 .

The simulations were run with the following parameters :

$$N = 64$$

$$f_{\text{sym}} = 1.152 \text{ Msym/sec}$$

$$\delta = 0.5$$

$$h = 1.0$$

Figure 5.13 : Accumulated Bit Errors for $E_b/N_0 = 10, 13, 16, 20, 30$

These conditions are representative of the hardware discriminator used in the next chapter of the thesis.

As can be seen from the figure, the use of the LMS algorithm allows the receiver to adapt in such a way as to optimize bit error performance in the presence of the particular signal and noise. This is evidenced by the fact that as the receiver adapts the slope of the accumulated bit errors curve flattens out. This implies that fewer bit errors are occurring per unit of time. The number of iterations required to reach steady state depends on the value of E_b/N_0 . Lower values of E_b/N_0 cause the LMS algorithm to search for a longer time in order to reach state, but also provide the most dramatic improvement in performance.

A receiver of this type is also able to adapt to changes in E_b/N_0 that occur as the receiver is operating in the field. This may tend to increase the users perception of the quality of the communication link, an important factor for the adaptation of digital technologies.

5.5) Conclusions

In this chapter simulation results of a Δ - Σ frequency discriminator model were presented as well as the use of LMS and RLS techniques to arrive at the optimum filter to process the bitstream from the discriminator. It was suggested that the RLS algorithm be used to derive the impulse response of a filter used to recover the transmitted data from the Δ - Σ bitstream. In addition, the LMS based filter with a DFE was shown to have the ability to reduce the bit errors when detecting the transmitted symbols as compared to a compromise matched filter, regardless of the E_b/N_0 value.

In the next chapter the design of the transmitter and the receiver digital filters is described. The receiver digital filter is then used to implement the filter with coefficients resulting from the RLS simulations. The use of the hardware implementation to process a bitstream from a board level Δ - Σ frequency discriminator is then presented.

Chapter 6 :

Hardware Design and Experimental Validation

6.1) Introduction

In order to validate the results of the simulations performed in the previous chapter, a hardware test-bed comprised of a pseudo-random bit source (PRBS), a Gaussian pulse shaping filter, a board-level frequency discriminator and a high speed digital filter was constructed. The objective was to validate the use of coefficients obtained through the adaptive filter simulations presented in chapter 5. Using these coefficients in a hardware based filter, samples from the discriminator could be processed and the results used to detect the transmuted symbols. By comparing this to the known sequence of transmitted symbols, a set of bit error rates for various frequency deviations was obtained.

The adaptive algorithm was still performed in software on a general purpose computer, but the final coefficient values obtained were incorporated on a real-time digital filter implemented on a XILINX field programmable gate array (FPGA). The real time digital filter is then used to process bitstreams from a board level implementation of a Δ - Σ discriminator.

6.2) Hardware Description

In order to perform an evaluation of the performance of the discriminator based receiver a number of modules had to be constructed and put to work. The overall test system is shown in figure 6.1. The pseudo-random binary sequence (PRBS) generator was used as

Figure 6.1 : Block Diagram of the Experimental Test Setup

a transmitted symbol source. The transmitted symbols were shaped into Gaussian pulses with $B_bT = 0.5$ using the digital Gaussian pulse shaper and converted to analog by applying the 8-bit digital samples to a digital-to-analog converter (DAC). The resultant baseband analog signal was used to drive the FM input of the Rhode & Schwarz SMHU signal generator to produce a bandpass FM GFSK signal centered at 865 MHz.

The FM signal was converted to a 1-bit digital representation of the frequency modulation using the $\Delta-\Sigma$ frequency discriminator board. The bits from the discriminator were then filtered using the high speed digital filter and the sign bit of the result was used to detect the transmitted bit. An exclusive-OR (XOR) gate was used to compare the (delayed) transmitted symbol with the detected symbol. By counting the number of pulses from the XOR gate, the number of bit errors was obtained and a BER was calculated.

6.2.1) The Frequency Discriminator

The discriminator used for this exercise was a board-level implementation of a second order $\Delta-\Sigma$ frequency discriminator which was constructed by Walt Bax as part of his thesis research [22]. The discriminator accepts an external 50 MHz clock signal which is divided down to 10MHz on the board itself. The frequency modulated input signal to the

Figure 6.2 : A Representative Schematic of the Δ - Σ Frequency Discriminator

discriminator is centered at 865 MHz. Although 865 MHz is not a typical IF frequency in most receiver applications, it does not affect the relevance of the results. The reason for this choice of frequency is that the discriminator available was originally developed for use in a frequency synthesizer for cellular telephony.

A basic description of the Δ - Σ frequency discriminator hardware is presented here. More complete details are published elsewhere [22]. A representative schematic of the Δ - Σ frequency discriminator is shown in figure 6.2.

The Δ - Σ frequency discriminator used was a second order type built around off-the-shelf components. The RF input signal is AC coupled to an ECL line driver that drives a multi-modulus divider. The output of the divider is then applied to an ECL based phase-frequency detector (PFD). In the PFD, the phase of the divided-down RF signal is compared to that of the reference signal, the difference of which is represented by a series of pulses that add or remove charge from the capacitor in the analog integrator. The output voltage from the integrator is then quantized as a one bit number using the analog comparator. This result is then latched and synchronized using a D-type flip-flop before being fed to the modulus control of the dual modulus divider.

6.2.2) The Digital Filter Board

In order to perform filtering of the sample sequence from the frequency discriminator, a digital filter with 192 taps, capable of processing 10 Msamples/sec had to be devised. Such a filter had to have the ability to process the samples in a real-time manner while keeping the complexity of the design within manageable limits. In order to do this, consider the digital filter shown in Chapter 4, figure 4.3. In order for this filter to have 192 taps, it can easily be imagined that a great deal of hardware would be required. In order to achieve a more efficient design, imagine partitioning the filter into 48 segments of 4 taps each. The partial result obtained from each of the 48 segments could then be summed for the final result as shown in figure 6.3. If only one filtered output sample was required of every 192 input samples, then each input sample would only have to be multiplied by its corresponding tap weight coefficient, since any intermediate results would be discarded.

With these considerations in mind, a filter was devised that would rely on precomputed coefficient sums for each set of 4 taps that were stored in EPROMs. The sums that were stored in the EPROMs served to avoid performing much of the math in real time and also allowed the clock speed inside the filter to be minimized. Each 4 tap filtering operation is performed immediately as each required set of 4 input samples becomes available, instead of waiting until all 192 samples arrive. The results obtained from each of the 4 tap filtering operations are then added in sequence using an accumulator instead of in a parallel manner as implied in figure 6.3.

Figure 6.3 : Digital Finite Impulse Response Filter Divided into 48 Segments

Figure 6.4 : EPROM Based Implementation of 192 Tap, 48 Segment FIR Filter

The basic architecture of the EPROM based filter is shown in figure 6.4. The parallel-to-serial converter collects the 4 input samples that belong to the current 4 tap filter. The counter keeps track of which of the 48 segments correspond to the current set of 4 input samples. The parallel to-serial converter output is used to index the particular precomputed sum required based on the input samples. The results from each of the 4 tap filters' precomputed sums are accumulated to form the final result. In this manner, the filtering can be performed in an efficient manner without creating any output that will be discarded.

The digital filter was implemented on a Xilinx XC3195-PPC175 FPGA. The FPGA contains the hardware used to derive all digital clocks from a master clock and to perform the required computations for the filter function. A set of EPROMs is used to store the coefficients for the filter. The XC3195 was chosen for its adequate size, good routing resources and abundant I/O. In order to maximize the efficiency of the implementation, a unique filter architecture was devised as has been shown in figure 6.4, with further detail in figure 6.5. A more detailed description of how the filter operates is undertaken in the following section.

6.2.2.1) Detailed Principle of Operation

This section describes the efficient architecture (in a gate count sense) that was derived to digitally filter the output of the Δ - Σ frequency discriminator. The key to understanding the operation of the filter is to recall that the operation of a filter is basically that of correlating a vector composed of a series of input samples with a tap weight vector. If the correlation operation is performed once for every input sample, then no decimation is implied in the filtering since there will be one filtered output sample for each input sample. The correlation operation can also be performed once for every N input samples, in which case there will be one filtered output sample for every N input samples. In this case there is a decimation by a factor of N implied in the filtering operation. The filter used to process the bits from the discriminator falls into the latter category. It has a 192 element tap weight vector and produces a filtered output sample for every 64 input samples.

The total impulse response of the filter spans 3 symbols. With an over-sampling ratio of 64, this requires a total of 192 taps to span all 3 symbol periods. Since the filter is required to produce a result once per symbol interval, there are, in essence, three filters implemented on the FPGA, each of which operates in parallel with the other two, but with each one offset from the other by one symbol period in time. Hence, each filter performs filtering over 3 symbol intervals, but the filters are timed such that each filter produces a result for every third symbol. In this way, the overall computing and storage requirements are minimized by not including the hardware required to produce output samples at times in between the symbol intervals.

Before proceeding further, some elaboration on the system clocks is in order. The fastest clock in the system is the 10MHz clock (FCLK) which is derived from the frequency discriminator. In the filter, FCLK is used to clock the serial-to-parallel shift register that receives the hits from the discriminator as well as to clock the divider that provides a divided down by four clock (SCLK) which runs the address counter and the accumulators. All remaining circuitry is clocked by SCLK, including the clear pulse generator for the accumulators, the 3 clocks (BETA0-2) that latch the current output decision, and the

Figure 6.5 : Block Diagram of Filter System

symbol clock (SYMCLK) that lets the user know when the decision output of the filter is valid. Details on the implementation of the clock system are provided in section 6.2.2.3.

As can be seen from figure 6.5, bits from the discriminator enter a 4-bit serial to parallel shift register. Each time a set of four bits has entered, these four bits are latched and used to form the four low order bits of the address lines to the EPROMs. The next six bits of the EPROM address are derived from the MSB address generator which is used to partition the impulse response of the filter into forty-eight segments, therefore requiring 48 sets of 4 input bits to form a result. As each set of four bits is latched, the EPROM's table lookup is performed and the values from the EPROMs are latched. These values are then added to the contents of their respective accumulators. Once all of the 48 partial products

are accumulated in any of the three accumulators, the sign bit of the accumulated result is taken to be an estimate of the transmitted bit as per Table 6.1.

Accumulator Sign Value	Transmitted Bit
+	1
-	0

Table 6.1 : Mapping of Accumulator Result to Transmitted Bit

6.2.2.2) The EPROM Look-up Table

This section proceeds to explain the organization of the EPROM look-up table (LUT). The organization of and the values stored in this table are central to the operation of the digital filter system.

In order to make the hardware design more tractable, the impulse response of the filter is partitioned into 48 segments. Each of these 48 segments stores the dot product between the 4 tap weights corresponding to that segment and each possible permutation of the four, 1-bit, input samples. Since the total number of possible permutations of the input samples is 16, there are 16 sets of partial dot products stored in each of the 48 segments.

During each of the 48 accumulator cycles, partial dot products are selected, one from each of the 48 sets of dot products, and are accumulated in sequence to form the final result. In other words, the 192 element dot-product more commonly associated with a filter formed of 192 taps is broken up into the sum of 48 dot-products of 4 elements each as follows :

$$\begin{aligned}
 Y &= [X_0, X_1, X_2, \dots, X_N, \dots, X_{2N}, \dots, X_{3n}] \bullet [C_0, C_1, C_2, \dots, C_{191}] \\
 &= [X_0, X_1, X_2, X_3] \bullet [C_0, C_1, C_2, C_3] + [X_4, X_5, X_6, X_7] \bullet [C_4, C_5, C_6, C_7] + \dots \\
 &\dots + [X_{188}, X_{189}, X_{190}, X_{191}] \bullet [C_{188}, C_{189}, C_{190}, C_{191}]
 \end{aligned}$$

Figure 6.6 : Memory Organization of the EPROM Based LUT

The advantage of performing the filtering operation this way is that since the incoming samples are processed in groups of 4, a great deal of computational savings are realized by storing the inner product of four filter tap weight coefficients (the partial inner product) with each possible combination of the four input samples in the EPROMs. Hence, a great deal of the computation is done a-priori (and stored in the EPROMs) instead of performing all of the computations on-line. This leads to an EPROM memory organization as shown in figure 6.6.

6.2.2.3) The Filter Clock System

Referring once again to figure 6.5, it can be seen that the "count-to-48" circuit is used to index each of the 48 filter response segments and hence the 16 possible partial inner products corresponding to each of these segments. In order to do this, the fast input clock

Figure 6.7 : Timing Diagram of the Digital FIR Filter

to the filter is divided by 4 to produce the clock known as "SCLK" which is used to latch the set of 4 input bits and also to drive the "count-to-48" circuit. Since the impulse response spans 3 symbol intervals, there are 3 results accumulated in three separate phases for each group of 4 input samples from the discriminator. This requires that the "count-to-48" circuit produces 3 different phases, each phase being offset by one symbol period, or equivalently, by $48/3 = 16$ SCLK cycles. The timing is demonstrated in figure 6.7. Note that the 4 LSBs of the address are equal to the 4 input samples (which have been set to zero for the purposes of timing simulation) and that the 5 MSBs for each of the three phases are offset by 16 SCLK periods with respect to each other.

The clock system for the digital filters is shown in figure 6.8. As can be seen from the figure, only one counter is used and the other two counter phases are derived from it. In order to produce the three phases from one counter, one phase is taken directly from the counter, while the other two phases are produced from the first phase by some

Figure 6.8 : Clock System for Digital Filter

combinatorial logic. In this manner the hardware that would be required to implement two additional counters is replaced by a few additional gates, and no preloading of any counters is required.

Also included in the clock system is the circuitry to generate the clear pulses for the accumulators. When any of the accumulators reaches the end of its 48 accumulation cycle and the final result (the sign bit) is latched, that accumulator is then cleared by applying a pulse to the clear circuit in the accumulators internal feedback path. The clear pulse causes a zero to be fed back to the input of the adder within the accumulator for one SCLK cycle.

The clear pulses are generated by a set of gates connected to the output of the 6-bit counter which generate a pulse when the end of an accumulator cycle is reached. The pulses are generated in three phases that are properly synchronized with the accumulators and also possess the proper duration (one SCLK cycle) to ensure that no accumulator

Figure 6.9 : Internal Block Diagram of Accumulators

results are lost. The output of the combinatorial circuitry is resynchronized with SCLK, using D-type flip-flops in order to minimize timing skew.

6.2.2.4) The Accumulators

The accumulators are used to accumulate the 48 partial inner products and pass the result on to the multiplexer which selects from one of the three accumulators. The accumulators themselves are comprised of an adder circuit, a 19 bit latch and a clearing circuit. The internal structure of the accumulators is shown in figure 6.9. As seen from the figure, the new 16 bit operand from the EPROM LUT is sign extended by 3 bits to form a 19 bit input operand and is added to the stored value fed back from the 19 bit latch. The sum is then stored in the 19 bit latch and added to the next input operand.

Figure 6.10 : 19 Bit Ripple Carry Adder

The schematic of the-19 bit adder is shown in figure 6.10. The operation of the adders will be explained in an intuitive manner. The sum output of a single adder is equal to one if either one or three inputs are equal to one; that is to say when an odd number of inputs are equal to one. As is well known, an exclusive-OR operation produces a one if an odd number of the operands is equal to one. Therefore the equation for the sum output of a single adder is :

$$S_n = A_n \oplus B_n \oplus C_{in,n} = (A_n \oplus B_n) \oplus C_{in,n}$$

The carry output of a single adder will be high if any pair or pairs of the three inputs is equal to one. If this happens, the adder overflows and the carry output is equal to one. The equation describing the carry output signal for a single adder can therefore be written as :

$$C_{out} = A \cdot B + A \cdot C_{in} + B \cdot C_{in}$$

In order to add two 19 bit numbers, 19 of the one bit adders have to be cascaded. In this manner, as the individual one bit sums from each one bit adder are formed, the carries are also formed and passed on to each subsequent stage of the 19 bit adder. Adders with this topology are known as "ripple-carry adders".

The propagation time for the carry to ripple through the entire adder limits the maximum frequency of operation for this circuit. In this case though, the adder has to produce results at the rate of 2.5 MHz, the frequency of SCLK. This is an acceptable speed for the adder to function properly, as verified by simulation of the circuit for worst case delay in the design phase.

Once 48 clock cycles are completed, a narrow clear pulse (BETAx) is applied to the clear circuit in the feedback path of the accumulator. The clear pulse causes all of the 19 feedback lines in the accumulator to be set to zero. The operation of the clear circuit is best understood by examining figure 6.11. Referring to the figure, it can be seen that

Figure 6.11 : 19 Bit Clear Circuit

when the clear pulse goes high, it forces the outputs of all 19 AND gates in the clear circuit to be low for the duration of the clear pulse. For this reason it is important that the clear pulse be synchronized to the rising edge of SCLK and have a duration of one SCLK cycle. This relation must be maintained even though the frequency of the clear pulse is 1/48 of the frequency of SCLK. When the clear signal is asserted low, the clear circuit is transparent. The zero from the clear circuit is then added to the new input operand, thus simultaneously clearing the accumulator and forming a new result in the output latch

6.2.2.5) The Three Phase Decision Clock Generator

The circuit of figure 6.12 shows the design of the 3-phase clock generator. The 3-phase clock generator is used as the control input to the MUX that selects the current valid output decision. This circuit uses SCLK to maintain synchronism with the rest of the filter

Figure 6.12 : 3-Phase Decision Clock Generator

2

of/de

2

PM-1 3 1/2"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

PRECISIONSM RESOLUTION TARGETS

Figure 6.13 : The Decision Multiplexer

system. From the SCLK input, 3 clocks are generated, each clock producing a logic level of '1' for 120 degrees of the SYMCLK cycle in a non-overlapping manner. In this manner, the level-triggered control inputs of the MUX select the current decision from the corresponding accumulator.

6.2.2.6) The Decision Multiplexer

The Decision multiplexer (MUX) is used to select the current valid decision variable from one of the three accumulators. The circuit diagram of the MUX is shown in figure 6.13. The circuit consists of three flip-flops at the input to latch the current decision. These are followed by an AND gate which takes the corresponding flip-flop output and gates with the corresponding phase of the 3-phase clock, thus selecting the current valid decision. The output of 3 AND gates are concentrated at the OR gate, which allows for a single output bitstream event, though the decisions are processed in three streams within the filter system.

6.2.3 Pseudo-Random Bitstream Generator and Gaussian Pulse Shaper

In order to be able to test the receiver, a suitable signal source for the baseband modulating waveform had to be constructed. To this end, a pseudo-random bitstream (PRBS) generator and a digital realization of a Gaussian lowpass filter to shape the bitstream were designed and constructed.

Figure 6.14 : PRBS Generator and Gaussian Pulse Shaper

The Gaussian pulse shaper (filter) system block diagram is shown in figure 6.14. The output of the PRBS generator is shifted into a register of length 3, a requirement driven by the fact that the impulse response of the Gaussian filter with $B_b T = 0.5$ spans 3 symbol periods. The bits in the shift register are then sent, along with the output of a 4-bit counter, to the address lines of an EPROM that stores the accumulated coefficients. The counter is used to divide the symbol period into 16 samples and hence to step all 16 samples once for each transmitted symbol. Such a large amount of oversampling is not required by the Nyquist theorem, but instead is used to ease the requirements of the lowpass filter after the D/A converter. By using such a high sampling rate, the filter can have a very gradual roll-off and thus alleviate any pulse distortion problems caused by large group delay variations within the bandwidth of the modulation signal. For each step of the counter, the output of the EPROM is latched and used to drive the D/A converter.

In order to obtain the necessary coefficients for the look-up EPROM, it is necessary to understand how the Gaussian pulse shaper operates. As can be seen from the timing diagram of figure 6.15, the counter (denoted COUNT_TO_16) starts at zero after rolling over at 15, thus permitting the use of 16 samples per symbol. During each sampling instant an address is sent to the EPROM. The address is composed of the current value

Figure 6.15 : Timing Diagram of PRBS and Gaussian Pulse Shaper

from the counter and the value of the previous transmitted bit, the current transmitted bit and the next transmitted bit. This address indexes the sum of the current value of the Gaussian pulse, the amount of pre-cursor ISI and the amount of post-cursor ISI for the particular combination of the current symbol, the previous symbol and the next symbol. This concept is demonstrated in figure 6.16. As can be seen from the figure, the Gaussian pulse spans 3 symbol intervals. Each one of the symbol intervals is divided into 16 samples, or equivalently, the overall Gaussian pulse is divided into 48 samples. The value stored at a particular EPROM address is therefore :

$$\text{Value}(k) = a_{i-1} * g(k-16) + a_i * g(k) + a_{i+1} * g(k+16)$$

where:

- a_{i-1} is the value of the previous transmitted symbol
- a_i is the value of the current symbol
- a_{i+1} is the value of the next symbol
- $g(k)$ is the value of the k^{th} sample of the Gaussian pulse

Figure 6.16 : Sampling Method for Gaussian Pulse Shaper

The value obtained by indexing the LUT is latched and presented to the DAC. The DAC used was an Analog Devices AD568, a 12-bit high-speed bipolar circuit. This device was

Figure 6.17 : Schematic Diagram of Pseudo-Random Bitstream Generator

chosen for its high speed, high resolution and availability. The unused digital inputs were tied low within the FPGA.

The schematic diagram of the PRBS generator is provided in figure 6.17. As can be seen from the figure, the PRBS generator is basically a shift register with combinatorial feedback to the input. The sequence length is adjusted by asserting N9, N10, N11 or N12 to obtain bit sequence lengths of 2^9 , 2^{10} , 2^{11} or 2^{12} , respectively.

6.3) Experimental Results

This section will present experimental results obtained from the hardware transmitter-receiver testbed. The experimental testing permits one to gain insight into the practical aspects of the system implementation. It allows for the identification of design issues that are not readily apparent from theory or simulation.

6.3.1) Modulated PSD from Frequency Discriminator

The PSD from the frequency discriminator with a sinusoidally modulated FM signal at its input was measured first in order to assess the noise performance of the printed circuit board based discriminator, and compare it to the simulation model. In order to do this, the test equipment was set up as shown in figure 6.18. As seen on the figure, the input of the Δ - Σ discriminator was driven by a Rhode & Schwartz SMHU signal generator with the internal FM modulator set to produce sinusoidal FM modulation with a deviation of 100 kHz and a rate of 100kHz. The clock input of the discriminator was driven by an HP8663A signal generator set for 50 MHz. As indicated earlier in section 6.2.1, the 50 MHz input clock corresponds to a sampling rate of 10 MHz since the clock input is divided down by circuitry on the discriminator board. The bitstream from the Δ - Σ discriminator was captured on an HP 16500 logic analyzer and then downloaded to an HP personal computer via the IEEE-488 interface. The stored bits were then moved to a SPARC-based workstation where they were processed using MATLAB to perform the Fast Fourier transforms (FFTs). In order to ensure consistency, the measured bitstreams

Figure 6.18 : Setup Used to Collect Bitstream from Discriminator Board

were processed in exactly the same manner, using the same software routine that was previously used with the bits derived from the simulation model of the discriminator.

The power spectral density obtained of the experimentally derived bitstream was plotted on the same graphs as the corresponding simulated bitstream from chapter 5 and the results were compared. The resulting graphs are shown in figure 6.19. As can be readily seen from the graphs, the noise PSD of the board level discriminator differs from that of the simulation model in one key area, the noise at baseband frequencies. Below 15 kHz the noise spectrum produced by the hardware discriminator board does not appear to roll off as rapidly as that of the model. In fact, at the lowest frequency resolved by the FFT, the noise density of the hardware discriminator is approximately 20 dB above that of the model. The difference in the noise floor at lower frequencies is probably even greater since the trend in the data shows that the noise density of the hardware discriminator and the model diverge rapidly below 15 kHz.

The fact that the spectral density of the noise above 15 kHz predicted by the model is in reasonable agreement with the hardware measurements is significant. Referring to figure 5.3(a-d) it can be seen that the main lobe of the GFSK signal spans approximately 150 kHz, at which frequency the first null occurs. This band width is significantly greater than the 15kHz in question. Therefore the noise contribution of the hardware discriminator

**Figure 6.19 : Measured and Simlated PSD of Discriminator Output
for 100kHz Deviation, 100 kHz Rate FM at the Input**

Figure 6.20 : Equipment Configuration for BER Measurements

relative to the model will not be so great as to render the system ineffective. It will however tend to increase the bit error rate slightly.

The sinusoidal modulation test case validates the use of the discriminator model to some degree, although at lower frequencies the validity of the model is questionable and requires further investigation and possibly some refinement. A test case using GFSK at the input would not have been able to yield the same sort of insight into the noise behavior of the discriminator. The spectrum of a random GFSK symbol stream would obscure the noise floor of the discriminator since its spectrum is distributed throughout the entire baseband of the discriminator, as seen previously in figure 5.3(a-d).

6.3.2) BER Measurement on the Overall System

The next step in the experimental procedure was to measure the BER performance from end-to-end of the transmitter-receiver testbed. In order to perform this measurement, the testbed was set-up as shown in figure 6.20. The transmitter system consisted of the

PRBS, the GMSK pulse shaper board and the Rhode & Schwartz SMHU signal generator. The GFSK signal produced by this combination was fed to the receiver. The receiver consisted of the Δ - Σ frequency discriminator and the high speed digital filter board. The 50 MHz master clock for the system was provided by the HP8663A signal generator which was phase locked to the SMHU signal generator. All of the other clocks in the system were then derived from this master clock. The 50 MHz master clock was divided down to 10 MHz on the discriminator board and used to run both the transmitter and receiver clock inputs. Since there was no timing recovery circuit present, a reset switch on the transmitter board was used to reset all of the digital circuits simultaneously and hence bring the system into synchronization. The logic analyzer was then used to store the pulses from the bit error detector. Each time a bit error occurred, the output of the XOR produced a logical '1' which was stored by the logic analyzer. The bits were then transferred to the PC via the IEEE-488 interface. From the PC, the data was compressed and subsequently transferred to a SPARC-based workstation for further processing.

The sampling frequency was restricted to 10 MHz by the design of the board level discriminator. The digital filter was designed to operate with an oversampling rate of 64; hence the data rate was determined based on these two constraints. Therefore, in order to obtain an oversampling ratio of 64, the symbol rate must be scaled accordingly :

$$f_{sym} \equiv \frac{\text{Sampling Rate}}{\text{Oversampling Ratio}} = \frac{10\text{MHz}}{64}$$

$$f_{sym} = 156,250 \frac{\text{Symbols}}{\text{sec}}$$

The scaling of the symbol rate was performed automatically since it was built into the digital hardware. The symbol rate must be known though, in order to be able to calculate the frequency deviation required to realize a particular value of modulation index or to determine the modulation index from the deviation.

Figure 6.21 : Measured Bit Error Rate vs Deviation

The BER measurements were performed for a multiplicity of frequency deviations. The deviation was varied as the independent parameter since it directly affects the signal to noise ratio (SNR) in the baseband of the discriminator. If an IF filter was used before the discriminator each of the various deviations would each require an IF filter of a particular bandwidth. Since an appropriate set of IF filters was not available, none was used. The information obtained from the tests is still highly useful since it leads to a set of requirements that must be imposed on the design of a Δ - Σ frequency discriminator in order to obtain a desired level of performance.

The plot of measured BER vs deviation is given in figure 6.21. As can be observed from the figure, the BER rolls off rapidly for higher deviations. The table of the data used to create the plot is also provided in table 6.2.

From the plot of BER vs deviation it can be seen that acceptable bit error rates occur for deviations of greater than 400 kHz. This deviation is too wide for the current generation

of narrowband communication systems. Therefore, some improvements have to be made to the discriminator in order to allow smaller deviations to be used. The improvements include creating a discriminator with a smaller delta (see section 5.2) and reducing the amount of noise in the baseband in the discriminator.

Deviation	h	Bit Error Rate
0	0	0.5 (Theoretical)
78.063	1	4.113×10^{-1}
156.125	2	1.97×10^{-1}
235.25	3	3.73×10^{-2}
313.5	4	3.10×10^{-3}
400	5.12	1.34×10^{-5}

Table 6.2 : Data for BER vs Deviation Plot

Reducing the delta (δ) of the discriminator or lowering the noise floor of the discriminator can be done jointly in order to reduce the BER for a given deviation. Each time the value of delta is halved it increases the signal level at the output of the discriminator by 6 dB, or equivalently, reduces by one half the deviation required to achieve a given BER. This is due to the fact that δ directly affects the phase resolution of the discriminator. Recall that the dual modulus divider at the input of the discriminator divides by either N or $N+\delta$ where in the current discriminator $\delta=1$. Therefore the discriminator can advance or retard the phase of the input signal by $\delta/2 \cdot 2\pi$, which for the current discriminator works out to π radians. This is much greater than the excess phase produced by GMSK during a sampling interval, which is $1/64$ of a symbol interval since the total excess phase produced by GMSK is $\pi/2$ radians per symbol interval. Reducing the value of δ will therefore provide the discriminator with the ability to resolve smaller changes in phase as are encountered in narrowband GFSK modulation. Therefore, there is a lot of room for improvement in the design of the discriminator. An fully integrated discriminator would

go a long way in improving the performance of the receiver but such a discriminator was not available for the work of this thesis.

In order to reduce the amount of noise in the baseband of the discriminator a higher order implementation may be helpful. The discriminator that was simulated and used in the hardware exercise was of order 2 (i.e. second order). A third order discriminator would reduce the amount of noise in the baseband by pushing a greater proportion of the quantization noise to higher frequencies [25], resulting in a greater signal noise ratio in the baseband frequencies. A third order frequency discriminator was not available for the work of this thesis.

There is also one other factor that may have contributed to the error. The modulation was performed with an open loop system. This leads to the possibility of frequency offsets in the modulated signal that may have biased the decisions. Although some attempt was made to minimize this problem by manually tuning the center frequency of the signal generator, a frequency locked synthesizer with the modulation occurring within the loop would minimize this type of impairment [23].

6.4) Conclusions

This chapter described the design of a testbed to evaluate the performance of a Δ - Σ frequency discriminator based receiver. The hardware consisted of a circuit to generate a pseudorandom Gaussian filtered pulse stream and a high speed filter to process the bits from the Δ - Σ discriminator. The hardware was then combined with an existing board level implementation of a Δ - Σ frequency discriminator to form a testbed for a Δ - Σ discriminator based transmitter-receiver.

The hardware description revealed the details of how innovative architectures for a Gaussian pulse shaper and a high speed filter for one-bit samples were realized in FPGA form. The same circuitry also lends itself to an efficient realization in a CMOS VLSI process. The Gaussian pulse shaper and the high speed digital filter required a relatively

small amount of digital logic circuitry. By relying on semiconductor memory for the storage of precomputed coefficient sums, the designs leverage advances in semiconductor memory to create a system that can be realized efficiently in a CMOS process. The area required for such a system would be relatively small, particularly if realized in a process that has efficient memory cells already available. An implementation with programmable memory would also allow the user to specify the filter response after fabrication, thus creating wider appeal for the part. The high speed digital filter is also efficient in power sense since the majority of the circuit (including the memory) is operated at a fraction of the oversampling rate.

Testing of the board level discriminator revealed that the model used in the simulations of chapter 5 accurately represents the noise performance of the discriminator for frequencies above 15 kHz. A more detailed model is required to accurately model the noise of a real discriminator at lower frequencies.

The testbed demonstrated that the Δ - Σ frequency discriminator is useful for the demodulation of wideband GFSK signals. It was also suggested that in order to demodulate narrowband GFSK signal such as GMSK a Δ - Σ frequency discriminator with a smaller delta (δ) and possibly higher order is required.

Chapter 7:

Conclusions and Recommendations for Future Work

7.1) Conclusions

The demand for reliable low-cost radio receivers for digital FM signals is growing rapidly every year. This justifies further research into the area of digital FM receiver architectures which are suitable for more efficient VLSI implementation. This thesis has attempted to bring such a radio receiver based on the Δ - Σ frequency discriminator based receiver one step closer to reality. Through simulation and printed circuit board level realization, this thesis has shown that such a receiver is feasible.

The simulation exercises in this thesis have demonstrated the application of adaptive filtering techniques to the design of filters for such receivers. The LMS technique was shown to be relatively slow and inaccurate relative to the RLS algorithm but simpler to implement. An LMS based FIR filter with a decision feedback section was shown through simulation to provide an improvement in BER as the filter adapted to the input signal.

The RLS technique was shown to be useful as a tool for fixed filter design when the optimum filter response is not readily evident. The coefficients obtained using the RLS algorithm were used in a printed circuit board level implementation of a fixed digital filter.

The hardware testbed constructed demonstrated the BER of the transmitter-receiver link versus frequency deviation. The deviations required to achieve a BER of less than 10^{-3} were considerably larger than those dictated by the recent PCS system standards such as

DECT, but this was due to limitations in the frequency discriminator used in this exercise. A discriminator with a smaller δ and/or higher order would bring the performance of the receiver demonstrated here in line with the new PCS standards.

7.2) Recommendations for Future Work

Following from the conclusions reached from this thesis, the first objective of future work in designing a radio based on the Δ - Σ frequency discriminator should be the design and implementation of a discriminator that is more suitable for PCS applications such as DECT. This will initially require some work on the architecture of a discriminator with a small value of delta (δ) and possible higher order. Other goals for such a discriminator include improved noise performance, low power consumption and the potential for high production yields. A monolithic implementation will also be able to operate on less power and therefore be able to support long battery life.

The filtering system designed and built as part of this thesis would, in a VLSI version, be implemented in a high speed CMOS process in order to increase speed, reduce the power consumption and reduce costs. A monolithic implementation could also include timing recovery and frequency offset compensation more readily than can be done with an FPGA implementation. Compared to an arctangent demodulator, the Δ - Σ frequency discriminator directly provides a measure of frequency deviation, eliminating the need for the multipliers and the arctangent LUT. The Δ - Σ discriminator and the arctangent circuits both require filtering of the signal following demodulation. The one-bit samples from the Δ - Σ discriminator can use filtering techniques as described in this thesis in order to avoid using multipliers, thus conserving power and area.

It was mentioned in chapter 4 that the work of this thesis focuses on detecting the transmitted symbols on a symbol-by-symbol basis. Future work can include methods for multi-symbol detection, which would provide improved bit error rate performance. Such techniques have been suggested in the literature [26] but require computationally expensive multipliers to calculate phase differences. As shown in figure 7.1, a

(a) Bandpass Phase Detection

(b) Discriminator Phase Detection

Figure 7.1 : Phase Difference Detection Using (a) Bandpass Sampling and (b) Discriminator Techniques

discriminator that provides a digital measure of frequency deviation makes it possible to replace the multipliers with adders.

Another useful area for future work may be in the area of antenna diversity and how it may best be applied to a Δ - Σ frequency discriminator based radio receiver. In applications such as DECT with slow, flat fading and wavelengths comparable to the physical size of the telephone handset, it is possible to use two antennas in the handset. By using two antennas the fading problem can be combated and hence provide improved quality of service to the user.

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Appendix A :

**Schematics of High Speed Digital Filter
for the Digital Receiver**

Figure A.2 : Clock Generator for Digital Filter

Figure A.3 : 3-Phase Clock Generator

Figure A.4 : 19 Bit Accumulator

Figure A.5 : 19 Bit Adder

Figure A.6 : 19 Bit Bus Clear

Figure A.7 : LSB Address Generator for Digital Filter

Appendix B :

**Schematics of Pseudorandom Bitstream
Generator and Gaussian Pulse Shaper**

Figure B.1 : Top-Level Schematic of Pseudorandom Bitstream Generator and Gaussian Pulse Shaper

Figure B.2 : Detailed Schematic of Pseudorandom Bitstream Generator

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