TECHNIQUES FOR LOW-POWER CMOS TRANSMITTER SYSTEM INTEGRATION FOR SHORT-RANGE RADIO-FREQUENCY COMMUNICATION

by

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Abstract

In this thesis, techniques for low-power CMOS transmitter system integration for short-range radio-frequency communication are developed, demonstrated and evaluated with the design and implementation of a low-power, energy-efficient, cost-effective and miniature-sized SoC transmitter for wireless dosimetry or thermometry, to name but two potential medical applications. "On-chip" antenna integration is a technique investigated for reducing the form-factor of the transmitter. Although the antenna's dimensions generally decrease with higher carrier frequencies, operating with a carrier at relatively lower frequencies – in the multi-gigahertz band, is a technique considered for reducing the power consumption of the transmitter while minimizing propagation path-loss. The antenna simultaneously serving as a far-field radiating element and an inductive element in the resonant tank of an oscillator is a technique investigated to remove the need for a power amplifier, and thus reduce system power consumption, while also addressing antenna power transfer. An open-loop modulation mode of a PLL-based modulator is a technique explored to lower the power consumption of the transmitter during a data packet transmission such that the system can be powered by an on-chip ultracapacitor and solar cell combination. The SoC transmitter's antenna is a single loop inductive structure of 0.6 mm^2 in area, and is the first small-loop antenna to be integrated without costly post-processing techniques in a mainstream CMOS process having a low-resistivity substrate. With an antenna-delivered power of 0 dBm, the transmitter's communication range is 2 m while maintaining 30 dB of fade margin with a conventional receiver, and thus demonstrates the feasibility of integrated small-loop antennas for short-range communication. The SoC transmitter is implemented in a 1.2 V 0.13 μm CMOS process and is revolutionary in that it is the first SoC to operate at the 6-GHz frequency band. Communicating over a 6.3 GHz FM carrier with a data rate of 300 kbps, the transmitter's average power consumption is 21 μW and transmits with an efficiency of 16%. In spite of the fact that the SoC transmitter operates at in a multi-gigahertz band and communicates with a lossy integrated antenna, these performance metrics compare favourably to those obtained from published state-of-the-art transmitter designs.

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Table of Contents

Abstract ii

Acknowledgements iii

Table of Contents iv

List of Tables viii

List of Figures and Illustrations ix

List of Abbreviations and Symbols xiii

1. Introduction 1

1.1. Motivation 1

1.1.1. Wireless Biomedical Sensor System 3

1.2. SoC Challenges Overview 4

1.2.1. Biomedical Sensor 5

1.2.2. Power Source 5

1.2.3. Antenna 6

1.3. Thesis Objectives 7

1.4. Thesis Contributions 7

1.4.1. Research Collaboration 9

1.5. Thesis Organization 10

2. SoC Transmitter Design Considerations 12

2.1. Antenna Fundamentals 12

2.1.1. Characteristics 12

2.1.2. Performance Metrics 16

2.1.3. Structures 22

2.1.4. Integration 25

2.2. Transmitter Fundamentals 28

2.2.1. Communication Link Budget 28

2.2.2. Power and Efficiency 29

2.2.3. Modulation 33
2.2.4. Architectures 36
2.2.5. Performance Comparison 39
2.2.6. Circuit Integration 43
2.2.7. Reference Oscillator 43
2.3. Power Source Fundamentals 44
2.3.1. Thin-Film Ultracapacitors 45
2.3.2. Thin-Film Solar Cells 45
2.4. Design Considerations Summary 46

3. SoC Transceiver Front-End Architecture 48
3.1. Technology 49
3.2. Integrated Small-loop Antenna 49
3.2.1. HFSS Antenna Model 50
3.2.2. Equivalent Lumped Circuit 53
3.3. Receiver Considerations 55
3.4. Communication Range 57
3.5. Oscillator Transmitter 59
3.6. System Analysis 60
3.7. Transceiver Front-End Summary 62

4. Open-Loop Modulation TX Design 64
4.1. TX Architecture 64
4.1.1. Direct OL Modulation Transmitter Behaviour 67
4.2. Voltage-Controlled Oscillator 68
4.2.1. Topology and Start-up Considerations 68
4.2.2. Current-Limited and Voltage-Limited Regimes 71
4.2.3. Oscillator Transmitter Efficiency 72
4.2.4. Simultaneous *gm* and Impedance Matching w/ Power Optimization 77
4.2.5. Design and Simulation 81
4.3. Divider 93

4.4. Phase Frequency Detector 95
4.5. Charge Pump 96
4.6. Up-Down Mux, Loop Switch and Leakage Buffer 98
4.7. Loop Filter 101
4.8. VCO Buffer and Output Buffer 103
4.9. Test Circuitry 105
4.10. TX Design Summary 106

5. Open-Loop Modulation TX Prototype 108
5.1. Top-Level Schematic 108
5.2. Simulations 110
5.2.1. Behavioural-Level 111
5.2.2. Transistor-Level 113
5.3. Implementation 117
5.3.1. Layout 119
5.3.2. Fabrication 120
5.4. Measurements 121
5.4.1. PLL Loop Filter Bandwidth 122
5.4.2. PLL Locking Time 123
5.4.3. VCO Phase Noise 124
5.4.4. Charge Pump Current Mismatch 125
5.4.5. Frequency Tuning Range 127
5.4.6. Modulation Range 127
5.4.7. Carrier Drift 128
5.4.8. FM Modulation (BFSK) 132
5.4.9. Antenna Impedance 132
5.4.10. Antenna Radiation 134
5.4.11. Transceiver Front-End Communication 136
5.5. Performance 138
5.5.1. Re-comparison 141
5.6. Discussion 142

5.7. TX Prototype Summary 143

6. Conclusion 146

6.1. Thesis Summary 146

6.2. Thesis Contributions 148

6.3. Publications Summary 149

6.4. Future Work 151

7. Appendix A 153

8. References 157

List of Tables

Table 1: A comparison of estimated small-loop antenna sizes in ISM and UNII. 27
Table 2: A comparison of published short-range transmitters. 40
Table 3: A performance comparison of published short-range transmitters 40
Table 4: A comparison of P_{nmos} for different VCO designs. 83
Table 5: TSPC prescaler transistor sizes 94
Table 6: Charge pump transistor sizes. 97
Table 7: Loop switch transistor sizes. 100
Table 8: Leakage buffer transistor sizes. 101
Table 9: Second order loop filter – bandwidth adjustments. 102
Table 10: VCO buffer transistor sizes. 103
Table 11: Output buffer transistor and resistor sizes. 104
Table 12: TX power, bias, low-frequency and high-frequency signal pins. 109
Table 13: Simulation; TX power consumption in closed-loop mode[†] 113
Table 14: Simulation; TX power consumption in open-loop mode[¥]. 114
Table 15: Simulation; TX test circuitry power consumption 114
Table 16: Simulation; Carrier drift rate over ambient temperature. 115
Table 17: Simulation; TX results summary. 116
Table 18: Modulation data rate considerations for frequency drift. 130
Table 19: Wired TX to RX test setup part list. 137
Table 20: Measurement & Simulation; TX results summary. 141
Table 21: Measurement & Simulation; TX power consumption. 141
Table 22: Measurement & Simulation; TX performance. 141

List of Figures and Illustrations

Figure 1-1: Thomson & Nielsen Electronics; a) MOSFET dosimeter sensor and b) patient with "wired" sensors. 3
Figure 1-2: Wireless biomedical sensor system 4
Figure 1-3: SoC transceiver architecture for wireless dosimetry 10
Figure 2-1: Spherical co-ordinate system. 14
Figure 2-2: Linear polarization; a) E-field vectors and b) trace figure. 15
Figure 2-3: Circular and elliptical polarization; a) circular trace figure and b) elliptical trace figure. 15
Figure 2-4: Antenna equivalent circuit. 19
Figure 2-5: Antenna power transfer associations 21
Figure 2-6: Half-wave dipole antenna; a) physical structure and b) radiation pattern. 23
Figure 2-7: Small-loop antenna; a) physical structure and b) radiation pattern. 24
Figure 2-8: Large-loop antenna; a) physical structure and b) radiation pattern. 24
Figure 2-9: Estimated integrated antenna dimensions. 27
Figure 2-10: Timing diagram of the encoded data 30
Figure 2-11: BFSK generation; a) VCO and b) switched oscillator. 35
Figure 2-12: Direct closed-loop modulation transmitter. 37
Figure 2-13: Direct open-loop modulation transmitter. 38
Figure 2-14: Oscillator transmitters; a) without PA and b) with PA. 38
Figure 2-15: Injection-locked transmitter. 39
Figure 2-16: P_{TX_avg} and η_{TX} comparison of published short-range transmitters. 41
Figure 3-1: HFSS model of the antenna. 52
Figure 3-2: HFSS radiation pattern and gain simulation; a) 3D and b) 2D. 52
Figure 3-3: Equivalent lumped circuit of the antenna. 53
Figure 3-4: Simulation; S_{11} a) HFSS antenna model and b) lumped circuit. 54
Figure 3-5: Inductance comparison of HFSS antenna model and lumped circuit. 54
Figure 3-6: Q comparison of HFSS antenna model and lumped circuit. 55
Figure 3-7: Injection-locked receiver and demodulator 57

Figure 3-8: Communication range estimate. 58
Figure 3-9: Communication link set-up options. 59
Figure 3-10: Oscillator transmitter (directly modulated) model. 60
Figure 3-11: Range, data rate, and RX injection-locking bandwidth. 61
Figure 4-1: Direct modulation transmitter topology in closed-loop mode. 65
Figure 4-2: Direct modulation transmitter topology in open-loop mode. 66
Figure 4-3: *LC* VCO; a) complementary cross-coupled schematic and b) equivalent small-signal circuit. 69
Figure 4-4: VCO output voltage amplitude V_{TANK} vs. bias current I_{VCO}. 71
Figure 4-5: Class B push-pull amplifier; a) schematic and b) waveforms. 74
Figure 4-6: *LC* VCO; a) complementary cross-coupled schematic and b) MOS switch model representation. 81
Figure 4-7: TX *LC* VCO; a) schematic and b) equivalent circuit of the antenna at 6.3 GHz. 82
Figure 4-8: Simulation; $P_{nmos}(t)$ with respect to T_{OSC}. 83
Figure 4-9: Simulation; P_{ANT}, P_{VCO_active} and $\eta_{P\text{-}VCO}$ with respect to gm. 84
Figure 4-10: Simulation; $I_{DS}(t)$ and $V_{DS}(t)$ of M_3. 85
Figure 4-11: Simulation; R_{ANT_diff}, R_{ANT} and Gm_{eff} with respect to antenna Q. 87
Figure 4-12: Simulation; P_{VCO}, P_{VCO_active}, P_{ANT} and $\eta_{P\text{-}VCO}$ with respect to antenna Q. 88
Figure 4-13: Simulation; $\eta_{P\text{-}VCO}$ with respect to antenna Q for different gm. 89
Figure 4-14: Simulation; imaginary part of the latch impedance over frequency. 91
Figure 4-15: Simulation; f_{OSC} as a function of V_{CNTRL}. 91
Figure 4-16: Simulation; f_{OSC} offset from 6.268 GHz as a function of V_{MOD}. 92
Figure 4-17: Simulation; phase noise as a function of f_{OSC} offset. 92
Figure 4-18: High-frequency low-power divider topology. 94
Figure 4-19: TSPC prescaler schematic. 94
Figure 4-20: Static CMOS prescaler gate-level schematic. 95
Figure 4-21: Tri-state PFD and D flip-flop schematic. 95
Figure 4-22: Single-ended CP schematic. 97
Figure 4-23: Simulation; I_{CP_OUT} as a function of output voltage. 98

Figure 4-24: PLL forward path. 98
Figure 4-25: Up down mux schematic. 99
Figure 4-26: Loop switch schematic. 100
Figure 4-27: Leakage buffer schematic. 101
Figure 4-28: Second order passive loop filter schematic. 102
Figure 4-29: PLL feedback path. 103
Figure 4-30: VCO buffer schematic. 104
Figure 4-31: Output buffer schematic. 104
Figure 4-32: Transmission gates TG_A and TG_B for testing. 105
Figure 5-1: TX block-level diagram with bond pads. 110
Figure 5-2: Simulation; locking and OL modulating the PLL ($\omega_{3dB} = 2\pi \cdot 215$ kHz). 112
Figure 5-3: Simulation; FM modulated (BFSK) VCO spectrum. 112
Figure 5-4: Simulation; open-loop voltage slope on V_{FILTER}. 115
Figure 5-5: Simulation; locking the PLL ($\omega_{3dB} = 2\pi \cdot 1.7$ MHz). 117
Figure 5-6: Noise suppression; a) system, b) circuit and c) device levels. 119
Figure 5-7: Layout of transmitter chip (without metal-fill). 120
Figure 5-8: Microphotograph of transmitter in 0.13 μm CMOS. 121
Figure 5-9: Photograph of Populated PCB with TX chip. 122
Figure 5-10: Measurement; PLL loop filter bandwidth. 123
Figure 5-11: Measurement; PLL transient step response on V_{CNTRL}. 124
Figure 5-12: Measurement; VCO phase noise as a function of f_{OSC} offset. 125
Figure 5-13: Measurement; I_{CP_OUT} as a function of output voltage. 126
Figure 5-14: Measurement; f_{OSC} as a function of V_{CNTRL}. 127
Figure 5-15: Measurement; f_{OSC} offset from 6.27784 GHz as a function of V_{CNTRL}. 128
Figure 5-16: Carrier drift measurement test-setup. 130
Figure 5-17: Measurement; carrier drift spectrum. 130
Figure 5-18: Measurement; Δf_{C_pos} as a function of T_{open_loop}. 131
Figure 5-19: Measurement; Δf_{C_neg} as a function of T_{open_loop}. 131
Figure 5-20: Measurement; TX FM modulated (BFSK) spectrum. 132
Figure 5-21: Inductance comparison (SE) of antenna model and measurement. 133

Figure 5-22: Q comparison (SE) of antenna model and measurement. 134
Figure 5-23: Anechoic chamber measurement test setup. 135
Figure 5-24: Measurement; received power from TX as a function of r_X. 135
Figure 5-25: Wired TX to RX test setup 137
Figure 5-26: Measurement; RX VCO spectrum – injection-locked to the FM signal.... 138
Figure 5-27: Measurement; TX input and RX output bitstreams at a rate of 2 kbps..... 138
Figure 5-28: P_{TX_avg} and η_{TX} comparison of published short-range transmitters. 142
Figure 5-29: Communication range estimate (revised). 143

List of Abbreviations and Symbols

ADC	Analog-to-Digital Converter
AHDL	Analog Hardware Description Language
AMOS	Accumulation Metal-Oxide-Semiconductor
BER	Bit Error Rate
BFSK	Binary Frequency Shift Keying
bps	bits per second
CAT	Computed Axial Tomography
CL	Closed-Loop
CMC	Canadian Microelectronics Corporation
CML	Common-Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
CP	Charge Pump
CPU	Central Processing Unit
ζ	damping factor
dBi	Decibels over Isotropic
DFT	Discrete Fourier Transform
DoE	Department of Electronics
EM	Electromagnetic
FM	Frequency Modulation
FSK	Frequency Shift Keying
HFSS	High Frequency Structure Simulator
IC	Integrated Circuit
ISM	Industrial, Scientific and Medical
LNA	Low Noise Amplifier
MA	top metal layer in IBM's CMOS 0.13μm technology
MEMS	Micro-Electro-Mechanical System
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor

NBFM	Narrowband Frequency Modulation
ω_{3dB}	loop bandwidth in radians
OL	Open-Loop
OOK	On-Off Keying
PCB	Printed-Circuit-Board
PFD	Phase-Frequency Detector
PSK	Phase-Shift Keying
PSRR	Power Supply Rejection Ratio
PLL	Phase-Locked Loop
PMOS	P-channel Metal-Oxide-Semiconductor
QAM	Quadrature Amplitude Modulation
RF	Radio-Frequency
RX	Receiver
SARS	Severe Acute Respiratory Syndrome
SAW	Surface Acoustic Wave
Σ-Δ	Sigma-Delta
SCL	Source-Coupled Logic
SE	single-ended
SoC	System-on-a-Chip
SOI	Silicon-on-Insulator
TSPC	True-Single-Phase-Clocking
TX	Transmitter
UNII	Unlicensed National Information Infrastructure
UWB	Ultra-wideband
VCO	Voltage Controlled Oscillator
V_{DD}	positive supply voltage
V_{SS}	negative supply voltage
λ	wavelength carrier frequency
WBAN	Wireless Body Area Network
WBFM	Wideband Frequency Modulation

WLAN	Wireless Local Area Network
WSN	Wireless Sensor Networks
Xtal	Quartz Piezoelectric Crystal Oscillator
Z	impedance

CHAPTER

1. Introduction

The application of engineering principles and techniques to the medical field is referred to as biomedical engineering – a multi-discipline field requiring the design and problem solving expertise of engineers with the medical expertise of physicians to help improve patient health care. A biomedical technology in development of interest is the area of non-intrusive, micro-sized and wireless sensors for the purpose of patient monitoring. The intent of this thesis is to develop, demonstrate and evaluate the techniques for low-power complementary metal-oxide semiconductor (CMOS) transmitter system integration for short-range radio-frequency communication. This would enable a revolutionary system-on-a-chip (SoC) solution for communication to-and-from biomedical sensors.

1.1. Motivation

The field of radiation dosimetry is to quantify the amount of energy that is absorbed in matter upon exposure to ionizing radiation. There are three different types of ionizing radiation [1]; the first type is charged particles such as alpha and beta particles, the second type is neutral particles such as neutrons, and the third type is electromagnetic radiation such as gamma rays and X-rays – this type is used for medical applications. Thomson & Nielsen Electronics Ltd. is a company which manufactures and markets metal-

oxide-semiconductor field effective transistors (MOSFET)s exclusively for electromagnetic radiation dosimetry. This dosimeter is used in a number of radiotherapy treatments such as total body irradiation, brachytherapy, intensity modulated radiation therapy and radiosurgery. This dosimeter is also used in a number of radiology diagnoses such as computed axial tomography (CAT) scans, fluoroscopy and mammography. The Thomson & Nielsen MOSFET dosimeter, photo shown in Figure 1-1 [2], has a very small form-factor (1 mm^2) such that it minimally interferes with the delivery of the radiation to the targeted tissue and can even be temporarily inserted in the patient's body.

In its current design, the MOSFET dosimeter is powered and communicates through wires obtrusive to the patient. A wireless readout of the dosimeter via a transceiver would result in less patient discomfort. The development of a wireless dosimeter is not easy however, as a battery powered device contains elements of high atomic mass numbers (in the battery) which could scatter the radiation to sensitive and/or healthy areas of the patient's tissue. Also, the form-factor of a wireless dosimeter would increase with the addition of an off-chip antenna, potentially making the sensor too intrusive for the treatment. Thus, to feasibly develop a wireless dosimeter, the solution must address the discussed power source and form-factor constraints.

The most common symptom of severe acute respiratory syndrome (SARS) is a fever of more than 38°C. A wireless readout of a bandage-type thermometer sensor via a transceiver would allow medical care workers to monitor potential SARS infected patients without direct physical contact. The feasibility of developing a wireless thermometer is dependent on reducing the system cost to be economical and therefore disposable.

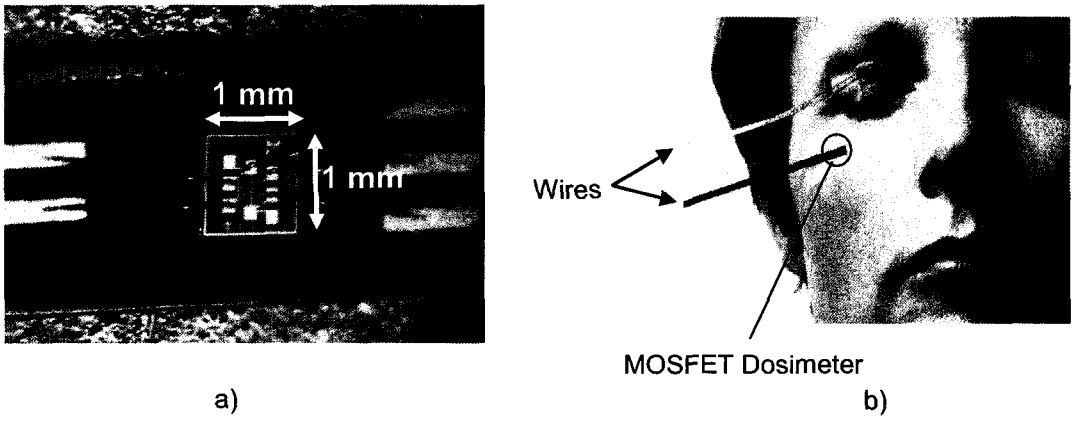

Figure 1-1: Thomson & Nielsen Electronics; a) MOSFET dosimeter sensor and b) patient with "wired" sensors.

1.1.1. Wireless Biomedical Sensor System

An illustration of a wireless biomedical sensor system is shown in Figure 1-2, composed of a sensor, transceiver integrated circuit (IC), power source and antenna. The sensor is a biomedical transducer which responds to a physical stimulus, such as ionizing radiation in the case of a dosimeter or body heat in the case of a thermometer, and generates a corresponding electrical signal. Depending on the type of sensor, it could be on-chip (i.e. integrated) or off-chip. The transceiver generally consists of an analog radio frequency (RF) front-end for communication as well as the digital back-end for baseband signal processing. The transceiver front-end contains a transmitter (TX) and a receiver (RX). The transceiver IC is normally powered by an off-chip power source.

The communication link with a wireless biomedical sensor system is quite different from that of a cellular network or wireless local area network (WLAN). For example, the link is highly asymmetric as the sensor is mainly transmitting the digitized and encoded data rather than receiving. The raw sensor information is digitized into packets of 100's to 1000's of bits in length, and due to the low rates of event stimulus, the packet rate of transmission is relatively low – typically, one packet per second. Another point of

distinction with other links is that the transmission distance is very short, 10 m or less, meaning lower carrier power is radiated by the antenna for communication.

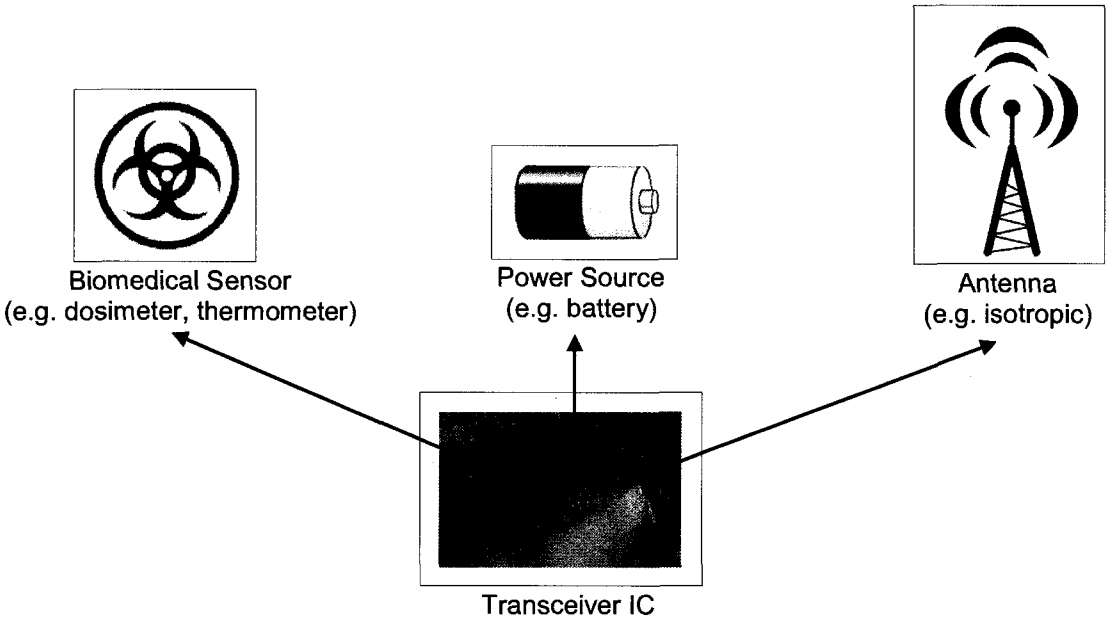

Figure 1-2: Wireless biomedical sensor system.

1.2. SoC Challenges Overview

A completely-integrated SoC transceiver solution for a wireless biomedical sensor would have revolutionary benefits for patient-care as in wireless dosimetry and thermometry, to give but two potential applications. The development of such a solution requires the integration of the off-chip components in Figure 1-2, namely the biomedical sensor, power source and antenna. For this SoC to be economically feasible requires using the lowest cost fabrication, packaging and assembling technologies, high integration to minimize the number of off-chip components, using inexpensive (if needed) external components, small die area, and a large volume production with a high manufacturing yield [23].

1.2.1. Biomedical Sensor

Biomedical sensors can be implemented using a number of different materials and manufacturing techniques; many however are fabricated in silicon using a micromachining process because of the economies of scale, the ready availability of highly accurate processing and the ability to incorporate electronics around the sensor. There are a number of potential advantages with integrating the sensor with circuits which can perform basic signal conditioning such as buffering, amplifying and multiplexing. These advantages include improved sensor sensitivity, temperature compensation, lower cost, easier A/D conversion, improved readability and a smaller system form-factor. Typically, the integrated sensor is fabricated with post-processing techniques. This can be challenging as the post-processing must not damage any of the existing devices or interconnects on the IC.

The sensor developed by Thomson & Nielsen Electronics Ltd. for medical dosimetry is in fact a MOSFET (sometimes called RADFET [3, 4]) whose gate oxide is affected by the absorption of radiation, which in turn causes a permanent change in the threshold voltage. The difference in the threshold voltage before and after exposure is proportional to the absorbed dose. As a MOSFET, this sensor could conceivably be incorporated on-chip with any mainstream CMOS semiconductor manufacturing technology.

1.2.2. Power Source

The energy sources for powering the integrated circuit (and the sensor) are classified into two categories; energy storage devices (such as batteries and ultracapacitors) and energy scavenging devices (such as solar cells, vibration, air flow converters, RF and inductive coupling). The differing characteristics between the two categories are that the performance of energy storage devices is independent of the operating environment and the cycle-life of energy scavenging devices is longer.

Thin-film ultracapacitors, where electric energy is stored in an electrochemical double layer (Helmholtz Layer) formed at the interface between a solid electrode material surface and a liquid electrolyte in the micropores of the electrode, has the potential to meet the power supply requirements of low-powered integrated circuits. A typical 100 μm thick nanostructure electrode device can generate up to 1 F/cm^2 [5] and can be manufactured on-top of an IC. The recharging of the ultracapacitor could be accomplished with a solar cell – typical power densities of 10 $\mu W/cm^2$ and 15 mW/cm^2 are obtainable in indoor and outdoor environments, respectively [6]. With the combining of both energy storage and energy scavenging devices, a hybrid power solution such as this could have a performance independent of the operating environment and a long cycle-life.

1.2.3. Antenna

Antennas for wireless communication are categorized in terms of their respective radiation pattern – a 3-dimensional spatial distribution of radiated energy as a function of an observer's position along a path or surface of constant radius [19]. An antenna which radiates energy equally in all directions (and is also lossless) is defined as an isotropic antenna. A directional antenna is defined as one which radiates (or receives) energy more effectively in one (or more) particular direction(s). A subclass of this type is an omni-directional antenna, and it is defined as one which has a non-directional radiation pattern in a given plane but a directional radiation pattern in any orthogonal plane.

As the isotropic antenna is a hypothetical model, the omni-directional antenna would be best suited for a biomedical sensor system application since the location of the reader is not generally known at the time of communication. For good radiation efficiency, the required dimensions of the antenna should be around $\lambda/4$ to $\lambda/2$ in size, where λ is the wavelength of the radiated carrier frequency.

For very short communication distances (less than 1 m), previous research in [7] and [8] have demonstrated successful use of inductive integrated antennas on high resistivity silicon substrates. The use of an integrated structure possessing the combined

properties of an antenna and an inductor is well suited to meet the small form-factor requirements of a wireless dosimeter or thermometer. However, the operating wavelength must be short enough to implement small inductive antennas with dimensions economically feasible for silicon integration.

1.3. Thesis Objectives

The main functions of a transmitter are to modulate data onto a high-frequency carrier and then broadcast the carrier via an antenna with enough power to establish a wireless communication link with a receiver. The discussion of system integration revealed three main specifications for an SoC transmitter design; (1) minimize the system's power consumption as well as its energy consumption to maximize the cycle-life of the power source, (2) reduce the system cost to be economical and therefore disposable, and (3) minimize the system form-factor for seamless, and non-intrusive, integration with the physical environment. Thus, in investigating an SoC solution for wireless biomedical sensor applications through "on-chip" antenna integration, the choices for the transmitter's architecture, the carrier frequency, the reduction of power consumption and the improvement of energy conservation are important. In this thesis, design techniques are developed, demonstrated and evaluated to meet the abovementioned specifications.

1.4. Thesis Contributions

This thesis presents the following scientific and engineering contributions:

1. A 6.3 GHz SoC transmitter design incorporating the integrated small-loop antenna. The transmitter is implemented in a 1.2 V 0.13 μm CMOS process and occupies an area of 2 mm^2. Making use of an integrated antenna to communicate, this transmitter chip is therefore revolutionary in that it is the first SoC and the smallest transmitter to operate at the 6-GHz frequency band. The transmitter features a phase-locked loop (PLL) - based modulator design with closed-loop and

open-loop operation modes to accurately define and frequency modulate (FM) the carrier of an oscillator, respectively. Active power consumption of the modulator is reduced such that the transmitter can be powered by an on-chip ultracapacitor and solar cell combination for wireless dosimetry applications.

2. A measurement and evaluation of the SoC transmitter which achieves relatively good efficiency and low average power consumption when compared to other known published transmitters. This is accomplished in spite of the fact that the SoC transmitter operates at a multi-gigahertz band and communicates with a lossy integrated antenna.

3. A complementary *LC* voltage-controlled oscillator (VCO) design procedure for achieving optimum oscillator power efficiency performance with respect to the inductive antenna that is incorporated into the VCO's resonant tank. This procedure amends the "simultaneous *gm* and impedance matching" design technique of [55] to also attain "power optimization".

4. A demonstration of the feasibility of an integrated small-loop antenna which radiates sufficient far field energy at 6.3 GHz for short-range communication. The integrated antenna, designed from [9] and [10], is to the author's knowledge, the first small-loop antenna to be integrated without costly post-processing techniques in a mainstream CMOS process having a low-resistivity substrate. The integrated antenna, which occupies 0.6 mm^2 of chip area, is also believed to be the smallest reported active antenna operating in the 6-GHz band.

5. A communication link analysis of a short-range SoC transceiver architecture – comprised of an injection-locked receiver and an oscillator transmitter, which communicates over a 6.3 GHz carrier using FM modulation, according to binary frequency shift keying (binary FSK or BFSK), with an integrated antenna. The analysis highlights the dynamic relationship between the communication range, data rate, and receiver injection-locking bandwidth.

1.4.1. Research Collaboration

The research presented in this thesis is part of a collaborative effort in the development of a completely-integrated SoC transceiver solution for biomedical sensor applications. As previously mentioned, an application example is a short-range self-powered wireless dosimeter – a proposed architecture of the chip is illustrated in Figure 1-3. The system's behaviour is described as follows: The integrated dosimeter operates as a transducer, responding to ionizing radiation by generating a corresponding electrical signal. The analog-to-digital converter (ADC) block converts this signal into digital data bits. Next, the central processing unit (CPU) block collects, stores and processes these bits, and then encodes the data for bandwidth efficient communication and error-control. The encoded data is fed to the TX. The TX modulates the encoded data onto a high-frequency carrier which is then transmitted via an integrated antenna. Alternatively, the RX demodulates encoded instructions on an incoming carrier from the antenna. The instructions are decoded by the central processing unit (CPU) to be acted upon. The CPU & controller block manages the active and sleep states of the transceiver. The entire system is to be powered by a thin-film ultracapacitor and a solar cell which serves as a trickle charger between packet communications. This hybrid power solution can be manufactured on top of the chip and would not contain elements of high atomic mass numbers (unlike a battery) which could scatter the radiation during medical treatment or diagnosis. A voltage regulator is required to maintain the power supply rail to the rated voltage level for the technology. It is advantageous that the SoC transceiver is implemented in a submicron semiconductor process, which features devices with a thin gate oxide. This would minimize the susceptibility of these devices to threshold changes as less ionizing radiation will be absorbed in the oxide.

The transceiver's front-end, bolded in blue in Figure 1-3, is the design responsibility of three Carleton Ph.D. candidates, Peter Popplewell, Atif Shamim and the author of this thesis. There is some design reuse practiced among the designers, as certain sections of the transmitter are identical to that of the receiver, and this thesis will give credit

where credit is deserved. The conclusions from this collaborative effort are expected to lead to important advancements in short-range radio-frequency transceiver system integration.

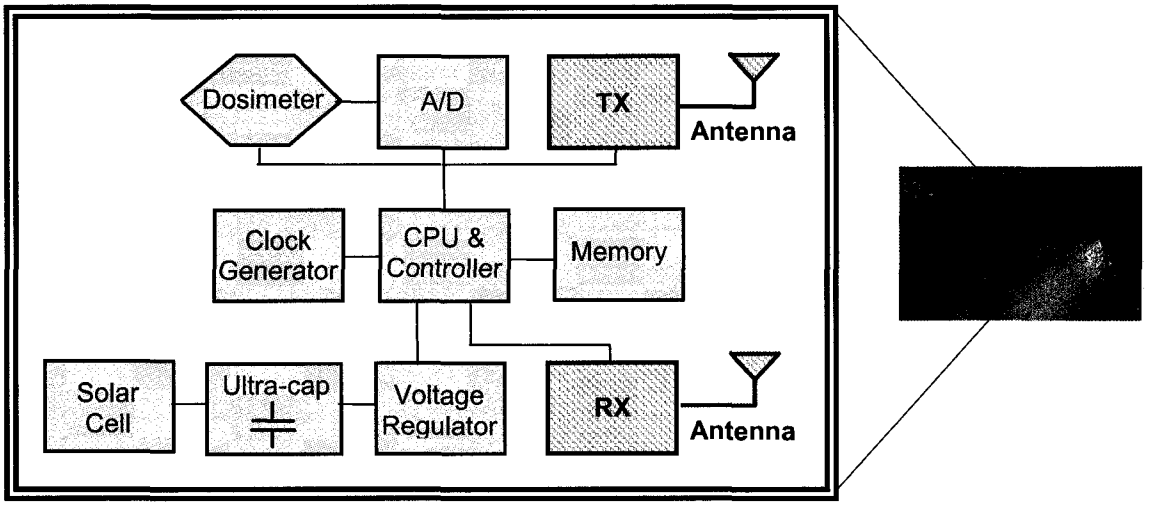

Figure 1-3: SoC transceiver architecture for wireless dosimetry.

1.5. Thesis Organization

This thesis is comprised of six chapters.

Chapter 2 will review the fundamentals of antenna, transmitter and power source design for a low-power and energy-efficient SoC transmitter, highlighting the various design choices and associated trade-offs.

Chapter 3 will present the process technology, the carrier frequency, the integrated antenna structure and the transceiver front-end architecture – in particular, the transmitter circuit which interfaces with the antenna, to realize a completely-integrated SoC solution for wireless biomedical sensors. A system analysis of the transceiver front-end communication link will also be explored.

Chapter 4 will present the transmitter architecture, and then will briefly explain its operation modes for low-power and energy-efficient communication. Circuit-level design details of the transmitter will also be presented.

Chapter 5 will focus on the transmitter prototype chip, presenting simulation results, an implementation methodology and then measurement results. This will be followed by a post-analysis of the transmitter's performance and then a discussion of the SoC transceiver front-end communication link.

Finally, Chapter 6 will provide a summary of this thesis, a list of thesis contributions, a list of publications from this research, and future work.

CHAPTER

2. SoC Transmitter Design Considerations

This chapter explores the fundamentals of antenna, transmitter and power source design for an SoC transmitter.

2.1. Antenna Fundamentals

2.1.1. Characteristics

In a transmitter, the antenna transforms a guided electromagnetic signal into an electromagnetic wave that propagates in the transmission medium. The transformation is achieved by exciting both the electrical and magnetic fields in the antenna's immediate surroundings – an area known as the near field [11].

The oscillating electrical and magnetic fields generate an electromagnetic (EM) wave whose propagation speed c is dependent on the relative dielectric constant ε_r and the relative permeability μ_r of the transmission medium, and is expressed by

$$c = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}} \tag{2.1}$$

where c_0 is the speed of light in free space, 3×10^8 m/s. The wavelength of the electromagnetic wave λ of an electrical signal of frequency f is given by the formula

$$\lambda = \frac{c}{f}. \tag{2.2}$$

The area where the antenna's electromagnetic wave is generated is divided into three regions [11, 19]; (1) the reactive near field, (2) the radiating near field and (3) the far field. The reactive near field is the portion of the antenna's near field where power is not only radiated outwards but a reactive power component circulates between the reactive near field and the power source, an external matching network, or both. Therefore, any variations in the electrical properties or magnetic properties will affect the antenna's input impedance. The outer boundary of the reactive near field $R_{reactive}$ is approximately a distance of

$$R_{reactive} \approx \frac{\lambda}{2\pi} \tag{2.3}$$

from the antenna. The radiating near field is the portion of the near field region, between the far field and the reactive portion of the near field region, wherein the angular distribution of the radiating field's intensity is dependent on the distance from the antenna. If the antenna is large compared to the wavelength of the EM wave, the radiating near field's $R_{radiating}$ outer boundary is approximately

$$R_{radiating} \approx \frac{2D^2}{\lambda} \tag{2.4}$$

where D is the largest dimension of the antenna. For an electrically small antenna, a radiating near field typically does not exist, and therefore the reactive near field transforms directly to the far field. The far field is the region where the angular distribution of radiating field's intensity is essentially independent of the distance from the antenna.

The radiation pattern can be described with the help of the spherical co-ordinate system shown in Figure 2-1, where the antenna is placed at the origin and radiates though an elemental (spherical) area *ds* at a range *r*. The z axis is assigned to be vertical and the x-y plane is assigned to be horizontal. The angle θ denotes the elevation angle and the angle φ denotes the azimuthal angle. For $\varphi = 0°$, the x-z plane is referred to as the eleva-

tion plane. For $\theta = 90°$, the x-y plane is referred to as the azimuthal (or horizontal) plane. The element $d\Omega = sin\theta\, d\varphi\, d\theta$ is that of a solid angle, and describes a 3-dimensional angle that, from the point of view of the center of a sphere, includes a given area on the surface of that sphere.

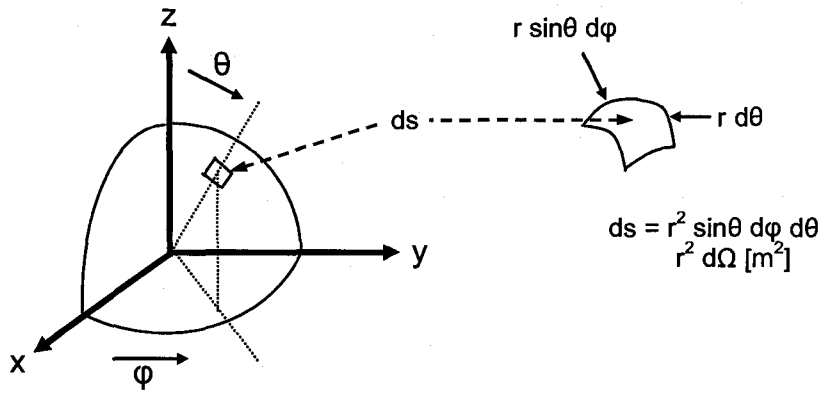

Figure 2-1: Spherical co-ordinate system.

The radiated electromagnetic wave in the far field region is a transverse wave, meaning the electric and the magnetic field vectors are orthogonal to the direction of propagation and also orthogonal to each other. The polarization of an antenna is the orientation of the electric field of the radiated wave with respect to the Earth's surface and is determined by the antenna's physical structure and orientation [12]. The type of polarization is described by the geometric figure traced by the wave's electric field vector (summation of field components) upon a stationary and impeding plane perpendicular to the direction of propagation. The different polarization types include linear (horizontal, vertical and neither), circular (right-hand and left-hand) and elliptical (right-hand and left-hand).

Consider Figure 2-2 where an electric field vector of an EM wave $\mathbf{E_{TOTAL}}$ is travelling in the z-direction and has two field components, $\mathbf{E_1}$ pointing in the x-direction and $\mathbf{E_2}$ pointing in the y-direction, which have the same phase. The figure traced by the propagating electric field vector is a line, hence termed linear polarization. It is also

called horizontal linear polarization if this line is parallel to the Earth's surface or vertical linear polarization if this line is perpendicular to the Earth's surface. Circular polarization occurs if the two field components, $\mathbf{E_1}$ and $\mathbf{E_2}$, had the same magnitude but a 90° phase difference. This type of trace-figure is illustrated in Figure 2-3 a) and is also described as right-hand polarization if the electrical field vector $\mathbf{E_{TOTAL}}$ rotates clockwise while propagating; otherwise it is described as left-hand polarization due to a counter-clockwise rotation. Elliptical polarization occurs if $\mathbf{E_1}$ and $\mathbf{E_2}$ have different magnitudes and are out of phase, but not necessarily by 90° or 0°, with respect to each other. This type of trace-figure is illustrated in Figure 2-3 b) and is also described as right-hand polarization when $\mathbf{E_{TOTAL}}$ rotates clockwise while propagating; left-hand polarization otherwise.

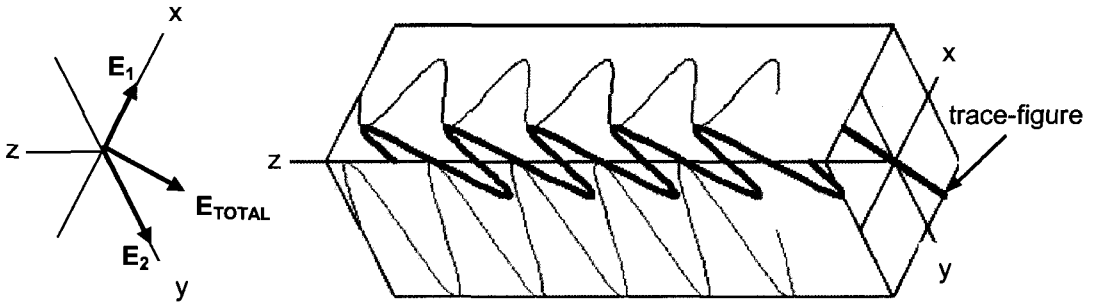

Figure 2-2: Linear polarization; a) E-field vectors and b) trace figure.

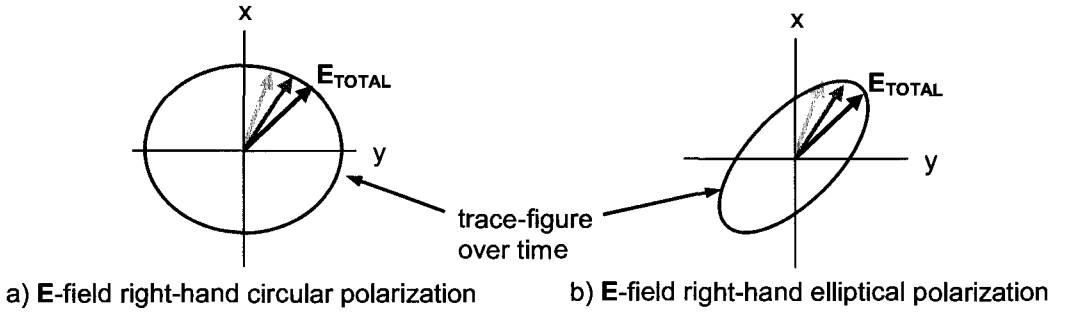

Figure 2-3: Circular and elliptical polarization; a) circular trace figure and b) elliptical trace figure.

In a wireless system, the optimal performance for a communication link occurs when the polarization of the transmitter antenna and the receiver antenna are identical (and parallel) to each other [11]. The link's performance would experience a 3 dB loss if, however, one antenna exhibits linear polarization while the other exhibits circular polarization. If both antennas exhibit linear polarization but their polarization is orthogonal with respect to one another, as in the case of vertical and horizontal linear polarization, the link should theoretically fail as none of the radiated power is received. The same outcome would occur if one antenna exhibits right-hand circular polarization while the other exhibits left-hand circular polarization. In an indoor (and sometimes outdoor) environment, the radiated wave may experience reflections causing its polarization to change and be difficult to predict. In a wireless system involving a portable antenna, it is prudent to have the polarization linear for one antenna and circular for the other antenna. This would avoid the situation of possible link failure from polarization misalignment or mismatch.

2.1.2. Performance Metrics

The average radiated power density associated with an electromagnetic wave is represented by the time average Poynting vector S_{avg} [19] and is defined by

$$S_{avg} = \frac{1}{2}\mathrm{Re}\left[\mathbf{E}\times\mathbf{H}^*\right] \quad [\mathrm{W/m^2}] \tag{2.5}$$

where **E** and **H** are phasor representations of time varying electric and magnetic fields, respectively. The average power radiated by an antenna P_{RAD}, also referred to as the radiated power, is found by integrating the radial component of the Poynting vector S_{radial} over a closed surface, usually a sphere, and is expressed by

$$P_{RAD} = \frac{1}{2}\oiint S_{radial}\cdot ds = \frac{1}{2}\oiint \mathrm{Re}\left[\mathbf{E}\times\mathbf{H}^*\right]\cdot ds \quad [\mathrm{W}] \tag{2.6}$$

where ds is the vector differential surface and equal to $r^2 d\Omega\ \hat{r}$. The radiation intensity U in a given direction is defined as the power radiated from an antenna per unit solid angle and is given by

$$U = r^2 \cdot S_{radial} \quad [\text{W}/\Omega]. \tag{2.7}$$

The average radiated power of an antenna can also be found by integrating the radiation intensity over the entire solid angle of 4π, this is expressed by

$$P_{RAD} = \oiint_{\Omega} U\, d\Omega \tag{2.8}$$

where $d\Omega$ is the solid angle element.

The radiation pattern of an antenna is the spatial distribution of the field intensity over θ and φ for a fixed r, characterizing the electromagnetic field generated by the antenna. A common reference with which to compare the performance of other antennas is the isotropic radiator. An isotropic antenna is an ideal source which radiates equally in all directions, generating a sphere-like radiation pattern. The isotropic antenna's radiation intensity U_0 [19] will be independent of angles θ and φ, and the radiated power is evaluated as

$$P_{RAD} = \oiint_{\Omega} U_0 d\Omega = U_0 \oiint_{\Omega} d\Omega = 4\pi U_0 \tag{2.9}$$

In terms of radiated power, the radiation intensity of an isotropic antenna is thus given by

$$U_0 = \frac{P_{RAD}}{4\pi}. \tag{2.10}$$

The directivity D of an antenna is a ratio of the antenna's maximum radiation intensity U_{max} to its radiation intensity averaged over all directions [19]. The average radiation intensity U_{avg} is the power radiated divided by 4π, and thus $U_{avg} = U_0$. In other words, directivity indicates how many times the antenna's maximum radiation intensity (power per unit solid angle) is greater than that of an isotropic radiator (radiation intensity averaged over a sphere), and is given by

$$D = \frac{U_{\max}}{U_0} = \frac{4\pi U_{\max}}{P_{RAD}}. \tag{2.11}$$

Directivity is a dimensionless quantity, and is usually expressed in dBi (decibels over isotropic).

The input impedance of an antenna Z_{ANT} is comprised of a resistance R_{ANT} in series with a reactance X_{ANT}, and is expressed by

$$Z_{ANT} = R_{ANT} + jX_{ANT}. \tag{2.12}$$

The antenna's resistance normally consists of two parts and is given by

$$R_{ANT} = R_{RAD} + R_{LOSS} \tag{2.13}$$

where R_{RAD} is the radiation resistance and R_{LOSS} is the loss resistance. The radiation resistance is associated with the power actually radiated by the antenna whereas the loss resistance is associated with the power dissipated as heat due to dielectric or conduction losses in the antenna. The antenna's reactance normally is composed of the capacitive C_{ANT} and inductive L_{ANT} elements. Figure 2-4 depicts the antenna's series equivalent circuit as seen by a voltage source V_S having an internal impedance given by

$$Z_S = R_S + jX_S \tag{2.14}$$

where R_S is the source resistance and X_S is the source reactance. The voltage source and internal impedance are representing a transmitter's (TX)'s driving ability and output impedance, respectively. The power transfer from the voltage source to the antenna is maximized when the internal impedance Z_S is a complex conjugate of the antenna's input impedance Z_{ANT}, analytically this means

$$R_S = R_{RAD} + R_{LOSS} \text{ and } X_S = -X_{ANT}. \tag{2.15) and (2.16}$$

With conjugate matching, the power supplied by the voltage source P_{VS}, having a peak voltage V_S, is given by

$$P_{VS} = \frac{|V_S|^2}{4}\left[\frac{1}{R_{RAD} + R_{LOSS}}\right], \tag{2.17}$$

of which half is dissipated as heat P_S in the internal resistance R_S and the other half, denoted by P_{ANT}, is delivered to the antenna resistance R_{ANT}. Thus, the power available to the antenna from the source P_{AVS} is given by

$$P_{AVS} = \frac{|V_S|^2}{8}\left[\frac{1}{R_s}\right], \tag{2.18}$$

which is equal to the power delivered to the antenna P_{ANT} [19].

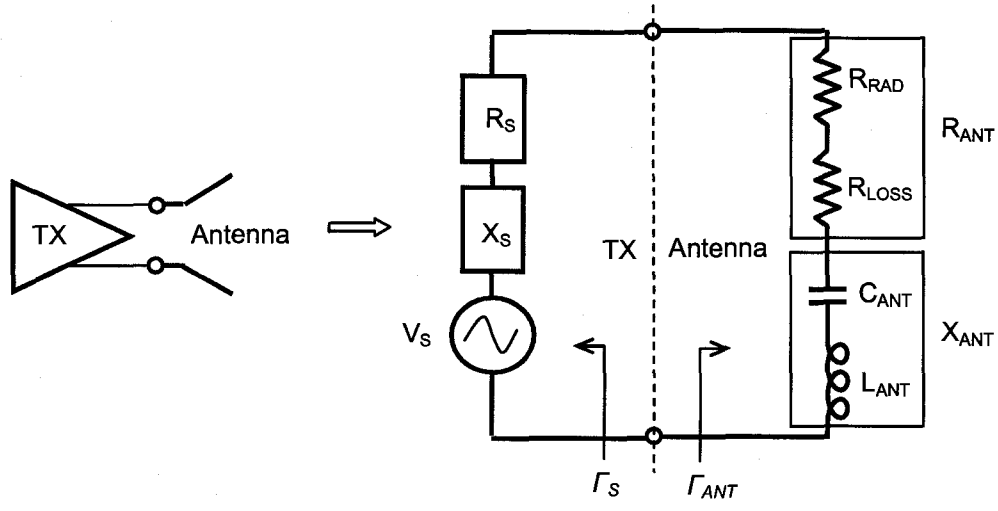

Figure 2-4: Antenna equivalent circuit.

The efficiency of an antenna e_{ANT} is a scalar composed of two parts; to account for 1) impedance mismatch losses at the input terminals of the antenna and 2) heat losses within the antenna. When the antenna's input impedance (Z_{ANT}) is not matched to the transmitter's output impedance (Z_S), part of the power supplied by the transmitter is reflected back rather than delivered to the antenna. The portion of power which is actually delivered to the load can be determined from the source reflection coefficient Γ_s and antenna reflection coefficient Γ_{ANT} – these reflection coefficients are given by

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \text{ and } \Gamma_{ANT} = \frac{Z_{ANT} - Z_0}{Z_{ANT} + Z_0}, \tag{2.19) and (2.20}$$

respectively, where Z_0 is the characteristic impedance reference. The reflection (or mismatch) efficiency e_R is the fraction of power not reflected (i.e. delivered to the antenna) [13] and is given by

$$e_R = \frac{(1-|\Gamma_S|^2)(1-|\Gamma_{ANT}|^2)}{|1-\Gamma_S\Gamma_{ANT}|^2}. \tag{2.21}$$

Thus, the actual power delivered to the antenna is given by

$$P_{ANT} = e_R \cdot P_{AVS}. \tag{2.22}$$

In the case of complex conjugate matching; $\Gamma_{ANT} = \Gamma_S^*$ and $e_R = 1$. This yields $P_{ANT} = P_{AVS}$ as expected. In the case of a purely resistive source impedance, i.e. $R_S = Z_0$, then $\Gamma_S = 0$ and $e_R = 1 - |\Gamma_{ANT}|^2$. The radiation efficiency e_{RAD} is the fraction of power radiated by the antenna (P_{RAD}) to the power delivered to the antenna (P_{ANT}) [19], and is given by

$$e_{RAD} = \frac{R_{RAD}}{R_{RAD} + R_{LOSS}}, \tag{2.23}$$

and thus $P_{RAD} = e_{RAD} \cdot P_{ANT}$. The overall efficiency of an antenna is therefore expressed by

$$e_{ANT} = e_R \cdot e_{RAD}, \tag{2.24}$$

and thus the radiated power as a function of the available source power is given by

$$P_{RAD} = e_{ANT} \cdot P_{AVS} \tag{2.25}$$

for an antenna.

The discussed power transfer from source to antenna is illustrated in Figure 2-5 to highlight the associations. P_{ANT} is also labeled P_{TX} when referring to the power delivered to the transmitter's antenna and, alternatively, P_{RX} when referring to the power delivered to (or captured by) the receiver's antenna.

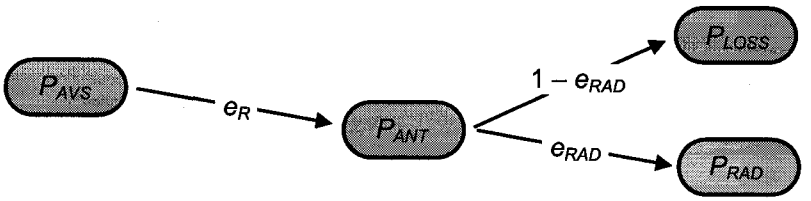

Figure 2-5: Antenna power transfer associations.

The gain of an antenna G is a ratio of the antenna's maximum radiation intensity to the radiation intensity of an isotropic antenna when the power delivered (accepted) by both antennas is P_{ANT}. As an isotropic antenna is lossless, the power delivered is equal to the power radiated (P_{RAD}) in evaluating its radiation intensity. The gain of an antenna [19] is therefore given by

$$G = \frac{U_{\max}}{U_0 \mid_{P_{RAD}=P_{ANT}}} = \frac{4\pi U_{\max}}{P_{ANT}}. \tag{2.26}$$

Antenna gain can be expressed as a function of directivity by the radiation efficiency as

$$G = \frac{4\pi U_{\max}}{P_{ANT}} = \frac{4\pi U_{\max}}{P_{RAD}/e_{RAD}} = e_{RAD} \cdot D. \tag{2.27}$$

Gain is a dimensionless quantity, and is usually expressed in dBi.

The effective area of an antenna A_{EFF} is defined (in a given direction) as the ratio of available power at the receiver's antenna terminals to the power flux density of an incident and polarization matched plane wave (from that direction) [19]. The power flux density is equal to the radiation intensity in the far-field region. The maximum effective area A_{EFF_max} of an antenna represents its power collecting capability when it is lossless and conjugately matched to the load for maximum power transfer, thus

$$A_{EFF} = e_{RAD} \cdot A_{EFF\_\max}. \tag{2.28}$$

The maximum effective area of an antenna is related to its directivity by

$$A_{EFF\_\max} = \frac{\lambda^2}{4\pi} D. \tag{2.29}$$

Therefore, antenna gain is a function of an antenna's effective area as

$$A_{EFF} = e_{RAD} \cdot A_{EFF\_max} = e_{RAD} \frac{\lambda^2}{4\pi} D = \frac{\lambda^2}{4\pi} G \tag{2.30}$$

with the substitution of (2.27).

2.1.3. Structures

There exist a number of different antenna structures, each having unique features which make them more suitable for certain applications. This subsection will describe three of the most common antennas for short-range communication, namely the half-wave dipole, the quarter-wave monopole and the loop antenna. The short-dipole is also mentioned.

The half-wave dipole antenna is formed by two conductors whose total end-to-end length is half the wavelength of the antenna's resonant frequency [11]. At this frequency, an RF carrier is fed differentially across the structure's centre as shown in Figure 2-6 a). As the half-wave dipole is symmetric around its axis, the generated radiation pattern is similarly symmetrical. Figure 2-6 b) shows this structure's radiation pattern. In the plane of the structure's axis, maximal radiation occurs at positions perpendicular to the axis and zero radiation occurs at positions in the direction of the axis. This directivity yields an antenna gain of 2.15 dBi for the half-wave dipole in the direction of maximum radiation, defining the antenna's boresight. The polarization of the radiated electromagnetic wave is linear (and horizontal if the x-y plane defines the earth's surface).

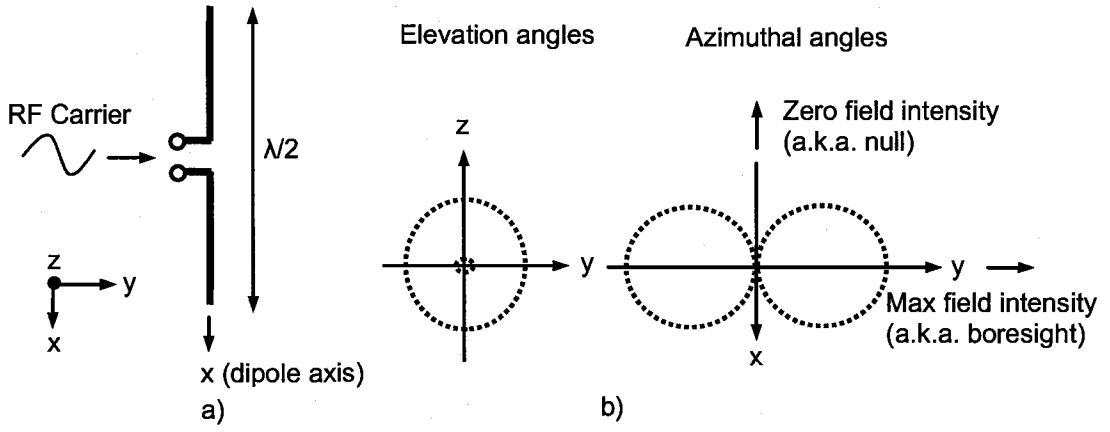

Figure 2-6: Half-wave dipole antenna; a) physical structure and b) radiation pattern.

The quarter-wave monopole antenna is formed by replacing one of the conductors in the dipole with an infinitely large ground plane perpendicular to the remaining conductor's axis. The ground plane acts as a mirror, creating an image of the "missing quarter-wave conductor". This results in a radiation pattern similar to the dipole except that radiation occurs only above the ground plane. With all the power being radiated above the ground plane, the monopole has 3 dB more gain than the half-wave dipole at the maximal radiation points. The monopole antenna is driven by a single-ended RF carrier signal and exhibits linear polarization (vertical if the ground plane is parallel to the earth's surface).

The loop antenna is formed by a conductor curved in the shape of a circle (or rectangle) whose ends are driven differentially by an RF carrier. The gain of the loop antenna is generally from –2 dBi to 3 dBi. If the circumference of this structure is electrically small, less than $0.1 \cdot \lambda$ as shown in Figure 2-7 a), it is considered a "small loop" antenna [19]. The radiation pattern of a small-loop antenna, shown in Figure 2-7 b), is similar to the dipole. Alternatively, when the circumference of the antenna is comparable to the wavelength of the carrier, the antenna is considered a "large loop" antenna, which has a different radiation pattern orientation as seen in Figure 2-8 b). Here, the large-loop antenna exhibits a non-directional pattern in the y-z plane and a broad double lobe pattern

in the x-y plane. In the latter plane, the lobes are in the directions perpendicular to the side containing the feed, while the nulls are in the directions parallel to the feed side. The polarization of the EM wave radiated from a loop antenna is linear (and horizontal if the x-y plane defines the earth's surface).

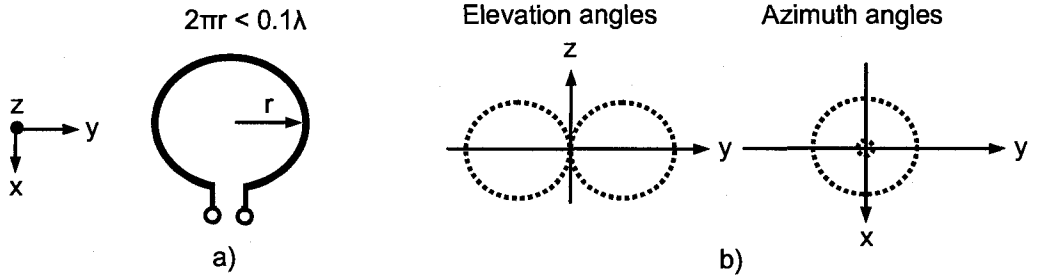

Figure 2-7: Small-loop antenna; a) physical structure and b) radiation pattern.

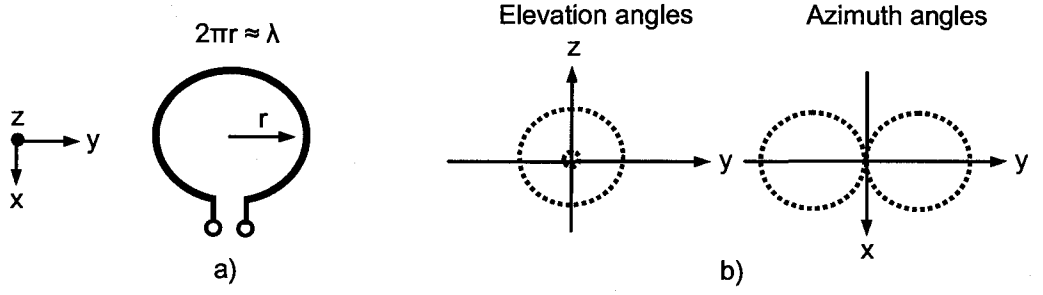

Figure 2-8: Large-loop antenna; a) physical structure and b) radiation pattern.

Dipole and monopole antennas can also be shorter than half-wavelength or quarter-wavelength structures, respectively. For instance, a Hertzian (or short) dipole is a dipole antenna whose length is significantly smaller than the wavelength by about $\lambda/10$ [14]. The radiation resistance of the Hertzian dipole is normally much smaller than the antenna's total real resistance. Thus, this antenna suffers from very poor radiation efficiency. The Hertzian dipole's imaginary impedance is typically capacitive, requiring high voltages relative to current for antenna excitement. This renders the Hertzian dipole impractical for most portable wireless applications which have low voltage power sources.

2.1.4. Integration

The antenna is normally an off-chip component which can be integrated to minimize the form-factor of a wireless system – an important requirement for a wireless dosimeter design, and to reduce the bill of materials. Antenna integration is economically feasible in CMOS when the wavelength of the carrier frequency is small enough to implement certain millimetre-sized antenna structures. The antenna structure which occupies a small physical area is the small-loop antenna. This structure is implemented for a 300 MHz carrier by researchers in [32]. Here, the dielectrically suspended loop antenna is implemented using a micro-machined silicon platform mounted on a glass back-plate for mechanical support and occupies an area of 25 mm^2. This antenna also served as the inductor in the oscillator transmitter's resonant tank. Further antenna miniaturization is possible as seen in [7] where an integrated 1 mm^2 squared loop antenna is presented for operation at 330 MHz and supporting a 10 cm communication link. This antenna is fabricated with a custom silicon process, and the structure is implemented on a high-resistivity silicon substrate ($\varepsilon_{rHR} = 11.7$) with a spin-on-glass insulating layer ($\varepsilon_{rSoG} = 3.1$) to reduce the attenuation of the signals and improve the loop's inductance and quality factor.

Integrated monopole and dipole antenna structures have been reported in [15], [16] and [17]. The monopole in [15], measuring 900 μm by 920 μm, is implemented on a silicon wafer having a resistivity of 10 Ω-cm with an additional 1.5 μm oxide grown on the substrate to increase RF isolation of the antenna. At 40 GHz, this monopole exhibited a maximum gain of –6 dBi but with a non-uniform radiation pattern having many lobes. An ion-implantation technique is used on the wafer to increase its resistivity to 10^6 Ω-cm. The antenna's gain displayed an improvement of 9 dB but still exhibited the same radiation pattern characteristics. The dipole in [16], measuring 380 μm by 620 μm, is also implemented on a high resistivity silicon substrate but achieves a gain of –3 dBi at 77 GHz. Alternatively, the dipole in [17] is implemented in a low 10 Ω-cm resistivity substrate from fabrication with standard CMOS processing techniques. This dipole, measuring 100 μm by 1500 μm, exhibits a gain of –8 dBi at 24 GHz with a dipole-like radiation

pattern. In terms of antenna performance, the work in [17] demonstrates the practical feasibility of antenna integration in a CMOS process.

To economically implement an antenna in a mainstream submicron CMOS process, the operating wavelength should be that of a multi-gigahertz (or higher) carrier frequency. In addition, the antenna should be fabricated with the metal layers readily available to the process, thus avoiding the extra costs associated with post-processing. This entails implementing the antenna with either aluminium or copper in silicon dioxide (ε_{rSiO2} = 4) on a low resistivity silicon substrate (ε_{rLR} = 12). For an estimate of the relative dielectric constant experienced by the electromagnetic wave generated from such an antenna, it is assumed the transmission medium is completely uniform and comprised of a material with ε_{r_avg} = 8, the average of ε_{rLR} and ε_{rSiO2}. Table 1 shows the expected circumference of an antenna needed to satisfy the small-loop criteria (of $0.1 \cdot \lambda_{on\text{-}chip}$) in silicon for selected Industrial, Scientific and Medical (ISM) and Unlicensed National Information Infrastructure (UNII) frequency bands. This can be compared to the estimated dimensions of the dipole antenna ($\lambda_{on\text{-}chip}/2$) and large-loop antenna ($\lambda_{on\text{-}chip}$) in silicon in Figure 2-9, with markers denoting the frequency bands. Considering that 2 mm is a reasonable dimension for an antenna structure, the small-loop antenna, dipole and large-loop antenna would become economically feasible for integration at (or after) the 5.2 GHz, 24 GHz and 60 GHz frequency bands, respectively. This assessment, although it agrees with the 1.5 mm dimension of the 24 GHz dipole implemented in [17], is based on approximate calculations and more accurate antenna dimensions should be determined through simulations in an EM modelling environment. Nevertheless, operating at the 5.2-GHz band with the small-loop antenna would be advantageous, as the transmitter circuitry to generate the carrier would consume less power than higher frequency bands.

Loop antenna structures are also preferred over dipole structures for body-worn or hand-held applications. This is a result of the type of radiated energy in the reactive near field. For the loop antenna, the energy is mostly magnetic whereas for the dipole, the energy is mostly electric. Thus, a dipole antenna is susceptible to detuning by materials

with a dielectric constant larger than one (such as the human body ε_{r_body} = 75 in wireless dosimetry applications) in the reactive near field [11]. However, considering that the dipole antenna can only be economically integrated at (or after) 24 GHz, the outer boundary of the reactive near field from this carrier frequency is approximately 2 mm (in air) according to (2.3), which is probably too small of a region to be a concern.

Table 1: A comparison of estimated small-loop antenna sizes in ISM and UNII.

Frequency	$\lambda_{0\ air}$	$\lambda_{on\text{-}chip}$ ε_{r_avg} = 8	Small-loop antenna circumference = 0.1·$\lambda_{on\text{-}chip}$
900 MHz (ISM)	333 mm	118 mm	11.8 mm
1.8 GHz (ISM)	167 mm	59 mm	5.9 mm
2.4 GHz (ISM)	125 mm	44 mm	4.4 mm
5.2 GHz (UNII)	58 mm	20 mm	2 mm
5.8 GHz (ISM)	52 mm	18 mm	1.8 mm
24 GHz (ISM)	12.5 mm	4.4 mm	0.44 mm
60 GHz (ISM)	5 mm	1.8 mm	0.18 mm

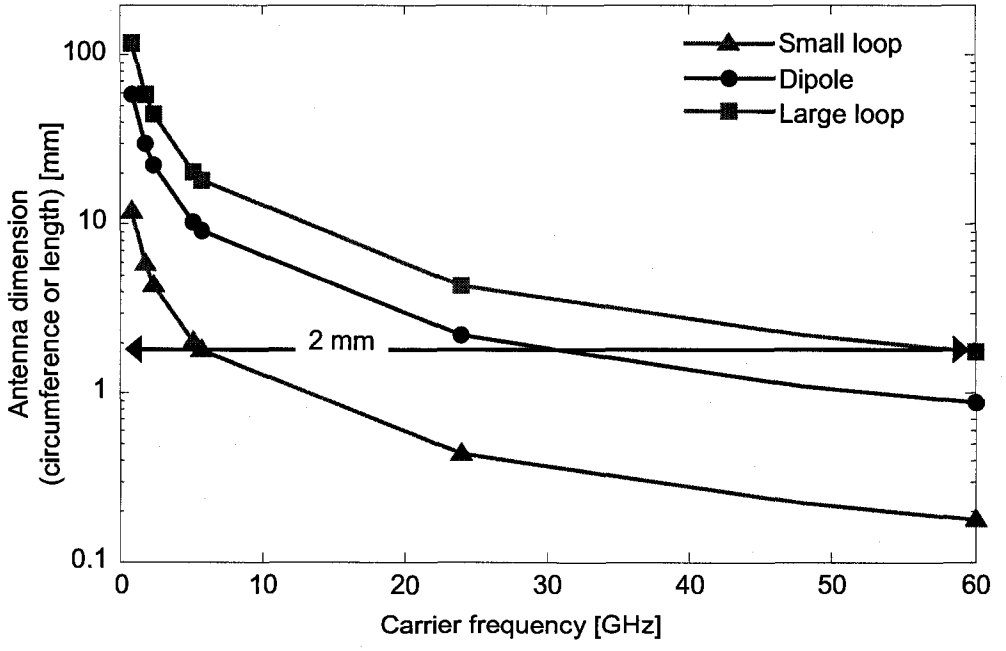

Figure 2-9: Estimated integrated antenna dimensions.

2.2. Transmitter Fundamentals

2.2.1. Communication Link Budget

The communication link between a transmitter and a receiver is governed by a link budget. The link budget relates the power delivered P_{RX} to the receiver's antenna to the power delivered P_{TX} to the transmitter's antenna. The Friis transmission equation [18] is commonly applied for link budgeting and is given by

$$P_{RX} = P_{TX} \cdot G_{TX} \cdot G_{RX} \left(\frac{\lambda_0}{4\pi r_X} \right)^2 \tag{2.31}$$

where G_{TX} and G_{RX} are the gains of the transmitter and receiver antennas respectively, λ_0 is the wavelength of the electromagnetic wave in free space, and r_X is the distance between the two antennas. The term $[\lambda_0/(4\pi r_X)]^2$, known as the free-space loss factor, is the loss in signal strength of an electromagnetic wave that would result from a line-of-sight path through free space. The Friis equation assumes that the input impedance of transmitting and receiving antennas are matched to their respective loads for zero reflection and are matched to the same polarization [19].

The minimum power level a receiver, with a noise figure NF, can detect with an acceptable carrier-to-noise ratio C_{RX} / N defines the receiver's sensitivity and is given by

$$P_{RX\_\min} = kTB \cdot NF \cdot C_{RX} / N \tag{2.32}$$

where k is Boltzmann's constant = 1.38065×10^{-23} J/K, T is the system temperature in Kelvin, and B is the receiver bandwidth. The carrier-to-noise ratio is related to the energy-per-bit to noise density ratio E_{bit} / N_o by

$$C_{RX} / N = E_{bit} / N_o \cdot R_{data} / B \tag{2.33}$$

where R_{data} is the data rate. Depending on the form of modulation, the energy-per-bit to noise density ratio determines the bit error rate (BER), a BFSK signal for instance requires an E_{bit} / N_o of 13 dB for a BER of 10^{-5} [20].

2.2.2. Power and Efficiency

In order to maximize the cycle-life of an on-chip power source, a transmitter must not only consume a minimal amount of power but also be energy-efficient in the communication of data. The low event rates of the biomedical sensor permit the transmitter to conserve energy by powering off between packet transmissions. With the aid of Figure 2-10, an example of a timing diagram of encoded data, the energy required to communicate one packet of L_{packet} bits of data at a rate of R_{data} bps is given by

$$E_{TX} = P_{MOD} \cdot T_{power-up} + (P_{MOD} + P_{PA}) \cdot T_{transmit} \tag{2.34}$$

where P_{MOD} is the power consumption of the transmitter's modulator, $T_{power\text{-}up}$ is the time required for the transmitter to power-up, and P_{PA} is the power consumption of the transmitter's power amplifier [23]. The time required to transmit a packet is $T_{transmit} = L_{packet} / R_{data}$, which is inversely proportional to the data rate for simple modulation schemes, such as on-off keying (OOK) or frequency shift keying (FSK), when the packet size is held constant. The transmitter's $T_{power\text{-}up}$ is the time required for circuits to reach their biasing points and, if the transmitter consists of a frequency synthesizer, the locking time of the RF carrier to the desired channel. The transmitter's average power consumption with respect to time P_{TX_avg} is given by

$$P_{TX\_avg} = \frac{E_{TX}}{T_{packet}} = \frac{E_{TX}}{T_{off} + T_{power-up} + T_{transmit}} \tag{2.35}$$

where T_{off} is the time when the transmitter is in the powered-down state and T_{packet} is the packet period which is the reciprocal of the packet rate R_{packet} [23]. Clearly, a low-power transmitter design can be achieved by minimizing the power consumptions of the PA and modulator. In addition to this, implementing an energy-efficient transmitter design would also require a fast power-up time and transmitting with a high data rate. P_{TX_avg} can also be reduced by lowering the packet rate or packet size; however these parameters are usually predetermined by factors unrelated to the transmitter, such as MAC addressing, synchronization header, error correction bits, payload size and allowable latency

from an event. The low event rates of the sensor, meaning $T_{off} >> T_{power\text{-}up} + T_{transmit}$, would lead to a low packet rate and result in the transmitter having a low active duty cycle DC_{TX}, where $DC_{TX} = (T_{power\text{-}up} + T_{transmit}) / T_{packet}$. For a packet transmission, the radiated energy-per-bit E_{bit} is given by

$$E_{bit} = \frac{e_{RAD} \cdot P_{ANT} \cdot T_{transmit}}{L_{packet}} = \frac{e_{RAD} \cdot P_{ANT}}{R_{data}} = \frac{e_{RAD} \cdot \eta_{PA} \cdot P_{PA}}{R_{data}} \tag{2.36}$$

from a substitution of (2.25) and of the PA's efficiency η_{PA}, which is expressed by

$$\eta_{PA} = \frac{P_{ANT}}{P_{PA}} = \frac{e_R \cdot P_{AVS}}{P_{PA}}, \tag{2.37}$$

a ratio of the PA's RF output delivered power (2.22) to the PA's DC power consumption.

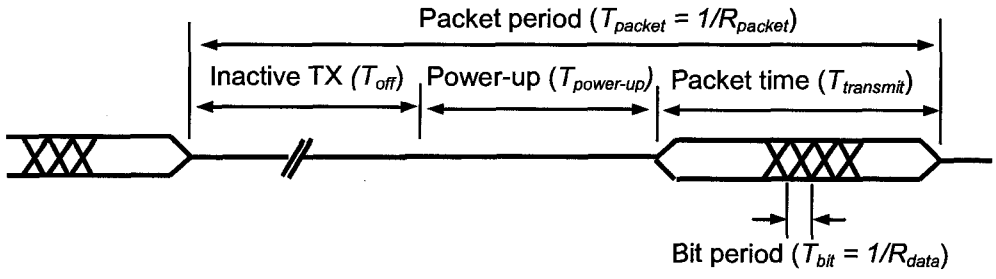

Figure 2-10: Timing diagram of the encoded data.

The maximum achievable PA efficiency is dependent on the type of PA architecture or "class" implemented. There are a number of different classes of PAs, and common convention is to group these into two main categories; "linear" and "non-linear" (or "switch-mode"). A linear PA generally refers to a design which has a linear relationship between the input and output signals – i.e. a PA which operates at constant gain, although the PA may have transistors operating in a nonlinear fashion. A non-linear PA generally refers to a PA designed to operate with a constant input power while the output power is varied by a change in gain. A study of linear and non-linear PA classes is presented in [21]. Here, a brief review of linear PAs – Class A, B and C, is provided with details of classification criteria and maximum theoretical efficiency [22].

For linear PA designs, the amplifiers are classed according to what proportion of the input signal cycle is used to actually switch on the amplifying transistor. The PA's linearity (i.e. the degree of linearity of the input-output relationship) and efficiency performance are design trade-offs. Consider a common-source PA with a tuned load. The Class A is the simplest form of PA design, the amplifying transistor is in its active region for the entire input cycle. The transistor is biased such that it is conducting at all times, even when no input signal is applied, and this current represents a continuous loss of power in the transistor. The maximum efficiency for this PA design is $\eta_{PA\text{-}A} = 50\%$. In the Class B PA design, the transistor is biased on the edge of conduction, requiring a large voltage excursion at the input to turn the transistor on. When the transistor is only conducting current for half the input cycle, the Class B can achieve a maximum efficiency of 78%. This improvement in maximum efficiency over the Class A design is achieved at the expense of linearity. Finally, in the Class C PA design, the transistor is biased below its threshold. A large voltage excursion at the input is again required to turn the transistor on, but the transistor turns on for only a fraction of the input signal cycle. The corresponding output signal, a current, will be a pulse representation of the input. Changes in the input voltage amplitude will not be significantly reflected in the output pulse, leading to increased distortion and degraded linearity. The output current is then filtered at the fundamental harmonic (usually when the PA is not acting as a multiplier) and delivered to the load. The maximum efficiency for the Class C PA is 100%. The reader should be aware that the maximum efficiencies for the PAs discussed thus far are based on theoretical calculations, and efficiencies of the actual implementations will be of course less.

In the case of a short-range transmitter, the antenna-delivered power is around 0 dBm and in all likelihood $P_{MOD} \approx P_{PA}$ or some small multiple thereof. Thus, from (2.35), shortening $T_{transmit}$ by increasing the data rate would decrease the transmitter's average power consumption – at diminishing returns, by reducing the effect of P_{MOD} [23]. A relatively minimal power consumption increase in the transmitter's modulator, however,

would be expected to support higher data rates. Consequently, for link budgeting, an increase in the data rate – ceteris paribus[1] – would also require a proportional increase in the transmitter's radiated power (as $P_{RAD} \alpha P_{ANT} = P_{TX}$) to compensate for the increase in the minimum power level that a receiver can detect (i.e. a reduction in receiver sensitivity given by (2.32)), and hence a P_{PA} increase for a given PA efficiency by (2.36), to maintain the same energy-per-bit. Thus increasing the data rate would not provide significant reductions in the transmitter's average power consumption when considering the specifications adopted for the communication system – those of the transmitter as well as the receiver. Therefore, in this context, the transmitter's average power consumption could be reduced with impunity by improving PA efficiency or employing power control techniques on P_{PA} when communicating at shorter distances. Alternatively, the communication system could indirectly trade-off power consumption between transmitter and the receiver. For instance, increasing the data rate but maintaining P_{TX} (and P_{PA}) constant, the reduction in receiver sensitivity could be improved (with a lowering of P_{RX_min}) by a decrease in the receiver's *NF* according to (2.32). *NF* improvement is generally at the expense of increased receiver active power consumption, and depending on the type of power source used by the receiver this may not be a concern. This scenario would allow the transmitter's average power consumption to be reduced, although it would be at the expense of the receiver's active power consumption. Therefore, for low-power short-range transmitter design, it is prudent to minimize the power consumption of the modulator as this avoids adjustments to other specifications of the system. This is also true if this transmitter consists of a frequency synthesizer which may require 100's of microseconds to lock the carrier making $T_{power\text{-}up} >> T_{transmit}$, and thus resulting in $P_{TX\_avg} \approx (P_{MOD} \cdot T_{power\text{-}up}) / T_{packet}$ which is independent of the data rate [23].

---

[1] Ceteris Paribus: a Latin phrase, rendered in English as "all other things being equal."

The transmit efficiency η_{TX} is defined as the fraction of antenna-delivered to consumed power during the period $T_{transmit}$, and is expressed by

$$\eta_{TX} = \frac{P_{ANT}}{P_{MOD} + P_{PA}} = \frac{e_R \cdot P_{AVS}}{P_{MOD} + P_{PA}} = \frac{\eta_{PA} \cdot P_{PA}}{P_{MOD} + P_{PA}} = \frac{\eta_{PA}}{P_{MOD} / P_{PA} + 1} \tag{2.38}$$

from a substitution of (2.25) and (2.37). If the power consumption of the modulator is minimized to the point where $P_{PA} >> P_{MOD}$, then the transmit efficiency is only dependent on PA efficiency (which is also a function of the mismatch efficiency).

2.2.3. Modulation

In digital carrier-based modulation, an analog carrier signal is modulated by a digital bitstream through a change in the carrier's amplitude, phase and/or frequency. Spectral efficiency is the term used to describe the amount of information that can be transmitted over a given bandwidth in a specific digital communication system. For a system to approach the theoretical channel data capacity limits, precise phase and amplitude control are required. This can be achieved at the expense of increased power consumption as additional circuitry is usually required in the form of up-conversion mixers and fast-settling high-precision PLLs. Generally, there exists a trade-off between the system's power efficiency and spectral efficiency. In a wireless sensor system, the low event rates of the sensor permit the transmitter to operate with a low active duty cycle and to maximize the battery's cycle-life with a low average power consumption, thus the optimal use of bandwidth is not a necessity.

The simplest form of digital modulation is on-off keying, in which the presence of a carrier for a specific duration in time represents a logic "1", while its absence for the same duration represents a logic "0". With OOK, abruptly changing the amplitude of the carrier by power cycling demands the transmitter's bias points must settle in less than a bit period, potentially limiting data rates. A more spectrally efficient modulation scheme is binary frequency-shift keying, usually referred to simply as FSK, where the carrier is frequency shifted between two discrete values, termed the mark frequency and the space

frequency. By convention, the mark and space correspond to a logic "1" and "0", respectively. Increasing the frequency shift separation relaxes the phase accuracy requirements for the transmitter and decreases the receiver's sensitivity to phase noise [34]. The constant envelope nature of BFSK enables the transmitter to use an efficient nonlinear PA.

BFSK is a binary form of frequency modulation (FM). The two conventional methods for BFSK generation are the VCO and the switched oscillator, which are illustrated in Figure 2-11 a) and b), respectively. In the VCO method, a pulse shape data signal is used to control the frequency of the oscillator, shifting the carrier between the mark and the space. The shape of the data signal could be a rectangle, raised cosine or Gaussian pulse shape. The raised cosine and Gaussian pulse shapes are commonly used as these result in gradual rather than abrupt frequency shifts, generating a continuous phase form of FSK. In the switched oscillator method, the data signal selects one of two carrier frequencies of equal amplitudes. This usually results in abrupt phase changes, generating a discontinuous phase form of FSK. The modulated carrier can be written in terms of basis functions as $S_{BFSK}(t) = \alpha_1 \cdot \cos 2\pi f_1 \cdot t + \alpha_2 \cdot \cos 2\pi f_2 \cdot t$, where $[\alpha_1, \alpha_2]$ = [0 1] or [1 0] in response to the modulating data signal [24]. For the basis functions to be orthogonal over a bit period T_{bit},

$$\int_0^{T_{bit}} \cos 2\pi f_1 \cdot t * \cos 2\pi f_2 \cdot t \, dt = 0. \tag{2.39}$$

For the case when $f_1 + f_2 >> f_1 - f_2$ in frequency, (2.39) above reduces to $\sin(2\pi f_1 - 2\pi f_2) \cdot T_{bit} / (2\pi f_1 - 2\pi f_2) = 0$, and therefore $(2\pi f_1 - 2\pi f_2) \cdot T_{bit} = n \cdot \pi$. When n = 1, the minimum frequency shift is thus $f_1 - f_2 = 1/(2T_{bit}) = R_{data}/2 = f_m$, the frequency of the data signal. A term called the modulation index m of an FM carrier is defined as

$$m = \Delta f / f_m \tag{2.40}$$

where Δf is called the frequency deviation and is given by

$$\Delta f = (f_1 - f_2)/2. \tag{2.41}$$

The modulation index describes the bandwidth of the modulated carrier. When $m << 1$, the modulation is narrowband FM (NBFM), and when $m >> 1$, the modulation is wide-band FM (WBFM). The bandwidth requirements B_T of a carrier that is frequency modulated by a continuous signal can be approximated by Carson's rule, which is defined as

$$B_T = 2(\Delta f + R_{data}) \tag{2.42}$$

where 98% of the FM spectrum power is contained [24].

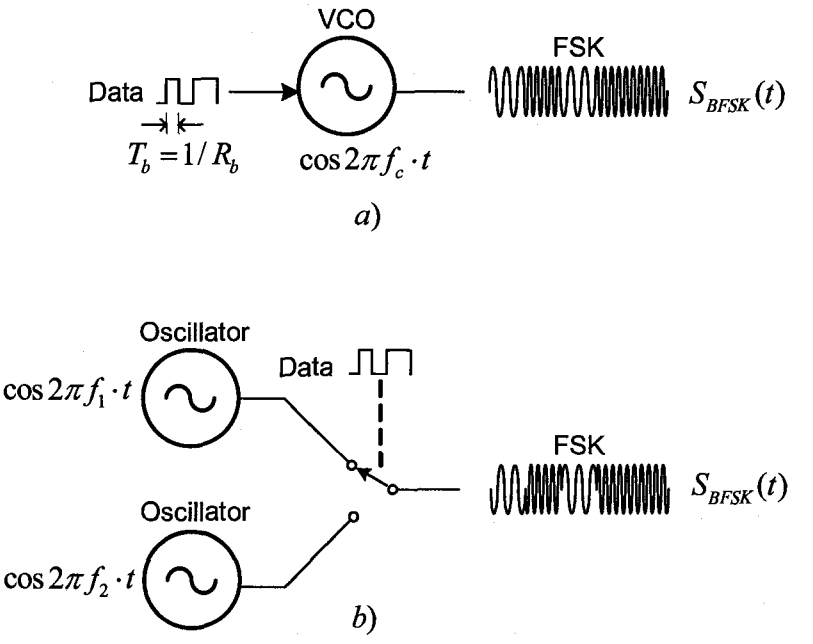

Figure 2-11: BFSK generation; a) VCO and b) switched oscillator.

Ultra-wideband (UWB) signals are generally defined as signals with a fractional bandwidth greater than twenty percent of their central frequency or as signals with a bandwidth of more than 500 MHz, whichever is less [25]. These signals are typically impulse-based, where carrier-less short duration (sub-nanosecond) pulses are digitally modulated using techniques such as OOK, pulse amplitude modulation or pulse position modulation. The short duration of UWB pulses instantaneously generates a very wide bandwidth in the frequency domain. UWB has several advantages over narrow-band (or

wideband) communication systems, such as a high data-rate and a low average radiated power. Although UWB signals looks like noise to narrowband systems, as an UWB signal energy is spread over a large frequency range, there are coexistence issues. A study [26] showed that an UWB system can greatly impact the performance of an 802.11a WLAN system. In addition, interference from an 802.11a WLAN system can also greatly impact UWB receiver performance.

2.2.4. Architectures

The function of the transmitter is to up-convert baseband (or intermediate-frequency) data of a modulated signal onto an RF carrier that can be transmitted via an antenna. The deployment of wireless sensor networks (WSN) has driven much of the recent research into low-power transmitter designs. In this subsection, the direct/indirect closed-loop modulation, the direct open-loop modulation, the oscillator transmitter and the injection-locked architectures of low-power are reviewed.

While low-power solutions have been demonstrated for UWB transmitters, such as in [27] for a wireless body area network (WBAN), low-power UWB receiver design remains very challenging due to the large bandwidth requirements of the analog front-end and baseband circuits, the high sampling rates of the ADC, and the strict timing signal synchronization [28]. A receiver is an essential part of a wireless sensor transceiver for receiving instruction commands, such as initiating a sensor calibration or reading. It is for this reason that UWB transmitter architectures are excluded from this literature review.

Direct/Indirect Closed-Loop (CL) modulation transmitter

This transmitter's modulator can consist of a phase-locked loop whose voltage controlled oscillator is modulated directly via a secondary VCO varactor (other than the one used by the PLL to lock the VCO) or indirectly through a PLL's frequency divider ratio. The indirect approach has been implemented with a sigma-delta (Σ-Δ) in a fractional-N synthesizer [29], but in using this approach the data rate is limited by the low-

pass filtering of the PLL. The direct VCO modulation approach does not have an upper bound on the data rate; however, low frequency components of the modulated data will be corrupted because the PLL acts as a high-pass filter from the VCO's perspective. The later approach has been implemented by [30], achieving a 6.5 GHz BFSK modulator, which could be integrated with a PA connected to an antenna to form the direct closed-loop modulation transmitter of Figure 2-12. Manchester data encoding is used in [30] to minimize the PLL's high-pass filter effect on modulation by removing the low frequency component of the data. This is achieved by generating a transition at the middle of each bit period. The drawback with this approach is that the effective data rate is halved.

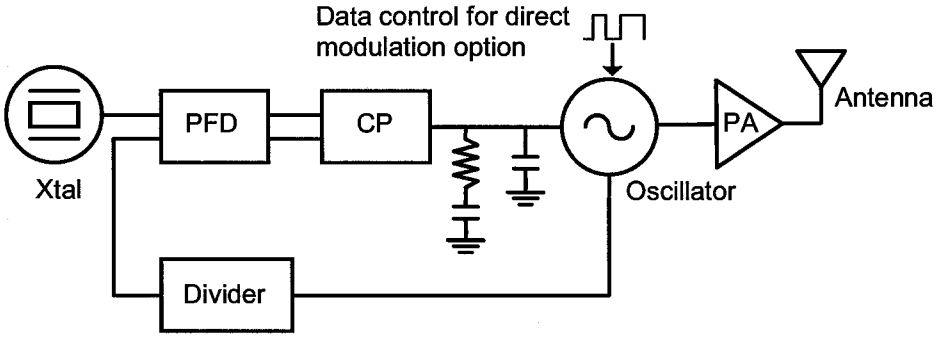

Figure 2-12: Direct closed-loop modulation transmitter.

Direct Open-Loop (OL) modulation transmitter

If the PLL of the direct modulation transmitter is opened after frequency (and phase) locking, and thereby eliminating the loop feedback mechanism on the VCO, the applied modulated data will not be corrupted by the (high-pass) filtering of the loop. This technique has been implemented by [31], realizing a 2.4 GHz FSK modulator. With no PLL feedback, the VCO's output frequency is vulnerable to being pulled by noise. However, as seen in [31], the frequency drift can be as minimal as 2.5 Hz/μs by using a low-off-leakage charge pump (CP) which traps charge on the filter's capacitors (denoted by C_1 and C_2 in Figure 2-13) when the loop is opened. As these capacitors are connected to the VCO's control line, the frequency drift is minimized, and then data can be switched

onto a secondary varactor line for FSK modulation. When a direct open-loop modulator such as the one described is integrated with a PA connected to an antenna, the transmitter of Figure 2-13 is formed.

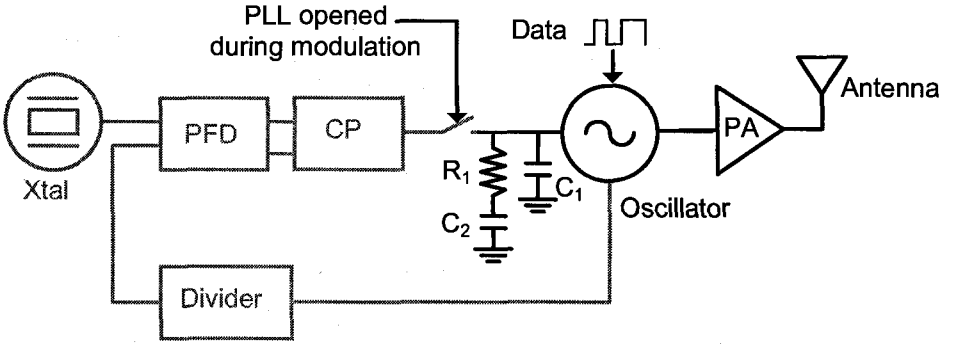

Figure 2-13: Direct open-loop modulation transmitter.

Oscillator transmitter

The most straightforward architecture is the oscillator transmitter, comprised of only an oscillator as presented in [32]. Here, an inductive coil in the Colpitts oscillator's resonant tank is also used as an antenna to radiate a 315 MHz OOK carrier, negating the need for a power amplifier. Alternatively, the antenna does not form part of the oscillator and is driven by a power amplifier. This has been implemented by [33] and [34] for 1.9 GHz OOK carrier and 2.4 GHz FSK carrier modulation, respectively. The oscillator transmitter architecture variants are shown in Figure 2-14 a) and b), respectively.

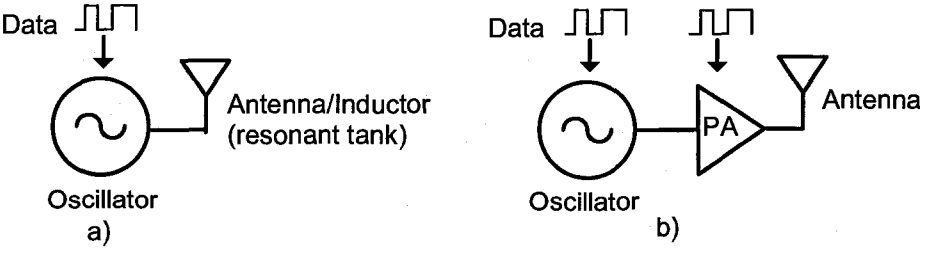

Figure 2-14: Oscillator transmitters; a) without PA and b) with PA.

Injection-locked transmitter

The injection-locked transmitter, described in [35], does not require a power amplifier as baseband data is modulated onto a 1.9 GHz carrier by power cycling (for OOK) an efficient power oscillator which drives an external antenna. As shown in Figure 2-15, this architecture obtains an accurate carrier frequency by injection-locking the power oscillator with a reference oscillator comprising of a high-Q film bulk acoustic resonator. In [36], a Colpitts oscillator is coupled to a surface acoustic wave (SAW) resonator for carrier stability. The oscillator drives a power amplifier which is power cycled to generated a 916.5 MHz carrier with OOK modulation.

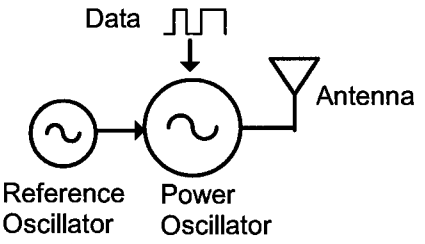

Figure 2-15: Injection-locked transmitter.

2.2.5. Performance Comparison

A comparison of short-range transmitters is listed in Table 2 – highlighting the architecture, implementation details (such as the die area of the modulator, PA and antenna), carrier frequency and modulation scheme. For each transmitter, the average power consumption for communicating a 1-kbit packet at a rate of 1 packet per second is evaluated based on the published data rate and assuming the power-up time can be neglected since, typically, $T_{transmit} >> T_{power\text{-}up}$. The transmit efficiency is also evaluated based on the published active power consumption ($P_{TX\_active} = P_{MOD} + P_{PA}$) and the output power ($P_{ANT}$, power delivered to the antenna/output load). These performance results are compared in Table 3, and, if possible, are plotted in Figure 2-16.

Table 2: A comparison of published short-range transmitters.

Reference	Architecture	Process	Area (est.)	Carrier	Modulation	Modulator	PA	Antenna
[29]	Indirect (CL)	0.5 µm CMOS	~3.5 mm^2 *	2.4 GHz	GFSK	•		
[37]	Indirect (CL)	0.25 µm CMOS	4.8 mm^2 *	0.4 GHz	FSK	•	•	
[30]	Direct (CL)	0.25 µm CMOS	~2.2 mm^2	6.5 GHz	BFSK	•		
[38]	Direct (CL)	0.25 µm CMOS	~0.4 mm^2 *	0.9 GHz	FSK	•	•	
[31]	Direct (OL)	0.2 µm CMOS $^{\Psi}$	1.5 mm^2	2.4 GHz	FSK	•		
[32]	Oscillator	CMOS	25 mm^2 *	0.3 GHz	OOK	○		•
[33]	Oscillator	0.13 µm CMOS	~0.4 mm^2 *	1.9 GHz	OOK	•	•	
[34]	Oscillator	0.13 µm CMOS	~1 mm^2	2.4 GHz	FSK	•	•	
[39]	Oscillator	0.13 µm CMOS	~250 mm^2	1.9 GHz	OOK	•	•	○
[40]	Oscillator	0.5 µm CMOS	~0.01 mm^2 *	0.4 GHz	FM	•		○
[35]	Injection-locked	0.13 µm CMOS	0.4 mm^2	1.9 GHz	OOK	•		
[36]	Injection-locked	0.18 µm CMOS	0.4 mm^2 *	916 MHz	OOK	•	•	

* Off-chip component(s), excluding the antenna, used which are not included in area estimation,

• denotes an on-chip component,

○ denotes an off-chip component, and

$^{\Psi}$ CMOS SOI process.

Table 3: A performance comparison of published short-range transmitters.

Reference	R_{data}	P_{TX_avg}	P_{TX_active}	P_{ANT}	η_{TX}
[29]	1 Mbps	135 µW $^{\text{¥}}$	135 mW	n/a	n/a
[37]	100 kbps	50 µW	5 mW $^{\Psi}$	1 mW	20%
[30]	2.5 Mbps	9 µW $^{\text{¥}}$	22 mW	n/a	n/a
[38]	100 kbps	13 µW	1.3 mW	0.25 mW	19%
[31]	~1 Mbps	17 µW $^{\text{¥}}$	17 mW	n/a	n/a
[32]	1 Mbps	0.3 µW †	0.6 mW	n/a	n/a
[33]	5 kbps	180 µW †	1.6 mW	0.375 mW	23%
[34]	500 kbps	2 µW	1 mW	0.3 mW	30%
[39]	330 kbps	4 µW †	2.7 mW	1.2 mW	44%
[40]	40 kbps	10 µW	0.41 mW	~0.01 mW *	2.4%
[35]	156 kbps	12 µW †	3.6 mW	1 mW	28%
[36]	500 kbps	9.1 µW †	9.1 mW	0.6 mW	6.6%

n/a: information not available,

$^{\text{¥}}$ P_{TX_avg} based solely on the modulator,

† P_{TX_avg} assumed equal probability of "1" and "0" for OOK,

$^{\Psi}$ P_{TX_active} includes other circuit blocks (like DSP, ADC, etc..), and

* P_{RAD} (and not P_{ANT}).

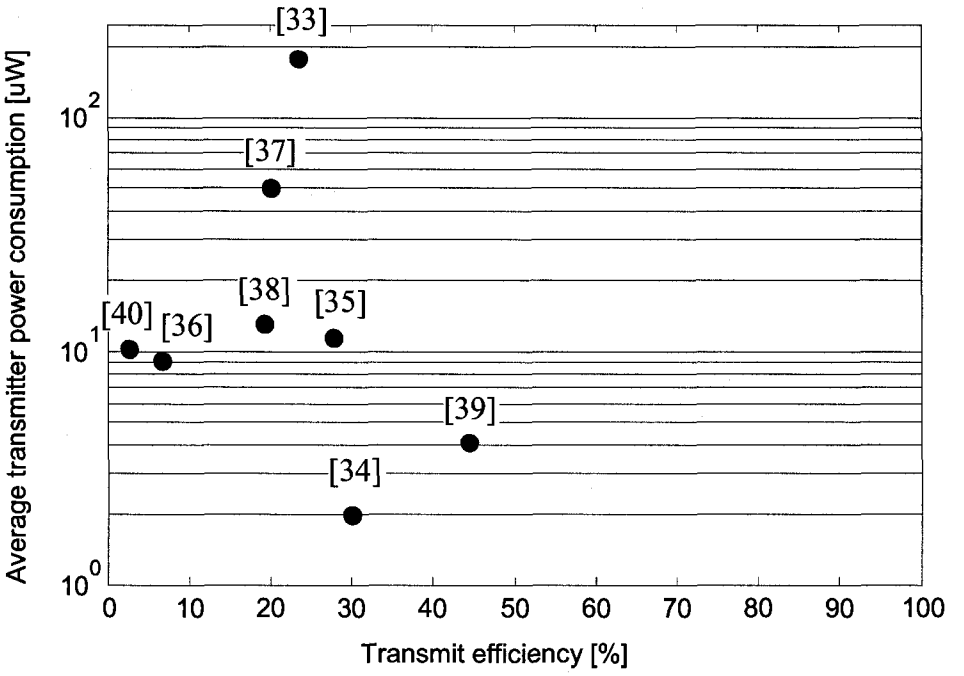

Figure 2-16: P_{TX_avg} and η_{TX} comparison of published short-range transmitters.

A low average transmitter power consumption and a high transmit efficiency is clearly desirable for the design of a mobile wireless transceiver. Based on these criteria, the superior performance of the oscillator transmitters in [34] and [39] is evident. From a system design perspective, the communication link budget of (2.31) is dependent, among other factors, on the attenuation undergone by the carrier as it propagates. In free space, this attenuation is proportional to the square of the carrier frequency. Accordingly, the carrier frequency is inversely related to the distance for communication. With this in mind, an antenna-delivered power ($P_{ANT} = P_{TX}$) comparable to [39] (at 1.2 mW) is that of the indirect closed-loop transmitter in [37] (at 1 mW) but with a carrier frequency that is lower by approximately a factor of "5". Hence, all other things in (2.31) being equal, transmitter [37] would be capable of communicating over a distance "5" times longer. Alternatively, a design trade-off with this increase in distance is possible by reducing the P_{TX} of this transmitter by a factor of "5^2". This option results in a proportional decrease in P_{RAD}, a lower transmit efficiency and a lower average transmitter power consumption

if $P_{PA} \approx P_{MOD}$ or greater. Operating at a lower carrier frequency, but radiating very low power ($P_{RAD} << 1\text{mW}$), may have been the design methodology followed in the oscillator transmitter of [40]. Therefore, when considering the communication range specification, a transmitter operated at a low carrier frequency would minimize the transmitter's active power consumption as less power would be required to be radiated (since $P_{PA}\ \alpha\ P_{RAD}$) than a design with a high carrier frequency. Thus, there exists the potential for design optimization of low-powered oscillator transmitters as the performance of [34] and [39] can both be improved by migrating to a lower carrier frequency. The major concern with this design methodology is the trade-off mentioned in Subsection 2.1.4 – the antenna's dimensions are directly proportional to the wavelength of the carrier frequency.

Since it is the objective of this research to design and implement an SoC transmitter solution by integrating the antenna in a mainstream submicron CMOS process, antenna integration only becomes economically feasible when the carrier frequency is increased to 5.2 GHz (or higher) as concluded from Table 1. The propagation losses with higher carrier frequencies can be compensated by increasing antenna directivity (and gain) with the use of an antenna array as suggested in [41]. This can be explained in terms of the antenna's effective area, which is generally proportional to the antenna's physical size. Thus, when a form-factor constraint is imposed, leading to a fixed effective area (A_{EFF}), antenna directivity (D) and gain (G) are seen to increase with frequency according to (2.30). With an increase in frequency, the effective area is maintained constant by employing an antenna array structure. It is stated in [41] that for a 60 GHz system with a 16 element antenna array, the gain is 3 dB higher than a 5-GHz omnidirectional system while occupying only a tenth of the antenna area. The drawback with an antenna array is the increased system complexity required to shift the phase of the RF signal for each antenna element to achieve beam steering. In addition, a 60 GHz system implemented in CMOS would consume more power than that of a 5-GHz system as the resistive losses due to transistor and interconnect layout parasitics are more significant.

2.2.6. Circuit Integration

The integration of the transmitter's digital, analog and RF circuitry on a single die for a mixed-signal chip solution can be cost-effective when fabricated with a low cost process technology like CMOS. The use of submicron CMOS allows for an unprecedented degree of scaling and integration in digital circuitry, and the high speed of the MOSFET transistors in this process enables RF functions to be implemented. In addition, the shrinking of feature size forces the supply voltage to scale down to ensure reliability, making this technology best suited for high-speed low-voltage design. There are challenges, however, with implementing in a submicron CMOS process. For example, the MOSFETs have increased gate leakage currents with the thinner gate oxide. For a low duty-cycle wireless biomedical sensor, there could be a non-negligible amount of power dissipated from leakage currents $P_{Leakage}$ during the transmitter's powered-down inactive state [23]. To include this loss in the transmitter's average power consumption, the expression for E_{TX} should be revised to

$$E_{TX} = P_{Leakage} \cdot T_{off} + P_{MOD} \cdot T_{power-up} + (P_{MOD} + P_{PA}) \cdot T_{transmit} . \tag{2.43}$$

Another challenge with implementing a mixed-signal integrated chip is the coupling of noise between the digital, analog and RF blocks. Noise coupling through the supply can be alleviated by routing separate power and ground signals for each of these blocks. A study [42] on noise coupling through the silicon substrate has shown that triple-well technology offers better isolation than that of guard ring or proton implant. A submicron CMOS process is also challenging for analog and RF design in particular, as MOSFETs have degraded large-signal linearity, less voltage gain, lower voltage handling capability, and potentially higher 1/f noise when scaled [43].

2.2.7. Reference Oscillator

The reference oscillator of a conventional wireless transceiver is generated from an off-chip crystal oscillator that uses the mechanical resonance of a vibrating crystal of piezoelectric material, such as quartz. The crystal oscillator is among the most difficult to im-

plement on-chip. The challenge of an integrated solution is in achieving the same level of accuracy and temperature stability (< 35 ppm over 0–70°C) that is intrinsic to the crystal's high quality Q-factor (of the order of 10 000) [44]. Recently, the authors of [45] presented a temperature-compensated self-referenced LC oscillator in a 0.35 μm CMOS technology, and claimed a total frequency accuracy of +/- 400 ppm on 96 MHz over process variations, a 10% variation in the power supply voltage and a temperature variation from 10 to +85°C. With the exception of high power consumption, 31 mW, the self-reference LC oscillator's frequency stability may be sufficient for some SoC designs. For instance, a 5.2 GHz carrier phase-locked to this reference source would have a frequency variation of +/- 2.08 MHz, which must be considered when determining the system's modulation scheme.

An alternative to crystal and self-referenced LC oscillators is on-chip vibrating micromechanical resonators based on micro-electro-mechanical system (MEMS) technology. In [46], researchers demonstrated a clamped-clamped beam micromechanical resonator at 10 MHz with a Q of 4 000 and a frequency stability of 34 ppm over 0–70°C. A wine glass disk micromechanical resonator in [47] achieved at 60 MHz a Q of 48 000. This resonator is connected to a sustaining transresistance amplifier fabricated in a 0.35 μm CMOS process, yielding a combined footprint of less than 160 μm by 160 μm. The power dissipation of this oscillator is < 1 mW, an attractive feature for SoC designs, however phase noise performance is only –130 dBc/Hz beyond a 10 kHz offset, which may affect the choice of the modulation scheme.

2.3. Power Source Fundamentals

The development of thin-film ultracapacitors, with charge storage densities of up to 100 F/cm^3, has the potential to meet the power supply requirements of a short-range low-power transmitter without the need for a battery. The advantages of ultracapacitors relative to conventional off-chip batteries (such as lead-acid, lithium-ion or nickel-cadmium batteries) are high power density, high efficiency, fast recharging, long shelf and cycle

life. Ultracapacitors, however, have a lower energy density when compared to these batteries especially in the case of high power requirements, where a decrease in the RC time constant of the ultracapacitor requires a sacrifice in its energy density given a set of manufacturing materials [5]. The recharging of an ultracapacitor can be accomplished through a number of power scavenging systems, involving RF, solar, vibration or thermoelectric energy harvesting. For the SoC dosimetry transceiver architecture, an ultracapacitor with a solar cell is proposed, as this hybrid power source can be manufactured on top of the chip. The power sourcing capability of this hybrid solution is briefly explored in this section for the transmitter.

2.3.1. Thin-Film Ultracapacitors

For the SoC transmitter, the size of the ultracapacitor C_{ultra} is primarily determined by time required to transmit a packet ($T_{transmit}$) and is given by

$$C_{ultra} = T_{transmit} \cdot I_{TX\_active} / \Delta V_{ultra} \tag{2.44}$$

where I_{TX_active} is the current consumed by the transmitter and ΔV_{ultra} is the change in voltage across the ultracapacitor. For instance, a transmitter design which requires 2.5 mA to transmit a 1 kbit packet at a rate of 100 kbps, would require 50 μF of capacitance if ΔV_{ultra} = 0.5 V. Therefore, a 50 mF ultracapacitor would store sufficient charge to complete 1000 packet transmissions while only occupying an area of 5 mm^2. In this application example, the power consumed by the power management circuits, such as the ultracapacitor's voltage regulator, are neglected.

2.3.2. Thin-Film Solar Cells

Solar cells, or photovoltaic cells, are devices which convert light energy into electrical energy by the photovoltaic effect. The development of cheaper and more efficient photovoltaic cells is the focus of present research. Promising photovoltaic technologies are thin-film amorphous silicon (a-Si), thin-film cadmium telluride (CdTe) and thin-film

polycrystalline cells. In contrast to the prevailing conventional manufacturing with crystalline silicon (c-Si), thin-film processing costs are less expensive.

An interesting application example for a thin-film solar cell is proposed [48], where the solar cell is to trickle charge a large storage capacitor which serves as the power source for an integrated wireless sensor system. This hybrid power solution is similar to that proposed in this thesis. In [48], the authors claim the thin-film solar cell is capable of generating power densities of 36 $\mu W/cm^2$ and 2.8 mW/cm^2 for indoor and outdoor environments, respectively. For the SoC transmitter, the dimensions of the thin-film solar cell are determined by the size of the ultracapacitor as it is assumed the operating environment for the system is inside a hospital. The power sourcing requirements of the solar cell does not necessarily need to recharge the entire ultracapacitor, but should be sufficient to replenish the charge lost from a packet transmission. For instance, the transmitter design of the previous subsection required 50 μF of capacitance for a transmission. The next transmission is dictated by the packet period (T_{packet}) – a reasonable presumption is 1 second per packet. Therefore, it is theoretically feasible for a thin-film solar cell to be manufactured on top of the ultracapacitors to trickle charge them in that time period using the ambient light inside a hospital.

2.4. Design Considerations Summary

An overview of the fundamental considerations for an SoC transmitter design is presented to highlight the various choices, and associated trade-offs, available to the designer.

The background antenna theory provided an understanding of this device as an instrument for radiating or receiving electromagnetic waves. Of the antenna structures discussed, the "small loop" antenna's dimensions are electrically small. Accordingly, the operating carrier frequency of small-loop antenna is lower than other structures of similar size. This attribute is advantageous for SoC integration, as the circuits that generate the carrier frequency generally consume less power at lower frequencies. The small-loop is

economically feasible for integration in a submicron CMOS process at the 5.2 GHz UNII band (or any frequency band higher than 5.2 GHz).

The fundamental aspects relating to low-power transmitter design are described – namely communication link budgeting, receiver sensitivity, average power consumption, transmit efficiency, and relevant modulation schemes to short-range wireless sensor systems. In a typical communication system, the transmitter could indirectly trade-off power consumption with the receiver through the data rate and receiver sensitivity, respectively, when maintaining an energy-per-bit specification. It is therefore prudent to first minimize the power consumption of the transmitter's modulator as this avoids adjustments to the other specifications of the system. A literature review of low-power transmitter architectures is reported, comparing and analyzing average power consumption and energy efficiency metrics. This revealed the superior performance of oscillator transmitters, and more specifically, with designs which have a low carrier frequency as propagation attenuation is proportional to the square of the carrier's frequency. However, for an SoC transmitter solution, antenna integration in CMOS dictates operating with gigahertz carrier frequencies. Ultimately, the integration challenges associated with a mixed-signal design in a submicron CMOS process are discussed, as well as a limited research review of on-chip oscillator references.

The use of a hybrid power source – an ultracapacitor with a solar cell, for the SoC dosimetry transceiver is proposed. This source's power capabilities are explored, as the size of the ultracapacitor and solar cell depend on the power consumption of the transmitter to transmit a packet and the packet period.

CHAPTER

3. SoC Transceiver Front-End Architecture

The next evolution in semiconductor device integration is the on-chip antenna, a method investigated in this thesis for reducing the form-factor of a wireless system. To demonstrate an integrated antenna that is economically feasible and, more importantly, suitable for low-power short-range communication applications requires properly choosing the process technology, the carrier frequency, the antenna structure and the transceiver front-end architecture. As this research is part of a collaboration effort, the work presented in this chapter predominantly focuses on techniques for the transmitter circuit to drive the integrated antenna with low power consumption. Thus, only a brief overview of the integrated antenna design is discussed in this chapter along with the implementation details. The antenna's design theory is to be disclosed in another thesis by Atif Shamim. Background information on the operation of the integrated antenna has been provided in Section 2.1.

This chapter begins with an overview of IBM's 0.13 μm CMOS technology, and then presents the merits for operating in the 5.2 GHz UNII band with an integrated small-loop antenna. Details of the physical and electrical models for the integrated antenna are disclosed. A receiver design for the transmitter is briefly described and the communication specifications for anticipated wireless links are determined. Then, an oscillator transmitter circuit is introduced which would satisfy these specifications as well as incor-

porates the integrated antenna to realize, together with the RX, an SoC transceiver front-end. Finally, a system analysis of the communication link is explored.

3.1. Technology

IBM's 1.2 V 0.13 μm CMOS technology is selected in which to manufacture the SoC transceiver with an integrated antenna for three main reasons. These reasons are the ease of integration of circuit and antenna structures on the same die without post-processing steps, the low operating voltage facilitating low power consumption, and the availability of excellent device models accessible for Carleton researchers through the Canadian Microelectronics Corporation (CMC).

This technology offers three thick RF metal layers suitable for high-Q inductors, the top metal layer (MA) is composed of aluminium. As this is a submicron CMOS technology, the substrate is of low resistivity silicon for increased latch-up immunity. Integrated antenna design is therefore more challenging as the low resistivity substrate increases the dielectric losses of the structure, thus reducing the antenna's gain and efficiency. This CMOS technology facilitates the implementation of multi-gigahertz RF functions as the MOSFETs can demonstrate a unity current gain frequency (f_T) and unity power gain frequency (f_{MAX}) of close to 100 GHz [49]. Finally, IBM's 0.13 μm CMOS process also makes use of triple-well technology, a feature which will be employed in the layout implementation to provide greater noise isolation between the digital, analog and RF sections of the chip.

3.2. Integrated Small-loop Antenna

Although the antenna's dimensions generally decrease with higher carrier frequencies, the resulting increases in both transmission path-loss and power consumption of the transmitter circuitry to drive the antenna justifies operating with a carrier at lower frequencies. Therefore, a carrier in the 5.2 GHz UNII band would enable a low-power

CMOS transmitter system with a silicon-integrated antenna – the small-loop antenna according to Table 1, while also being economical to manufacture in a semiconductor process. As the transmitter from this research is intended for a wireless biomedical sensor, the location of the receiver is not generally known to the transmitter at the time of communication. For this reason, the small-loop antenna, which exhibits an omni-directional radiation pattern with broad lobes, would be well suited for a wireless application such as this.

3.2.1. HFSS Antenna Model

As part of a collaborative effort, Atif Shamim designed and modelled an integrated single-turn small-loop antenna with Ansoft's 3D High Frequency Structure Simulator (HFSS) for the SoC transceiver. With regard to this structure's electrical properties, a loop is inherently inductive and is well balanced [19] – allowing this antenna to be easily driven by a differential circuit, such as an oscillator transmitter.

The HFSS model of the small-loop antenna disclosed in [9] and [10] is based on a rectangular 1 mm by 1 mm loop composed of aluminium top-metal MA. The simulated differential impedance of the antenna is 7.12 + j66 Ω at 5.2 GHz – the intended carrier frequency, corresponding to a net inductance of 2.0 nH with a quality factor of 9.2. After implementing the antenna, and performing a post analysis of its electrical properties, it was discovered the substrate thickness parameter of the HFSS model had been incorrectly assumed to be 760 μm. This, according to IBM's 0.13 μm CMOS technology documentation, is the thickness of the wafer. However, the wafer's thickness is reduced by the packaging vendor who backgrinds each wafer to a die thickness of 250 μm prior to dicing the wafer [50]. With the substrate thickness parameter corrected to 250 μm, the updated HFSS model exhibits a lower net inductance at 5.2 GHz. This oversight was partly responsible for the carrier frequency of the fabricated transmitter to be shifted upward in the frequency spectrum to 6.3 GHz. Thus, for consistency, the antenna and SoC trans-

ceiver front-end are presented and analyzed in this thesis at the measured operating carrier frequency of 6.3 GHz.

The updated HFSS model of the small-loop antenna, accurately reflecting the structure which was implemented, is a rectangular 675 μm by 825 μm loop composed of aluminium top-metal MA with a trace width of 100 μm as is shown in Figure 3-1. The antenna is to be differentially driven through a pair of feeding paths, which are 200 μm long with a trace width of 10 μm. The simulated differential impedance of the antenna is 3.7 + j54.2 Ω at 6.3 GHz – the operating carrier frequency of the transmitter, corresponding to a net inductance L_{ANT} of 1.37 nH with a quality factor Q_{ANT} of 14.65. The simulated radiation efficiency e_{RAD} of this antenna is 0.06. A 6% radiation efficiency is consistent with other published on-chip antenna work [51]. As shown in Figure 3-2, the integrated antenna displays an omni-directional radiation pattern with a maximum gain of –31.7 dBi (θ = -90°, φ = 0°). The antenna exhibits a non-directional pattern in the x-y plane (θ = 90°) and a broad double lobe pattern in the y-z plane (φ = 90°). In the x-z plane (φ = 0°), the lobes are unsymmetrical due to the presence of the antenna feed port along the positive side of the x-axis. As the radiated power is maximum in the plane of the loop, defining the antenna's boresight, the antenna is displaying the radiation pattern characteristics of a "small loop" antenna. Accordingly, nulls exist along the z axis, perpendicular to the plane of the loop. Although the circumference of this rectangular loop, at 3 mm, is larger than the estimated size for a small-loop antenna from Table 1, HFSS is nevertheless predicting that the criterion for a small-loop radiation pattern is satisfied at this carrier frequency. HFSS simulations have also predicted that when the antenna is placed on an infinite-size highly conductive ground plane, a greater portion of the radiated energy is directed upwards which causes the antenna's gain in those directions to increase.

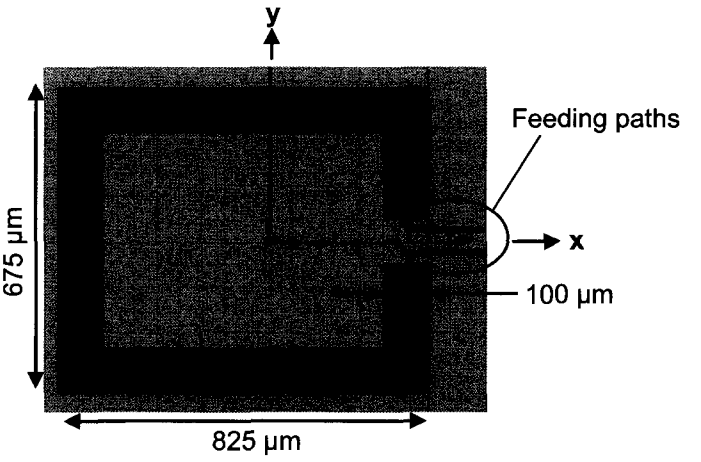

Figure 3-1: HFSS model of the antenna.

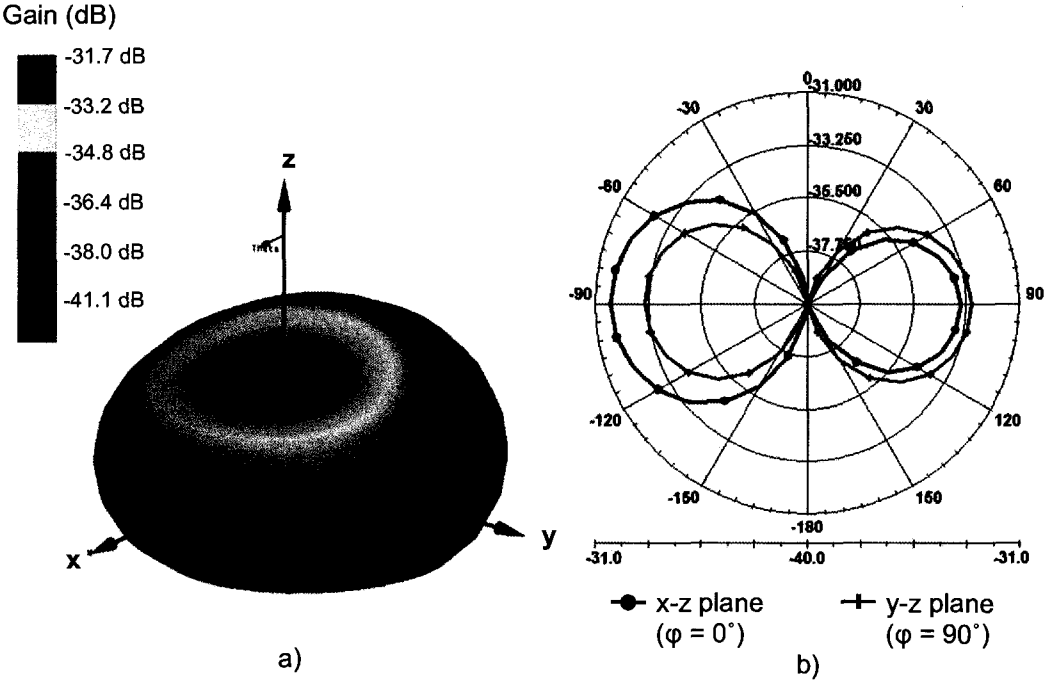

Figure 3-2: HFSS radiation pattern and gain simulation; a) 3D and b) 2D.

3.2.2. Equivalent Lumped Circuit

From HFSS's simulated differential s-parameters of the antenna model, an equivalent differential lumped circuit is generated using the optimization routine in Agilent's ADS which matches the lumped circuit's simulated s-parameters with that of the antenna over the frequency range of interest. The lumped circuit can then be used in circuit-level simulations of the transmitter and receiver. In the lumped circuit shown in Figure 3-3, R_{series}, R_{SUB}, C_{OX}, C_{SUB} and L_{series} represent the series resistance, the substrate resistance, the oxide capacitance, the substrate capacitance and the series inductance associated with the integrated antenna, respectively [52].

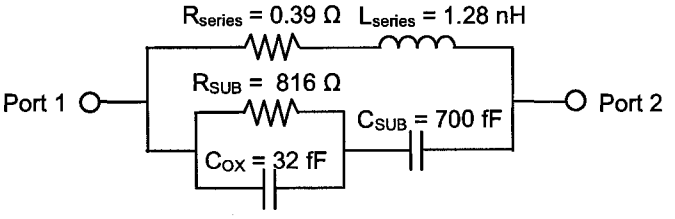

Figure 3-3: Equivalent lumped circuit of the antenna.

A comparison of the differential s-parameters (S_{11}) of the HFSS antenna model and its equivalent lumped circuit from 1 GHz to 10 GHz are shown in Figure 3-4 a) and b), respectively. Since the antenna is to serve also as an inductor, the net inductance and quality-factor (Q) are properties of interest. Figure 3-5 and Figure 3-6 are plots over frequency of the net inductance and Q, respectively, from the impedances of the HFSS antenna model and its equivalent lumped circuit.

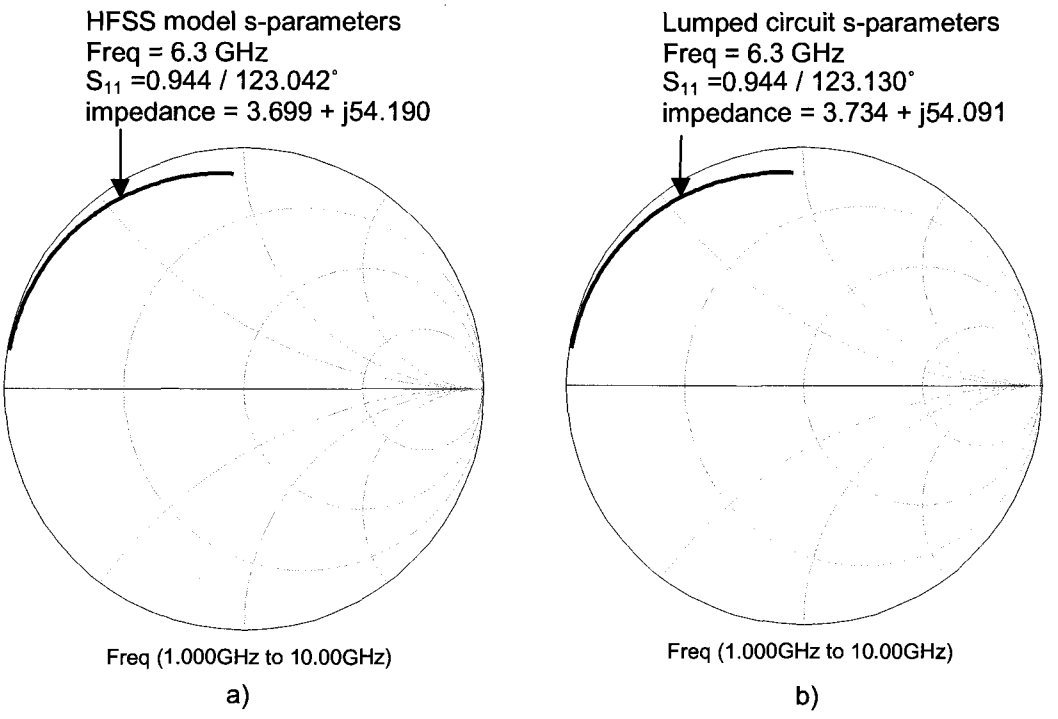

Figure 3-4: Simulation; S_{11} a) HFSS antenna model and b) lumped circuit.

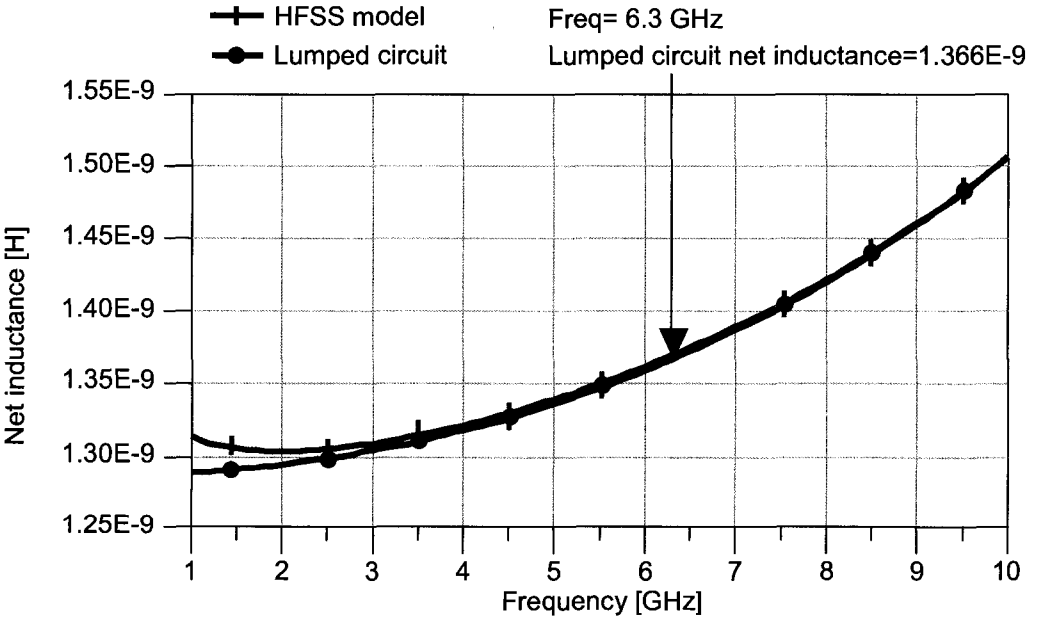

Figure 3-5: Inductance comparison of HFSS antenna model and lumped circuit.

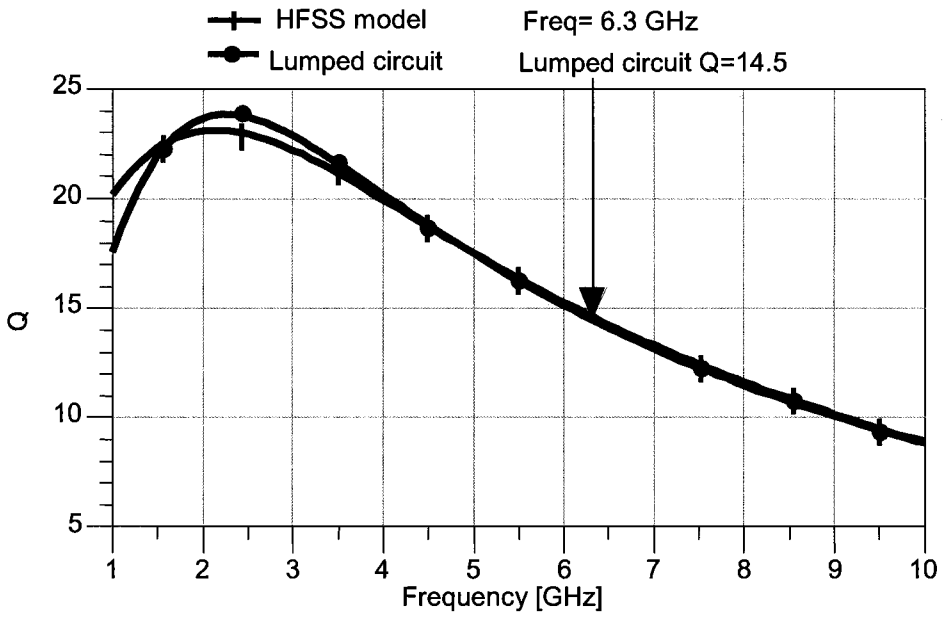

Figure 3-6: Q comparison of HFSS antenna model and lumped circuit.

3.3. Receiver Considerations

The transmitter is to communicate with the injection-locked receiver (RX) of the topology presented in [10] which Peter Popplewell designed and implemented. Here, the RX makes uses of a low noise amplifier (LNA) and a traditional 3rd order PLL, as illustrated in Figure 3-7, to receive and demodulate a BFSK signal. The RX's PLL is initially locked to the centre frequency of the BFSK signal, i.e. f_0 = 6.3 GHz. Then the loop is opened, allowing the free-running VCO to be injected-locked by the LNA with an FM modulated signal of sufficient amplitude. With a gain of 20 dB, the LNA is connected to an antenna to capture and amplify the incoming FM (BFSK) modulated carrier. When the amplitude of the injected voltage V_{inj} is much smaller than the amplitude of the free-running oscillator V_{osc}, the single-sided injection-locking bandwidth f_L of the VCO can be approximated by [53]

$$f_L \approx \frac{f_0}{2Q_U}\frac{V_{inj}}{V_{osc}} \tag{3.1}$$

where f_0 is the oscillation frequency and Q_U is the quality factor of the unloaded tank circuit. The oscillator in the receiver can be injection-locked from $f_0 - f_L$ to $f_0 + f_L$ for a given V_{inj}, and therefore requiring the frequency shifts Δf of the carrier to be less than f_L. For demodulation, the carrier frequency is divided down by 64 and compared to the reference frequency of 98.4375 MHz (= f_0 / 64) at the phase-frequency detector (PFD). Here, the PFD will send pump-up signals to the charge pump (CP) blocks when the reference frequency is greater (by Δf / 64 or less) than the instantaneous divided-down carrier frequency (corresponding to when the carrier is $f_0 - \Delta f$ frequency shifted). Similarly, the PFD will send pump-down signals to the CP blocks when the reference frequency is less (by Δf / 64 or less) than the instantaneous divided-down carrier frequency (corresponding to when the carrier is $f_0 + \Delta f$ frequency shifted). Based on the PFD's outputs, the second CP will generate a logic "0" signal from pump-up signals and a logic "1" from pump-down signals, thus demodulating the received bitstream encoded in the carrier. A drawback with this demodulator is that when there is a bit transition, the PFD requires a finite amount of time to deduce a "0" or a "1". As explained in [10], this time delay is dependent on the phases of the reference and the divided-down carrier when the transition occurs. The maximum delay is equal to the beat period T_{beat} based on the inputs to the PFD and is given by

$$T_{beat} = \frac{1}{\Delta f / 64}. \tag{3.2}$$

Therefore, this maximum delay should be no greater than two-thirds of the bit period to ensure the PFD has sufficient time to compare its inputs, and thus sets a fundamental limit on the data rate of the bitstream in the modulated signal. The relationship between the maximum data rate and the frequency deviation is analytically given by

$$R_{data} = 66.7\% \cdot (\Delta f / 64). \tag{3.3}$$

The oscillator of the receiver is to have a free-running differential peak-to-peak swing of V_{osc} = 1.0 V and a tank inductor with $Q_U \approx 5$ after degeneration. Thus at an operating frequency of f_0 = 6.3 GHz, the required voltage for injection-locking the oscillator

is 952 μV for a locking bandwidth of f_L = 600 kHz according to (3.1). As this injection-locking signal is to be provided from an LNA with 20 dB of voltage gain, the corresponding power level at the input to the LNA is P_{RX} = –88.5 dBm, assuming the LNA is conjugately matched to the integrated antenna. At this power level (or greater), the receiver would be able to sufficiently capture a 6.3 GHz BFSK carrier with a Δf = 500 kHz. Since this frequency deviation corresponds to a beat period of 128 μs, according to (3.3) the maximum data rate of the bitstream should be $R_{data} \approx$ 5 kbps for the receiver. Thus describing a WBFM carrier with a modulation index m = 200.

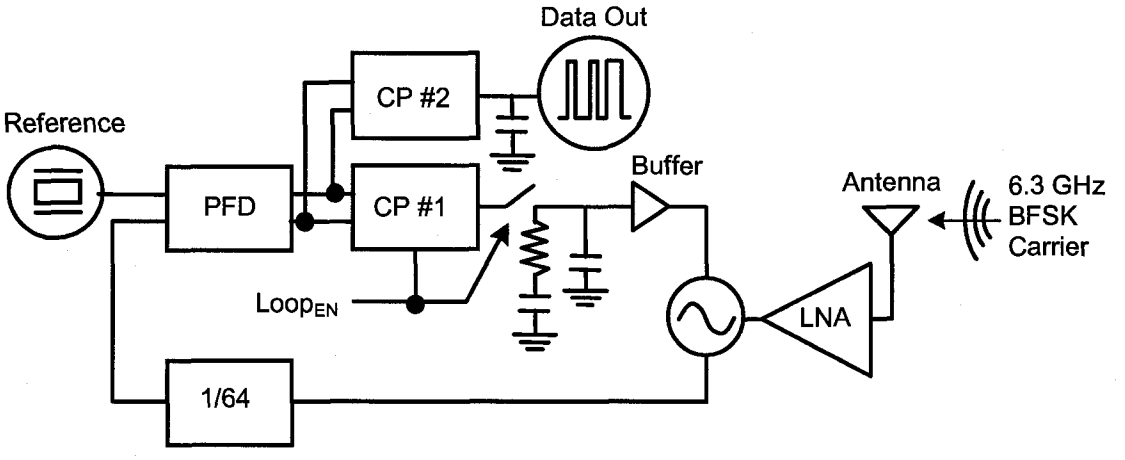

Figure 3-7: Injection-locked receiver and demodulator.

3.4. Communication Range

The communication link between the proposed transmitter and receiver is governed by (2.31). Assuming conjugate matching to the antenna's impedance, the same integrated antenna of Section 3.2 with a $G_{TX} = G_{RX}$ = –31.7 dBi is used by the TX and RX, the receiver's sensitivity at –88.5 dBm is used as the power delivered to the receiver's antenna P_{RX} (as this is equal to the power delivered to the receiver's LNA based on the above assumption), and the TX is able to deliver 0 dBm of power to the antenna, a communication

range of 6.5 cm is possible for a 6.3 GHz carrier provided the antennas' polarizations are aligned. This is illustrated in the plot of Figure 3-8 and in the block diagram of Figure 3-9, as well as the case for an off-chip receiver 50 Ω patch antenna with a gain of 6.7 dBi which suggests the communication range can be increased to 1.3 m. The latter case illustrates an interesting point, given that the gain increased by 6.7 + 31.7 = 38.4 dB, this did not materialize directly in an improvement in distance of 19.2 dB according to the Friis transmission equation of (2.31), but rather improved only 13 dB. The reason is because a larger receiver sensitivity of –76.4 dBm is necessary at the 50 Ω input of a conjugately matched LNA for an injected voltage of V_{inj} = 952 μV at the receiver's oscillator, assuming the LNA's 20 dB of voltage gain is maintained. For either case, the TX should be designed to deliver 0 dBm or greater to its antenna for wireless biomedical sensors applications as discussed in Section 1.1.

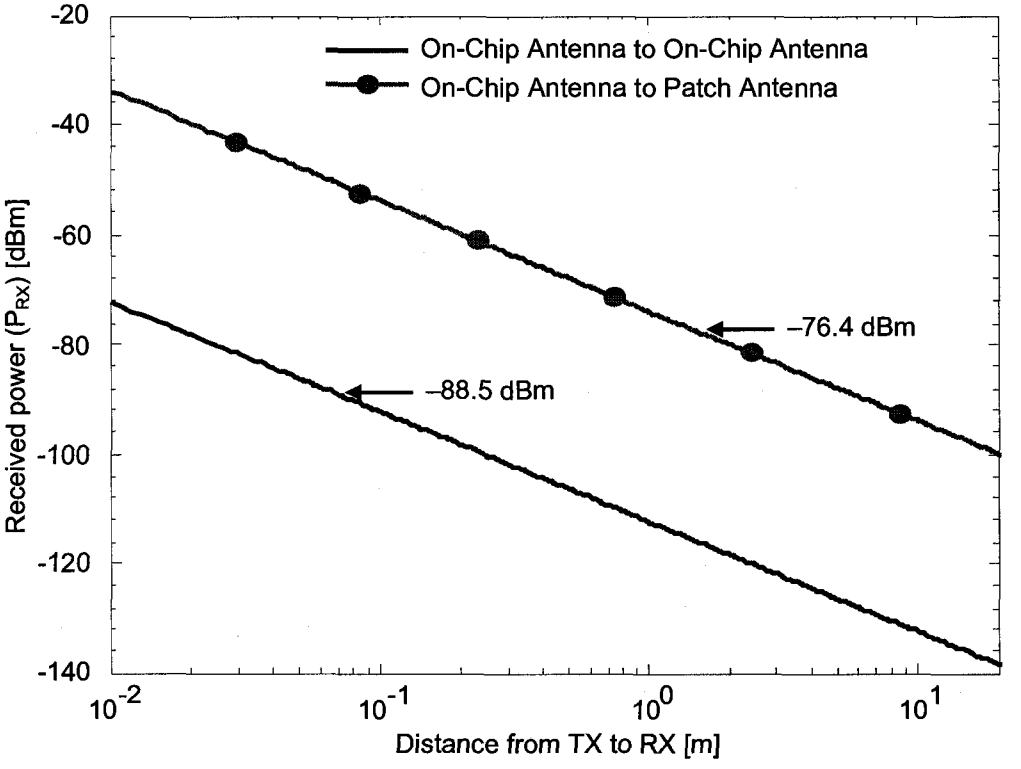

Figure 3-8: Communication range estimate.

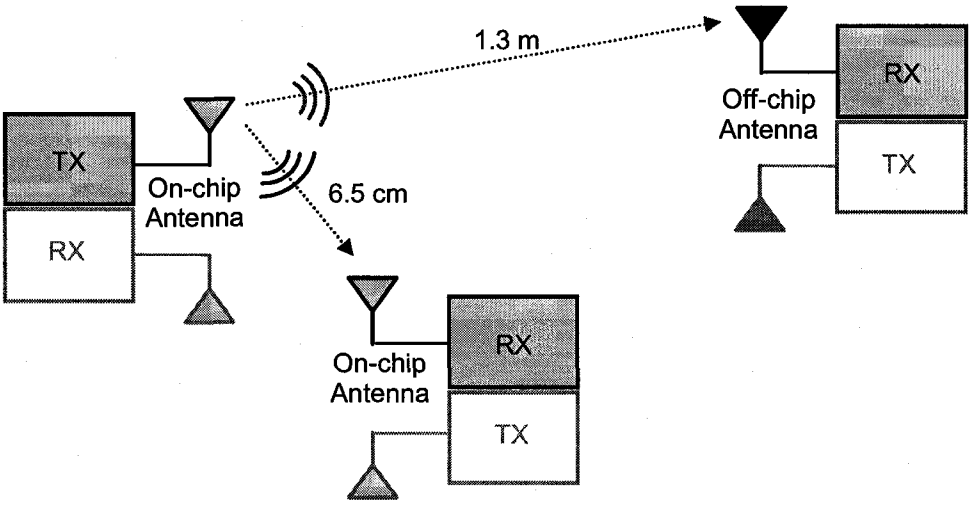

Figure 3-9: Communication link set-up options.

3.5. Oscillator Transmitter

Of the transmitter architectures reviewed and discussed in Subsection 2.2.4, the oscillator transmitter demonstrated superior low average transmitter power consumption and high transmit efficiency. This topology is also best suited to incorporate the integrated antenna for short-range communication. The primary reason is that with the inductive properties (L_{ANT} and Q_{ANT}) of the antenna, it can serve as a differential inductor in the oscillator's resonant tank and permit an efficient method to radiate the carrier. In addition, this topology removes the need for a power amplifier – a potential power saving for the system. Thus, for this work, a 6.3 GHz oscillator transmitter (TX) is proposed, with link budget specifications for short-range communication as determined in this chapter. Unlike other published designs, this oscillator transmitter would be the first circuit implementation with an integrated inductive antenna which is designed as a far-field and omni-directional radiating element. The circuit design details of the TX are presented in Chapter 4.

Implementing a multi-gigahertz oscillator with IBM's 0.13 μm CMOS process is undemanding due to the high f_T and f_{MAX} of this technology's MOSFETs. FM modulation

of the carrier is achieved by varying the oscillation frequency through a varactor. The varactor is voltage-controlled by a modulation line where the data bitstream is directly applied; a block-level model of this voltage-controlled oscillator is shown in Figure 3-10. The amplitude of the bitstream and the gain of the varactor are chosen to shift the carrier from 6.2995 GHz to 6.3005 GHz for a BFSK spectrum with a Δf = 500 kHz. To determine if sufficient power is radiated for short-range communication, the real power delivered to the inductive antenna is examined. Considering that the supply voltage for this technology is 1.2 V, the differential peak voltage across the inductive antenna V_{ANT_diff} is assumed to be 1.2 V. The power delivered can then be calculated by applying this voltage across the differential real impedance of the antenna, R_{ANT_diff}. According to the antenna's series resistance R_{ANT} = 3.7 Ω and quality factor Q_{ANT} = 14.65, the differential resistance can be found with the following impedance transformation

$$R_{ANT\_diff} = R_{ANT}(Q_{ANT}^2 + 1) = 798\Omega. \tag{3.4}$$

Thus, the power delivered to the antenna is expected to be $P_{TX} = V_{ANT\_diff}^2 / (2R_{ANT\_diff}) =$ 903 μW, or approximately 0 dBm, which is sufficient for short-range communication according to Figure 3-8. Since the antenna's radiation efficiency is 6%, the power radiated is $P_{RAD} = 0.06 \cdot P_{TX} = 54.2$ μW.

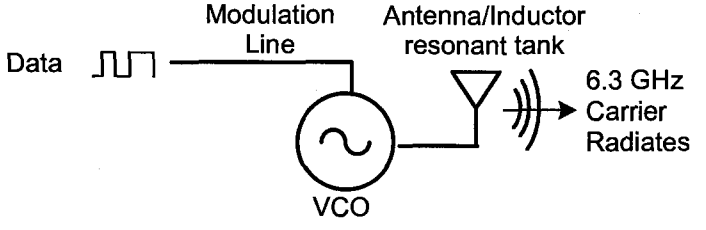

Figure 3-10: Oscillator transmitter (directly modulated) model.

3.6. System Analysis

The link budget analysis between the proposed TX and RX showed a predicted communication range as a function of power collected at the receiver. Revisiting this relation-

ship for the case when the RX is fitted with a 6.7 dBi off-chip patch antenna, it is possible that the link could support higher data rates (greater than 5 kbps) when the communication range is reduced (lower than 1.3 m). For instance, according to (3.3), a higher R_{data} would require a proportionally larger frequency shift of the BFSK carrier. To ensure this larger Δf will injection-lock the receiver's VCO, its single-sided injection-locking bandwidth f_L would have to increase by the same proportion. According to (3.1), this could be achieved by an increase in the amplitude of the injected voltage V_{inj} which requires greater power to be collected from the receiver's antenna. Thus, from this system's link budget (2.31), a higher P_{RX} is achieved when the communication range is reduced if the TX is sustaining a 0 dBm power-level delivered to the transmit antenna. The dynamic relationship between the communication range, data rate, and RX injection-locking bandwidth can be shown graphically in Figure 3-11. Therefore, it is possible to optimize the data rate depending on the communication range from the TX to RX. For example, at a distance of 1 cm, the data rate can be as high as 759 kbps.

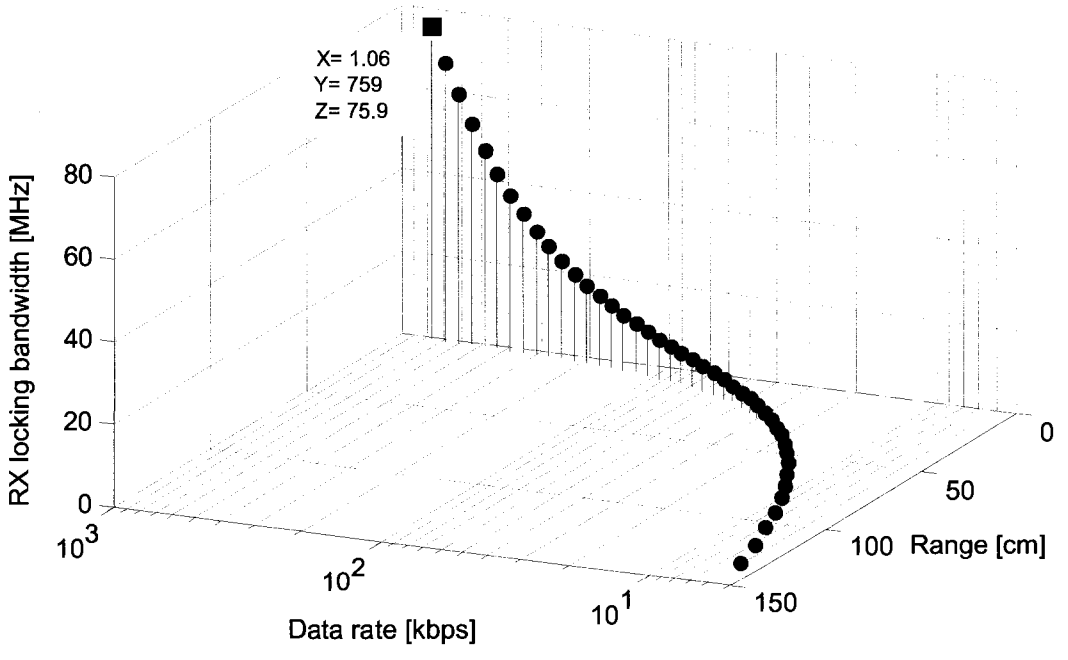

Figure 3-11: Range, data rate, and RX injection-locking bandwidth.

3.7. Transceiver Front-End Summary

IBM's 0.13 μm CMOS technology is selected in which to manufacture the SoC transceiver with an integrated antenna that is economically feasible and theoretically suitable for low-power short-range communication applications.

The integrated antenna is a small-loop structure for the 5.2 GHz UNII band, which is more advantageous with regards to propagation path-loss and transmitter power consumption than other integrated antenna structures of similar size which require operation at much higher carrier frequencies. This antenna is physically modelled in HFSS, however a modelling oversight resulted in the antenna (and transmitter) operating at 6.3 GHz. At this frequency, an updated HFSS model predicted a L_{ANT} of 1.37 nH with a Q_{ANT} of 14.65 and exhibited an omni-directional radiation pattern with a maximum gain of –31.7 dBi and a 6% radiation efficiency. From the simulated differential s-parameters of the HFSS antenna model, an equivalent differential lumped circuit model is generated in Agilent's ADS.

The RX of the SoC transceiver is an injection-locked topology – the integrated small-loop antenna is connected to an LNA which is electrically coupled to an oscillator for receiving a BFSK signal at 6.3 GHz, and uses a traditional 3rd order PLL to demodulate the signal. For a Δf of 500 kHz, the mechanism for demodulation supports a maximum data rate of 5 kbps. The injection-locking characteristics support a minimum receiver sensitivity of –88.5 dBm.

A communication link study determined the power delivered to the transmitter's antenna should be a minimum of 0 dBm. For an RX conjugately matched to the integrated antenna, a communication range of 6.5 cm can be supported. This distance can be increased to 1.3 m when the RX is conjugately matched to a 50 Ω patch antenna with a gain of 6.7 dBi.

To satisfy these communication ranges, the TX of the SoC transceiver is based on an oscillator transmitter circuit, allowing the integrated small-loop antenna to serve as a

differential inductor in the oscillator's resonant tank and permitting an efficient method to radiate the carrier. BFSK FM modulation of the carrier is achieved by varying the oscillation frequency through a varactor.

The communication link can support higher data rates as the power collected at the receiver is increased. This increase is evident when the RX is fitted with a 6.7 dBi off-chip patch antenna and the communication is reduced from 1.3 m while the transmit power is held constant. The dynamic relationship between the communication range, data rate, and RX injection-locking bandwidth is graphically explored in Figure 3-11.

CHAPTER

4. Open-Loop Modulation TX Design

The integration challenges for a wireless biomedical sensor can be addressed with the implementation of an energy-efficient direct open-loop modulation transmitter. Open-loop modulation is a technique explored to lower the power consumption of the transmitter, during a data packet transmission, such that the system can be powered by an on-chip ultracapacitor and solar cell combination. Making use of an integrated antenna to communicate, this transmitter is therefore revolutionary in that it is a completely integrated SoC.

In this chapter, a PLL-based modulator is disclosed which incorporates the oscillator transmitter of Section 3.5. The resulting architecture is a direct modulation transmitter, and its operation modes are briefly explained. Then, the design details of the transmitter's components from a schematic capture in Cadence's Virtuoso Analog Design Environment are presented, as well as circuitry realized to test and debug parts of the modulator.

4.1. TX Architecture

As the RX is anticipating a 6.3 GHz carrier, with a +/- 500 kHz frequency deviation according to BFSK modulation, the oscillator transmitter must be able to accurately generate this carrier frequency to communicate. To implement an oscillator transmitter for this

specification is nearly impossible because of the limits in device and parasitic modelling in the design phase and process variations in the fabrication phase, both of which can affect the oscillation frequency. Thus, a PLL is needed to accurately set the carrier frequency of the oscillator via a varactor (other than the one connected to the modulation line). However, the low-frequency components of direct VCO modulation will be corrupted by the high-pass filtering of the loop. To eliminate the loop feedback mechanism on the VCO, the PLL is opened prior to the start of modulation at the filter line by a switch, as illustrated in the block-level diagrams of Figure 4-1 and Figure 4-2 when the switch is closed and opened, respectively. When the PLL is opened, the VCO is then directly modulated, realizing a direct open-loop (OL) modulation transmitter design. With no PLL feedback, the VCO's output frequency is vulnerable to being pulled by interferers and noise. However, as previously mentioned, the frequency drift can be made minimal at 2.5 Hz/μs with careful design for a low-voltage VCO in a modern semiconductor process [31].

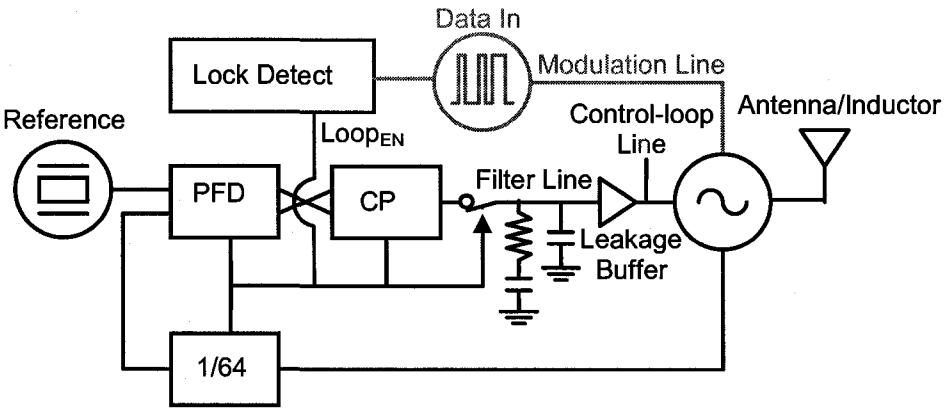

Figure 4-1: Direct modulation transmitter topology in closed-loop mode.

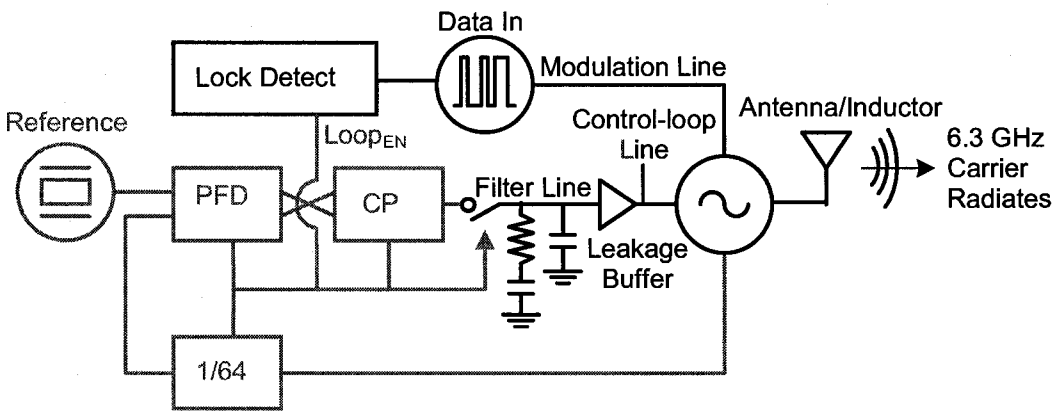

Figure 4-2: Direct modulation transmitter topology in open-loop mode.

As concluded in Subsection 2.2.2 Power and Efficiency, for a low-power short-range transmitter design, it is necessary to minimize the power consumption of the modulator to achieve a low P_{TX_avg} as this avoids adjustments to other specifications of the system – namely at the receiver. In addition to this, for implementing an energy-efficient transmitter design, requires the modulator to have a fast power-up time.

The proposed direct OL modulation transmitter can satisfy both of the design guidelines mentioned above. In closed-loop mode, the power of the modulator during $T_{power\text{-}up}$ is equal to that of the PLL, P_{PLL}, and the PLL should be designed for a fast acquisition time. In open-loop mode, the power of the modulator during $T_{transmit}$ can be reduced by turning off the circuit blocks which are not necessary for OL modulation, namely the reference oscillator, PFD, CP and divider, all of which have been grayed out in Figure 4-2. Thus, the modulator's power consumption is lowered to approximately that of the VCO. A revised expression for the transmitter's average power consumption is given by

$$P_{TX\_avg} \approx \frac{P_{PLL} \cdot T_{power-up} + P_{VCO} \cdot T_{transmit}}{T_{packet}} \tag{4.1}$$

where P_{VCO} is the power consumption of the VCO, and assuming the non-grayed circuit bocks in Figure 4-2 consume relatively low power. Similarly, the expression for transmit efficiency η_{TX} can be revised to

$$\eta_{TX} \approx \frac{P_{ANT}}{P_{VCO}}. \tag{4.2}$$

4.1.1. Direct OL Modulation Transmitter Behaviour

With reference to the timing diagram of Figure 2-10, illustrating the sequence for a packet transmission, the direct OL modulation transmitter of Figure 4-1 is powered up after a predetermined period of inactivity, T_{off}. During $T_{power\text{-}up}$, the PLL operates in a closed-loop mode and locks the VCO to a multiple of the reference. For a reference signal at 98.4375 MHz, the VCO is locked to 6.3 GHz. Six fixed divide-by-two prescalers are cascaded together to form the divider instead of a multi-modulus divider design. The resulting lack of channel selection is not considered serious since one TX is expected to be the only one operating in the area (or another TX is expected to have a different reference frequency or timing synchronization). Once the VCO is phase locked, a lock detection circuit triggers the loop to open (via $Loop_{EN}$), and the control-loop line voltage for a VCO frequency of 6.3 GHz is momentarily held on the second order loop filter. With the PLL in open-loop mode as shown in Figure 4-2, a unity gain buffer, referred to as the leakage buffer, between the filter and VCO minimizes charge leakage and hence VCO drift. The digital bitstream containing the input data is switched onto a modulation line for the period of $T_{transmit}$, and the VCO spectrum is FM modulated (BFSK) in accordance with the bits in the data packet. Furthermore, during open-loop VCO modulation, energy is conserved by turning off the reference, PFD, CP and divider.

The leakage buffer, to be discussed in Section 4.6, is an inverting unity gain amplifier. This added inversion in the PLL's loop results in a positive feedback to the VCO. To re-establish the negative feedback required for phase locking the loop, another inverter must therefore be introduced after the PFD. Alternatively, the inversion can be

accomplished by swapping the outputs of the PFD to the CP. The latter is the option applied to this PLL design, as shown in Figure 4-2.

4.2. Voltage-Controlled Oscillator

This section begins by exploring *LC* VCO topologies, for an oscillator transmitter application, and start-up considerations. Next, the steady-state operation of the VCO is described in terms of two regimes, current-limited and voltage-limited, and the performance metric, oscillator efficiency, is discussed. Then, a design technique to achieve simultaneous *gm* and impedance matching with power optimization is introduced. Finally, this technique is applied to a VCO design for the proposed TX.

4.2.1. Topology and Start-up Considerations

From the power delivered specification for the transmitter's antenna, a differential peak voltage across the inductive antenna of around 1.2 V, i.e. the supply voltage, is required. A complementary *LC* VCO topology is implemented as shown in Figure 4-3 a); variants of this design either have a tail-biased (illustrated below), top-biased or no current source. The differential operation of this VCO suppresses the circuit's sensitivity to undesired common-mode substrate noise generated from the other blocks on the chip. Alternative differential *LC* VCO topologies exist, such as tail- or top-biased cross-coupled N-channel metal-oxide-semiconductor (NMOS) or P-channel metal-oxide-semiconductor (PMOS) VCO configurations. However, these topologies would require a single-loop inductor with a centre-tap for DC biasing which would negatively impact this structure's radiation characteristics if it is also serving as an antenna.

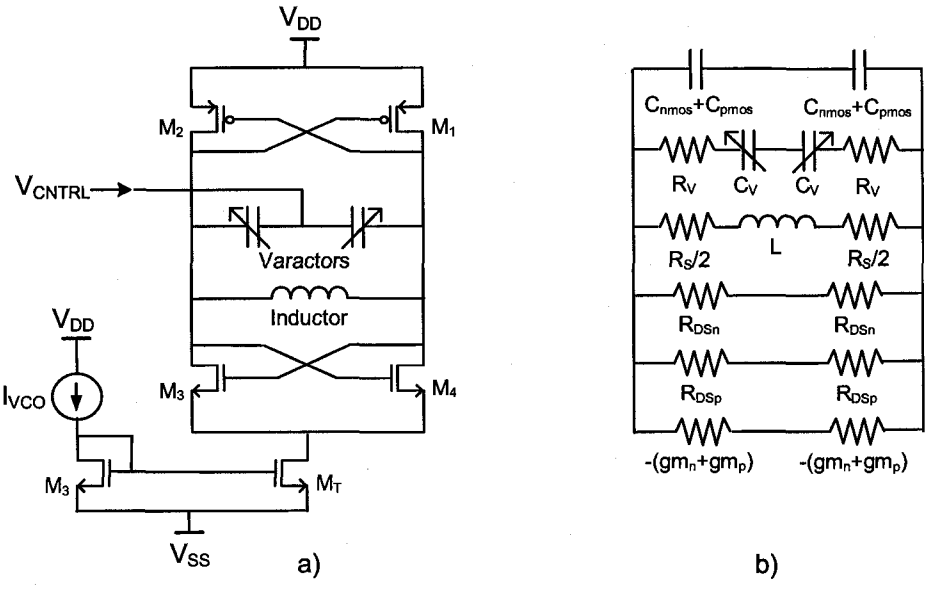

Figure 4-3: *LC* VCO; a) complementary cross-coupled schematic and b) equivalent small-signal circuit.

In Figure 4-3, the total device parasitic capacitances of the cross-coupled NMOS (M_3 and M_4) and PMOS (M_1 and M_2) transistors are represented by C_{nmos} and C_{pmos}, respectively. A set of frequency control varactors, with a capacitance dependent on the voltage signal V_{CNTRL}, is represented by C_V. The small-signal transconductance of the NMOS and PMOS transistors are given by gm_n and gm_p, respectively. Similarly, the output resistance of the NMOS and PMOS transistors are given by R_{DSn} and R_{DSp}, respectively. As the operating point of the transistors will vary over the course of the oscillation cycle, the values for these parameters are considered when the voltage across the *LC* resonator tank is zero – a legitimate approximation according to [54].

A cross-coupled transistor latch forms a negative conductance. For the complementary VCO, the equivalent negative conductance of the NMOS and PMOS latches is given by

$$Gm_{eff} = -(gm_n + gm_p)/2. \tag{4.3}$$

The equivalent negative impedance Zm_{eff}, the inverse of Gm_{eff}, is to compensate for the losses seen by the LC tank resonator. The equivalent parallel resistance of these losses [55] is given by

$$R_{TANK} = 2R_{DSn} // 2R_{DSp} // R_I \cdot (Q_L^2 + 1) // 2R_V \cdot (Q_C^2 + 1), \tag{4.4}$$

where the parasitic series resistance of the inductor R_I is transformed to a differential resistance from the inductor's quality factor Q_L, and the parasitic series resistance of the varactor R_V is transformed to a differential resistance from the varactor's quality factor Q_C. For the VCO to oscillate, $|Zm_{eff}|$ must be less than or equal to R_{TANK} to overcome all resistive losses. Then, the LC resonator becomes purely reactive and resonates without amplitude attenuation. To guarantee oscillation start-up under all operating temperatures and worst-case process variations, $|Zm_{eff}|$ is typically around 3 times smaller than R_{TANK}, and therefore

$$|Zm_{eff}| = \left|\frac{1}{Gm_{eff}}\right| = \frac{R_{TANK}}{3}. \tag{4.5}$$

The impedance of the inductive element in Figure 4-3, L_{TANK}, is transformed to a parallel inductance which is given by

$$L_{TANK} = L \cdot Q_L^2 / (Q_L^2 + 1). \tag{4.6}$$

Similarly, the varactors are transformed to parallel capacitances, and together with device parasitics C_{nmos} and C_{pmos}, form an equivalent parallel capacitance which is given by

$$C_{TANK(V_{CNTRL})} = 1/2 \cdot [C_{nmos} + C_{pmos} + C_{V(V_{CNTRL})} \cdot Q_C^2 / (Q_C^2 + 1)]. \tag{4.7}$$

C_{nmos} is primarily composed of the gate-to-source capacitance C_{gs}, the drain-gate capacitance C_{dg}, and the drain-to-bulk capacitance C_{db} – all of which are proportional to gate width. C_{nmos} is given by

$$C_{nmos} = C_{gs,n} + 4C_{gd,n} + C_{db,n}, \tag{4.8}$$

where the subscript "n" denotes reference to an NMOS device [54]. A corresponding expression for C_{pmos} can be given in terms of the parasitics of the PMOS device. The

above inductive and capacitive elements of the complementary VCO, L_{TANK} and C_{TANK}, form the circuit's resonant tank with a frequency of oscillation f_{OSC} given by

$$f_{OSC(V_{CNTRL})} = \frac{1}{2\pi\sqrt{L_{TANK} \cdot C_{TANK(V_{CNTRL})}}}. \tag{4.9}$$

4.2.2. Current-Limited and Voltage-Limited Regimes

The steady-state operation of the VCO can be classified into two different regimes; namely the current-limited and voltage-limited regimes [56, 57]. This simplified view of the mechanism that determines the oscillator's output amplitude will provide useful insight for designing a power-efficient oscillator transmitter.

The VCO in Figure 4-3 is considered operating in the current-limited regime when the output swing across the LC tank is primarily a function of the bias current I_{VCO} and is within the available voltage headroom – determined by the supply voltages and the drain-source voltage of M_T. As the bias current is increased, the output swing eventually becomes voltage limited, and thus the VCO is considered operating in the voltage-limited regime. The amplitude of the steady-state output swing V_{TANK} is plotted as a function of I_{VCO} in Figure 4-4.

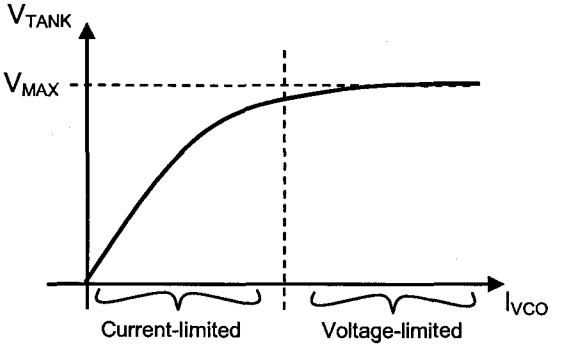

Figure 4-4: VCO output voltage amplitude V_{TANK} vs. bias current I_{VCO}.

In the current-limited regime, the output swing is typically large enough to fully commutate the bias current of Figure 4-3 through the LC tank of the VCO. This, in ef-

fect, produces a +/- I_{VCO} current square-wave flowing differentially across the LC tank. From the Fourier series expansion of a square-wave, the amplitude of fundamental harmonic is $4/\pi \cdot I_{VCO}$. As higher order harmonics are shorted through the tank's capacitor, the differential output voltage amplitude in the current-limited regime is given by

$$V_{TANK} = I_{TANK} \cdot R_{TANK} = \frac{4}{\pi} I_{VCO} \cdot R_{TANK} \quad \text{(current-limited)}. \tag{4.10}$$

where I_{TANK} is the current through the tank's equivalent resistance. At higher frequencies, however, the finite switching time of the transistors and limited gain cause I_{VCO} to behave more like a sinusoidal wave, and therefore the tank voltage would then be approximated as $V_{TANK} \approx I_{VCO} \cdot R_{TANK}$. As the bias current is increased, the gate-source voltages of the cross-coupled NMOS pair (M_3 and M_4) and PMOS pair (M_1 and M_2) increase by approximately the square root of I_{VCO}. Consequently, the drain-source voltage of current source transistor M_T is eventually reduced to the point where M_T enters the triode region of operation – whereupon the VCO transitions from the current-limited to the voltage-limited regime. The differential output voltage amplitude in the voltage-limited regime is given by

$$V_{TANK} = V_{MAX} \propto I_{MAX} \cdot R_{TANK} \quad \text{(voltage-limited)}, \tag{4.11}$$

where V_{MAX} is saturated output voltage of the VCO and I_{MAX} is saturated drain current of M_T.

4.2.3. Oscillator Transmitter Efficiency

In designing a complementary LC VCO as an oscillator transmitter, the resonant tank's inductor is to serve as a far-field radiating element when implemented as a small-loop structure. Therefore, this structure's R_{ANT} and Q_{ANT} are equivalent to the parasitic series resistance R_1 and quality factor Q_L of an inductor, respectively. Generally, the primary design goal of the circuit driving the antenna is to maximize the power delivered to the antenna ($P_{TX} = P_{ANT}$). This is essential for establishing the longest communication range, according to the Friis transmission equation of (2.31), as P_{TX} is directly related to the ra-

diated power (P_{RAD}) by the antenna's radiation efficiency (e_{RAD}) property. However, in an SoC transmitter design P_{RAD}, and hence P_{TX}, must be maximized efficiently to prolong the cycle-life of the power source – especially when the source is implemented on-chip. Therefore, an efficiency metric of the oscillator transmitter circuit should be investigated for optimization.

For oscillator transmitter design, the PA efficiency can be readily adapted from (2.37) to an oscillator power efficiency performance metric given by

$$\eta_{P-VCO} = \frac{\textit{Power dissipated in antenna}}{\textit{Power consumed}} = \frac{P_{ANT}}{P_{VCO}} = \frac{P_{ANT}}{P_{ANT} + 2P_V + 2P_{nmos} + 2P_{pmos} + P_{MT}}, \quad (4.12)$$

a ratio of the power delivered to the antenna to the DC power consumed by the VCO P_{VCO} – which includes the power dissipated by the antenna (P_{ANT}), the varactors ($2P_V$), the cross-coupled NMOS transistors ($2P_{nmos}$), the cross-coupled PMOS transistors ($2P_{pmos}$) and the current source transistor M_T (P_{MT}).

The complementary transistor pairs (M_2 & M_4, M_1 & M_3) of this oscillator work to commutate current through the antenna load in a manner which similar to that of the "push-pull" Class B amplifier in Figure 4-5 a). The push-pull amplifier features a pair of complementary transistors (M_{B1} & M_{B2}) where M_{B2} turns on when the sinusoidal input signal is positive and then pulls current i_{B2} from the load R_L while M_{B1} is off. Alternatively, when the input signal is negative, M_{B1} turns on and then pushes current i_{B1} into the load while M_{B2} is off. At the amplifier's output, the DC components and the even harmonics of i_{B1} and i_{B2} cancel, leaving only the fundamental component i_{B1} - i_{B2} = $I_P \cdot \cos(\omega t)$, where I_P is the amplitude of this current.

As mentioned in Subsection 2.2.2, the classification of an amplifier is according to the fraction of a full input cycle for which current is flowing in the driver transistor [22]. This fraction is generally described by the conduction angle θ_C. For instance, if the current is always flowing, the conduction angle is 360° and the operation is Class A. If the current is flowing for half the input cycle, the conduction angle is 180° and the opera-

tion is Class B. A conduction angle between 180° and 360° is Class AB operation. Class C operation is when the conduction angle is between 0° and 180°. From the time domain waveforms in Figure 4-5 b), the conduction angle of the push-pull amplifier is 180° and thus the maximum theoretical efficiency is 78% for Class B operation. Equally, it should be theoretically possible to attain this efficiency with the complementary *LC* VCO. However, one can expect realistic efficiencies to be less, and the VCO to likely exhibit Class AB operation. Therefore, an achievable oscillator power efficiency target of ≈ 50% is considered for this complementary *LC* VCO design.

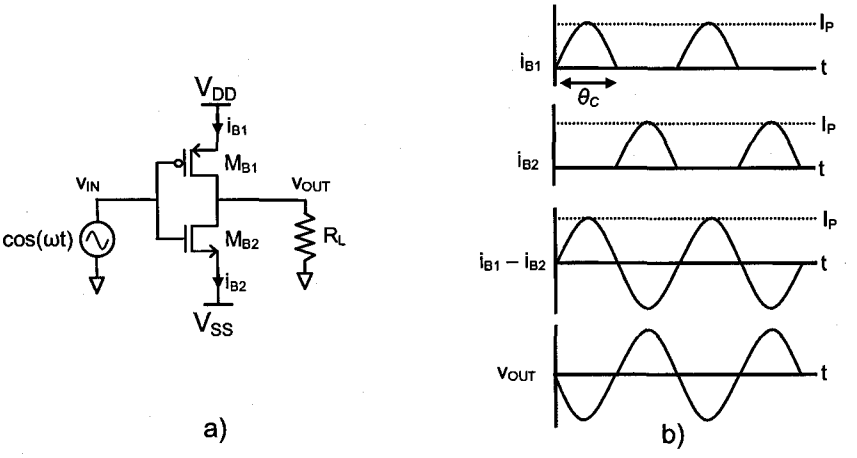

Figure 4-5: Class B push-pull amplifier; a) schematic and b) waveforms.

Consider the case of an integrated complementary *LC* VCO design with a $Q_L << Q_C$ and the power dissipated by the varactors is minimal. When the VCO is operating in the current-limited regime, oscillator power efficiency can be expressed as

$$\eta_{P\text{-}VCO} = \frac{P_{ANT}}{P_{VCO}} = \frac{I_{ANT}^{\,2} \cdot R_{ANT\_diff} / 2}{I_{VCO} \cdot V_{DD}} \tag{4.13}$$

where I_{ANT} is the current through the inductive antenna and R_{ANT_diff} is the transformed differential antenna resistance as given by (3.4). Therefore, if the bias current I_{VCO} is increased, the efficiency is predicted to increase provided that R_{ANT_diff} is smaller than the parallel combination of transistor output resistances $2R_{DSn}$ and $2R_{DSp}$. In the case where these output resistances are significantly larger than R_{ANT_diff}, the current $I_{ANT} \approx I_{TANK}$, and

therefore the differential output voltage is related to the bias current by (4.10). This substitution in (4.13) is given by

$$\eta_{P-VCO} = \frac{(4/\pi I_{VCO})^2 \cdot R_{ANT\_diff}/2}{I_{VCO} \cdot V_{DD}} = \frac{(8/\pi^2) I_{VCO} \cdot R_{ANT\_diff}}{V_{DD}} \text{ (current-limited)} \quad (4.14)$$

which clearly shows that increasing the bias current or inductor's quality factor (for a given inductance) will improve oscillator power efficiency. When the bias current is exclusively increased causing the output voltage to increase until the drain current of M_T is saturated to I_{MAX} and the VCO is operating in the voltage-limited regime, the efficiency is then given by

$$\eta_{P-VCO} = \frac{P_{ANT}}{P_{VCO}} = \frac{V_{MAX}{}^2/(2R_{ANT\_diff})}{I_{MAX} \cdot V_{DD}} \text{ (voltage-limited).} \quad (4.15)$$

Any further increases in the bias current will have no impact on the VCO's power consumption or the antenna's power dissipation, thus the efficiency is expected to reach a maximum value in this regime of operation. Whether or not oscillator power efficiency nears the design target of $\approx$ 50% appears to be related to the differential antenna resistance R_{ANT_diff} for a particular LC VCO design. In contrast to (4.14), increasing the inductor's quality factor (for a given inductance) in the voltage-limited regime is predicted to reduce oscillator efficiency through a decrease in P_{ANT}. However, since the equivalent tank resistance, encompassing R_{ANT_diff}, is to some extent related to the output voltage V_{MAX} as suggested by (4.11), then I_{MAX} is expected to decrease as well to maintain V_{MAX} constant (i.e. voltage-limited). The decrease in I_{MAX} will result in a decrease in P_{VCO} and thus is predicted to improve oscillator efficiency. It is therefore not entirely clear what the net effect will be on oscillator power efficiency as the differential antenna resistance is increased for a given oscillator transmitter design. The oscillator efficiency in the voltage-limited regime is to be studied further in the following subsection.

In [58], the efficiency of an oscillator is explored in terms of the energy stored in the resonator's tank E_{TANK} to the total DC energy consumed in one period T_{OSC}. This is known as the energy transfer efficiency $\eta_{E\text{-}VCO}$, and it can be expressed as

$$\eta_{E-VCO} = \frac{Energy\ stored}{Power\ consumed \cdot T_{OSC}} = \frac{E_{TANK}}{P_{VCO} \cdot T_{OSC}} = \frac{C_{TANK} \cdot V_{TANK}^{\ 2} / 2}{I_{VCO} \cdot V_{DD} \cdot T_{OSC}} \tag{4.16}$$

where the tank energy is given by $E_{TANK} = C_{TANK} \cdot V_{TANK}^2/2$. Assuming that the power dissipated by the varactors is negligible and the oscillator's transistor output resistances are significantly larger than R_{ANT_diff} (and thus $R_{TANK} \approx R_{ANT\_diff}$), the quality factor of the tank Q_{TANK} is given by

$$Q_{TANK} = \omega_{OSC} \frac{Energy\ stored}{Power\ dissipated\ in\ antenna} = \frac{T_{OSC}}{2\pi} \frac{R_{ANT\_diff}}{L_{TANK}} \tag{4.17}$$

which is a ratio of the energy stored in the resonator to the energy dissipated per radian. Energy transfer efficiency can be re-written in terms of the differential antenna resistance with the substitution of (4.10) for the output voltage amplitude in the current-limited regime. Then, $\eta_{E\text{-}VCO}$ is given by

$$\eta_{E-VCO} = \frac{4 I_{VCO} \cdot R_{ANT\_diff}^{\ 2} \cdot \sqrt{C_{TANK} / L_{TANK}}}{\pi^3 \cdot V_{DD}} \text{ (current-limited)}, \tag{4.18}$$

noting that (4.18) no longer remains valid when the current source transistor M_T enters the triode region of operation – whereupon the VCO transitions into the voltage-limited regime. It is evident that the oscillator's energy transfer efficiency can be related to power efficiency with (4.17) by

$$\eta_{P-VCO} \cdot \frac{Q_{TANK}}{2\pi} = \eta_{E-VCO} \tag{4.19}$$

since

$$\frac{Power\ dissipated\ in\ antenna}{Power\ consumed} \cdot \frac{Energy\ stored}{T_{OSC} \cdot Power\ dissipated\ in\ antenna} = \frac{Energy\ stored}{Power\ consumed \cdot T_{OSC}}. \tag{4.20}$$

Increasing the quality factor of the tank will improve energy transfer efficiency and is known to enhance the phase noise performance of the oscillator [58]. In [59], the phase noise due to thermal effects for a complementary *LC* oscillator is minimized through a maximizing of $\eta_{E\text{-}VCO}$.

4.2.4. Simultaneous *gm* and Impedance Matching w/ Power Optimization

The design of the complementary *LC* VCO follows the procedure of simultaneous transconductance and impedance matching of the NMOS and PMOS latches as described in [55] for optimum phase noise performance. This procedure will be briefly summarized for the reader's convenience and then slightly amended for optimum oscillator power efficiency performance. The complementary *LC* VCO topology best suited for optimum efficiency is the variant which does not include a current source bias, as shown in Figure 4-6. This design is intended for operation in the voltage-limited regime, with a rail-to-rail output swing, where oscillator power efficiency is expected to peak.

gm matching

Setting the DC operating voltage of the resonator to $V_{DD}/2$ (for V_{SS} = 0 V), the transconductance of the NMOS and PMOS transistors in the saturation region are matched such that

$$\frac{gm_n}{gm_p} = \frac{\mu_n \cdot C_{OX} \cdot W_n / L_n(|V_{GS,n} - V_{TH,n}|)}{\mu_p \cdot C_{OX} \cdot W_p / L_p(|V_{GS,p} - V_{TH,p}|)} == 1, \tag{4.21}$$

and therefore $gm_n = gm_p = gm$, where the subscript "*n*" denotes reference to an NMOS device and, similarly, a subscript "*p*" denotes reference to an PMOS device, μ is the mobility of the charge carrier, C_{OX} is the oxide capacitance, W is the gate width, L is the gate length, V_{GS} is the gate-source voltage (here, $V_{GS} = V_{DD}/2$) and V_{TH} is the threshold voltage of the device. In satisfying (4.21) for the relative transconductance of these transistors, the output swing is maximized. The absolute transconductance of these transistors must also satisfy (4.5) to guarantee oscillation start-up.

Impedance matching

To achieve a symmetrical waveform of the output signal as it swings up and down about $V_{DD}/2$, the impedance seen by the resonant tank should be the same, i.e. $C_{nmos} = C_{pmos}$. To a first order, this requires matching $C_{gs,n} = C_{gs,p}$ which is given by

$$\frac{C_{gs,n}}{C_{gs,p}} = \frac{(2/3)W_n \cdot L_n \cdot C_{OX}}{(2/3)W_p \cdot L_p \cdot C_{OX}} = \frac{W_n \cdot L_n}{W_p \cdot L_p} == 1. \tag{4.22}$$

The conditions for *gm* and impedance matching cannot be simultaneously satisfied unless a non-minimum gate length is used for either the NMOS or PMOS transistors. As a non-minimum gate length degrades the speed of the transistor and the carrier mobility of a PMOS device is lower than that of an NMOS device, the rational choice is to set the PMOS transistors of the VCO such that

$$L_p = L_{min}, \tag{4.23}$$

where L_{min} is the minimum gate length. The sizes of the NMOS and PMOS transistors for simultaneously *gm* and impedance matching [55] can therefore be determined with (4.21) and (4.22) as

$$W_p = \frac{gm}{\mu_p \cdot C_{OX}(|V_{DD}/2 - V_{TH,p}|)} \cdot L_{min}, \tag{4.24}$$

$$L_n = \sqrt{\frac{\mu_n \cdot C_{OX}(|V_{DD}/2 - V_{TH,n}|)}{\mu_p \cdot C_{OX}(|V_{DD}/2 - V_{TH,p}|)}} \cdot L_{min}, \text{ and} \tag{4.25}$$

$$W_n = \frac{gm}{\mu_n \cdot C_{OX}(|V_{DD}/2 - V_{TH,n}|)} \cdot L_n. \tag{4.26}$$

Power optimization

The NMOS latch which commutates the supply current through the *LC* tank of the VCO can be modelled as a pair of resistive switches, each exhibiting an infinite off-resistance and a finite on-resistance $R_{on}(t)$ between the drain and source terminals of the transistor. The NMOS on-resistances, denoted by $R_{on\_n}(t)$ in Figure 4-6 b), vary in resis-

tance over the course of an oscillation period. Similarly, the PMOS latch can be modelled by a pair of resistive switches and is denoted by $R_{on\_p}(t)$ in Figure 4-6 b). The on-resistances $R_{on\_n}(t)$ and $R_{on\_p}(t)$ are each labelled with an arrow whose direction indicates the relative change in resistance over the oscillation period, e.g. the resistance of M_1 will be 180° out of phase with that of M_2. The difficulty in modelling the VCO's metal-oxide-semiconductor (MOS) devices as switches is that $R_{on}(t)$ is time-varying and a non-linear function of the voltage across the terminals of the transistor. However, since $R_{on}(t)$ is inversely proportional to the W/L ratio of a device, this modelling is expected to provide insight for optimizing the oscillator's power efficiency performance.

The total power consumed by the VCO is the sum of the time-average powers dissipated in the resistances of Figure 4-6 b). The time-average power of a MOS device is given by

$$P_{mos} = \frac{1}{T_{OSC}} \int_{t_1}^{t_1+T_{OSC}} P_{mos}(t)\,dt \tag{4.27}$$

where $P_{mos}(t)$ is a periodic function of the instantaneous power dissipated by the device over one oscillation period T_{OSC}. For a MOS device, $P_{mos}(t)$ is a function of the device's drain-source voltage $V_{DS}(t)$ and drain-source current $I_{DS}(t)$, and since $I_{DS}(t)$ is related to $R_{on}(t)$ by Ohm's Law, (4.27) can be expressed as

$$P_{mos} = \frac{1}{T_{OSC}} \int_{t_1}^{t_1+T_{OSC}} V_{DS}(t)\cdot I_{DS}(t)\,dt = \frac{1}{T_{OSC}} \int_{t_1}^{t_1+T_{OSC}} V_{DS}^{\,2}(t)/R_{on}(t)\,dt\,. \tag{4.28}$$

Assuming a rail-to-rail output swing, as the VCO is intended for operation in the voltage-limited regime, the drain-source voltage seen by the NMOS transistor M_3 is given by

$$V_{DS}(t) = \frac{V_{DD}}{2} + \frac{V_{DD}}{2}\cos(2\pi f_{OSC}\cdot t) \tag{4.29}$$

for a negative supply V_{SS} equal to 0 V. The corresponding gate-source voltage seen by M_3 is given by

$$V_{GS}(t) = V_{DD} - V_{DS}(t) = \frac{V_{DD}}{2} - \frac{V_{DD}}{2}\cos(2\pi f_{OSC} \cdot t). \quad (4.30)$$

Thus, according to (4.28), the power dissipation of M_3 can only be influenced by its on-resistance and would therefore scale with the *W/L* ratio of this device. To maintain simultaneous *gm* and impedance matching, all the VCO's transistors must scale in size by the same proportion. For matching the power dissipated of the active devices, denoted by P_{VCO_active}, with that dissipated in the passive device – ideally this should be comprised mainly of the oscillator's inductor as it serves as an antenna, the transistors should be scaled such that

$$2P_{mos\_n} + 2P_{mos\_p} = P_{VCO\_active} \approx 4P_{mos} = P_{ANT}. \quad (4.31)$$

This would result in a $\eta_{P\text{-}VCO} \approx 50\%$ according to (4.12) if the power dissipated by the varactors could be neglected. Since the maximum power delivered to the antenna in the voltage-limited regime is given approximately by

$$P_{ANT\_max} \approx V_{DD}^{\ 2}/(2R_{ANT\_diff}), \quad (4.32)$$

the time-average power dissipation of a VCO's MOS device should be one quarter of this value.

The proposed simultaneous *gm* and impedance matching with power optimization technique can bring about a low-power or high-power complementary *LC* VCO design and accordingly satisfy a low-radiated power or high-radiated power transmitter specification, respectively. This assumes that for either case, a suitable antenna can be designed with a differential resistance derived from (4.32) and that the antenna's radiation efficiency remains the same. For a given supply voltage, the current consumption of the VCO can be indirectly controlled by scaling the *W/L* ratio of the devices. In the low-power VCO design, the downward scaling of the devices' *W/L* ratio would be limited by a failure to satisfy the oscillator start-up condition of (4.5). In the high-power VCO design, the upward scaling of the devices' *W/L* would decrease the switching speed of the devices which eventually would limit the VCO's oscillation frequency.

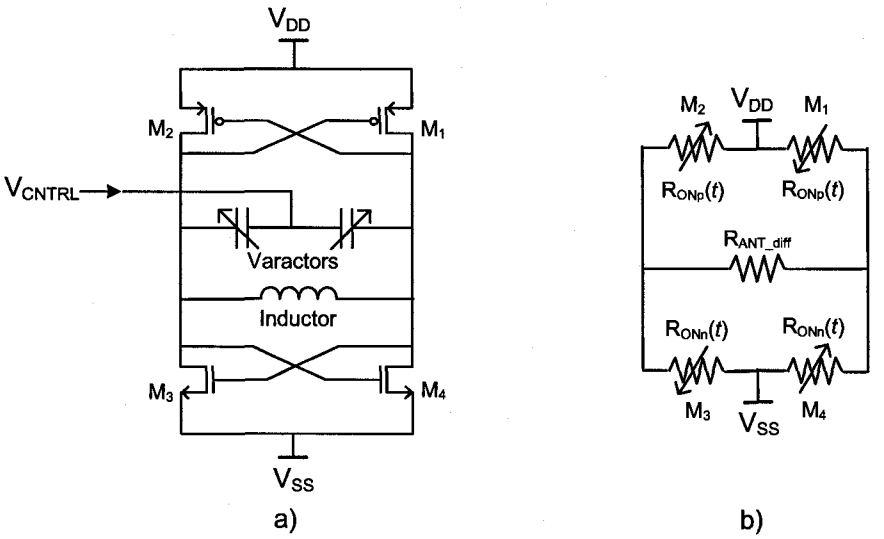

Figure 4-6: *LC* VCO; a) complementary cross-coupled schematic and b) MOS switch model representation.

4.2.5. Design and Simulation

The design of the complementary *LC* VCO for the TX, shown in Figure 4-7, begins by selecting a minimum sized gate length for the PMOS transistors to satisfy $L_p = L_{min}$. For this CMOS technology, L_{min} = 120 nm. The quality factor of the integrated inductive antenna is assumed to be poorer than that of the varactors and to dominate the resistive losses seen by the *LC* tank resonator. Thus, from (4.4), $R_{TANK} \approx R_{ANT\_diff}$ = 798 Ω. To satisfy the oscillation start-up condition of (4.5), the equivalent negative conductance of the NMOS and PMOS latches (Gm_{eff}) requires $|Zm_{eff}|$ to be 266 Ω (or smaller). As the equivalent negative conductance magnitude of the latches is the same as the device transconductances when *gm* matching for this VCO topology, $|Gm_{eff}| = gm_n = gm_p = gm$ = 3.7 mS. With this, W_p is derived for the PMOS transistors according to (4.24), and similarly, W_n and L_n are derived for the NMOS transistors according to (4.26) and (4.25), respectively. These transistor sizes are then optimized for simultaneous *gm* and impedance matching, which resulted in an L_n of 240 nm. The widths of the devices are then scaled to achieve the desired oscillator power efficiency performance ($\eta_{P\text{-}VCO}$).

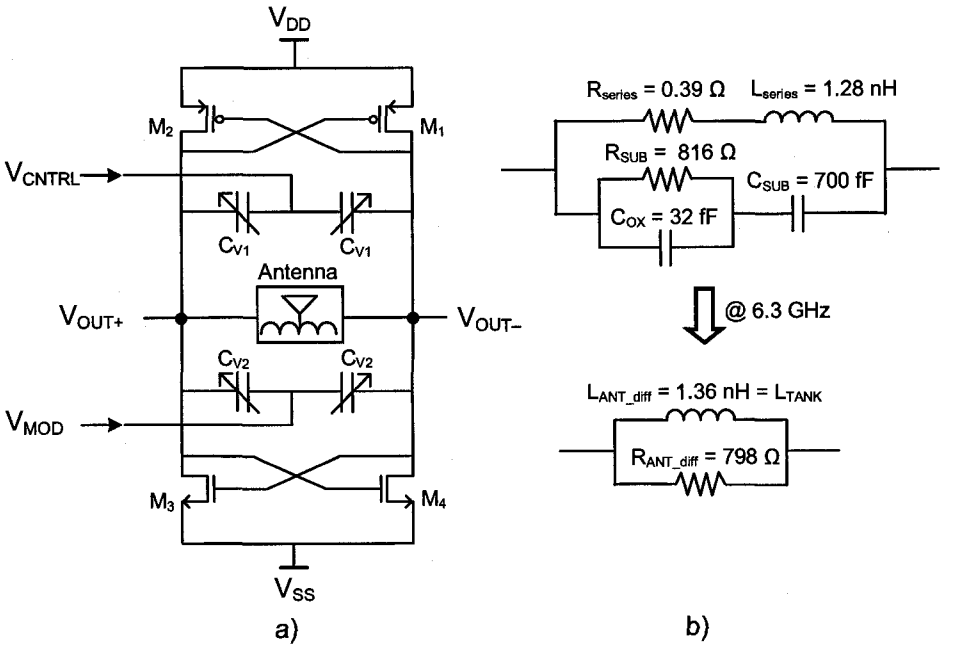

Figure 4-7: TX *LC* VCO; a) schematic and b) equivalent circuit of the antenna at 6.3 GHz.

The scaling of the VCO's transistors for power optimization is examined. In Figure 4-8, the simulated results of the instantaneous power for the NMOS transistor M_3 ($P_{nmos}(t)$) is observed for three VCO designs – VCO1, VCO2 and VCO3. The device widths of VCO1 are 1.5 times smaller than those of VCO2. Conversely, the device widths of VCO3 are 1.5 times greater than those of VCO2. From Figure 4-8, it is evident that the expression for the instantaneous power dissipated by a device (4.28), based on (4.29) and (4.30), would be consistent with the simulated results across an oscillation cycle if the expression predicted a negative power region. Negative power is attributed to a reversal in current flow due to M_3 sourcing rather than sinking current between the drain and source terminals. This would require the on-resistance ($R_{on}(t)$) in (4.28) of M_3 to be negative for part of the oscillation cycle. Nevertheless, evaluating the time-average power dissipated by M_3 (P_{nmos}) for each VCO design in Table 4 shows that P_{nmos} is closely correlated to the scaling of the VCO's transistors. Therefore, (4.28) serves as a helpful design guide in optimizing the power to the antenna.

Table 4: A comparison of P_{nmos} for different VCO designs.

VCO design	W_n normalized to VCO2	W_p normalized to VCO2	P_{nmos}	P_{nmos} normalized to VCO2
VCO1	$(1.5)^{-1}$	$(1.5)^{-1}$	230 μW	$(1.43)^{-1}$
VCO2	1.0	1.0	330 μW	1.0
VCO3	1.5	1.5	480 μW	1.45

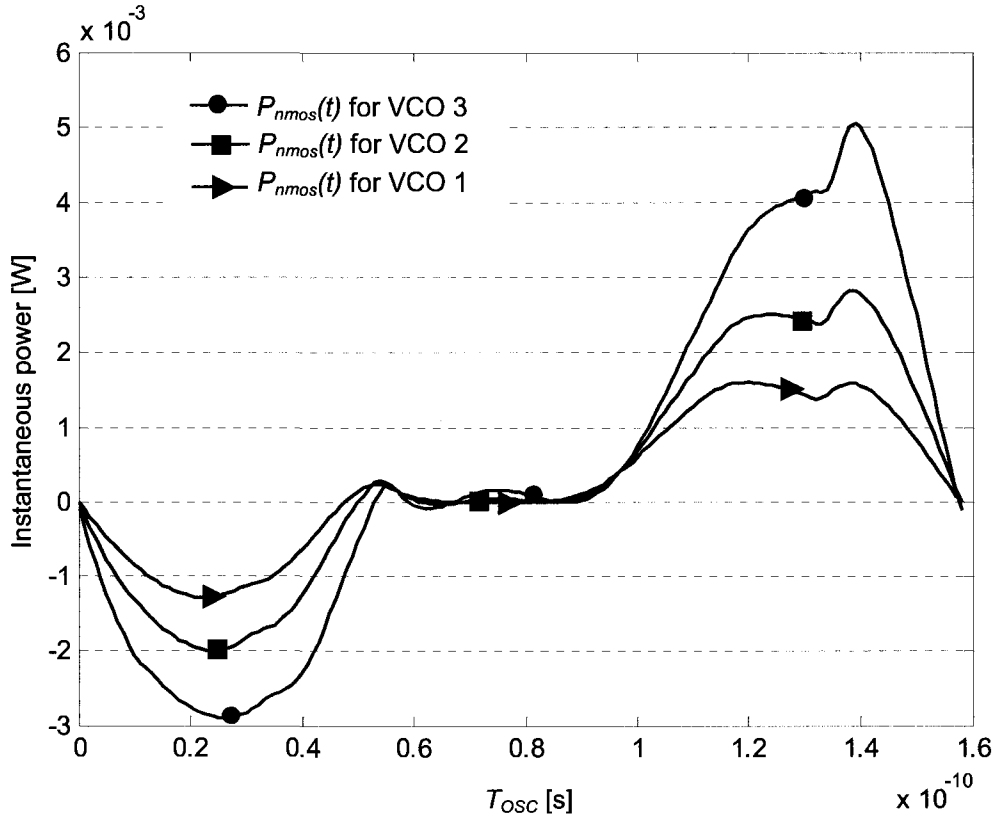

Figure 4-8: Simulation; $P_{nmos}(t)$ with respect to T_{OSC}.

As the widths of the VCO's devices are scaled, the DC transconductance of the devices increase by the same proportion, and plots of $\eta_{P\text{-}VCO}$, where the power delivered to the antenna (P_{ANT}) and the power dissipated in the VCO's four active devices (P_{VCO_active}) with respect to gm are shown in Figure 4-9. The oscillator power efficiency is therefore expressed in terms of

$$\eta_{P-VCO} = \frac{P_{ANT}}{P_{VCO}} = \frac{P_{ANT}}{P_{ANT} + P_{VCO\_active}}. \tag{4.33}$$

In Figure 4-9, P_{VCO_active} is seen to linearly increase with gm, where as P_{ANT} increases with diminishing returns – eventually limited to P_{ANT_max} from (4.32). Oscillator power efficiency is seen to decrease, from a high of 46%, as gm is increased. It appears that for maximizing power efficiency, the optimum device transconductance should be 3 mS. However, at this transconductance, the differential output voltage amplitude V_{TANK} has not reached the saturated voltage of V_{DD} and consequently the link budget specification for a P_{TX} of 0 dBm (where P_{TX} =P_{ANT}) is not achieved. Therefore, the NMOS and PMOS device widths are scaled to W_n of 27 μm and W_p of 48 μm, respectively, resulting in a gm of 9 mS which satisfied this antenna power delivery requirement while maintaining a relatively high oscillator power efficiency of 40%.

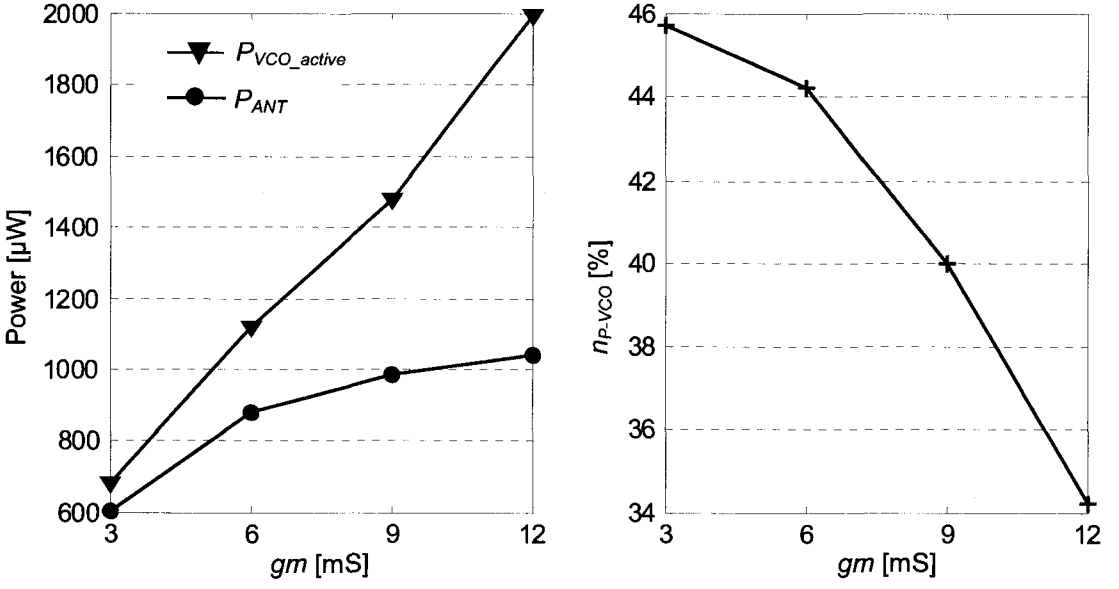

Figure 4-9: Simulation; P_{ANT}, P_{VCO_active} and η_{P-VCO} with respect to gm.

To assess the validity of the push-pull behaviour supposition discussed earlier for the complementary LC VCO, the time domain waveforms of drain current $I_{DS}(t)$ and drain-source voltage $V_{DS}(t)$ of transistor M_3 are examined in Figure 4-10. Here, the tran-

sistor is generally conducting current for half the oscillation cycle, a characteristic of Class B operation. However, it is apparent that $I_{DS}(t)$ contains other harmonics which are possibly causing the transistor to conduct current at other times as well. In addition, $I_{DS}(t)$ is phase-shifted in comparison to a typical Class B current waveform, which is also shown in Figure 4-10, whose peak current and minimum output voltage are aligned in time. These differences from ideal push-pull behaviour would reduce the oscillator's power efficiency to Class AB or lower.

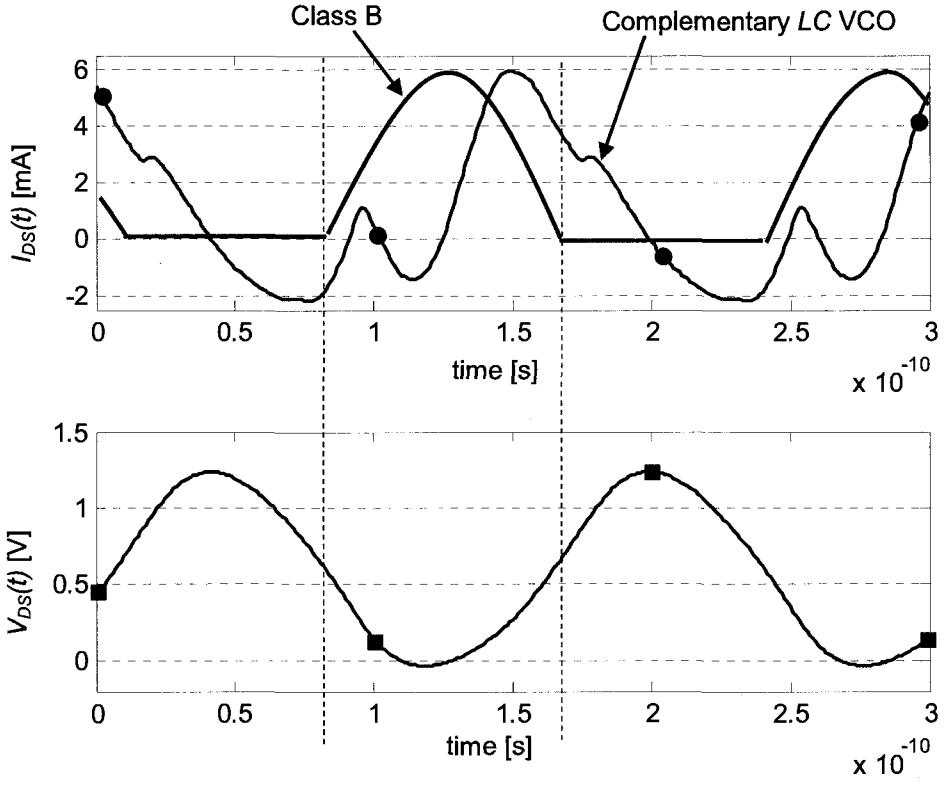

Figure 4-10: Simulation; $I_{DS}(t)$ and $V_{DS}(t)$ of M_3.

Another reason for choosing a transconductance value that is more than double the necessary value, which is required to guarantee oscillation start-up under all operating temperatures and worst-case process variations, is to compensate for inaccuracies in HFSS's modelling of the integrated antenna. Typically, when developing the design kits of a semiconductor process, the new device is modelled using a computer-aided design

tool, implemented and then characterized with measurements. The measurements are used to improve the device model such that it can be confidently used for circuit design and simulation. In the design flow of this TX, the new device – an inductive antenna is to be used in the oscillator directly from the initial results of the modelling phase. Thus, this oscillator is designed to start-up even if HFSS overestimated the antenna's Q by a factor of two. Consider the following analysis where the antenna's Q is varied by altering the real part of this structure's impedance. In Figure 4-11, the antenna's differential resistance (R_{ANT_diff}) and series resistance (R_{ANT}) are plotted with respect to Q, as well as the equivalent negative conductance magnitude of the NMOS and PMOS latches $|Gm_{eff}|$ which is required to satisfy the oscillation start-up condition of (4.5). Recalling from Subsection 3.2.1, HFSS predicted an antenna quality factor (Q_{ANT}) of 14.65 at 6.3 GHz. Therefore, if the implemented Q_{ANT} is actually around 6 at this frequency, the proposed VCO design would have a sufficient device transconductance value to guarantee oscillation start-up.

The VCO's power consumption and efficiency performance are also studied as the antenna's Q is varied. In Figure 4-12, the simulated results of P_{VCO}, P_{VCO_active} and P_{ANT} are plotted with respect to Q, as well as the corresponding $\eta_{P\text{-}VCO}$. Oscillator power efficiency peaks at the onset of the voltage limited regime to 48% when the antenna's Q is around 6. After a Q of 12, the power consumption of the VCO's active devices remains constant. This is indicating that the VCO is operating deep in the voltage-limited regime, where the differential output voltage is saturated to V_{DD}, and that the power dissipated in the MOS devices is limited as suggested by (4.28) for terminal voltages given by (4.29) and (4.30). In contrast, the power delivered to the antenna decreases linearly as power is inversely related to resistance.

The above study suggests that power efficiency in a complementary *LC* VCO peaks when the magnitude of the equivalent negative conductance, which is equal to the (DC) transconductance of the VCO's devices in a *gm* matched design, is given by the oscillation start-up condition of (4.5). In other words, for achieving the maximum $\eta_{P\text{-}VCO}$,

the optimum device transconductance $gm = |Gm_{eff}| = [R_{TANK}/3]^{-1}$. To corroborate this association, power efficiency is observed as the antenna's Q is varied for three different device transconductances. The change in transconductance is achieved by scaling the NMOS and PMOS device widths. The simulated results are plotted in Figure 4-13 which shows the abovementioned association to be true and therefore serve as a future design guideline for maximizing $\eta_{P\text{-}VCO}$ when reliable and tested antenna models are available.

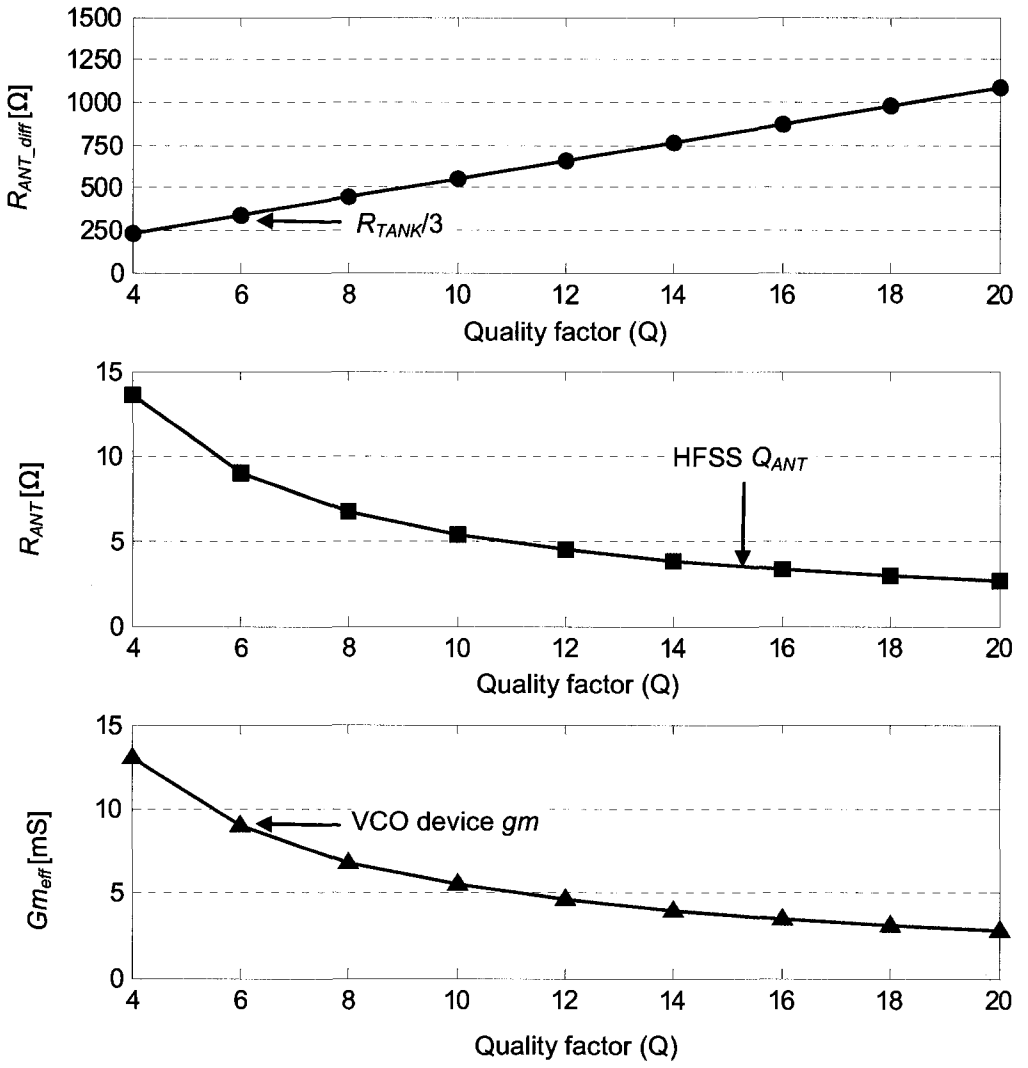

Figure 4-11: Simulation; R_{ANT_diff}, R_{ANT} and Gm_{eff} with respect to antenna Q.

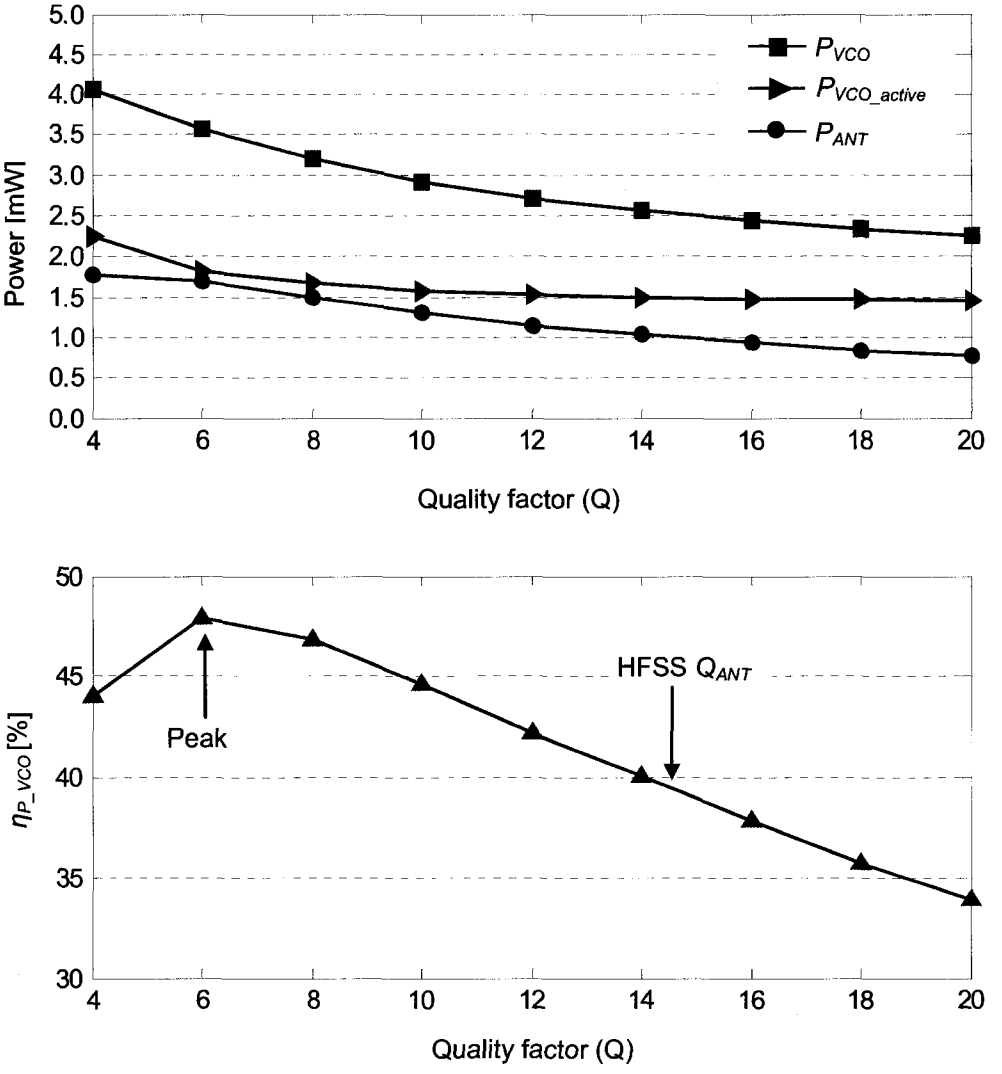

Figure 4-12: Simulation; P_{VCO}, P_{VCO_active}, P_{ANT} and $\eta_{P\text{-}VCO}$ with respect to antenna Q.

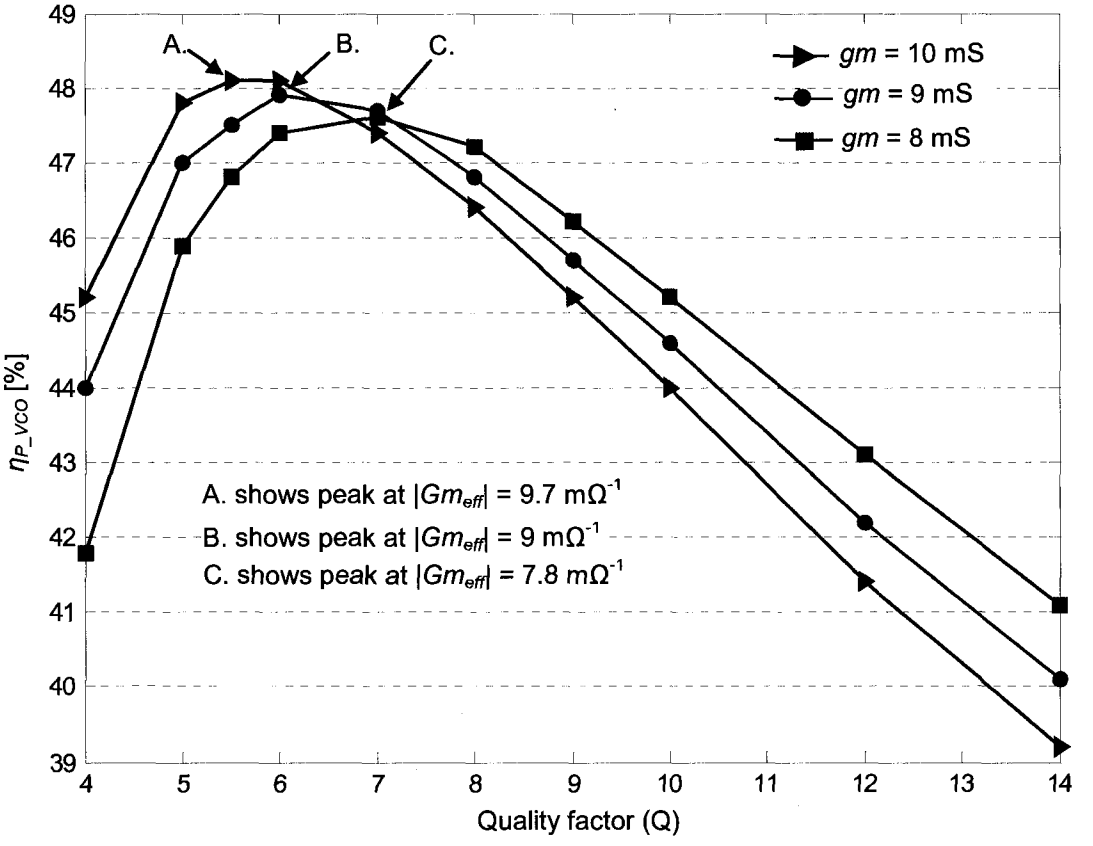

Figure 4-13: Simulation; $\eta_{P\text{-}VCO}$ with respect to antenna Q for different gm.

The input impedance of the NMOS and PMOS latches of the VCO, Z_{NMOS} and Z_{PMOS}, respectively, are determined by s-parameter simulations across the frequency band of interest, the testbench for these simulations are obtained from [55]. Figure 4-14 is a plot of the simulated imaginary parts of Z_{NMOS} and Z_{PMOS}, which are matched for a first-order approximation to achieve waveform symmetry.

The frequency of oscillation f_{OSC} of the TX LC VCO in Figure 4-7 is given by

$$f_{OSC(V_{CNTRL},V_{MOD})} = \frac{1}{2\pi\sqrt{L_{TANK}C_{TANK(V_{CNTRL},V_{MOD})}}} \tag{4.34}$$

where L_{TANK} is transformed parallel inductance of the antenna, C_{TANK} is primarily formed from n-type accumulation metal-oxide-semiconductor (AMOS) varactors – a set of con-

trol-loop varactors (C_{V1}) and a set of modulation varactors (C_{V2}), driven by the voltage signals V_{CNTRL} and V_{MOD}, respectively. The desired tuning range for the modulation varactors is 1 MHz. To ensure the VCO meets this specification, the modulation varactors are sized to permit a greater turning range, such as 8 MHz, with a rail-to-rail bitstream on V_{MOD}. Thus, a form of amplitude control on the modulation input will be required to properly interface with the RX. The control-loop varactors form the remainder of the capacitance needed for *LC* tank resonance at 6.3 GHz, as oppose to fixed capacitors. This provides the PLL with a large turning range to compensate for any inaccuracies in HFSS's modeling of the integrated antenna's inductive and capacitive properties. The simulated oscillation frequency as a function of V_{CNTRL} for V_{MOD} = 0.6 V is plotted in Figure 4-15. The expected control-loop varactor gain K_{VCO} is approximately 340 MHz/V, and the expected turning range is from 6.06 GHz to 6.47 GHz. The simulated oscillation frequency in terms of its offset from 6.268 GHz is plotted in Figure 4-16 as a function of V_{MOD} for V_{CNTRL} = 0.6 V. Here, the expected modulation varactor gain K_{MOD} is approximately 7 MHz/V, which is observed between a V_{MOD} of 0 to 1.2 V.

The simulated results of the VCO's phase noise at offsets from the 6.3 GHz centre frequency are plotted in Figure 4-17. The predicted phase noise at a 1 MHz offset is –114 dBc/Hz. Although the in-band phase noise is expected to be reduced when the VCO is locked in a PLL, during modulation the PLL is opened, and therefore the phase noise of the carrier is that of the free running VCO.

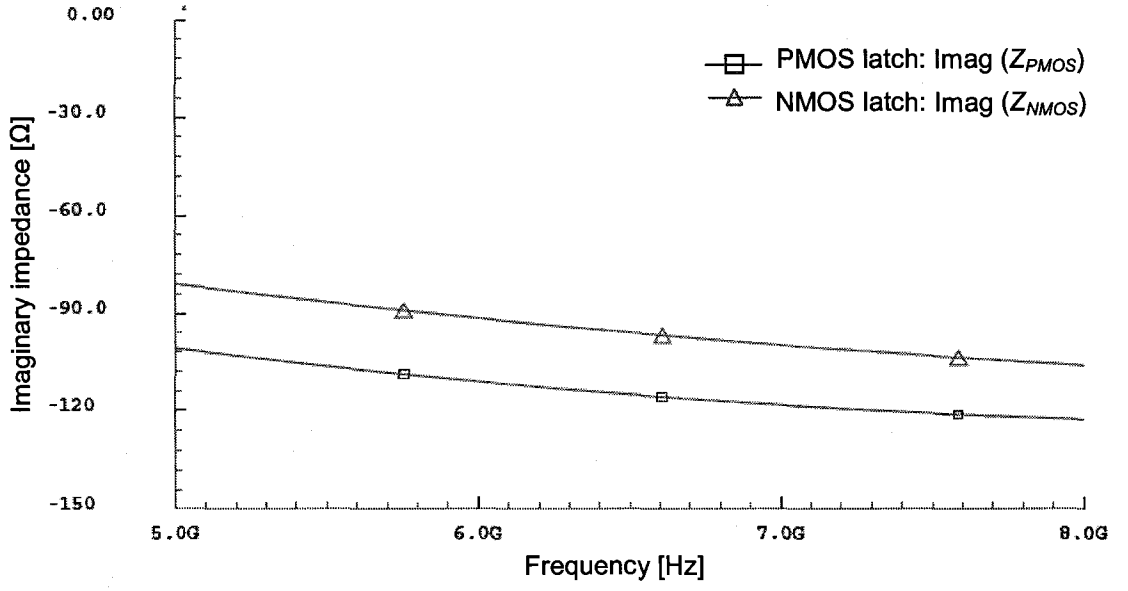

Figure 4-14: Simulation; imaginary part of the latch impedance over frequency.

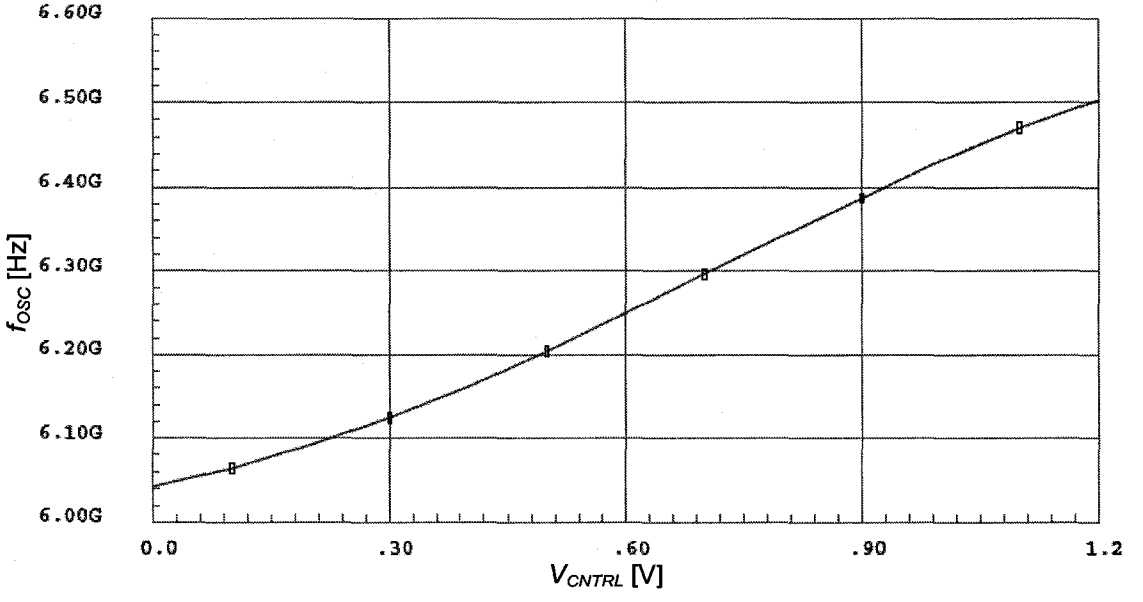

Figure 4-15: Simulation; f_{OSC} as a function of V_{CNTRL}.

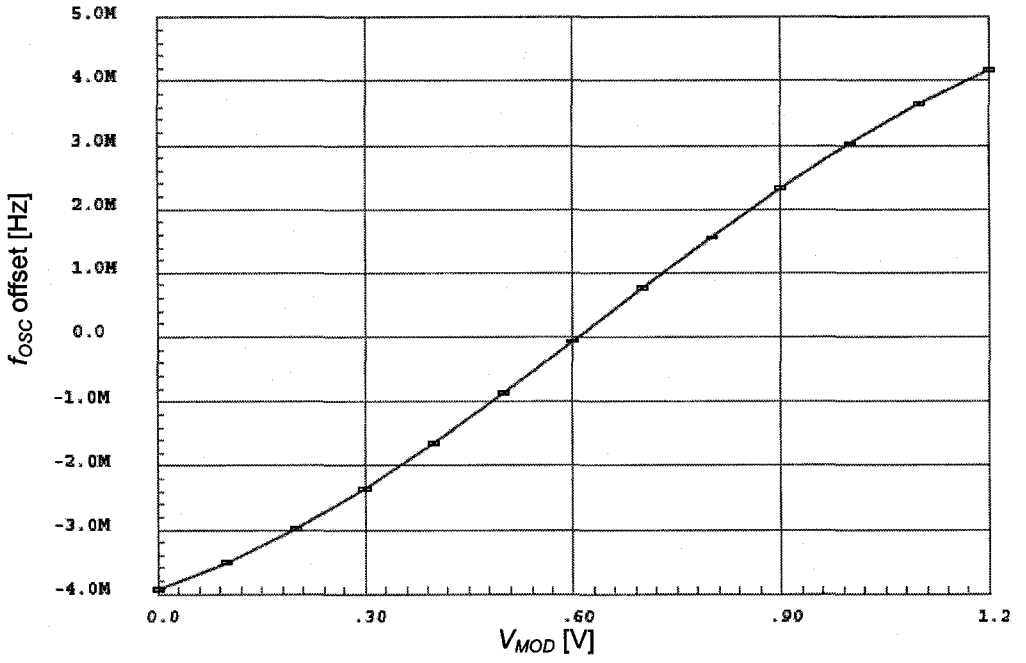

Figure 4-16: Simulation; f_{OSC} offset from 6.268 GHz as a function of V_{MOD}.

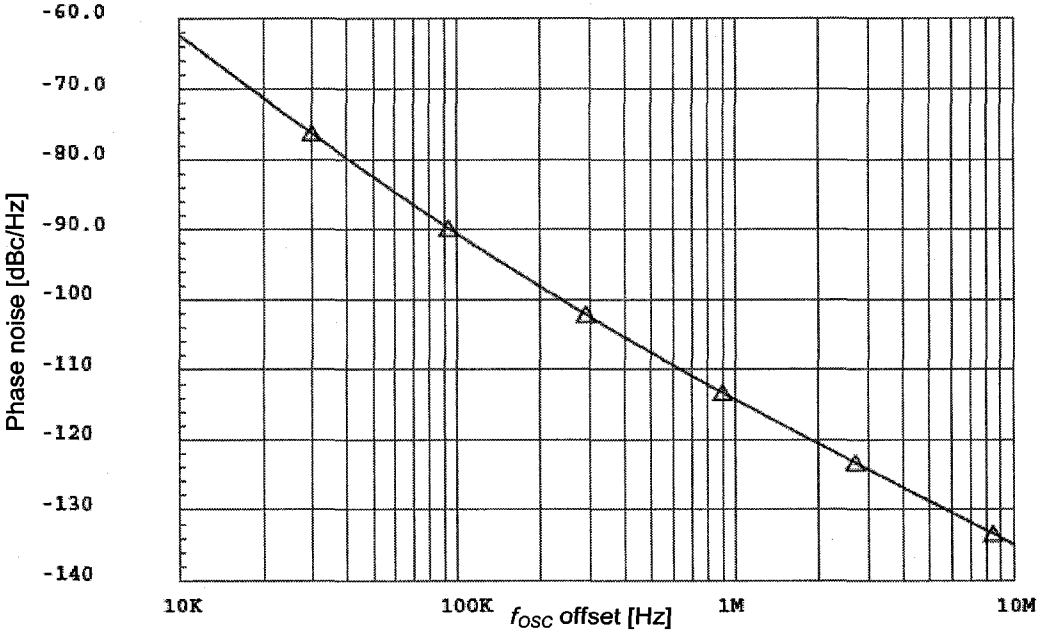

Figure 4-17: Simulation; phase noise as a function of f_{OSC} offset.

4.3. Divider

In a gigahertz frequency synthesizer, the dominant power consumer is often multi-modulus dividers specifically the first few stages where the divider's digital logic must operate near the carrier frequency, and thus requires much more power than later stages [60, 61]. For reducing power consumption, fixed divide-by-two prescalers can be used at the first few stages of the divider, and then multimodulus dividers, for channel selection, at the later stages operating at lower frequencies [30]. Lowest possible power is achieved through fixed dividers resulting in some lost flexibility as discussed in Subsection 4.1.1, and that is the approach taken here. The TX's integer divider is formed by cascading 6 fixed divide-by-two prescalers, realizing the required divide ratio of 64. As shown in Figure 4-18, the first 3 prescalers of the divider are implemented using dynamic true-single-phase-clocking (TSPC) logic [62], while the latter 3 are implemented using static CMOS logic. TSPC logic is preferred over source-coupled logic (SCL), also known as common-mode logic (CML), in multi-gigahertz type dividers because TSPC requires only a single clock phase, less implementation area, and consumes much less power relative to SCL [63]. The drawback with TSPC is that it requires a large input voltage and thus generates more switching noise as compared to SCL. To insure the level of the input is sufficient, CMOS-based inverter buffers are placed between the TSPC prescalers. During open-loop modulation, the feedback of the PLL's loop is stopped, thus allowing the divider to be temporarily turned off to conserve energy. As the prescalers dissipate minimal static power, the divider can be powered down by latching the input signal low (or high). This is accomplished with a NAND gate controlled by the $Loop_{EN}$ signal which is also used to open/close the loop. The NAND gate is placed after the first prescaler to minimize frequency pulling at the VCO when the $Loop_{EN}$ signal is switched to a logic "low". This placement requires the gate to operate at 3.15 GHz, which is achievable with static CMOS logic in this 0.13 μm technology.

The TSPC prescaler is a divide-by-two delay-type flip-flop, as shown in Figure 4-19, and consists of only nine transistors. When the input signal (F_{IN}) makes a low-to-

high transition, the output (F_{OUT}) will latch to its complement. The static power dissipation of the circuit is minimal because there is no direct path from the supply voltages, V_{DD} to V_{SS}. The TSPC prescaler is designed for operation at 7 GHz, the optimized transistor sizes are listed in Table 5. The CMOS prescaler is also a divide-by-two delay-type flip-flop but is based on static CMOS logic, a gate-level schematic of this prescaler is shown in Figure 4-20.

Table 5: TSPC prescaler transistor sizes.

Transistor	W / L ratio	Transistor	W / L ratio
M_1	6.0 µm / 120 nm	M_5	6.0 µm / 120 nm
M_2	6.0 µm / 120 nm	M_6	6.0 µm / 120 nm
M_3	3.0 µm / 120 nm	M_7	9.0 µm / 120 nm
M_4	6.0 µm / 120 nm	M_8	6.0 µm / 120 nm
		M_9	6.0 µm / 120 nm

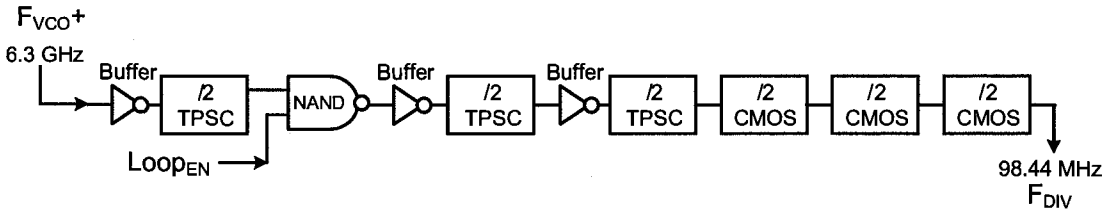

Figure 4-18: High-frequency low-power divider topology.

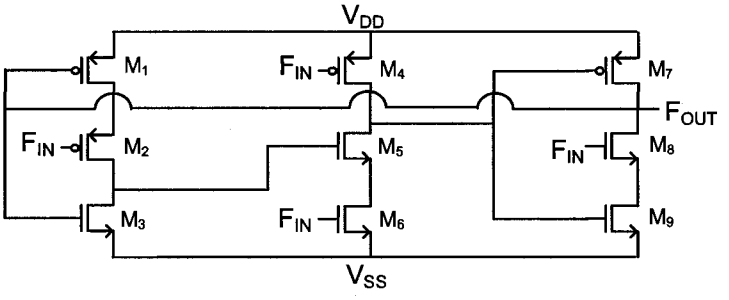

Figure 4-19: TSPC prescaler schematic.

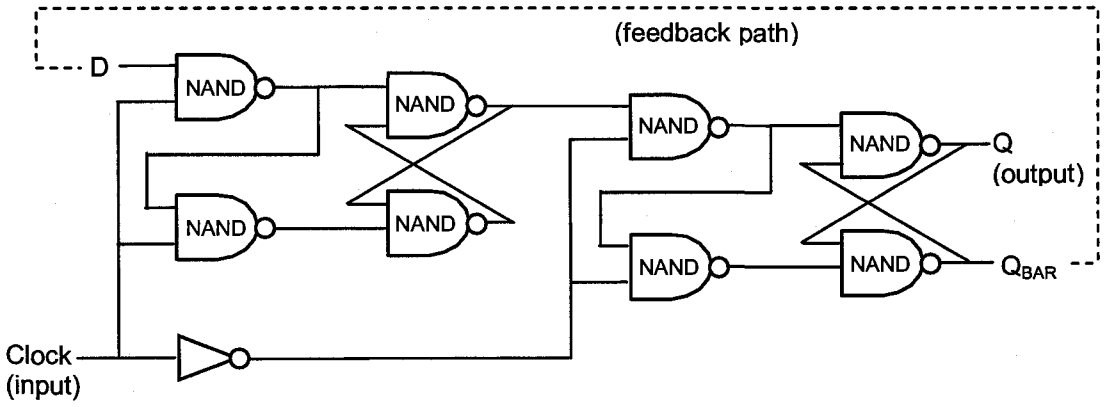

Figure 4-20: Static CMOS prescaler gate-level schematic.

4.4. Phase Frequency Detector

A standard tri-state PFD with two resetable D-type flip-flops and an AND gate is implemented in the PLL of the modulator. As depicted in Figure 4-21, the D flip-flops are designed using NOR gates. The gates are realized with static CMOS logic.

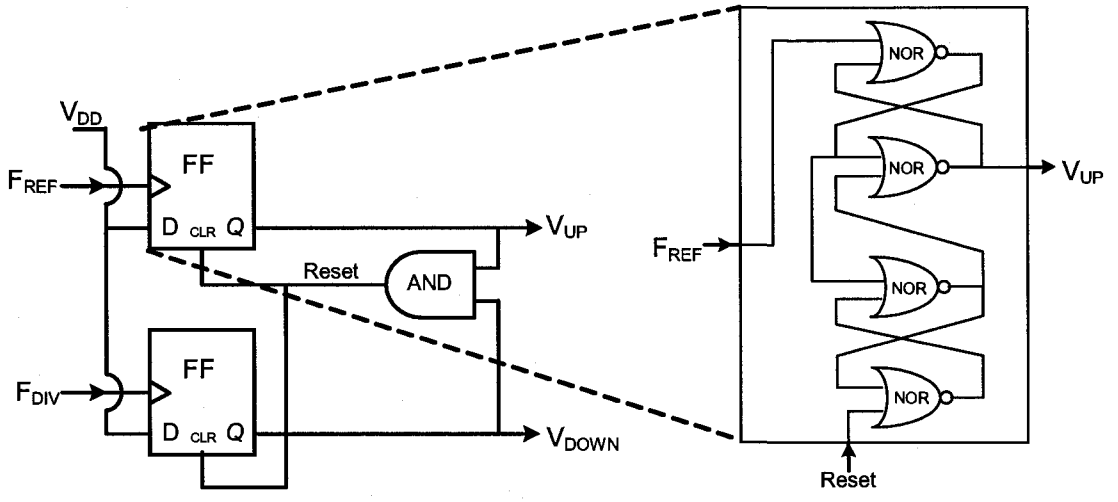

Figure 4-21: Tri-state PFD and D flip-flop schematic.

4.5. Charge Pump

The charge pump is responsible for adding and removing charge from the loop filter based on the V_{UP} and V_{DOWN} signals, respectively. These inputs are generated from the PFD when comparing the divided VCO signal's phase and frequency (F_{DIV}) with the reference signal's phase and frequency (F_{REF}), and are used to correct the tuning voltage of the loop to decrease the phase/frequency error between F_{DIV} and F_{REF}.

The CP in the PLL of the modulator, shown in Figure 4-22, is designed and implemented by Peter Popplewell. In a conventional PLL, the V_{UP} and V_{DOWN} signals control the output current signal (I_{CP_OUT}) as described above for phase/frequency locking. However, as mentioned in Section 3.6, the inclusion of the leakage (inverting) buffer requires another inversion in this PLL to re-establish negative feedback. Thus, when the leakage buffer is enabled, the V_{UP} and V_{DOWN} inputs to the CP are swapped from conventional PLL design. The technique to swap these signals is discussed later in Section 4.6. As seen in Figure 4-22, the V_{UP} and V_{DOWN} signals are each gated through a NAND gate by $Loop_{EN}$. This is to prevent these signals from turning on the output current I_{CP_OUT} through transistor-type switches M_1 and M_4 during open-loop modulation – when the charge on the loop filter must be stable. These transistors also serve as degeneration for the output current mirror, increasing the mirror's output impedance for better current matching between the sinking and sourcing directions. Also, delay cells are inserted after the NAND gate to better match the timing of the V_{UP} and V_{DOWN} signals to these transistors. The charge pump's optimized transistor sizes are listed in Table 6. In addition, a capacitor C_{CP} of 8 pF is added to the output current mirror bias to minimize switching noise on the loop filter.

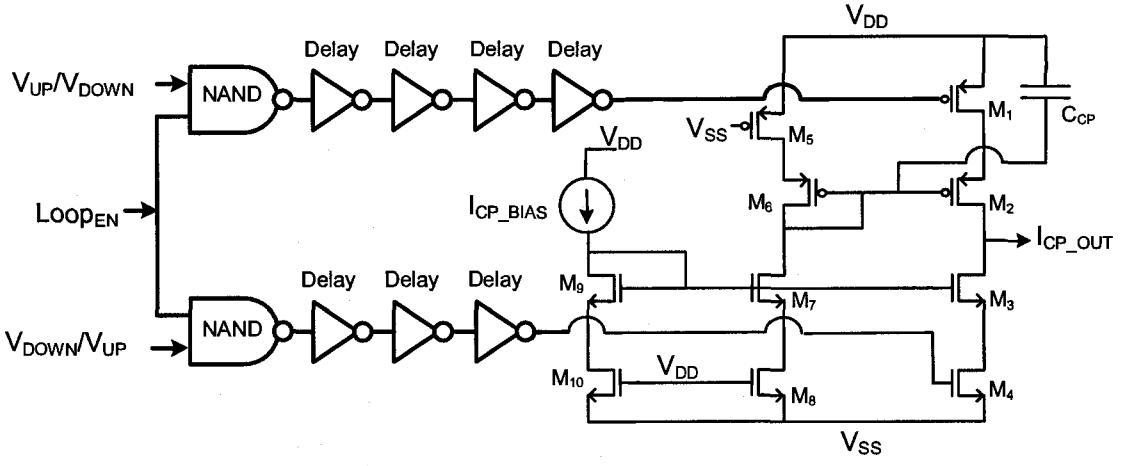

Figure 4-22: Single-ended CP schematic.

The magnitude of the output current I_{CP_OUT} is designed to be 100 µA in either direction and is mirrored in a one-to-one ratio through the bias signal I_{CP_BIAS}. The current matching between the sinking (attributed to a V_{DOWN}/V_{UP} pulse) and sourcing (attributed to a V_{UP}/V_{DOWN} pulse) directions is observed as the output voltage at the I_{CP_OUT} branch is varied, and the simulated results are plotted in Figure 4-23. The output voltage point at which there is a zero current mismatch is 0.6 V. When this voltage changes by 250 mV in either direction, the current mismatch is approximately 10%.

Table 6: Charge pump transistor sizes.

Transistor	W / L ratio	Transistor	W / L ratio
M_1	10 µm / 120 nm	M_6	30 µm / 240 nm
M_2	27 µm / 240 nm	M_7	20 µm / 480 nm
M_3	20 µm / 480 nm	M_8	10 µm / 180 nm
M_4	10 µm / 180 nm	M_9	20 µm / 480 nm
M_5	10 µm / 120 nm	M_{10}	10 µm / 180 nm

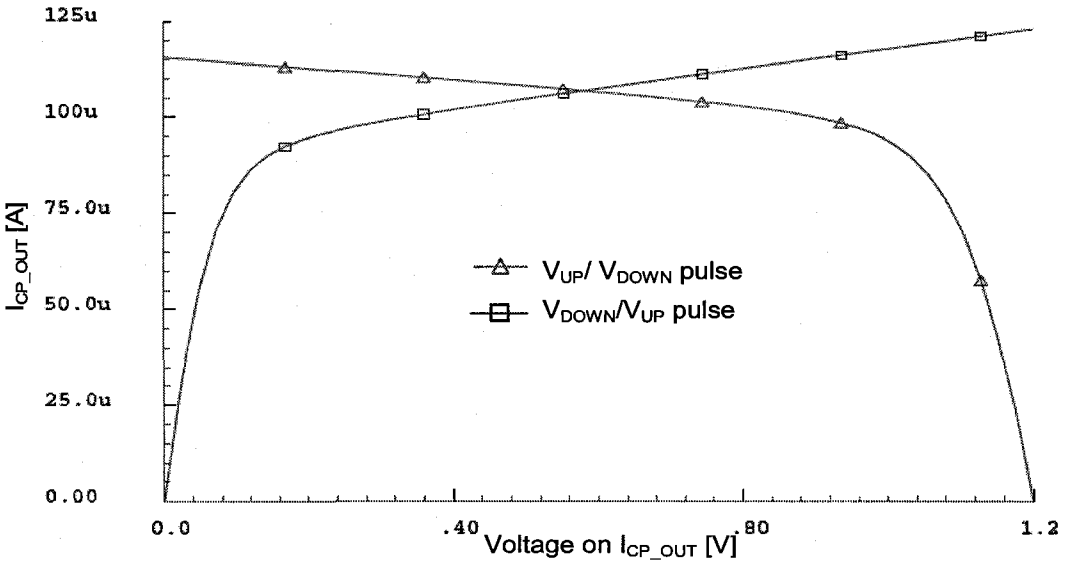

Figure 4-23: Simulation; I_{CP_OUT} as a function of output voltage.

4.6. Up-Down Mux, Loop Switch and Leakage Buffer

The forward path of the PLL is depicted at the block-level in Figure 4-24. The design differs from a conventional PLL with the inclusion of three circuit blocks, namely the up-down mux, loop switch and leakage buffer. These circuits were designed and implemented by Peter Popplewell, and their functions are briefly described in the following paragraphs.

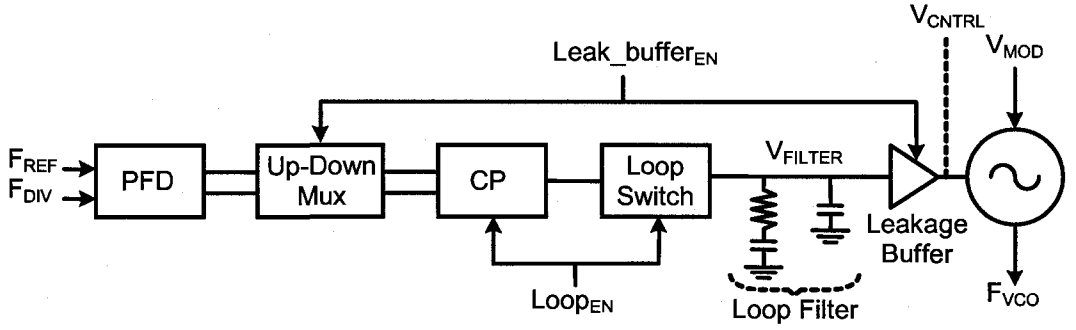

Figure 4-24: PLL forward path.

The up-down mux, shown at the transistor level in Figure 4-25, is used to swap the V_{UP} and V_{DOWN} inputs to the CP when the leakage buffer is enabled – indicated by a logic "high" on $Leak\_buffer_{EN}$. This signal is used to toggle the transmission gates to allow or impede the propagation of V_{UP} and V_{DOWN} as expected.

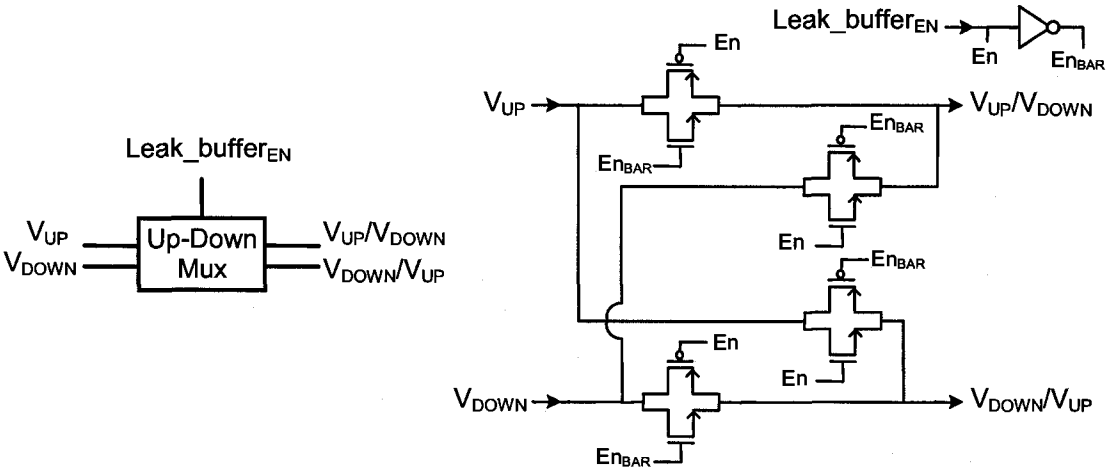

Figure 4-25: Up down mux schematic.

The loop switch circuit, shown in Figure 4-26, is used to disconnect the output of the CP, I_{CP_OUT}, from the PLL's loop filter during open-loop modulation – indicated by a logic "low" on $Loop_{EN}$. Due to high varactor gain, the VCO oscillation frequency is sensitive to the voltage (and thus charge) level on the filter. Thus, minimizing the injection of charge on the filter line during a disconnection is critical in preserving the carrier at 6.3 GHz, as carrier drift will degrade the transceiver's performance. A loop switch implemented with a transmission gate can cause charge injection when in operation. The source of this effect is the mobile charge in the MOS transistors' inversion layer. This charge is forced to leave the channel when the gate voltage changes. The transmission gate in this loop switch is realized by M_1 and M_3. A technique [64] to cancel charge injection to a first order is to insert dummy switches M_2 and M_4 at half the size of their respective counterparts, M_1 and M_3. The dummy switches are to be driven by an inverse gating signal and are to absorb the charge injected from M_1 and M_3, preventing the charge

from being added onto the loop filter. To be effective, this technique requires good matching between the fall and rise times of the gating and inverse gating toggle signals. This is achieved with addition of delay cells (and capacitors C_1) in paths of the toggle signals. From the perspective of the loop filter, when the loop switch is opened, the path to the CP will be in high impedance (high Z). The loop switch's optimized transistor sizes are listed in Table 7.

Table 7: Loop switch transistor sizes.

Transistor	W / L ratio	Transistor	W / L ratio
M_1	1.0 µm / 120 nm	M_3	3.0 µm / 120 nm
M_2	0.5 µm / 120 nm	M_4	1.5 µm / 120 nm

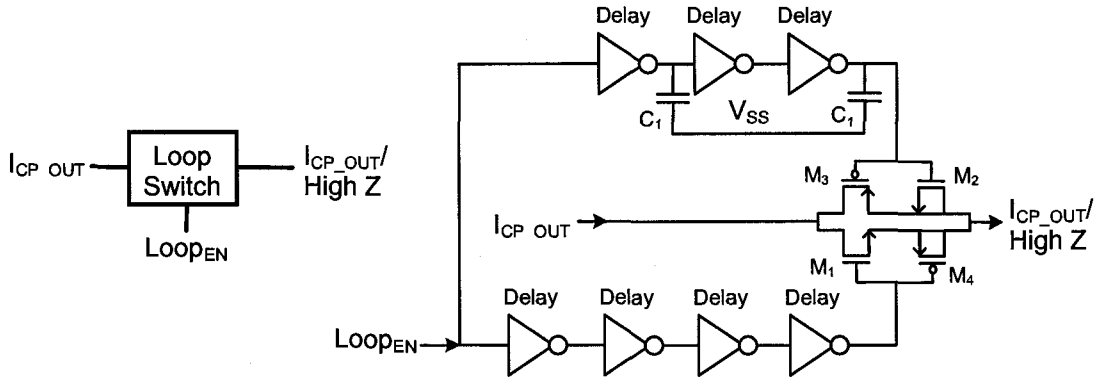

Figure 4-26: Loop switch schematic.

The leakage buffer, shown in Figure 4-27, is used to minimize charge leakage from the loop filter, and hence VCO carrier drift, when enabled – indicated by a logic "high" on $Leak\_buffer_{EN}$. The leakage buffer is implemented with a unity gain common-source amplifier, and acts as an isolation buffer between the loop filter and the control-loop varactors of the VCO. This buffer is critical during open-loop modulation in pre-serving the carrier at 6.3 GHz as any charge escaping through the anode (formed by the source and drain tied together) of the AMOS varactors can be replenished through the supply, based on V_{FILTER}, instead of being removed from the loop filter. Thus, as long as V_{FILTER} remains constant, the leakage buffer and VCO together provide a steady carrier

frequency for OL modulation. The leakage buffer's optimized transistor sizes are listed in Table 8.

Table 8: Leakage buffer transistor sizes.

Transistor	W / L ratio	Transistor	W / L ratio
M_1	1.5 µm / 360 nm	M_2	1.0 µm / 360 nm

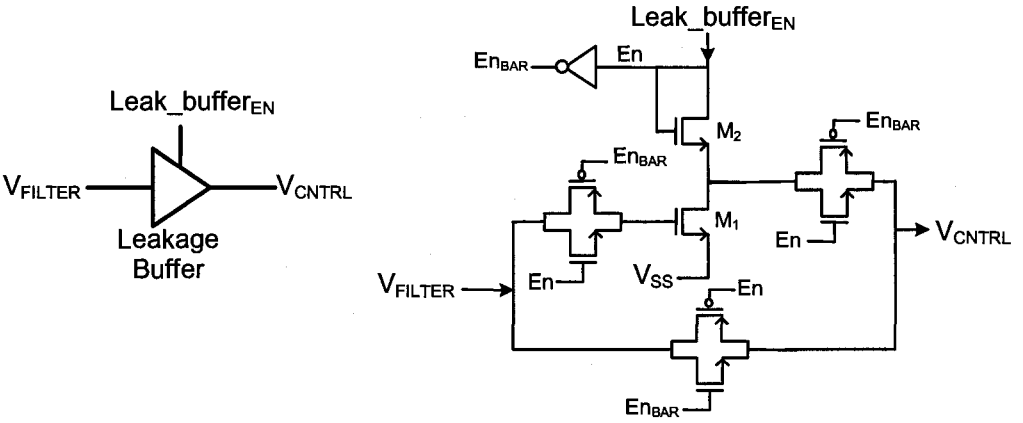

Figure 4-27: Leakage buffer schematic.

4.7. Loop Filter

The loop filter, shown in Figure 4-28, is a second order passive filter. It is designed and implemented such that the PLL of the modulator has a loop bandwidth ω_{3dB} of $2\pi \cdot 215$ kHz with the option to be increased up to 1.7 MHz through laser trimming. As the loop filter is integrated on-chip, this design approach [65] allows flexibility to permanently adjust the locking dynamics of the PLL after fabrication. A narrow loop bandwidth requires a larger filter capacitance. This is advantageous for open-loop modulation as more charge can be stored on the filter, and thus the fraction of any charge leakage will be smaller. However, decreasing the loop bandwidth increases the locking time of the PLL – ceteris paribus. The values of the passives R_1, C_1 and C_2 for a 215 kHz loop bandwidth are 3.42 kΩ, 34.2 pF and 518 pF respectively, assuming the PLL has a frequency response damping factor ζ of 1. These component values are determined using a behav-

ioural PLL simulator called the "PLL" [66]. With regards to loop stability, the phase margin of the loop φ_{PM} [67] is related to the damping factor by

$$\sec(\varphi_{PM}) - \tan(\varphi_{PM}) = \frac{1}{4 \cdot \zeta^2}. \tag{4.35}$$

Determined at the loop bandwidth frequency, the phase margin is 180° minus the phase of the open loop transfer function from the reference to the VCO's output. For a ζ of 1, the PLL is expected to have a φ_{PM} of around 60°. In Table 9 below, the laser trimming sites of Figure 4-28 depict the possible loop bandwidths from the remaining passives connected to the filter line. The natural frequency of the loop ω_n is a measure of the response time of the loop and is related to the loop bandwidth for $\zeta < 1.5$ by the approximation [68]

$$\omega_{3dB} \approx \left(1 + \zeta\sqrt{2}\right) \cdot \omega_n. \tag{4.36}$$

Table 9: Second order loop filter – bandwidth adjustments.

Loop Bandwidth	R_1	C_1	C_2	Laser trimming sites
2π · 215 kHz	3.42 kΩ	34.2 pF	518 pF	none
2π · 425 kHz	6.84 kΩ	8.5 pF	129 pF	X_1
2π · 850 kHz	13.7 kΩ	2.1 pF	33.2 pF	X_1, X_2
2π · 1.7 MHz	27.4 kΩ	480 fF	7.9 pF	X_1, X_2, X_3

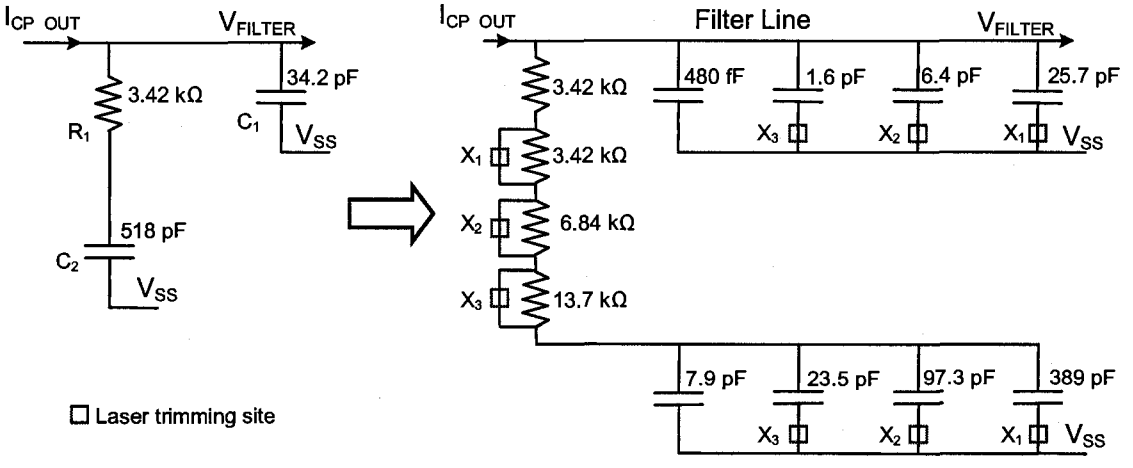

Figure 4-28: Second order passive loop filter schematic.

4.8. VCO Buffer and Output Buffer

The differential outputs of the VCO, $F_{VCO}+$ and $F_{VCO}-$, each drive a buffer as shown in Figure 4-29. Together, the buffers are used to symmetrically load the VCO and provide circuit isolation with a minimum impact on the VCO's performance.

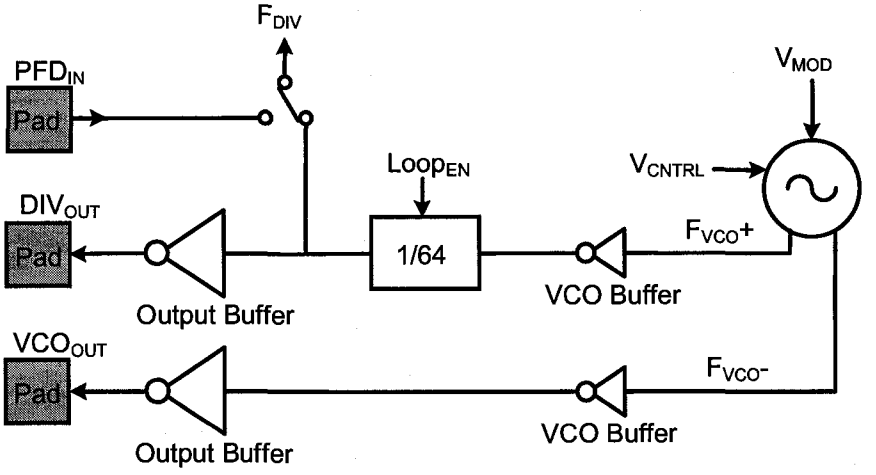

Figure 4-29: PLL feedback path.

The VCO buffer circuit, shown in Figure 4-30, is an ac-coupled inverter with resistive feedback – thereby creating a transresistance amplifier (whose output voltage is proportional to its input current) rather than a voltage amplifier with a very high DC gain [69]. The feedback resistor, denoted by R_1, is 3 kΩ and is used to self-bias the inverter's input to its threshold voltage, desensitizing it to DC offsets. The capacitor, denoted by C_1, is 150 fF and is used to ac-couple the 6.3 GHz carrier frequency to the inverter's input. The VCO buffer's optimized transistor sizes are listed in Table 10.

Table 10: VCO buffer transistor sizes.

Transistor	W / L ratio	Transistor	W / L ratio
M_1	6.0 µm / 120 nm	M_2	18 µm / 120 nm

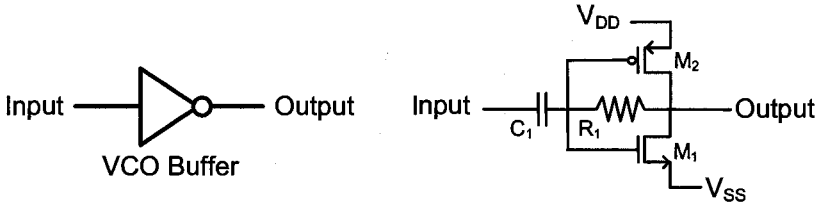

Figure 4-30: VCO buffer schematic.

To observe the 6.3 GHz carrier frequency from the VCO with a spectrum analyzer (at VCO_{OUT}) and the divided-down frequency with an oscilloscope (at DIV_{OUT}), an output buffer is used on each of these paths from the PLL to drive the bond pad and the test equipment's 50 Ω input/load impedance. The output buffer circuit, shown in Figure 4-31, is comprised of 3 cascaded common-source amplifiers. From the buffer's input, each amplifier's current-driving capability is gradually scaled upwards by a factor of about 3. The output buffer is ac-coupled to the test equipment with a 10 pF capacitor, denoted by C_1. This capacitor is excluded from the output buffer circuit on the divided-down frequency path and can be replaced, if needed, with a larger off-chip capacitor. The output buffer's optimized transistor sizes and resistor values are listed in Table 11.

Table 11: Output buffer transistor and resistor sizes.

Transistor	W / L ratio	Resistor	Resistance
M_1	30 µm / 120 nm	R_1	450 Ω
M_2	90 µm / 120 nm	R_2	30 Ω
M_3	162 µm / 120 nm	R_3	150 Ω
		R_4	10 Ω
		R_5	50 Ω

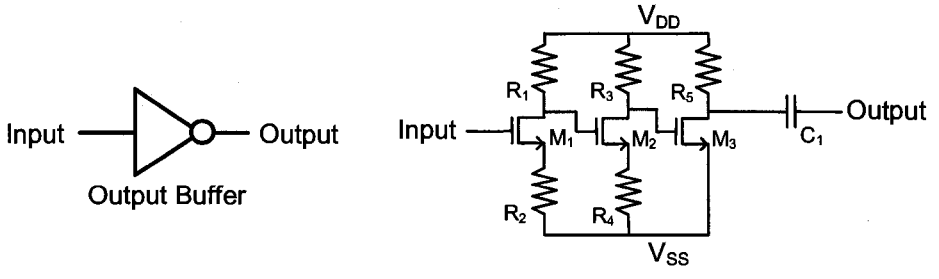

Figure 4-31: Output buffer schematic.

4.9. Test Circuitry

Transmission gates, toggled by the external signal PFD_{TG}, are inserted in the feedback path of the PLL at the PFD as shown in Figure 4-32. In normal PLL operation, when the feedback path is enabled – indicated by a logic "high" on PFD_{TG}, transmission gate TG_A is active, allowing the propagation of the divider's output to the PFD input F_{DIV}, while transmission gate TG_B is inactive. In the event of a suspected non-functioning divider upon fabrication (such as the divisor rate is not equal to 64), the on-chip feedback path of the PLL can be disabled by de-activating TG_A with PFD_{TG}, thereby impeding the propagation of the divider's output to the PFD. At the same time, a logic "low" on PFD_{TG} activates TG_B, allowing the propagation of an external signal of around 98.4375 MHz (at PFD_{IN}) to be sent to the PFD input F_{DIV}. The open-loop response of the PLL can then be observed at VCO_{OUT} to verify for a divider fault. In addition, an off-chip feedback path of the PLL can be established by using an off-chip 6 GHz divider from VCO_{OUT} to PFD_{IN}.

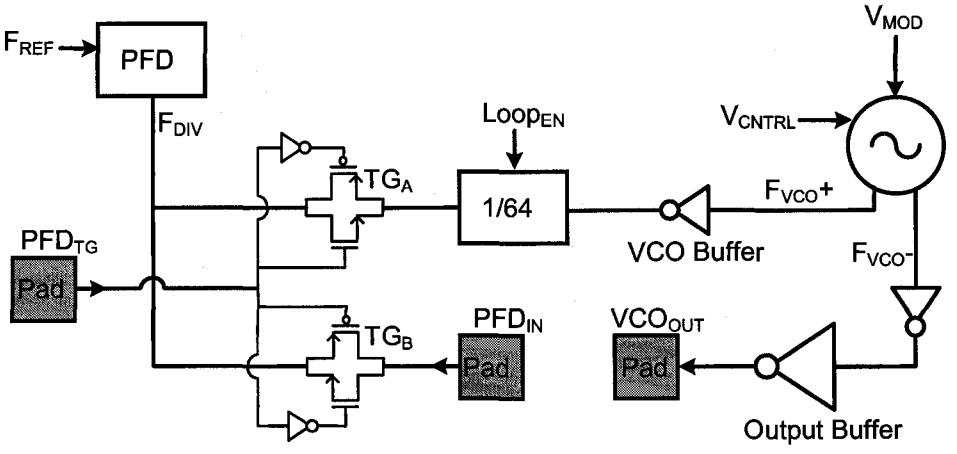

Figure 4-32: Transmission gates TG_A and TG_B for testing.

4.10. TX Design Summary

A low-power and energy-efficient direct open-loop modulation transmitter is disclosed for the SoC transceiver front-end. In this transmitter topology, a PLL-based modulator, encompassing the oscillator with the integrated antenna, operates in open-loop and closed-loop modes. In closed-loop mode, the PLL accurately sets the carrier frequency of the oscillator to 6.3 GHz. Once the VCO is phase locked, the loop is opened and the control-loop line voltage is momentarily held on the loop filter with a leakage buffer to minimize VCO drift. With the modulator in open-loop mode, the VCO is then directly modulated according to BFSK. Furthermore, energy is conserved by disabling the PFD, CP and divider.

The voltage-controlled oscillator of the TX is a complementary *LC* VCO design, which permits a differential peak voltage across the inductive antenna of $\approx$ 1.2 V to meet the antenna power delivered specification of 0 dBm. The conditions to guarantee oscillation start-up under all operating temperatures and worst-case process variations are identified, along with the two regimes observed in the VCO's steady-state operation, namely current-limited and voltage-limited. The performance metric oscillator power efficiency is a ratio of the power delivered to the antenna to the DC power consumed, and this efficiency is expected to reach a maximum value in the voltage-limited regime. A design procedure called "simultaneous *gm* and impedance matching with power optimization" is described for achieving optimum oscillator power efficiency performance ($\eta_{P\text{-}VCO} \approx$ 50%). This procedure is applied in designing the TX's VCO. A study of power efficiency suggested that $\eta_{P\text{-}VCO}$ peaks in a complementary *LC* VCO when the magnitude of the equivalent negative conductance, which is equal to the *gm* of the VCO's devices, is given by the oscillation start-up condition of (4.5). The expected frequency tuning range of the VCO is from 6.06 GHz to 6.47 GHz, and the expected modulation range (for frequency shifting) is –4 MHz to 4.4 MHz about the centre frequency.

The PLL of the modulator uses a low-power divider design, 6 fixed divide-by-two prescalers are cascaded together to realize the required divide ratio of 64. The first 3 prescalers of the divider are implemented using dynamic TSPC logic, while the latter 3 are implemented using static CMOS logic. The divider can be disabled when the PLL loop is opened. A standard tri-state PFD is designed with two resetable D-type flip-flops and an AND gate. A single-ended CP is designed with transistor degeneration on the output current mirror to increase its output impedance and for better current matching between the sinking and sourcing directions. The forward path of the PLL includes three new circuit blocks different from conventional design, namely the up-down mux, loop switch and leakage buffer. The up-down mux is used to swap the inputs to the CP when the leakage buffer is enabled. The loop switch is used to disconnect the output of the CP from the loop filter during open-loop modulation. The leakage buffer is used to minimize charge leakage from the loop filter, and hence VCO carrier drift, in the open-loop mode. The loop filter is a second order passive filter and is designed such that the PLL has a loop bandwidth of 215 kHz. The differential outputs of the VCO drive buffers which are used to provide circuit isolation with a minimum impact on the VCO's performance. Output buffers on the VCO and divider outputs are designed to drive 50 Ω test equipment. Test circuitry is incorporated into the feedback path of the PLL for debugging purposes.

The simulation results of the direct open-loop modulation transmitter chip are presented in the following chapter.

CHAPTER

5. Open-Loop Modulation TX Prototype

In this chapter, the circuit blocks of the direct open-loop modulation transmitter of Chapter 4 are assembled together to form the schematic for the prototype TX chip. Behavioural-level and transistor-level simulations of the TX are conducted and analyzed. Then, the methodology for implementing the TX chip in IBM's 0.13 μm CMOS technology is discussed, along with the layout details of the VCO and the open-loop modulator. The following section presents measurement results of the TX chip. Then, important performance metrics are summarized. Finally, the communication link and the power supply requirements of the TX are assessed.

5.1. Top-Level Schematic

The circuits of the transmitter and its test circuitry are assembled together to form the top-level schematic, shown in Figure A.1 of Appendix A. A block level representation of the TX chip with bond pads is illustrated in Figure 5-1. The signal pins for the chip are listed in Table 12, a description of most of these signals has been given in Chapter 4. The pin labelled VCO_{OUT}/F_{VCO-} is indicating that the signals VCO_{OUT} and F_{VCO-} are both shorted together at the pad, requiring a laser microsurgery technique to disconnect the unwanted signal for testing. The signal pin designations of the pads and their placements

around the chip permit the option to probe the die for testing purposes. The die test setup would require a probing station with a DC probe, high-speed (MHz) probe and two multi-contact (8-pin) wedge probes configured with P-G-S-G-S-S-G-P tip footprints, where P, G, and S stand for DC power, ground, and RF signal (GHz), respectively.

Table 12: TX power, bias, low-frequency and high-frequency signal pins.

Power signals	**Block(s)**
VDD_{PLL}	PFD, Up-Down Mux, CP, Loop Switch, Divider, VCO Buffer(s)
VDD_{VCO}	VCO
VDD_{OUT_BUF}	Output Buffer(s)
$Leak\_buffer_{EN}$	Leakage Buffer
VSS	-common to all blocks-
Bias signals	**Block(s)**
I_{CP_BIAS}	CP
$Loop_{EN}$	PFD, CP, Loop Switch, Divider
PFD_{TG}	TG(s)
Low-frequency signals	**Block(s)**
V_{CNTRL}	VCO
V_{MOD}	VCO
F_{REF}	PFD
PFD_{IN}	TG(s)
DIV_{OUT}	Output Buffer
Radio-frequency signals	**Block(s)**
FVCO+	VCO
VCO_{OUT}/FVCO-	Output Buffer/VCO

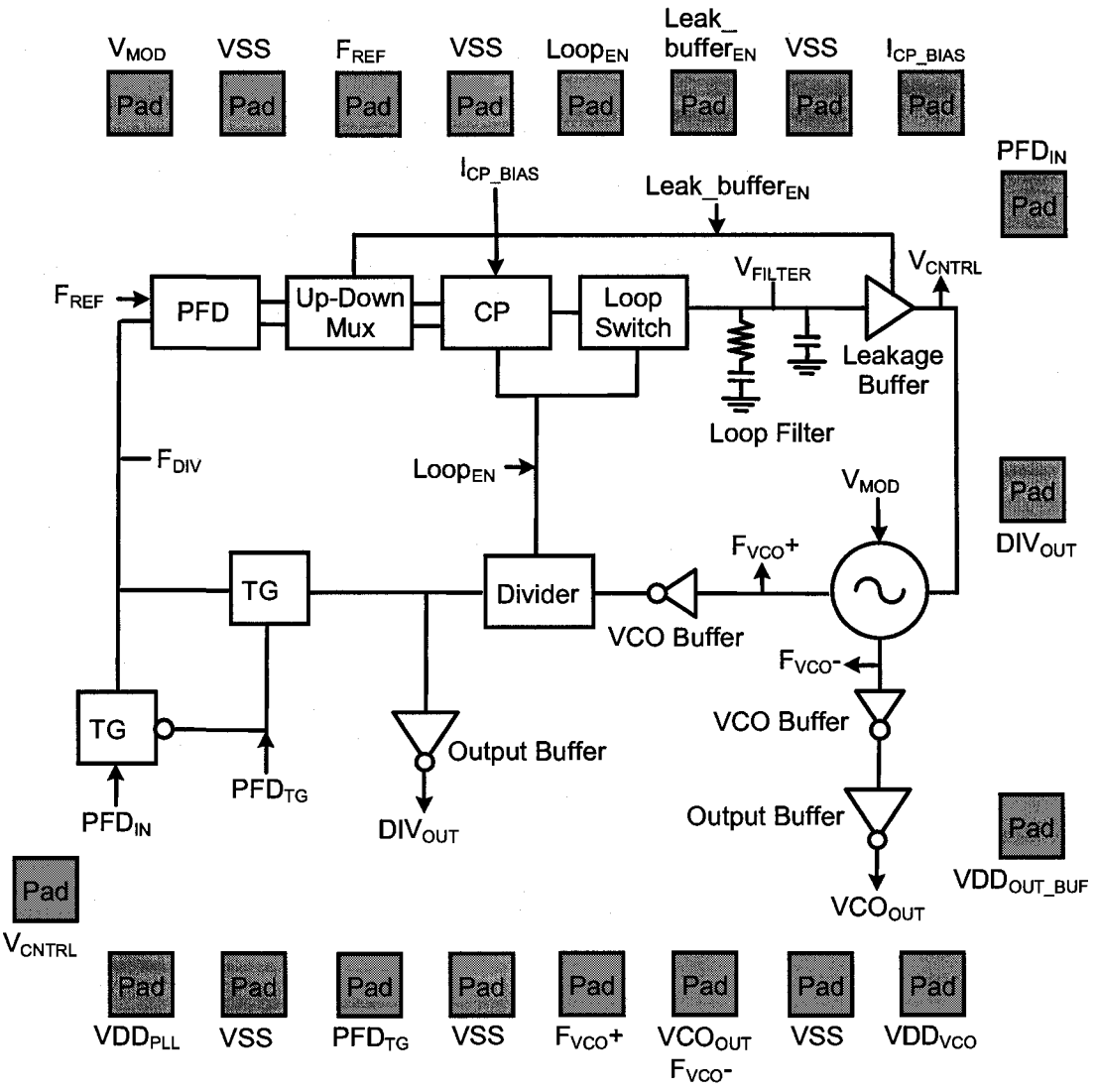

Figure 5-1: TX block-level diagram with bond pads.

5.2. Simulations

The simulations are performed in the Virtuoso Analog Design Environment with 0.13 μm CMOS Spectre models provided from IBM through CMC.

5.2.1. Behavioural-Level

The circuit blocks of the direct OL modulator in Figure 4-2 are modelled with Analog Hardware Description Language (AHDL). This is to permit a system-level simulation of the modulator for a behavioural study of the sequences of events to transmit a packet. In this subsection, the results are presented and re-annotated from Section 3.6 for the reader's convenience.

After a predetermined period of inactivity, the modulator begins the power-up phase $T_{power\text{-}up}$. Although the time required for the transmitter's circuits to reach their biasing points is not modelled, for the most part $T_{power\text{-}up}$ is comprised of the modulator's PLL frequency and phase acquisition time as the PLL locks the VCO to the 6.3 GHz carrier frequency. A simulation of this transient behaviour predicts a locking time of approximately 25 µs as shown in Figure 5-2 by the settling of V_{FILTER} (filter line) from 0 V. During this locking time, V_{MOD} is set mid-rail such that the capacitance of the modulation varactors can later be increased and decreased to vary the VCO's carrier frequency about 6.3 GHz, +/- 500 kHz. Once the VCO is phase locked, a lock detection circuit then opens the PLL with a logic "low" on $Loop_{EN}$. The voltage for a VCO frequency of 6.3 GHz is momentarily held on the second order loop filter with the opening (deactivation) of the loop switch, and this voltage is held and replicated by the leakage buffer to the VCO's control-loop varactors. The $Loop_{EN}$ signal also commences the packet transmission phase, $T_{transmit}$, by initiating a bitstream on V_{MOD} for modulating the VCO's carrier according to BFSK. For a frequency deviation of 500 kHz, the required amplitude on V_{MOD} for the 5 kbps bitstream is 75 mV about the $V_{DD}/2$ offset, as shown in Figure 5-2. This is confirmed through a discrete Fourier transform (DFT) of the FM modulated VCO spectrum which is shown in Figure 5-3. Once the packet is transmitted, the modulator re-enters the powered-down state T_{off}.

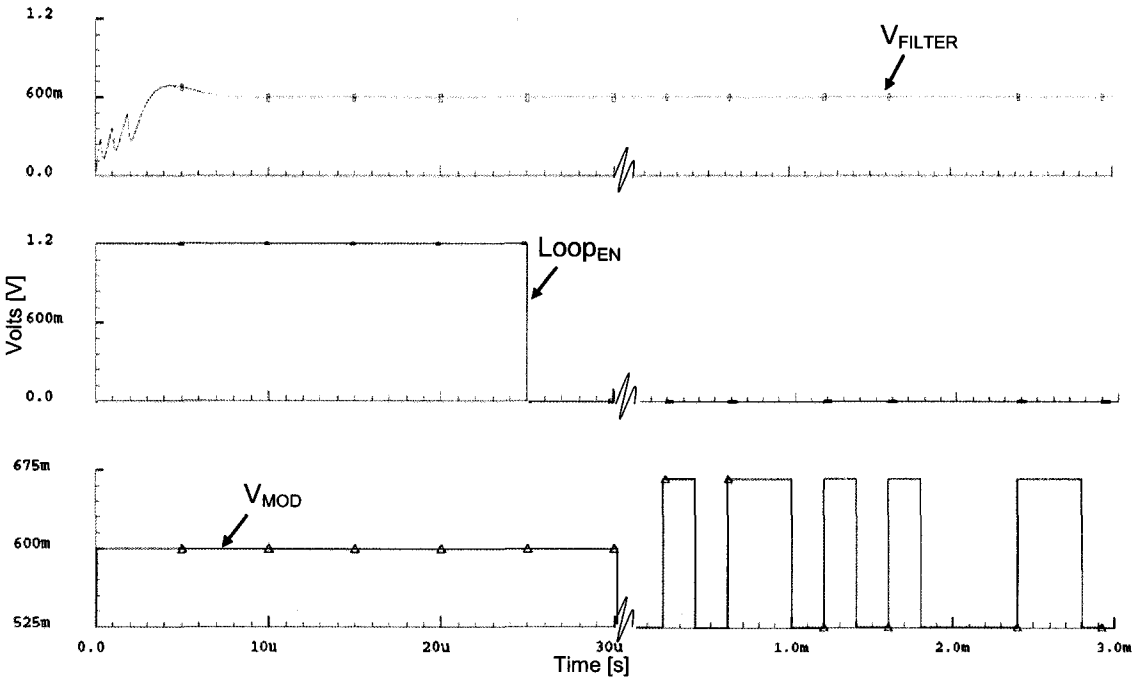

Figure 5-2: Simulation; locking and OL modulating the PLL ($\omega_{3dB} = 2\pi \cdot 215$ kHz).

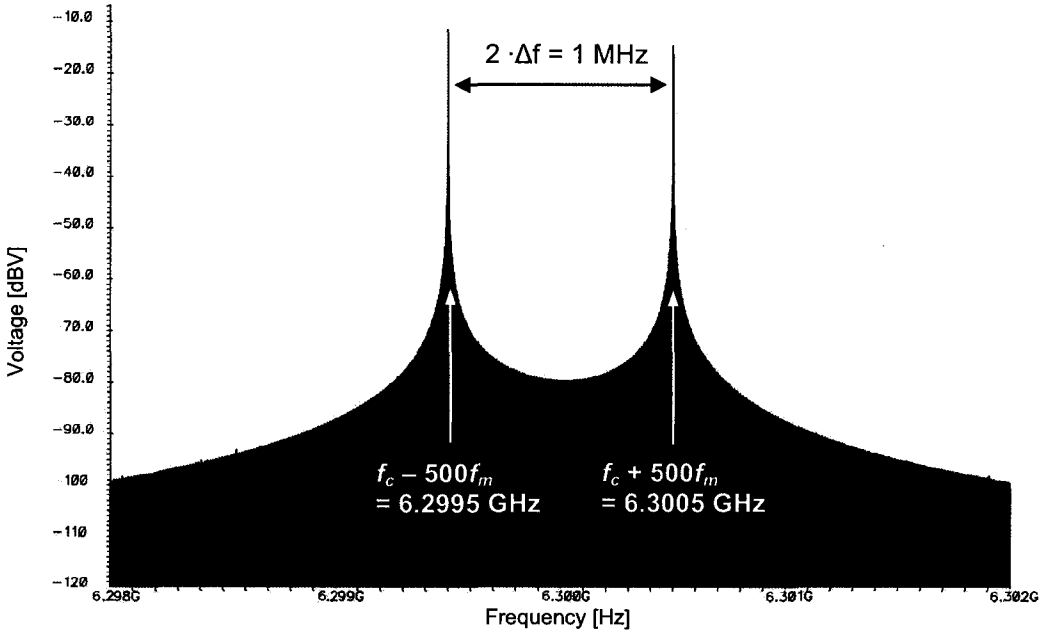

Figure 5-3: Simulation; FM modulated (BFSK) VCO spectrum.

5.2.2. Transistor-Level

A top-level simulation of the TX with device-level models is performed to predict power consumption, study carrier drift and observe the locking behaviour of the TX's PLL.

The simulated results of power consumption by each circuit block of the TX in closed-loop and open-loop modes are listed in Table 13 and Table 14, respectively. The power consumed by the positive supply rails are also listed in these tables. Recalling that when the $Loop_{EN}$ signal is switched from a logic "high" to a logic "low", the loop is opened and the CP and sections of the divider are turned off – which effectively turns off the PFD. Thus, from closed-loop to open-loop modes, the TX power consumption reduces by 1 mW. In the scenario where the TX is operating as an oscillator transmitter, and therefore carrier synchronization would be required at the receiver end, the TX power consumption would be 2.7 mW. The functionality of the test circuitry is verified, and the power consumption by test signal is listed in Table 15.

Table 13: Simulation; TX power consumption in closed-loop mode†.

Power consumption by block	Simulation result
VCO	2.7 mW
Divider	2.3 mW
PFD, Up-Down Mux, CP, Loop Switch, Leakage Buffer	380 µW
VCO Buffer	660 µW
Power consumption by signal	**Simulation result**
VDD_{VCO}	2.7 mW
VDD_{PLL}	4.0 mW

† $Loop_{EN}$ = 1.2 V.

Table 14: Simulation; TX power consumption in open-loop mode[¥].

Power consumption by block	Simulation result
VCO	2.7 mW
Divider	1.4 mW
PFD, Up-Down Mux, CP, Loop Switch, Leakage Buffer	300 µW
VCO Buffer	650 µW
Power consumption by signal	**Simulation result**
VDD_{VCO}	2.7 mW
VDD_{PLL}	3.0 mW

[¥] $Loop_{EN}$ = 0 V.

Table 15: Simulation; TX test circuitry power consumption.

Power consumption by test signal	Simulation result
$VDD_{PADBUFFER}$	54.1 mW
DIV_{OUT}	3.5 mW
VCO_{OUT}	1.3 mW

Output Buffer (at 6.3 GHz) 27.5 mW
Output Buffer (at 98.4375 MHz) 26.6 mW

The effectiveness of the leakage buffer to help minimize leakage current and maintain a constant voltage on the filter line to reduce open-loop carrier drift is studied. The rate-of-change, or slope, of the voltage on the filter line (V_{FILTER}) with respect to time is related to the leakage current $I_{leakage}$ by capacitance as expresses in

$$\frac{I_{leakage}}{C_{FILTER}} = \frac{\Delta V_{FILTER}}{\Delta t} \tag{5.1}$$

where C_{FILTER} is the capacitance of the loop filter and approximated to C_2. As the control-loop varactor gain (K_{VCO} = 340 MHz/V) describes the change in oscillation frequency with respect to the control-loop line (V_{CNTRL}), the carrier's drift rate $\Delta f_{OSC}/\Delta t$ can be analytically approximated by

$$\frac{\Delta f_{OSC}}{\Delta t} = \frac{\Delta V_{FILTER} \cdot A_{leakage\_buf}}{\Delta t} \frac{\Delta f_{OSC}}{\Delta V_{CNTRL}} \approx \frac{-\Delta V_{FILTER}}{\Delta t} K_{VCO} \tag{5.2}$$

where $A_{leakage\_buf}$ is the voltage gain of the leakage buffer which is ≈ -1. A simulation monitoring the slope of V_{FILTER} when the loop is opened is shown in Figure 5-4 for the

cases when the leakage buffer is enabled (i.e. used in the loop) and disabled (i.e. not used in the loop) by $Leak\_buffer_{EN}$. When the leakage buffer is enabled, the slope of V_{FILTER} is –1 V/s and the corresponding $\Delta f_{OSC}/\Delta t$ is 340 Hz/µs. Alternatively, when the leakage buffer is disabled, the slope of V_{FILTER} is –220 V/s and the corresponding $\Delta f_{OSC}/\Delta t$ is –75 kHz/µs (removing the $A_{leakage\_buf}$ term from (5.2)). Thus, the leakage buffer is expected to reduce carrier drift by a magnitude of 220 times. The carrier's drift rate is observed with respect to selected ambient temperatures, the simulated results listed in Table 16 show no significant change in the drift rate.

Table 16: Simulation; Carrier drift rate over ambient temperature.

Temperature	Leakage buffer	Drift rate
0°C	Enabled	370 Hz/µs
27°C	Enabled	340 Hz/µs
54°C	Enabled	290 Hz/µs

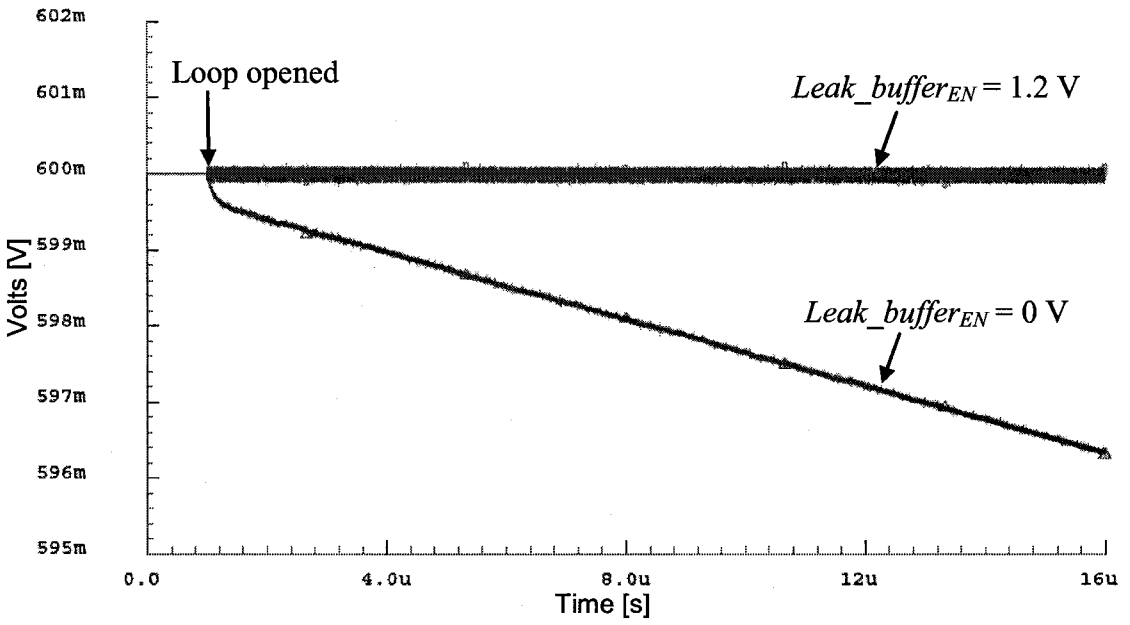

Figure 5-4: Simulation; open-loop voltage slope on V_{FILTER}.

The drift rate of the carrier determines the packet size (L_{packet}) which can be transmitted when the loop is opened for modulation, as a carrier drift equal to Δf will move the

carrier outside the injection-locking bandwidth of the RX. This relationship can be analytically expressed as

$$\Delta f = L_{packet} \cdot T_{bit} \cdot \frac{\Delta f_{OSC}}{\Delta t} = T_{ransmit} \cdot \frac{\Delta f_{OSC}}{\Delta t}. \tag{5.3}$$

As the intended frequency deviation is 500 kHz and the intended data rate is 5 kbps for the RX, the packet size for a transmission is therefore limited to 7 bits in length when the leakage buffer is enabled. To accommodate a larger packet size, the packet would have to be transmitted in parts to allow the TX's loop to periodically close to re-lock the carrier back to 6.3 GHz. In the case when the RX is fitted with a 6.7 dBi off-chip patch antenna, higher data rates are supported according to Figure 3-11, and therefore carrier drift is no longer an issue when determining the packet size.

To reduce the time required to lock the TX's PLL to 6.3 GHz, and decrease simulation time, the bandwidth of the loop filter is increased from 215 kHz to 1.7 MHz. The simulated filter line and control-loop line voltages as the loop acquires lock from power-up are shown in Figure 5-5, the inverting action of the leakage buffer is clearly observed. With the increased bandwidth, these voltages have a settling time of approximately 2 µs. The simulated performance of the TX is summarized in Table 17.

Table 17: Simulation; TX results summary.

Specification	Simulation result
Supply voltages	1.2 V and 0 V
PLL frequency tuning range (K_{MOD} = 0.6 V)	6.13 GHz to 6.43 GHz
VCO frequency tuning range (K_{MOD} = 0.6 V)	6.06 GHz to 6.47 GHz.
Modulation range (K_{VCO} = 0.6 V)	–4 MHz to 4.4 MHz
K_{VCO}	340 MHz/V
K_{MOD}	7 MHz/V
VCO Phase noise @ 1 MHz offset (free-running)	–114 dBc/Hz
PLL settling time ($\omega_{3dB} = 2\pi \cdot 215$ kHz)	≈ 25 µs
PLL settling time ($\omega_{3dB} = 2\pi \cdot 1.7$ MHz)	≈ 2 µs
Carrier drift rate (27°C)	340 Hz/µs

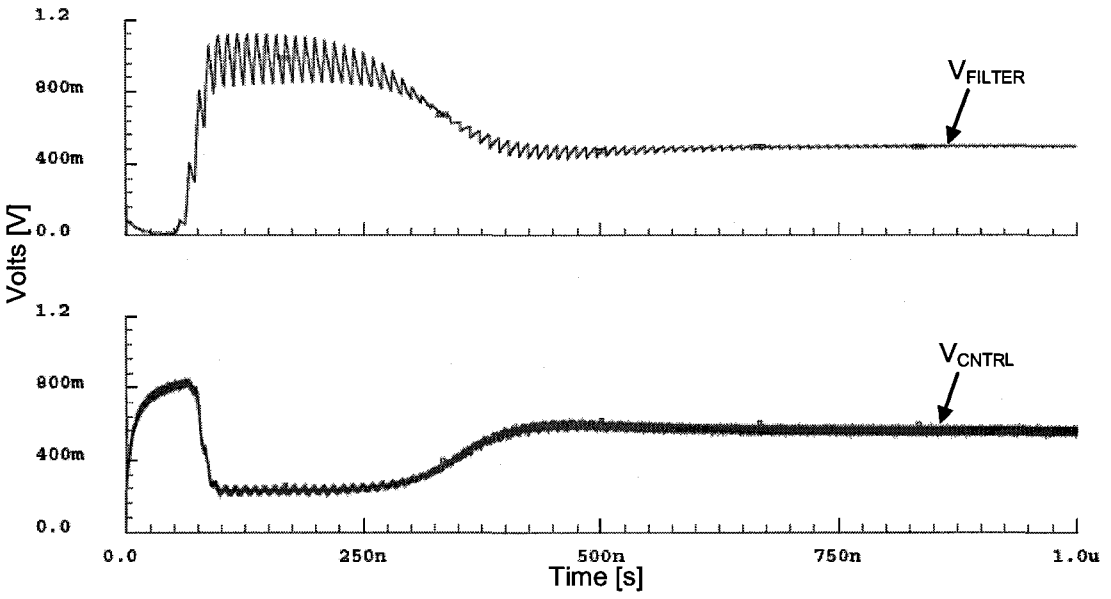

Figure 5-5: Simulation; locking the PLL ($\omega_{3dB} = 2\pi \cdot 1.7$ MHz).

5.3. Implementation

The layout of the TX chip is accomplished with the Virtuoso Layout Suite from Cadence. The die area allocated by CMC for this chip design is 2 mm^2. Due to this space constraint, and the unavailability of extra multi-contact wedge probes, the circuit blocks of Figure 5-1 share a common negative supply rail (VSS) which is connected to ground. For similar reasons, all the circuit blocks of the TX chip, except for the VCO, share a common positive supply rail (VDD_{PLL}) which is connected to 1.2 V.

At the system-level of the TX, the power distribution technique called "star distribution", or "star connection", is applied to minimize the coupling of circuit-induced and magnetically-induced supply current noise [70]. In the case of the former, and with reference to the system's ground, the finite resistance of the grounding path can cause voltage drops to develop if the returning current is significant. This in turn will make the local ground for circuits along the ground path to the VSS pad different than zero volts, and

would negatively impact the performance of linear circuits, such as amplifiers, which use ground as a reference potential. For a high-powered multi-gigahertz divider, the returning current is time varying and could induce noise in the system by coupling through the stray capacitances of the bias network for the amplifier and subsequently be amplified. Noise can also be induced in linear circuits from magnetically-induced supply current. In a system with a ground loop, i.e. multiple current return paths from a circuit to the VSS pad, circulating currents in the ground can be caused by changing external magnetic fields. These currents can be large enough to cause voltage drops along the grounding path due to its finite resistance, leading to supply current noise as described earlier. When the star distribution technique is applied to a negative supply rail in the layout, a physical point is chosen to connect all the negative supply paths of the various circuit blocks. This can also be done when there is a common positive supply rail. The main objective of star distribution is to ensure that a supply path with high current does not allow the current to flow through a sensitive supply path and potentially couple noise in the system.

At the circuit-level of the TX, the bypassing technique is applied to minimize the effects of noise or perturbations on the supply rails. Bypassing is the reduction of high frequency current flow in a high impedance path by shunting that path with a bypass, usually a capacitor [71]. A bypass capacitor C_{bypass} is placed at each of the circuit blocks of Figure 5-1 between supply rails which radiated from a star distribution. A measure of how well a circuit rejects a ripple of various frequencies originating from the supply rail is known as the power supply rejection ratio (PSRR).

At the device-level of the TX, triple-well technology is applied by using substrate-isolated n-FETs. This is to minimize noise coupling through the conductive substrate to the n-FETs. A cross section of a triple-well structure is shown in Figure 5-6 c), where the n-FET is located in an isolated n-well. Noise isolation between the integrated-antenna, digital, analog and RF sections of the TX is a major concern due to their close proximity to one another.

The applied techniques to suppress on-chip noise are illustrated in Figure 5-6.

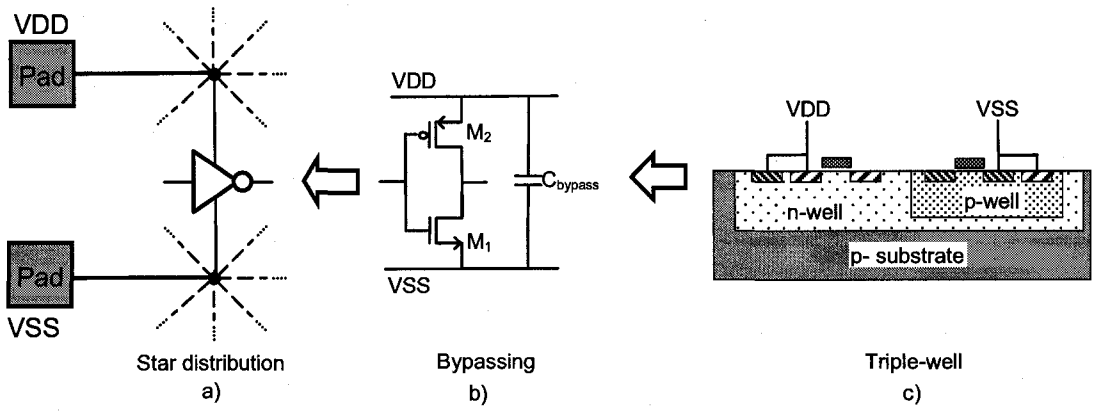

Figure 5-6: Noise suppression; a) system, b) circuit and c) device levels.

5.3.1. Layout

A picture of transmitter's layout, without the metal-fill, is shown in Figure 5-7. A more detailed view of this layout is located in Figure A.3 of Appendix A, as well as layout legend for notable layers and their purpose in Figure A.2. The voltage-controlled oscillator is located inside the rectangular loop formed by the integrated antenna and close to its feed point. The rest of the PLL circuit blocks are located outside of the loop, along the bottom left side of the antenna. The loop filter also occupies a significant portion of the chip space as just over 0.5 nF of capacitance is integrated for a loop bandwidth of 215 kHz. A layout extraction of the chip is done to model the resistive and capacitive parasitics from the interconnect layers, and post-layout simulations are conducted to verify the transmitter's performance.

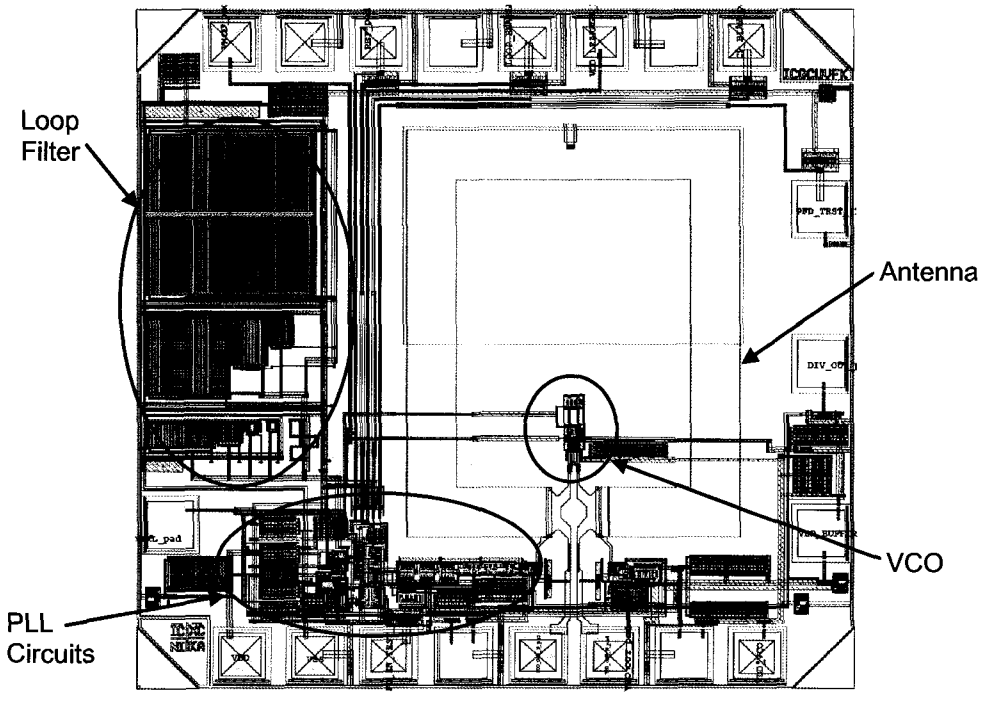

Figure 5-7: Layout of transmitter chip (without metal-fill).

5.3.2. Fabrication

A microphotograph of the fabricated transmitter chip is shown in Figure 5-8. The PLL, loop filter, VCO and integrated antenna sections of the chip are labelled. The TX chip occupies a die area of 2 mm^2.

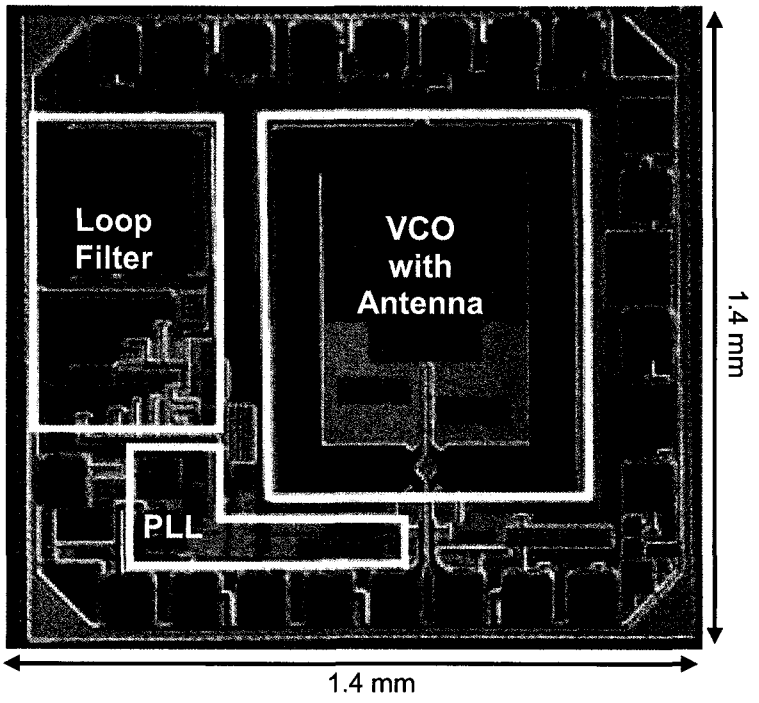

Figure 5-8: Microphotograph of transmitter in 0.13 μm CMOS.

5.4. Measurements

The TX chip is mounted on a printed circuit board (PCB) using chip-on-board wire bonding techniques. This facilitated the testing of the chip by providing more robust and repeatable measurements than die probing methods. The PCB was designed by Peter Popplewell and intended for his Master's research [72]. With some minor trace modifications, the PCB was successfully adapted for the pad placements of the TX chip. A photo of the populated PCB with the TX chip is shown in Figure 5-9.

The measurement experiments performed on the TX chip and the associated results are presented in the following subsections, these include PLL loop bandwidth, PLL locking time, VCO phase noise, CP current mismatch, frequency tuning range, modulation range, carrier drift, FM modulation, antenna impedance, antenna radiation, and transceiver front-end communication.

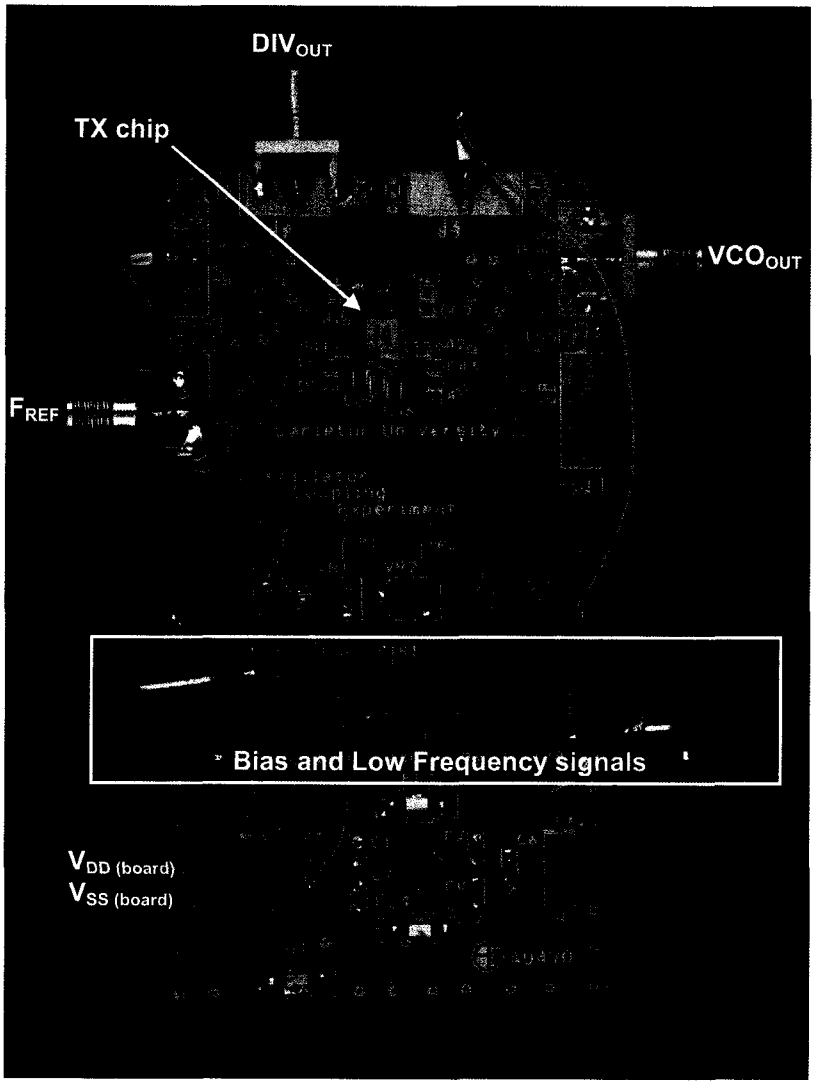

Figure 5-9: Photograph of Populated PCB with TX chip.

5.4.1. PLL Loop Filter Bandwidth

The PLL's loop bandwidth is the unity gain frequency of the transfer function of the forward loop path shown in Figure 4-24. As this would be a fairly complex measurement, requiring a network analyzer, the 0 dB bandwidth of the noise spectrum is measured instead since it is a sufficient estimate of the loop filter bandwidth [73]. The 0 dB bandwidth is defined as the frequency where the phase noise falls back to the level of the

close-in value (adjacent to the carrier's fundamental tone) after rising to its peak value. From Figure 5-10, a screen capture from a Hewlet Packard Spectrum Analyzer, the measured 0 dB bandwidth is found to be 150 kHz. Therefore, ω_{3dB} is $\approx 2\pi \cdot 150$ kHz, which is 70% of the anticipated bandwidth from simulation.

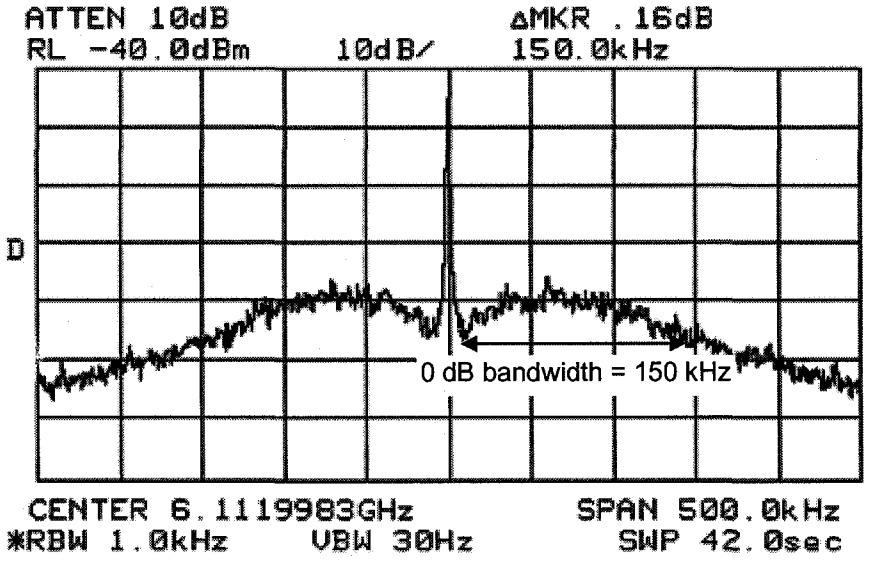

Figure 5-10: Measurement; PLL loop filter bandwidth.

5.4.2. PLL Locking Time

The transient step response of the PLL to a 2.7 MHz step at the reference input is shown in Figure 5-11, a screen capture from a Tektronix Oscilloscope (TDS684B) observing the control-loop voltage. As the frequency of the ringing of the transient response is the natural frequency of the loop, ω_n can be derived by measuring the period of the ringing T_n which is determined to be 16.2 μs. Hence, ω_n is equal to $2\pi \cdot 62$ kHz. From (4.36), which relates the natural frequency to the loop bandwidth, ω_{3dB} from this step response is $\approx 2\pi \cdot 150$ kHz for a ζ of 1 and this result agrees with the loop bandwidth measurement estimation in Subsection 5.4.1. However, from the transient response of Figure 5-11, the damping factor appears to be slightly less than one, which suggests the loop bandwidth is less than 150 kHz. The settling time $T_{settling}$ of the PLL is found to be ≈ 65 μs. The dis-

crepancy between this measured settling time and the calculated settling time of 25 μs is attributed to the loop bandwidth appearing 1.4 times smaller than the design specification of $2\pi \cdot 215$ kHz. Settling time is the sum of the PLL's frequency and phase acquisition time, the former being inversely proportional to the square of ω_{3dB}, while the latter being inversely proportional to ω_{3dB} [68]. A characteristic of the PLL in frequency acquisition mode (from a large step in frequency) is the occurrence of cycle slipping on the control-loop voltage. This is not evident on V_{CNTRL} in Figure 5-11, and the reason may be attributed to the leakage buffer filtering out the cycle slips on V_{FILTER} as seen in Figure 5-5 from simulation.

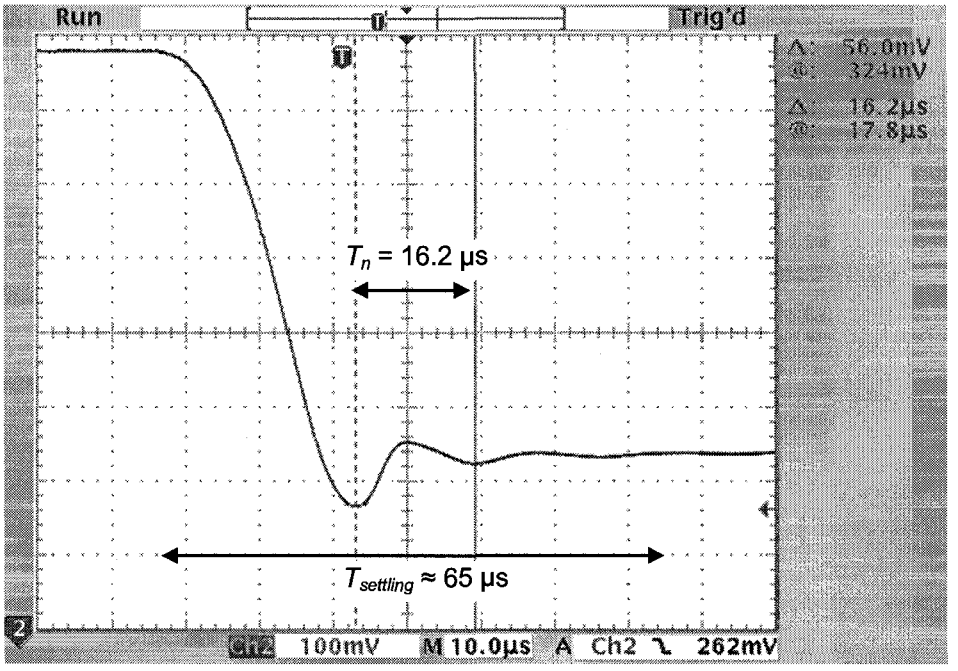

Figure 5-11: Measurement; PLL transient step response on V_{CNTRL}.

5.4.3. VCO Phase Noise

The phase noise performance of the VCO is shown in Figure 5-12 – a screen capture from a Hewlet Packard Spectrum Analyzer (HP8564E) with a phase noise measurement module. Figure 5-12 depicts the phase noise as a function of frequency offsets from the

VCO's oscillating frequency (f_{OSC}) when the PLL is in closed-loop and open-loop operation modes. In open-loop, when modulation of the VCO is to occur, the measured phase noise is dominated by the VCO and is –97 dBc/Hz at 1 MHz offset. The discrepancy between this measurement and the simulated phase noise result is discussed in Section 5.5. The measured closed-loop PLL phase noise is relatively flat in-band and then rolls off with a slope of 20 dB/decade out-of-band until the noise floor is reached, as expected.

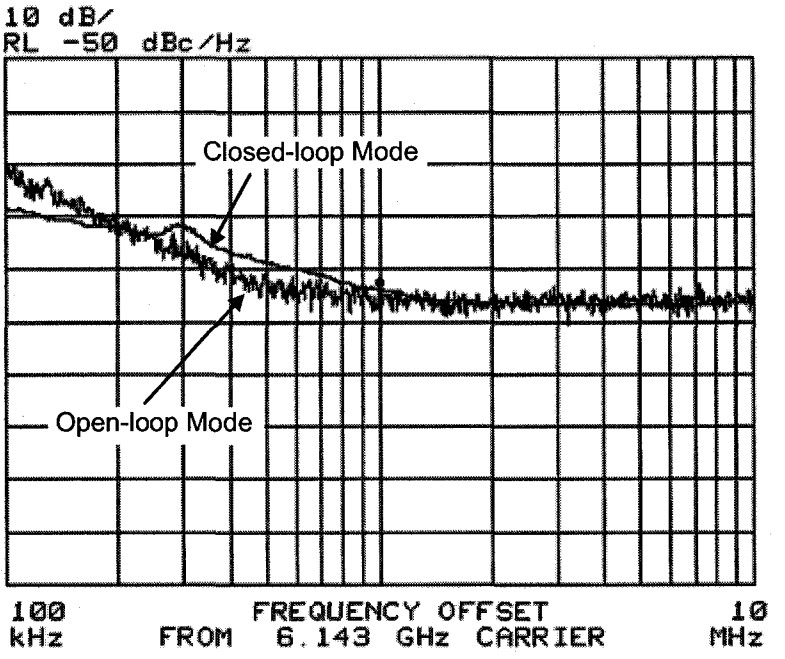

Figure 5-12: Measurement; VCO phase noise as a function of f_{OSC} offset.

5.4.4. Charge Pump Current Mismatch

The current matching between the sinking (attributed to a V_{DOWN}/V_{UP} pulse) and sourcing (attributed to a V_{UP}/V_{DOWN} pulse) directions is measured as the output voltage at the I_{CP_OUT} branch is varied, and the simulated results are plotted in Figure 5-13.

To set the output voltage, the leakage buffer is disabled with a logic "low" on $Leak\_buffer_{EN}$ such that the loop filter is directly connected to the control-loop varactors

of the VCO by a transmission gate as shown in Figure 4-27. This configuration allows the voltage on the loop filter, and hence the voltage on I_{CP_OUT}, to be directly set and varied by an external power source on the V_{CNTRL} pad. With the leakage buffer disabled, the V_{UP} and V_{DOWN} inputs to the up-down mux are no longer swapped. Therefore, V_{DOWN}/V_{UP} pulses are a result of V_{DOWN} pulses from the PFD when the frequency of F_{DIV} is greater than F_{REF}, and alternatively, V_{UP}/V_{DOWN} pulses are a result of V_{UP} pulses. To observe the sinking capability of the CP, the F_{REF} signal is grounded at the pad, and the current drawn from the power source on V_{CNTRL} is recorded. The sourcing capability is similarly observed by grounding the F_{DIV} signal, which is achieved by disabling the feedback path of the PLL (shown in Figure 4-32) with a logic "low" on PFD_{TG} and the grounding of PFD_{IN} at the pad.

From Figure 5-13, the output voltage point at which there is a zero current mismatch is 0.6 V. However, when this voltage changes by 100 mV in either direction, the current mismatch is approximately 10%.

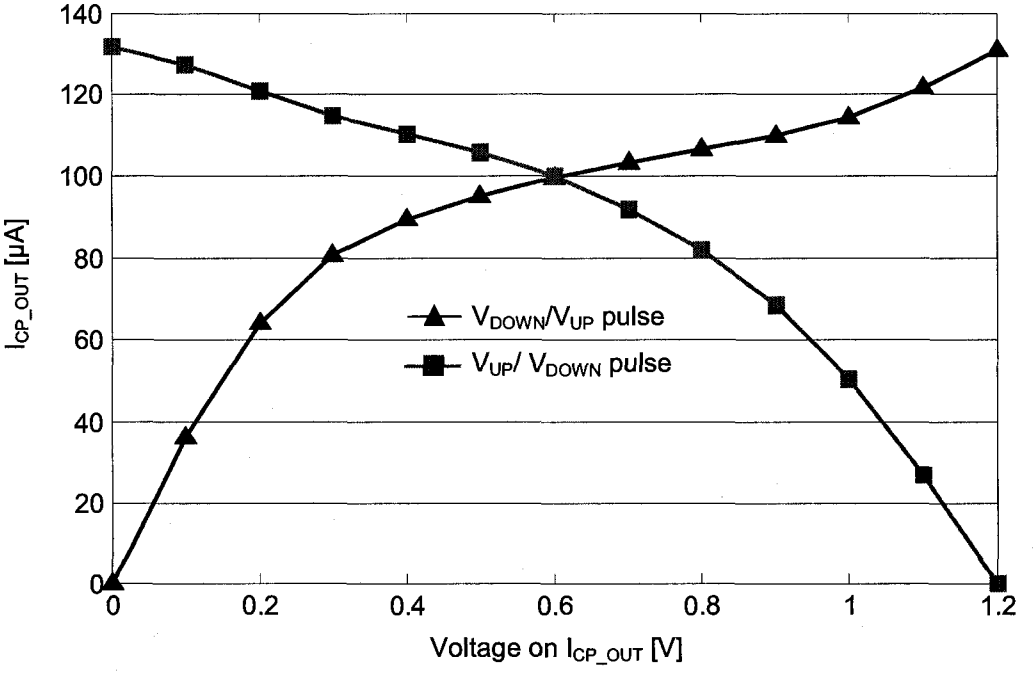

Figure 5-13: Measurement; I_{CP_OUT} as a function of output voltage.

5.4.5. Frequency Tuning Range

The VCO's frequency of oscillation as a function of the control-loop line voltage (V_{CNTRL}) for V_{MOD} = 0.6 V is measured and plotted in Figure 5-14. The VCO's frequency turning range is about 8% (from 6.087 GHz to 6.596 GHz). The control-loop varactor gain K_{VCO} is ≈ 420 MHz/V. When the leakage buffer is enabled, the frequency tuning range achieved by the PLL is from 6.120 GHz to 6.585 GHz.

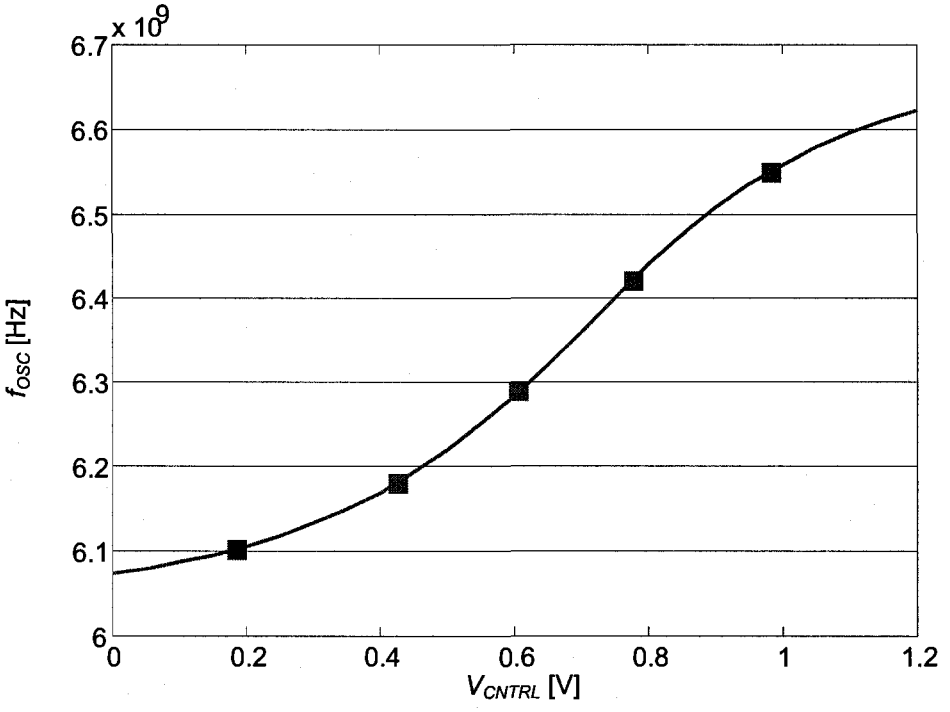

Figure 5-14: Measurement; f_{OSC} as a function of V_{CNTRL}.

5.4.6. Modulation Range

The oscillation frequency in terms of its offset from 6.27784 GHz is plotted in Figure 5-15 as a function of V_{MOD} for V_{CNTRL} = 0.6 V. The measured modulation varactor gain K_{MOD} is approximately 7.5 MHz/V, which is observed between a V_{MOD} of 0 to 1.2 V.

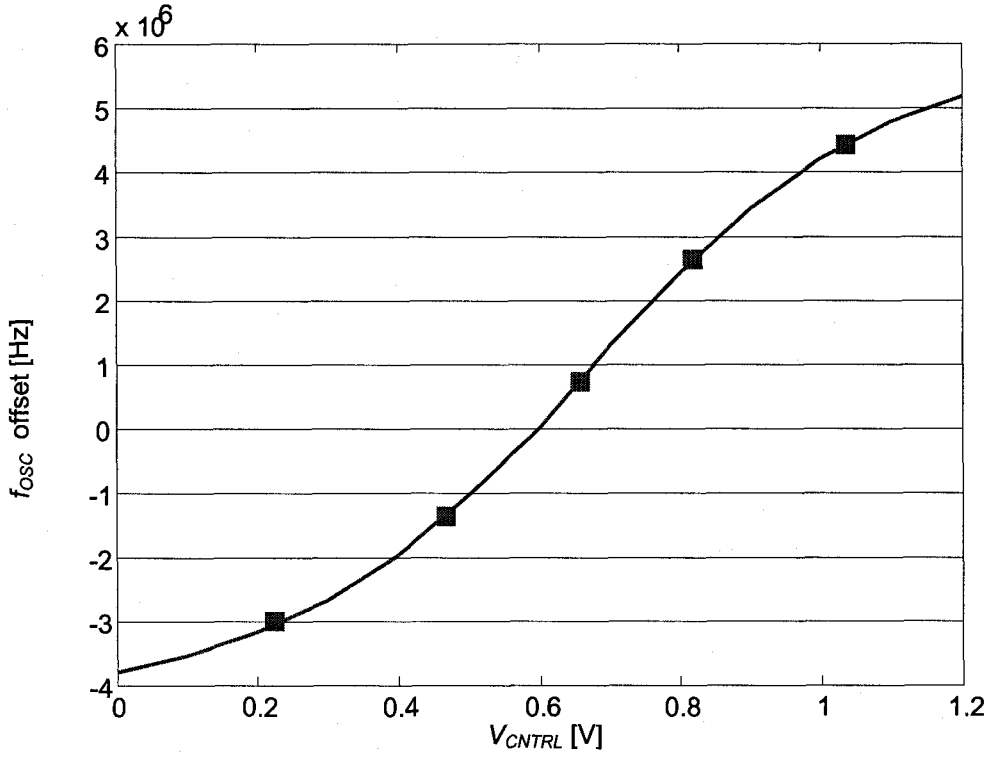

Figure 5-15: Measurement; f_{OSC} offset from 6.27784 GHz as a function of V_{CNTRL}.

5.4.7. Carrier Drift

Due to supply-voltage fluctuation, noise on the VCO control line (coupled with significant varactor gain), and the leakage current of charge on the loop filter, direct open-loop VCO modulation generally suffers from a drift in the centre frequency f_C of transmission. The direction of frequency drift can be increasing (positive) and/or decreasing (negative) with respect to f_C. For this PLL design, when the loop is opened by the signal $Loop_{EN}$, an injection of charge on the loop filter from the loop switch is likely. This would cause a negative frequency drift Δf_{C_neg} of the carrier due to the voltage inverting leakage buffer driving V_{CNTRL}. While the loop is opened, there is a leakage of charge on the loop filter, decreasing V_{FILTER}. This would cause a positive frequency drift Δf_{C_pos} of the carrier due to the voltage inverting leakage buffer. The positive frequency drift is expected to increase with T_{open_loop} – the time during which $Loop_{EN}$ is disabled.

The test-setup to quantify the carrier drift performance of the TX is illustrated in Figure 5-16. The TX is powered-up and its PLL is locked to an f_C of 6.27127 GHz. A square wave signal generator is used to enable/disable $Loop_{EN}$, during which the VCO spectrum is observed with a spectrum analyzer. As the loop is opened and closed, the outermost frequency drifts of the carrier are measured using the spectrum analyzer's "max hold" function – a screen capture of this is shown in Figure 5-17 for a particular T_{open_loop}. The positive (Δf_{C_pos}) and negative (Δf_{C_neg}) frequency drifts, as well as their spot drift rates (in Hz per T_{open_loop}), are plotted in Figure 5-18 and Figure 5-19, respectively, for a V_{MOD} fixed to 0.6 V. As expected, the positive frequency drift increases with T_{open_loop}, and this is reflected with reasonably constant spot drift rate average of $\approx$ 220 Hz/µs, which is comparable to the simulated drift rate result of 340 Hz/µs. Alternatively, although the deviation in negative frequency drift is more significant than Δf_{C_pos}, Δf_{C_neg} is relatively independent of T_{open_loop}. Hence, the negative spot drift rate exhibits a decreasing trend with T_{open_loop}.

The impact of frequency drift on the data rate for modulation can be explained with the aid of Table 18. The TX data rate for communicating with the RX, connected to an integrated antenna, is limited to 5 kbps. Although, as shown in Figure 3-11, higher communication link data rates can be supported when the RX is connected to an off-chip antenna. In the case when T_{open_loop} is 0.3 ms, a packet size (L_{packet}) of 1 bit is possible for an R_{data} = 5 kbps. In addition, Δf_{C_pos} and Δf_{C_neg} would be a significant fraction of the 500 kHz frequency deviation (Δf) required for FM modulation (BFSK). A more acceptable packet size of 9 bits is possible if R_{data} is increased to 30 kbps. As this increase would necessitate a large RX injection locking bandwidth, and hence Δf, of 3 MHz according to Figure 3-11, frequency drift of the carrier is no longer a concern. When T_{open_loop} is 3.33 ms, a 99 bit or $\approx$ 100 bit packet is possible for an R_{data} = 30 kbps. Logically, a 1 kbit packet would require an R_{data} = 300 kbps.

Table 18: Modulation data rate considerations for frequency drift.

T_{open_loop}	0.3 ms	3.33 ms
Δf_{C_pos}	92 kHz	500 kHz
Δf_{C_neg}	133 kHz	330 kHz
L_{packet} for R_{data} = 5 kbps	1 bit	16 bits
L_{packet} for R_{data} = 30 kbps	9 bit	99 bits
L_{packet} for R_{data} = 300 kbps	90 bits	999 bits

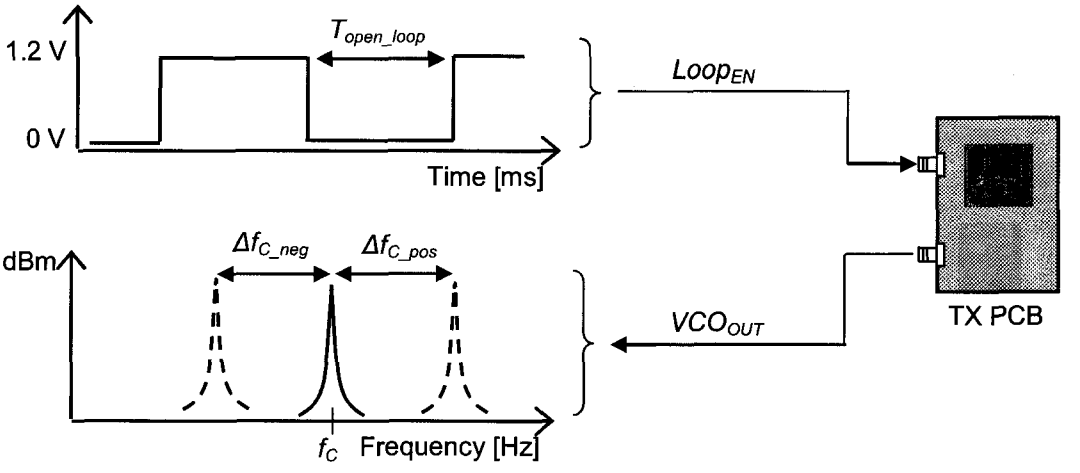

Figure 5-16: Carrier drift measurement test-setup.

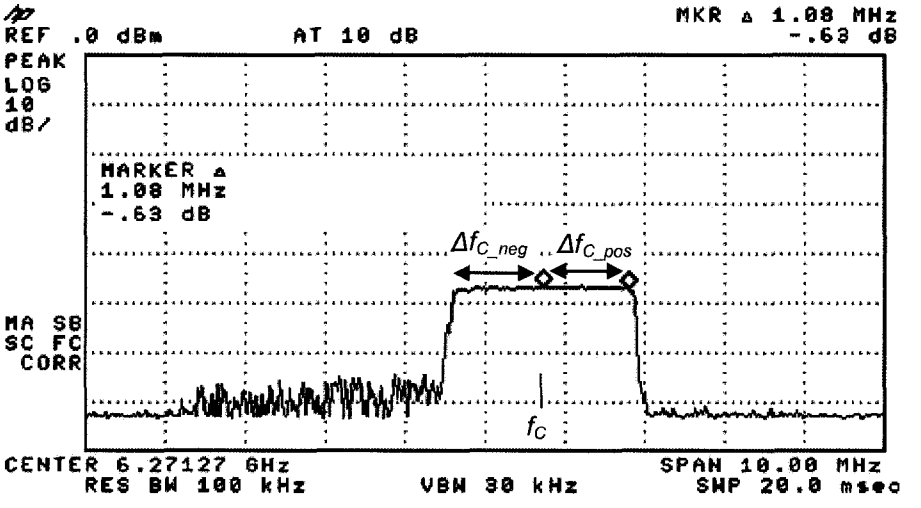

Figure 5-17: Measurement; carrier drift spectrum.

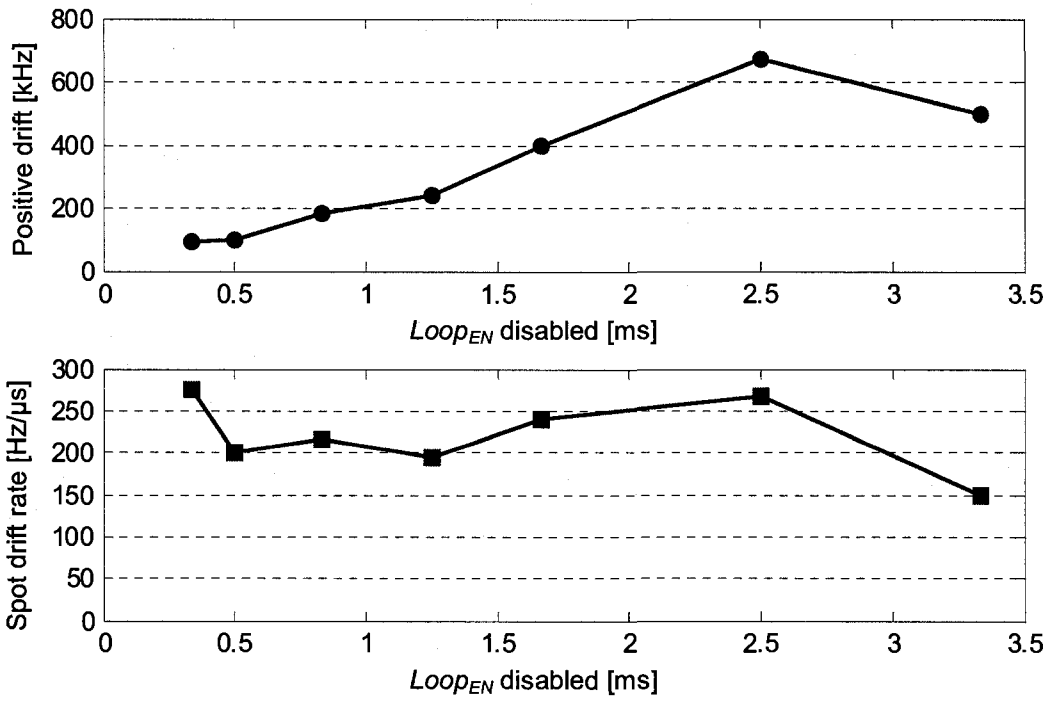

Figure 5-18: Measurement; Δf_{C_pos} as a function of T_{open_loop}.

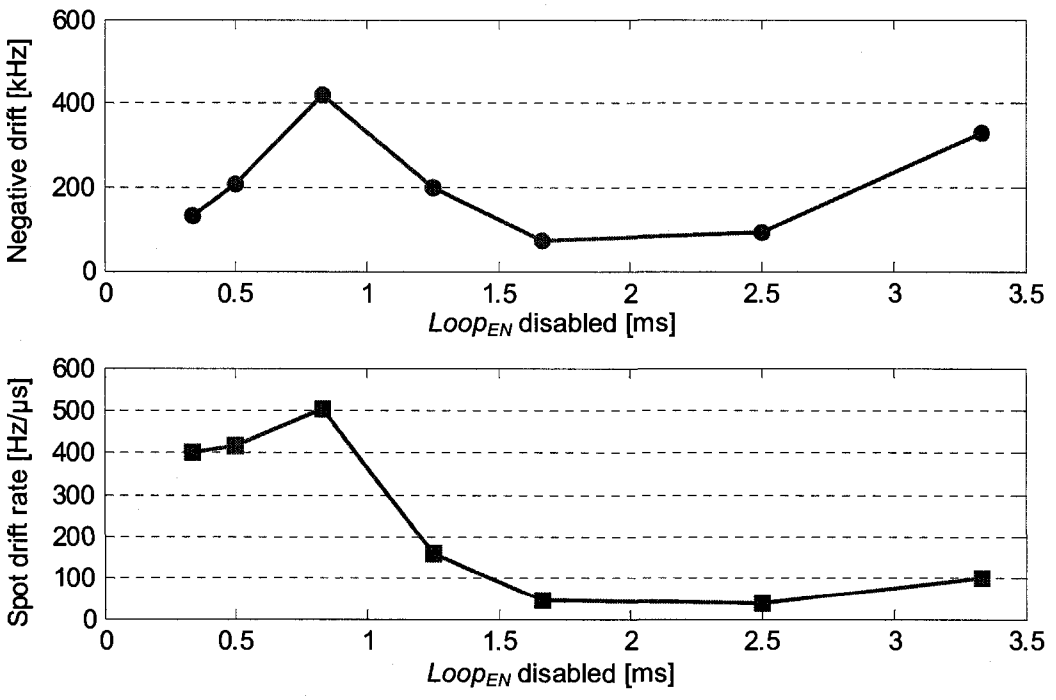

Figure 5-19: Measurement; Δf_{C_neg} as a function of T_{open_loop}.

5.4.8. FM Modulation (BFSK)

The spectrum of the FM carrier with a frequency deviation of 3 MHz at a rate of 300 kbps is shown in Figure 5-20, depicting a wideband signal using BFSK with a modulation index $m = 20$. The voltage on V_{CNTRL} is externally fixed such that the carrier centre frequency is 6.3 GHz. To communicate with the RX at this rate, a frequency deviation of 30 MHz is required according to the theory of Figure 3-11.

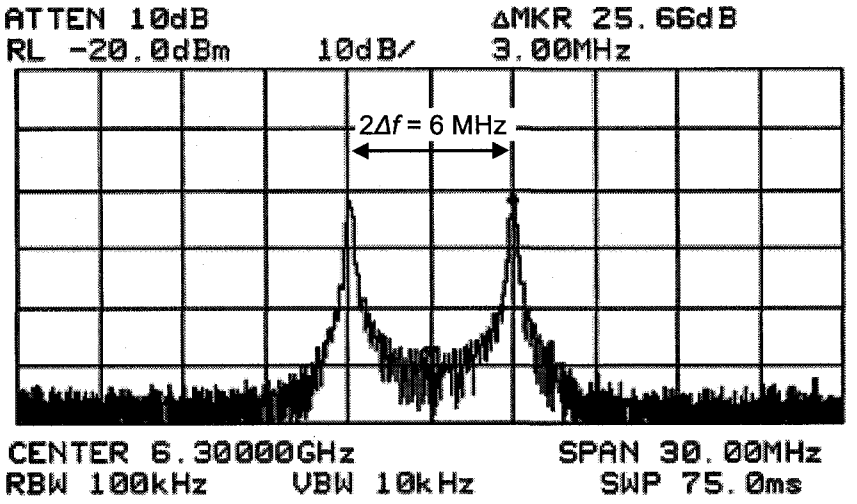

Figure 5-20: Measurement; TX FM modulated (BFSK) spectrum.

5.4.9. Antenna Impedance

A laser microsurgery procedure on a particular TX chip removed the VCO_{OUT} connection to the VCO_{OUT}/F_{VCO-} pad of Figure 5-1, enabling the characterization of the antenna's impedance by die probing through the F_{VCO-} and F_{VCO+} pads. Due to the unavailability of a calibration substrate for the 8-pin wedge probes, a 3-pin wedge probe with a G-S-G footprint is used – unfortunately, only a single-ended (SE) impedance measurement is possible with this setup. With a die area restriction of 2 mm^2 for the TX chip, the necessary de-embedding structures to the antenna's feed points could not be implemented. Consequently, an impedance measurement would include bond pad and interconnect parasitics which are not present in the HFSS antenna model of Subsection 3.2.1. To incorporate the

chip's bond pad structures in the antenna model would be exceptionally difficult because of the bond pad's composition of multiple metal layers. Nevertheless, an attempt is made to compare the antenna's single-ended net inductance and Q measurements with the corresponding simulation results of the HFSS model.

The single-ended inductance and Q of the simulated antenna model are plotted in Figure 5-21 and Figure 5-22, respectively, courtesy of Atif Shamim. These two figures also include single-ended inductance and Q measurements of the antenna, respectively. At the 6.3 GHz operating frequency, the discrepancy between the simulated and measured inductance is 0.5 nH, which can be attributed to extra narrow interconnects leading to the bond pads from the antenna's feeding paths. Also, the measured inductance appears to have a lower self-resonate frequency, which is probably a result of the bond pads' parasitic capacitance. In Figure 5-22, the Q measurements are in good agreement with the simulation results above 4 GHz. Below this frequency, however, HFSS predicts lower resistive losses for the antenna. This discrepancy is not a major concern, as the TX is operating in the 6-GHz band.

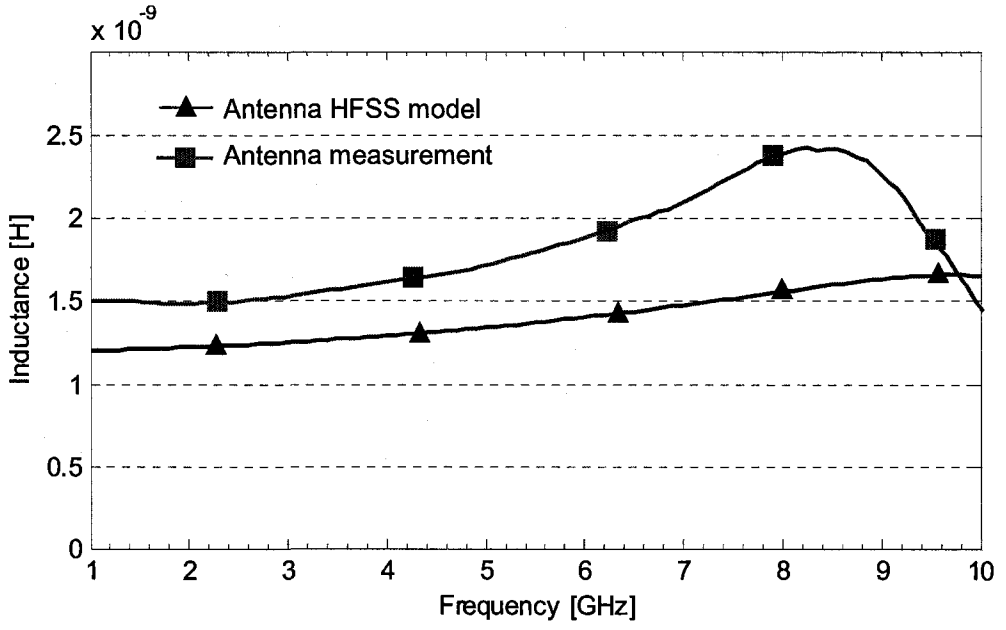

Figure 5-21: Inductance comparison (SE) of antenna model and measurement.

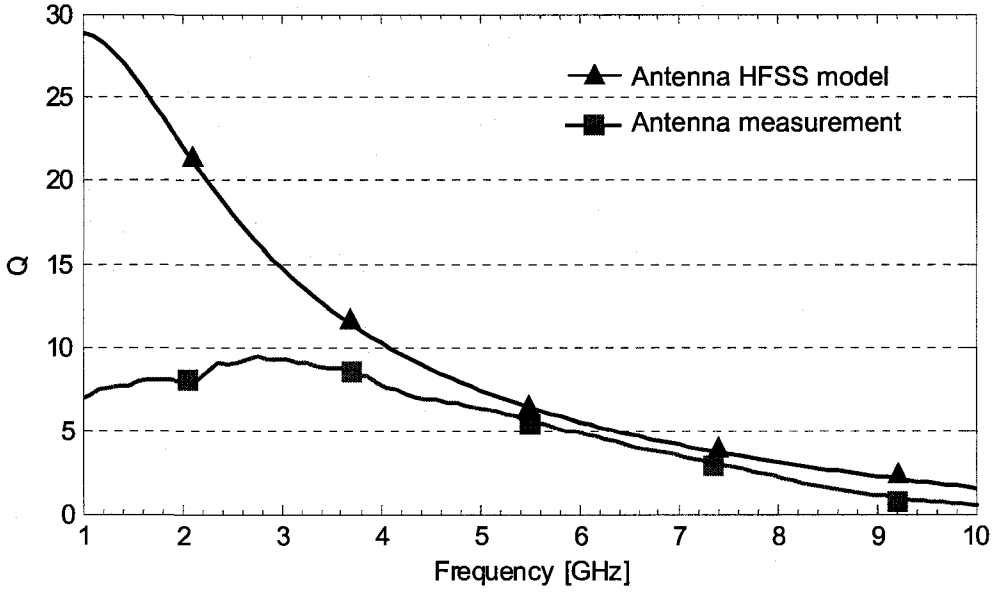

Figure 5-22: *Q* comparison (SE) of antenna model and measurement.

5.4.10. Antenna Radiation

The TX is mounted in an anechoic chamber, as shown in Figure 5-23, and measurements of the radiation pattern reveal a maximum gain of –22 dBi ($\theta = 45°$, $\varphi = 90°$) which is +45° above the predicted HFSS boresight gain in the plane of the loop. This change in the radiation pattern is attributed to interference of the PLL circuits (which are on one side of the integrated antenna) with the antenna's reactive near-field and to the unsymmetrical position of the antenna with respect to the edges of the TX's die. Acting as a receiver, a patch antenna with a gain of 6.7 dBi is connected to a spectrum analyzer and the received power at 6.4 GHz is recorded for different distances between the TX and RX (from 0.3 m to 1.5 m, in 0.3 m steps). The measurements are plotted in Figure 5-24 with the predicted received power using the Friis transmission equation of (2.31) to verify the validity of the setup. The power delivered to the antenna by the oscillator is determined to be slightly greater than 0 dBm.

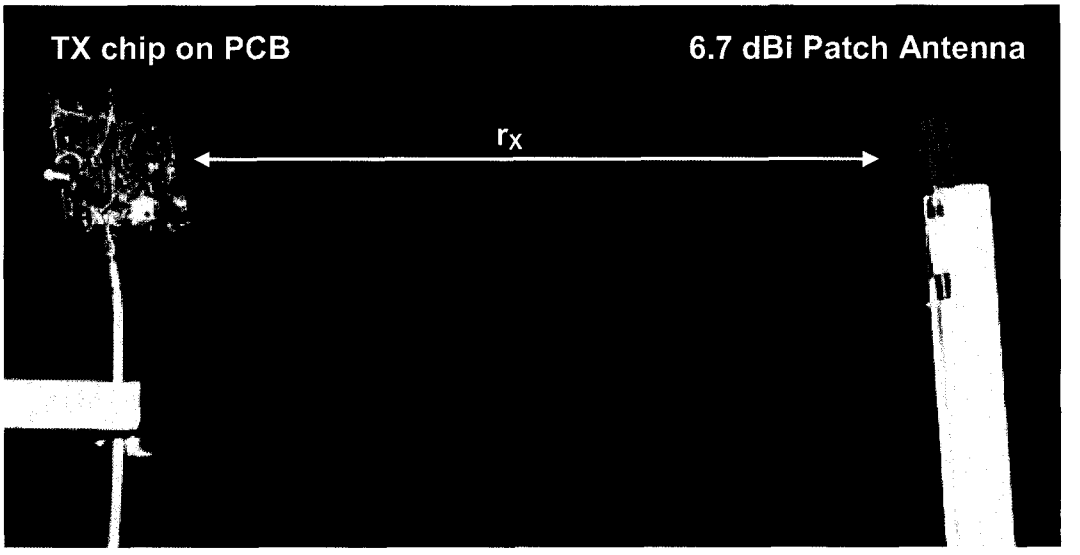

Figure 5-23: Anechoic chamber measurement test setup.

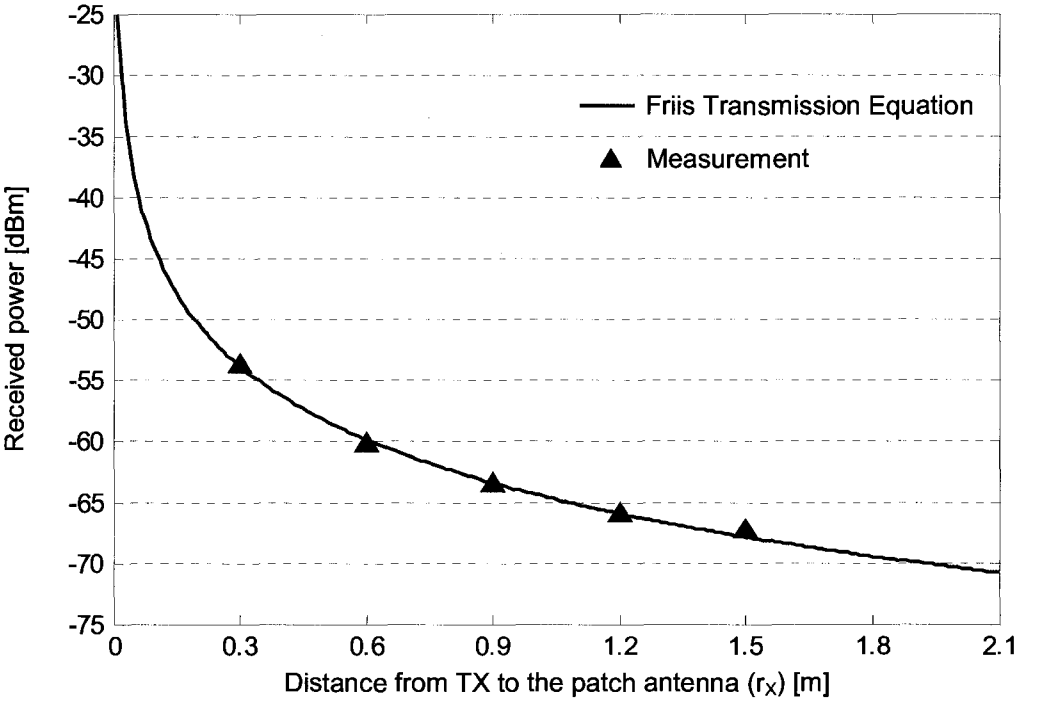

Figure 5-24: Measurement; received power from TX as a function of r_X.

Consider a typical FM receiver with a noise figure NF of 7 dB, requiring an E_{bit}/N_o of 13 dB for an acceptable BER of 10^{-5} [20]. From the receiver's carrier sensitivity of (2.32), this receiver, when connected to a 6.7 dBi patch antenna, could adequately process a –70 dBm BFSK signal (with a data rate of 300 kbps) from the TX while maintaining 30 dB of fade margin. From Figure 5-24, this would represent a communication range of 2 m, provided the antennas' polarizations are aligned.

5.4.11. Transceiver Front-End Communication

As a result of the change in the TX's operating band, from 5.2 GHz to 6.3 GHz, wireless communication with the actual RX chip is not possible. To test the transceiver's end-to-end link communication, and observe transmitter modulation to receiver demodulation capability, a wired test setup is devised. Figure 5-25 contains a photo of this test setup, where the TX VCO's FM modulated (BFSK) carrier signal is amplified and then down-converted to a frequency inside the injection-locking bandwidth of the RX's VCO. The amplified down-converted signal is differentially split into two to drive the inputs of the RX's LNA with enough signal strength to cause the RX's oscillator to be injection-locked. The RX's PLL components, as illustrated earlier in Figure 3-7, serve to demodulate the signal. A parts list for this wired test setup is provided in Table 13, as well as some general comments.

A screen capture of the spectrum analyzer observing the RX VCO's spectrum is shown in Figure 5-26. Here, the RX VCO's is being injection-locked by the FM modulated (BFSK) signal with a +/- 1 MHz frequency deviation. Figure 5-27 shows a screen capture of the oscilloscope comparing the demodulated output bitstream from the RX and the input bitstream to the TX. The noise on the output bitstream during a logic "1" is an artifact of the interface between the RX's PLL and output pad buffer. This noise, in the form of downward pulses, results from cycle slips at the PFD inputs which occur at the beat frequency between the reference signal and the divider output. With reference to Figure 3-7, the secondary CP integrates charge onto a small on-chip capacitor to demodu-

late the received bitstream. After the occurrence of a cycle slip, this CP might inadvertently remove enough charge, by leakage or other means, to cause the capacitor's voltage to cross the switching threshold of the pad buffer – resulting in an output change.

Table 19: Wired TX to RX test setup part list.

Part	Comments
TX	• f_{OSC} = 6.07953 GHz +/- 1 MHz • FM modulated (BFSK) with a 2 kbps bitsteam
Amplifier (MITEQ Model AFS4-020001800-60-20P-4)	• Gain 15 dB
Mixer (Nortel Model TB0440LW1)	• RF port at 6.07953 GHz • LO port 10 dBm at 10.77274 GHz • IF expected at 4.69321 GHz • Conversion loss 12 dBm
Balun (Picosecond Model 5315A)	• Insertion loss 8 dB
RX	• F_{REF} = 4.69321 GHz / 64 = 73.331 MHz

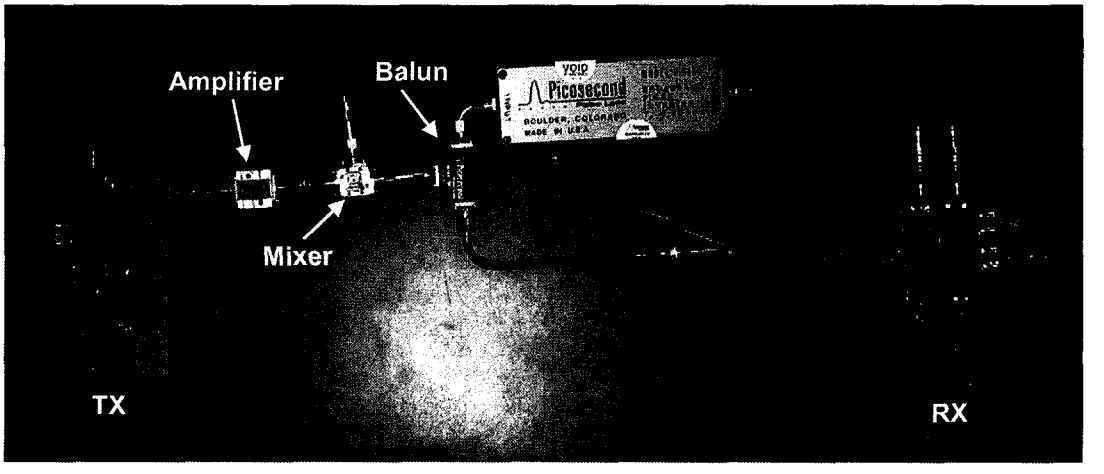

Figure 5-25: Wired TX to RX test setup.

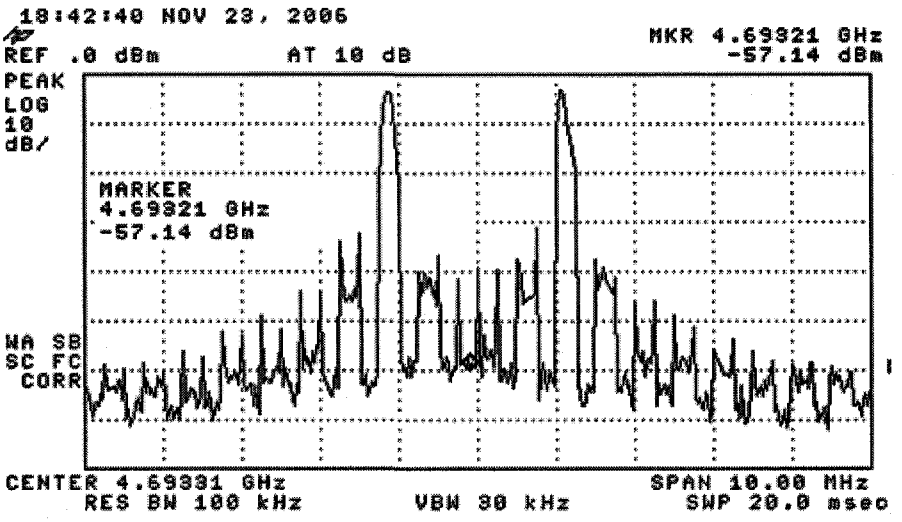

Figure 5-26: Measurement; RX VCO spectrum – injection-locked to the FM signal.

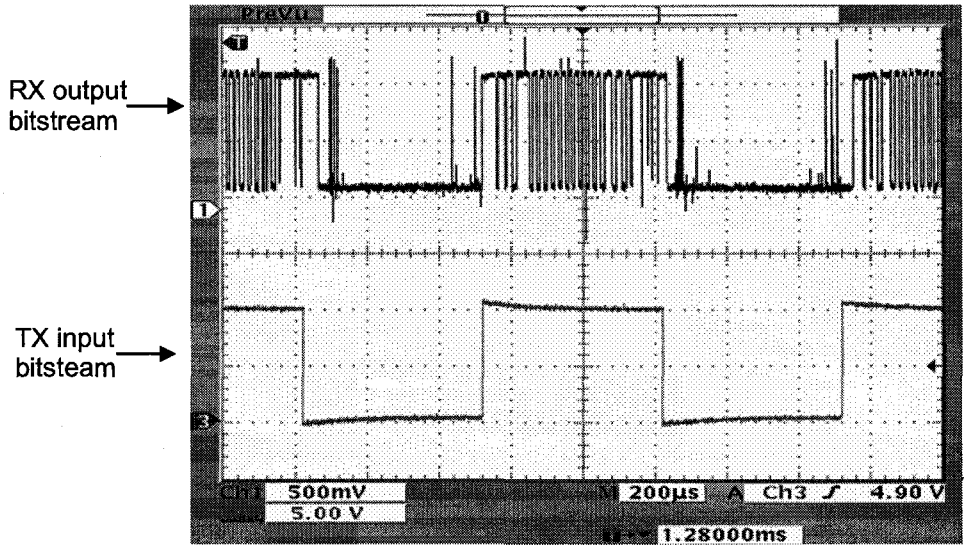

Figure 5-27: Measurement; TX input and RX output bitstreams at a rate of 2 kbps.

5.5. Performance

The simulation and measurement results of the TX are summarized in Table 20 and are generally in agreement. The discrepancy in the PLL's settling time is attributed to a de-

crease in the loop's bandwidth. The phase noise of the measured VCO is justifiably worse, attributable to a noisy DC power supply and to a decrease in the quality factor of the integrated antenna. A reduced Q_{ANT} would lead to an increase in VCO power consumption as seen in Table 21, which lists the TX's simulation and measured power consumption results for the closed-loop and open-loop operation modes. Here, the measured VCO power is 3.2 mW, 0.5 mW greater than expected. With reference to Subsection 4.2.5, Figure 4-12 contains a plot of the VCO's power consumption with respect to antenna Q and demonstrates that a $P_{VCO} = 3.2$ mW corresponds to a $Q_{ANT} = 8$. According to Figure 4-11, a 3 Ω increase in the antenna's HFSS series resistance would account for the apparent reduction in the antenna's Q after fabrication, since the antenna's inductance remained constant. With a Q_{ANT} of 8, the simulated phase noise of the VCO would be degraded by ≈ 6 dB.

From the design, yield optimization and manufacturing phases of an IC fabrication process, there are a number of factors to consider which could explain the antenna's increased series resistance from the HFSS antenna model. From the design phase, there is the unaccounted resistance of the metal interconnects from the VCO's active devices to the antenna's feed ports. The interconnect to each feed port is partly routed with a trace of metal M3 which is about 15 μm long and 1 μm wide. This is of significance as the sheet resistance of M3, 0.0639 Ω/sq, would yield a resistance of ≈ 0.75 Ω for the trace. A netlist extraction of the VCO layout for interconnect parasitics could have modelled this resistance. From the yield optimization phase, the impact of metal cheesing should be considered. Cheesing is a process in which slots of metal are removed from wide traces, which obviously increases the resistance of these traces. From the manufacturing phase, the effect of metal dishing from chemical mechanical planarization (CMP) of the wafer should be considered. Metal dishing reduces the thickness of a metal trace causing an increase in the trace's resistance.

Although the abovementioned factors could be modelled as an increase in the antenna's series resistance, the antenna's radiation efficiency would subsequently be re-

duced as it is reasonable to assume the antenna's loss resistance (R_{LOSS}) would increase relative to the radiation resistance (R_{RAD}). In the anechoic chamber measurements of Subsection 5.4.10, the antenna demonstrated a maximum gain of –22 dBi which is +45° above the predicted HFSS boresight gain. This gain measurement is a 13 dB increase relative to the HFSS simulation result of –35 dBi for that direction ($\theta = 45°$, $\varphi = 90°$). The cause of the increase, however, is attributed to the distortion of the antenna's radiation pattern, envisaged by simulation in Figure 3-2, and not to an improvement in radiation efficiency.

To account for the power consumed by sections of the PLL (such as the VCO buffers) which are not deactivated when the loop is opened, this is denoted by $P_{residual}$, the transmitter's average power consumption expression of (4.1) is modified to

$$P_{TX\_avg} \approx \frac{P_{PLL} \cdot T_{power-up} + (P_{residual} + P_{VCO}) \cdot T_{transmit}}{T_{packet}}. \tag{5.4}$$

From Table 21, the measured P_{TX_avg} is determined to be 21 μW if the power-up time is neglected and 22 μW if the power-up time is essentially comprised of the PLL's settling time. These calculations are based on the communication of a 1-kbit packet at a rate of 1 packet per second and transmitting at 300 kbps. Similarly, the expression for transmit efficiency is modified to

$$\eta_{TX} \approx \frac{P_{ANT}}{P_{residual} + P_{VCO}}. \tag{5.5}$$

With an antenna-delivered power of 0 dBm, the measured transmit efficiency is 16%. The average power and efficiency performance of the TX from measurement and simulation results are listed in Table 22. These performance metrics can both be improved by minimizing $P_{residual}$. For instance, the complete deactivation of all the divider's stages when the PLL is opened would save ≈ 1.25 mW, requiring the $Loop_{EN}$'s NAND gate to be placed at the divider's input and therefore operate at 6.3 GHz. With this placement, there is an increase risk of frequency pulling at the VCO when the $Loop_{EN}$ signal is switched, which is also the reason for not deactivating the two VCO buffers. If the TX is

to function as an oscillator transmitter, by powering-down the supply voltage VDD_{PLL}, a P_{TX_avg} of 11 µW and a η_{TX} of 31% are achievable.

Table 20: Measurement & Simulation; TX results summary.

Specification	Simulation result	Measurement result
Supply voltages	1.2 V and 0 V	1.2 V and 0 V
PLL frequency tuning range (K_{MOD} = 0.6 V)	6.13 GHz to 6.43 GHz	6.120 GHz to 6.585 GHz
VCO frequency tuning range (K_{MOD} = 0.6 V)	6.06 GHz to 6.47 GHz.	6.087 GHz to 6.596 GHz
Modulation range (K_{VCO} = 0.6 V)	–4 MHz to 4.4 MHz	–3.8 MHz to 5.2 MHz
K_{VCO}	340 MHz/V	420 MHz/V
K_{MOD}	7 MHz/V	7.5 MHz/V
VCO phase noise @ 1 MHz offset	–114 dBc/Hz	–97 dBc/Hz
PLL settling time	≈ 25 µs	≈ 65 µs
PLL loop bandwidth (ω_{3dB})	$2\pi \cdot 215$ kHz	$2\pi \cdot 150$ kHz
Positive carrier drift rate (27°C)	340 Hz/µs	220 Hz/µs
Negative carrier drift rate (27°C)	n/a	–240 Hz/µs
Maximum antenna gain	–31.7 dBi (θ = -90°, φ = 0°)	–22 dBi (θ = 45°, φ = 90°)

Table 21: Measurement & Simulation; TX power consumption.

Power Consumption	Simulation result	Measurement result
VDD_{VCO} (closed-loop)	2.7 mW	3.3 mW
VDD_{PLL} (closed-loop)	4.0 mW	4.0 mW
VDD_{VCO} (open-loop)	2.7 mW	3.2 mW
VDD_{PLL} (open-loop)	3.0 mW	3.2 mW

Table 22: Measurement & Simulation; TX performance.

Metric	Simulation result	Measurement result
P_{TX_avg}	19 µW	21 µW
η_{TX}	18%	16%
$\eta_{P\text{-}VCO}$	37%	31%

5.5.1. Re-comparison

From the short-range transmitters reviewed in Subsection 2.2.5, a performance comparison with the TX is illustrated in Figure 5-28 where TX_{PLL} and TX_{OSC} denote operation with and without a PLL, respectively. Although the oscillator transmitters of [34] and [39] demonstrate superior performance, neither design is implemented with an integrated

antenna nor is operated at a carrier frequency which would enable antenna integration to be economically feasible. All in all, the performance of the TX comparers favourably with other published transmitters.

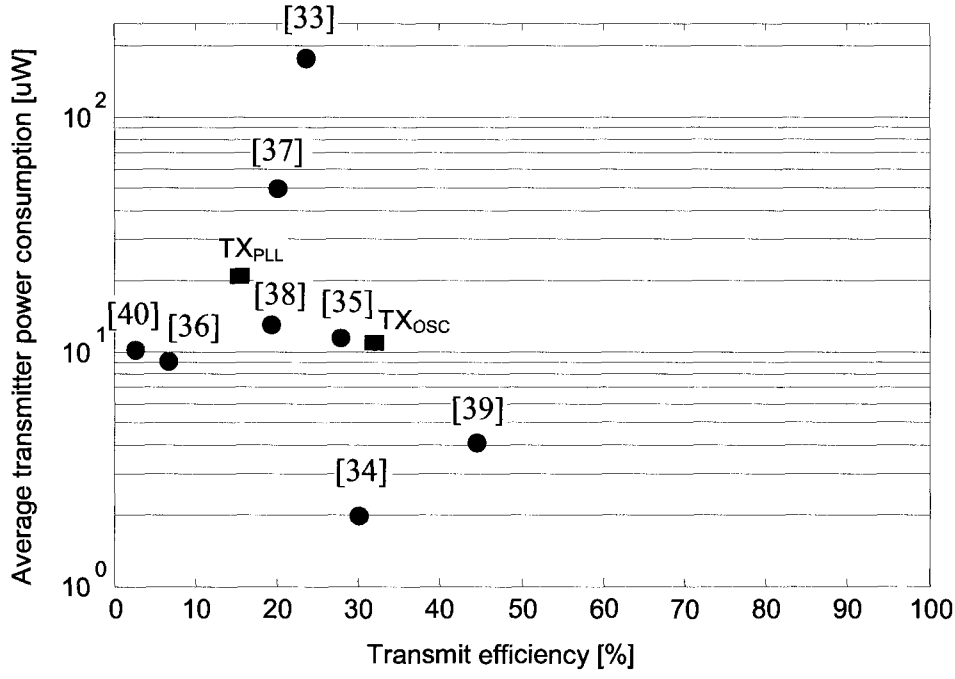

Figure 5-28: P_{TX_avg} and η_{TX} comparison of published short-range transmitters.

5.6. Discussion

The communication link between the TX and RX can be updated to include the measured integrated antenna gain of –22 dBi, a revised plot of the Friis transmission equation of (2.31) is shown in Figure 5-29. With the TX delivering a $P_{TX} = 0$ dBm, and the RX conjugately matched to the integrated antenna, a communication range of 60 cm can be supported. This distance can be increased to 4.1 m when the RX is conjugately matched to a 50 Ω patch antenna with a gain of 6.7 dBi. Both of these communication range estimates do not take into account a fade margin for the link.

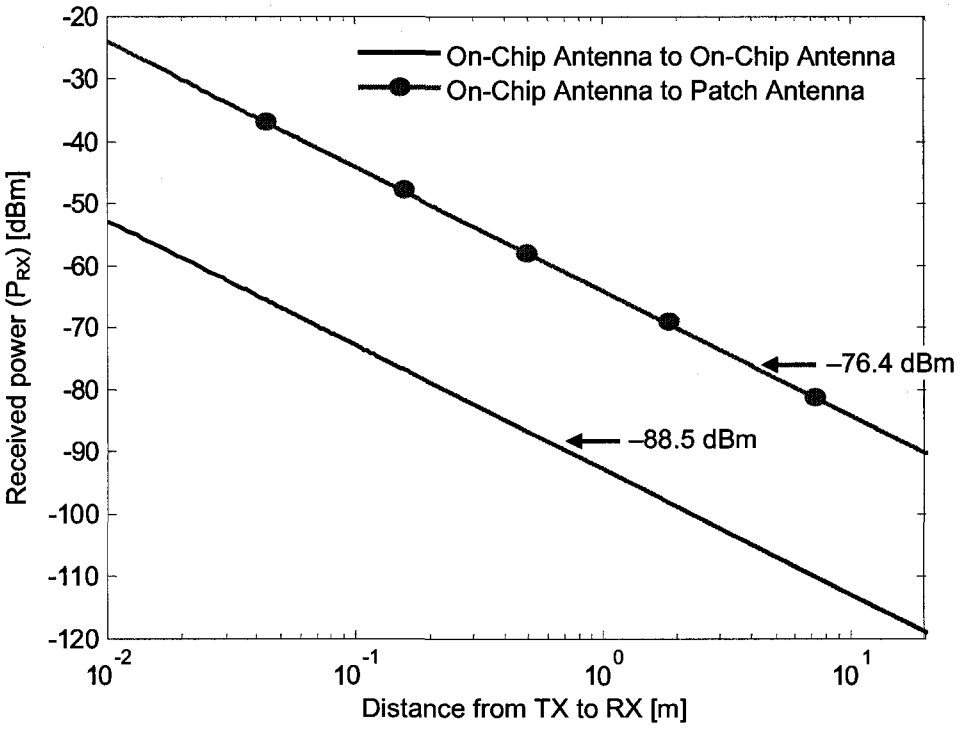

Figure 5-29: Communication range estimate (revised).

For the SoC solution, the size of the thin-film ultracapacitor to meet the power requirements of the transmitter can be determined with (2.44). As the transmitter requires 2.7 mA to transmit, a 1 kbit packet at a rate of 300 kbps would require 16 μF of capacitance if ΔV_{ultra} = 0.5 V. Therefore, a 16 mF ultracapacitor would store sufficient charge for 1000 packet transmissions while only occupying an area of 1.6 mm^2. This estimate neglects the power consumed by power management circuits, such as the ultracapacitor's voltage regulator. In between transmissions, for the length of the packet period, a thin-film solar cell is to trickle charge the ultracapacitors using the ambient light.

5.7. TX Prototype Summary

The TX prototype is revolutionary in that it makes use of an integrated antenna to communicate and is a low-power design which is able to be powered by a thin-film ultracapacitor for a completely integrated SoC.

The circuit blocks of the transmitter are assembled together to form the top-level schematic of the prototype chip. The circuit blocks of the modulator are modelled in AHDL for a system-level behavioural study. Then, a transistor-level simulation of the TX chip is performed. The simulated power consumption of each circuit block is noted for the closed-loop and open-loop operation modes of the TX. The leakage buffer effectively reduced carrier drift by a magnitude of 220 times, the simulated carrier drift rate is 340 Hz/μs. The simulated settling time for the PLL to acquire lock is ≈ 25 μs with an anticipated loop bandwidth of 215 kHz.

The layout of the TX chip occupies a die area of 2 mm^2. Three implementation techniques are applied to suppress on-chip noise, namely star-distribution, bypassing and triple-well (substrate-isolated n-FETs) usage.

The TX chip is mounted on a PCB to facilitate testing. The measured PLL loop bandwidth is ≈ 150 kHz. The observed settling time of the PLL is ≈ 65 μs, and is attributed to the loop bandwidth appearing 1.4 times smaller than designed. The measured phase noise of the carrier in open-loop mode is –97 dBc/Hz at 1 MHz offset. The measured CP's output voltage point at which there is a zero current mismatch is 0.6 V, and a current mismatch of ≈ 10% occurs when this voltage changes by 100 mV. When the leakage buffer is enabled, the measured frequency tuning range achieved by the PLL is from 6.120 GHz to 6.585 GHz. The measured modulation range (for frequency shifting) is from –3.8 MHz to 5.2 MHz about the centre frequency. The measured positive and negative spot drift rates are approximately 220 Hz/μs and –240 Hz/μs, respectively. The impact of frequency drift on the data rate for modulation is explored. Radiation pattern measurements revealed a maximum gain of –22 dBi which is +45° above the predicted HFSS boresight gain in the plane of the loop. Finally, the transceiver's end-to-end link communication is measured, and transmitter modulation to receiver demodulation capability is verified in a wired test setup.

The power and efficiency performance metrics of the TX are calculated from measurement results. The TX's average power consumption is 21 μW if the power-up

time is neglected. This is based on the transmission of a 1-kbit packet at a rate of 1 packet per second and a data rate of 300 kbps. The TX's transmit efficiency is 16%. These performance metric results compare favourably to those obtained from published state-of-the-art transmitter designs.

A wireless link between the TX and RX can support a communication range of 60 cm, when considering the measured gain of the integrated antenna. To meet the power requirements of the TX, a 16 mF ultracapacitor would store sufficient charge for 1000 packet transmissions while only occupying an area of 1.6 mm^2 on top of the chip.

CHAPTER

6. Conclusion

6.1. Thesis Summary

In this thesis, techniques for low-power CMOS transmitter system integration for short-range radio-frequency communication were presented. These techniques were applied to the design and implementation of an SoC transmitter. This transmitter is a low-power, energy-efficient, cost-effective and miniature-sized SoC solution for wireless dosimetry or thermometry, to name but two potential biomedical applications.

Chapter 2 explored fundamental antenna theory, to provide an understanding of this device as an instrument for radiating or receiving electromagnetic waves. A review of antenna structures, revealed the electrically small dimensions of the "small" loop antenna. The small-loop is economically feasible for integration in a submicron CMOS process at the 5.2 GHz UNII band (or any frequency band higher than 5.2 GHz). The fundamental aspects relating to low-power transmitter design were then described – namely communication link budgeting, receiver sensitivity, average power consumption, transmit efficiency, and relevant modulation schemes to short-range wireless sensor systems. A literature review revealed the superior performance of oscillator transmitters, and more specifically, with designs which have a low carrier frequency as propagation attenuation is proportional to the square of the carrier's frequency. However, for an SoC

transmitter solution, antenna integration in CMOS dictates operating with gigahertz carrier frequencies. The integration challenges associated with a mixed-signal design in a submicron CMOS process were discussed, as well as a limited research review of on-chip oscillator references. Finally, some fundamental considerations for the proposed hybrid power source, an ultracapacitor trickle charged by a solar cell, were explored.

Chapter 3 presented an overview of IBM's 0.13 μm CMOS technology, and then presented the merits for operating in the 5.2 GHz UNII band with an integrated small-loop antenna. A modelling oversight resulted in the antenna (and transmitter) operating at 6.3 GHz. The physical and electrical models for the integrated antenna were disclosed. A receiver design for the transmitter was briefly described and the communication specifications for anticipated wireless links were determined. A circuit, the oscillator transmitter, was then introduced which would satisfy these specifications and incorporates the integrated antenna to realize an SoC transceiver front-end. Finally, a system analysis of the communication link was explored.

Chapter 4 disclosed a PLL-based modulator which incorporates the oscillator transmitter circuit. The resulting architecture is a direct open-loop modulation transmitter, and its operation modes were briefly explained. Then, the design details of the transmitter's blocks from a schematic capture in Cadence's Virtuoso Analog Design Environment were presented, as well as circuitry realized to test parts of the modulator.

Chapter 5 focused on the transmitter prototype chip. Behavioural-level and transistor-level simulations of the transmitter were conducted and analyzed. Then, the methodology for implementing the transmitter chip in IBM's 0.13 μm CMOS technology was discussed, along with the layout details of the VCO and the open-loop modulator. The measurement results of the transmitter chip were presented. Then, important performance metrics were summarized. Finally, the communication link and the power supply requirements of the transmitter were assessed.

Finally, in this chapter, a list of thesis contributions, a list of publications from this research and a list of future work are provided.

6.2. Thesis Contributions

Several techniques are considered for low-power CMOS transmitter system integration for short-range RF communication. "On-chip" antenna integration is investigated for reducing the form-factor of the transmitter. Operating an integrated antenna at a relatively low carrier frequency, as compared to previously published integrated antenna designs, is a technique considered for reducing transmitter power consumption while minimizing propagation path-loss. Integrating the antenna as an inductive element in the resonant tank of an oscillator is a technique investigated to remove the need for a power amplifier and save power. Open-loop modulation of a PLL-based modulator is a technique explored to lower the transmitter's power consumption, during a data packet transmission, for an on-chip power source option – an ultracapacitor and solar cell combination. The application of the abovementioned techniques resulted in the following contributions:

1. The 6.3 GHz SoC transmitter design incorporating the integrated small-loop antenna. The transmitter is implemented in a 1.2 V 0.13 μm CMOS process and occupies an area of 2 mm^2. Making use of an integrated antenna to communicate, this transmitter chip is therefore revolutionary in that it is the first SoC and the smallest transmitter to operate at the 6-GHz frequency band. The transmitter features a PLL-based modulator design with closed-loop and open-loop operation modes to accurately define and FM modulate the carrier of an oscillator, respectively. Active power consumption of the modulator is reduced such that the transmitter can be powered by an on-chip ultracapacitor and solar cell combination for wireless dosimetry applications.
2. The measurement and evaluation of the SoC transmitter which achieves relatively good efficiency and low average power consumption when compared to other known published transmitters. This is accomplished in spite of the fact that the

SoC transmitter operates at a multi-gigahertz band and communicates with a lossy integrated antenna.

3. The complementary *LC* VCO design procedure for achieving optimum oscillator power efficiency performance with respect to the inductive antenna that is incorporated into the VCO's resonant tank. This procedure amends the "simultaneous *gm* and impedance matching" design technique of [55] to also attain "power optimization".

4. The demonstration of the feasibility of an integrated small-loop antenna which radiates sufficient far field energy at 6.3 GHz for short-range communication. The integrated antenna, designed from [9] and [10], is to the author's knowledge, the first small-loop antenna to be integrated without costly post-processing techniques in a mainstream CMOS process having a low-resistivity substrate. The integrated antenna, which occupies 0.6 mm^2 of chip space, is also believed to be the smallest reported active antenna operating in the 6-GHz band.

5. The communication link analysis of a short-range SoC transceiver architecture – comprised of an injection-locked receiver and an oscillator transmitter, which communicates over a 6.3 GHz carrier using FM modulation (BFSK) with an integrated antenna. The analysis highlights the dynamic relationship between the communication range, data rate, and receiver injection-locking bandwidth.

6.3. Publications Summary

The following paper contributions were submitted and successfully accepted for publication as a direct result of this thesis work:

[9] A. Shamim, P. Popplewell, V. Karam, L. Roy, J. Rogers and C. Plett, "5.2 GHz on-chip antenna/inductor for short range wireless communication applications," *IEEE Int. Workshop on Antenna Technology*, Mar. 2006, pp. 213-216.

[10] P. H. R. Popplewell, V. Karam, A. Shamim, J. Rogers, M. Cloutier, and C. Plett, "5.2 GHz self-powered lock and roll radio using VCO injection-locking and on-chip antennas," *IEEE Int. Symp. on Circuits and Systems*, May 2006, pp. 5203-5206.

[74] A. Shamim, P. Popplewell, V. Karam, L. Roy, J. Rogers, and C. Plett, "Silicon differential antenna/inductor for short range wireless communication applications," *IEEE Canadian Conf. on Electrical and Computer Engineering*, May 2006, pp. 94-97.

[75] P. Popplewell, V. Karam, A. Shamim, J. Rogers, C. Plett, "A 5.2 GHz BFSK receiver with on-chip antenna for self-powered RFID tags and medical sensors," *IEEE Radio Frequency Integrated Circuits Symp.*, June 2007, pp. 669-672.

[76] V. Karam, P. Popplewell, A. Shamim, J. Rogers, C. Plett, "A 6.3 GHz BFSK transmitter with on-chip antenna for self-powered medical sensor applications," *IEEE Radio Frequency Integrated Circuits Symp.*, June 2007, pp. 101-104.

[77] P. Popplewell, V. Karam, A. Shamim, J. Rogers, C. Plett, "An injection-locked 5.2 GHz SoC transceiver with on-chip antenna for self-powered RFID and medical sensor applications," *VLSI Circuits Symp.*, June 2007, pp. 88-89.

[78] A. Shamim, M. Arsalan, V. Karam, M. Usama and L. Roy, "5.2 GHz VCO transmitter with on-chip antenna for biomedical sensor applications," presentation at *International Union of Radio Science Conf.*, July, 2007.

[79] P.H.R. Popplewell, V. Karam, A. Shamim, J. Rogers, L. Roy, and C. Plett, "A 5.2-GHz, BFSK transceiver using injection-locking and on-chip antennas," *J. of Solid State Circuits*, vol. 43, no. 4, pp. 981-990, Apr. 2008.

[80] A. Shamim, V. Karam, P. Popplewell, L. Roy, J. Rogers, and C. Plett, "A CMOS Active Antenna/Inductor for System on a Chip (SoC) Applications" *Symp. on An-*

tennas and Propagation and USNC/URSI National Radio Science Meeting, to be published in July 2008.

6.4. Future Work

Areas for future research opportunities include:

- The unsymmetrical position of the antenna with respect to the edges of the transmitter's die, and the possible interference of the PLL circuits (which are on one side of the integrated antenna) with the antenna's reactive near-field, are leading theories based on HFSS post-analysis simulations to explain the small-loop antenna's distorted radiation pattern. This interoperability problem should be researched further and guidelines should be established for the next small-loop antenna implementation in CMOS. This may lead to a more elegant integrated antenna solution, such as having all the transmitter circuitry inside the loop. With any antenna design, a proper characterisation of the antenna's impedance from de-embedding structures should be done.

- On the advancement of antenna integration, the suitability of other antenna structures should be explored and then assessed with circuit integration. Here, the operating frequency is expected to be a determining factor. Also, integrated antenna implementation should be demonstrated with other CMOS technologies, specifically a high resistivity (> 1000 Ω·cm) silicon-on-insulator (SOI) process. Mixed-signal (RF and digital) integration is limited by severe substrate coupling in low resistivity bulk CMOS. A high resistivity process would reduce crosstalk and lower substrate losses, enabling the integration of high quality on-chip inductors (or loop antennas). As a higher resistivity substrate will lead to higher latch-up susceptibility in bulk CMOS, an SOI process should therefore be exploited for its latch-up immunity [81].

- An adequately-sized ultracapacitor with a solar cell should be manufactured on top of the transmitter chip, but not covering the antenna section, to demonstrate the feasibil-

ity of power source integration for SoC solutions. This would also require the design and implementation of power management circuits, such as a voltage regulator to maintain the necessary voltage supply for the transmitter.

- A controller circuit for the transmitter should be designed, with a lock detection, which could be programmed to close and open the loop at pre-programmed intervals or when necessary to re-lock the carrier when its drift is significant enough to affect the performance of the communication link. Techniques to reduce carrier drift should also be explored by minimizing or compensating for the leakage of charge from the loop filter.
- For the development of a completely-integrated SoC transceiver, the back-end circuit blocks of Figure 1-3 should be designed and implemented – namely the A/D, CPU & controller, and clock generator. Together with the transceiver front-end, these circuits should be integrated with a MOSFET dosimeter for a wireless dosimeter solution.

7. Appendix A

In this appendix, schematics and layout plots are presented. The first schematic is that of the top-level TX chip.

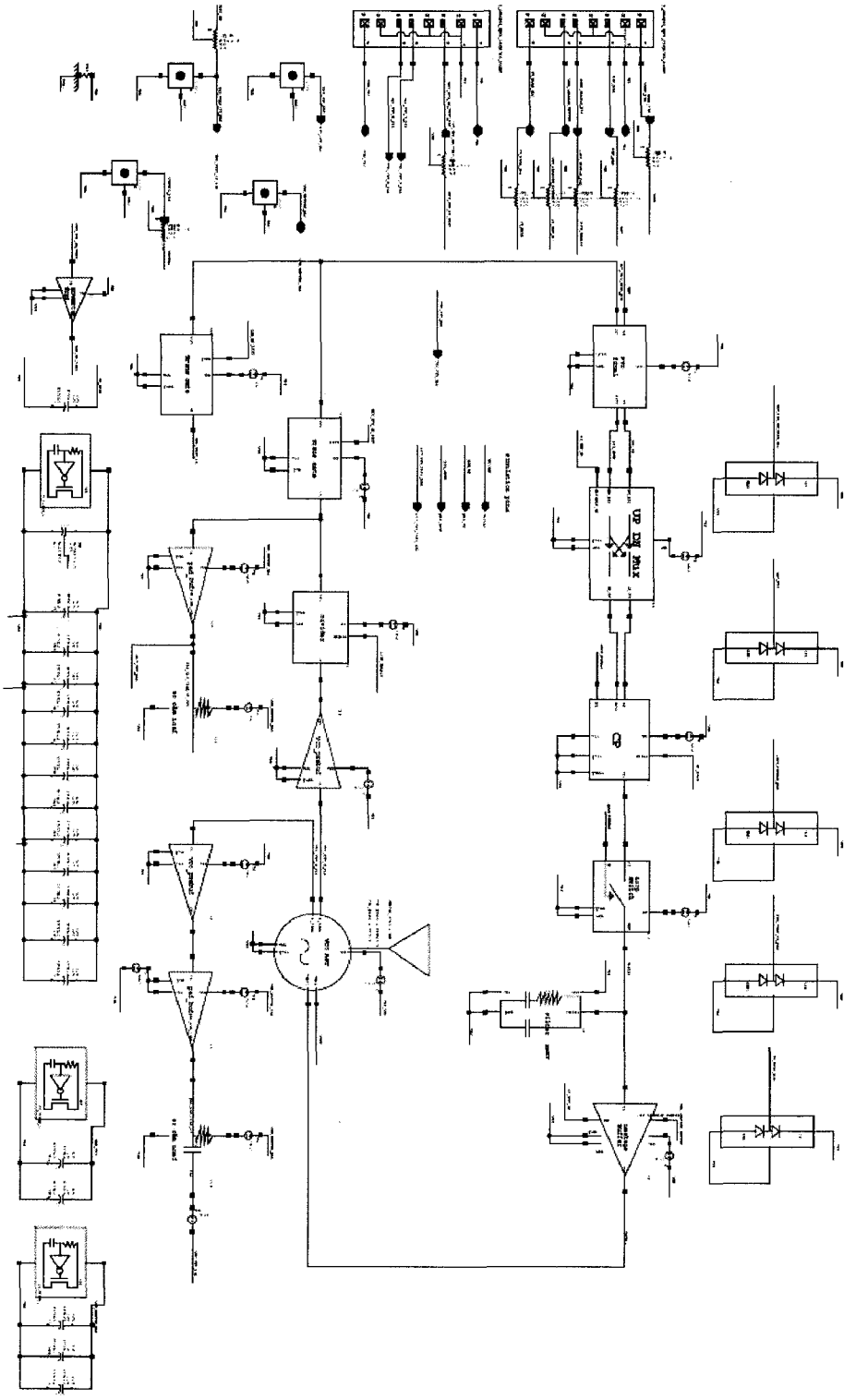

Figure A.1: Top-level TX schematic.

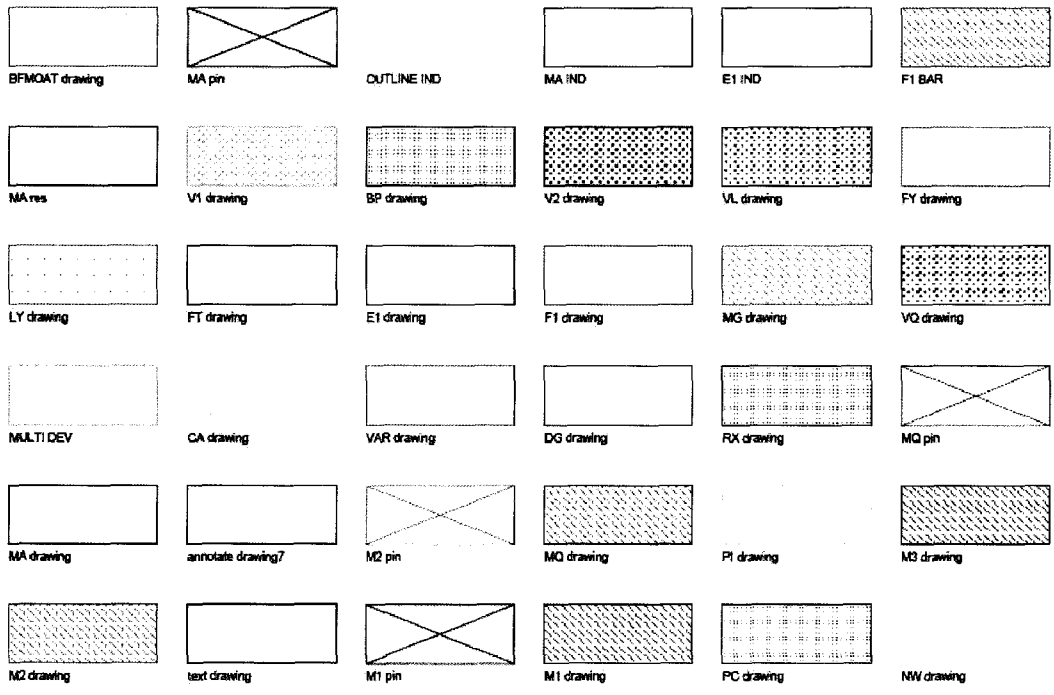

Figure A.2: Layout legend – subset; layer and purpose.

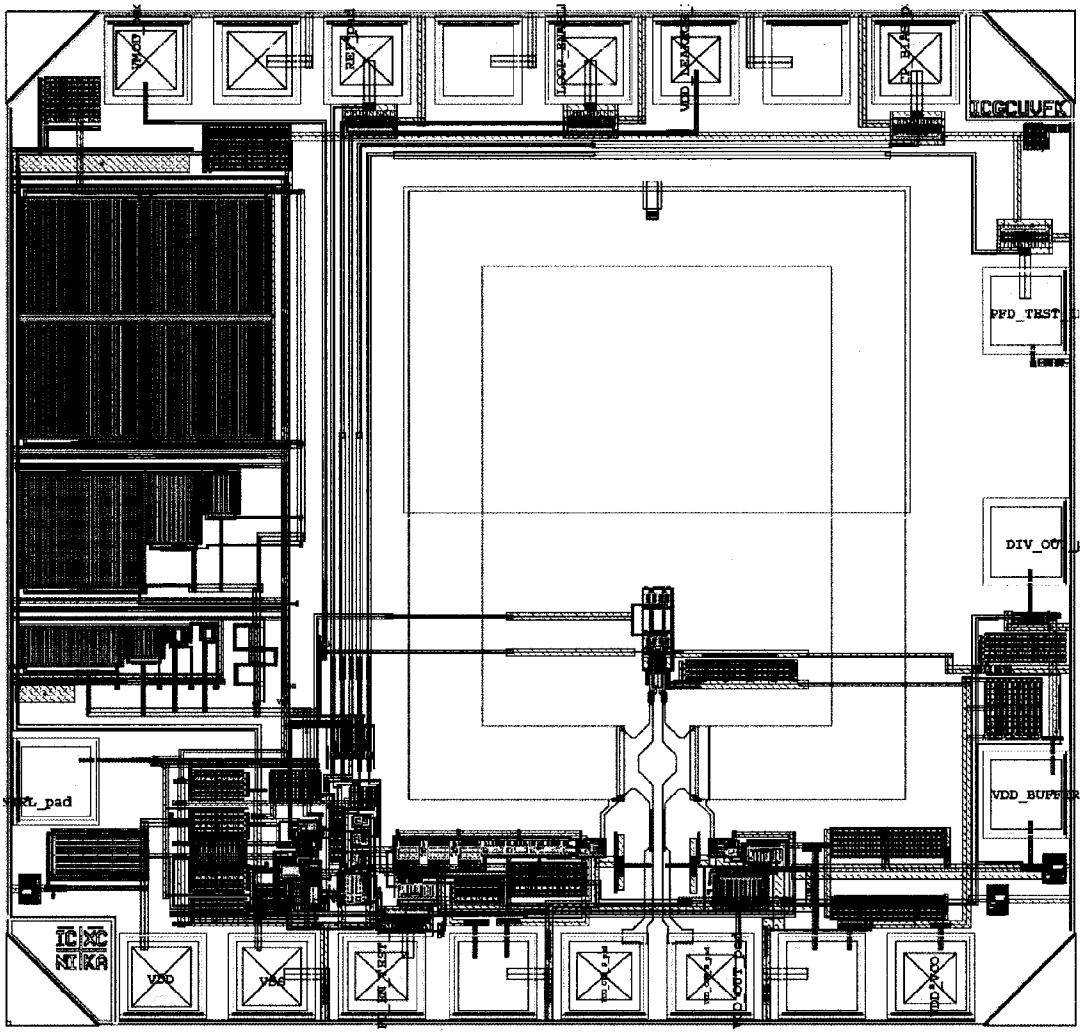

Figure A.3: TX chip layout (without metal-fill).

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