DOUBLE-GATE-LINE COPLANAR WAVEGUIDE
DISTRIBUTED AMPLIFIER

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ABSTRACT

Broadband power amplifiers are key components in lightwave communication systems. Obtaining a combination of high power, ultra-broadband and high power-added-efficiency (PAE) requires improved microwave circuit design techniques.

To obtain efficient broadband amplification for potential use in optical modulator driver applications, a double-gate-line coplanar waveguide (CPW) distributed amplifier was designed and implemented using 0.2 μm pHEMT technology and 4x15- μm device periphery.

The proposed amplifier consists of two 5-stage conventional distributed amplifiers with common-source gain cells.

To get a high output power, the two distributed amplifiers are put in parallel and share a common drain line so that their currents are added. This topology has the advantage of effectively doubling the device periphery without doubling the gate capacitance. Thus the gate attenuation and device size are kept small.

The realized circuit had a total chip area of 0.9x3.2 mm², an average power gain of 7.3 dB, a 3-dB bandwidth of 45 MHz - 41 GHz, and a maximum PAE of 18%. DC power dissipation of 0.288W with an output voltage swing of 2.5Vp-p at midband was obtained.

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Chapter 1: Introduction

1.1 Motivation

With the development of high-speed optical systems capable of operating at 40 Gb/s and above, the demand for microwave-monolithic-integrated-circuit (MMIC) wide-band external modulator drivers has been continually increasing over the last decade. These drivers are required to have high power levels, high operating frequency, high efficiency, high linearity and high output voltages. Unfortunately, existing modulators tend to have poor efficiency and low output voltages.

Optical transmitter systems operating at 40 Gb/s and above typically consist of a multiplexer, a driver, a laser diode and an electro-absorption (EA) modulator (Figure 1-1).

Figure 1-1: Fiber optic transmitter with external modulator

In typical 40-Gbit/s optical transmitters, the modulator-drivers for electroabsorption (EA) or Mach-Zehnder modulators are required to operate at both high-speed and high drive voltages (2.3 V_{peak-to-peak} or higher) [1]. Such drive voltages are required to ensure a sufficient extinction ratio at 40 Gb/s [8] and are characteristic of a power amplifier.

As will be seen in chapters three and five, many recent works in the field have been done to produce such drivers [2,3,5,6,7]. In particular, two MMIC distributed amplifiers have been designed using the Phillips OMMIC 0.2 μm transistors [43]. The first one employed a cascode configuration and the second one is a matrix configuration. Both configurations yield good performance comparable to other designs using a similar technology reported in the literature but better efficiency, smaller DC dissipation and larger output voltage swings would be desired.

Since reactively-matched microwave power amplifier configurations do not provide high output voltage swings and high efficiencies over multi-octave bandwidths, there is still great interest in investigating new amplifier topologies in order to obtain similar or better performance.

1.2 Objective

The objective of this thesis is to investigate novel broadband MMIC amplifiers capable of producing large output voltages and having power-added-efficiencies comparable to or exceeding currently available modulator drivers.

More specifically, the objectives of this thesis are as follows:

- a) To investigate a new driver amplifier configuration. The configuration is a double-gate-line distributed amplifier, using common-source pHEMTs and the coplanar-waveguide technology.
- b) To identify the power-limiting factors of other distributed amplifiers; and to predict and optimize the performance-improving mechanisms of this new driver amplifier with the aid of theoretical and CAD tool analysis.
- c) To fabricate and experimentally verify the performance of this new driver amplifier and to compare it with conventional distributed amplifiers.

1.3 Thesis organization

The thesis is divided into eight chapters. Chapter 2 surveys the fundamental principles of power amplifier design and lays out the constraints in designing power amplifiers. These constraints are related to the class of operation, load-line, and bandwidth. Chapter 3 presents different circuits used in RF and microwave power amplifier design and the typical characteristics of these circuits concerning bandwidth and efficiency. Chapter 4 outlines the basics of coplanar waveguide structures and the foundry process characteristics. Chapter 5 describes the theories of the conventional distributed amplifier design and presents a survey of common distributed amplifier topologies and the power-limiting mechanisms of the conventional distributed amplifier. Chapter 6 discusses the design of the double-gate-line CPW distributed amplifiers. Chapter 7 presents the experimental results of the fabricated double-gate-line CPW distributed amplifier. Chapter 8 concludes the thesis, citing the achievements and suggestions for future work.

Chapter 2: Constraints in power amplifier design

Designing high power amplifiers requires consideration of many constraints which are often trade-offs between different desired performance characteristics. High power MMIC amplifiers usually operate over a narrow bandwidth. As the bandwidth increases the amplifier output power decreases for a given device technology. Achieving both high power and large bandwidth requires overcoming fundamental constraints associated with both the circuit architectures and device technology. This chapter will discuss general constraints related to designing a basic power amplifier cell. These constraints are: amplifier's class of operation, load impedance, and bandwidth. More specific constraints related to broadband amplifiers will be discussed in chapter three.

2.1 Constraint related to the class of operation

Generally, only class-A and class-AB push-pull configuration are used in linear broadband power amplifiers. Typically the classes are defined based on the biasing point, the load seen by the device, and the conduction angle.

2.1.1 Class-A

A class-A amplifier is usually chosen to achieve minimum distortion. One of the inherent constraints of class-A amplifier is its relative low efficiency. Class-A is usually used in the first stage of an amplifier chain where power level is low, thus not much power is actually wasted.

Figure 2-1 shows a basic amplifier. The figure does not show the input and output matching networks. With class-A amplifiers the bias is made at a point where the device is always on, which is at the mid-point between the peak-to-peak output current and the mid-point between the peak-to-peak output voltage.

Figure 2-1: Basic amplifier configuration

At low frequency operation, class-A amplifiers' load line has a slope that is the inverse of the optimum load resistance. When the load-line varies between the maximum allowed drain to source voltage (knee voltage V_k to break down voltage V_{br}) and at the same time varies between the minimum and maximum drain current ($I_d=0$ to I_{dss}), one obtains the maximum power from the device (Figure 2-2).

Figure 2-2: Different load lines for class-A operation

To obtain the maximum power, the optimum load resistance R_{opt} should be:

$$R_{opt} = \frac{(V_{br} - V_k)}{I_{dss}} \quad (2.1)$$

The maximum output power can be formulated as:

$$P_{out_{max}} \leq \frac{(V_{br} - V_k)I_{dss}}{8} = \frac{(V_{br} - V_k)^2}{8R_{opt}} \quad (2.2)$$

Since the maximum output power varies linearly to the inverse of the load, we have:

$$\begin{aligned} 1) \text{ For } R > R_{opt}: P_{out} &= \frac{(V_{br} - V_k)^2}{8R} = P_{out_{max}} \frac{R_{opt}}{R} < P_{out_{max}} \\ 2) \text{ For } R < R_{opt}: P_{out} &= \frac{I_{dss}^2 R}{8} = P_{out_{max}} \frac{R}{R_{opt}} < P_{out_{max}} \end{aligned} \quad (2.3)$$

The drain voltage V_{ds} and drain current I_d waveforms of class-A amplifiers are shown in Figure 2-3.

Figure 2-3: Bias and load line of a class-A amplifier

For class-A amplifiers, the maximum drain efficiency (ratio of the output RF power to the DC power) is theoretically 50%. This maximum is greatly reduced if matching network losses, transmission line losses, and other losses are taken into account. Despite its low efficiency, class-A amplifiers provide high linearity and wide bandwidth.

2.1.2 Class-B and Class-AB

In class-AB amplifiers the device is biased close to pinch-off and in class-B, at pinch-off. Thus the device is conducting for half the cycle and turned off for the other half of the cycle. The drain is biased at about half the peak-to-peak RF output voltage swing. The drain voltage V_{ds} and drain current I_d waveforms are shown in Figure 2-4.

The optimum load resistance of class-B amplifiers is half of the one for class-A.

Since the device is only conducting on half of the cycle, DC consumption diminishes and maximum power efficiency can theoretically increase up to 78.5% [69].

Figure 2-4: Class-B load line and bias point

2.1.3 Push-pull

Devices operating in push-pull have two devices biased alternatively for half-cycle in class-B, each provides half of the combined output currents. Relatively wideband output signal can be obtained with this configuration but it is necessary to have broadband transformers.

Since each device provides $I_{dss}/2$ current at the output, the total peak-to-peak current is I_{dss} and hence the output power is similar to class-A amplifiers.

For microwave frequency applications, 180° hybrid couplers (baluns) are used to create 180° out of phase equal amplitude input voltage for the devices.

As with class-B, push-pull class-B allows a theoretical maximum efficiency as high as 78.5% [69]. Unfortunately, MMIC baluns with acceptable performances for bandwidth greater than 20 GHz are difficult to implement.

Figure 2-5: Optimum load-line of a push-pull amplifier.

2.1.4 Class-C amplifiers

In class-C amplifiers, the device is biased well into the cut-off region. The device conduction angle is less than 180° [69].

Unfortunately, as with class-B cases, the required filter circuit at the output of class-C amplifiers in order to obtain the fundamental power limits the bandwidth.

For broadband amplifiers, only class-A and push-pull class-B or AB are suitable. In fact, to the best of my knowledge, almost all ultra-wideband amplifiers reported in the literature are distributed amplifiers and operate either in class-A or push-pull class-B. In this thesis, class-A

will be employed since amplifiers operating in class-A provide the highest gain [67] and the most linear output power.

2.2 Constraint on the load resistance

The second constraint is related to the load resistance. It limits the range of load resistance that can be used in broadband amplifiers. For single-device amplifiers operating in class-A, the load resistance is given by [67]:

$$R_{opt} = \frac{(V_{br} - V_k)^2}{8P_{out,max}} \quad (2.4)$$

To improve output power, it is thus required to have a high break down voltage or a lower load resistance.

Lowering the load resistance (R_{opt}) can be done by increasing I_{dss} , that is by increasing the device periphery. But that implies the use of a larger impedance transformation network at the output to transform the load resistance to the standard Z_0 (50 Ω). The problem is that it is difficult to realize broadband impedance transformation networks without a major loss and a reduction of bandwidth.

In this thesis, we choose to adopt the 50- Ω input and output impedance system but as future works, co-design of modulators integrated with the driver could allow Z_0 to be smaller.

In fact, no monolithic impedance-transformation network for bandwidths greater than 30 GHz has been reported in literature. Such broadband transformers would be fabricated off-wafer and occupy very large chip area, as it will consist of multiple sections of quarter-wave lines at the center frequency. Such transformers are unavoidably lossy. Therefore, any power gained resulting from a smaller R_{opt} would be lost in the transformers. As a result, hardly any improvement in the output power is realized without a low loss transformer.

2.3 Constraint on bandwidth

The third constraint is a consequence of increasing the device periphery. When the device periphery is large, the input capacitance increases.

For FET devices, the transistor input capacitance (C_{gs}) is given by:

$$C_{gs} = \frac{g_m}{2\pi f_T} \quad (2.5)$$

where g_m is the device intrinsic large signal transconductance and is proportional to the gate width.

If g_m is increased, C_{gs} also increases, which implies a reduction of the maximum operating frequency. Note that the maximum operating frequency is determined by the low-pass filter response between the source-generator and the device input. To reduce the input capacitance, one could use capacitive degeneration by inserting a series capacitance at the gate. However, capacitive degeneration would reduce the gain because it reduces the drive level.

2.4 Implications in designing a basic power amplifier cell

Some design rules can now be made to take into account, to a certain extent, the above-mentioned constraints while designing a power amplifier cell.

First, the device should operate in class-A mode for maximum linearity. Secondly, the input and output impedance should be as close to 50 Ω as possible since the efficiency of broadband transformers deteriorates quickly as the difference in impedances increases. Thirdly, the device technology employed should have the highest possible $f_T \cdot V_{br}$ product. However this choice often depends on the availability and accessibility of such process.

These implications form the basic guidelines in designing a cell in power amplifiers. Other constraints specific to this thesis are discussed in the following chapters.

Chapter 3: Microwave broadband power amplifiers

This chapter considers in detail different conventional broadband microwave power amplifier topologies in the literature and summarizes their performance in terms of bandwidth, output power and efficiency. These topologies are common-source amplifier, amplifier with a reactively matching input network, amplifier with a lossy matching network or with a bridge-tee matching network, shunt feed-back amplifier, and distributed amplifier. But first, this chapter will define some basic concepts often encountered in discussions regarding the amplifier performance. These concepts are the short-circuit current gain, the maximum-available-gain, the unity current gain cut-off frequency f_T , the power gain cut-off frequency f_{max} and the power-added-efficiency.

3.1 Basic concepts

Short circuit current gain is defined as the current gain of the device when the output is short-circuited and the input is driven using a current source.

Figure 3-1: Simplified pi-model for a FET

A simplified A.C. model for the transistor is used in the following analysis (Figure 3-1).

The short circuit current gain is given by:

$$H_{21} = \frac{I_{out}}{I_{in}} = \frac{g_m}{j2\pi f C_{gs}} \equiv \frac{f_T}{j \cdot f} \quad (3.1)$$

where $f_T = g_m / 2\pi C_{gs}$ is the unity-current-gain-cut-off-frequency.

The low-noise OMMIC PHEMT transistor used in this thesis will have a f_T of about 60 GHz.

The unity-current-gain-cut-off-frequency (f_T) is the frequency at which the current gain becomes unity. The power-gain-cut-off frequency f_{max} is the frequency at which the maximum-available-gain becomes unity [10] and is defined as:

$$f_{max} = f_T \frac{1}{2\sqrt{R_i/R_{ds}}} \approx \frac{g_m}{4\pi C_{gs}} \sqrt{\frac{R_{ds}}{R_i}} \quad (3.2)$$

f_T and f_{max} are both independent of the device periphery (W), whereas other transistor parameters are scaled with respect to the device periphery (W), that is: I_{dss} , C_{gs} and g_m are all proportional to W ; whereas R_i and R_{ds} are both proportional to $1/W$.

The power gain obtained when both the input and output are conjugate matched to the source and load impedance respectively is called the Maximum Available Gain (MAG). MAG is given by:

$$MAG = \frac{P_{load}}{P_{av,src}} = \frac{g_m^2 R_{ds}}{16\pi^2 f^2 C_{gs}^2 R_i} \quad (3.3)$$

Power Added Efficiency (PAE%) is defined as the ratio of the R.F. output-input power difference, to the total D.C. power provided by all bias supplies:

$$PAE(\%) = \frac{P_{out} - P_{in}}{P_{dc}} 100\% = \frac{P_{out}}{P_{dc}} \left(1 - \frac{1}{G}\right) 100\% \quad (3.4)$$

Here P_{in} is the RF input power, P_{out} is the RF output power, P_{dc} is the total DC power from all sources and G is the power gain.

It is noted that a high input drive (and a low power gain) would lead to a low PAE, thus the higher the power gain, the higher PAE.

3.2 Common source amplifier

For class-A common source power amplifiers, the optimum load resistance is [67]:

$$Z_o = (V_{br} - V_k) / I_{dss} \quad (3.5)$$

For the purpose of this analysis, the following assumptions are made: FET width and I_{dss} chosen according to equation (3.5); load resistance equals Z_o and $R_i \ll Z_o$. Using the simplified pi-model for the FET, a common source amplifier has a fixed mid-band voltage gain of:

$$S_{21} = g_m * Z_o, \quad (3.6)$$

and a bandwidth of

$$f_{3dB} = \frac{1}{2\pi (Z_o + R_i) C_{gs}} \quad (3.7)$$

where we have assumed that $Z_g = Z_o$.

The gain-bandwidth product would then be:

$$S_{21} \cdot f_{3dB} = \frac{g_m Z_o}{2\pi (Z_o + R_i) C_{gs}} \approx \frac{g_m}{2\pi C_{gs}} = f_T \quad (3.8)$$

Thus the gain-bandwidth product for a common source amplifier under the conditions stated is limited by f_T .

The gain or bandwidth can be adjusted by adding a series capacitance at the gate or a shunt resistor at the source; such technique is also called capacitive or resistive degeneration [11]. Capacitive and resistive degenerations do not affect the gain-bandwidth product.

Figure 3-2: Transistor with capacitive degeneration.

In the case of capacitive degeneration (Figure 3-2), the gate resistance (R_i) remains unchanged and the extrinsic transconductance is:

$$G_m = \frac{g_m C_{deg\ en}}{C_{deg\ en} + C_{gs}} \quad (3.9)$$

The net input capacitance is:

$$C_{in} = \frac{C_{deg\ en} * C_{gs}}{C_{deg\ en} + C_{gs}} \quad (3.10)$$

From equation (3.6), the mid-band gain and the 3-dB bandwidth are respectively:

$$S_{21} = \frac{g_m C_{deg\ en} Z_o}{C_{deg\ en} + C_{gs}} \quad (3.11)$$

$$f_{3db} = \frac{1}{2\pi (Z_o + R_i) C_{in}} \quad (3.12)$$

Capacitive degeneration reduces the input capacitance, allowing the selection of a larger device without increasing C_{gs} . However it also reduces the gain.

Figure 3-3: Resistive degeneration

In the case of resistive degeneration (Figure 3-3), the gate resistance (R_i) also remains the same; the extrinsic transconductance is:

$$G_m = \frac{g_m}{1 + g_m R_s} \quad (3.13)$$

The net input capacitance is:

$$C_{in} = \frac{C_{gs}}{1 + g_m R_s} \quad (3.14)$$

Therefore the mid-band gain and the 3 dB bandwidth are respectively:

$$S_{21} = \frac{g_m Z_o}{1 + g_m R_s} \quad (3.15)$$

$$f_{3dB} = \frac{1 + g_m R_s}{2\pi(Z_o + R_i)C_{gs}} \quad (3.16)$$

Both techniques of degeneration improve bandwidth at the cost of gain. Hence the gain-bandwidth product is still limited by f_T .

3.3 Amplifier with lossy matching network

In addition to capacitive and resistive degeneration, a power amplifier's bandwidth can also be improved by using a lossy input matching network [12, 13]. This network consists of a shunt inductor and a shunt resistor between the gate of the FET and the broadband impedance transformer, as shown in Figure 3-4.

The shunt inductance (L) resonates with C_{gs} at the center frequency f_o . The shunt conductance G_i as well as the broadband impedance transformer provide the input match to Z_o .

For design frequencies $f_o \ll 1/(2\pi R_i C_{gs})$, Z_{in} is given by,

$$Z_{in} = \frac{1}{G_i + G_l} \quad (3.17)$$

where $G_l = 4\pi^2 f_o^2 C_{gs}^2 R_i$

The amplifier bandwidth can be improved by decreasing Z_{in} since:

$$f_{3dB} = \frac{1}{\pi C_{gs} Z_{in}} \quad (3.18)$$

The gain is given by:

$$S_{21} = \frac{g_m Z_o}{2\pi f_o * C_{gs} \sqrt{Z_o * Z_{in}}} \quad (3.19)$$

Therefore, as G_i is increased, the amplifier bandwidth is increased, but with a gain reduction. Also the gain bandwidth product depends on f_o , which was not the case with the common source amplifier.

Figure 3-4: Common source amplifier with a lossy matching network

3.4 Amplifier with bridge-tee matching network

Conventional power amplifiers can use a bridge-tee matching network to slightly broaden the bandwidth [14, 15], as shown in Figure 3-5. This network consists of a lossy all-pass filter. The required inductances and capacitances for designing an optimal bridge-tee input matching are the following:

$$L1 = (Z0 - R_i) Z0 C_{gs} / 2 \quad (3.20)$$

$$L2 = (Z0 + R_i) Z0 C_{gs} / 2$$

$$C_l = \frac{C_{gs}}{4} \left(1 - \frac{R_i^2}{Z0^2} \right) \quad (3.21)$$

Bridge-tee amplifiers have similar gain bandwidth product as with the common source amplifiers.

Figure 3-5: Common source amplifier with Bridge-Tee lossy matching network

3.5 Amplifier with shunt feedback matching network

Typical power amplifiers' bandwidth can also be improved by using a shunt feedback loop [16, 17], as shown in Figure 3-6.

Figure 3-6: Shunt feed-back loop

The optimal matching is obtained by having a feed-back resistance of:

$$R_f = Z_0 (1 - A_v). \quad (3.22)$$

where A_v is the mid-band voltage gain and is given by:

$$A_v = 1 - g_m * Z_0 \approx (V_{br} - V_k) / V_p \quad (3.23)$$

This amplifier has the same gain and bandwidth as the common source amplifier (section 3.2). However, shunt feed-back amplifiers yield a higher efficiency and provide good output reflection coefficients.

3.6 Distributed amplifier

All the techniques mentioned above use a frequency selective impedance matching network. These techniques slightly improve the bandwidth of a power amplifier. Ultra broadband amplifiers mostly use a different configuration called distributed amplifiers [11, 18, 19, 20, 37, 38, 40, 46]. Distributed amplifiers, as shown in Figure 3-7, are also called traveling-wave amplifiers (TWA). They provide high bandwidth by absorbing the transistor capacitances into an artificial transmission line.

Figure 3-7: Schematic of a conventional distributed amplifier.

Here R_{og} and R_{od} are the dummy terminal gain and drain load respectively; L_g and L_d are the gate and drain line inductance; C_p is the shunt drain capacitance.

The transistors are connected in parallel separated by inductors or microstrip lines. The gate and drain capacitors combined with their separating inductors or microstrip lines form what is essentially a lumped-element artificial transmission line. The line connecting the gates is referred to as *gate line* and likewise, the line connecting the drains is referred to as *drain line*. The input signal (V_{in}) enters at one end of the gate line, then propagates down the gate artificial transmission line. Some of the input power enters each FET; the rest is absorbed at the other end by the gate termination impedance whose value is equal to the equivalent line impedance. On the drain line, the output signal from the individual FET travels in both directions; the signal traveling to the left is absorbed at the end of the drain line by the drain termination impedance and that to the right travels toward the output port. To have maximum output signal, constructive phasing of the output signals requires the propagation constants of the gate and drain line be equalized. The input artificial line adds delays between each transistor. A similar artificial output (drain) transmission line compensates for these delays, resulting in an in-phase addition of the AC currents from the individual transistors in the drain line. In HEMTs since the drain-source capacitance (C_{ds}) is much smaller than the gate-source capacitance (C_{gs}), compensating shunt capacitances should be added on the drain line to equalize the phase delay.

Chapter 3: Microwave broadband power amplifiers

The gain-bandwidth product of a distributed amplifier is limited by $f_{\max}$ and can be shown [10] to be:

$$A_o * f_{1dB} \approx 0.8 f_{\max} \quad (3.24)$$

where

$$f_{\max} = \frac{f_T}{2 \sqrt{\frac{R_i}{R_{ds}}}} \quad (3.25)$$

$$\text{and } f_T = \frac{g_m}{2\pi C_{gs}} \quad (3.26)$$

This means the gain-bandwidth product of the lumped conventional amplifier is limited by the transistor unity current gain cut-off frequency f_T , whereas the gain-bandwidth product of the distributed amplifier is limited by the unity maximum available power gain cut-off frequency $f_{\max}$. Chapter 5 will present in more details the design equations for the distributed amplifier.

Chapter 4: Coplanar waveguide and foundry process characteristics

The first section of this chapter discusses the propagation medium used for implementing the design, which is the coplanar waveguide (CPW) line. Closed-form formulas for computing the characteristic impedances, effective dielectric constants, and losses for CPW are given for reference. The second section of this chapter presents the characteristics of the foundry process, including HEMT, substrate, resistors, capacitors, and inductors.

4.1 Coplanar waveguide

The coplanar waveguide (CPW) has several advantages compared to microstrip such as elimination of via holes for grounding, reduction of cross talk between lines, lower substrate thickness sensitivity, lower dispersion and radiation loss [61]. CPW is chosen here because of the need to reduce parasitic inductances in the grounding of the HEMT source terminals.

Figure 4-1 shows cross sections of a conventional and a conductor-backed CPW. Closed-form expressions for the effective dielectric constant and characteristic impedance of these transmission lines assuming negligible strip thickness have been derived [21, 22].

Equations 4.1-4.7 are used in this work to obtain a preliminary CPW dimensions for the various lines employed. A more refined analysis is performed subsequently with an EM CAD tool (Momentum). Equations 4.1 and 4.2 give the expressions for the effective dielectric constant and characteristic impedance, respectively, of CPW.

Figure 4-1: Coplanar Waveguides: a) Conventional, b) Conductor-backed

$$\epsilon_{eff} = 1 + \frac{(\epsilon_r - 1)}{2} \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')} \quad (4.1)$$

and

$$Z_o = \frac{30\pi}{\sqrt{\epsilon_{eff}}} \frac{K(k')}{K(k)} \quad (4.2)$$

where

$$k = \frac{a}{b} \quad (4.3)$$

$$k' = \sqrt{1 - k^2} \quad (4.4)$$

$$k_1 = \frac{\sinh(\pi a / 2h)}{\sinh(\pi b / 2h)} \quad (4.5)$$

$$k_1' = \sqrt{1 - k_1^2} \quad (4.6)$$

$K(k)$ and $K(k')$ represent the complete elliptic integral of the first kind and its complement. The $K(k)/K(k')$ ratio can be obtained approximately by [23]:

$$\text{For } 0 \leq k \leq 0.707: \frac{K(k)}{K(k')} = \frac{\pi}{\ln \left(2 \frac{1+\sqrt{k'}}{1-\sqrt{k'}} \right)} \quad (4.7)$$

$$\text{For } 0.707 \leq k \leq 1: \frac{K(k)}{K(k')} = \frac{1}{\pi} \ln \left(2 \frac{1+\sqrt{k}}{1-\sqrt{k}} \right)$$

When taking into account the thickness t of the central strip and of the ground planes, the width of the strip effectively increase and the gaps effectively decrease. The effective dielectric constant and characteristic impedance can be found, taking these effects into account, using the following formulae [24]:

$$\epsilon_{eff}(t) = \epsilon_{eff} - \frac{0.7(\epsilon_{eff} - 1) \frac{t}{b-a}}{\frac{K(k)}{K(k')} + 0.7 \frac{t}{b-a}} \quad (4.8)$$

and

$$Z_o = \frac{30\pi}{\sqrt{\epsilon_{eff}(t)}} \frac{K(k_e')}{K(k_e)} \quad (4.9)$$

where

$$\begin{aligned} k_e &= \frac{S_e}{S_e + 2W_e} \\ k_e' &= \sqrt{1 - k_e^2} \\ S_e &= 2a + \Delta \\ W_e &= b - a - \Delta \\ \Delta &= \frac{1.25t}{\pi} \left[1 + \ln \left(\frac{8\pi a}{t} \right) \right] \end{aligned} \quad (4.10)$$

For a given type of substrate, the characteristic impedance Z_o is controlled by the width and the spacing. From equation (4.2), it is clear that a high Z_o may be realized by having a small width and (or) a large spacing. However, the width can not be too small since it is

limited by the current capacity, fabrication tolerance, and conductor loss. Meanwhile the spacing can not be too large to avoid spurious mode and increased chip size.

4.2 Material and process characteristics

GaAs pHEMT distributed amplifier ICs were fabricated using the Phillips OMMIC process. This is a low-noise 0.2 μm gate length pHEMT process which has both enhancement and depletion mode pHEMTs with multi layer gold interconnect on a multi-layer dielectric substrate. Both nichrome resistors and metal-insulator-metal (MIM) capacitors are available.

The substrate has the following specifications: a resistivity of at least 107 $\Omega\cdot\text{cm}$; a diameter of $76.2\pm 0.2\text{mm}$ (3 inches); and a thickness of $620\pm 20\mu\text{m}$.

Although no library of elements exists for this process in a commercial microwave CAD tool, the designer has access to a separate Java script containing the necessary design equations for the OMMIC resistor and capacitor elements.

The process has 2 metal layers. The top layer is called IN and is used for microstrip lines. The second under-pass layer is called BE and is used for air-bridges and capacitors.

4.3 Resistors

Two types of resistors are available, thin-film (Nichrome) and implant (GaAs) resistors. The thin-film resistor is for very small resistance value and is not employed in this work. The GaAs resistor model parameters are:

- Length L in μm is the distance between the two ohmic-contact (OH mask) edges.
- The Width W in μm is the width of the active layer (LI mask).

Figure 4-2: Resistor dimensions

Since the resistive layer is very thin, no skin effect has to be taken into account for the calculation of the resistance. The resistor values and the limit current and voltage are calculated from L and W in μm as follows.

$$\begin{aligned} R(\Omega) &= \frac{300 + 195 * L}{W - 1.0} \\ I_{\max}(mA) &= \frac{V_{lin}}{R} \approx 0.38 * W \\ V_{\max}(V) &\approx 0.075 * L \end{aligned} \quad (4.11)$$

Since GaAs exhibits a field-dependent electron mobility, these maximum current and voltage considerations are to avoid current saturation.

W and L (μm) can be calculated based on the resistance value (Ω) and the saturation current (mA), as follow:

$$\begin{aligned} W_{\min} &\approx 2.6 * I_{\max} \\ L &= \frac{R * (W - 1.0) - 300}{195} \end{aligned} \quad (4.12)$$

W and L (μm) can be calculated as well based on the resistance (Ω) and the saturation voltage (V):

$$\begin{aligned} L_{\min} &= 13 * V_{lin} \\ W &= 1.0 + \frac{300 + 195 * L}{R} \end{aligned} \quad (4.13)$$

When designing the distributed amplifier circuit, it is important to take into account these expressions so that resistors may be made as small as possible but still operate as linear elements.

The parasitic ground capacitance of a resistor may be taken into account using the equivalent circuit shown below where C_p is the total ground capacitance (including the edge effect) of a metallic pattern of same dimensions as the resistor pattern. However these capacitances are only significant for thinner substrates ($100 \mu\text{m}$) than the ones employed here

(600 μm). They are of the same order of magnitude as capacitive parasitic couplings occurring in the circuit (typically smaller than 0.2 or 0.3 pF).

Figure 4-3: Resistor model.

4.4 Capacitors

Two types of capacitors are available: Silicon-Nitride (SiN) and Silicon-Nitride+Silicon dioxide capacitors. The latter is for very small capacitance value and is not employed in this work.

The SiN MIM capacitor model parameters are the area (S) in μm^2 and the perimeter (P) in μm , both defined by the TE mask layer (hashed area in Figure 4-4).

Figure 4-4: Capacitor dimensions.

The capacitance value can be calculated from its lay-out dimensions as follows:

$$C = 392 * 10^{-6} * S + 0.5 * 10^{-3} * P \quad (4.14)$$

where C is in pF, S in μm^2 , $P=2 \times (W1+W2)$ in μm .

4.5 PHEMT devices

The wider (W) the gate finger, the higher the gate resistance ($R_g = R_{g0} \times W$), resulting in a decrease of the maximum available gain, and an increase of the noise. Using several fingers in parallel will alleviate this drawback, as $R_g = R_{g0} \times W / (N_{bd})^2$, where N_{bd} is the number of gate fingers.

The number of gate fingers should be even to have a source pad on each side of the FET. When more than 2 fingers are used, the source pads should be interconnected.

Table 4.1 shows the main pHEMT DC characteristics.

Table 4.1: Main pHEMT DC characteristics.

<i>Name</i>	<i>Definition</i>	<i>Unit</i>	<i>Scaling</i>	<i>Value</i>
<i>V_t</i>	<i>Threshold Voltage</i>	<i>V</i>	-	-0.9
<i>I_{dss}</i>	<i>Drain Source current</i>	<i>mA/mm</i>	$\times W$	250
<i>V_{brgss}</i>	<i>Effective Drain+Source to Gate voltage (Drain and Source short circuited) before breakdown</i>	<i>V</i>	-	-8.0
<i>V_{leak}</i>	<i>Maximum Drain+Source to Gate voltage (Drain and Source short circuited) without gate current leakage</i>	<i>V</i>	-	-4.6
<i>g_m</i>	<i>DC transconductance</i>	<i>mS/mm</i>	$\times W$	440

Figure 4-5 shows an OMMIC 4-finger FET. Using a P-HEMT with more than 6 gate fingers causes the center sources of the P-HEMT not correctly grounded and a phase shift between the gate fingers.

Figure 4-5: A OMMIC 4-finger FET.

4.6 Summary of process characteristics

The main features of this process are summarized below:

- There is no backside metal. The substrate thickness is 620 μm .
- Pseudomorphic (GaInAs) active layer.
- Depletion and enhancement mode recessed transistors: $V_t=0.225\text{V}$ or -0.9V .
- 2 types of diodes (0.18 μm "GM" and 3 μm "BE") for mixing, level shifting, or varactors.
- Resistors, using the GaAs active layer.
- Resistors, using a thin film metal layer (NiCr).
- 2 types of MIM capacitors, using the Si₃N₄ layer and the Si₃N₄ + SiO₂ layer.
- SiO₂/Si₃N₄ + air bridge isolation between layers to reduce the parasitic capacitances.

- 1.25 μm thick gold metallisation for interconnections and spiral inductors.

The multi-substrate is based on GaAs, GaAlAs and GaInAs and is obtained by metal-oxide-vapor-phase-epitaxy (MOVPE). The average particle and defect level is less than $10/\text{cm}^2$ for defect sizes over $0.15\mu\text{m}^2$.

The MIM capacitor bottom electrode and diodes are formed by mask BE which has the total metal thickness of 650nm. All ground planes and microstrip lines are formed using the interconnection metal (IN) of 1.25 μm thickness. Figure 4-6 illustrates the process layer profile for the microstrip version. The actual CPW process employed in this work has a thicker substrate and no via nor ground back-plane.

Figure 4-6: Layer profile

Chapter 5: Conventional distributed power amplifier

In chapter 3 we have overviewed several techniques to improve bandwidth in power amplifiers. In particular, we have seen that distributed amplifiers [11, 18, 19, 20] can provide ultra broad bandwidth. It was noted that conventional distributed amplifiers can provide gain–bandwidth products up to the power-gain cutoff frequency, f_{max} [19, 20]. In contrast, chapter 3 had established that common source amplifiers have gain–bandwidth products limited by the transistor current-gain cut-off frequency, f_T . Despite this advantage, conventional distributed amplifiers have lower output voltage and lower gain, consequently poorer efficiency.

In this chapter, we will discuss in more details the performance of distributed amplifiers. The first two section of this chapter will present the fundamentals of distributed amplification and the design equations for the conventional distributed amplifier. The next section discusses the power-limiting mechanisms of the conventional distributed amplifier and presents modifications to overcome those mechanisms. In the last section, various distributed amplifier topologies published in the literature are overviewed.

5.1 Fundamentals of distributed amplification

Distributed amplification principles have been applied to a wide range of circuits, such as oscillator [26, 27], traveling wave tubes [28], photodetectors [29], paraphase amplifiers [30, 31], phase-shifters [32], and most commonly traveling wave amplifiers [11,18,19,20].

The rationale of distributed amplification is based on distribution of active devices in such a way to superimpose the output signals from different devices in a concurrent way so that the gain can be added while maintaining a very large bandwidth.

Figure 5-1: Lumped conventional distributed amplifier

Figure 5-1 shows the schematic of a typical conventional distributed amplifier.

One of the most important concepts in distributed amplification is the artificial transmission line structure. The artificial transmission line structures can be formed by well known *constant-k sections* using transistor intrinsic capacitance and inductors or microstrip lines. The image impedances in an arbitrary two-port network, as shown in Figure 5-2, are defined as [33]

Z_{i1} : Input impedance at port 1 when port 2 is terminated with Z_{i2} .

Z_{i2} : Input impedance at port 2 when port 1 is terminated with Z_{i1} .

Figure 5-2: Two-port network

When the network is specified by its ABCD parameters, the image impedances are:

$$Z_{i1} = \sqrt{\frac{AB}{CD}} \quad Z_{i2} = \sqrt{\frac{BD}{AC}} \quad (5.1)$$

where, by symmetry, $A=D$.

The propagation constant, γ , of the network is given by:

$$\gamma = \cosh^{-1} \sqrt{AD} \quad (5.2)$$

where $\gamma = \alpha + j\beta$.

Figure 5-3 shows the T and π form of the low-pass constant-k section. A constant-k section can also be formed by cascading two L-sections, as shown in Figure 5-3C. The image impedance of the π -form is given by:

$$Z_{i\pi} = \frac{\sqrt{\frac{L}{C}}}{\sqrt{1 - \frac{\omega^2}{\omega_c^2}}} \quad (5.3)$$

Figure 5-3: Lumped artificial transmission line sections.

The corresponding propagation constant is:

$$\gamma = \text{acosh} \left(1 - \frac{\omega^2}{\omega_c^2} \right) \quad (5.4)$$

where $\omega_c = \frac{2}{\sqrt{LC}}$.

ω_c denotes the line cut-off frequency where the image impedances change from real to imaginary.

The magnitude of the normalized image impedance $Z_{i\pi}$ is plotted in Figure 5-4. At low frequencies the characteristic impedance is equal to $\sqrt{L/C}$ or Z_0 .

Figure 5-4: Normalized image impedance of the π -section versus normalized frequency.

Within the pass band ($0 < f < f_c$), the T or π -section's attenuation α and phase delay β are respectively:

$$\alpha = 0 \text{ and } \beta = 2 \operatorname{asin}(f/f_c).$$

Within the stop band ($f_c < f < \infty$), the T or π -section's attenuation and phase delay are respectively:

$$\alpha = 2 \operatorname{acosh}(f/f_c) \text{ and } \beta = \pi.$$

Attenuation and phase delay constants are plotted in Figure 5-5. The propagation constant changes from purely imaginary to purely complex at $\omega/\omega_c=1$. Hence, below ω_c , the T or π section displays no attenuation but only a phase shift; whereas at frequencies above ω_c , it displays a 180 degrees phase-shift and a high attenuation.

Figure 5-5: Attenuation (α) and phase (β) constants of an L-section versus normalized frequency.

It is essential when implementing a distributed amplifier to provide a proper termination to the image impedance of the constant-k filter section. As shown previously, the constant-k section image impedances equal Z_0 only at frequencies below cut-off.

Therefore, to match the constant-k section image impedances to Z_0 , an m-derived half circuit is inserted between the constant-k section and the resistive termination, as shown in Figure 5-6.

Figure 5-6: M-derived matching circuit.

The impedance of the m-derived half circuit looking from the left matches the image impedance of constant-k section. The impedances of the m-derived half circuit looking from the right are illustrated in Figure 5-7 with constant $m=0.6, 0.5$ and 0.4 .

Figure 5-7: Image impedance of the m -derived matching network for $m=0.6$, 0.5 and 0.4 .

The impedance of the m -derived half circuit looking from the right is given by [65]:

$$Z_{i_{\pi, m\text{-derived}}} = \frac{Z_0(1 - x^2(1 - m^2))}{\sqrt{1 - x^2}} \quad (5.5)$$

where $x = \omega/\omega_c$ and $Z_0 = \sqrt{L/C}$.

As depicted in Figure 5-7, the m -derived section impedance matches to Z_0 for frequencies almost up to cut-off when $m=0.6$.

As a result of the peaking effect of the m -derived section at frequencies near cut-off, the gain rises sharply at cut-off. An optimization technique can eliminate this problem. This technique called staggering was first introduced by Sarma [34]. This technique involves making the cutoff frequency of the gate line higher than that of the drain line so that the gain starts to decline before the frequency where the peaking effect appears. However, reducing the gain peak also reduces the cut-off frequency.

In theory the ideal distributed amplifier has an infinite gain-bandwidth product. In practice, it is limited by the number of devices that can be used. This number is in turn limited by the attenuation present in the gate and drain lines of the amplifier. In the presence of attenuation, the gate signal decays as it propagates down the line. Thus beyond a certain point the added devices are not driven sufficiently to overcome the losses in the drain line. For this reason, there will be a point at which the losses incurred from the extra section in the gate and

drain lines prevails over the added gain. There exist an optimum number of devices which will maximize the gain given by [10]

$$N_{opt} = \frac{\ln(\alpha_d / \alpha_g)}{\alpha_d - \alpha_g} \quad (5.6)$$

where α_g and α_d are the attenuations per section on the gate and drain line.

An upper bound for the total number of sections is given by [65]:

$$N \leq \frac{2}{R_{gs}\omega^2 C_{gs} Z_{od}} \quad (5.7)$$

where G is the power gain, g_m is the small-signal transconductance of the gain stage. The gain depends directly on the line impedances $Z_{od} = \sqrt{L_d/C_d}$ and $Z_{og} = \sqrt{L_g/C_g}$.

There are two advantages of maximizing the number of sections. The magnitude of the gain ripple near mid-band is proportional to $1/N$ [35], where N is number of sections. The other advantage is that the intrinsic noise figure of a distributed amplifier improves with higher number of stages assuming no losses in the artificial transmission lines [36].

Figure 5-8: Lossless cascade of T-sections forming an artificial transmission line.

In the case of a lossless lumped cascade of T-section (Figure 5-8), the propagation coefficient and image impedance are respectively given by [33]:

$$Z_i = \sqrt{\frac{L}{C} \left[1 - \left(\frac{\omega}{\omega_c} \right)^2 \right]} \quad (5.8)$$

$$e^{\gamma} = 1 - \frac{2\omega^2}{\omega_c^2} + \frac{2\omega}{\omega_c} \sqrt{\frac{\omega^2}{\omega_c^2} - 1} \quad (5.9)$$

$$\text{where } \omega_c = \frac{2}{\sqrt{LC}}$$

From these equations, the drain artificial transmission line inductances and characteristic impedances are given by:

$$L_d = \frac{4}{\omega_c^2 (C_{ds} + C_p)} \quad (5.10)$$

$$Ro_d = \sqrt{\frac{L_d}{C_{ds} + C_p}} \quad (5.11)$$

Similarly, the gate artificial transmission line inductances and characteristic impedances are given by:

$$L_g = \frac{4}{\omega_c^2 C_{gs}} \quad (5.12)$$

$$Ro_g = \sqrt{\frac{L_g}{C_{gs}}} \quad (5.13)$$

For pass-band ($f < f_c$), the artificial transmission line has a purely real image-impedance Z (Figure 5-9); the phase constant β is non-null and the attenuation is small (Figure 5-10 and Figure 5-11).

For stop-band ($f > f_c$), the image impedance is null; the phase constant tends towards negative π (Figure 5-10) and the attenuation is exponentially increasing (Figure 5-11).

Figure 5-9: Image impedance of the artificial transmission line with $f_c=20$ GHz.

Figure 5-10: Phase constant of the artificial transmission line with $f_c=20$ GHz.

Figure 5-11: Attenuation constant of a given lossless T-section network.

As shown in Figure 5-10, the phase response is not linear when we approach f_c . Therefore, we must operate the artificial transmission line sections well below their cut-off values.

5.2 Design equations for a conventional distributed amplifier

This section presents the systematic design procedure for distributed amplifiers introduced by Beyer et al. [10]. The analysis focuses on fundamental design considerations and establishes the maximum gain bandwidth product for the distributed amplifier.

In distributed amplifiers, the artificial input (gate) and output (drain) transmission lines absorb the transistor input and output capacitances (C_{gs} and C_{ds}). On the input artificial line, delays occur between each transistor. The artificial output line sections compensate for these delays such that the signal currents of the individual transistor add up in-phase at the output. In HEMTs, since the drain-source capacitance (C_{ds}) is much smaller than the gate-source capacitance (C_{gs}), additional shunt capacitances are usually added along the output line sections to insure equal phases.

For a conventional doubly-terminated distributed amplifier, the A.C. drain current of each transistor travels equally in both direction: toward the load and toward the dummy load on the output line.

At low frequencies, due to the reverse waves, 50% of the output power is wasted through the dummy load, despite the facts that the lengths of the sections are electrically small, the loss is thus minimal and each device is equally matched to its optimum load.

At high frequencies, the line section delays are more significant. The reverse waves do not add up in phase and the power loss through the dummy load is thus negligible [9] at high frequencies. However the load seen by each device is now not optimal. Thus a reduction of the output power at high frequency range is also expected.

These two factors reduce the maximum efficiency of class-A from 50% to about 25%. Taking into account impedance mismatching, line attenuation and other losses and the efficiency drops even lower.

For these reasons, millimeter-wave monolithic power distributed amplifiers generally have lower PAE than non-distributed power amplifiers. While improved PAEs have been shown using modified configurations such as tapered-drain-line distributed amplifiers [37], they are

difficult to realize in monolithic form due to current carrying constraints of on-chip narrow lines.

A conventional distributed amplifier, in which a dummy load terminates the end of both the gate and the drain line, is depicted in Figure 5-12. Notice the presence of the shunt C_x where $C_x + C_{ds} = C_{gs}$. The analysis uses the simplified A.C. FET model [10] shown in Figure 5-13 because it provides a good initial estimate of distributed amplifier performance.

Figure 5-12: Equivalent circuit model of a conventional distributed amplifier.

Figure 5-13: Simplified π -model of a FET

The signal current travels in the gate and drain line with a propagation constant $\gamma = \alpha + j\beta$, where α is the attenuation per line section and β is the phase delay constant.

The equations to characterize wave propagations in a section of artificial line with series inductance "L" and shunt capacitance "C" are given by [68]:

$$V_{n+1} = V_n * e^{-(\alpha + j\beta)}$$

$$\alpha + j\beta = a \cosh\left(1 + \frac{\omega^2 LC}{2}\right) \quad (5.14)$$

The artificial line has a cut-off frequency f_c and a characteristic impedance Z_o , given by [64]:

$$f_c = \frac{1}{\pi \sqrt{LC}} \quad (5.15)$$

$$Z_o = \sqrt{\frac{L}{C}} \quad (5.16)$$

and the phase delay constant per section is:

$$\beta = \sqrt{LC} \quad (5.17)$$

Combining the two equations for f_c and Z_o , the cut-off frequency of the artificial gate line can be written as:

$$f_{c,g} = \frac{1}{\pi \sqrt{L_g (C_{gs})}} = \frac{1}{\pi Z_{og} C_{gs}} \quad (5.18)$$

This equation implies that for a given value of the gate-line characteristic impedance Z_{og} , the maximum gate-line cut-off frequency is determined by the value of C_{gs} , which determines the maximum gate periphery of the FET.

The gate resistance R_i in series with C_{gs} introduces a frequency dependent attenuation per line section of [66]:

$$\alpha_g = 4\pi^2 f^2 C_{gs}^2 R_i * Z_o / 2 \quad (5.19)$$

By similar analysis, the artificial drain line has a cut-off frequency of:

$$f_{c,d} = \frac{1}{\pi \sqrt{L_d (C_{ds} + Cx)}} \quad (5.20)$$

For pass-band, the artificial drain line is matched to Z_o and the characteristic impedance and phase delay per line section are respectively given by,

$$Z_{od} = \sqrt{\frac{L_d}{C_{ds} + Cx}} \quad (5.21)$$

$$\beta_d = \sqrt{L_d(C_{ds} + Cx)} \quad (5.22)$$

The shunt drain output conductance introduces a frequency independent attenuation per line section of [66]:

$$\alpha_d = \frac{Zo}{2R_{ds}} \quad (5.23)$$

The power gain can be derived using the simplified FET model, assuming that the phase velocity of the drain line is matched to the gate line by adding additional shunt drain capacitance, and thus the output currents add constructively. This is equivalent to:

$$\frac{2}{\sqrt{L_g C_{gs}}} = \frac{2}{\sqrt{L_d(C_{ds} + Cx)}} \quad (5.24)$$

The total output current of an N-stage distributed amplifier is given by [10]:

$$I_o = \frac{1}{2} g_m e^{-\gamma d/2} \sum_{k=1}^N V_{ck} e^{-(N-k)\gamma d} \quad (5.25)$$

where V_{ck} is the voltage drop across the kth stage input capacitor, given by [10]:

$$V_{ck} = \frac{V_i * e^{\frac{-(2k-1)\gamma_g}{2} - j \arctan \frac{\omega}{\omega_g}}}{\sqrt{1 + \left(\frac{\omega}{\omega_g}\right)^2} \sqrt{1 - \left(\frac{\omega}{\omega_c}\right)^2}} \quad (5.26)$$

Substituting V_{ck} into (5.25), we obtain (Appendix 1):

$$I_o = \frac{g_m V_i \sinh \left[\frac{N}{2} (\alpha_d - \alpha_g) \right] e^{\frac{-N(\alpha_d + \alpha_g)}{2} - jN\beta - j \arctan \frac{\omega}{\omega_g}}}{2 \sqrt{1 + \left(\frac{\omega}{\omega_g}\right)^2} \sqrt{1 - \left(\frac{\omega}{\omega_c}\right)^2} \sinh \left[\frac{1}{2} (\alpha_d - \alpha_g) \right]} \quad (5.27)$$

The input and output powers are formulated as follows:

$$\begin{aligned}
 P_o &= \frac{1}{2} |I_o|^2 \text{Re}(Z_{id}) \\
 P_i &= \frac{1}{2} \frac{|V_i|^2}{|Z_{ig}|^2} \text{Re}(Z_{ig})
 \end{aligned} \tag{5.28}$$

The expression for the power gain is thus:

$$G = \frac{\text{Re}(Z_{id})}{\text{Re}(Z_{ig})} |Z_{ig}|^2 \frac{g_m^2 \sinh^2 \left[\frac{N}{2} (\alpha_d - \alpha_g) \right] e^{\frac{-N(\alpha_d + \alpha_g)}{2}}}{4 \left[1 + \left(\frac{\omega}{\omega_g} \right)^2 \right] \left[1 - \left(\frac{\omega}{\omega_c} \right)^2 \right] \sinh^2 \left[\frac{1}{2} (\alpha_d - \alpha_g) \right]} \tag{5.29}$$

The distributed amplifier voltage gain (S_{21}) is similar to the common source power amplifier gain detailed in chapter 3 except for the fact that the distributed amplifier has a dummy load. This is because at frequencies below cut-off, the line propagation delays are negligible. This voltage gain is thus:

$$|S_{21}| = \frac{Ng_m Z_o}{2} \tag{5.30}$$

Using Equation (5.35) for $f_h = f_{\max}$, the gain bandwidth product can be formulated as follow:

$$|S_{21}|_{f_{\max}} \leq \frac{Ng_m Z_o}{2} \frac{3}{4\pi C_{gs} \sqrt{R_i Z_o}} \tag{5.31}$$

From Equation (3.1) which states that $f_T = g_m / (2\pi C_{gs})$, the gain bandwidth product becomes:

$$|S_{21}|_{f_{\max}} \leq f_T \frac{3\sqrt{Z_o}}{4\sqrt{R_i}} \tag{5.32}$$

For a 0.2 μm pHEMT, $Z_o = 50 \Omega$ and R_i varies between 9 and 11 Ω , the gain bandwidth product is thus approximately 1.7 f_T . Note that the single-device amplifier discussed in chapter three has a gain-bandwidth product limited by f_T . Thus for OMMIC process having $f_T = 60$ GHz, we get a gain bandwidth product of 102 GHz.

5.3 Power-limiting mechanisms of the conventional distributed amplifier

A distributed amplifier's power and efficiency are limited by the following mechanisms: delay mismatch between the gate and drain lines, gate-line attenuation, drain-line attenuation and maximum total device periphery.

5.3.1 Delay mismatch between the gate and drain lines

Delay mismatch occurs when the output currents do not add in phase, due to the phase delay in the gate being different than the one in the drain, that is: $\beta_g - \beta_d$ is not zero.

The gain for a distributed amplifier with N transistors is given by:

$$\frac{V_o}{V_i} = \frac{-g_m Z_o}{2} \sum_{n=1}^N e^{-(n-1/2)\gamma_g - (N-n+1/2)\gamma_d} \quad (5.33)$$

To simplify the analysis of this limitation, let assume zero attenuation (α_g and $\alpha_d=0$).

Thus:

$$\begin{aligned} \left\| \frac{V_o}{V_i} \right\| &= \frac{g_m Z_o}{2} \left\| \sum_{n=1}^N e^{-j(n-1/2)\beta_g - j(N-n+1/2)\beta_d} \right\| \\ &= \frac{g_m Z_o}{2} \left\| \sum_{n=1}^N e^{-j(n-1/2)(\beta_g - \beta_d)} \right\| \end{aligned} \quad (5.34)$$

It can be seen that the gain becomes maximum when $\beta_g - \beta_d = 0$.

Hence to reduce delay mismatch, the output impedance should be as close to the input impedance as possible.

5.3.2 Gate-line attenuation

The gate-line attenuation attenuates the gate drive of each transistor. The input voltage of the last transistor is attenuated by a factor of $e^{-(N-1/2)\alpha_g}$. In order to limit the gate drive attenuation of the Nth transistor within 0.5 dB (1.122), the gate line attenuation and the gate line maximum frequency should be limited to:

$$\alpha_g \equiv 2\pi^2 f_h^2 C_{gs}^2 R_i * Z_o \leq 1.122$$

$$i.e.: f_h \leq \frac{3}{4\pi C_{gs} \sqrt{R_i Z_o}} \quad (5.35)$$

Therefore, to minimize the gate-line attenuation, the line cut-off frequency f_{cg} should be lower than f_h .

5.3.3 Drain-line attenuation

The output of the first stage is attenuated by a factor of $e^{-(N-1/2)\alpha_d}$ before it reaches the load terminal. In order to limit the drain line attenuation within 0.5 dB (1.122), the following conditions are essential:

$$\alpha_d \equiv \frac{Z_o}{2R_{ds}} \leq 1.122$$

$$i.e.: \frac{Z_o}{R_{ds}} \leq 2.244 \quad (5.36)$$

Therefore, to reduce this drain-line attenuation, dual-gate or cascode (common source common gate) devices can be used since they increase the drain resistance R_{ds} [38, 39].

5.3.4 Maximum total device periphery

This power-limiting mechanism is in fact a consequence of the gate line attenuation mechanism. Referring to the attenuation (α_g) in equation (5.35), for a specified maximum frequency of operation and a given FET, there is an upper limit to the maximum C_{gs} and consequently maximum device periphery that can be employed. Note that as the device periphery increases, C_{gs} increases but R_i decreases. However, the attenuation increase due to C_{gs} is of the second-order magnitude (C_{gs}^2) while the attenuation decrease due to R_i is only of the first-order magnitude.

Therefore, better performance would be realized if one could increase the device periphery without increasing the input capacitance. The next chapter describes a topology which realizes this task.

5.4 Survey of various distributed power amplifiers topologies

Numerous topologies have been attempted to improve the gain and efficiency of the conventional distributed amplifier [11, 40, 41, 43, 45-47]. These include: tapered capacitive degeneration in series with the gate, gate line tapering or drain line tapering, independent biasing of the stages, matrix distributed amplifier. Distributed amplifiers using a Wilkinson combiner or a corporate power combiner, and class-B push-pull distributed amplifiers using distributed paraphase converters have also been designed.

5.4.1 *Tapered capacitive degeneration in series with the gate*

This technique, proposed by Ayasli et al. [11], consists of varying the capacitive degeneration in series with the gate so that the drive levels at each gate are equal at one frequency (Figure 5-14). For best performance, this frequency is usually the highest frequency of interest because that is where the loss is the highest. The issue at hand is that the drive levels are not uniform at the gate of each device at high frequencies because of the frequency-dependency of the gate line attenuation. If the series capacitor reduces the input capacitance by half, the device periphery can be doubled, reducing the input-resistance (R_i) also by a factor of two. The gate-line attenuation, which is proportional to $R_i \omega^2 C_{gs}^2$, is therefore reduced by a factor of two.

The adverse effect of this technique is that it changes the phase of the gate signals; therefore phase correction using different line lengths at the drain should be used for compensation.

Figure 5-14: Tapered capacitive degeneration ($C1 < C2 < C3 < C4$)

5.4.2 Gate line tapering

This technique [40] consists of tapering the gate line so that each line section is matched to the subsequent load, which includes the next line-section and the FET input impedance. Optimization is done at the highest frequency of interest where the loss is the highest. Phase difference in the gate line implies a need for phase correction in the drain line as well. Figure 5-15 shows a tapered gate line distributed amplifier. From Figure 5-15, for a 4-stage distributed amplifier, let $Z_{g1} = Z_0 = 50\Omega$ and R_{in} the input resistance of the FET, then the line impedances Z_{g2} , Z_{g3} , Z_{g4} , Z_{g5} can be found using the following algorithm.

Let $Z_{g5} = x \Omega$, where x is unknown. Then

$$Z_{g4} = x \parallel R_{in},$$

$$Z_{g3} = x \parallel R_{in} \parallel R_{in} = x \parallel (R_{in}/2)$$

$$Z_{g2} = x \parallel R_{in} \parallel R_{in} \parallel R_{in} = x \parallel (R_{in}/3)$$

Thus:

$$Z_{g1} = x \parallel R_{in} \parallel R_{in} \parallel R_{in} \parallel R_{in} = x \parallel (R_{in}/4) = \frac{x \frac{R_{in}}{4}}{x + \frac{R_{in}}{4}} = \frac{x R_{in}}{(4x + R_{in})} = Z_0$$

Since we know Z_0 and R_{in} , we can easily solve for x .

Figure 5-15: Tapered gate line distributed amplifier

5.4.3 Drain line tapering

This technique [37, 41] consists of tapering the drain line sections in such a way that the backward wave currents cancel each other. The characteristic impedance for each section is $N^{\text{th}} \cdot Z_0$ where Z_0 is the characteristic impedance of the last stage and N is the stage number. A N -section distributed amplifier thus requires the following line impedances:

$$Z_{dN} = Z_0, Z_{dN-1} = Z_0 [N/(N-1)], Z_{dN-2} = Z_0 [N/(N-2)], Z_{dN-3} = Z_0 [N/(N-3)], \dots$$

$$Z_{d1} = Z_0 \cdot N.$$

For example, a 4-section distributed amplifier with a 50Ω output load requires the following line impedances: $Z_{d4} = 50 \Omega$, $Z_{d3} = 67 \Omega$, $Z_{d2} = 100 \Omega$ and $Z_{d1} = 200 \Omega$ (Figure 5-16). Such high impedance (200Ω) cannot be realized in MMIC microstrip, because such line would be too narrow, typically less than $4 \mu\text{m}$ width. Such narrow lines would lead to high process variation, low current-carrying capability and high skin-effect losses. Instead, partial tapering is usually implemented [42].

For example, with partial tapering, the microstrip lines are linearly tapered from 60 to 100Ω . The drain dummy termination is sometimes selected to be very high (230Ω) to reduce power dissipation in the termination. It was found that a slight increase in power would result by completely eliminating the drain dummy termination. Elimination of the dummy termination slightly degrades output match and VSWR. However this degradation is negligible [37].

Figure 5-16: Tapered drain line distributed amplifier

5.4.4 Independent biasing of the stages

At high frequency, each device does not see the same load line at its output. Typically the device farther away from the input does not operate at its peak output when the first device is optimally driven. One way to equalize the drive is to independently bias the devices. The adverse effect of this technique is mainly the increased parasitics that accompany a more complex circuitry, especially in coplanar waveguide circuits.

5.4.5 Matrix distributed amplifier

The matrix distributed amplifier [43] consists of an array of m rows and n columns of active devices. Each column is linked to the next one by a lumped inductor or distributed transmission line, while each row is coupled to the successive one by the trans-conductance of the active devices (Figure 5-17).

Figure 5-17: Lumped-element matrix distributed amplifier

It has been found [44] that the matrix distributed amplifier offers similar performance in terms of small-signal gain, reflection coefficients and noise figures when compared to an equivalent cascaded two-stage distributed amplifier. Therefore, this design is more space efficient than conventional distributed amplifiers.

5.4.6 Differential distributed amplifier

Figure 5-18: Example of a fully differential distributed amplifier.

Some differential distributed amplifiers have been reported [45,46,47]. Figure 5-18 displays the schematic of a typical fully-differential distributed amplifier, consisting of four differential gain stages. The artificial transmission lines of the single-ended distributed amplifier have been replaced with a pair of transmission lines for each gate and drain line. A

pair of complementary signals applied to the gate lines produces amplified differential signals across the drain lines by the differential stages. The ports are terminated with a load equaled to the line characteristic impedance. The differential unit cell consists of a pair of PHEMTs and with their common source connected to the drain of another PHEMT which acts as a current source. The gate and the source of the current source PHEMT are grounded through a resistor. The DC current of the unit cell is determined by the size of the current source PHEMT and its source resistor. The DC current can be adjusted by varying the source resistor of the current source PHEMT. When compared to a similar non-differential distributed amplifier [6], it has been found that the differential approach yields an increase by 2.5V in output voltage but with an decrease of about 4dB in gain.

Differential distributed amplifiers have a voltage gain of [45]:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{-Ng_m}{2\sqrt{1-\omega^2/\omega_c^2}} \sqrt{\frac{L_d}{C_d}} e^{-N\theta} \quad (5.37)$$

where N is the number of stages, g_m is the small-signal transconductance of the differential gain stage, and ω_c is the cutoff frequency $2/\sqrt{LC}$. As evidenced in equation (5.37), the gain is directly proportional to the line impedance, $Z_0 = \sqrt{L_d/C_d}$. Due to the complementary differential inputs, the line impedance of the differential circuit should be equal to half of the desired input impedance. For most case, the desired input impedance is 50Ω and hence, each separate gate line impedances should be 25Ω .

The advantages of the differential distributed amplifier are the requirement of a smaller line inductance and a higher output voltage.

However there are many drawbacks. A differential distributed amplifier has a larger power dissipation since twice larger g_m is required to produce the same gain as in the corresponding non-differential circuit. In addition, a differential distributed amplifier requires more layout space and produces a higher noise figure due to the doubling of circuit complexity compared to a non-differential version. These drawbacks often reduce the performance of the differential distributed amplifier for millimeter-wave applications. In the case of a CPW process, more parasitics between the air bridges and the lines and between the two complementary lines will further reduce the performance of the MMIC differential distributed amplifier.

5.4.7 Other variations of the distributed amplifier

Other variations of the basic distributed amplifier include: distributed power amplifier using corporate power combiner [48, 49], class-B push-pull distributed amplifier using a distributed paraphase converter [50]. Dual-gate or cascode distributed amplifiers [38,39] improve the output power by offering the following characteristics: 1) higher output shunt resistance reduces loading of the drain line (higher gain), 2) lower gate-to-drain capacitance reduces negative feedback at the high end (higher bandwidth), and 3) gain control is achieved.

To sum up, all the topologies mentioned in this chapter, except for the differential distributed amplifier, can improve the efficiency but not the output voltage swing of the conventional distributed amplifier. The next chapter will discuss one novel topology that tries to address this issue.

Chapter 6: Design of double-gate-line CPW distributed amplifier

In chapter 5 we have established some power-limiting mechanisms of the conventional distributed amplifier (DA). On the basis of these mechanisms, we will next examine the double-gate-line distributed amplifier as one alternative topology to improve the conventional distributed amplifier.

The first section of this chapter will present the characteristics of the pHEMT employed in this work. The second section will discuss the lumped element design and simulation results of the proposed amplifier. The third section will compare the single and double-gate line distributed amplifier performance. The last section will present the implementation of the double-gate-line distributed amplifier.

In the proposed topology, in order to obtain a higher output voltage swing, the output currents from two conventional distributed amplifiers will be combined into one single output line, as shown in Figure 6-1.

Figure 6-1: Simple diagram of a double-gate-line distributed amplifier.

Two similar designs have been realized before. The first one by Ayasli used a passive power divider and operated over the frequency range 2-20 GHz [62]. The second one used a double-drain-line distributed amplifier acting as a power-divider stage and a double-gate-line

distributed amplifier as the main stage [63]. Each stage has 10 cascode cells using 0.15 μm pHEMT. The achieved gain was 17.3 dB over DC-41.5 GHz. The average output voltage was 3Vpk-pk. However, this excellent performance was achieved at the expense of large DC power consumption.

For the purpose of this thesis, a double-gate-line distributed amplifier with improved power efficiency is to be designed using CPW lines. The available chip area was initially set at around $2 \times 1 \text{ mm}^2$. A power gain of 8 dB or more is to be realized. The bandwidth is 40 GHz and the output voltage swing of this amplifier is to be maximized. To minimize the chip size, off-chip DC de-coupling capacitors at the input and output are used. In addition, the input and output return loss of the amplifier should be better than 10 dB over the pass-band in a 50 Ω system.

With the double-gate-line distributed amplifier, the effects of some of the power-limiting mechanisms outlined in chapter 5 have been reduced. First, the input signal is separated into two gate lines and combined on a single drain line, effectively giving a $4 \times 30\text{-}\mu\text{m}$ device periphery instead of a $4 \times 15\text{-}\mu\text{m}$. The total device periphery is therefore doubled without increasing the gate capacitance. Thus the gate attenuation is limited to a $4 \times 15\text{-}\mu\text{m}$ periphery whereas the output power is determined by a $4 \times 30\text{-}\mu\text{m}$ periphery; the gate-line maximum frequency as well as attenuation thus remains unchanged.

The design was carried out using the Agilent's microwave circuit CAD Advanced-Design-System (ADS) and Momentum EM simulator.

The entire design process involves selecting the device size; designing and simulating the lumped elements circuit as well as the bias and terminal matching circuit; replacing the lumped elements in the circuit by CPW equivalents; and finally, implementing the circuit layout using Philips-OMMIC ED02AH process foundry rules. The basic design essentially follows the distributed amplifier guidelines presented in [35] and [10].

6.1 pHEMT characteristics

The integrated circuits have been fabricated using the GaAs 0.2 μm pseudomorphic HEMT technology from Philips OMMIC foundry. With the ON-type FET (as opposed to the OFF-type which has a positive threshold voltage), the transistor has a threshold voltage V_t of -0.9 V , a drain-gate breakdown voltage (V_{brdg}) of 8 V , and a transition frequency* f_T of 60 GHz .

The gate width (and the number of fingers) selection is critical in determining the upper cutoff frequency of a circuit. After sweeping the gate width and the number of fingers, it was determined that a $4 \times 15\text{ }\mu\text{m}$ pHEMT would provide a cut-off frequency of over 41 GHz and a C_{gs} value about twice as large as C_{ds} .

To obtain maximum linearity in voltage and power, class-A operation was selected. The DC operating point of the pHEMT was initially set to: $V_{\text{ds}} = 3\text{ V}$, $I_{\text{ds}} = I_{\text{dss}}/2$, $V_{\text{gs}} = -0.2\text{ V}$. The DC I-V curves are given in Figure 6-2.

* Transition frequency is referred to as "extrinsic frequency" in the Phillips OMMIC manual (section: PCM and Guarantees).

Figure 6-2: Device I-V curves for a 4x15um pHEMT (V_{GS} from $-0.8V$ to $0.3V$ with $0.1V$ increment)

The transconductance of a 4x15 pHEMT is 22 mS. Equation (5-7) approximates the number of stages for an ideal DA to be five.

The I_{DSS} of a 60 μm HEMT is 13 mA. Since the operation point of all devices is located at midpoint of I_{DSS} , the peak current is 6.5 mA and the maximum current swing is 13 mA. For a five-stage distributed amplifier, the total peak current is about 32.5 mA. Hence the output voltage swing of this circuit can be predicted to be 3.2 Vpp for a 50 Ω system.

6.2 Lumped element design and simulation

Double-Gate-Line distributed amplifier is a distributed amplifier having two input gate lines and a common output drain-line. Each gain cell consists of a single common source

device. The input signal is split into two gate lines via a power divider. An impedance-matching network matches the line impedance to 50 Ω .

Figure 6-3 and Figure 6-4 show the input and output capacitances of the 4x15 μm pHEMT cell. The output capacitance ($C_{\text{out}} = -(\omega X)^{-1} = -(\omega \cdot \text{imag}\{Z_{\text{out}}\})^{-1}$) is much larger at the lower frequency end.

The gate artificial transmission line absorbing the input capacitance should then have a cut-off frequency of

$$f_c = (\pi C_{\text{in}} Z_0)^{-1} = 65 \text{ GHz.}$$

Figure 6-3: Input capacitance of a pHEMT cell.

Figure 6-4: Output capacitance of a pHEMT cell.

However, the maximum frequency of operation is approximately 86% of the artificial transmission line cut-off frequency in order to maintain a return loss of less than 10 dB [56]. Therefore, the maximum artificial transmission line frequency is 55.9 GHz. This maximum

frequency is obtained with the assumption that the artificial transmission line is ideal, i.e. lossless.

To minimize the phase delay difference per section between the gate and the drain line, the total per-section output capacitance should be equal to the total per-section input capacitance, and the gate-line impedance should be equal to the drain-line impedance. Since the two drain lines are combined, i.e. a pair of output capacitances are in parallel, the total output capacitance per section is doubled. At 42 GHz, the value of the input capacitance is around 0.097 pF and the value of the output capacitance is around 2×0.05 pF. The total output capacitance per section is thus almost the same as the total input capacitance.

The schematic diagram of a double-gate-line distributed amplifier with lumped elements is shown in Figure 6-5.

Figure 6-5: Schematic of a lumped double-gate-line distributed amplifier.

The double-gate-line distributed amplifier has five gain stages with a common source configuration. Input signals are applied to the two gate lines via a power divider. The overall circuit forms a 6-port device with four of the ports terminated with a load. The gate line has a characteristic impedance of 78Ω and the drain line 50Ω .

To prevent oscillation, a small series inductance is added to the FET source.

Coplanar waveguide technology was used in this design because of its superior high-frequency properties. If microstrip lines were used in this design, the circuit would have been less complex due to elimination of the air-bridges between the lines.

6.3 Comparison between the double-gate-line and the conventional distributed amplifier

It is interesting to now compare the performance of the conventional (single-gate-line) with the double-gate-line distributed amplifier in order to assess the relative merits of each topology.

The conventional distributed amplifier schematic is shown in Figure 6-6.

Figure 6-6: Lumped conventional distributed amplifier.

For the benefit of a fair comparison, both topologies will have equivalent gain, bandwidth and input and output matching. Both use ideal lumped elements. Both have the same number of stages and transistor size.

The only differences between the two topologies are that with the double-gate-line distributed amplifier, the DC-power-dissipation is doubled and, and the drain-line does not require shunt capacitances.

The s-parameters of both circuits are shown from Figure 6-7 to Figure 6-9. With the double-gate-line-distributed amplifier, the S21 parameter is simulated between the combined input gate-line and the common output drain-line.

After optimization, the lumped double-gate-line circuit shows an average gain of 10 dB with an in-band ripple of about 1 dB from 3-44 GHz. Meanwhile, the conventional distributed amplifier shows an average gain of about 2-dB less than the double-gate-line-distributed-amplifier (Figure 6-7).

Figure 6-7: Gain of the lumped double-gate-line (solid line) and conventional (dash line) distributed amplifiers.

Figure 6-8: Input return loss of the lumped double-gate-line (solid line) and conventional (dash line) distributed amplifiers.

Figure 6-9: Output return loss of the lumped double-gate-line (solid line) and conventional (dash line) distributed amplifiers.

Simulations show that the output voltage of the lumped double-gate-line circuit is 5.2 Vpp while the output voltage of the conventional circuit is 4 Vpp (Figure 6-10). This increased output voltage is attributed to the combined currents on the drain line.

Figure 6-10: Output voltage of the lumped double- and conventional distributed amplifiers.

Output versus input power plot (Figure 6-11) also shows that the double-gate-line circuit's output power is about 2.5 dB higher than the corresponding conventional circuit output power. This increased output power is attributed to the doubling of the circuit's transconductance.

Figure 6-11: P_{out} versus P_{in} of the lumped double-gate-line (dashed line) and conventional (solid line) distributed amplifiers.

From the plots given in this section, it can be argued that the double-gate distributed amplifier yields similar gain and bandwidth as with a conventional distributed amplifier. However, the double-gate-line distributed amplifier offers an increased output power by 2.5 dB and an increased output voltage swing by 37%.

6.4 Layout and MMIC implementation of the circuit

The design was realized with CPW technology as the propagation medium. The drain and gate CPW lines widths are selected based on the current requirements and the required inductance and characteristic impedance. The five-stage distributed amplifier requires high current on the drain line, and much lower current on the gate line. In order to have enough space to layout the drain-line and its coplanar ground planes, it was necessary to introduce a long line strip between the drain-line and the FETs. This extension line can be made shorter in a microstrip circuit.

There might exist an advantage to design distributed amplifiers with microstrip lines. A comparison between two identical distributed amplifiers over frequency range of 2-20 GHz, one realized in microstrip technology and one in CPW [52], had found that the CPW version

shows a gain drop of about 2dB compared to the microstrip version. It was however mentioned that this gain offset could be attributed to the differences in transconductance from different wafers. On the other hand, the CPW version offers advantages such as a more simplified process (no vias, no backplane gold plate), lower cost over similar microstrip amplifiers. However, either version offers similar phase linearity and noise figure.

The layout dimensions of the proposed design were optimized with Momentum in order to obtain the highest and flattest gain, while keeping the chip size as small as possible. After optimization, the gate and drain lines widths are $12\ \mu\text{m}$ and $15\ \mu\text{m}$, respectively. Their gaps are respectively $3\ \mu\text{m}$ and $38\ \mu\text{m}$ and their characteristic impedances are $48\ \Omega$ and $62\ \Omega$.

Since the total gate width is $4 \times 15\ \mu\text{m} = 60\ \mu\text{m}$ or $0.060\ \text{mm}$ and the drain current I_{dss} per gate width is $250\ \text{mA}/\text{mm}$, the current per HEMT is $15\ \text{mA}$ and the total current of a class-A amplifier is $10 \times 0.060\ \text{mm} \times 250\ \text{mA}/\text{mm} = 150\ \text{mA}$.

The current through the microstrip line is calculated for a microstrip line width of $15\ \mu\text{m}$:

$$150\ \text{mA}/15\ \mu\text{m} = 10\ \text{mA}/\mu\text{m}$$

Given $I_{\text{dss}}/2$ operation, the current through the microstrip line is $5\ \text{mA}/\mu\text{m}$. Since the maximum DC limit for a safe current is $6\ \text{mA}/\mu\text{m}$, the current is within the safe limits.

Figure 6-12: Layout of the double-gate-line distributed amplifier

Figure 6-12 shows the layout of the double-gate-line distributed amplifier where the RF input pad and the RF output pad are respectively on the left and right extremities. The V_g DC biases are applied to the HEMT's through two DC pads, the top-right and bottom-right pads. On the other hand, the V_d DC biases can be applied to the HEMT's through either one of the two DC pads, the top-left and bottom-left pads.

The gate line terminations (top-right and bottom-right pads) are composed of a strip line acting as an inductor, a shunt capacitor acting as a RF-choke, a series resistor and a DC probe-pad. The drain line terminations are composed of a series resistor, a large shunt capacitor acting as a RF-choke, a long strip line acting as an inductor and a DC probe-pad.

Figure 6-13: Zoom up image of 2 pHEMTs

Figure 6-13 shows the layout of the $4 \times 15 \mu\text{m}$ PHEMT. Each finger has a gate width and length of $15 \mu\text{m}$ and $0.2 \mu\text{m}$. The four fingers are in parallel, making up the gate resistance. Hence the gate resistance of a four-finger PHEMT is lower than the one of a two-finger PHEMT, provided both have the same total gate width. The four PHEMT fingers share common drain and source terminals in order to offer a good area efficiency.

To improve the return losses, a short transmission line is inserted on both sides of each FET, between the source and the ground plane (Figure 6-13). The stability of the circuit is thereby increased, but with a trade-off of high frequency gain. The circuit is unconditionally stable up to 46 GHz.

Air bridges are used to connect the two CPW ground planes. Air bridges in coplanar design are used to suppress the even mode propagation along a line and to keep the reference ground bias constant along the line. These bridges are primarily placed at the discontinuities. A 50 Ω CPW was employed at the amplifier input and output to reach the edge of the chip.

Four bias pads were provided for biasing the HEMTs' gates and drains.

The simulation results for the final circuit as laid out are shown in Figure 6-16. The gain (S_{21}) is 8 ± 1 dB with a 3 dB bandwidth of 41 GHz. The input return loss is better than 7.5 dB and the output return loss is better than 10 dB up to 39 GHz. The gain and return loss degradation is attributed to the decreased effectiveness of the input matching network to match to 50 Ω .

The OMMIC process only provides models for the microstrip-type components. Since all of the passive components in this design are CPW-type, EM simulation is critical. The EM simulation was carried out with Agilent-EEsof's Momentum simulator. The EM simulations were done separately for the input power divider, the gate line and the drain line including the matching networks. It has been found that the gate line and drain line could not be simulated together since there would have been 20 ports. Simulating them separately allows reduction of the number of ports to five, and the simulation time to a feasible duration.

The input power divider layout is shown in Figure 6-14. Its simulated s-parameter is shown in Figure 6-15.

Figure 6-14: Layout of the power divider.

Figure 6-15: S-parameter of the power divider.

All of the EM simulation results were then put in the overall circuit simulation as S-parameter blocks.

The final layout size of the CPW double-gate-line distributed amplifier is 3.2 mm x 0.9 mm. The momentum simulation results for the final circuit are shown in Figure 6-16. The total DC power dissipation was 288mW.

Figure 6-16: *S*-parameters of the double-gate-line distributed amplifier layout.

Chapter 7: Experimental results

7.1 Introduction

This chapter presents experimental results of the CPW double-gate-line distributed amplifier designed in Chapter 6. First, the test setups used for the small-signal s -parameters and output power measurements of the double-gate-line distributed amplifier are described. Then, plots of the results including s -parameters, group delays, PAE and 1dB power-gain-compression point are given. Finally, deviations between measured results and predicted values are explained. All MMIC measurements were made with on-wafer probing. All the measurements were taken from a 4" wafer at the Communication Research Centre (CRC) microwave lab in Ottawa.

7.2 S-parameter measurement setup

The test setup is shown in Figure 7-1 and includes DC-supplies, device-under-test (DUT) and a network analyzer.

Figure 7-1: Test setup for s -parameter measurements.

The DUT is a fabricated 5-stage CPW double-gate-line distributed MMIC amplifier as shown in Figure 7-2.

Figure 7-2: Microphotograph of the CPW double-gate-line distributed amplifier.

The S-parameter measurements were performed with a HP8510C network analyzer. The network analyzer is capable of accurately extracting the s-parameters of the device over the frequency band 45 MHz to 65 GHz. The HP8510C was calibrated up to the probe tips with the Open-Short-Load-Through (OSLT) calibration method. Coplanar waveguide probes were used for the RF signals. The RF connecting cable between the probes and the test equipments are of type-V. Cables and connector of type-V can operate up to 65 GHz.

For DC biasing, six-pin probes were employed. All of the unused pins are grounded.

7.3 Output power measurement setup

Figure 7-3: Power Measurements Setup

The output power measurement setup is shown in Figure 7-3 and includes a Wiltron signal generator that generates RF signal over the frequency range 10 MHz to 40 GHz. Note that because of the limited signal power that the Wiltron can generate and the higher coaxial cable

losses at 30 GHz and 40 GHz, an additional power amplifier was added to the Wiltron signal generator to provide increased power up to 11 dBm at these frequencies. An HP8565E Spectrum Analyzer and a power meter were used to monitor the output power.

For accurate measurement, the power meters were calibrated before the DUT was connected. After calibration, the input power to the DUT is the incident power minus the loss between the generator and the DUT. The output power is the power read on the power meter plus the cable loss between the DUT and the power meter.

7.4 Measured s-parameter results

Figure 7-4 shows the magnitudes of the measured S-parameter of the double-gate-line distributed amplifier. The measured gain is 7.3 ± 1 dB. The 3-dB bandwidth is about 41 GHz. Figure 7-5, Figure 7-6 and Figure 7-7 compare the simulated versus the measured results for each S-parameter.

Figure 7-4: S-parameter measurements of the double-gate-line distributed amplifier.

Figure 7-5: Measured (dotted-line) and simulated (solid-line) gain.

Figure 7-6: Measured (dotted-line) and simulated (solid-line) input return loss.

Figure 7-7: Measured (dotted-line) and simulated (solid-line) output return loss.

The S21 plot (Figure 7-5) shows that the measured gain differs from the simulated gain at around 0.5-3 GHz and beyond 40 GHz. But it is in close agreement (± 1 dB) with the simulated gain between 3 GHz and 40 GHz.

One of the possible explanations for the peaks in the measured gain curve at low frequency is the fact that the power splitter and the two gate-lines were simulated separately. Note that during momentum-simulation, these two structures, as well as the drain-line, were simulated separately because of the high number of ports on these structures (seven on the gate-line, twelve on the drain-line), which when combined with the multiple layers substrate, causes convergence problem with Momentum-simulator.

Though the output return loss is mostly in agreement with the simulated results, the input return loss is about 5dB worse than the simulated one, as seen in Figure 7-6. This increased input mismatch is due to the fact that the power splitter and the two gate-lines were simulated separately. Also, although care had been taken to include the drain-bias lines in the simulation in order to account for the capacitive parasitic at the air bridges between the gate lines and the drain bias lines, Momentum may not have predicted the correct small-signal behaviors.

Another possible explanation for the differences is the process's immaturity regarding CPW structures modeling in power amplifier design. Momentum simulation of the passive CPW components (capacitors, inductors, resistors) was a time-consuming process where over or under-estimation can happen. Also, the CPW passive components modeling of this process as well as its multi-layer substrate modeling are still at its experimental stage and further

future work should include more analysis and comparison of the performance of these CPW structures.

Finally, it is important to note that the gain roll-off of this amplifier is very gradual at 40 GHz, which is important for digital applications, as a sharp gain roll-off often seen in distributed amplifiers will lead to excessive group delay peaking and a deteriorated eye-diagram [51].

7.5 Effects of gate and drain bias voltages on frequency response

The effects of gate bias voltages on the gain and return losses while the drain voltage V_d is set to 4 V are illustrated in Figure 7-8. It was found that the gain is highest at $V_g = -0.2$ V. The gain drops below zero when V_g is -0.1 V and this is attributed to the bias sensibility of the impedance matching networks.

Figure 7-8: Gains at 3 different V_g (while $V_d=4$ V)

Likewise, the effects of drain bias voltages on the gain and return losses while the gate voltage V_g is set to -0.2 V are illustrated in Figure 7-9. The gain is relatively the same when V_d is increased from 4 to 4.5 V.

Figure 7-9: Gains at 3 different V_d (while $V_g = -0.2$ V)

As V_d is increased from 3 V to 4 V, the drain current increases, thus the gain increases. A further increase in V_d does not increase the gain.

Figure 7-10 and Figure 7-11 show the return losses. The output return loss at $V_g = -0.1$ V (dotted-line) deviates significantly from the other two curves of $V_g = -0.2$ V and -0.3 V. This may be caused by the fact that the bias point is too high and too close to the maximum gate voltage (0 V).

Figure 7-10: Output return loss at 3 V_g while $V_d=4$ V.

Figure 7-11: Input return loss at 3 V_g while $V_d=4$ V.

7.6 Group delay

In order to minimize signal distortion and timing jitter, the group delay is preferred to be relatively constant within the driver amplifier frequency range of operation. The group delay of the double-gate-line distributed amplifier is shown in Figure 7-12. The average group delay is about 140 ± 5 ps.

Figure 7-12: Measured group delay of the CPW double-gate-line distributed amplifier.

7.7 PAE, 1-dB power compression point and output voltage swing

Figure 7-13 shows the output power and PAE with respect to the input power and Figure 7-14 shows the 1dB compression point (P_{out}) and PAE with respect to frequency. The maximum PAE is 18% and occurs at 14 dBm input power and 18 dBm output power. The output power and PAE decrease at high frequency. The decrease of the output power and PAE at high frequency is attributed to the input return loss rapid degradation. A better power divider design should improve the PAE at the upper frequency range.

Figure 7-13: P_{out} and PAE versus P_{in} .

Figure 7-14: 1dB power compression point and PAE versus frequency at $P_{in}=10$ dBm.

From the measured output power, the 1-dB power compression point is determined to be about 12 dBm input power and 17 dBm output power.

The eye diagram was not tested. Instead, the measured output power was used to calculate the output voltage swing of the driver amplifier.

The maximum output power is the ratio of the squared peak-to-peak voltage to 8 times R where R is the 50 Ω load impedance. Since the output powers are 13 dBm, 12 dBm, 11 dBm and 10 dBm (at 10 GHz, 20 GHz, 30 GHz and 40 GHz), the corresponding output voltage

swings are 2.83 V, 2.52 V, 2.24 V and 2.00 V, respectively. The expected output voltage swing was 3.2V.

7.8 Comparison with other amplifiers

This section compares the performance of similar amplifiers reported in the literature. Such comparison is always difficult to make since the amplifier performance depends on many criteria, including bandwidth, process materials, FETs gate periphery, biasing operating point, number of stages, etc.

To simplify the comparison, only amplifiers reported in the literature having a gate length of 0.2 μm GaAs FET or HEMT technology are shown in the following table.

Gate periphery (μm)	Gain (dB)	Bandwidth (GHz)	Midband voltage Swing (V)	DC-power dissipation (W)	Area (mm^2)	Reference
500	7	2-20	unavail.	unavail.	unavail.	[52]
660	10	2-30	unavail.	0.36	1 x 2	[53]
5400	20	6-21	2.9	unavail.	unavail.	[57]
600	7.3	0.05-41	2.52	0.288	0.9 x 3.2	This work
600	5.7	0.5-40	3	1.1	3 x 2.5	[58]
unavail.	6.8	0.5-40	2.9	1.6	1 x 1	[59]
unavail.	7	0-44	unavail.	1	1.5 x 2.5	[60]
600	8	1-53	3	0.35	2.1 x 1.0	[43]
300	5.5	5-50	unavail.	unavail.	unavail.	[54]
unavail.	4	9-70	2.3.	unavail.	1 x 0.5	[55]
400	9	2-52	2.1	unavail.	2 x 2.5	[61]

It can be seen from the table that this work has one of the highest gains and lowest power dissipations in the 0.5-40 GHz category of driver amplifiers, while maintaining an average output voltage swing and chip size.

Limiting the comparison to only designs realized in Ommic's 0.2 μm pHEMT MMIC technology, the following observations may be made:

Type	P_{DC}	Simulated Gain	Bandwidth	Simulated Output Voltage Swing
Matrix	0.72W	10 dB	41 GHz	6.4Vpp
Conventional	0.144W	10 dB	41 GHz	4Vpp
Double-Gate-Line	0.288W	10 dB	41 GHz	5.2Vpp

Matrix distributed amplifiers have some advantages over the conventional. First, the matrix amplifier configuration is more flexible since the gain can be increased by using additional rows of transistors. Secondly, matrix amplifiers have higher output voltage swing.

On the other hand, double-gate-line distributed amplifiers also have several advantages over conventional and matrix distributed amplifiers. Compared with conventional DAs, double-gate-line distributed amplifiers have a higher output voltage swing. Compared with the matrix DAs, double-gate-line distributed amplifiers have a lower power dissipation.

However, the double-gate-line distributed amplifier configuration is more difficult to design and implement since the combined drain-line is surrounded by the two gate lines. Moreover, cross-over between the gate-line and the drain bias line can affect the impedance matching.

Chapter 8: Conclusion and future work

8.1 Summary

In this thesis a general investigation of circuit topologies for broadband, efficient and high power microwave amplifiers was realized. This thesis also provides a survey of common distributed amplifier topologies. Power-limiting mechanisms of the conventional distributed amplifiers have been analyzed and possible solutions have been proposed. On the basis of these power-mechanisms, a five-stage double-gate-line CPW distributed amplifier has been designed and implemented using 0.2 μm pHEMT technology and 4x15- μm device periphery.

To get a high output voltage, and consequently a high output power, the basic idea is to put two distributed amplifiers in parallel to add their currents in a single common drain-line. This topology has the advantage of combining on a single drain line two conventional distributed amplifiers, effectively doubling the device periphery without doubling the gate capacitance. Thus the gate attenuation is not increased and the device size is kept small.

The realized circuit had a chip area of 0.9x3.2 mm². An average power gain of 7.3 dB and a 3-dB bandwidth of 41 GHz were achieved. A maximum PAE of 18% was also realized. The DC power dissipation was 0.288W with an output voltage swing of 2.5Vp-p at midband.

Compared to the conventional distributed amplifier performance, the double-gate-line distributed amplifier offers similar small signal gain and bandwidth but an increased output power by 2.5 dB and an increased output voltage swing by 37%.

Compared with other driver amplifiers in the 0.5-40 GHz category, the proposed topology has one of the highest gains and lowest power dissipations.

Although the proposed topology allows a lower power dissipation than the matrix distributed amplifier, its implementation is more complex because of the cross-over between the gate-lines and the drain-bias line as well as the limited space available for the drain line.

These are promising results for such circuits and driver modules. This circuit topology is one of the many possible approaches in long haul optical transmission system applications.

8.2 Future work

This GaAs pHEMT based distributed amplifier was intended for optical modulator driver applications. To meet the requirements for these applications of ultra-broadband, efficient, linear MMIC high power microwave amplifiers with over DC-40 GHz bandwidth, >2.5 V output voltage swing, >15% PAE and high linearity, improvements at both the device level and circuit level are essential.

At the device level, improvements in efficiency could be obtained by using pHEMT technology with higher breakdown voltage. HBTs process could be used to improve circuit performance. These devices have a higher power capability than HEMTs. Reported amplifiers with HBT's are also capable of very high power added efficiency. In addition, InP-based HEMT can also be utilized instead of GaAs to obtain higher circuit performance, since these devices have significantly improved transconductance and f_t , when compared with GaAs HEMT.

Improvements in efficiency can be obtained using a low-loss broadband power divider. An active power-divider-preamplifier can also be used. The pre-amplifier can be a distributed amplifier with a single input gate-line and two output drain-lines, providing two in-phase input signals for the main amplifier.

Cascode cells could also be employed since they allow a better input-output isolation. A microstrip line would be preferred due to the high reliability of today's via hole technology and, especially when cascode cells are used, better performance could be obtained since the cross-talks at the unavoidably frequent air-bridges would be eliminated.

APPENDIX 1: DERIVATION OF IO

$$I_o = \frac{1}{2} g_m e^{-\gamma_d/2} \sum_{k=1}^N V_{ck} e^{-(N-k)\gamma_d}$$

where V_{ck} is the voltage drop across the k th stage input capacitor, given by:

$$V_{ck} = \frac{V_i * e^{\frac{-(2k-1)\gamma_g}{2} - j \arctan \frac{\omega}{\omega_g}}}{\sqrt{1 + \left(\frac{\omega}{\omega_g}\right)^2} \sqrt{1 - \left(\frac{\omega}{\omega_c}\right)^2}}$$

After substituting V_{ck} into I_o :

$$I_o = K e^{(-1/2 \gamma_d)} \left(\sum_{k=1}^n e^{(-1/2 (2k-1) \gamma_g)} e^{-(n-k) \gamma_d} \right)$$

$$\text{Where } K = \frac{g_m V_i e^{\left(-j n \beta - j \arctan \left(\frac{\omega}{\omega_g}\right)\right)}}{2 \sqrt{1 + \left(\frac{\omega}{\omega_g}\right)^2} \left(1 - \left(\frac{\omega}{\omega_c}\right)^2\right)}$$

Taking out terms containing n yields:

$$I_o = K e^{(-1/2 \gamma_d + 1/2 \gamma_g - n \gamma_d)} \left(\sum_{k=1}^n e^{(-k \gamma_g + k \gamma_d)} \right)$$

Let $\Delta = \gamma_d - \gamma_g$, then

$$I_o = K e^{\left(-\frac{\Delta}{2} - n\gamma_d\right)} \left(\sum_{k=1}^n e^{(-k\Delta)} \right)$$

Multiplying the summation and the denominator by $e^{\Delta} - e^{(-\Delta)}$ yields:

$$I_o = \frac{K e^{\left(-\frac{\Delta}{2} - n\gamma_d\right)} \left(\sum_{k=1}^n (e^{[(k+1)\Delta]} - e^{[(k-1)\Delta]}) \right)}{e^{\Delta} - e^{[-\Delta]}}$$

After rewriting the above equation:

$$I_o = \frac{K e^{\left(-\frac{\Delta}{2} - n\gamma_d\right)} \left(\left(\sum_{k=1}^{n-2} (e^{[(k+1)\Delta]} + e^{[n\Delta]} + e^{[(n+1)\Delta]}) \right) - \left(\sum_{k=1}^{n-2} e^{[(k+1)\Delta]} \right) - e^{\Delta} - 1 \right)}{e^{\Delta} - e^{[-\Delta]}}$$

Eliminating similar terms yields:

$$I_o = \frac{K e^{\left(-\frac{\Delta}{2} - n\gamma_d\right)} (e^{[n\Delta]} + e^{[(n+1)\Delta]} - e^{\Delta} - 1)}{e^{\Delta} - e^{[-\Delta]}}$$

After factoring out $e^{\left(\frac{n\Delta}{2}\right)} e^{\left(\frac{\Delta}{2}\right)}$:

$$I_o = \frac{K e^{\left(-n\gamma_d + \frac{n\Delta}{2}\right)} \left(e^{\left[\frac{(n+1)\Delta}{2}\right]} - e^{\left[\frac{(1-n)\Delta}{2}\right]} + e^{\left[-\frac{(1-n)\Delta}{2}\right]} - e^{\left[-\frac{(n+1)\Delta}{2}\right]} \right)}{e^{\Delta} - e^{[-\Delta]}}$$

Multiplying the numerator and denominator by $e^{\left(\frac{\Delta}{2}\right)} - e^{\left(-\frac{\Delta}{2}\right)}$ yields:

$$I_o = \frac{K e^{\left(-n\gamma_d + \frac{n\Delta}{2}\right)} \left(e^{\left[\frac{n\Delta}{2}\right]} - e^{\left[-\frac{n\Delta}{2}\right]} \right)}{e^{\left[\frac{\Delta}{2}\right]} - e^{\left[-\frac{\Delta}{2}\right]}}$$

After applying the identity $\sinh x = \left(\frac{1}{2}\right)(e^x - e^{(-x)})$ and replacing Delta by $\gamma_d - \gamma_g$:

$$I_o = \frac{K e^{\left[-\frac{1}{2}n(\gamma_d + \gamma_g)\right]} \sinh\left(\frac{1}{2}n(\gamma_d - \gamma_g)\right)}{\sinh\left(\frac{1}{2}\gamma_d - \frac{1}{2}\gamma_g\right)}$$

End of derivation.

BIBLIOGRAPHY

[1] Z. Lao, M. Yu, V. Ho, K. Guinn, M. Xu, S. Lee, V. Radisic, K.C. Wang; "40 Gbit/s monolithic integrated modulator driver in InP SHBT technology", Electronics Letters ,Volume: 39 , Issue: 16 , 7 Aug. 2003, Pages: 1181 – 1182

[2] M. Leich, M. Ludwig, A. Kuri, A. Hulsmann, M. Schlechtweg, "6 Vpp-66 GHz-ultrabroadband amplifier for fibre-optical transmission systems", Electronics Letters , Volume: 37, Issue: 23 , 8 Nov 2001, Pages: 1397 - 1398

[3] M. Leich, M. Ludwig, A. Hulsmann, V. Hurm, F. Steinhagen, A. Thiede, M. Schlechtweg, "40 Gbit/s high voltage modulator driver in P-HEMT technology", Electronics Letters , Volume: 35 , Issue: 21 , 14 Oct. 1999, pp:1842 – 1844

[4] D. Willems, I. Bahl, K. Wirsing, "High voltage distributed amplifier", Electronics Letters , Volume: 27 , Issue: 25 , 5 Dec. 1991,pp:2369 - 2370

[5] W. Mouzannar, F. Jorge, S. Vuye, E. Dutisseuil, R. Lefevre, "40 Gbit/s high performances GaAs pHEMT high voltage modulator driver for long haul optical fiber communications", Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 2002. 24th Annual Technical Digest , 20-23 Oct. 2002, pp:163 – 166

[6] C. Yuen, K. Laursen, Duc Chu; K. Mar, "50 GHz high output voltage distributed amplifiers for 40 Gb/s EO modulator driver application", Microwave Symposium Digest, 2002 IEEE MTT-S International , Volume: 1 , 2-7 June 2002, Pages: 481 - 484

[7] K. Takahata, Y. Muramoto, H. Fukano, Y. Matsuoka, "40-Gbit/s WGPd/HEMT monolithic photoreceiver with output voltage of 1 V_{p-p}", Communications, 1999. APCC/OECC '99. Fifth Asia-Pacific Conference on ... and Fourth Optoelectronics and Communications Conference, Volume: 2, 18-22 Oct. 1999, Pages: 1657 - 1659 vol.2

[8] K. Hagimoto, M. Yoneyama, A. Sano, A. Hirano, T. Kataoka, T. Otsuji, K. Sano, and K. Nogushi, "Limitation and challenges of single-carrier full 40-Gbit/s repeater system based on optical equalization and new circuit design," in Dig. Tech. Papers OFC'97, 1997, Pages: 242-243.

[9] M.J.W. Rodwell, M. Riazat, K.J. Weingarten, B.A. Auld, D.M. Bloom, "Internal Microwave Propagation and Distortion Characteristic of Traveling-Wave Amplifiers Studied by Electrooptic Sampling", IEEE Transactions on Microwave Theory and Techniques, vol. 34, no. 12, 1986, Pages: 1356-1362.

[10] J.B. Beyer, S.N. Prasad, R.C. Becker, J.E. Nordman, G.K. Hohen-warter, "MESFET Distributed Amplifier Design Guidelines", IEEE Transactions on Microwave Theory and Techniques, vol. 32, no. 3, 1984, Pages: 268-275.

[11] Y. Ayasli, S.W. Miller, R. Mozzi, L.K. Hanes, "Capacitively coupled traveling-wave power amplifier" IEEE Transactions on Electron Devices, vol. 31, (no. 12), 1984, Pages: 1937-42.

[12] K.H. Koo; C.W. Lee; "International Conference on Circuits and Systems", Conference Proceedings, China, 16-17 June 1991, Pages: 482 - 485 vol.2

[13] K.B. Niclas, "On Design and Performance of Lossy Match GaAs MESFET Amplifiers", IEEE Microwave Theory and Techniques Symposium Digest, 1982, Pages: 162-165.

[14] T. Arell, T. Hongmatip, "A Unique MMIC Broadband Power Amplifier Approach", IEEE Journal of Solid-State Circuits, vol. 28, no. 10, 1993, Pages: 1005-1010.

[15] P.K. Ikalainen, "An RLC Matching Network and Application in 1-20 GHz Monolithic Amplifier", Microwave Symposium Digest, IEEE MTT-S International, 1989, Pages: 1115-1118, vol.3.

[16] A.M. Pavo, "A Network Modeling and Design Method for a 2 - 18 GHz Feedback Amplifier", IEEE Microwave and Guided Wave Letters, vol. 9, no. 7, 1999, Pages: 277-279.

[17] C.J. Madden, R.L. Van Tuyl, M.V. Le, L.D. Nguyen, "A 17 dB Gain, 0.1-70 GHz InP HEMT Amplifier IC", IEEE International Solid-State Circuits Conference, 1994, Pages: 178-179.

[18] Y. Ayasli, L.D. Reynolds, R.L. Mozzi, L.K. Hanes, "2-20-GHz GaAs traveling-wave power amplifier" IEEE Transactions on Microwave Theory and Techniques, vol. 32, (no. 3), 1984, Pages: 290-5

[19] B. Agarwal, A.E. Schmitz, J.J. Brown, M. Matloubian, M.G. Case, M. Le, M. Lui, M.J.W. Rodwell, "112 GHz, 157 GHz, and 180 GHz InP HEMT Traveling-Wave Amplifiers", IEEE Transactions on Microwave Theory and Techniques, Dec. 1998, Pages:2553-2559.

- [20] E.L. Ginzton, W.R. Hewlett, J.H. Jasberg, J.D. Noe, "Distributed Amplification", Proceedings of the I.R.E, vol. 36, 1984, Pages: 956-969.

- [21] G. Ghione, C. Naldi, "Analytical Formulas for Coplanar Lines in Hybrid and Monolithic MICs," Electron. Lett., Vol. 20, No. 4, Pages: 179-181, Feb. 1984.

- [22] G. Ghione, C. Naldi, "Parameters of Coplanar Waveguides with Lower Ground Plane," Electron. Letters, Vol. 19, No. 18, Pages: 734-735, Sept. 1983.

- [23] W. Hilberg, "From Approximation to Exact Relations for Characteristic Impedances," IEEE Trans. Microwave Theory Tech., Vol. MTT-13, Pages: 29-38, Jan. 1965.

- [24] K.C. Gupta, R. Garg, and I.J. Bahl, Microstrip Lines and Slotlines, Artech House, Dedham, MA, 1979, Pages: 277-280.

- [25] K.C. Gupta, R. Garg, and R. Chadha, Computer-Aided Design of Microwave Circuits, Artech House, Dedham, MA, 1981, p. 72.

- [26] L. Divina, Z. Skvor, Z., "The distributed oscillator at 4 GHz", Microwave Theory and Techniques, IEEE Transactions on , Volume: 46 , Issue: 12 , Dec. 1998, Pages: 2240 - 2243

- [27] Z. Skvor, S.R. Saunders, C.S. Aitchison, "Novel decade electronically tunable microwave oscillator based on the distributed amplifier ", Electronics Letters , Volume: 28 , Issue: 17 , 13 Aug. 1992, Pages: 1647 - 1648

- [28] J.R. Pierce and L.M. Field, "Traveling Wave Tubes", Proceedings of IRE, vol. 35, Feb. 1947, Pages: 108-111.

[29] Jin-Wei Shi; Chi-Kuang Sun; J.E. Bowers, "Taper line distributed photodetector", Lasers and Electro-Optics Society, 2001. LEOS 2001. The 14th Annual Meeting of the IEEE , Volume: 1 , 12-13 Nov. 2001, Pages: 382 - 383 vol.1

[30] Yiwei Chen, J. Beyer, V. Sokolov, J. Culp, "A 11GHz hybrid paraphase amplifier", Solid-State Circuits Conference. Digest of Technical Papers. 1986 IEEE International , Volume: XXIX , Feb 1986, Pages:: 236 – 237

[31] Y.W. Chen, J.B. Beyer, S.N. Prasad, "MESFET wideband distributed paraphase amplifier", International Journal of Electronics, vol. 58, no. 4, 1985, Pages: 553-569.

[32] D. Levy, A. Noblet, Y.W. Bender, "A 2-18 GHz monolithic phase shifter for electronic warfare phase array applications", Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1988. Technical Digest 1988., 10th Annual IEEE , 6-9 Nov. 1988, Pages: 265 – 268

[33] D. M. Pozar, Microwave Engineering, Addison Wesley Publishing Company, Ind., Reading MA, 1990.

[34] D.G. Sarma, "On distributed amplification," Proc. IEEE, vol. 102B, Pages: 689-697, 1954.

[35] T.Y. Wong, Fundamentals of distributed amplification, Artech House, 1993.

[36] C.S. Aitchison, "The intrinsic noise figure of the MESFET distributed amplifier", IEEE Trans. on Microwave Theory and Techniques, vol. MTT-33, Pages: 460-466, June 1985.

[37] B. Kim, H.Q. Tserng, "High Power Distributed Amplifier Using MBE Synthesized Material", IEEE Microwave and Millimeter-wave Monolithic Circuits Symposium Digest, 1985, Pages: 35-37

[38] R. Halladay, A.M. Pavio, C. Crabill, "A 1-20 GHz dual gate distributed power amplifier", IEEE Gallium Arsenide Integrated Circuit Symposium Digest, Pages: 219-22, 1987.

[39] J. Pusi, B. Agarwal, R. Pullela, L.D. Nguyen, M.V. Le, M.J.W. Rodwell, L. Larson, J.F. Jensen, R.Y. Yu, M.G. Case, "Capacitive-Division Traveling-Wave Amplifier with 340 GHz Gain-Bandwidth Product", IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest, 1995, Pages: 175-178.

[40] P.H. Ladbrooke, "Large-signal criteria for the design of GaAs FET distributed power amplifiers", IEEE Transactions on Electron Devices, vol. 32, no. 9, 1985, 1745-1748.

[41] M. Campovecchio, B. Le Bras, M. Lajugie, J. Obregon, "Optimum Design of Distributed Power-FET Amplifiers: Application to a 2 - 18 GHz MMIC Module Exhibiting Improved Power Performances", IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest, 1994, Pages: 125-128.

[42] R. Halladay, M. Jones, S. Nelson, (Edited by: C. Huang), "A producible 2 to 20 GHz monolithic power amplifier" IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest, 1987, Pages: 19-21.

[43] Q. Xia, Investigation of GaAs pHEMT Distributed Amplification for Broadband Modulator Driver Applications, Master Thesis, Carleton University, 2003.

[44] S. D'Agostino, C. Paoloni, "Comparison between MMIC matrix and distributed amplifiers", IEE Proceedings on Microwaves, Antennas and Propagation, Volume: 142, Issue: 1, Feb. 1995, Pages: 75 – 77

[45] H.T. Ahn; D.J. Allstot, "A 0.5-8.5 GHz fully-differential CMOS RF distributed amplifier", Southwest Symposium on Mixed-Signal Design, 27-29 Feb. 2000, Pages: 109-112

[46] C. Yuen, K. Laursen, Duc Chu; K. Mar, "50 GHz high output voltage distributed amplifiers for 40 Gb/s EO modulator driver application", Microwave Symposium Digest, 2002 IEEE MTT-S International, Volume: 1, 2-7 June 2002, Pages: 481 - 484

[47] L. Zhihao, A. Thiede, U. Nowotny, H. Lienhart, V. Hurm, M. Schlechtweg, J. Hornung, W. Bronner, K. Kohler, A. Hulsman, B. Raynor, T. Jakobus, "40-Gb/s high-power modulator driver IC for lightwave communication systems", IEEE Journal of Solid-State Circuits, Volume: 33, Issue: 10, Oct. 1998, Pages: 1520 - 1526

[48] E.S. Shapiro, J. Xu, A.S. Nagra, F. Williams Jr., U.K. Mishra, R.A. York, "A high-efficiency traveling-wave power amplifier topology using improved power-combining techniques", IEEE Microwave and Guided Wave Letters, vol. 8, no. 3, Pages: 133-5, 1998.

[49] J.J. Xu, Y-F. Wu, S. Keller, G. Parish, S. Heikman, B.J. Thibeault, U.K. Mishra, R.A. York, "1-8 GHz GaN Based Power Amplifier Using Flip-Chip Bonding", IEEE Microwave and Guided Wave Letters, vol. 9, no. 7, 1999, Pages: 277-279.

[50] M. N. Yoder, "Distributed, monolithic traveling-wave amplifiers", International Journal of Electronics, vol. 58, no. 4, 1985, Pages: 543-551.

[51] Y. Baeyens, G. Georgiou, J.S Weiner, A. Leven, V. Houtsma, P. Paschke, Q. Lee, R.F. Kopf, Y. Yang; L. Chua, C. Chen, C.T. Liu, Young-Kai Chen; "InP D-HBT ICs for 40-Gb/s and higher bit rate lightwave transceivers", IEEE Journal of Solid-State Circuits, Volume: 37 , Issue: 9 , Sep 2002, Pages: 1152 - 1159

[52] K. Minot, B. Nelson, W. Jones, "A low noise, phase linear distributed coplanar waveguide amplifier", IEEE Trans. on Microwaves Theo. and Tech., Vol. 41, 9, 1993.

[53] Kun-You Lin; Luo-Liang Deng; Po-Wei Kuo; Shin-Der Yang; Huei Wang; Tah-Hsiung Chu; "K-Band monolithic GaAs PHEMT amplifiers", Microwave Conference, 2000 Asia-Pacific , 3-6 Dec. 2000, Pages: 153 – 156

[54] E. Legros, A. Merrar, M. Billard, C. Joly, P. Blanconnier, "Low noise 20 Gbit/s photoreceiver with distributed GaAs P-HEMT amplifiers", Electronics Letters , Volume: 32 , Issue: 18 , 29 Aug. 1996, Pages: 1693

[55] N. Camilleri, P. Chye, A. Lee, P. Gregory, "Monolithic 9 to 70 GHz distributed amplifier", IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1990. Digest of Papers., 7-8 May 1990, Pages: 27 – 30

[56] P.H. Ladbrooke, MMIC Design GaAs FETs and HEMTs, Artech House, 1989.

[57] K. W. Kobayashi et al., "A 6-21 GHz Monolithic HEMT 2 x 3 Matrix Distributed Amplifier," IEEE Microwave and Guided Wave Letters, Vol. 3, Pages: 11-13, Jan. 1993.

[58] M. Miyashita et al., "An AlGaAs/InGaAs Pseudomorphic HEMT Modulator Driver IC with Low Power Dissipation for 10-Gb/s Optical Transmission Systems", IEEE Tran. Microwave Theory Tech., Vol. 45, Pages: 1058-1064, July 1997.

[59] Z. Lao et al., "40-Gb/s High-Power Modulator Driver IC for Lightwave Communication Systems", IEEE Journal of Solid-state Circuit, Vol. 33, Pages:1520-1526, Oct. 1998.

[60] S. Kimura et al., "0 - 40 GHz GaAs MESFET Distributed Baseband Amplifier IC's for High-Speed Optical Transmission", IEEE Tran. Microwave Theory Tech., Vol.44, Pages: 2076-2680, 1996.

[61] R.Heilig et al. "A Monolithic 2-52 GHz HEMT Matrix Distributed Amplifier in Coplanar Waveguide Technology," IEEE MTT-s Digest, Pages: 459-462, 1994.

[62] Y. Ayasli, L.D. Reynolds, R.L. Mozzi, L.K. Hanes, "2-20 GHz GaAs Traveling-wave power amplifier", IEEE Trans. On Microwave Theory and Techn., Vol MTT-32, No.3, March 1984, Pages: 290-295

[63] A. Thiam, E. Legros, S. Vuye, P. Andre, E. Wawrzynkowski, C. Joly, "40 Gbit/s GaAs P-HEMT driver module for optical communications", Electronics Letters, Vol.34, No. 23, Nov. 1998, Pages:2232-2234.

[64] B.J. Minnis, Designing microwave circuits by exact synthesis, Artech House, 1996, Pages:249.

[65] T. Wong, Fundamentals of Distributed Amplification, Artech House, 1993, p.101

[66] Y. Ayasli, R.L. Mozzi, J.L. Vorhaus, L.D. Reynolds, R.A. Pucel, "A Monolithic GaAs 1-13-GHz Traveling-Wave Amplifier", IEEE Transactions on Microwave Theory and Techniques, Volume: 82 , Issue: 7 , Jul 1982, pp:976 – 981

[67] J. L.B. Walker, High-Power GaAs FET Amplifier. Artech House, 1993.

[68] D. Pozar, Microwave Engineering, 2nd Ed. John Wiley, 1998

[69] J. Smith, Modern Communication Circuits, 2nd Ed. McGraw-Hill, 1998